AN ABSTRACT OF THE DISSERTATION OF

Youngho Jung for the degree of Doctor of Philosophy in Electrical and Computer Engineering, presented on August 13, 2014.

Title: Wideband and High Accuracy Delta Sigma Modulation Data Converter

Abstract approved: _____

Gabor. C. Temes

Nowadays, needs for wideband and high accuracy analog-to-digital converter are increasing rapidly in manifold applications such as wireless communication, digital video and other consumer electronics. Besides, low power consumption is required to have longer battery life in portable systems. CMOS technology scaling and innovative modulator topology make the implementation much easier and practicable.

In this dissertation, first, various incremental ADCs are discussed and analyzed. Incremental ADC with extended counting and 2+2 MASH incremental ADC were designed and fabricated in 0.18μm 2P4M CMOS process to achieve wide bandwidth, high accuracy, and low latency. Incremental ADC with extended counting ADC achieves 91.6dB dynamic range and 77.8dB peak SNDR with 1.25MHz signal band. The total power consumption is 53.5mW. 2+2 MASH incremental ADC achieves 94.2dB dynamic range and 74.8dB peak SNDR up to 1.25MHz signal band. The total power consumption is 67mW.

Secondly, feedback timing relaxed ΔΣ ADC with noise coupling was proposed. Because of the relaxed the feedback timing, we are able to use the low speed comparator

and DEM circuitry resulting in low power consumption. Two slightly different prototypes were implemented in 0.18μm 2P4M CMOS process. Sampling capacitor is separated from DAC capacitor in prototype A while they are shared in prototype B. Even if prototype B has half of kT/C noise than prototype A due to the less capacitor at the input branch of the modulator, prototype B suffers from signal dependent reference error. Measurement results of prototype A achieves 90.5dB dynamic range, 81.2dB peak SNDR with 2.1MHz signal band. On the other hand, prototype B achieves 95.6dB dynamic range, 74.2dB peak SNDR up to 2.1MHz signal band under same test environment. Both of two prototypes consume 98mW. Based on the measurement results, prototype B where sampling capacitor is shared with DAC capacitor suffers from higher harmonic distortion than prototype A.

Finally, double noise coupled ΔΣ modulator was proposed. The proposed architecture is less sensitive to finite opamp DC gain effects and complex on clock generator design than the second order noise shaping ΔΣ modulator.

WIDEBAND AND HIGH ACCURACY DELTA SIGMA MODULATION DATA CONVERTER

by

Youngho Jung

A DISSERTATION

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Doctor of Philosophy

Presented August 13, 2014
Commencement June 2015

Doctor of Philosophy dissertation of Youngho Jung presented on August 13, 2014

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I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Youngho Jung, Author

ACKNOWLEDGEMENTS

First of all, I would like to express my deep gratitude to my advisor, Professor Gabor C. Temes. He gave me a big chance to do research under his advisory. It would be impossible for me to finish this Ph.D. work without him. He always gave me a lot of inestimable advice and kind support on my research and personal life. He is the most admirable professor who I have ever seen. I will remember his enthusiasm for research and teaching forever. Special thanks to Professor Patrick Chiang for giving a chance to study at OSU.

I also appreciate following Ph.D. program committee members: Professor Un-Ku Moon, Professor Arun Natarajan, Professor Raviv Raich, Professor Maggie Niess, Professor Wade Marcum, Professor Huaping Liu, Professor Karti Mayaram, Professor Thinh Nguyen, and Professor Adam Schultz. They offered their valuable time and advice for my Ph.D. program. In addition to committee professor, Professor Pavan Hanumolu always gave me good answers about various questions.

Thank you to AKM for supporting my research. A special thanks to Koichi Hamashita, Kazuki Sobue, and Mitsuru Aniya of AKM for supporting my research and the chip fabrication.

I would like to express my gratitude to many research group members present and past: Ming-Hung Kuo, Wenhuan Yu, Yan Wang, Weilun Shen, Tong Tao, Wang Tao, Wei Li, Po-Yao Ke, Jiaming Lin, Chia-Hung Chen , Sanghyeon Lee, Jeongseok Chae, Yi Zhang, Pedram Payandeh Nia, Tao He, Xin Meng, Jinzhou Cao, Mahmoud Sadollahi, Ali Fazli Yeknami, Tasnim Ferdous without specific order in mind. Specially, I would like to

thank to Sanghyeon Lee and Jeongseok Chae. When I arrived at Corvallis in 2009, Sanghyeon Lee and Jeongseok Chae helped me to settle and gave me valuable discussion and advice about my research and personal difficulties. I am also specifically thankful to Chia-Hung Chen and Tao He for their deep technical support and personal conversations with me.

I am indebted to many colleagues in analog and mixed-signal group of OSU, Jeff Pai, Brian Young, Sachin Rao, Hari Prasath Venkatram, Yue (Simon) Hu, Jiao Cheng, Kangmin Hu, Mattew Brown, Seokmin Jung, Seongjoong Kim, Wooseok Choi, Hoyoung Lee, Taehwan Oh, and Hyuk Sun who helped me broaden my knowledge and supported me as a colleague. Also, in no specific order, thanks for Professor Ben Lee, Professor Byong-Deok Choi, Professor Kwangho Shin, Professor In-soo Shon, Roderick Hwang, Younghoon Hwang, Jongbum Ryu for helps and advices.

Thanks to all members of Korean Presbyterian Church at Corvallis for their sharing love of God.

I would like to thank to Ferne Simendinger, Colisse Franklin, Nicole Thompson, Todd Shechter, Renee Lyon, and Gillian Yu for all their supports.

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DEDICATION

I would like to express my heartfelt gratitude to my family for their sacrifice and unconditional love. I would like to dedicate this dissertation to my parents, Kwangjin Jung and Soonja Han, my mother-in-law, Byungjoo Kwon. My parents always have done their best to support their family in their life. Also they showed me an endless love and sacrifice. My adored mother-in-law gave me a deep faith and encouragement. This work was made possible with the priceless sacrifice and patience of my beloved and treasured wife, Eunsoo Choi. I wouldn't have been able to finish my Ph.D. work without her encouragement and devoted support. I would like to thank my adorable daughter, Yooeun, for health, love and brightness.

To my parents Kwangjin Jung and Soonja Han,

my mother-in-law Byungjoo Kwon,

my wife Eunsoo Choi,

my daughter Yooeun

WIDEBAND AND HIGH ACCURACY DELTA SIGMA MODULATION DATA CONVERTER

CHAPTER 1. INTRODUCTION

1.1 Motivation

Analog-to-digital converter links between analog world and digital world of signal processing and data handling. Therefore, both analog-to-digital conversion as well as digital-to-analog conversion is essential function for taking advantage of digital processing. Among the various types of ADCs, delta sigma ADCs have been utilized for high accuracy conversion with the aid of oversampling and noise shaping. Typical application of the delta sigma ADCs contains measurement, biosensor, and audio for low bandwidth and high accuracy. However, nowadays, needs for wideband and high accuracy analog-to-digital converter are increasing rapidly in manifold applications such as wireless communication, digital video and other consumer electronics. Besides, low power consumption is required to have longer battery life in portable systems. CMOS technology scaling and innovative modulator topology make the implementation much easier and practicable.

In this dissertation, incremental analog-to-digital converters are designed and analyzed to reduce the complexity of the digital filter. Also, a novel delta sigma topology is

proposed to achieve wideband and high accuracy. Both incremental ADC and conventional ΔΣ modulator with the new scheme are fabricated and measured.

1.2 Contributions

- Incremental ΔΣ modulator was analyzed and compared with conventional ΔΣ modulator.
- Incremental ΔΣ modulator with extended counting was designed and fabricated in $0.18\mu m$ 2P4M CMOS process.
- 2+2 MASH (Multi-Stage Noise Shaping) incremental ΔΣ modulator was designed and fabricated in $0.18\mu m$ 2P4M CMOS process.
- ΔΣ ADC with relaxed feedback timing is proposed to achieve wideband and high accuracy. Two slightly different prototypes were designed and fabricated in $0.18\mu m$ 2P4M CMOS process.
- A novel double noise coupling delta-sigma topology is proposed. The new topology is less dependent on the opamp DC gain than the earlier ΔΣ modulator with second-order noise shaping enhancement. Also, the proposed architecture reduces the complexity of the clock generator.

1.3 Organization of dissertation

Chapter 2 reviews operation principle and analysis of the conventional ΔΣ modulator

and incremental analog to digital converter. Chapter 3 describes design and measurement results of two different incremental analog-to-digital converters to achieve wide band, high accuracy and low latency. One is the incremental ΔΣ ADC with extended counting. The other one is 2+2 MASH (Multi-Stage Noise Shaping) incremental ΔΣ ADC. Chapter 4 discusses the ΔΣ modulator with relaxed feedback timing. To verify the proposed idea, two slightly different prototypes were designed and measured. Chapter 5 describes the proposed double noise coupled ΔΣ modulator. Chapter 6 summarizes the contribution of this research and concludes the dissertation.

CHAPTER 2. OVERSAMPLING ADC AND INCREMENTAL ADC

Nowadays, most electronic systems process signals in digital domain. Because, digital circuits are less sensitive to noise, supply fluctuation, and process variations, etc. However, the signals such as voice, human body signal and communication signal in the real world are all analog form. Therefore analog-to-digital and digital-to-analog converters are essential blocks in the system [2.1]. Analog-to-digital converters can roughly be split into two families. The first family is one of memoryless high speed and medium accuracy converters, also referred to as Nyquist converters. Its accuracy depends on the analog circuit imperfection such as mismatch and noise, even if there are several calibration techniques to overcome those limitations. The second family is the one of memorized high accuracy and low speed converters, often referred to as oversampled converters, typically used for audio and low MHz range. Fig. 2.1 shows the trade-off between signal bandwidth and SNDR (Signal-to-Noise-and-Distortion Ratio) in various ADC architectures [2.2]. Although oversampled converters can easily achieve high accuracy with the help of oversampling and noise shaping, the signal bandwidth is limited as a consequence of the oversampling. Recently, the needs for wired and wireless communication systems, digital video and other consumer electronics are requiring wideband and high resolution data converters. For signal bandwidth around 10 MHz, delta sigma analog to digital converters have often been used in these system [2.3-5]. At the same time, there is increasing demand for low power consumption data converters for portable systems [2.6].

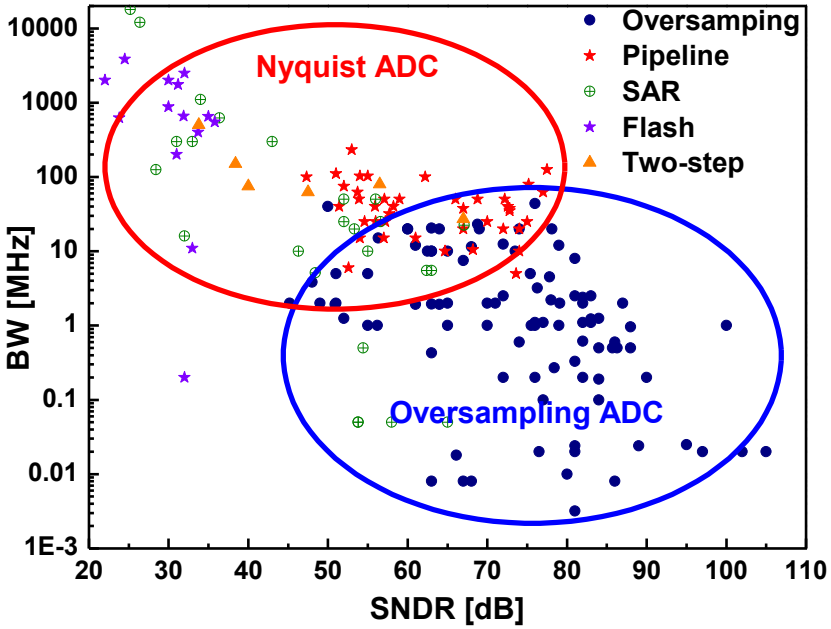


Fig. 2.1 Various ADC architectures and performance.

2.1 Oversampling analog-to-digital converters

Fig. 2.2 shows the concept of the quantization noise and its linear model. Let us assume the input signal *U* is a ramp. Such an input signal results in *Y* appearing as a staircase. Taking the difference between these two signal (*U* and *Y*) gives us the noise signal *E* called quantization error. The quantization error is unavoidable fundamental limit of the quantization process. It becomes zero only when the number of bit, quantization resolution, goes to infinity, which is infeasible in practice [2.7]. If the input signal stays within the input range of the quantizer and changes by sufficiently large amounts from sample to sample so that its position within a quantization interval is

essentially random, then it is permissible to assume that *E* is a white noise with samples uniformly distributed between -Δ/2 and Δ/2 [2.8]. Also, in order to make the analysis tractable, the quantizer is often linearized by using an input independent additive white noise model, as shown in Fig. 2.2.

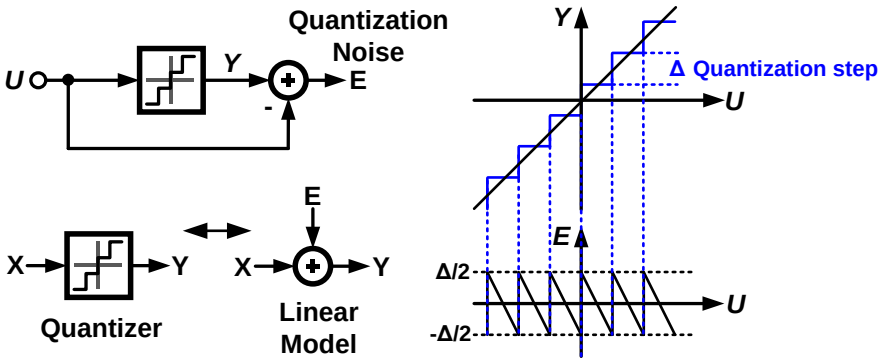


Fig. 2.2 Quantization noise.

Fig. 2.3 shows the noise power spectral densities of the Nyquist and oversampling ADC. If we assume that the quantization noise is uniformly distributed from $-f_s/2$ to $f_s/2$, the Nyquist ADC's total quantization noise power in signal band is $\Delta^2/12$. However, the quantization noise in oversampling ADC spread out from $-OSR \cdot f_s/2$ to $OSR \cdot f_s/2$. Here, OSR (Over Sampling Ratio) is defined the ratio between the sampling rate and two times the signal bandwidth. Since the signal of the interest is between $-f_s/2$ to $f_s/2$, the out of signal band quantization noise is eliminated after low-pass filtering. Therefore, the total quantization noise power in signal band is divided by OSR, $(\Delta^2/12)/OSR$. It means doubling OSR gives a total quantization noise reduction in signal band by 3dB. Although oversampling gives a SNR (Signal-to-Noise Ratio) of 3dB/octave, a large quantity of quantization noise still remains in the signal band.

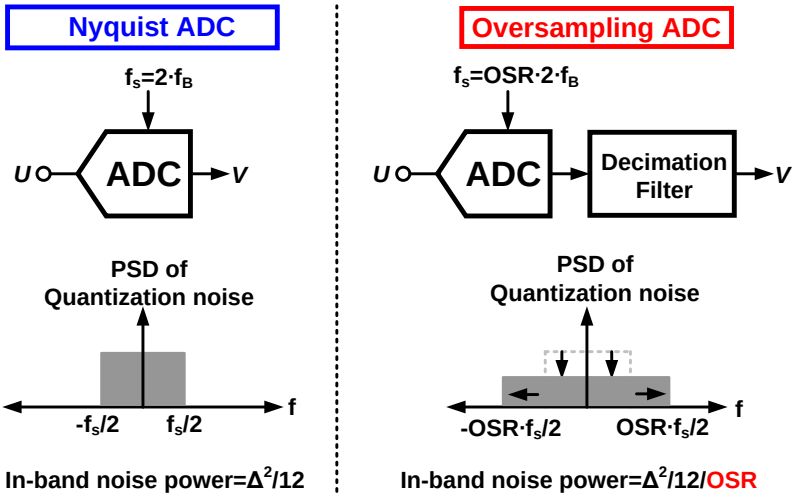


Fig. 2.3 PSD of the nyquist and oversampling ADC.

How to reduce more? The basic idea is to combine the current quantization noise and delayed one. Because, at the low frequency (in-band), the delayed quantization noise is almost same as current one, if subtraction is done, the quantization noise would be cancelled [2.9]. This is called noise-shaping which is a very effective way to reduce the quantization noise more in the signal band. Fig. 2.4 shows the procedure of the noise shaping. Here, $(1-z^{-1})$ means the difference the current state's quantization noise and delay one in time domain. As mentioned before, total quantization noise in the signal band is reduced evidently. Having more noise in high frequency regions is not problematic since the digital filter after modulator removes it. Therefore, noise shaping changes the white noise spectrum of the quantization noise into a shaped spectrum as shown in Fig. 2.4.

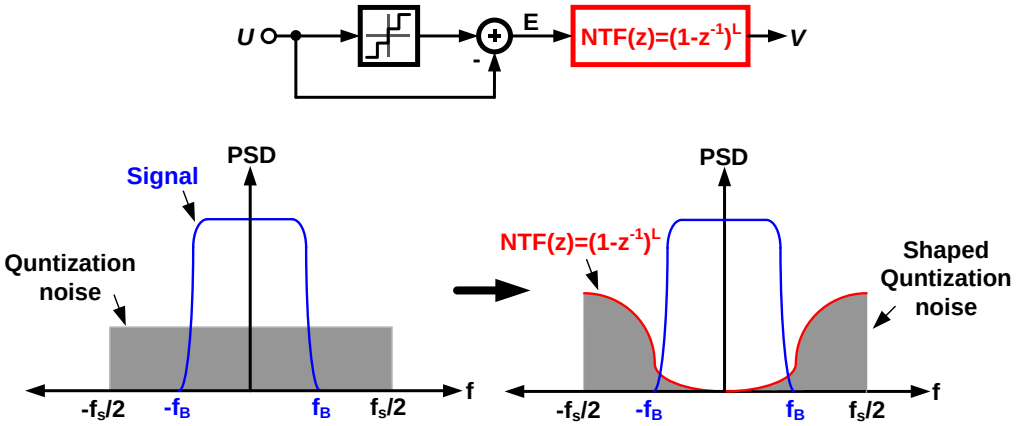


Fig. 2.4 Noise shaping procedure.

Fig. 2.5 shows the implementation of the noise shaping. In this structure, the quantizer is placed in the feedback loop. Eqs. (1) and (2) show the signal transfer function and noise transfer function respectively. If the frequency band of interest is around DC (form 0 to f_B) and choose H(z) to be large from 0 to f_B (in-band frequency), signal transfer function (STF) is almost 1 and noise transfer function (NTF) is almost zero. In other words, the signal is low-pass filtered and the quantization noise is high-pass filtered as we desire. Since the scheme of Fig. 2.5 is the integration (Σ) of the difference (Δ), the modulator is named ΔΣ modulator.

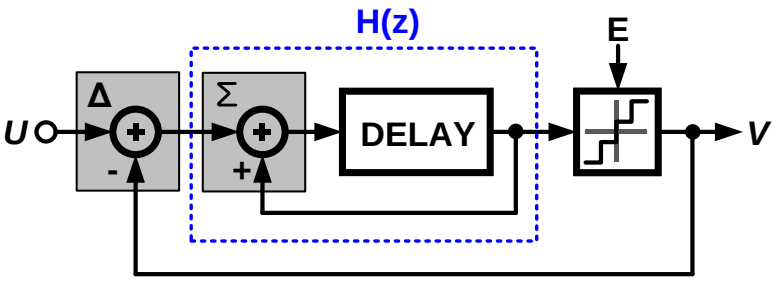


Fig. 2.5 Implementation of noise shaping.

$$STF(z) = \frac{V(z)}{U(z)} = \frac{H(z)}{1 + H(z)} \tag{2.1}$$

$$NTF(z) = \frac{V(z)}{E(z)} = \frac{1}{1 + H(z)} \tag{2.2}$$

Fig. 2.6 shows the structure for the first order ΔΣ modulator and its noise shaping. To realize the first-order noise shaping, the noise transfer function, NTF(z), should have a zero at DC (i.e z=1) so that the quantization noise is high-pass filtered as we desire. We can obtain first-order noise shaping by letting the loop filter, H(z) be a discrete-time integrator.

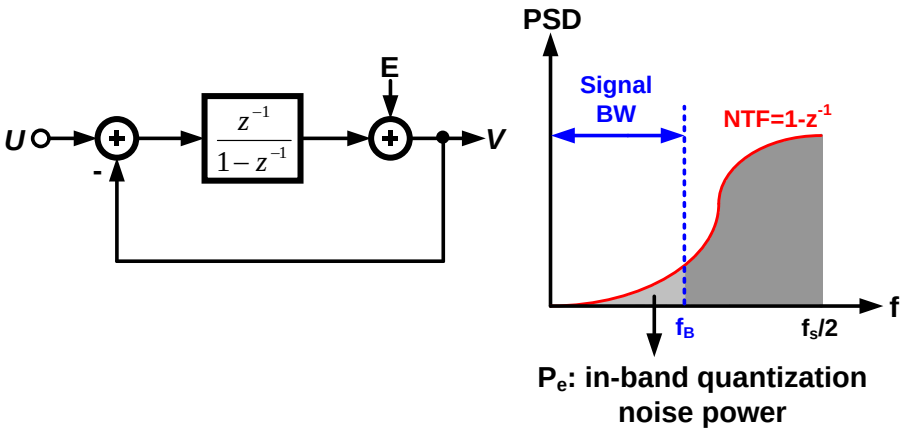


Fig. 2.6 First order ΔΣ modulator and its noise shaping.

The total quantization noise power in signal band and maximum achievable SNR for this case is given by

$$P_e \approx \left(\frac{\Delta^2}{12}\right) \cdot \left(\frac{\pi^2}{3}\right) \cdot \left(\frac{1}{OSR}\right)^3 \tag{2.3}$$

$$SNR_{max} \approx 6.02 \cdot N + 1.76 - 5.17 + 30 \cdot \log(OSR) \tag{2.4}$$

We see here that the doubling OSR gives a SNR improvement by 9 dB or, equivalently, a gain of 1.5bits/octave. Fig. 2.7 shows structure for L[th] order noise shaping for more general case [2.8]. Increasing the order of the filter H(z) leads to an increase of the order of NTF(z) under stable condition, resulting in a more effective cancellation of the quantization noise in signal band.

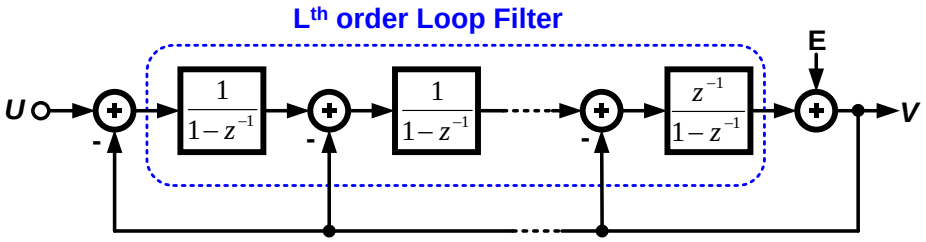


Fig. 2.7 L[th] order ΔΣ modulator.

In this case, the noise transfer function is given by

$$NTF(z) = \frac{V(z)}{E(z)} = (1 - z^{-1})^L \tag{2.5}$$

If the OSR is large enough, the total quantization noise power in in-band and maximum achievable SNR is given by

$$P_e \approx \left(\frac{\Delta^2}{12}\right) \cdot \left(\frac{\pi^{2L}}{2L+1}\right) \cdot \left(\frac{1}{OSR}\right)^{2L+1} \tag{2.6}$$

$$SNR_{max} \approx 6.02 \cdot N + 1.76 + (20L + 10) \cdot \log_{10}(OSR) - 10\log_{10}(\frac{\pi^{2L}}{2L+1}) \qquad (2.7)$$

In Eq. (2.7), the first two terms are obtained by quantizer resolution and the last two terms provide additional SNR improvement with the help of oversampling and noise-shaping. Generally speaking, doubling OSR increases SNR by $(6L + 3dB)$, or $(L + 0.5bit/octave)$ equivalently.

2.2 Incremental analog-to-digital converters

Delta sigma ADC with oversampling and noise shaping is well-known analog-to-digital converter to achieve high accuracy. These converters are mainly used for communication and consumer electronics such as cell phone, video camera, and cable modem etc. In these applications, a running waveform is digitized continuously because the spectral behavior such as dynamic range and signal-to-noise (SNR) is important. On the other hand, in instrumentation and measurement applications such as senor and digital voltmeters, individual sample's digitization is critical. To realize one-to-one mapping between input and output samples and high accuracy, incremental ADC is a good candidate. Incremental data converters operated on a similar principle to ΔΣ modulator but are reset periodically. In other words, in contrast to conventional ΔΣ modulator, it does not operate continuously. Also, analog and digital integrators are reset after each conversion cycle. The big advantage of incremental ADC is the implementation of the decimation filter is much simpler than conventional ΔΣ modulator

[2.10]. Fig. 2.8 shows the first order increment ADC and its timing diagram as a simple example [2.11].

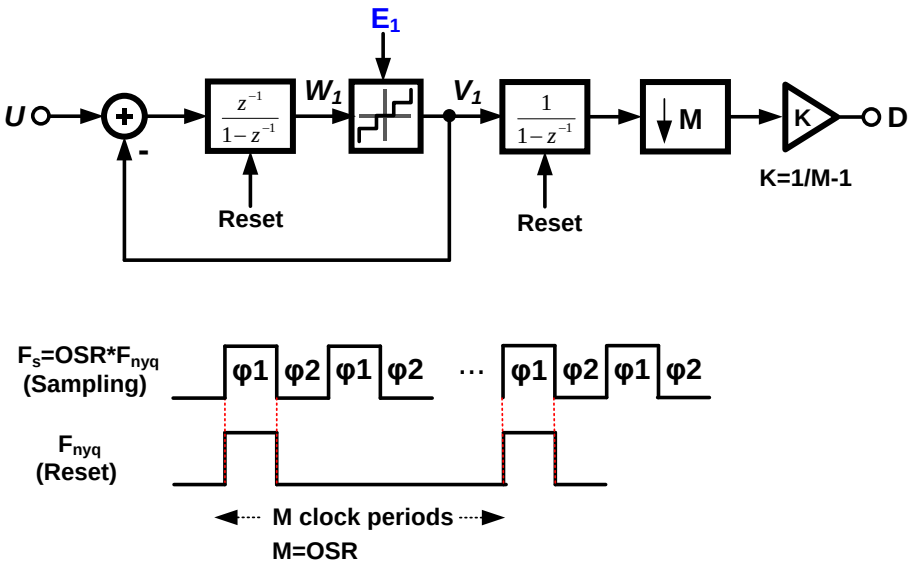


Fig. 2.8 First order incremental ΔΣ modulator.

After M clock period, output of the integrator, W_1 is expressed as

$$W_1[M] = \sum_{L=1}^{M-1} U[i] - \sum_{L=1}^{M-1} V_1[i] \tag{2.8}$$

Digital output (V_1) of the modulator with linear quantizer model can be expressed as

$$W_1[M] + E_1[M] = V_1[M] \tag{2.9}$$

If we assume that the input signal U is slow or S/H at the input, the average of the input

signal is

$$\bar{u} = \frac{1}{M-1} \cdot \sum_{i=1}^{M-1} U[i] \tag{2.10}$$

Rewriting Eq. (2.8) with Eq. (2.9) is

$$\sum_{L=1}^{M-1} U[i] - \sum_{L=1}^{M-1} V_1[i] + E_1[M] = V_1[M] \tag{2.11}$$

Substituting with Eq. (10), we can derive the design equation of the first order incremental ADC as shown in Eq. (2.12)

$$\bar{u} + \frac{1}{M-1} \cdot E_1[M] = \frac{1}{M-1} \cdot \sum_{i=1}^{M} V_1[i] \tag{2.12}$$

Therefore, equivalent quantization noise of the first order incremental ADC is

$$E_{IDC} = \frac{1}{M-1} \cdot E_1[M] \tag{2.13}$$

where M is the oversampling ratio and E_1 is the internal quantization noise. With calculated equivalent quantization noise, first order incremental ADC can be modeled as

Nyquist ADC as shown Fig. 2.9.

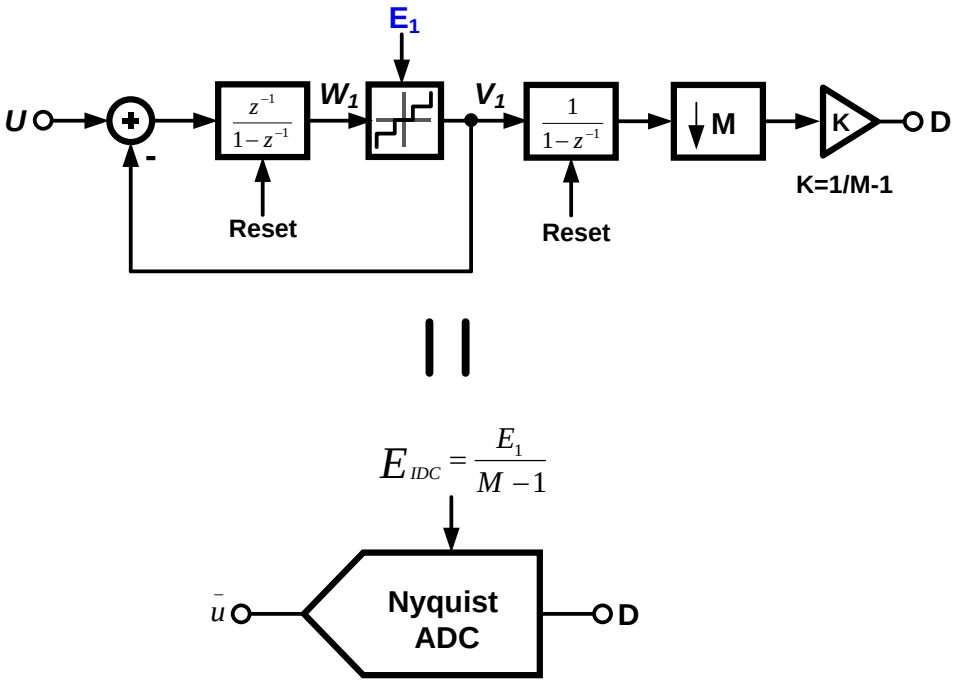


Fig. 2.9 Equivalent model of the first order incremental ΔΣ modulator.

Also, based on the Eq. (2.13), signal to quatization noise (SQNR) with N-bit internal quantizer can be estimated as

$$SQNR = 20 \cdot log_{10}\left(\frac{V_{REF}}{E_{IDC}}\right)$$

$$= 20 \cdot log_{10}\left(\frac{V_{REF}}{\frac{1}{M-1} \cdot \frac{V_{REF}}{2^N}}\right)$$

$$= 20 \cdot log_{10}[(M-1) \cdot 2^N)] \qquad (2.14)$$

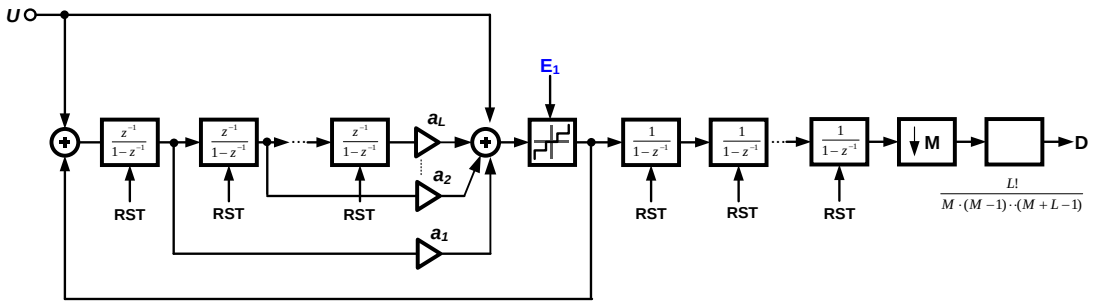


Fig. 2.10 L[th] order incremental ΔΣ modulator.

For the more general case, the equivalent quantization noise of the L[th] order incremental ADC with N-bit internal quantizaer as shown in Fig. 2.10 can be expressed as

$$E_{IDC} = \frac{L!}{M \cdot (M+1) \cdots (M+L-1)} \cdot E_1[M] \tag{2.15}$$

Therefore, the achievable maximum SQNR is

$$SQNR = 20 \cdot log_{10}\left(\frac{V_{REF}}{E_{IDC}}\right)$$

$$= 20 \cdot log_{10}\left(\frac{M \cdot (M+1) \cdots (M+L-1)}{L!} \cdot 2^N\right) \tag{2.16}$$

References

[2.1] H. V. D. Ploge and B. Nauta, "Calibration Techniques in Nyquist A/D Converters," *Springer*, 2006.

[2.2] B. Murmann, "ADC Performance Survey 1997-2010," [Online] Available at: http://www.stanford.edu/~murmann/adcsurvey.html

[2.3] M. Park and M. H. Perrott, "A 0.13 μm CMOS 78 dB SNDR 87 mW 20 MHz BW CT ΔΣ ADC with VCO-based integrator and quantizer," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 170-171, Feb. 2009.

[2.4] K. Reddy, S. Rao, R. Inti, B. Young, A. Elshazly, M. Talegankar, and P. K. Hanumolu, "A 16mW 78dB-SNDR 10MHZ-BW-CT ΔΣ ADC using residue-cancelling VCO-based quanizer," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 152-153, Feb. 2012.

[2.5] R. Kaald, B. Hernes, C. Holdo, F. Telsto, and Ivar Lokken, "A 500MS/s 76dB SNDR continuous time delta sigma modulator with 10MHz signal bandwidth in 0.18 μm CMOS," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, pp. 1-4, Sep. 2013.

[2.6] Y. Wang, P. K. Hanumolu, and G. C. Temes, "Design techniques for wideband discrete-time delta-sigma ADCs with extra loop delay," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 58, no. 7, pp. 1518-1530, Jul. 2011.

[2.7] F. Maloberti, "*Data Converters*," *Springer*, 2007.

[2.8] R. Schreier and G. C. Temes, "*Understanding of Delta-Sigma Data Converters"*, New York: Wiley, 2005.

[2.9] A. Vazquez and F. Medeiro, “Low-Pass Sigma-Delta Modulator: Princiles and Architectures,” *Lecture Note of Design of Embeddable Data Converters*: Sigma-Delta Converters at Universidad de Sevilla.

[2.10] J. Markus, J. Silva, G. C. Temes, “Theory and applications of incremental ΔΣ converters,” *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 51, no. 4, pp. 678-690, Apr. 2004.

[2.11] T.C. Caldwell, D. A. Johns, “Incremental data converters at low oversampling ratio,” *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 57, no. 7, pp. 1525-1537, Jul. 2010.

CHAPTER 3. INCREMENTAL ΔΣ ADC WITH EXTENDED COUNTING AND 2+2 MASH INCREMENTAL ΔΣ ADC

This chapter describes two kinds of incremental analog to digital converters which achieve low latency, wideband and high accuracy. One is the incremental ADC with SAR ADC for extended counting and the other one is 2+2 MASH (Multi Stage Noise Shaping) incremental ADC. Two protoypes were fabricated with 0.18*um* CMOS process and measured.

3.1 Introduction

Delta sigma ADC provides high accuracy with the aid of oversampling and noise shaping even using inaccurate analog components [3.1]. There are several design parameters: quantizer resolution, loop filter order, and oversampling ratio. Increasing any of these parameters will improve the resolution of the ADC. For wideband applications, increasing OSR is limited by the bandwidth of the amplifiers and power consumption.

At low OSR, higher oreder noise shaping and higer quantizer level is better way to achieve the high accuracy taking advantage of delta sigma ADC. However, higher order modulator can cause stability problem due to increase of the signal swing. Also, the number of quantizer level is limited by the linearity requirement in the feedback DAC.

Therefore, a cascaded modulator can overcome this drawback by utilizing high

resolution multi-bit quantizer in the second stage [3.2,3].

Section 3.2 analyzes the incremental ADC with extended couting and derives the design equations for optimal digital filter. Section 3.3 discusses the proposed incremental ADC with extended counting for wideband and high accuracy. Section 3.4 presents a hardware prototype implemented in 0.18*um* CMOS process. Section 3.5 describes the measurement results of the prototype. Section 3.6 discusses about 2+2 MASH incremental ΔΣ ADC and measurement results follow in Section 3.7.

3.2 Incremental ΔΣ ADC with extended counting

The accuracy of an incremental ADC can be increased by means of a technique called extended counting. [3.4,5,6]. An example of incremental ADC with extended counting is shown in Fig. 3.1 [3.7]. At the end of *M* (=OSR) clock cycle, the quantization noise (E_1) of the first loop will be stored at the output of the second integrator. After M clock period W_2 is

$$W_2[M] = \sum_{L=1}^{M-1}\sum_{i=1}^{L-1} U[i] - \sum_{L=1}^{M-1}\sum_{i=1}^{L-1} V_1[i] \tag{3.1}$$

The digital output of the second ADC with linear quantizer model can be expressed as

$$W_2[M] + E_2[M] = D_2 \tag{3.2}$$

Combination of Eq. (3.1) and Eq. (3.2) gives

$$\overline{u} + \frac{2}{(M-1)\cdot(M-2)} \cdot E_2[M] = \frac{1}{(M-1)\cdot(M-2)} \left\{ \sum_{L=1}^{M-1} \sum_{i=1}^{L-1} V_1(i) + D_2 \right\} \tag{3.3}$$

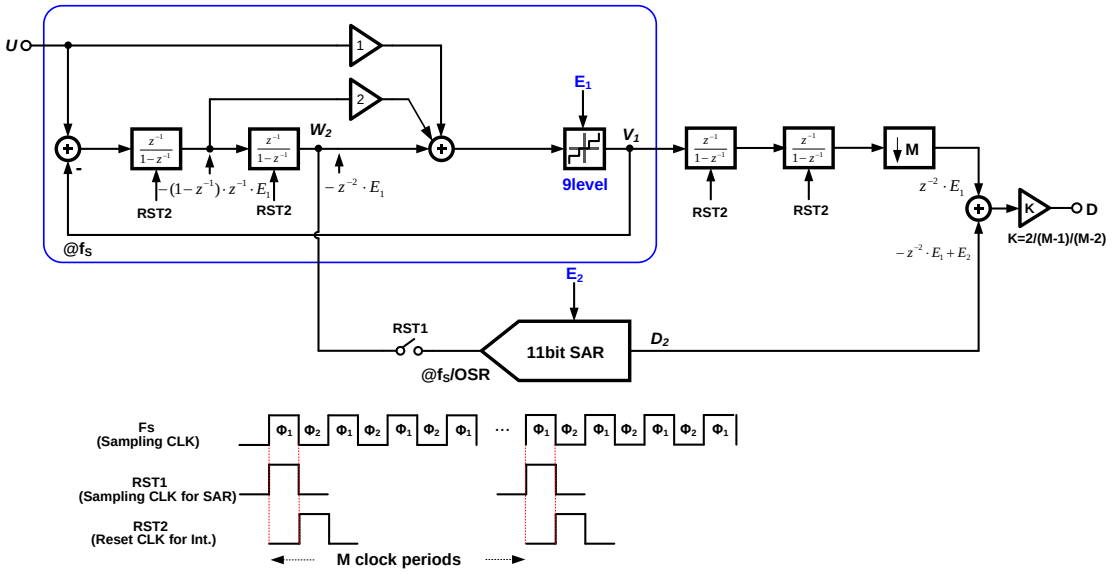


Fig. 3.1 Incremental ΔΣ ADC with extended counting and its timing diagram.

As expressed in Eq. (3.3), the quantization noise of the first loop is completely cancelled out and only the quantization noise of the second loop remains at the modulator output. This is more evident in the z-domain analysis. In Fig. 3.1, V_1 is $(1-z^{-1})^2$ and after passing through two delayed integrator it will be $z^{-2}\cdot E_1$. SAR ADC output, D_2, is $-z^{-2}\cdot E_1 + E_2$. After summing in the digital domain, the quantization noise of the first loop, E_1, is completely cancelled. Also, from the Eq. (3.3), the equivalent quantization noise of the incremental ADC with extended counting is

$$E_{IDC} = \frac{2}{(M-1)(M-2)} \cdot E_2 \tag{3.4}$$

where M is the oversampling ratio and E_2 is the quantization noise of the second ADC. Therefore, we can increase the oversampling ratio or decrease the quantization noise of the second ADC to increase the SQNR.

The overall operation principle is almost same as 2-0 MASH ΔΣ ADC [3.8]. The only difference between the conventional 2-0 MASH structure and this architecture is reset. First, quantization noise of the first loop will be stored at the output of the second integrator. Before the reset of the first loop, the stored quantization noise will be sampled at the input of the second ADC and then it will be resolved again in second ADC to decrease the quantization noise further. After summing the digital output from the first loop and second loop, we can obtain Nyquist rate digital output.

3.3 Architectural consideration

As mentioned before, SQNR of the incremental ADC with extended counting ideally only depends on oversampling ratio and quantization noise of the second ADC. For wide band applications, increasing OSR is limited by the bandwidth of the amplifiers and power consumption. Therefore, decreasing quantization noise of the second ADC is more efficient way. To decrease the quantization noise more of the second ADC we can introduce inter-stage gain scaling technique. Fig. 3.2 shows the incremental ADC with extended counting and inter–stage gain scaling. As shown in Fig. 3.2, we introduce inter-

stage gain G in the first loop. After M clock periods, W_2 is

$$W_2[M] = G \cdot \left(\sum_{L=1}^{M-1} \sum_{i=1}^{L-1} U[i] - \sum_{L=1}^{M-1} \sum_{i=1}^{L-1} V_1[i] \right) \tag{3.5}$$

And, digital output of the second ADC is express as

$$G \cdot W_2[M] + E_2[M] = D_2 \tag{3.6}$$

Combining with Eq. (3.5) and Eq. (3.6) gives

$$\overline{u} + \frac{1}{G} \cdot \frac{2}{(M-1) \cdot (M-2)} \cdot E_2[M]$$

$$= \frac{1}{G} \cdot \frac{1}{(M-1) \cdot (M-2)} \cdot D_2 + \frac{1}{(M-1) \cdot (M-2)} \cdot \sum_{L=1}^{M-1} \sum_{i=1}^{L-1} V_1(i) \tag{3.7}$$

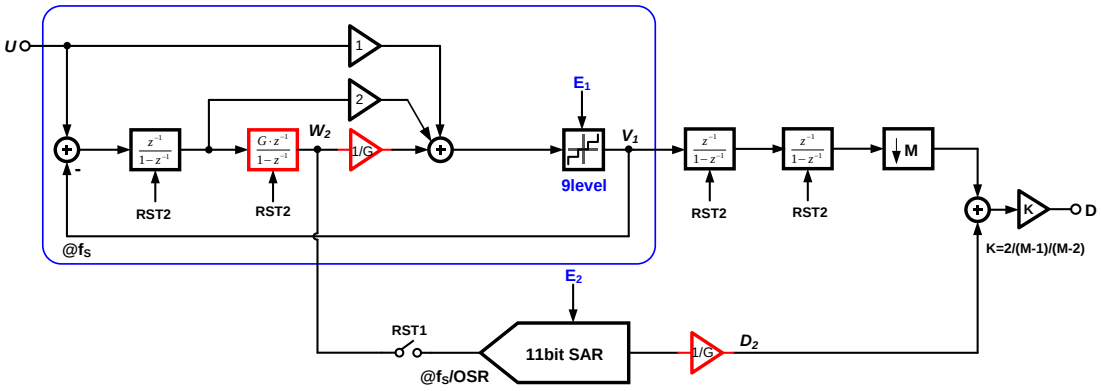


Fig. 3.2 Incremental ΔΣ ADC with extended counting with inter-stage gain.

Therefore, the equivalent quantization noise of the incremental ADC with extended counting and inter-stage gain is

$$E_{IDC} = \frac{2}{G \cdot (M-1)(M-2)} \cdot E_2 \tag{3.8}$$

As expressed in Eq. (3.8), we can decrease the equivalent quantization by a factor of *G* compared to Eq. (3.4). Equivalently, every doubling inter-stage gain *G* improves SQNR by 6dB.

3.3 1 CIFF2 incremental ΔΣ ADC

In our design, we used the low distortion feed-forward architecture [3.9] as the first ADC. We can extract quantization noise directly from the integrator output for the second ADC without any additional circuitry. Also, because each integrator processes only quantization noise in this architecture, output swing of the each integrator is bounded with quantization error and its amplitude is small depending on quantizer level. Thus, no slewing happens at the integrator, providing low power consumption and excellent linearity performance. Therefore, overall requirements of the analog circuitry are relaxed. Fig. 3.3 shows an example of the second order low distortion feed-forward architecture.

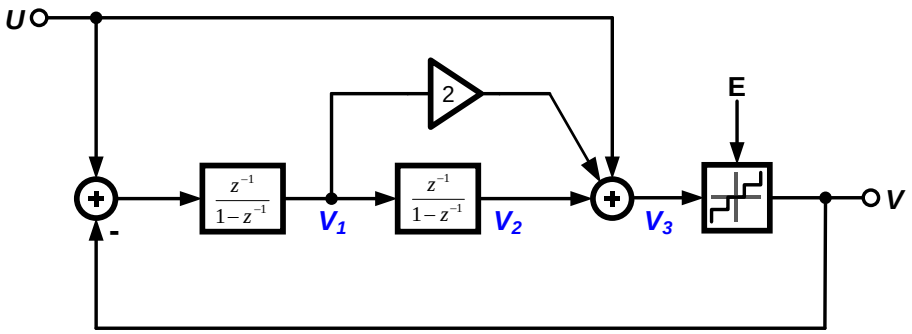


Fig. 3.3 Second order low distortion feed-forward ΔΣ modulator.

One disadvantage of this structure is that it requires analog active adder to sum analog signals in front of the quantizer. Because the active adder has a lot of input branch, the feedback factor is quite low and might consume power as much as the first integrator. Also, because input signal enter into the active adder directly, the output swing of the adder is quite large causing slewing and non linear distortion. To overcome this drawback, we applied the dynamic range optimization technique. By using this technique, the output swing of the active adder can be reduced greatly. Besides, feedback factor of the active adder increases which is helpful to reduce the power consumption. Fig. 3.4 shows the gain scaled second order low distortion feed-forward ΔΣ modulator.

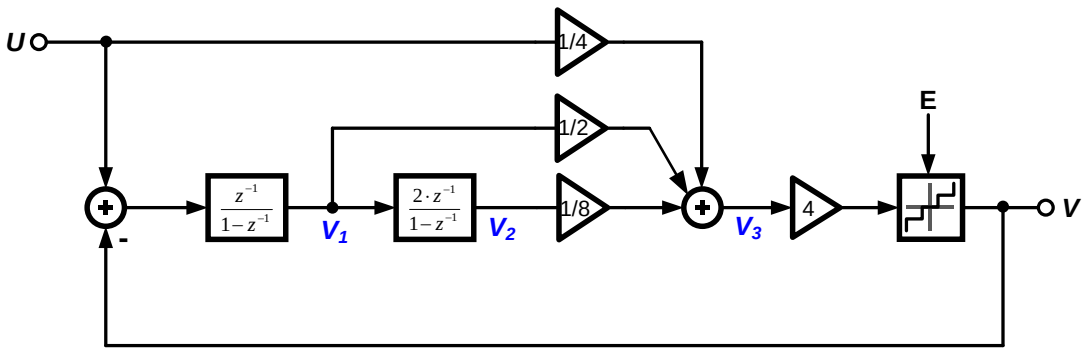


Fig. 3.4 Gain scaled second order low distortion feed-forward ΔΣ modulator.

Figs 3.5.(a), (b), (c) show the histogram of the each integrator's output swing before gain scaling. Figs 3.5.(d), (e), (f) show the histogram of the each integrator's output swing after the gain scaling. As shown in Fig. 3.5, the output swing of the active adder, V_3, is reduced greatly compared to conventional case. Using gain scaling techinque requires gain of 4 in front of the quantizer as shown in Fig. 3.4. It can be realized by reducing the reference voltage in the resistive ladder.

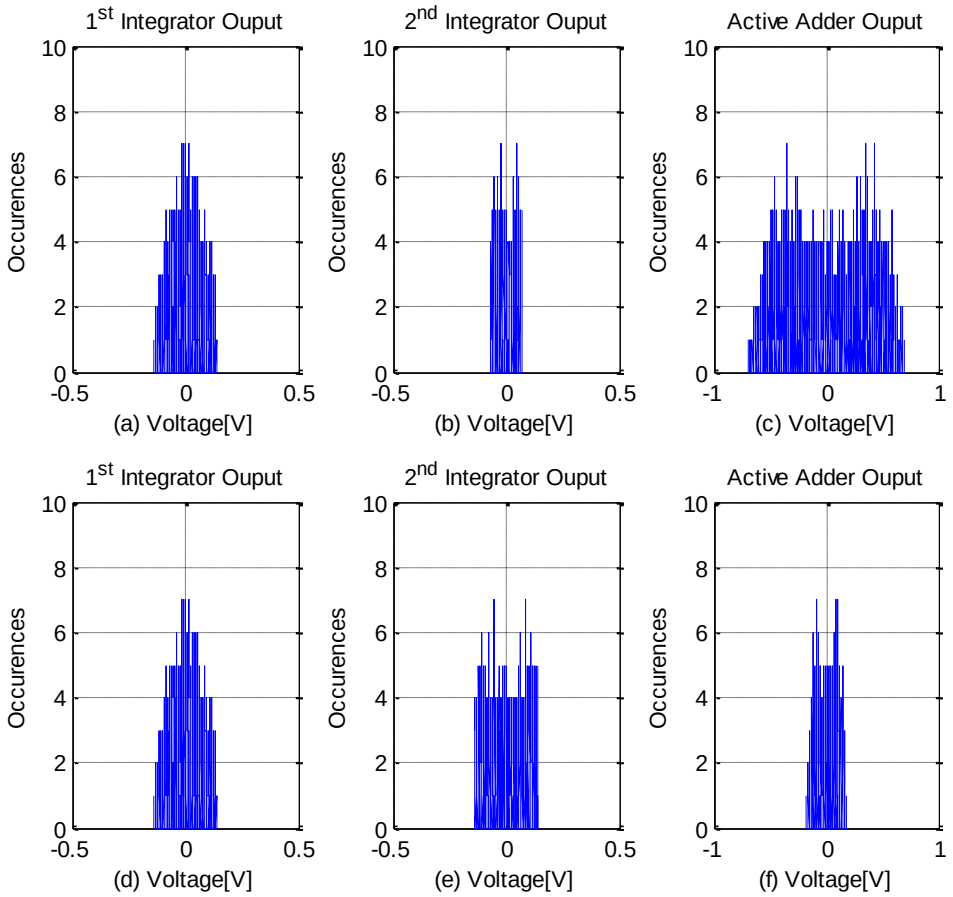


Fig. 3.5. (a), (b), (c) Histogram of each integrator output swing before scaling.
(d), (e), (f) Histogram of each integrator output swing after scaling.

3.3.2 Nyquist ADC

The second ADC in the incremental ΔΣ ADC with extended counting is a Nyquist rate ADC which can be a SAR ADC or any other power efficient ADC. Because the SAR ADC is most power efficient ADC for medium accuracy while meeting conversion rates up to 5MHz, we select a SAR ADC as a second ADC.

One thing we need to consider in using a SAR ADC as the second ADC is capacitive loading. As shown in Fig. 3.1, the input of the second ADC is a loading of the 2^{nd} integrator in the first ADC. In other words, the accumulated quantization noise of the 2^{nd} integrator should be sampled at the input of the second ADC within half of the sampling period for proper operation. Therefore, power consumption and settling error of 2^{nd} integrator depends on the capacitive loading of the second ADC. Fig. 3.6 shows the conventional 11bit SAR ADC structure.

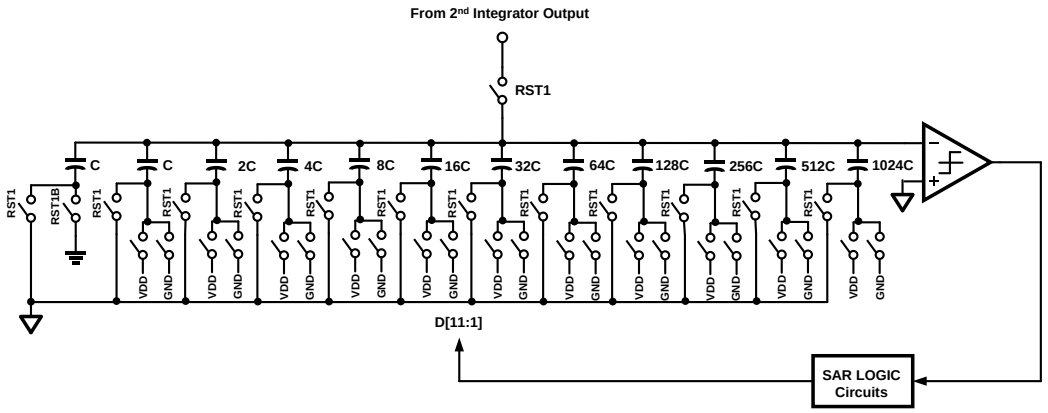


Fig. 3.6 Conventional 11bit SAR ADC.

As shown in Fig. 3.6, the total input capacitance in conventional SAR ADC is around 2048C to implement an 11bit SAR ADC. If the unit capacitor size is 30fF, total input capacitance is about 6.1pF which is huge loading of the 2nd integrator. To solve large capacitive loading problem on the first ADC, the dual capacitor array SAR ADC structure [3.10] in Fig. 3.7 was used. The series capacitance C_{se} separates the 6-bit most-significant bit (MSB) array from the 5-bit least significant bit (LSB). If the unit capacitor size is 30fF, total input capacitance is about 3pF which is half of the conventional SAR ADC. Therefore, using dual capacitor array DAC architecture help the 2nd integrator reduce the power consumption and improve the settling error with same power consumption.

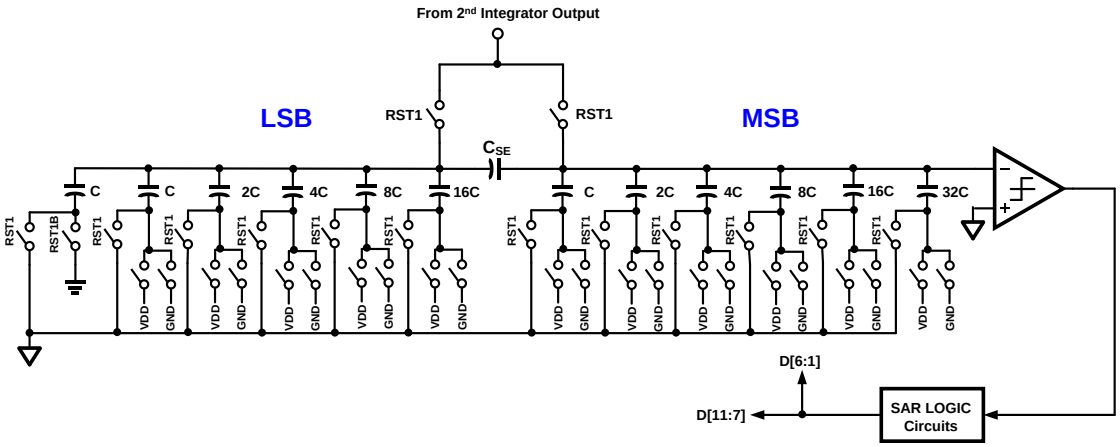


Fig. 3.7 11bit SAR ADC using dual capacitor array DAC.

Fig. 3.8 shows the proposed block diagram and its timing diagram based on our discussion and consideration. The first ADC utilizes second order low distortion architecture with gain scaling technique to reduce the output swing and power consumption. The second ADC uses a dual capacitor array 11 bit SAR ADC to reduce the capacitive loading of the 2nd integrator. The overall design equation is

$$\overline{u} + \frac{1}{G} \cdot \frac{2}{(M-1)\cdot(M-2)} \cdot E_2[M]$$
$$= \frac{1}{G} \cdot \frac{1}{(M-1)\cdot(M-2)} \cdot D_2 + \frac{1}{(M-1)\cdot(M-2)} \cdot \sum_{L=1}^{M-1} \sum_{i=1}^{L-1} V_1(i) \tag{3.8}$$

And, the equivalent quantization noise is

$$E_{IDC} = \frac{2}{G \cdot (M-1)(M-2)} \cdot E_2 \tag{3.9}$$

Therefore, the achievable SQNR with 11-bit SAR ADC is

$$SQNR = 20 \cdot log \frac{V_{FS}}{E_{IDC}} = 20 \cdot log \left(2^{11} \cdot \frac{(M-1)(M-2)\cdot G}{2} \right) \tag{3.10}$$

To achieve more than 15.5 bit accuracy we choose M=16 (oversampling ratio) and G=2 (inter-stage gain). Based on Eq. (3.10), we can obtain 18.4 bit ideally.

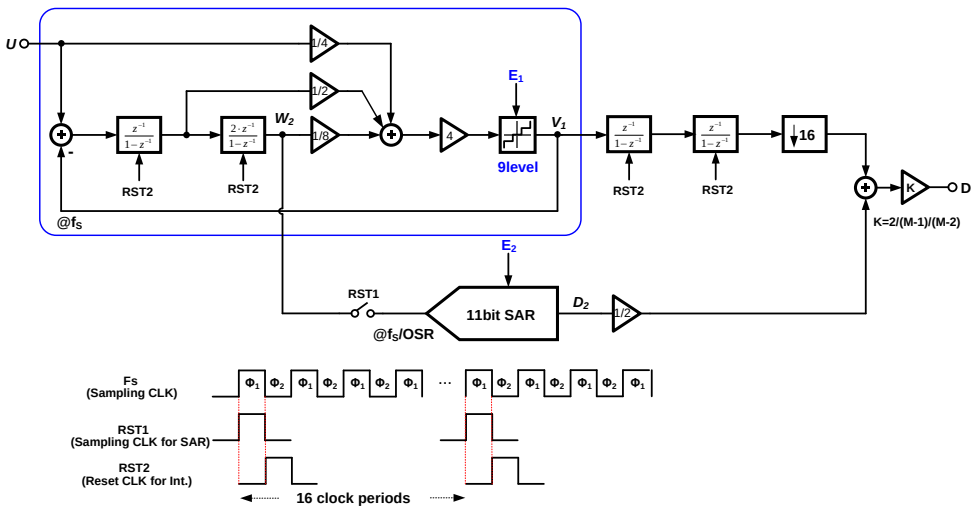


Fig. 3.8 Proposed incremental ΔΣ ADC with extended counting.

3.4 Circuit design

3.4.1 Opamp design

To determine the gain requirement of the amplifier, system level simulation was done in Matlab Simulink. In this simulation, each opamp gain was varied individually while other opamps' gain are set to almost ideal. Gain requirement of the opamp is plotted in Fig. 3.9. For the first and second integrator, more than 70dB gain is required. Generally, gain requirement of the amplifier is relaxed in the latter stages in the single loop ΔΣ ADC because the settling error of the latter stage is reduced by former stage gain.

However, due to the matching requirement between analog loop filter and digital transfer function, high accuracy analog components are needed to minimize the quantization noise leakage [3.1]. Thus, we also need higher gain amplifier in the second integrator compared to that of in the single loop ΔΣ ADC. Fig. 3.10 shows the effect of the coefficient error of the second integrator on the overall performance. A 1% coefficient error degrades the SQNR more than 10dB. Based on the simulation results, most power efficient, single stage telescopic cascade with gain boosting amplifier was used for first and second integrator. With the low distortion architecture and gain scaling technique, the output of each integrator is not very large. Thus, single stage telescopic cascode amplifier has no slewing and voltage headroom issue.

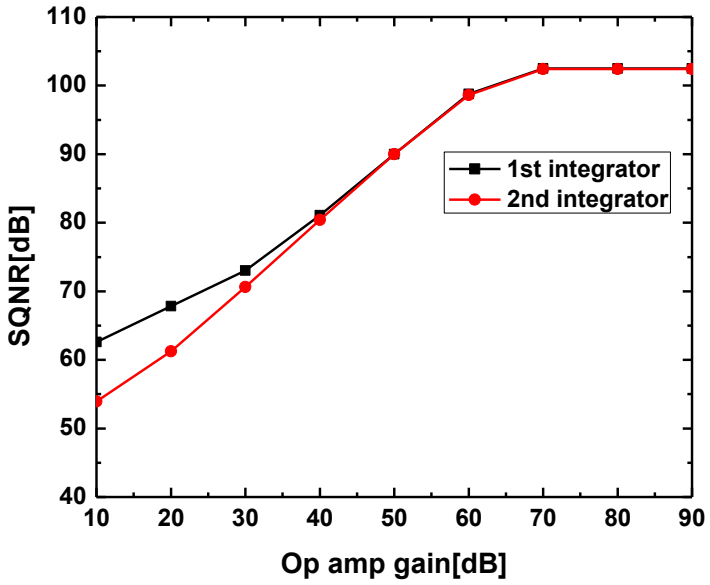


Fig. 3.9 SQNR versus opamp gain.

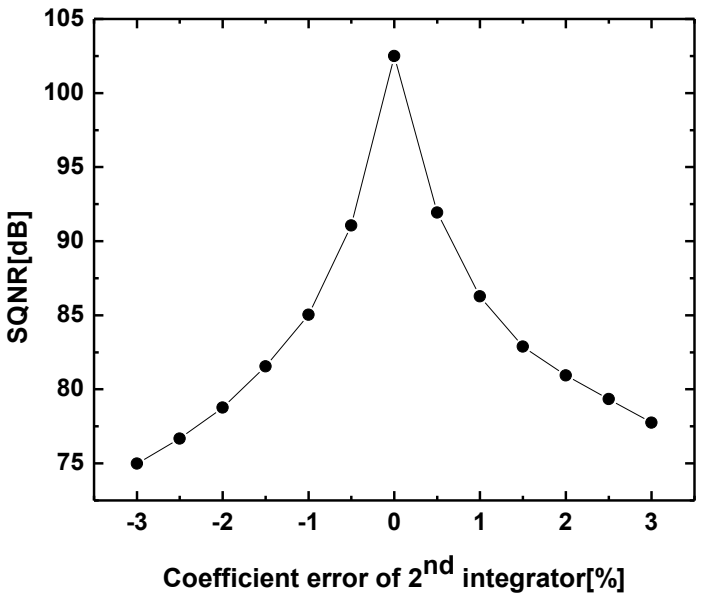


Fig. 3.10 SQNR versus coefficient error of the second integrator.

Fig. 3.11 shows the telescopic cascode amplifer with gain boosting for the first and second integrator. This amplifier achieves a GBW of 1.5GHz and a dc gain of 75dB with 3.3V supply voltage. Noise contribution from the top PMOS transistors was minimized by assigning the large overdrive voltages for the given output swing requirement. Also, NMOS input pairs were used to maximize the transconductance with given energy. An active adder also used the telescopic cascode structure without gain boosting as shown in Fig. 3.12.

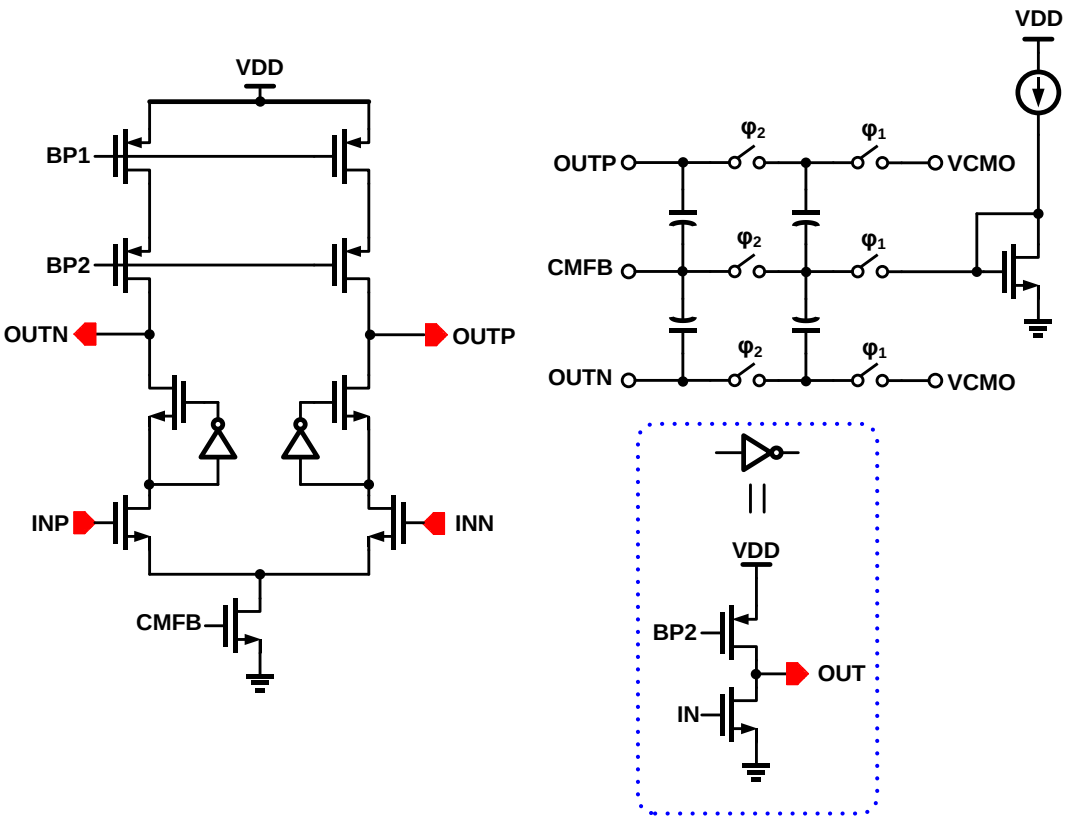


Fig. 3.11 Telescopic cascode opamp with gain boosting for the first and second integrator.

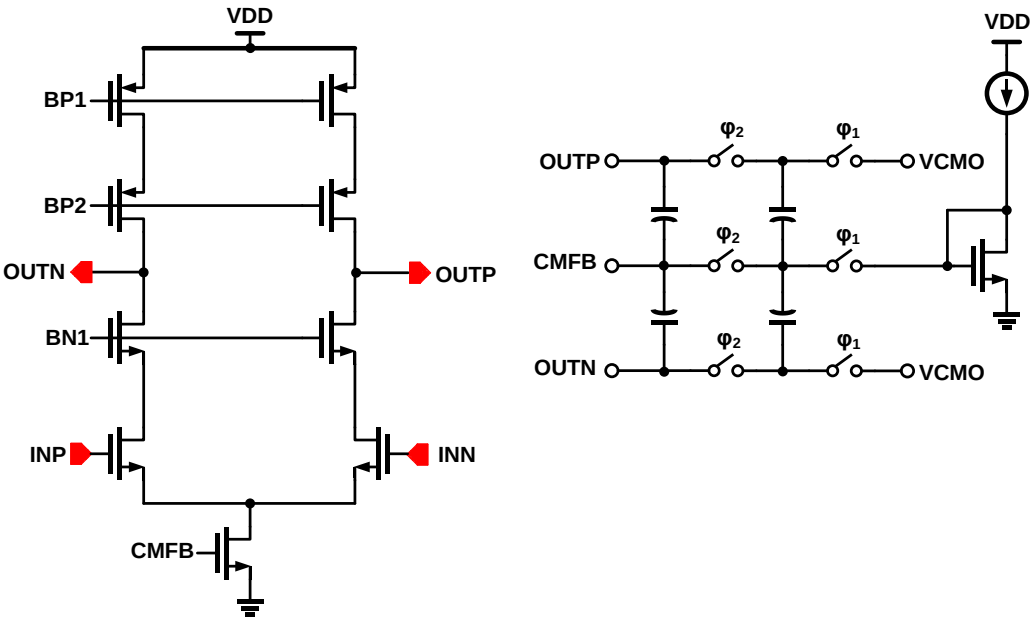


Fig. 3.12 Telescopic cascode opamp for the active adder.

3.4.2 Thermal noise

Generally, for high-fidelity audio ADCs, 75% noise budget is allocated for thermal noise because quantization noise should be very low with high OSR. Only 5% is assigned for noise budget for quantization noise in this kind of system [3.1]. However, for wideband application, high OSR might not be applicable due to the large power consumption and bandwidth limitation of the amplifier. Therefore, we assigned a 40% noise budget for thermal noise and quantization noise. The rest of the budget is for opamp, feedback DAC and other noise sources from the modulator. To achieve 96dB SNR, noise power should be

$$P_n = \frac{0.72}{10^{\frac{96}{10}} \cdot 0.4} = 4.5 \times 10^{-10}(V^2/Hz) \quad (3.11)$$

with -4.4dBFS of the input signal. Because latter stage noise contribution is attenuated by former stage gain, their noise contribution can be negligible. Thus, Eq. (3.11) can be used to estimate sampling capacitor size in the first integrator. Because we designed the separated feedback DAC structure in the incremental ΔΣ ADC, sampling capacitor size from the noise analysis of [3.11,12] to meet a given SNR is

$$C = \frac{4}{3} \cdot \frac{8kT}{OSR} \cdot \frac{1}{P_n} \cong 6pF \quad (3.12)$$

where, k is Boltzmann constant ($1.38 \times 10^{-23} J/K$), T is absolute temperature ($300^o C$), and OSR is 16.

3.4.3 Comparator design

8-level quantizer in the first ADC consists of pre-amplifier, track and latch stage and a set and reset (SR) latch as shown in Fig. 3.13. A single stage pre-amplifier was used to prevent the kick back noise from the latch. Also, because this preamplifier is continuously working during integration phase, pre-amplification time can be reduced which is helpful for high speed operation. DC gain of the pre-amplifier is 15dB and GBW is very large due to the small capacitive loading from the input pair of the track

and latch stage.

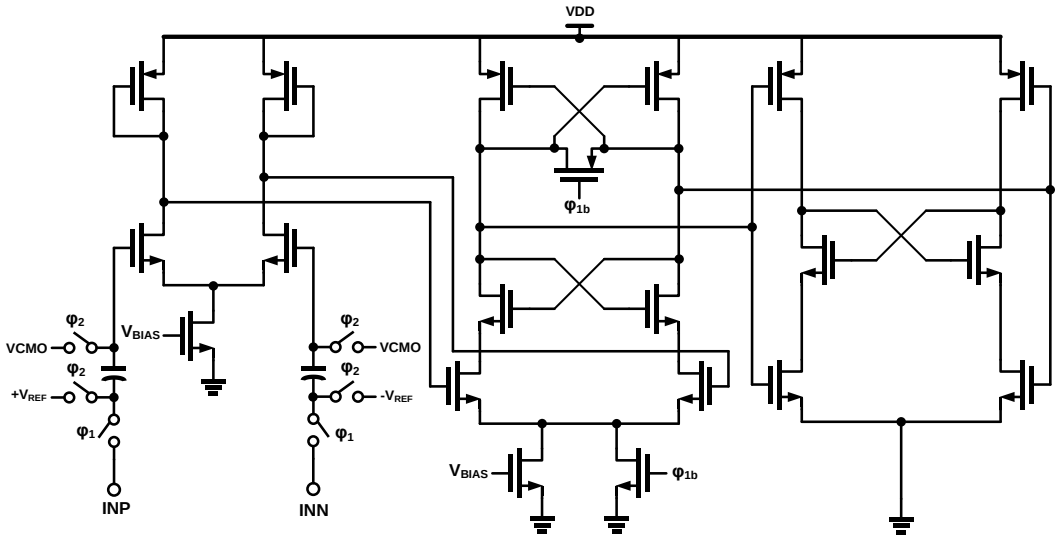


Fig. 3.13 High speed and low power comparator.

One thing we need to consider very carefully in the comparator design is the offset voltage. Because we scaled the gain of the integrator to reduce the swing of the integrator, effective gain of the comparator should be 4 as shown in Fig. 3.8. In this implementation, positive VREF is 2.65V, negative VREF is 0.65V, and output common mode voltage is 1.65V. To have the effective gain of 4 in the comparator, we need to generate positive VREF is 1.9V and negative VREF is 1.4V. Thus, a single full scale reference becomes from $2V_{pp}$ to $0.5V_{pp}$. The reduced reference voltage can be easily generated in resistor string as shown in Fig. 3.14. Because of the reduced reference voltage, we need to check the offset voltage of the comparator for proper operation. Monte-Carlo simulation was done 1000 times in Hspice based on designed comparator with 3 sigma threshold voltage variation for all transistors. Fig. 3.15 shows the

simulation result whose maximum offset voltage is 9.9mV. This offset voltage is much smaller than half of 1 LSB (125mV).

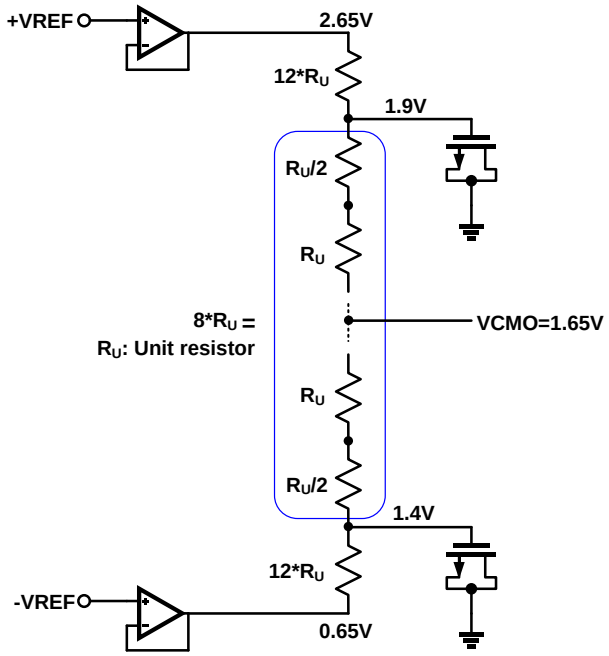


Fig. 3.14 Reduced reference voltage in resistive string.

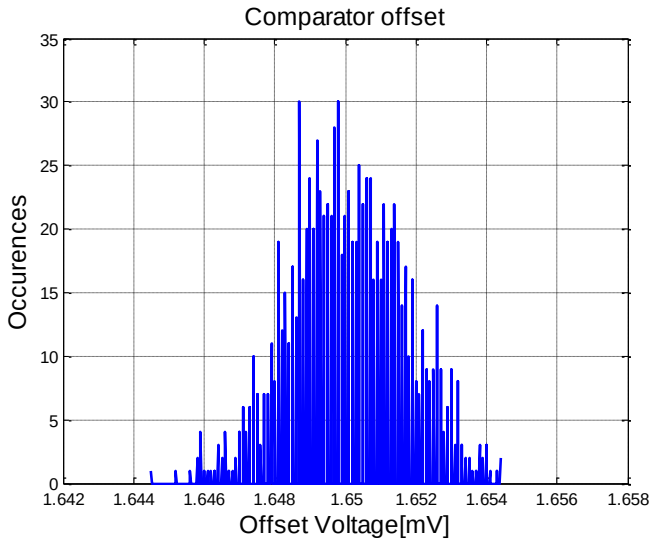


Fig. 3.15 Comparator offset voltage using Monte-carlo simulation.

3.4.4 Data weighted averaging

Using multi-bit quantizer in the ΔΣ ADC offers low quantization noise and low power consumption due to the small output swing of the integrator. However, feedback DAC mismatch error with multi-bit capacitors, resistors, or current sources array cause nonlinearity of the feedback DAC. Therefore, dynamic element matching is usually used to filter the DAC mismatch error out of signal band, by using a scrambler to shuffle the thermometer coded quantizer output before they are applied on the feedback DAC. In our design DEM circuit with barrel shifter was designed to shape the mismatch error of 8-level DAC in the first stage.

3.4.5 SAR ADC design

In our implementation, the second ADC used the most power efficient SAR ADC. As mentioned in Ch. 3.3, we designed the dual capacitor array SAR ADC to reduce the capacitive loading of the 2nd integrator. As shown in Fig. 3.7, series capacitance C_{se} separates the 6-bit most-significant bit (MSB) array from the 5-bit least significant bit (LSB). The size of C_{SE} can be chosen the combination C_{SE} , C_{LSB} (the total capacitance on the LSB side) and C_{P2} (the parasitic capacitance on the LSB side), as shown in Fig. 3.16.

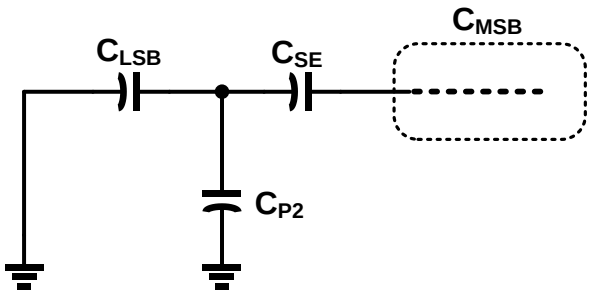


Fig. 3.16 Equivalent single ended circuit diagram of a portion of the capacitor array.

The design equations are given in Eq. (13) and (14).

$$C_{SE} \approx \frac{C_u \cdot C_{LSB}}{C_{LSB} - C_u} + \frac{C_u \cdot C_{P2}}{C_{LSB} - C_U} \tag{3.13}$$

$$C_{SE} \approx \frac{32}{31} C_u + \frac{1}{31} C_{P2} \tag{3.14}$$

where C_u is the unit capacitor size and C_{p2} is the total capacitance of the C_{LSB} and C_{SE}. In our design, $C_u = C_{SE}$ =30fF was used. Even if a unit capacitance was used for C_{SE}, the simulation result was no big difference. Also, although in the 0.18μm technology used the PIP (Poly insulator Poly) capacitor has better matching characteristic than MIM (Metal insulator Metal) capacitor, we used MIM capacitor to reduce the parasitic capacitance in the SAR ADC.

3.4.6 Simplified switched capacitor circuit

Fig. 3.17 shows the single-ended switched capacitor circuit of the designed modulator. A prototype ΔΣ ADC was fabricated in 0.18μm 2-poly and 4-metal CMOS process. The input sampling and feedback DAC capacitors are separated to avoid signal dependent reference loading effect [3.13]. The CIFF2 incremental ΔΣ ADC used poly-insulator-ploy (P1P) capacitor to achieve better matching characteristic and the SAR ADC utilized the metal-insulator-metal (MIM) to have less parasitic capacitance based on the design manual. Bootstrapped switch was used for input sampling switch to achieve high linearity and prevent signal dependent charge injection [3.14]. Data weighted averaging (DWA) with barrel shifter was applied to filter out mismatch error of the 8 capacitor array [3.15]. Analog power supply is 3.3V and digital power supply is 1.8V.

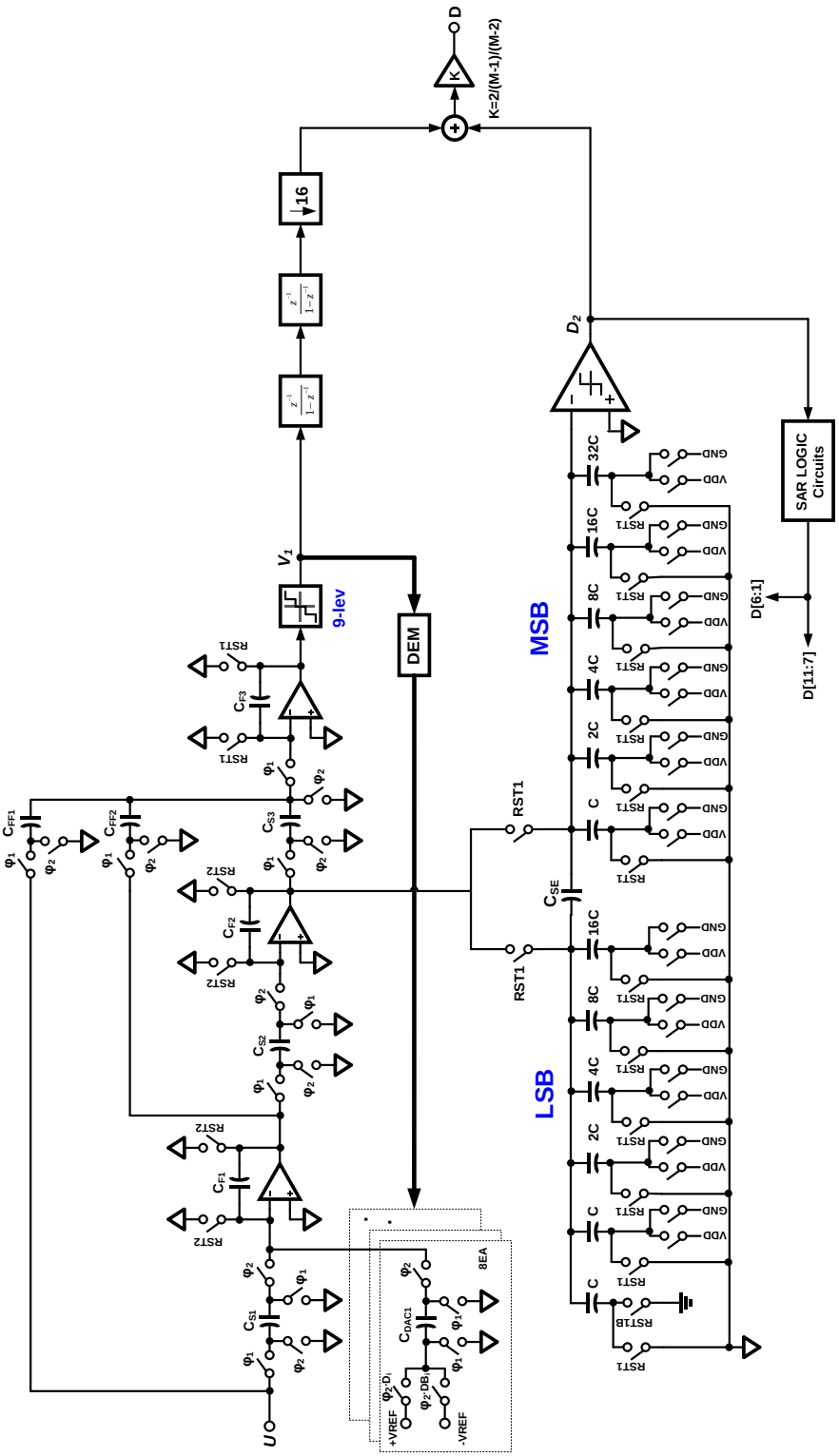


Fig. 3.17 Single ended switched capacitor circuit of the modulator.

3.5 Experimental results

3.5.1 Test setup

A 4-layer PCB was designed as shown in Fig. 3.18. The top and bottom layer are used for signal routing. The 2nd layer is for ground plane and the 3rd layer is for different power plane. The 2nd layer and 3rd layer are filled with copper to reduce the parasitic resistance. Decoupling capacitors for power pins of the DUT (Device Under Test) were placed as close as possible to the chip. Also, the decoupling capacitance difference is less than 10:1 to prevent anti-resonance phenomenon where the self-resonant frequencies of two capacitors differ. [3.16]. Reference voltages and control signal is generated from variable resistors and reference generator. Different power supply voltages to the chip are generated from LDO (Low Dropout Regulator) and variable resistors. Balun generates the differential signal from single ended signal at the left side of the chip. Two 8x2 connectors and one 4x2 connectors at the right side are used to extract the reference clock and digital output of the ADC. Fig. 3.19 shows the test setup. Fig. 3.20 shows the PCB layout for standalone SAR ADC. Fig. 3.21 shows the detailed block diagram of the test setup. Differential input signal is generated by signal generator, band-pass filter, and balun. The clock from signal generator is applied to the DUT with bias-tee to move the common mode voltage. 4-bit digital output from the first ADC and 11-bit digital output from the second ADC is grabbed in Logic Analyzer after passing through digital buffer. And then, summing each digital output, digital filtering, down-

sampling, and FFT was done in Matlab.

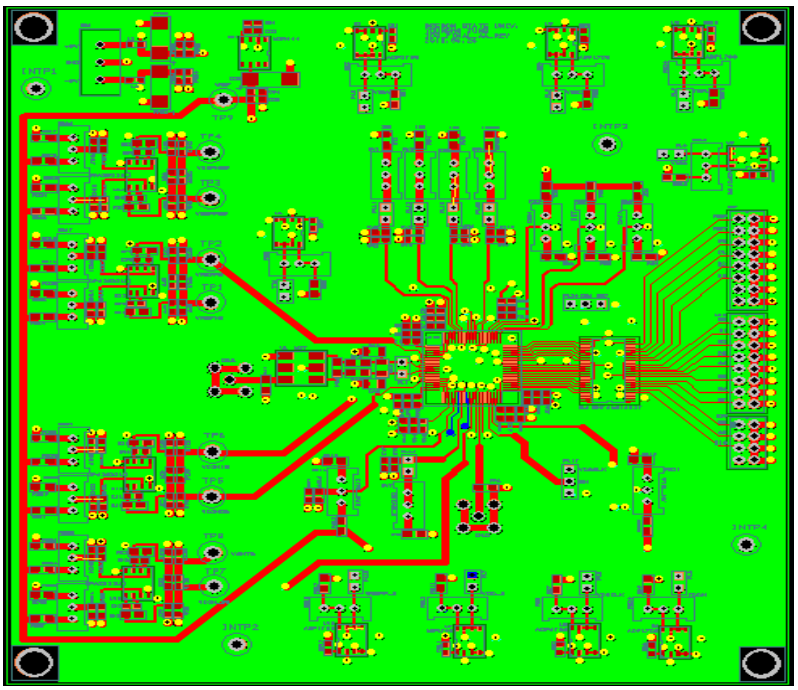


Fig. 3.18 PCB layout for incremental ΔΣ ADC with extended counting.

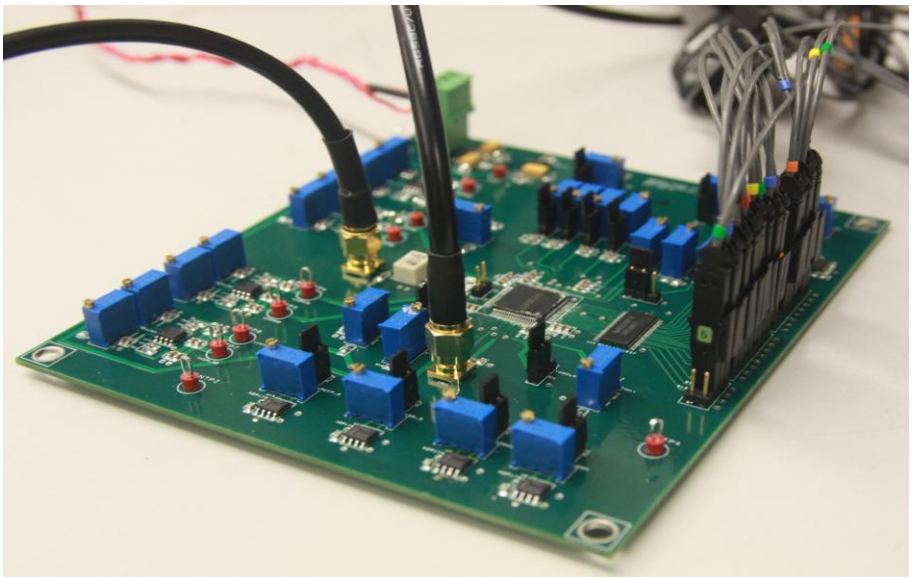


Fig. 3.19 Test setup.

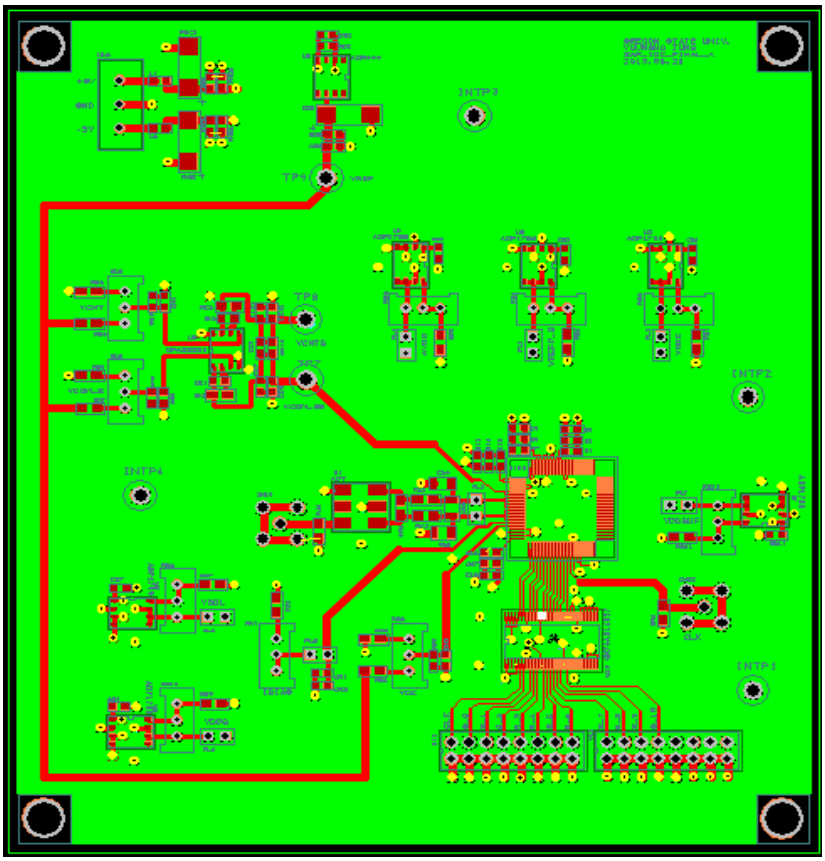


Fig. 3.20 PCB layout for SAR ADC.

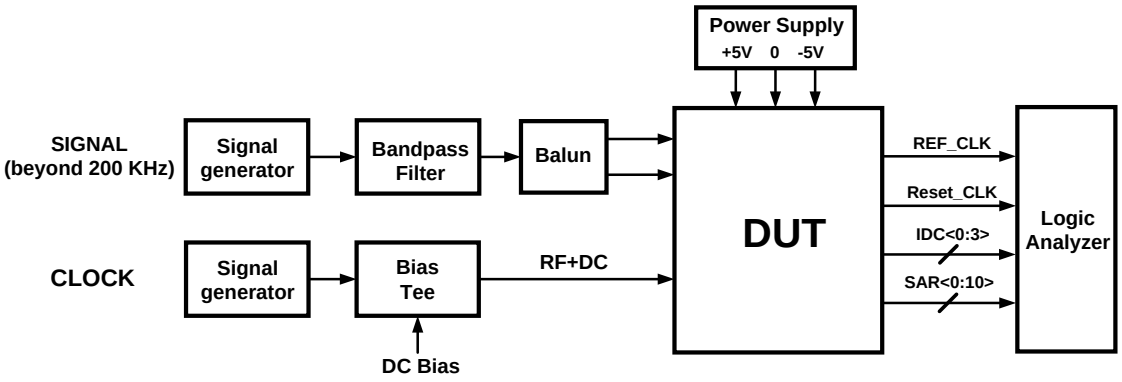


Fig. 3.21 Block diagram of the test setup.

3.5.2 Measurement results

Fig. 3.22 shows the die micrograph. The prototype ADC occupies $3.12mm^2$ $(2080\mu m \times 1500\mu m)$.

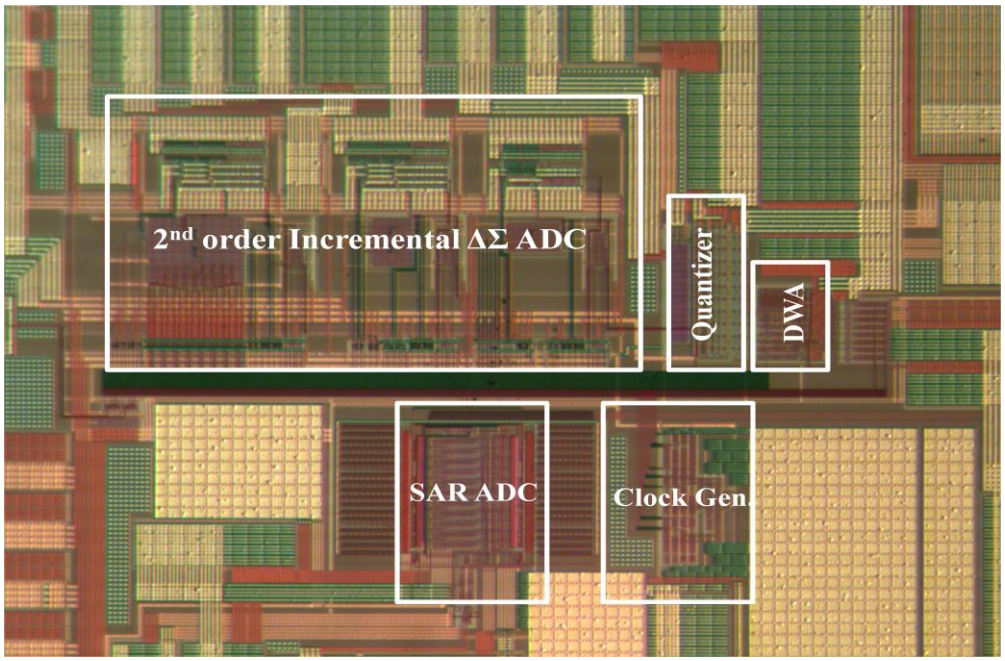


Fig. 3.22 Die micrograph.

Fig. 3.23 shows the measured output spectrum of the first ADC (CIFF2 incremental ΔΣ ADC). It shows 53.8dB SNDR in the 0~2.5MHz signal band with 200.19 kHz input tone. Measurement result is almost same as post-layout simulation result whose SNDR is 54.5dB. Fig. 3.24 shows the measured output spectrum of the standalone SAR ADC (11-bit SAR ADC). It shows 53dB SNDR in the 0~2.5MHz signal band. SAR ADC measurement result is also comparable to its post-layout simulation result whose SNDR

is 54.4dB. Dynamic range testing result is shown in Fig. 3.25. Dynamic range is the value of the input signal at which the SNR is 0dB [3.17]. With -89.58dBFS input signal, output spectrum shows 2.1dB SNDR. Thus, dynamic range in 0-1.25MHz is about 91.6dB. Fig. 3.26 shows the measured spectrum of the 2nd order incremental ΔΣ ADC with extended counting. It shows 77.8dB SNDR in the 0~1.25MHz signal band. Even if each ADC works properly in 0-2.5MHz signal, it does not work properly in this signal band after combining together. This might be caused by insufficient settling time or impure residue voltage.

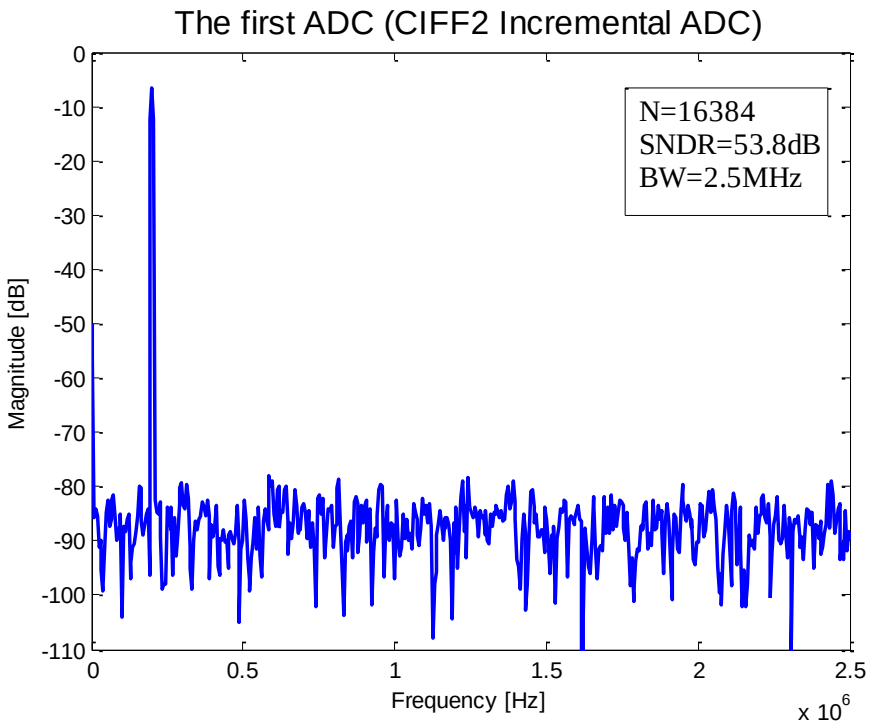


Fig. 3.23 Measured spectrum of the first ADC (CIFF2 incremental ΔΣ ADC).

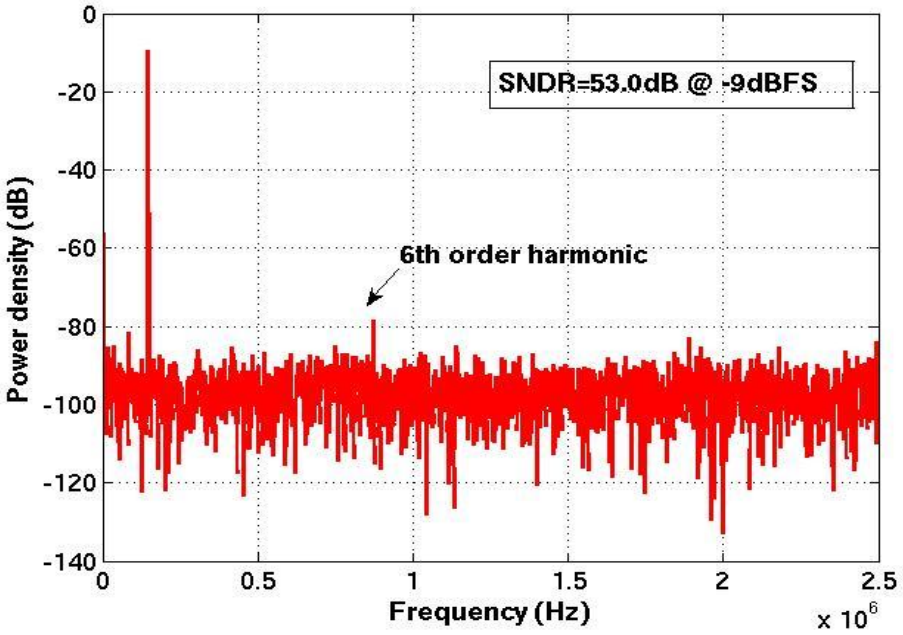


Fig. 3.24 Measured spectrum of the second ADC (11-bit SAR ADC).

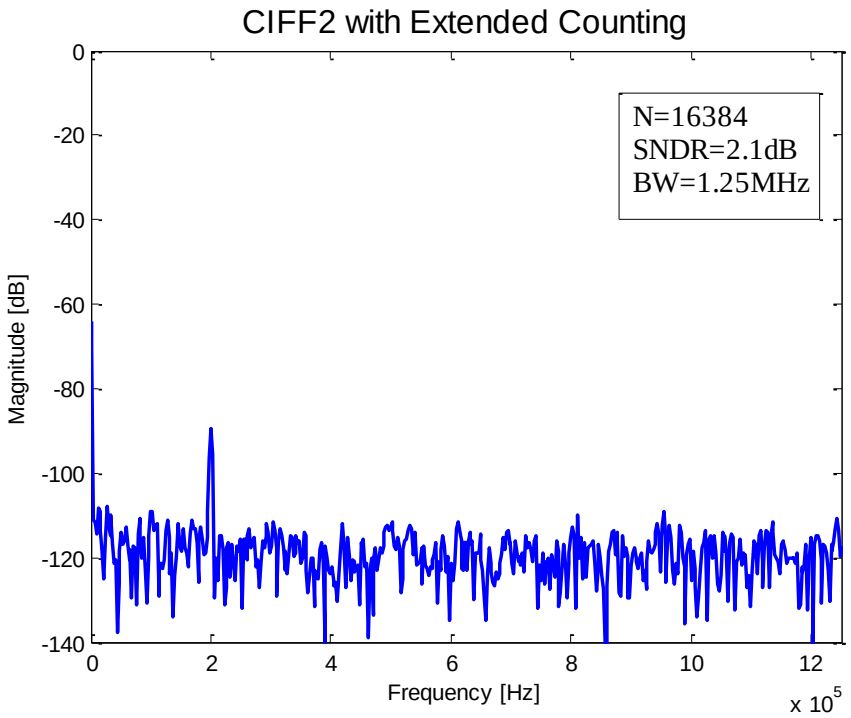


Fig. 3.25 Measured spectrum of incremental ΔΣ ADC with extended counting.

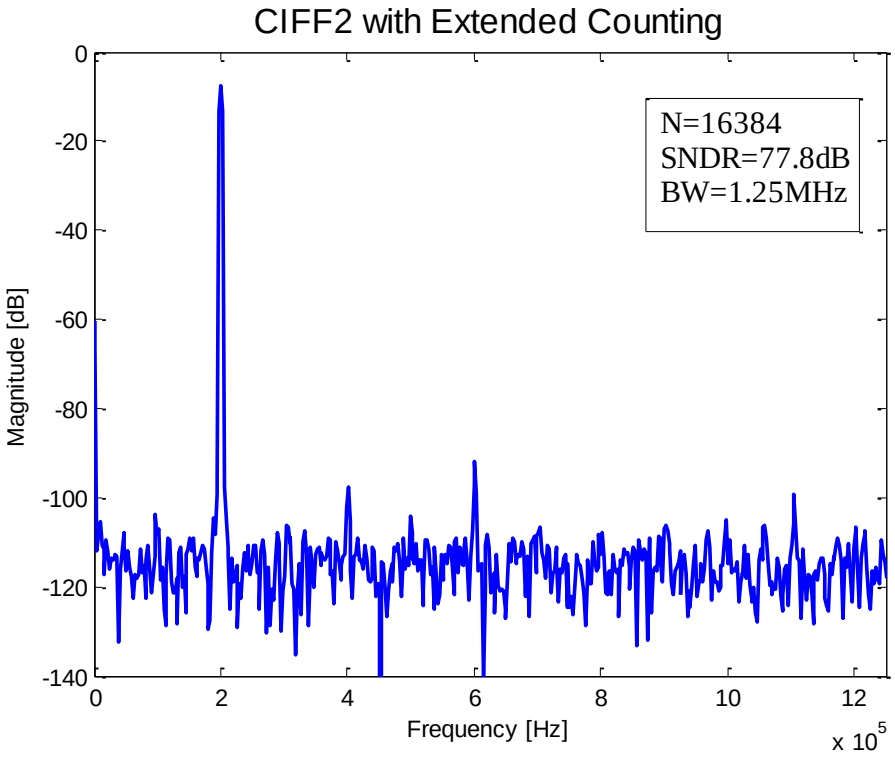


Fig. 3.26 Measured spectrum of incremental ΔΣ ADC with extended counting.

The measurement results are summarized in Table 3.1. It achieves 91.6dB dynamic range and 77.8dB peak SNDR. The overall performance degraded due to the large 3rd order harmonic distortion. Most of the power consumes in the first ADC in the incremental ΔΣ ADC due to analog circuitry. SAR ADC consumes about 10% of the total power.

Table 3.1 Summary of measured performance

Sampling frequency	40MHz
Signal bandwidth	1.25MHz
OSR	16
Dynamic range	91.6dB
Peak SNDR	77.8dB
Power consumption	48.4mW(CIFF2) 5.1mW (SAR ADC)
Power supply	3.3V (A)/1.8V (D)
Process	0.18μm 2P4M CMOS

3.5.3 Summary

Incremental ΔΣ ADC with extended counting was described and analyzed. The prototype ADC was fabricated with 0.18μm 2P4M CMOS process. Also, standalone SAR ADC was also fabricated for debugging. First, second order incremental ΔΣ ADC and 11-bit SAR ADC were measured separately. Second, incremental ΔΣ ADC with extended counting was measured and it achieves 91.6dB dynamic range, 77.8dB SNDR in 0-1.25MHz signal band. The total power consumption is 53.5mW with power supply (analog 3.3V, digital 1.8V).

3.6 2+2 MASH (Multi-Stage Noise Shaping) incremental ΔΣ ADC

3.6.1 Architecture

Motivation of 2+2 MASH [3.18,19] incremental ΔΣ ADC is similar to incremental ΔΣ ADC with extended counting. Fig. 3.27 shows the block diagram and timing diagram of the 2+2 MASH incremental ΔΣ ADC. This architecture utilizes another low distortion architecture as a second ADC instead of using SAR ADC. As I mentioned before, the input of the second ADC is a big capacitive loading of the 2nd integrator in the first ADC. Even if we can reduce the capacitive loading with dual capacitor array DAC structure to achieve around 9-bit accuracy, total input capacitance at one side is still 3pF. To decrease the capacitive loading further, we replaced the SAR ADC with second order low distortion architecture. Based on the sampling capacitor size, input sampling capacitor size of the second ADC can be reduced with proper ratio to make small contribution of kT/C noise. In our design, the ratio between the input sampling capacitor in the first ADC and that in the second ADC is 1/10 which is 500fF. The first ADC uses 9-level quantizer with simple rotational data-weighted averaging. The second ADC used 15-level quantizer to achieve around 10-bit accuracy without DWA, because the feedback DAC mismatch in the second ADC is shaped by the first ADC. Digital filter of the first loop consists of 2 non-delay integrators and 2 delayed integrators. Digital filter of the second loop digital filter consists of 2 non-delay integrators. Alternatively, two non-delayed integrators can be shared in real implementation to reduce the area.

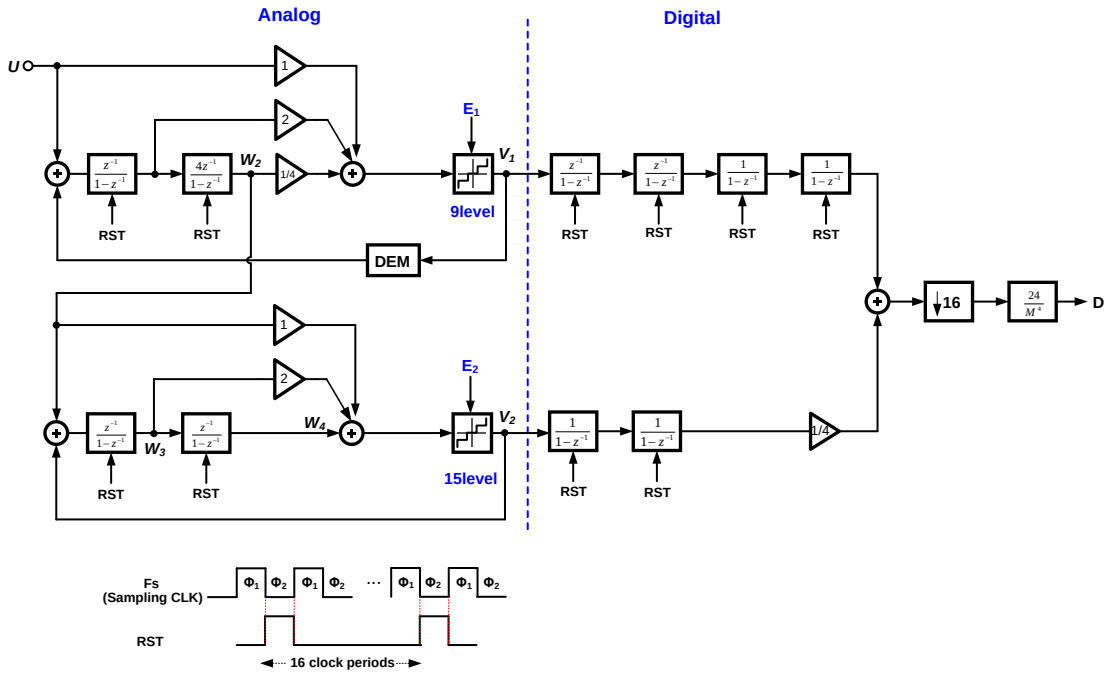


Fig. 3.27 Block diagram of the 2+2 MASH incremental ΔΣ ADC.

After M clock periods, W_2 and W_3 are expressed as

$$W_2[M] = 4 \cdot \sum_{L=1}^{M-1} \sum_{i=1}^{L-1} U[i] - \sum_{L=1}^{M-1} \sum_{i=1}^{L-1} V_1[i] \tag{3.15}$$

$$W_3[M] = 4 \cdot \sum_{M=1}^{N-1} \sum_{L=1}^{M-1} \sum_{i=1}^{L-1} U[i] - 4 \cdot \sum_{M=1}^{N-1} \sum_{L=1}^{M-1} \sum_{i=1}^{L-1} V_1[i] - 4 \cdot \sum_{i=1}^{N-1} V_2[i] \tag{3.16}$$

Digital output of the second ADC, V_2, is after M clock period

$$W_4[M] + 2 \cdot W_3[M] + W_2[M] + E_2[M] = V_2[M] \tag{3.17}$$

Substitution with Eq. (3.15) and Eq. (3.16) in Eq. (3.17) gives

$$4 \cdot \left[\sum_{N=1}^{O-1} \sum_{M=1}^{N-1} \sum_{L=1}^{M-1} \sum_{i=1}^{L-1} U[i] + 2 \cdot \sum_{M=1}^{N-1} \sum_{L=1}^{M-1} \sum_{i=1}^{L-1} U[i] + \sum_{L=1}^{M-1} \sum_{i=1}^{L-1} U[i] \right] + E_2[M]$$

$$= 4 \cdot \left[\sum_{N=1}^{O-1} \sum_{M=1}^{N-1} \sum_{L=1}^{M-1} \sum_{i=1}^{L-1} V_1[i] + 2 \cdot \sum_{M=1}^{N-1} \sum_{L=1}^{M-1} \sum_{i=1}^{L-1} V_1 i] + \sum_{L=1}^{M-1} \sum_{i=1}^{L-1} V_1[i] \right]$$

$$+ \sum_{N=1}^{O-1} \sum_{i=1}^{N-1} V_2[i] + 2 \cdot \sum_{i=1}^{N-1} V_2[i] + V_2[M] \tag{3.18}$$

Therefore, we can obtain design equation of the 2+2 MASH incremental ΔΣ ADC as shown in Eq. (3.19).

$$\therefore \ \bar{u} + \frac{6}{M^4} \cdot E_2[M] = \frac{24}{M^4} \left\{ \sum_{N=1}^{O} \sum_{M=1}^{N} \sum_{L=1}^{M-1} \sum_{i=1}^{L-1} V_1[i] + \frac{1}{4} \sum_{N=1}^{O} \sum_{i=1}^{N} V_2[i] \right\} \tag{3.19}$$

As shown right side in Eq. (3.19), digital filter of the first loop is comprised of 2 delayed integrators and 2 non-delayed integrators. The second loop's digital filter consists of 2 non-delayed integrators. If the realization does not meet design equation, the quantization noise of the first loop will not be cancelled out completely and degraded the performance dramatically. Equivalent quantization noise of the modulator is expressed as

$$E_{IDC} = \frac{6}{M^4} \cdot E_2[M] \tag{3.20}$$

To achieve more than 15.5 bit accuracy we choose M=16 (oversampling ratio) and G=4 (inter stage gain). Based on Eq. (3.20), we can obtain 17 bit ideally.

3.6.2 Circuit design

Fig. 3.28 shows the single ended switched capacitor circuit of the 2+2 MASH incremental ΔΣ ADC. Most blocks of the first stage are almost the same as those of incremental ΔΣ ADC with extended counting except inter-stage gain. 3 integrators in the second stage are scaled based on the active adder of the first stage. Small signal swing from the 2nd integrator in the first stage and low distortion architecture allows to use a telescopic cascode amplifier which is a power efficient single stage structure in the second ADC. Sampling switch of the second stage also used bootstrapped switch to achieve highly linear sampling. DEM circuit with barrel shifter was designed to shape the mismatch error of 9-level DAC in the first stage. Because the feedback DAC mismatch error caused by 15-level DAC in the second stage is shaped by preceding stage, DEM circuitry is not implemented in the second stage.

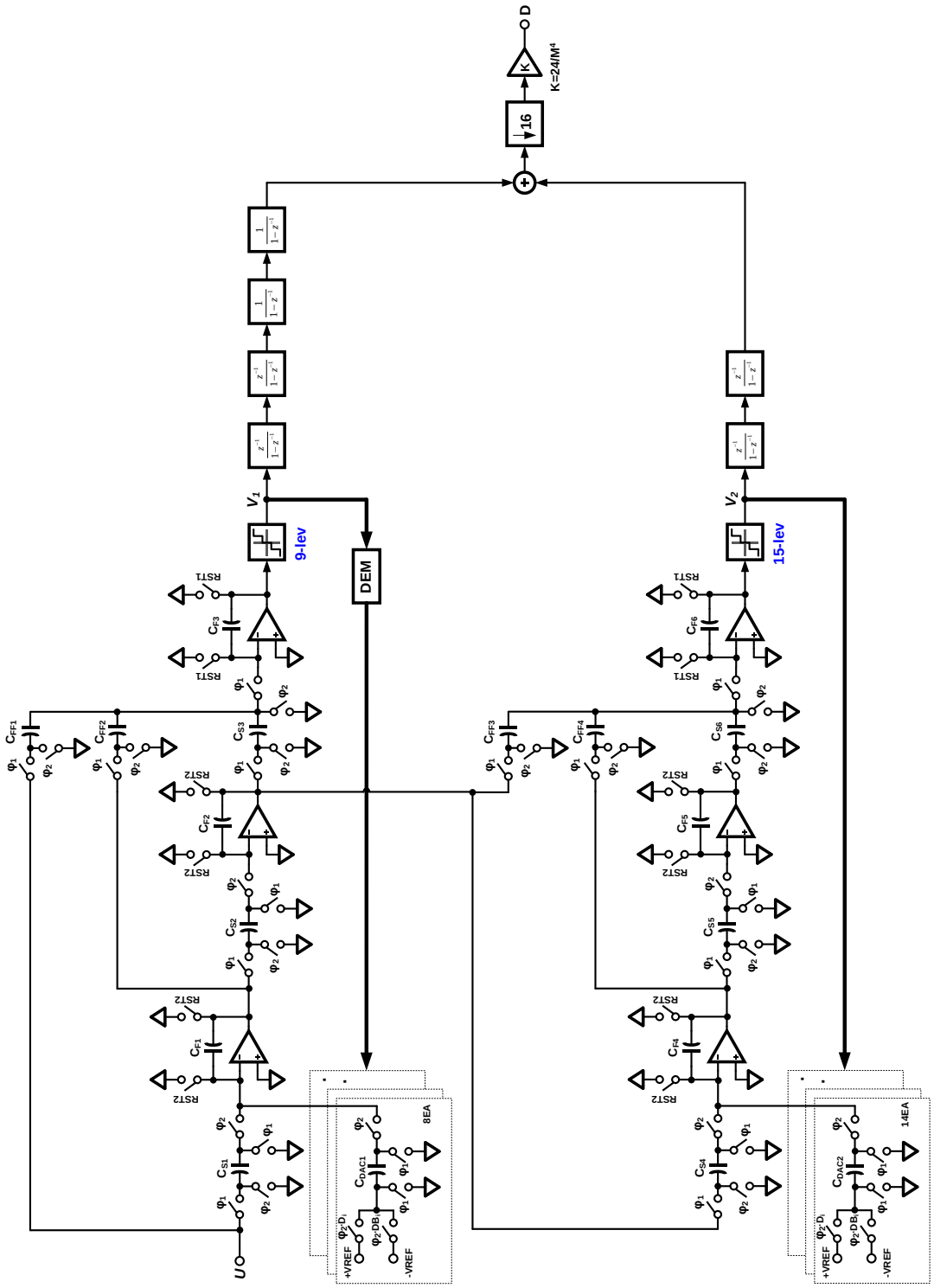


Fig. 3.28 Single ended switched capacitor circuit of the modulator.

3.7 Experimental results

3.7.1 Test setup

2+2 MASH incremental ΔΣ ADC was fabricated in 0.18μm 2-poly and 4-metal CMOS process. Fig. 3.29 shows the die micrograph and the ADC core area is 3.92mm^2 (2450$\mu m \times 1600\mu m$). Fig. 3.30 and Fig. 3.31 show the PCB layout and test setup, respectively.

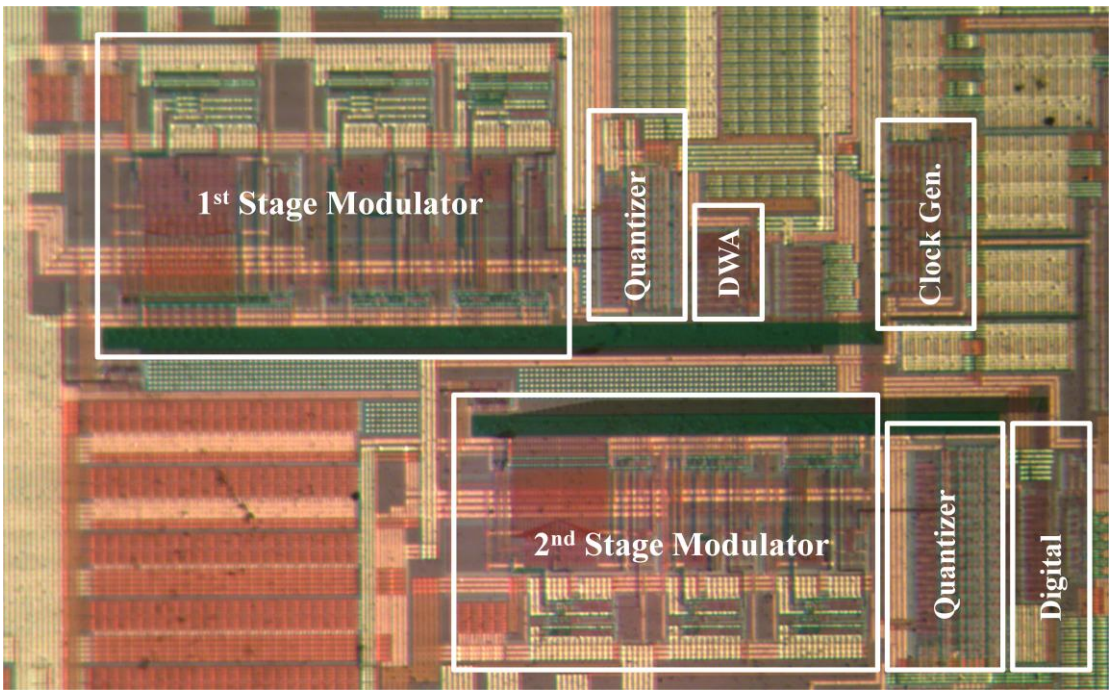


Fig. 3.29 Die micrograph.

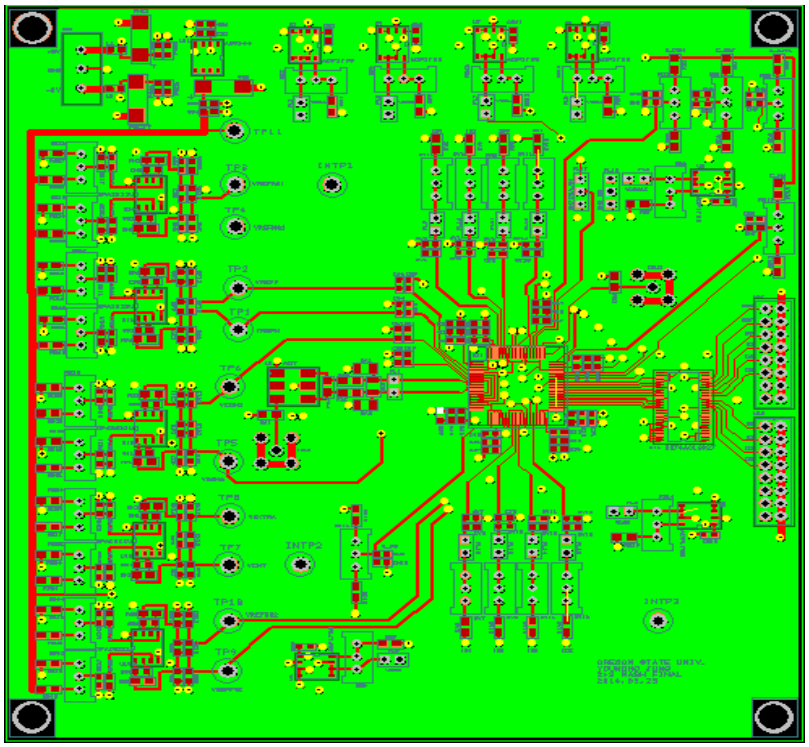


Fig. 3.30 PCB layout for 2+2 MASH incremental ΔΣ ADC.

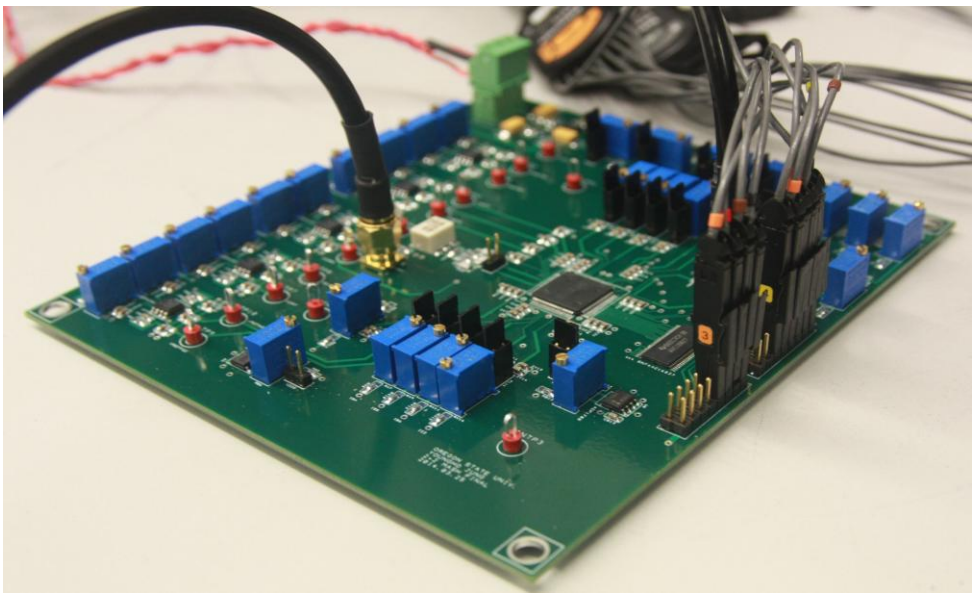


Fig. 3.31 Test setup.

3.7.2 Measurement results

Fig. 3.32 shows the measured output spectrum of the first stage in 0-2.5MHz signal band. It shows 53.5dB SNDR in the 0~2.5MHz signal band. The measurement result is quite comparable to post-layout simulation. With -91.96dBFS input signal, measured output spectrum of the overall modulator is shown in Fig. 3.33. Fig. 3.34 shows the measured output spectrum of the overall modulator. It shows 74.8dB peak SNDR up to1.25MHz signal band.

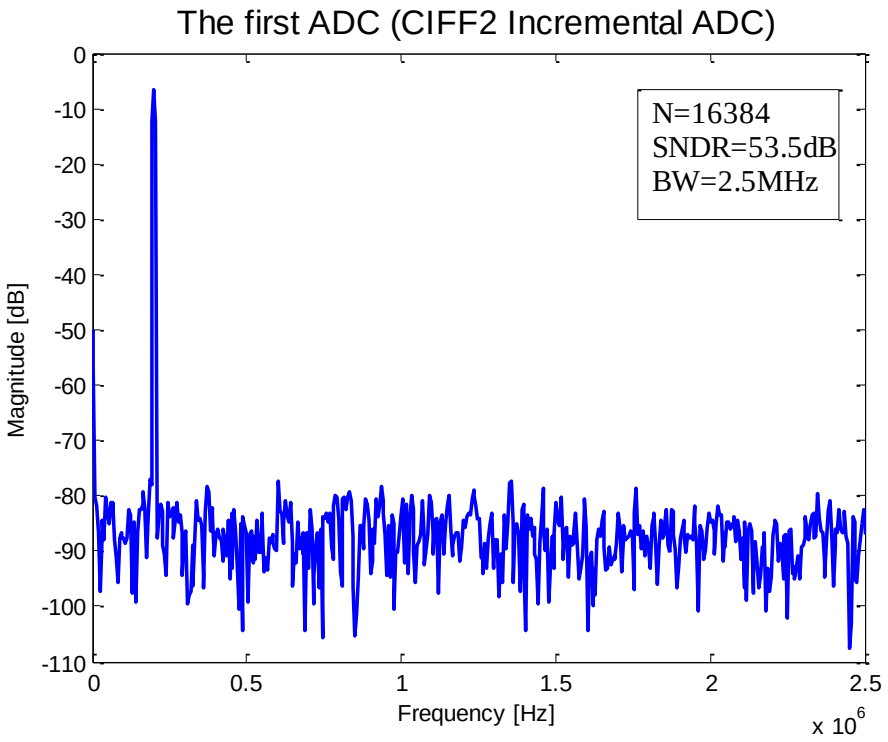


Fig. 3.32 Measured spectrum of the first ADC (CIFF2 incremental ΔΣ ADC).

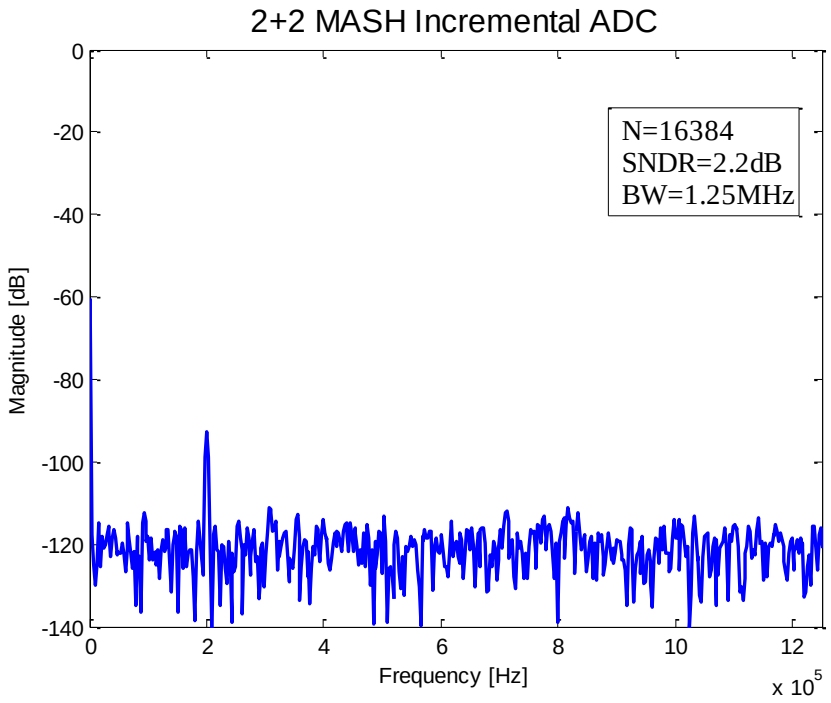


Fig. 3.33 Measured spectrum of the 2+2 MASH incremental ΔΣ ADC.

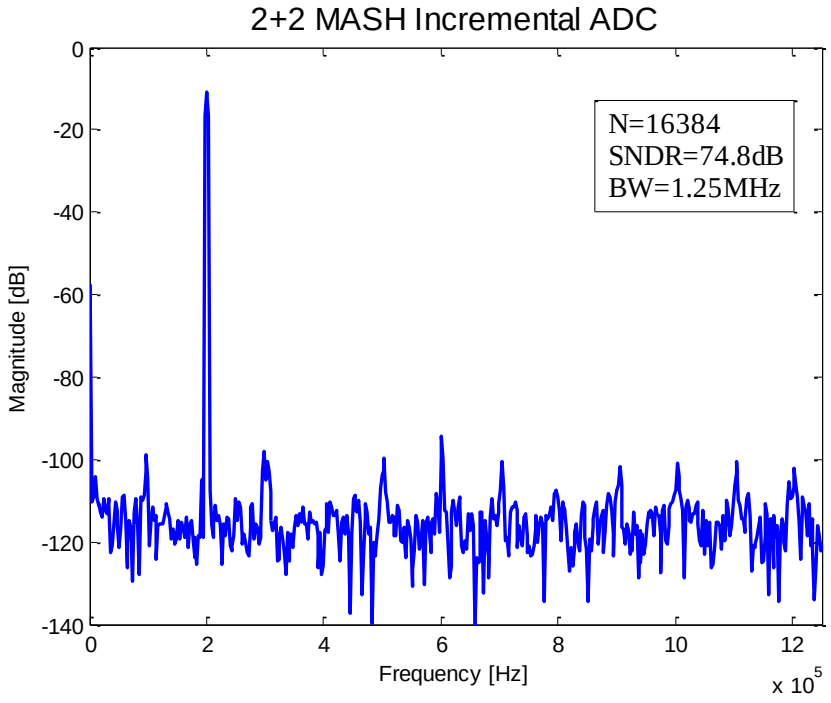


Fig. 3.34 Measured spectrum of the 2+2 MASH incremental ΔΣ ADC.

The measurement results are summarized in Table 3.2. It achieves 94.2dB dynamic range and 74.8dB peak SNDR up to 1.25MHz. The overall performance degraded because of the large harmonic distortion and noise floor increase.

Table 3.2 Summary of measured performance

Sampling frequency	40MHz
Signal bandwidth	1.25MHz
OSR	16
Dynamic range	94.2dB
Peak SNDR	74.8dB
Power consumption	32.3mW(A) 34.8mW (D)
Power supply	3.3V (A)/1.8V (D)
Process	0.18μm 2P4M CMOS

3.7.3 Summary

2+2 incremental ΔΣ ADC was discussed and analyzed. The prototype ADC was fabricated with 0.18μm 2P4M CMOS process. It achieves 94.2dB dynamic range, 74.8dB SNDR in 0-1.25MHz signal band. The total power consumption is 67.1mW with power supply (analog 3.3V, digital 1.8V).

References

[3.1] R. Schreier and G. C. Temes, "*Understanding of Delta-Sigma Data Converters"*, New York: Wiley, 2005.

[3.2] Z. Zhang, J. Steensgaard, G. C. Temes, and J. Y. Wu, "A split 2-0 MASH with dual digital error correction," *in IEEE Symp. VLSI Circuits Dig*., pp. 242-243, Jun. 2007.

[3.3] A. Rusu, M. Ismail, and H. Tenhunen, "A modified cascaded sigma-delta modulator with improved linerarity," *in IEEE Symp. VLSI Circuits Dig*., pp. 77-82, May. 2005.

[3.4] J. De Mayer, P. Rombouts, and L. Weysten, "A double-sampling extended-counting ADC,", *IEEE J. Solid-State Circuits*, vol. 39, no. 3, pp. 411-418, Mar. 2004.

[3.5] C. Jasson, "A high-resolution, compact, and low-power ADC suitable for array implementation in standard CMOS," *IEEE Trans. Circuits Syst. I, Fundam. Theory Applicat*., vol. 42, no. 11, pp. 904-912, Nov. 1995.

[3.6] P. Rombouts, W. De Wilde, and L. Weyten, "A 13.5-b 1.2-V micro power extended counting A/D converter," *IEEE J. Solid-State Circuits*, vol. 36, no. 2, pp. 176-183, Feb. 2001.

[3.7] A. Agah, K. Vleugels, P. B. Griffin, M. Rodaghi, J. D. Plummer, and B. A. Wolley, "A high-resolution low-power incremental ΔΣ ADC with extended range for biosensor arrays," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1099-1110, Jun. 2010.

[3.8] T. C. Leslie and B. Singh, "An improved sigma-delta modulator architecture," *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 1, New Orleans, LA, May 1-3, pp. 372-375, 1990.

[3.9] J. Silva, U. Moon, J. Steensgaard, and G. C. Temes, “Wideband low-distortion ΔΣ ADC topology,” *Electron. Lett.*, vol. 37, no. 12, pp. 737-738, Jun. 2001.

[3.10] Y. P. Tsividis, P. R. Gray, D. A. Hodges, and J. Chacko, “A Segmented μ-255 law PCM voice encoder utilizing NMOS technology,” *IEEE J. Solid-State Circuits*, vol. sc-11, no. 6, pp. 740-747, Jun. 1976.

[3.11] R. Schreier, J. Silva, J. Steensgaard, and G. C. Temes, “Design-oriented estimation of thermal noise in switched-capacitor circuits,” *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 52, no. 11, pp. 2358-2368, Nov. 2005.

[3.12] J. Markus, J. Silva, and G. C. Temes , “Theory and applications of incremental ΔΣ converters,” *IEEE Trans Circuits Syst. I: Regular Papers*, vol. 51, no. 4, pp. 678-690, Apr. 2004.

[3.13] E. Fogleman, J. Welz, and I. Galton, “An audio ADC delta-sigma modulator with 100 dB SINAD and 102 dB DR using a second-order mismatch-shaping DAC,” in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, pp. 17-20, Sep. 2000.

[3.14] M. Dessouky and A. Kaiser, “ Very low-voltage digital-audio ΔΣ modulato r with 88-Db dynamic range using local switch bootstrapping,” *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 349-355, Mar. 2001.

[3.15] R. T. Baird and T. S. Fiez, “Linearity enhancement of multibit ΔΣ A/D and D/A converters using data weighted averaging,” *IEEE Trans Circuits Syst. II, Analog Digit. Signal. Process*, vol. 42, pp. 753-762, Dec. 1995.

[3.16] Murata Manufacturing, “Application manual for power supply noise suppression and decoupling for digital ICs,” Jul. 2010.

[3.17] F. Maloberti, “Data Converters,” *Springer*, 2007.

[3.18] T. Hayashi, Y. Inabe, K. Uchimura , and A. Iwata, “A multi stage delta-sigma modulator without double integration loop,” *ISSCC Digest of Technical Papers*, pp. 182-183, Feb. 1986.

[3.19] Y. Matsuya, K. Uchimura, A. Iwata, T. Kobayashi, M. Ishikawa and T. Yoshitome, “A 16-bit oversampling A-to-D conversion technology using triple-integration noise shaping,” *IEEE J. Solid-State Circuits*, vol. 22, pp. 921-929, Dec. 1987.

CHAPTER 4. ΔΣ ADC WITH RELAXED FEEDBACK TIMING FOR WIDEBAND AND HIGH ACCURACY

This chapter describes a ΔΣ ADC with realxed feedback timing to achieve wide band and high accuracy. Two slightly different protoypes were designed and fabricated with 0.18*um* 2-poly and 4-metlal CMOS process and measured. Difference betwwen two prototype is the input branch in the modulator. Sampling capacitor and feedback DAC capacitor are separated in Prototype A while they are shared in Protoype B.

4.1 Introduction

Recently, broadband communications system requires high accuracy analog to digital converter with signal bandwidth above 1MHz [4.1]. Generally, a delta-sigma ADC offers high resolution with cheap quantizer by taking advantage of oversampling and noise shaping [4.2]. To achieve wide bandwidth, oversampling ratio should be decreased. Higher order modulator or higher bit quantizer are needed to keep the high resolution. A modulator with higher order noise shaping can cause stability problem. Besides, it results in more power consumption by adding more active components in the modulator. Using a high resolution quantizer also increases the power consumption due to the increased number of comparator [4.3,4] As an alternate solution, the noise-coupled delta-sigma ADC [4.5,6] was proposed in the low distortion architecture [4.7]. Because of the removal of the input signal at the input of the loop filter, each loop filter only processes

the quantization noise. Therefore, the circuit requirements of the loop filter such as opamp DC gain, output swing can be relaxed resulting in low power consumption and excellent linearity. However, one disadvantage of this structure is stringent feedback timing due to the input feedforward path. This means we need to design fast comparator and DEM circuitry causing higher power consumption. Sec. 4.2 describes the proposed method to relax the feedback timing in the ΔΣ modulator. Sec. 4.3 presents the circuit implementation in 0.18μm 2P4M CMOS process. Measurement results follow in Sec. 4.4.

4.2 Proposed ΔΣ modulator with relaxed feedback timing

4.2.1 Low distortion feedforward ΔΣ modulator

Fig. 4.1 shows the second order low distortion feedforward ΔΣ modulator. This architecture has a lot of advantages. First of all, each integrator only processes the quantization noise. Therefore, we can achieve good linearity even with non linear amp. Because quantization noise has white noise spectrum, it will not generate any harmonic components. Also, each integrator output only contains the quantization noise. Since its amplitude is small, we can reduce the power consumption. However, the feedback timing of this architecture is quite stringent because of the input feedforward path. Specially, if we want to design high speed or high accuracy ΔΣ ADC with multi bit quantizer, this timing issue becomes more critical.

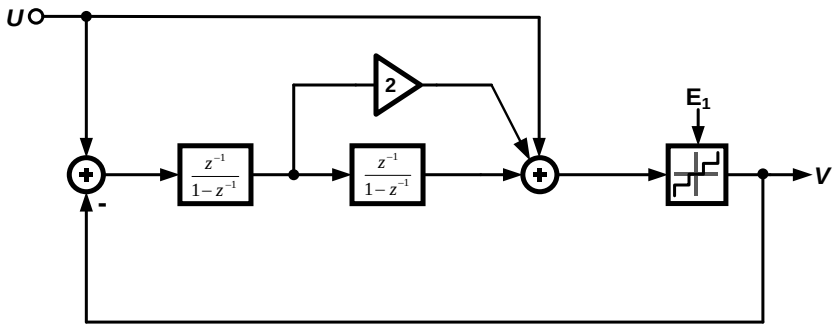


Fig. 4.1 Second order low distortion architecture.

4.2.2 Proposed ΔΣ modulator with relaxed feedback timing

Fig. 4.2 shows the first order single ended switched capacitor circuit and timing diagram of the conventional low distortion architecture [4.8]. To generate modulator output V in Fig 4.2, quantizer needs $V_F[n]$ and $V_I[n]$. And then, digital output, V, should be fed back to the input before $\varphi 2$ for DAC operation. Because $V_F[n]$ is available at the end of $\varphi 1$, we only have non-overlap time between $\varphi 1$ and $\varphi 2$ to perform quantizer and dynamic element matching (DEM) to linearize the DAC mismatch. Therefore, we need fast quantizer and DEM circuitry for high speed operation with multi-bit quantizer to meet timing requirement. This is a potential factor for increasing power consumption.

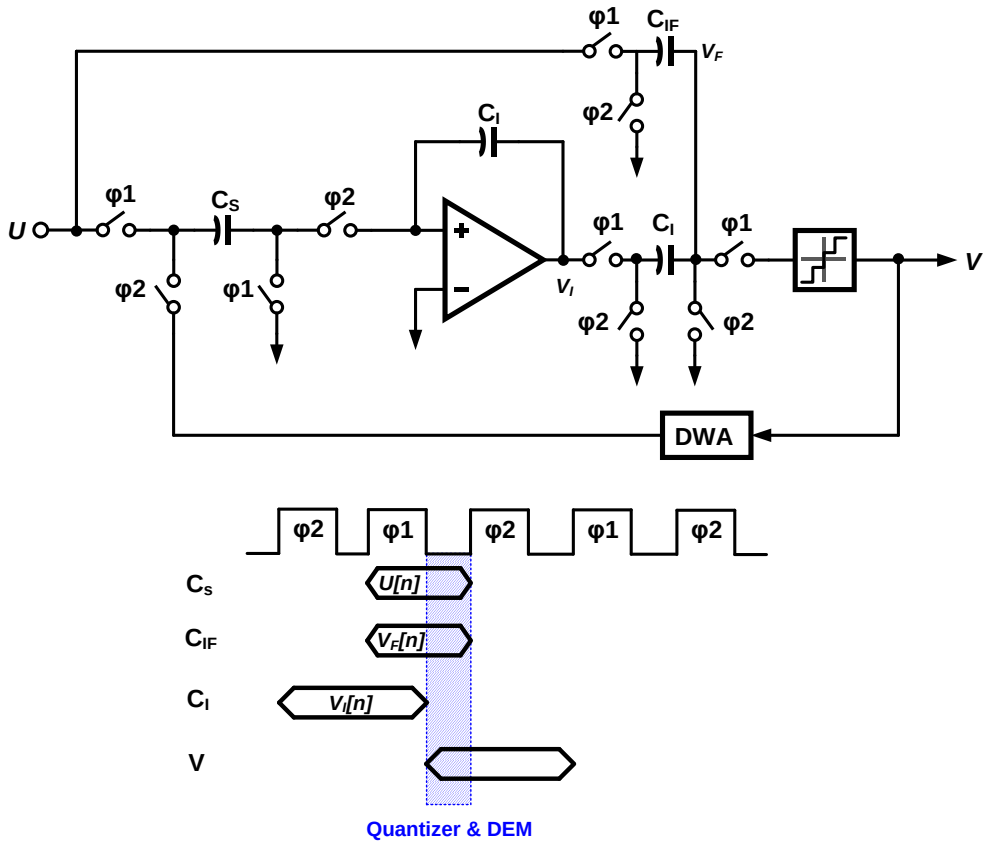


Fig. 4.2 First order switched capacitor circuit and its timing diagram with input feedforward path.

Fig. 4.3 shows the proposed first order switched capacitor circuit and its timing diagram to relax the feedback timing. To generate output V, we still need $V_F[n]$ and $V_I[n]$. Even if $V_F[n]$ is available at the end of $\varphi 1$ same as before, by changing the sampling phase ($\varphi 1$) and integration phase ($\varphi 2$) at the first integrator, DAC operation will be done next $\varphi 1$ instead of $\varphi 2$. In other words, we can have one full clock cycle more to operate the quantizer and DEM circuitry compared to conventional low distortion architecture. Because of the relaxed feedback timing, we can implement low power and low speed

comparator and DEM circuitry.

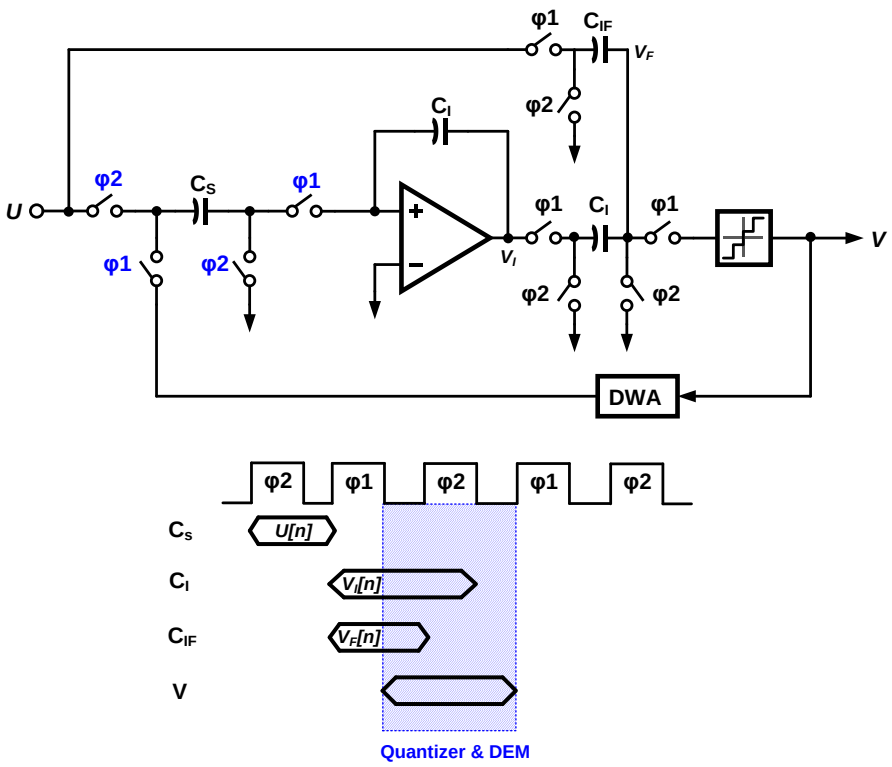


Fig. 4.3 Proposed first order switched capacitor circuit and its timing diagram with input feedforward path.

Main source of the delay in the feedback path is quantizer and DEM to shape the DAC mismatch error. Fig. 4.4 shows conventional DWA block diagram. It consists of thermometer to binary encoder, pointer generator, and shifter. Pointer indicates which unit element should be used as the starting point in the DAC operation. Shifter maps the relationship between the thermometer code from the quantizer and DAC unit elements. As shown in Fig. 4.4, because encoder and pointer generator operation is done outside

the loop, their delay does not affect feedback operation. However, shifter delay directly reflects on the feedback delay because it is in the modulator loop. Therefore, delay of the shifter is critical to determine the total delay in the feedback operation.

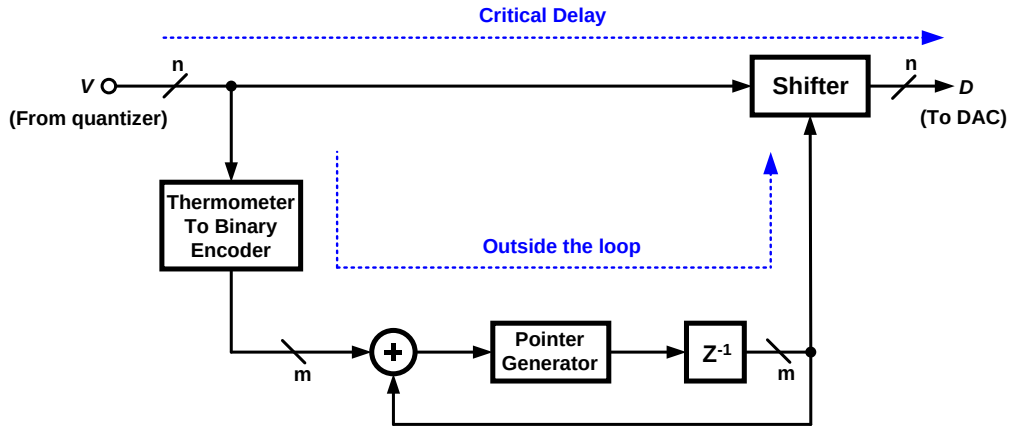
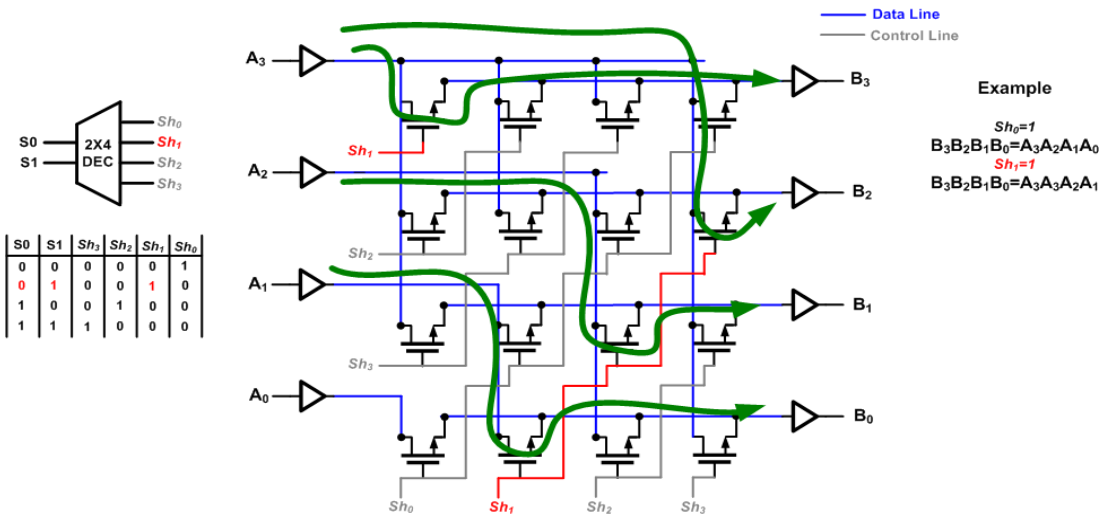


Fig. 4.4 Block diagram of DWA.

There are two types of shifter. One is a barrel shifter and the other one is logarithmic shifter [4.9]. Each shifter has trade-off between power consumption and propagation delay. Fig. 4.5 shows the example of 4-bit barrel shifter. Barrel shifter needs a control signal (Sh_0~ Sh_3) for every shift bit as shown in Fig. 4.5. Based on the control signal 4 bit input data (A_0~ A_3) will be shifted. To shift the bit, only one control signal should be high. This function can be realized by using decoder. Because of the decoder, barrel shifter will consume more power than logarithmic shifter. For example, if we want to shift 1 bit to the right Sh_1 signal should be on. When Sh_1 is high, each input data will transfer to the output passing through only on gate. Therefore, the propagation delay is constant and independent of shifter value or shifter size. It means that barrel shifter is

useful for high speed operation.



S0	S1	Sh3	Sh2	Sh1	Sh0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Fig. 4.5 Example of 4-bit barrel shifter.

Fig. 4.6 shows the part of 8 bit logarithmic shifter. Compared to the barrel shifter, logarithmic shifter does not need to have decoder for control signal, because every control signal should be on or off to shift the bit. First stage shifts input data 0 or 1 bit based on the control signal. Second stage shifts data 0 or 2 bit. Third stage shifts data 0~4 bit. Therefore, combination of 3 stages can shift input data from 0 to 7 bit. For example, to shift the input data by 2 bit in Fig. 4.6, control signal should Sh_0=0, Sh_1=1, and Sh_2=0. In other words, first stage is 0 bit shift, second stage gives 2 bit shift, and third stage gives 0 bit shifts. Compared to barrel shifter, input data should pass through every stage in the logarithmic shifter. Thus, propagation delay is large and depends on the number of stages. More practical propagation delay can be estimated by using equation of Elmore delay [4.10].

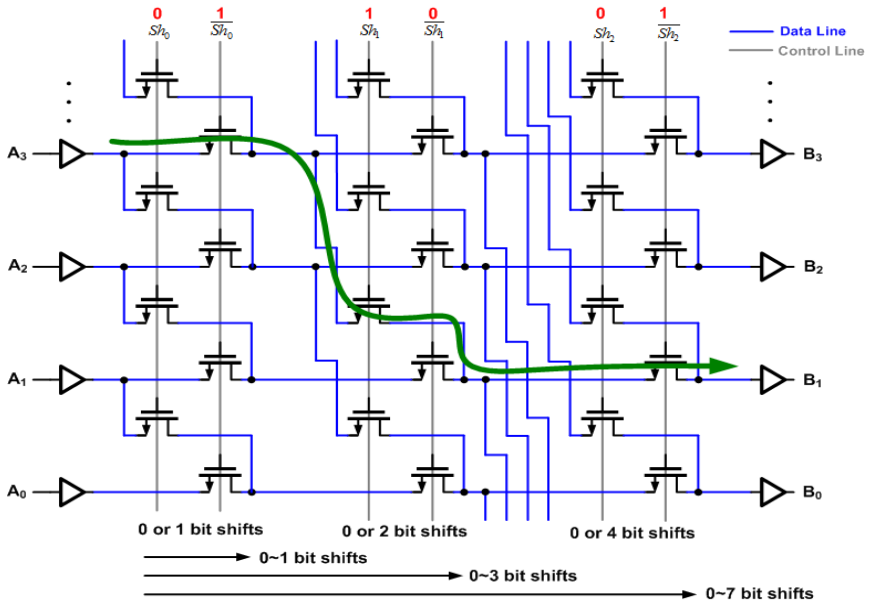


Fig. 4.6 Example of 8-bit logarithmic shifter.

4.3 Circuit implementation

The proposed ΔΣ modulator was implemented in 0.18μm 2-poly and 4-metal CMOS process. Fig. 4.7 shows the realized the ΔΣ modulator using self noise coupling [4.11] and relaxed feedback timing technique. In this architecture, quantization noise is extracted, delayed, and subtracted at the summing node before the quantizer. The injected shaped quantization noise effectively increases the order of noise shaping by one without adding active components. Therefore, only 3 integrators are needed to achieve third order noise shaping by using noise coupling technique while 4 integrators are required in conventional ΔΣ modulator. Also, we are able to use low power consuming logarithmic shifter and low speed comparator because of the relaxed feedback timing. Half clock cycle delay from the input signal path and one full clock

cycle delay in the feedback path came from changing sampling and integrator phase.

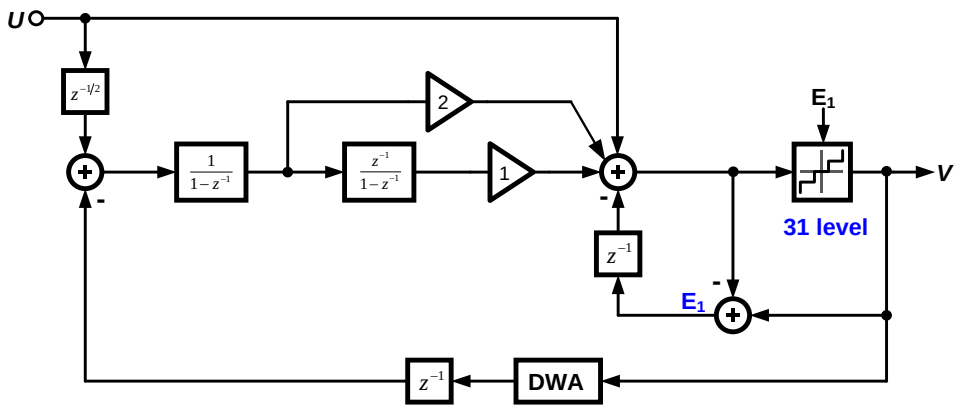


Fig. 4.7 Proposed ΔΣ modulator with relaxed feedback timing.

Fig. 4.8 shows the simplified switched capacitor circuit diagram. The input sampling and feedback DAC capacitor are separated to avoid signal dependent reference error [4.12]. Poly-insulator-ploy (P1P) capacitor was used instead of using metal-insulator-metal (MIM) to achieve better matching performance even if PIP capacitor has more parasitic capacitance based on the design manual. Bootstrapped switch was used for input sampling switch to achieve high linearity and prevent signal dependent charge injection [4.13]. One full clock cycle delay of the digital output for noise coupling is realized by a simple D flip flop.

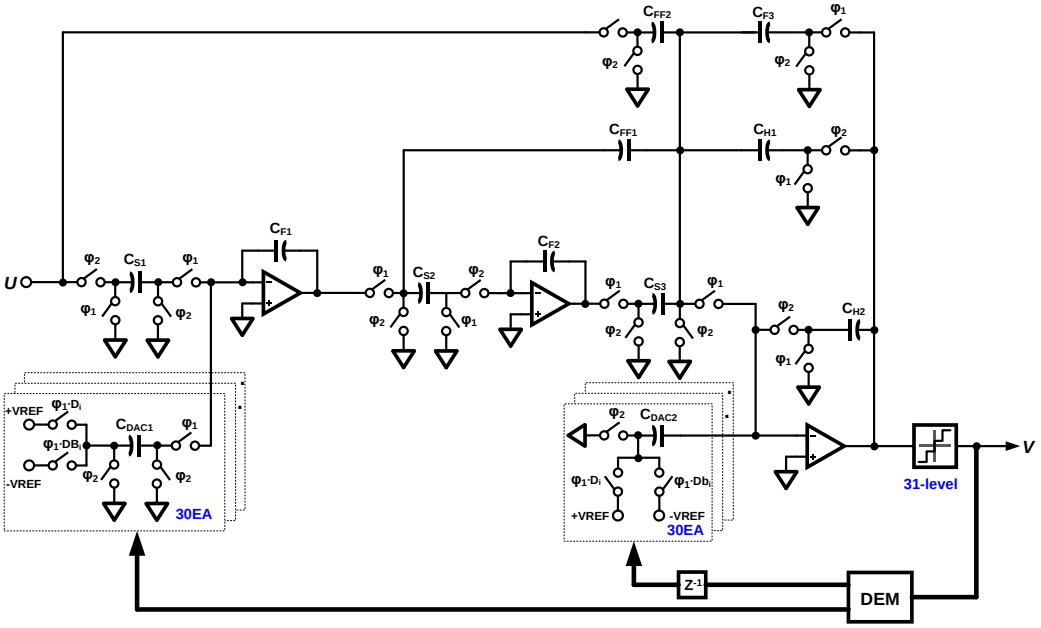


Fig. 4.8 Single ended switched capacitor circuits of ΔΣ modulator.

Small signal swing due to the low distortion architecture allows the use of power efficient telescopic cascode amplifier with switched-capacitor common mode feedback circuit as shown in Fig. 4.9. Therefore, two integrators and one active adder used that structure with 3.3 power supply. Noise contribution from the top PMOS transistors was minimized by assigning the large overdrive voltages for the given output swing requirement. Also, NMOS input pairs were used to maximize the transconductance with given energy. 5-bit quantizer consists of preamplifier, track and latched, SR latched as shown in Fig. 3.13. Proposed relaxed feedback timing technique allows to use logarithmic shifter for low power consumption. Therefore, data weighted averaging (DWA) with logarithmic shifter was utilized to filter out mismatch error of the 30-level DAC [4.14]. Two sets of DWA were implemented to relax the circuit design complexity

as illustrated in Fig. 4.10. DWA circuitry operates at 1.5V power supply and their outputs are shifted by level up shifter to 3.3V for DAC operation. Fig. 4.11 shows implemented cross coupled PMOS load level up shifter [4.15].

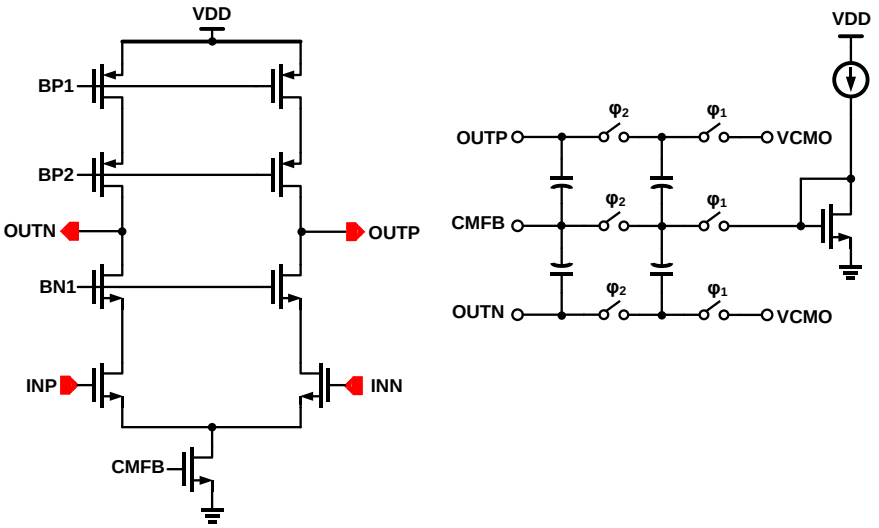


Fig. 4.9 Telescopic cascode opamp with common mode feedback.

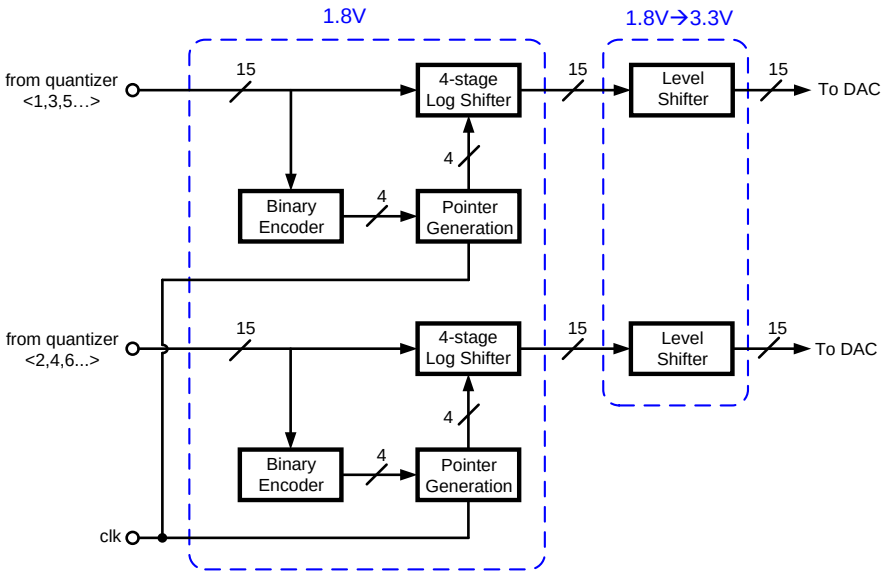


Fig. 4.10 Block diagram of the two sets of DWA.

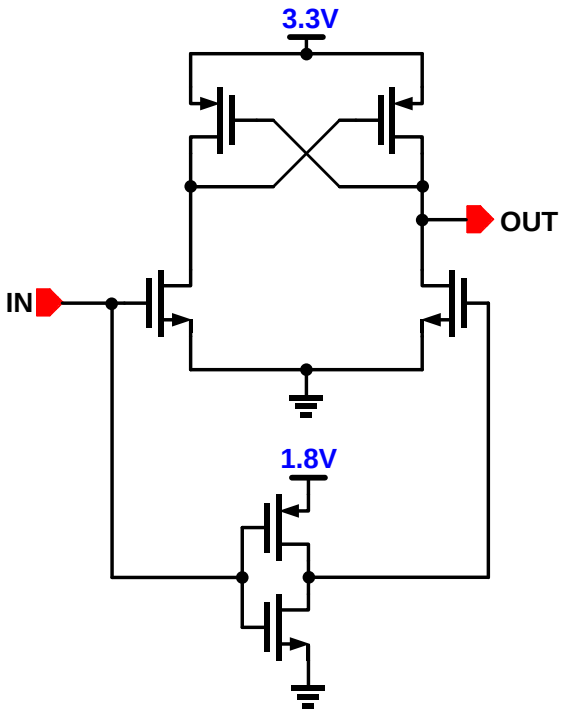


Fig. 4.11 Cross coupled level up shifter.

In this implementation, two slightly different prototypes were fabricated. In prototype A, the sampling capacitor is separated from DAC capacitor while they are shared in prototype B. Theoretically, prototype B has half of kT/C noise than prototype A due to the lesser capacitor at the input branch of the modulator. However, prototype B suffers from signal dependent reference error [4.12]. The designed and fabricated two prototypes are exactly the same except for input sampling and DAC structure. Fig. 4.12 shows the input branch schematic of the prototypes A and B.

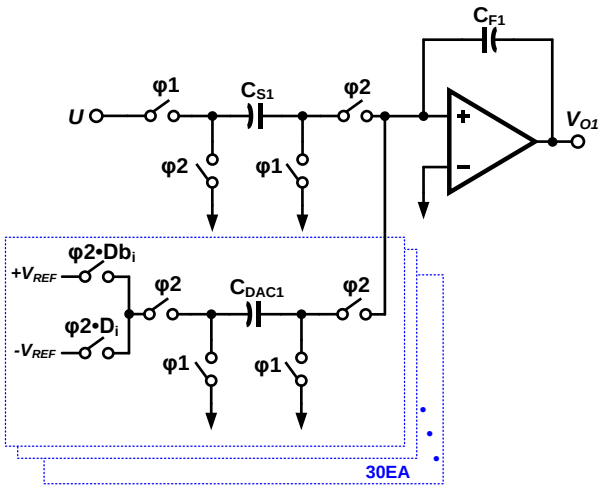


Fig. 4.12 (a) Input branch of Prototype A.

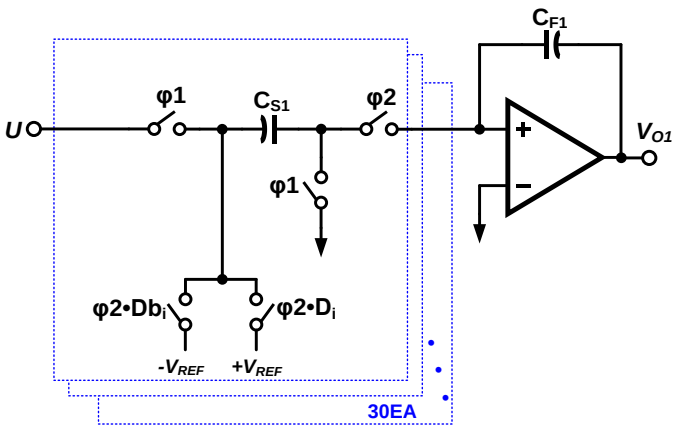


Fig. 4.12 (b) Input branch of Prototype B.

4.4 Experimental results

4.4.1 Test setup

A 4-layer PCB was designed as shown in Fig. 4.13. Top and bottom layers were used for signal routing. The 2nd layer is for ground plane and the 3rd layer is for power plane. The 2nd layer and 3rd layer are filled with copper to reduce the parasitic resistance. Decoupling capacitors for power pins of the DUT (Device Under Test) were placed as close as possible to the chip. Also, the decoupling capacitance difference is less than 10:1 to prevent anti-resonance phenomenon where the self-resonant frequencies of two capacitors differs. [4.16]. Reference voltages and control signal is generated from variable resistors and reference generator. Different power supply voltages to the chip are generated from LDO (Low Dropout Regulator) and variable resistors. Balun generates the differential signal from single ended signal at the left side of the chip. One 8x2 connectors is used to extract the reference clock and digital output of the ADC. Fig. 4.14 shows the test setup. Fig. 4.15 shows the block diagram of the test setup. Differential input signal is generated by signal generator, band-pass filter, and balun. Clock from signal generator is applied to the DUT with bias-tee to move the common mode voltage. 5-bit digital output is captured in the Logic Analyzer after passing through digital buffer.

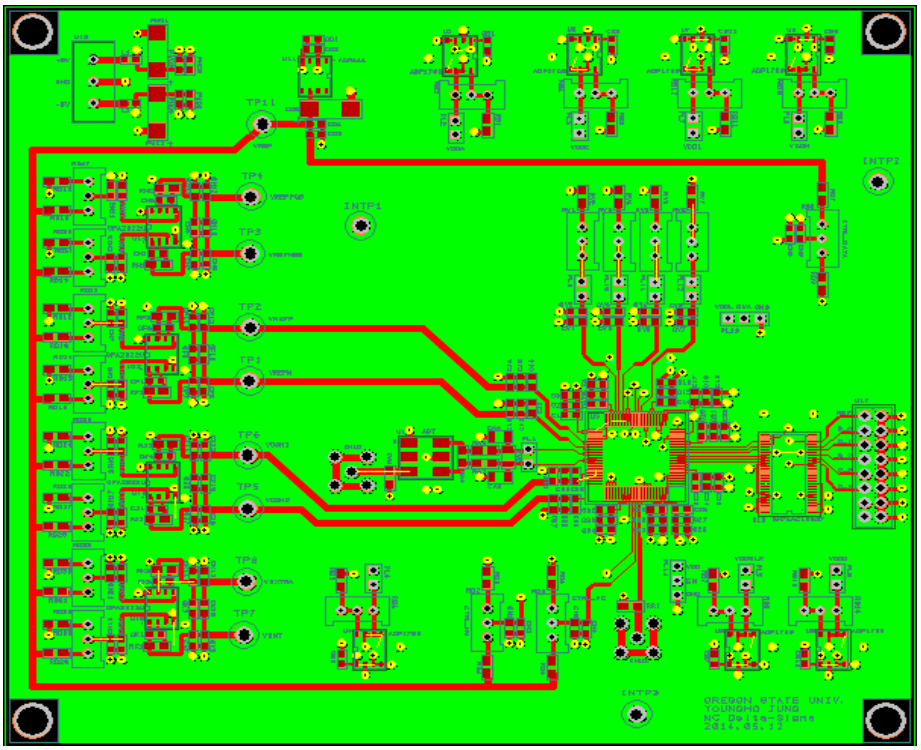


Fig. 4.13 PCB layout for ΔΣ ADC with relaxed feedback timing.

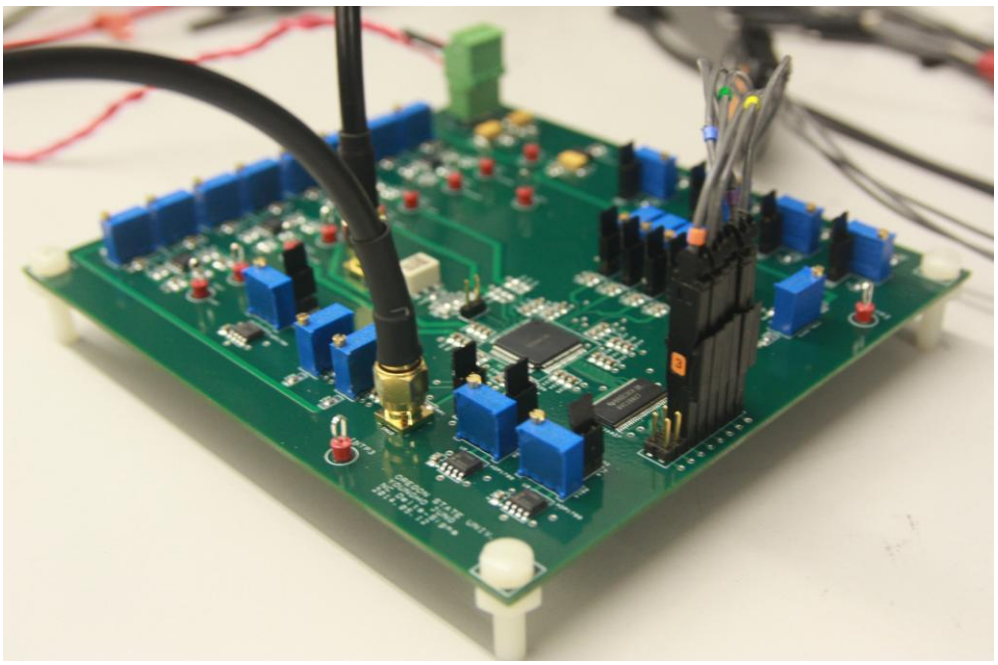


Fig. 4.14 Test setup.

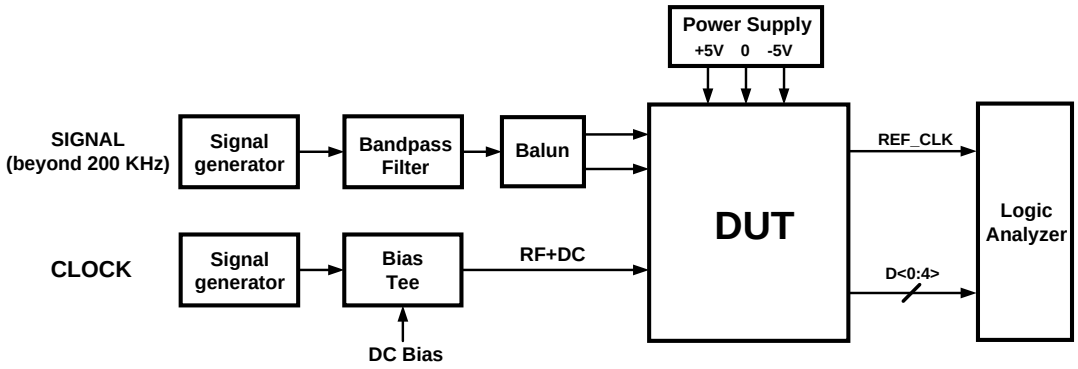


Fig. 4.15 Block diagram of the test setup.

4.4.2 Measurement results

Fig. 4.16 shows the die micrograph. Prototypes A and B occupy $4.02mm^2$ $(2810\mu m \times 1430\mu m)$. Fig. 4.17 and Fig. 4.18 shows the measured output spectra of prototypes A and B with 100MHz sampling clock when the input signal amplitude is -87.5dBFS and -92.8dBFS, respectively. Prototype B achieves higher dynamic range than Prototype A as we expected. Fig. 4.19 shows the measured output spectrum of prototype A at 100MHz sampling clock and 201KHz input signal. It shows 81.2dB peak SNDR in the 2.1MHz signal band. Fig. 4.20 shows peak 72.4dB SNDR up to 2.1MHz signal band with the same test environment. The measurement results are summarized in Table 4.1.

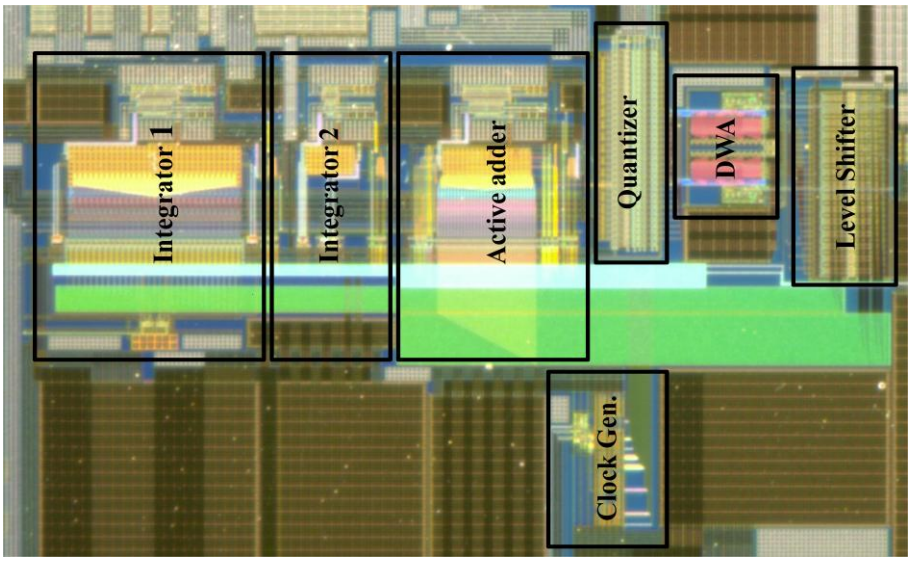


Fig. 4.16 Die micrograph.

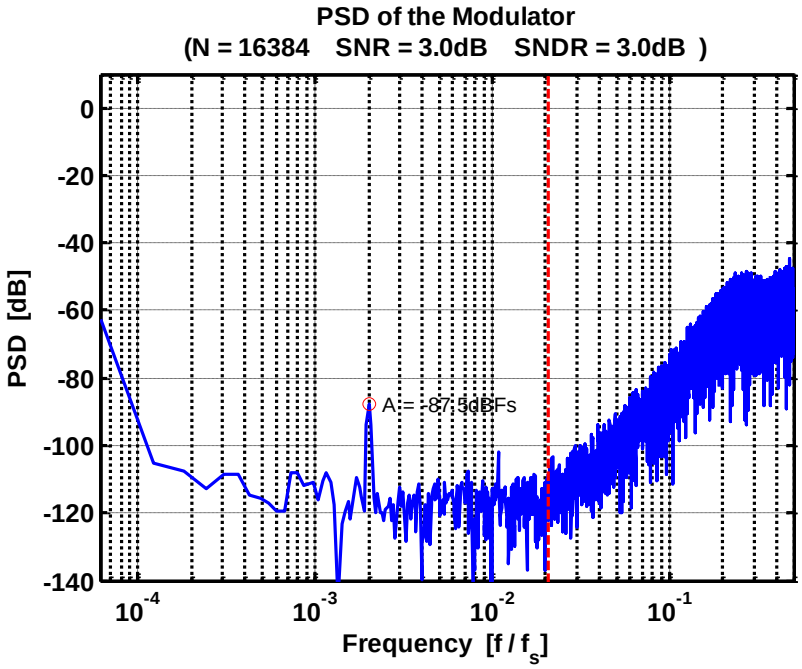


Fig. 4.17 Measured output spectrum of Prototype A.

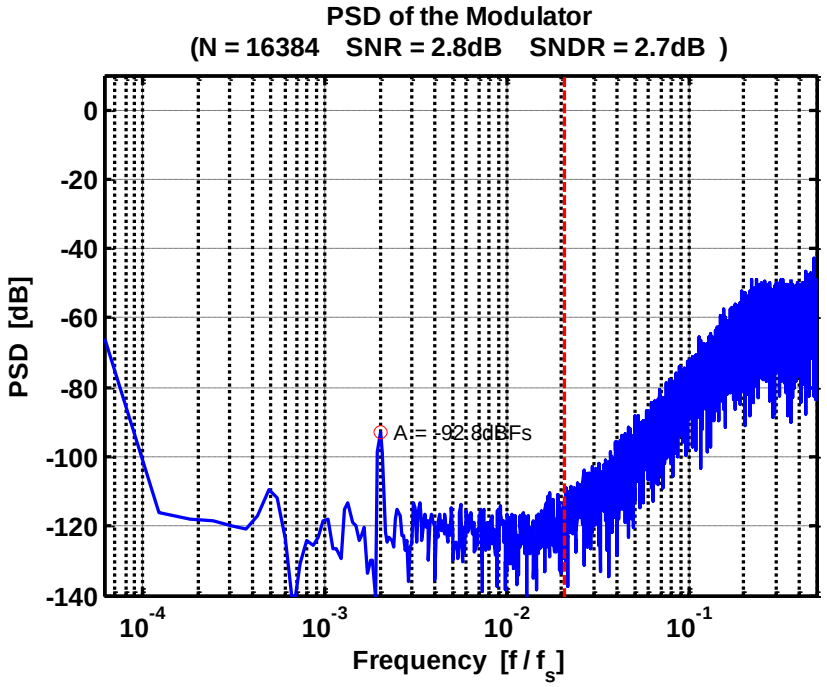


Fig. 4.18 Measured output spectrum of Prototype B.

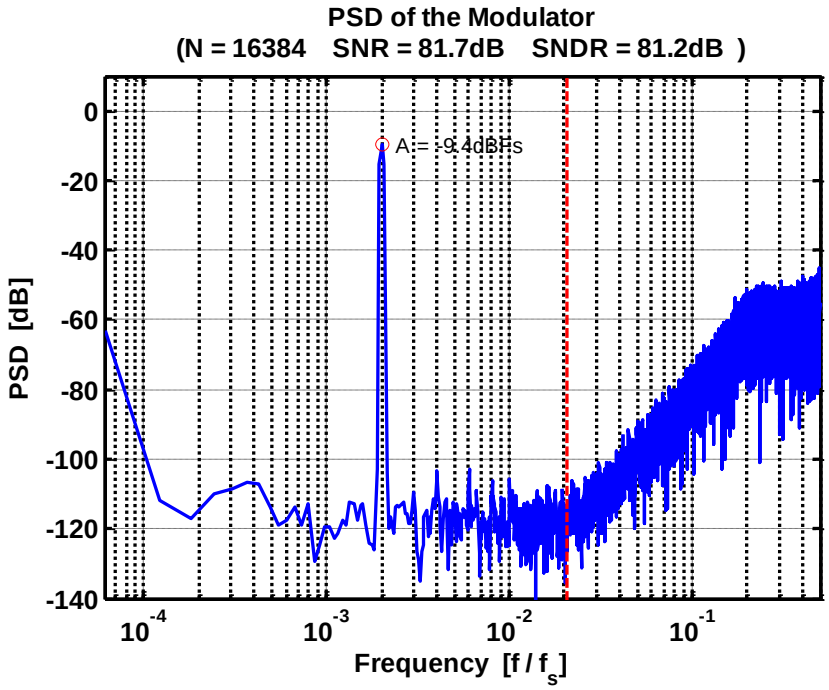


Fig. 4.19 Measured output spectrum of Prototype A.

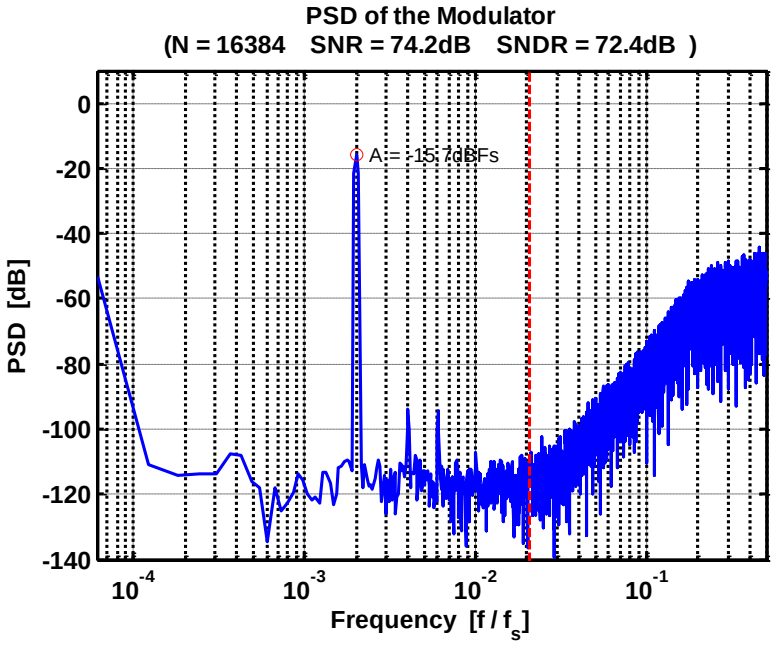


Fig. 4.20 Measured output spectrum of Prototype B.

Table 4.1 Summary of measured performance

	Prototype A	Prototype B
Sampling frequency	100MHz	100MHz
Signal bandwidth	2.1MHz	2.1MHz
OSR	24	24
Dynamic range	90.5dB	95.6dB
Peak SNDR	81.2dB	72.4dB
SFDR	95.1dB	80dB
Power consumption	35mW(A) 63mW (D)	
Power supply	3.3V(A)/1.5V(D)	
Process	0.18μm 2P4M CMOS	

4.4.3 Summary

The relaxed feedback timing ΔΣ ADC with noise coupling was described and analyzed. Two prototype ΔΣ modulator were fabricated with 0.18μm 2P4M CMOS process. In prototype A, sampling capacitor is separated from DAC capacitor while they are shared in prototype B. Prototype A achieves 90.5dB dynamic range, 81.2dB SNDR, and 95.1dB SFDR while prototype B achieves 95.6dB dynamic range, 72.4dB SNDR, and 80dB SFDR up to 2.1MHz with same testing environment because prototype B suffers from higher harmonic distortion than prototype A. The total power consumption is 98mW with power supply (analog 3.3V, digital 1.5V).

References

[4.1] K. Nam, S. M. Lee, D. K. Su, and B. A. Wooley, "A low-voltage low power sigma-delta modulator for broadband analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 40, no. 9, pp. 1855-1864, Sep. 2005.

[4.2] R. Schreier and G. C. Temes, "*Understanding of Delta-Sigma Data Converters"*, New York: Wiley, 2005.

[4.3] O. Rajaee, T. Musah, N. Maghari, S. Takeuchi, M. Aniya, K. Hamashita, and U. K. Moon, "Design of a 79dB 80MHz 8x-OSR hybrid delta-sigma/pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 719-730, Apr. 2010.

[4.4] R. Zanbaghi, S. Saxena, G. C. Temes, and T. S. Fiez, "A 75-dB SNDR, 5-MHz bandwidth stage-shard 2-2 MASH ΔΣ modulator dissipating 16mW power," *IEEE Trans.*

Circuits Syst. I: Regular Papers, vol. 59, no. 8, pp. 1614-1625, Aug. 2012.

[4.5] K. Lee, J. S. Chae, M. Aniya, K. Hamashita, K. Takasuka, and G. C. Temes, "A noise-coupled time-interleaved delta-sigma ADC WITH 4.2MHz bandwidth, -98dB THD, and 79dB SNDR," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2601-2612, Dec. 2008.

[4.6] Y. Wang and G. C. Temes "ΔΣ ADCs with second-order noise-shaping enhancement," *Proc. IEEE MWSCAS'09*, pp.345-348, Aug. 2009.

[4.7] J. Silva, U. Moon, J. Steensgaard, and G. C. Temes, "Wideband low-distortion ΔΣ ADC topology," *Electron. Lett.*, vol. 37, no. 12, pp. 737-738, Jun. 2001.

[4.8] A. Gharbiya, and D. A. Johns, "On the implementation of input-feedforward delta-sigma modulator," *IEEE Trans Circuits Syst. II: Express Briefs*, vol. 53, no. 6, pp. 453-457, Jun. 2006.

[4.9] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, "Digital Integrated Circuits," 2nd Edition, Prentice Hall, 2003.

[4.10] E. Elmore, "The transient response of damped linear networks with particular regard to wideband amplifiers," *J. Applied Physics*, pp. 55-63, Jan. 1948.

[4.11] K. Lee, M. R. Miller, and G. C. Temes, "An 8.1mW, 82dB delta-sigma ADC with 1.9MHz BW and -98dB THD," *IEEE J. Solid-State Circuits*, vol. 44, no. 8, pp. 2202-2211, Aug. 2009.

[4.12] E. Fogleman, J. Welz, and I. Galton, "An audio ADC delta-sigma modulator with 100 dB SINAD and 102 dB DR using a second-order mismatch-shaping DAC," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, pp. 17-20, Sep. 2000.

[4.13] M. Dessouky and A. Kaiser, "Very low-voltage digital-audio ΔΣ modulator with 88-dB dynamic range using local switch bootstrapping," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 349-355, Mar. 2001.

[4.14] R. T. Baird and T. S. Fiez, "Linearity enhancement of multibit ΔΣ A/D and D/A converters using data weighted averaging," *IEEE Trans Circuits Syst. Ⅱ, Analog Digit. Signal. Process*, vol. 42, pp. 753-762, Dec. 1995.

[4.15] K. H. Koo, J. H. Seo, M. L. Ko, and J. W. Kim, "A new level-up shifter for high speed and wide range interface in ultra deep sub micron," *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 2, pp. 1063-1065, 2005.

[4.16] Murata Manufacturing, "Application manual for power supply noise suppression and decoupling for digital ICs," Jul. 2010.

CHAPTER 5. DOUBLE NOISE COUPLING ΔΣ ADC

In this chapter, a novel ΔΣ analog-to-digital (ADC) architecture is proposed for second-order noise shaping enhancement. The new architecture is less dependent on the opamp DC gain than the earlier ΔΣ ADC with second-order noise shaping enhancement. Also, the proposed architecture reduces the complexity of the clock generator and zero optimization compared to the earlier one. A ΔΣ ADC using the new configuration was designed and simulated. The results verify the advantages of the proposed structure.

5.1 Introduction

Recent advances in wired and wireless communications demand ADCs with increased signal bandwidth and accuracy. ΔΣ ADCs can provide high resolution and linearity even with a low resolution quantizer by taking advantage of oversampling and noise shaping. However, to obtain wide bandwidth in delta-sigma ADCs is quite challenging. It can be achieved by increasing the sampling frequency or reducing the oversampling ratio. However, the sampling frequency is limited by process technology, and higher sampling frequency also requires higher power consumption. Also, reducing the oversampling ratio decreases the SQNR (Signal to Quantization Noise Ratio). One of the options to maintain the SQNR is to increase the modulator's order. But a modulator with higher order loop filter will result in more power consumption. [5.2,3] As an alternative, ΔΣ ADCs using noise coupling techniques were introduced [5.1,4] to enhance the noise

shaping order without adding active blocks. In this chapter, a novel ΔΣ ADC architecture realizing double noise coupling techniques is proposed. It is less sensitive to finite opamp DC gain than the earlier second order noise coupling structure of ref. [5.1] and requires much simpler digital circuitry.

5.2 Double noise coupling ΔΣ ADC

Fig. 5.1 shows a ΔΣ ADC using second order noise coupling technique [5.1]. This architecture can save an active component compared to ΔΣ ADCs using first order noise coupling [5.4]. It needs only one integrator and one active adder to realize 3rd-order noise shaping. However, in order to implement the term z^{-2} (i.e, two full clock cycle delay), the clock generator needs to provide four additional clock phases for the active adder [5.1]. Therefore, the complexity of the clock generator is increased in this architecture. Also, such ΔΣ ADC is more sensitive to finite opamp DC gain than a single noise-coupled one [5.4], because of the reduced number of opamps. To overcome these disadvantages, a novel ΔΣ ADC using double noise coupling techniques is proposed. It is shown in Fig. 5.2. In contrast to earlier ΔΣ ADCs using first- or second-order noise coupling technique, the proposed ΔΣ ADC couples the quantization noise to the modulator twice. The quantization noise E_1 is delayed by one clock cycle and subtracted at the summing node before the quantizer. The shaped quantization noise $E_2 = E_1 \cdot (1 - z^{-1})$ resulting from the first noise coupling is again delayed and subtracted at the summing node, giving

$$V(z) = W(z) + E_2 \cdot (1 - z^{-1}) \tag{5.1}$$

$$E_2 = E_1 \cdot (1 - z^{-1}) \tag{5.2}$$

$$V(z) = W(z) + E_1 \cdot (1 - z^{-1})^2 \tag{5.3}$$

Therefore, if *H(z)* is an integrator, the z-domain output is

$$V(z) = U(z) + E_1 \cdot (1 - z^{-1})^3 \tag{5.4}$$

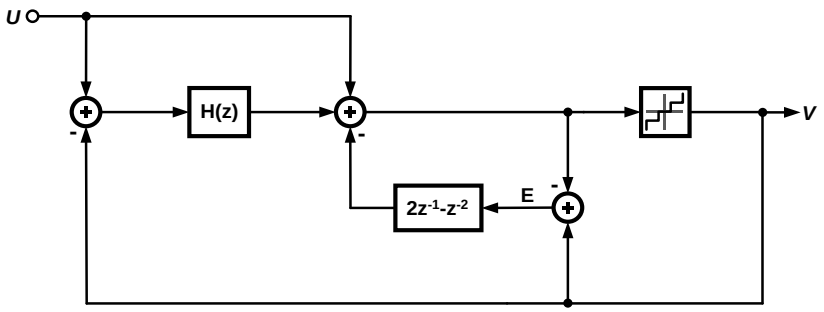


Fig. 5.1 ΔΣ ADC with second order noise coupling. [5.1]

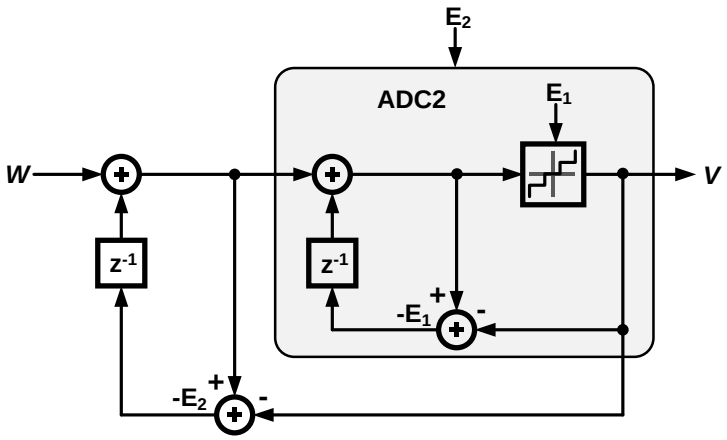


Fig. 5.2 The proposed ΔΣ ADC using double noise coupling technique.

By injecting quantization noise into the modulator twice, the proposed modulator thus provides a 3rd-order noise shaping, as did the ones described in refs. [5.1,4]. However, the ΔΣ ADC of Fig. 5.2 needs only z^{-1} delay blocks to implement double noise coupling, and hence the complexity of the clock generator is significantly reduced. Next, the opamp gain sensitivity is investigated. Assuming that all opamps have the same DC gain, the quantization noise floor is determined by the total DC gain of all opamps used in the modulator. Therefore, a modulator with fewer opamps is more sensitive to finite DC gain. Fig. 5.3 compares the gain dependence of a third order ΔΣ ADC using second-order noise coupling [5.1] with the proposed one, when all opamp gains are varied simultaneously. As expected, the proposed modulator is less sensitive to low opamp DC gain.

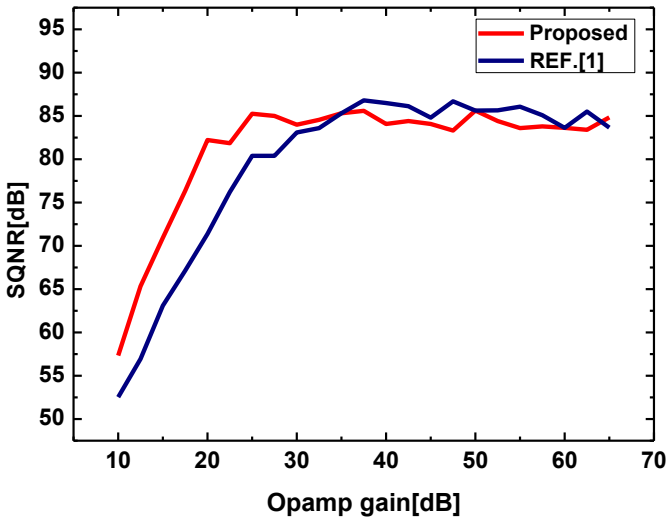


Fig. 5.3 SQNR dependence on opamp DC gain.

In ΔΣ ADCs, one can apply zero optimization technique to increase the SQNR [5.5].

However, in a ΔΣ ADC using second-order noise coupling [5.1] it is difficult to use zero optimization, because the coefficient needed in the noise-coupling path to implement the zero is a fractional digital number. Hence, zero optimization requires a complex digital multiplier. By contrast, in the double noise coupling ΔΣ ADC, zero optimization can be carried out easily in the analog domain by choosing proper capacitor value.

5.3 Design example

As a demonstration of the proposed design technique, a third-order double-noise coupling ΔΣ ADC was designed with an oversampling ratio of 16 and an SQNR of 80 dB. The single-ended circuit diagram of the proposed modulator is shown in Fig. 5.4. The z^{-1} delay delay blocks were realized using the scheme of ref. [5.1]. Also, an input feed-forward path [5.6] and a 15-level quantizer were used to relax the demand on the analog loop filter, and to improve the accuracy without increasing the modulator order or the oversampling ratio.

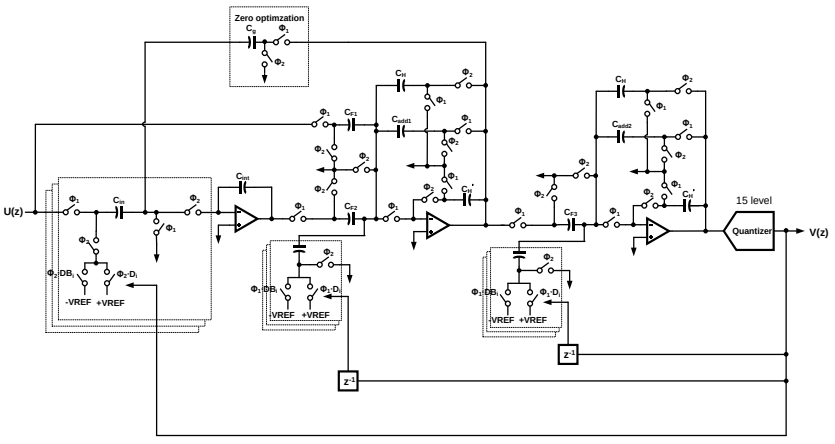


Fig. 5.4 The single ended circuit diagram of the proposed ΔΣ ADC.

5.4 Simulation results

The dynamic behavior of the proposed modulator was simulated using the Cadence Spectre simulator. Fig. 5.5 shows the simulated output spectrum of the proposed ΔΣ ADC, with and without zero optimization. As expected, the ΔΣ ADC provides a 3rd order noise shaping, and zero optimization increases the SQNR by about 8 dB.

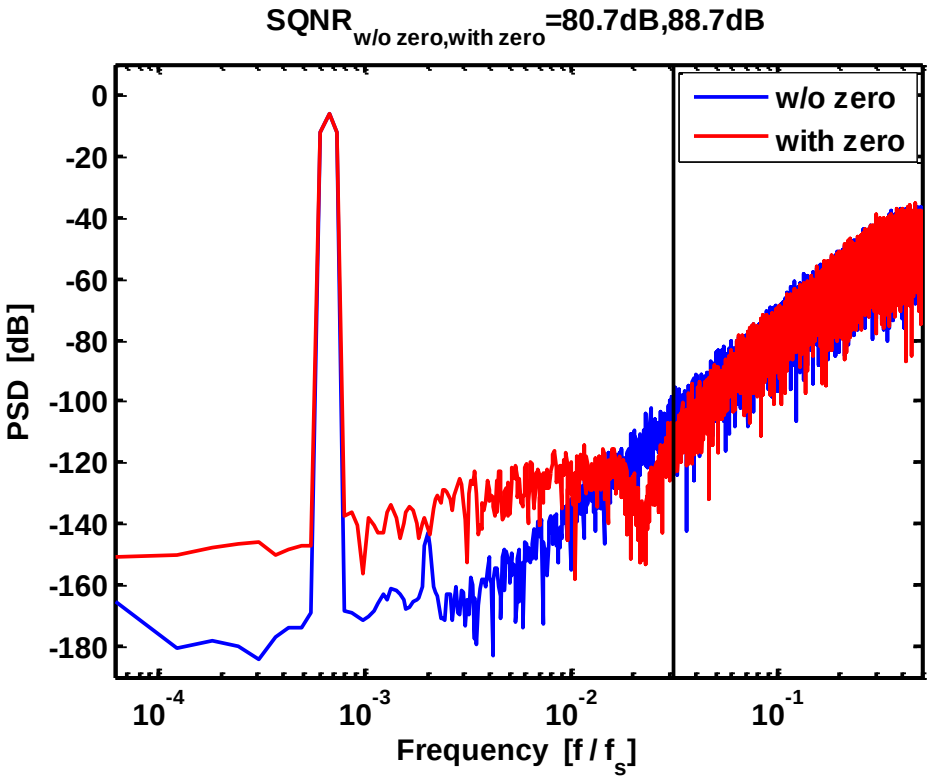


Fig. 5.5 Simulated PSD of the proposed ΔΣ ADC with and without zero.

5.5 Summary

A novel double-noise-coupling ΔΣ ADC configuration is proposed for high bandwidth and high accuracy performance, combined with low power dissipation. The proposed architecture is less sensitive to finite opamp DC gain effects than the previous one described in [5.1]. Moreover, the new double-noise-coupling ΔΣ ADC reduces the complexity of the clock generator, and of the zero optimization circuitry. A third-order modulator was simulated to verify the effectiveness of double noise coupling technique. Using zero optimization, the SQNR was increased by 8 dB.

References

[5.1] Y. Wang and G. C. Temes, "ΔΣ ADCs with Second-Order Noise-Shaping Enhancement", *IEEE MWCAS* '09, Aug. 2009, pp.345-348.

[5.2] O. Rajaee, T. Musah, N. Maghari, S. Takeuchi, M. Aniya, K. Hamashita, and U.K. Moon, "Design of a 79 dB 80MHz 8X-OSR Hybrid Delta-Sigma/Pipelined ADC", *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 719-730, Apr. 2010.

[5.3] R. Zangbaghi, T. S. Fiez, G. C. Temes, "A New Zero-optimization Scheme for Noise-Coupled ΔΣ ADCs", *IEEE Circuit and Systems*, May 2010, pp. 2163-2166.

[5.4] K. Y. Lee, M. R. Miller, and G. C. Temes, "An 8.1mW,82 dB Delta-Sigma ADC With 1.9 MHz BW and -98 dB THD", *IEEE J. Solid-State Circuits*, vol. 44, no. 8, pp. 2202-2211, Aug. 2009.

[5.5] R. Schreier and G. C. Temes, "*Understanding of Delta-Sigma Data Converters"*, New York: Wiley, 2005.

[5.6] J. Silva, U. Moon, J. Steensgaard and G. C. Temes, "Wideband low-distortion delta-sigma ADC topology", *Electronics Letters*, vol.37, no.12, pp.737-738, Jun. 2001.

CHAPTER 6. CONCLUSION

In this dissertation, first, the incremental ADC was discussed and analyzed. To achieve widebandwidth, high accuracy, and low latency an incremental ADC with extended counting and 2+2 MASH incremental ADC were designed and fabricated in 0.18μm 2P4M CMOS process. Incremental ADC with extended counting ADC achieves 91.6dB dynamic range and 77.8dB peak SNDR in 0-1.25MHz signal band. The total power consumption is 53.5mW. The 2+2 MASH incremental ADC achieves 94.2dB dynamic range and 74.8dB peak SNDR up to 1.25MHz signal band. The total power consumption is 67mW.

Secondly, relaxed feedback timing ΔΣ ADC with noise coupling was proposed. Because of the relaxed feedback timing, we can utilize the low speed comparator and DEM circuitry resulting in low power consumption. Two slightly different prototypes were implemented in 0.18μm 2P4M CMOS process. In prototype A, the sampling capacitor is separated from the DAC capacitor while they are shared in prototype B. Theoretically, prototype B has half of kT/C noise than prototype A due to the less capacitor at the input branch of the modulator. However, prototype B suffers from signal dependent reference error. Prototype A achieves 90.5dB dynamic range, 81.2dB peak SNDR, and 95.1dB SFDR in the 2.1MHz signal band. On the other hand, prototype B achieves 95.6dB dynamic range, 72.4dB peak SNDR, and 80dB SFDR up to 2.1MHz signal band with same test environment. Based on the measurement result, prototype B where sampling capacitor is shared with DAC capacitor suffers from higher harmonic

distortion than prototype A. Total power consumption is 98mW.

Finally, a double noise coupled ΔΣ modulator was proposed. The proposed architecture is less sensitive to finite opamp DC gain effects and needs less complex clock generator than the second order noise shaping ΔΣ modulator.