AN ABSTRACT OF THE DISSERTATION OF

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Title: Low Power Design Techniques for High Speed Pipelined ADCs

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Real world is analog but the processing of signals can best be done in digital domain. So the need for Analog to Digital Converters(ADCs) is ever rising as more and more applications set in. With the advent of mobile technology, power in electronic equipment is being driven down to get more battery life. Because of their ubiquitous nature, ADCs are prime blocks in the signal chain in which power is intended to be reduced. In this thesis, four techniques to reduce power in high speed pipelined ADCs have been proposed. The first is a capacitor and opamp sharing technique that reduces the load on the first stage opamp by three fold. The second is a capacitor reset technique that aids removing the sample and hold block to reduce power. The third is a modified MDAC which can take rail-to-rail input swing to get an extra bit thus getting rid of a power hungry opamp. The fourth is a hybrid architecture which makes use of an asynchronous SAR ADC as the backend of a pipelined ADC to save power. Measurement and simulation results that prove the efficiency of the proposed techniques are presented.

Low Power Design Techniques for High Speed Pipelined ADCs

by

Naga Sasidhar

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APPROVED:

Co-Major Professor, representing Electrical and Computer Engineering

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Dean of the Graduate School

I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Naga Sasidhar, Author

ACKNOWLEDGEMENTS

Before starting graduate school, my idea of PhD is to become an expert. Little did I know that it is something more. And that too when it is in the field of Analog Circuits, it is something else. At the end of it I am sure I have a long way to go. But the best thing is I am on the right way and I am confident that I will reach there.

I am indebted to my advisor Prof.Un-Ku Moon who gave me the opportunity to work with him. He is both technically and personally superb. I have enjoyed his nature of being critical when it comes to feedback yet at the same time being supportive to forward the end goal. His insight into intricate circuit design issues is something that I hope to have learnt.

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Chapter 1 . INTRODUCTION

1.1 Background

Analog to Digital converters are essential blocks in any signal chain. The fact that processing of signals is best done in digital domain whereas real world is analog necessitates ADCs be present everywhere. Also, many of the modern communication channels require ADCs operating at different speeds and resolution. Of the architectures around such as flash, sub-ranging, 2-step, pipeline, SAR & delta sigma, pipeline falls in the sweet spot of medium to high resolution and high speed where many applications exist. This fact has evoked much interest in this architecture and it continues to grow. Some of the applications for pipeline ADCs include video & bluetooth which like many others are used mostly in battery operated gadgets like cameras and laptops. This and also for reasons to save power in general, minimizing power consumption is a major design challenge in pipeline ADCs considering their ubiquitous nature.

1.2 Motivation

Growing mobility of electronic equipment requires longer battery life. A typical communication channel on the receiver side is shown in Fig. 1.1. ADC is an essential block in such systems and often the most power hungry. Process scaling has marginally helped power scaling in analog blocks. In fact, it has been argued that scaling might increase the power [1]. Performance of pipeline ADC which is

popularly implemented using switched capacitor circuits is limited by thermal noise (kT/C noise in specific) which doesn't change with process scaling and opamp gain which becomes worse. Opamp, which is the essential building block of a pipeline ADC becomes tougher to design efficiently as process scales. So catching up with the power scaling of digital blocks require architecture level changes in ADCs and there are two ways of going by it.

a) Instead of trying to design a high gain opamp, the ADC is implemented using a low gain opamp and is calibrated either in analog or digital domain.

b) A high gain opamp is realized but the use of it is minimized or the number of such opamps is minimized with some architectural changes thereby reducing power.

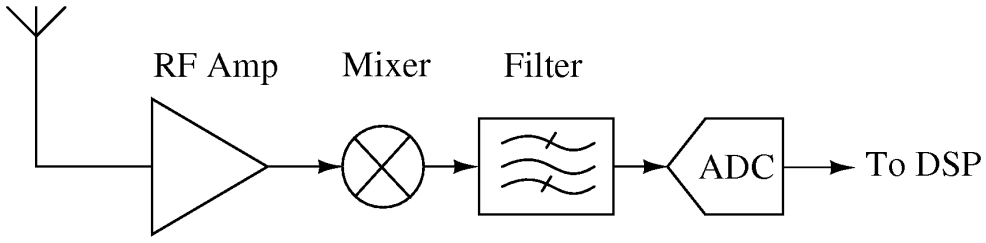


Figure 1.1: A communication receive channel

Theoretically both the techniques described above are power efficient but practical implementations to date incline the bar towards the latter because of its ease of implementation and efficiency. This thesis focuses on the latter.

In addition to the above mentioned techniques, recent ADCs have been implemented without the front end sample and hold (SAH) block to reduce power. A typical SAH burns as much power as 30% of the overall ADC power. SAH, in addition to doing the holding operation also acts as a buffer between the signal source and the input of the converter during sampling phase. In the absence of this block, the kickback from the sampling capacitors can cause substantial per-

formance degradation at high speed operation. In this thesis, this issue also has been looked into to reduce power.

1.3 Existing Methods

Opamp sharing is a popular method in which an opamp is shared between two consecutive stages of a pipeline [2]. As it happens, alternate stages in a pipeline work during the same clock phase. So two consecutive stages always operate on opposite clock phases allowing the opamp to be shared between them. A variation of it is used in [3] where the compensation capacitor and the second stage of a 2-stage opamp of ADC's first stage are used as the input capacitor and opamp of the ADC's second stage thereby reducing the power. Though this technique looks similar to one of the proposed low power techniques in this thesis, it is important to note that this technique has some design constraints that cannot be easily dealt with. The compensation capacitor's size and the gain of second stage of the opamp may not be appropriate for the ADC's second stage.

In [4], a multi-bit per stage architecture is chosen, but the problem of decreased feedback factor is alleviated using Merged Capacitor Switching technique where the input capacitors are merged in pairs to double the feedback factor yet retaining the same functionality by digital decoding. In [5] a DNL improving commutated feedback capacitor switching (CFCS) technique is proposed. In a gain-of-2 stage, the capacitor that is used at the input and the one that is used for feedback are fixed during design. Contrary to that, the CFCS technique decides the input and feedback capacitors basing on the digital code from sub-ADC. This is shown to have decreased DNL substantially, which helps in a lower capacitor size being used in terms of matching, thereby reducing power. Similar work was done in [6] where the

capacitor mismatch is reduced using Passive Capacitor Error Averaging thereby facilitating use of a smaller capacitor. This technique has two amplification phases making it a three phase system. In the first amplification phase, the input and feedback capacitors are in their usual positions but only one capacitor of the next stage is charged to the opamp output. In the second amplification phase, the input and feedback capacitors are swapped allowing the output to settle again and this time the other capacitor from next stage is connected to the opamp output. This helps alleviating the capacitor mismatch problem.

The effect of not having a SAH has been traditionally overcome by going for a three phase system with the third phase being the reset phase. During this phase, the capacitors are reset before going for sampling thereby overcoming kickback issues. In [7], this problem is solved by using an extra set of oppositely pre-charged capacitors that are combined with the input capacitors to cause the reset operation by charge sharing.

1.4 Proposed Approaches

Four low power techniques have been proposed in this thesis as described below.

a) Capacitor and opamp sharing: The feedback capacitor of the first stage MDAC is used as the input branch for the second stage. This capacitor sharing helps getting rid of the dedicated load capacitors for the first stage MDAC thereby achieving threefold power saving. This technique also goes well with the existing opamp sharing technique.

b) Capacitor reset without extra overhead: The SAH block has been dropped to save power. But the performance degradation issue is overcome by a new reset technique that we have proposed. Both the techniques described before

to overcome the kickback problem have extra overhead in the form of decreased conversion speed or increased input capacitance. The technique we propose splits the input capacitors into two halves and combines the positive and negative halves which are existent in a differential implementation during sampling to cause charge sharing thereby resetting the capacitors.

c) MDAC with rail-to-rail input swing: Input signal swing to the converter can go rail to rail but often reduced range is taken in because of opamp linearity requirements. In [8, 9], full scale input is taken in but it is later compressed thereby getting only reduced benefits. We propose a technique in which the full scale swing is used to resolve a bit and then the bit information is used to compress the signal so that we save on an opamp. This opamp saved is the 'first stage' opamp thereby giving huge power benefit.

d) Asynchronous SAR(ASAR) backend: Recent research [10–12] has shown that high speed and low resolution ADCs can be efficiently implemented using asynchronous SAR architecture. Thus, a scheme has been proposed where the first few MSBs are resolved using a pipeline ADC and the backend is replaced with an ASAR. In addition to giving tremendous power advantage, this architecture also gives huge area reduction because the backend opamps and capacitors are now replaced with mostly digital blocks of ASAR.

1.5 Thesis Organization

The thesis is organized as follows. The basic operation and design techniques of pipelined ADCs are described in Chapter 2. Some of the existing low power design techniques are discussed in Chapter 3. Two of the proposed techniques capacitor and opamp sharing & capacitor reset without extra overhead are used to design

an ADC and are described in Chapter 4. In Chapter 5, the other two techniques: MDAC with rail to rail input swing & asynchronous SAR backend are described. The two techniques used to design a ADC and its design and simulation results are also presented. The conclusions and a summary of research are given in Chapter 6.

Chapter 2 . REVIEW OF PIPELINED ADC

Before describing the pipelined ADC architecture, it is good to know how it arose from the 'line of thought' flash ADC architecture.

2.1 ADC architectures

2.1.1 Flash ADC

Fig. 2.1 shows a regular 3-bit flash ADC. It has $2^3 - 1$ comparators with each getting a reference voltage. Input is applied to all the comparators at the same time and those comparators with reference below the applied input would trip to 1 whereas others would continue to hold out 0. The output is a string of 1's followed by 0's if seen from the bottom and is often called 'thermometer code' indicating the resemblance to the common thermometer. This string of 1's and 0's is converted to binary code using an encoder. Flash works best for high speed and low resolution applications. Main disadvantage associated with flash is its power and area increase w.r.t resolution. For every extra bit that is intended to be resolved, power and area double thereby making it cumbersome to deal with for resolutions beyond 8 bits. Apart from that, another issue with flash is the comparator offset.

Methods to cancel or reduce this offset [13, 14] have become standard practices and continue to be explored even today [15] but it becomes a power hungry solution beyond 8-bits because of the increased number of comparators. To overcome the

issues associated with flash, two architectures have been derived from it: Sub-ranging and 2-step.

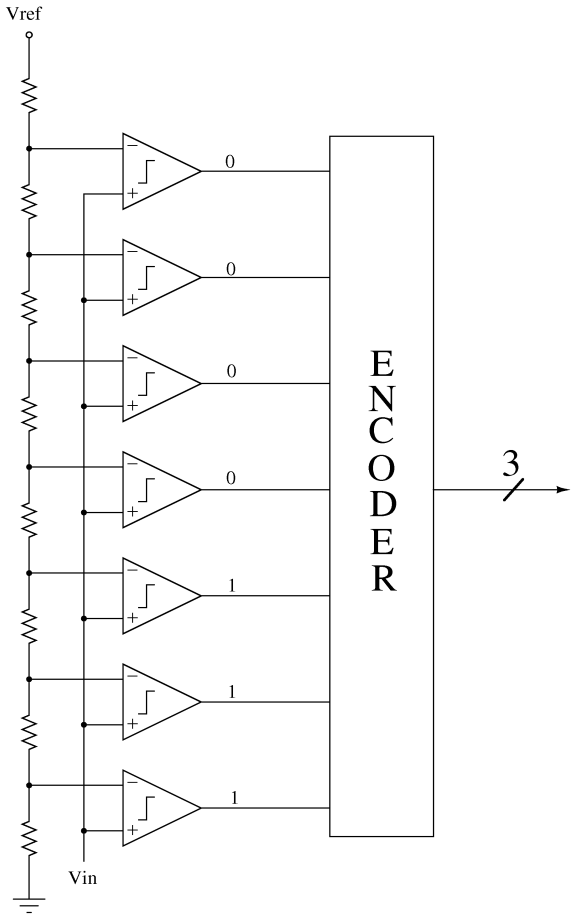


Figure 2.1: A 3-bit flash ADC

2.1.2 Sub-ranging ADC

A 4-bit sub-ranging ADC is shown above. It operates in two steps with the same input being applied to both the stages. The first stage is the coarse stage and the later the fine stage. In $\phi 1$, the coarse stage resolves two MSBs. Knowing the range in which the signal is, that particular reference now becomes the input to the resistor ladder of fine stage.

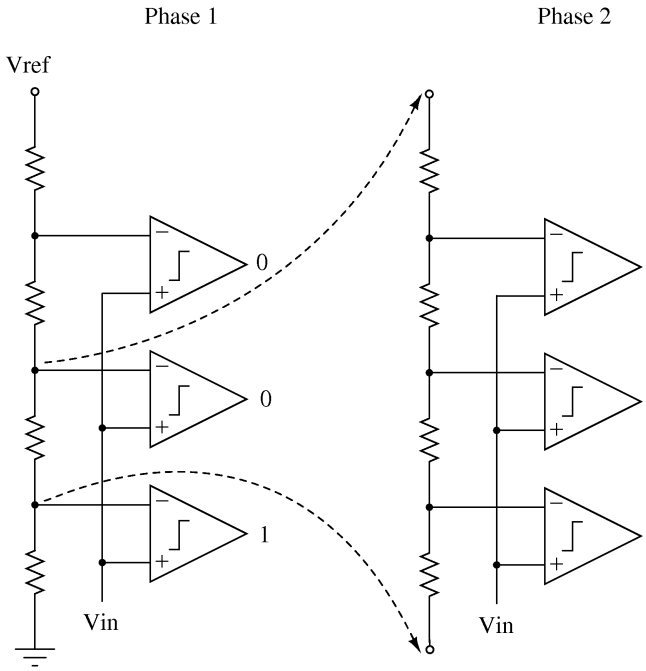


Figure 2.2: A 4-bit sub-ranging ADC

An example is shown in Fig. 2.2. Fine stage now resolves the two LSBs hence completing the 4-bit resolution. As can be seen, the immediate advantage is the gain in area and power overhead. An N bit flash ADC requires $2^N - 1$ comparators where as when implemented in sub-ranging architecture, the ADC requires $2\times(2^{N/2} - 1)$ comparators. The offset issue is downsized to a certain extent here. The comparators in coarse ADC need to be only N/2 bit accurate whereas the fine stage comparators have to be N-bit accurate. This helps in saving power by implementing complex offset cancellation schemes only in the fine stage. But the fact that a N-bit accurate comparator is still required is a problem here. Another issue with sub-ranging ADC is the reference settling of the second stage. The reference range of the fine stage keeps changing every sample basing on the coarse ADC output. This is a speed limiting operation and can become the bottleneck in terms of achievable resolution.

2.1.3 2 step ADC

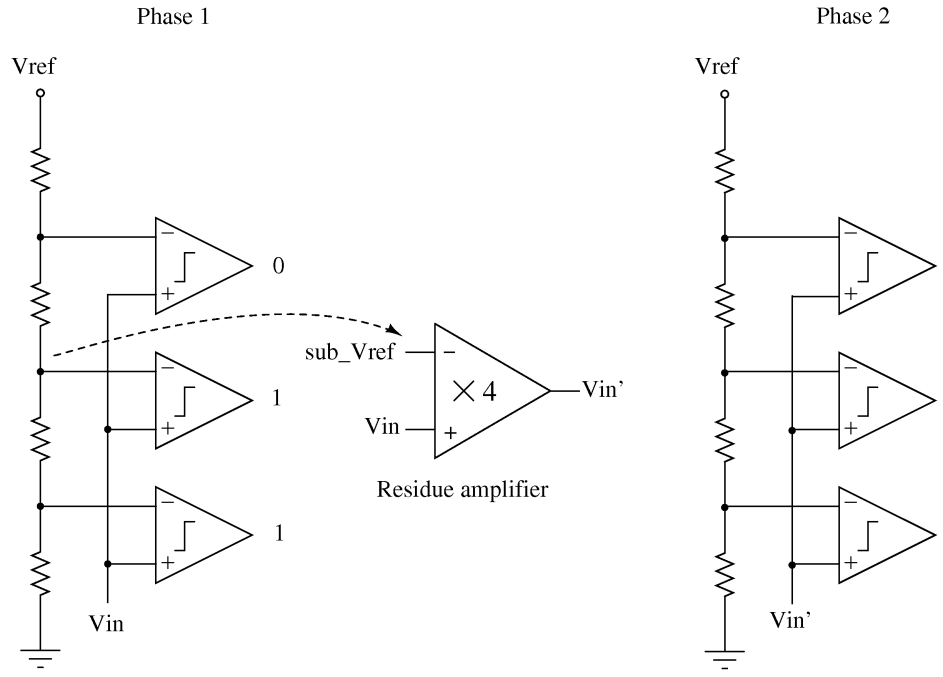


Figure 2.3: A 4-bit 2-step ADC

A 4-bit 2-step ADC shown in Fig. 2.3 has all the advantages of a sub-ranging ADC and solves the comparator offset issue and the reference settling issue completely. Same as in sub-ranging case, the first stage resolves two MSBs. Now, an amplifier amplifies the residue which is the difference between the input and the nearest reference that is lower than the input by a factor of 4 (In the case of a N-bit ADC, assuming the first stage resolves N/2 bits, the amplification factor is $2^{N/2}$). This amplified residue is applied as input to the second stage which has the same reference levels as the first stage. The second stage now resolves the two LSBs thereby completing 4-bit resolution.

The limiting block in a 2-step ADC is the residue amplifier(RA) which is often implemented using switched capacitor circuits as shown in Fig. 2.4. During sampling phase, the input is sampled onto $2^{N/2}$ unit capacitors of size C each . During

amplification phase, all the sampled charge is transferred into one capacitor of size C using an opamp thus achieving the amplification factor required. The reference is also subtracted in the process to form the residue. A gain of $2^{N/2}$ means a feedback factor of $1/2^{N/2}$. In higher gate length processes (>0.5μm) achieving such gain was possible for N in the range of 12. But as process scaled, meeting such high gain and bandwidth requirements has become a tough design challenge if at all possible. Also, the $2^{N/2}$ unit capacitors used in RA have to match to N-bit level which is difficult to achieve with all the process variations possible on die. This matching is as important as the opamp gain and will determine the final resolution achievable.

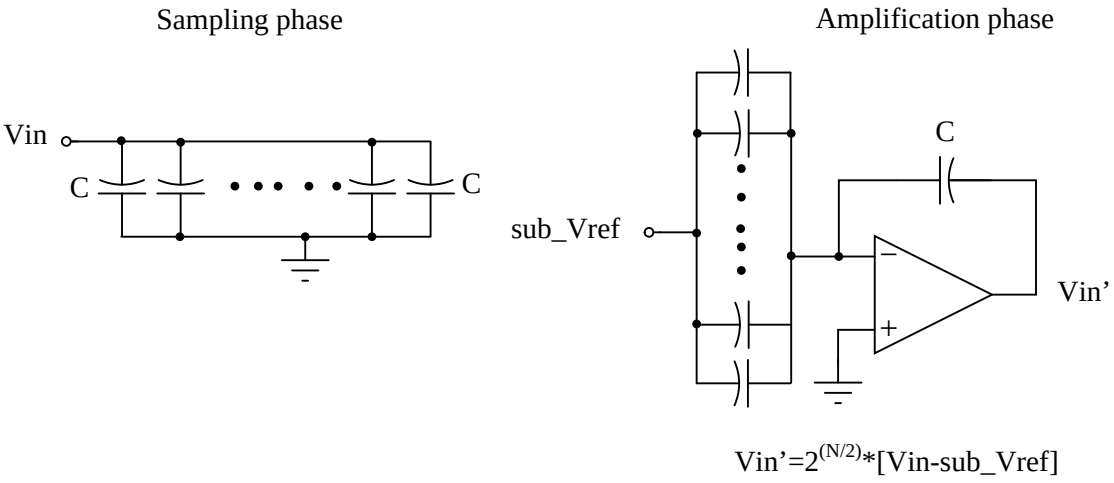


Figure 2.4: A N-bit residue amplifier

2.1.4 Pipeline ADC

A workaround for the two issues discussed above is the N-step ADC shown in Fig. 2.5 which by virtue of the inherent pipelining existent is called the pipelined ADC. Here, each stage resolves one bit as shown. The first stage comparator compares the input to Vref/2 and the RA amplifies the residue by a factor of 2.

This amplified residue is held as next stage's input. The residue curve after first stage looks as show in Fig. 2.6. Like wise, each stage's RA holds the input for the next stage. At the end of N clock cycles, the output digital code is available giving the ADC N cycle latency. This latency is not an issue in many applications and is acceptable. Because of the holding operation available in the RA, each stage can process a different sample as there is no need to wait till a particular sample has been processed by all the stages. This means that the sampling clock rate is the conversion rate of the ADC.

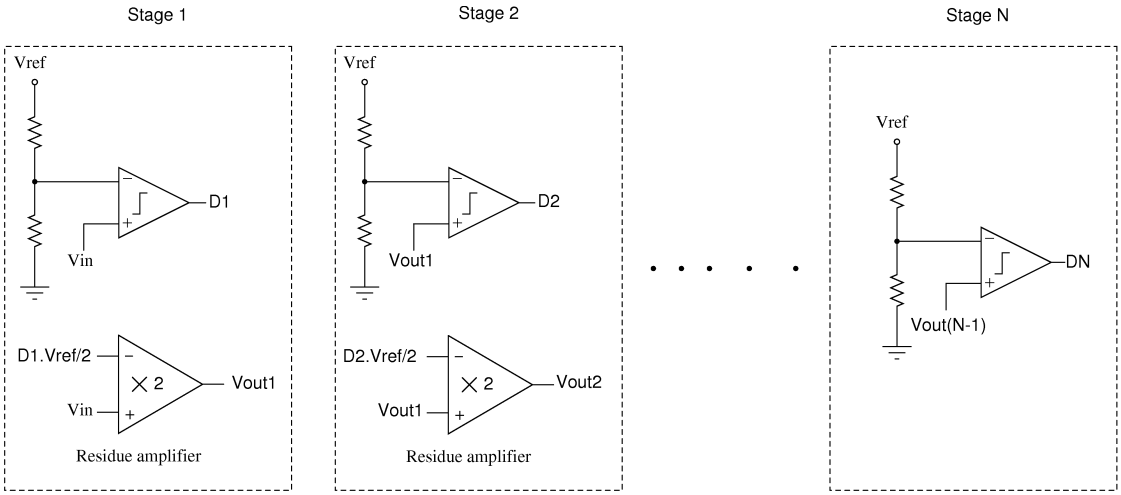


Figure 2.5: A N-step ADC

As it can be observed, the gain of the RA now is 2 which means that the feedback factor is 1/2: a great deal of improvement from the 2-step ADC case. Though the capacitor accuracy requirement is still the same, the number of capacitors that have to be matched now is two, which is much easier to implement. These two advantages of the pipelined ADC help in achieving high speed operation along with high resolution.

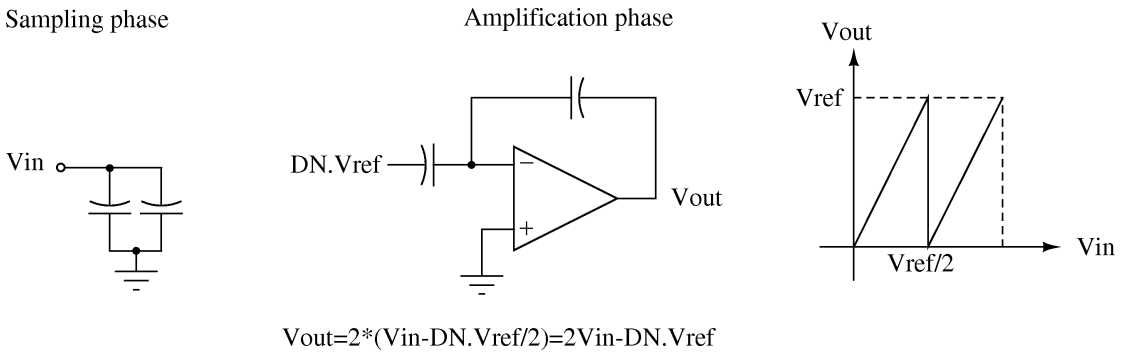


Figure 2.6: A gain of 2 residue amplifier used in a N-step ADC followed by its transfer curve

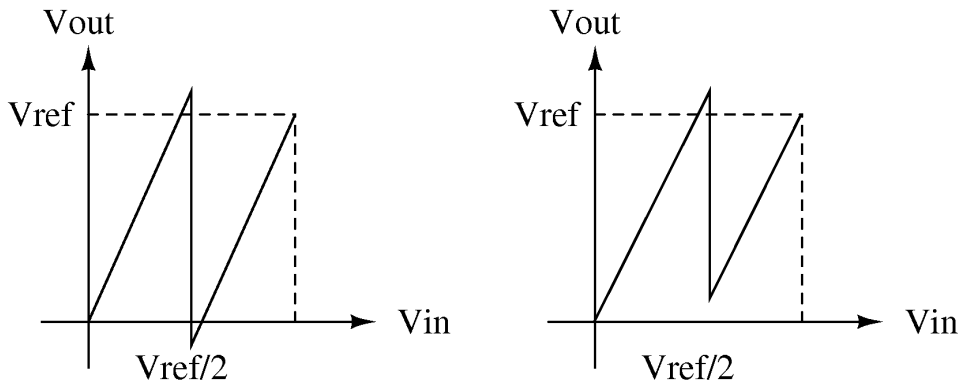


Figure 2.7: (a): Transfer curve due to opamp gain error or capacitor mismatch (b): Due to comparator offset

Some of the problems associated with a 1-bit per stage pipelined ADC are finite opamp gain, capacitor mismatch and comparator offset. The first two are generic issues and their effect on the residue transfer curve is shown in Fig. 2.7(a). A more important problem is the comparator offset. Fig. 2.7(b) shows the altered residue curve with comparator offset. In both the cases the RA output exceeds the allowable signal range causing missing codes that lead to distortion. A solution is to reduce the inter stage gain to keep the output well within range. This approach can be implemented at the cost of increased digital complexity. In most situations the problems due to opamp and capacitor can be overcome by choosing appropriate values of gain and size basing on the resolution required. On the other hand

comparator offset has to be completely canceled to avoid missing codes. The cancellation schemes can become quite complex leading to huge power consumption.

2.2 1.5-bit per stage architecture

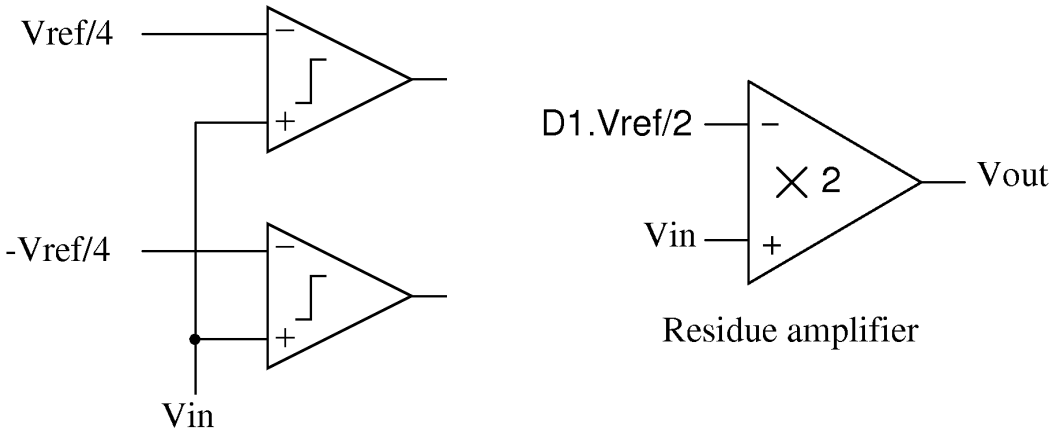


Figure 2.8: A 1.5-bit per stage architecture

A workaround for this is to introduce redundancy that can tolerate comparator offset as suggested in [16]. The 1-bit per stage now becomes 1.5-bit per stage and looks as shown in Fig. 2.8. For convenience the DC level of the signal has been shifted to 0. This doesn't change any of the discussion so far. The sub-ADC stage now consists of two comparators instead of one. The reference levels of the comparators are optimally placed at +Vref/4 and -Vref/4. Each stage gives a 2-bit output D coded as 00, 01, 10 depicting the 3-level ADC formed by two comparators. The residue is given by the following equations and is plotted in Fig. 2.9.

$$\begin{aligned} Vres &= 2Vin + Vref; \quad if \quad D = 00 \\ &= 2Vin; \quad if \quad D = 01 \\ &= 2Vin - Vref; \quad if \quad D = 10 \end{aligned} \tag{2.1}$$

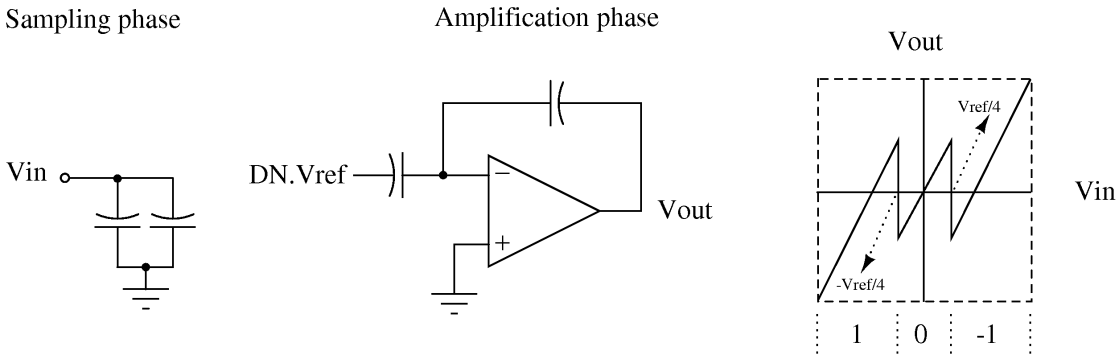


Figure 2.9: A 1.5-bit per stage residue amplifier followed by its transfer curve

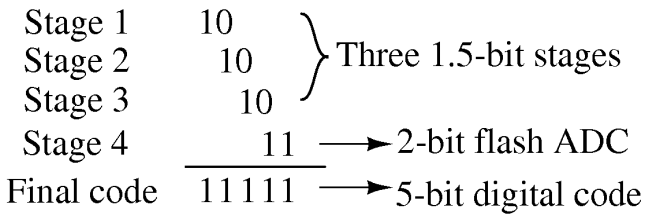


Figure 2.10: Digital correction operation

Though each stage gives a 2-bit output, the final ADC code is still N bits wide. This 'digital correction' operation which is just shifting and adding happens as shown in Fig. 2.10. An N-bit ADC is usually implemented using (N-2) 1.5-bit stages followed by a 2-bit flash ADC. The example shows a 5-bit pipeline ADC in which each stage gives its maximum code. It should be noticed that a 1.5-bit stage has a 3-level ADC where as the last stage is a regular 2-bit flash which is a four level ADC.

By virtue of the extra bit coming out, each stage has a redundancy of Vref/4 built in for the comparator offset. This is illustrated with an example. Let us consider a 5-bit pipelined ADC implemented using 1.5-bit per stage architecture. If the input is 5Vref/14, the digital codes and residue of each stage look as shown in Fig. 2.11. Now if the comparator at +Vref/4 in the first stage has an offset of Vref/4, the comparison level moves to +Vref/2. This changes the digital code of the first stage as seen in Fig. 2.12. But this error is corrected by the second stage as shown in the example and the final output code is the same as the ideal situation. Thus a comparator offset of Vref/4 is completely absorbed by the ADC. The error caused in first stage due to comparator offset has been corrected by the second stage and the final output retained. Likewise error in a particular stage is corrected by the stages following it. This error correction mechanism has made the 1.5-bit per stage a popular architecture for the implementation of pipelined ADCs. For a more detailed explanation of 1.5-bit per stage, please refer to [16].

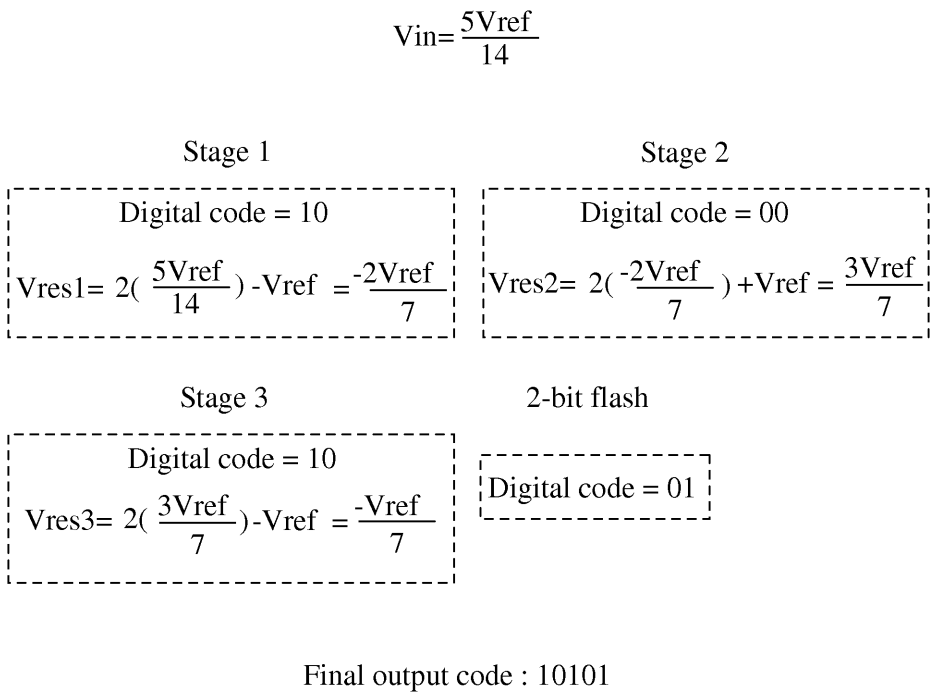


Figure 2.11: Digital code and residue of each stage of an ideal 5-bit ADC

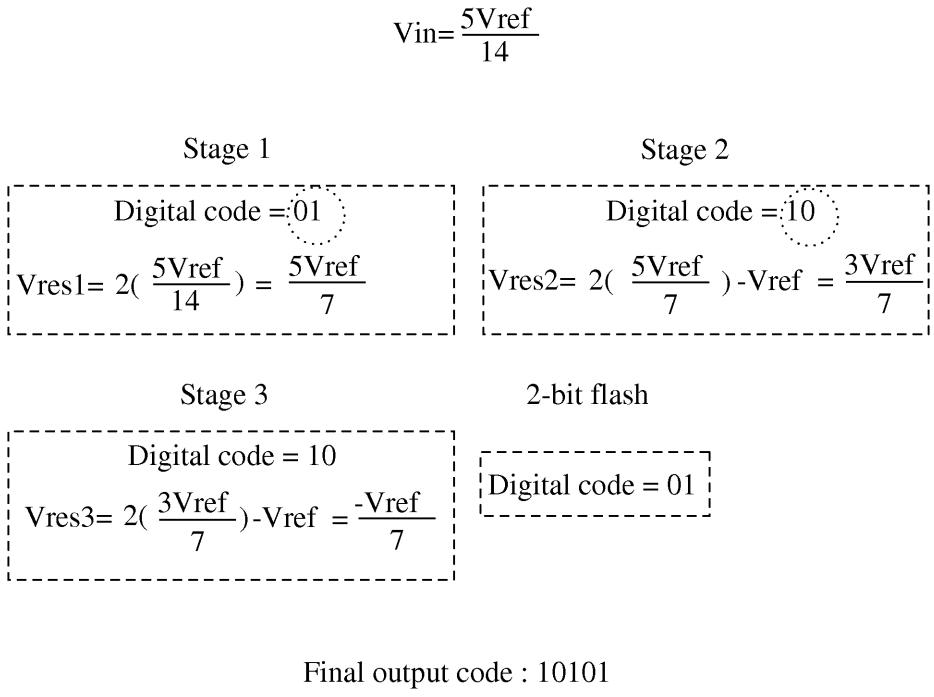
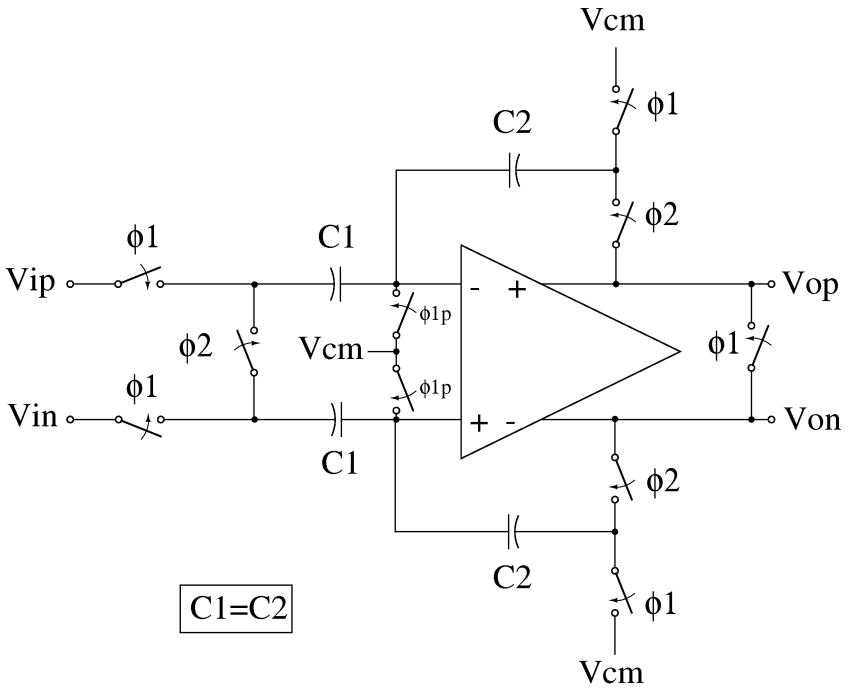


Figure 2.12: Digital code and residue of each stage of a 5-bit ADC in the presence of offset on the first stage comparator

2.3 Building Blocks

2.3.1 Sample and Hold



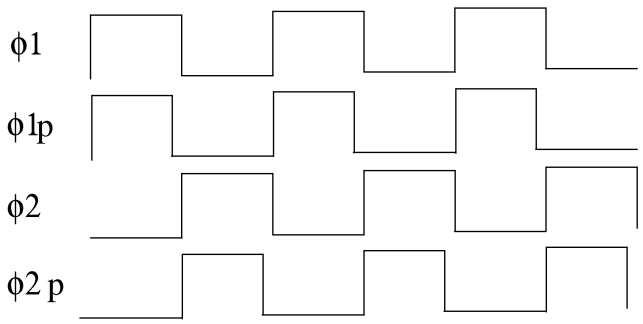


Figure 2.13: A charge redistribution sample and hold

The input is sampled and held by the SAH for processing by sub-ADC and the RA. One of the common implementations of SAH called the charge redistribution architecture is shown in Fig. 2.13. During $\phi 1$ input is sampled onto the C1 set of capacitors. The C2 capacitors are reset during this time. During $\phi 2$ the charge

on C1 is transferred onto the C2 capacitors. As C1=C2, the output voltage of the SAH is the same as the sampled input value. In the following $\phi 1$ when C1 goes for sampling they don't have any charge on them as all of it has been transferred to C2 in the previous phase. This is an advantage with this structure as it prevents any kickback during sampling. As mentioned before, SAH is a power hungry block as it has to meet the noise and linearity requirements of the entire ADC. Careful observation of Fig. 2.13 shows that the mentioned SAH can be modified and be included in first stage MDAC as shown in Fig. 2.14 thus avoiding a dedicated SAH. During $\phi 1$ the input is sampled onto both the capacitors that are nominally equal

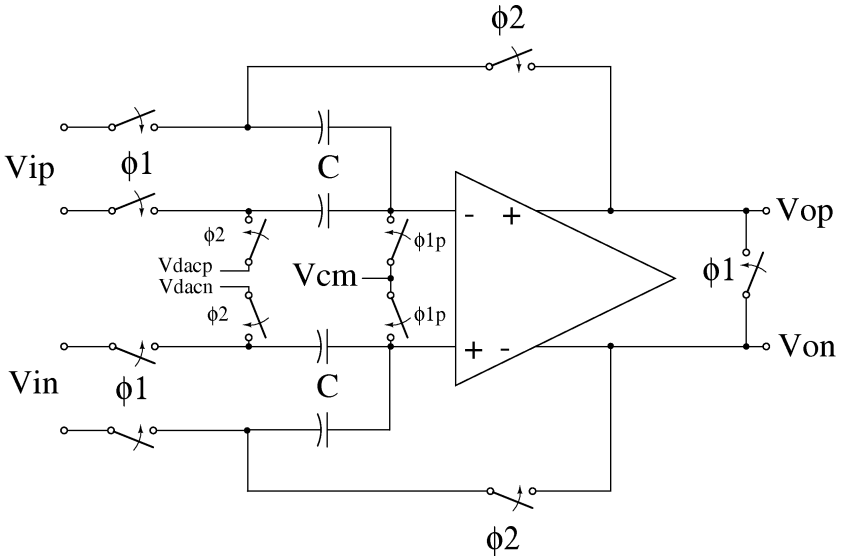


Figure 2.14: A 1.5-bit MDAC stage

to C. During $\phi 2$, one of them is flipped over and connected between the output and virtual ground node of the opamp. The other capacitor is connected between the appropriate reference value Vdacp or Vdacn and the virtual ground node of the opamp. At the end of $\phi 2$ all the charge on the input capacitor gets transferred to the feedback capacitor like in a regular SAH. As the feedback capacitor already has input sampled onto it, the new charge that is being transferred gets added

to it thereby making the output voltage twice the sampled input value. At the same time the reference gets added or subtracted from the input capacitor as it is now connected to the reference voltage. The output is given by the Eqn.2.1 thus completing the MDAC. This approach has become popular recently to save power and the recent ADCs that have been published show this trend [17]. Commercially available ADCs are still to embrace this change though. Many of them still have a dedicated SAH that acts as a buffer between the input signal and the converter. Another common implementation of the SAH called the flip over architecture is

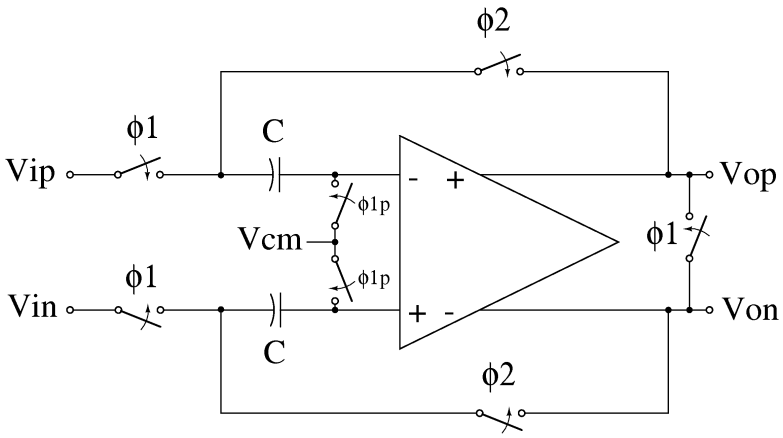


Figure 2.15: A flip around sample and hold

shown in Fig. 2.15. Here there is only one set of capacitors. The input is sampled onto them during $\phi 1$ and during $\phi 2$ they are flipped and connected between the output and virtual ground nodes of the opamp. As there is no charge transfer occurring during $\phi 2$, this SAH can be operated at very high speed. A disadvantage with this structure is the charge kickback during sampling phase. The capacitors have the previous sampled value on them when they go for sampling. It means that the time required to sample a new value onto the capacitors is more than what it would be if they had no charge on them. At high speed operation this could cause improper sampling thereby leading to distortion.

Two disadvantages of not having a dedicated SAH are:

a) Timing mismatch between the comparator sampling path and the RA sampling path

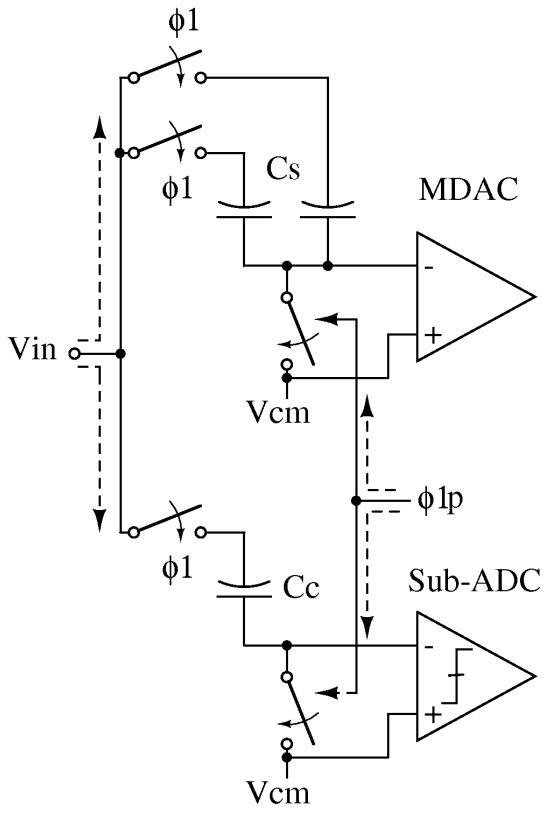


Figure 2.16: Illustration of different sampling paths

In the presence of a SAH, the input to the sub-ADC and the RA will be the output of SAH thus ensuring that both the blocks process the same value. In the absence of a SAH, the sampling paths are different as shown in Fig. 2.16. Mismatch either in the input signal paths or the sampling clock paths lead to different sampled values which has the same affect as comparator offset which means that it eats into the real comparator offset margin. Apart from maintaining same physical path lengths in layout, the RC time constant of the networks should also be matched to ensure proper functionality in the absence of a SAH.

b) Kickback during sampling operation

The sampling capacitors in a dedicated SAH shown in Fig. 2.13 have no charge on them before going for sampling. In the absence of a SAH, the capacitors shown in Fig. 2.14 have some residual charge on them when they go for sampling which is different from cycle to cycle. During sampling, it becomes the burden of the input signal source to discharge this residual charge and then put a new voltage on the capacitors. At low speed operation this sampling operation is not an issue. But at high speeds, there is not enough time to discharge and then put a new charge accurately on the capacitors. This inaccurate sampling operation leads to distortion thus leading to reduced performance of the ADC. A workaround has been proposed for this problem in [7, 18].

2.3.2 Multiplying Analog to Digital Converter (MDAC)

MDAC is the most critical block in a pipelined ADC. A commonly used 1.5-bit per stage MDAC is shown in Fig. 2.17. During $\phi 1$ the sampling phase, the input is sampled on both the capacitors C1 and C2. This sampling, popularly called the 'bottom plate sampling' is done on the bottom plates to nullify the effect of parasitic capacitors. During the same phase, the sub-ADC also keeps track of the input and the comparators are triggered at the falling edge of $\phi 1$ when sampling of C1 and C2 ends. The non-overlap time between $\phi 1$ and $\phi 2$ is used by the sub-ADC to resolve the bits and by the beginning of $\phi 2$, the output digital code which is the DAC control signal is available. In $\phi 2$ the amplification phase, C2 is flipped over with its bottom plate going to the output of the opamp. The top plate of C1 is connected to the virtual ground node and the bottom plate is connected to the reference voltage $\pm$Vref or 0 basing on the DAC control signal from sub-ADC. At

the end of $\phi 2$, the output voltage Vo of the opamp is given by Eqn. 2.2. In the case of a 1.5-bit per stage architecture as the desired gain is 2, C1 and C2 are chosen to be equal.

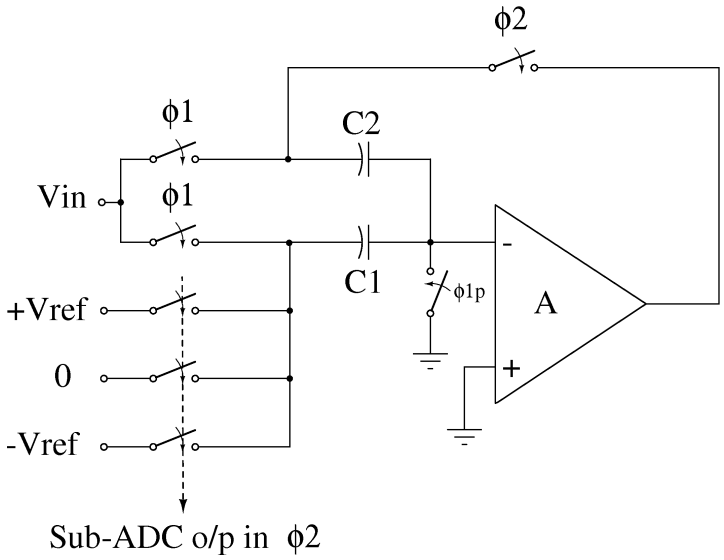


Figure 2.17: A 1.5-bit per stage MDAC

$$Vo = \frac{C1 + C2}{C1} Vin \pm \frac{C1}{C2} Vref \tag{2.2}$$

The attainable resolution of the ADC is determined by the accuracy of the MDAC stage. Also as this the most power hungry block in the ADC, most of the concentration to improve performance is on this block. As seen in Fig. 2.17, opamp being the only active circuit in a MDAC is of main interest.

Most MDACs are implemented using switched capacitor circuits and hence the opamp can truly be an OTA (operational transconductance amplifier) with high output impedance. Some of the popular OTA structures are shown in Figs. 2.18 & 2.19. For resolution of interest ($\geq$10 bits), the OTA loop gain has to be greater than 60 dB. To account for process variations this is usually chosen to be greater than 70 dB. Such high gain dictates the use of cascode and cascade structures. The

Structure	Advantages	Disadvantages
Telescopic cascode	High speed Low Power	Reduced signal swing
Folded cascode	Reasonable signal swing High input common mode range	Reduced speed Not power efficient
Two stage	High signal swing Suitable for low voltage application	Slow Power hungry

Table 2.1: Comparison of opamp architectures

three popular OTAs are compared in the Table 2.1. High gain and bandwidth are the important requirements of the OTA. It has been observed that in 0.18μm process, the gm.ro product is roughly equal to 25 dB. In 90nm, the same drops to 20 dB. This indicates that the regular cascode structures of telescopic or folded cascode are not enough to get the required gain.

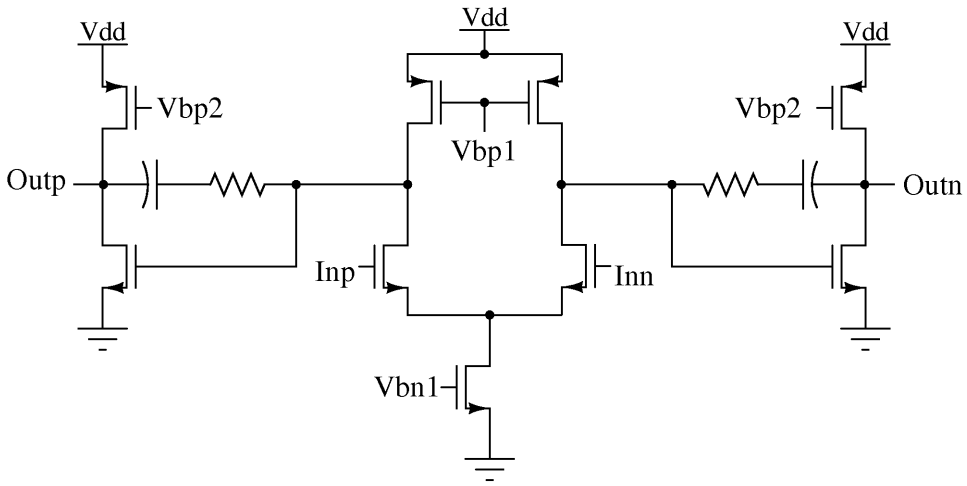


Figure 2.18: A two stage opamp

To meet the gain specifications, the basic cascode amplifiers are either cascaded like in a two stage opamp or gain boosted. The first approach involves Miller compensation which requires a lot of power being wasted in maintaining the stability in addition to losing speed. It has the benefit of higher signal swing though which makes it popular in low voltage structures. The second approach of gain boosting

shown in Fig. 2.20 is much more efficient and is becoming the choice of designers these days. The gain boosting amplifier can be a nested structure as shown in [6] with stability the only limiting criteria thus boosting the gain immensely. Stability in this case is much easier to deal with and can be maintained reliably with little design effort. A detailed treatise on gain boosting amplifiers is found in [19].

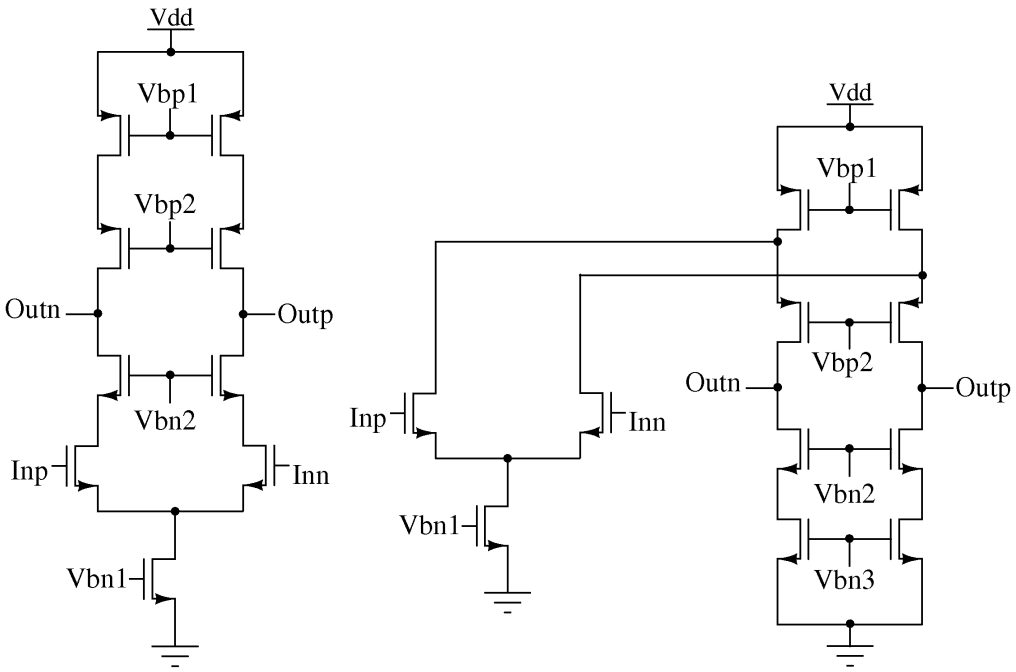


Figure 2.19: Telescopic and folded cascode opamps

The regular MDAC implementations are differential to have good PSRR and CMRR. This necessitates a common mode feedback (CMFB) loop to maintain the output common mode voltage at the desired level. Of the many existing structures, the switched capacitor implementation shown in Fig. 2.20 is popularly used in MDACs. The clocks $\phi 1$ and $\phi 2$ are same as the MDAC clocks. One of the two main advantages of this structure is its passive nature that doesn't need any extra power. The other advantage is its capability to handle high signal swing which is a major limiting factor in other structures. The latter makes it preferred

as often the signal swing of the OTA can be limited by the CMFB loop's inability to handle high swing.

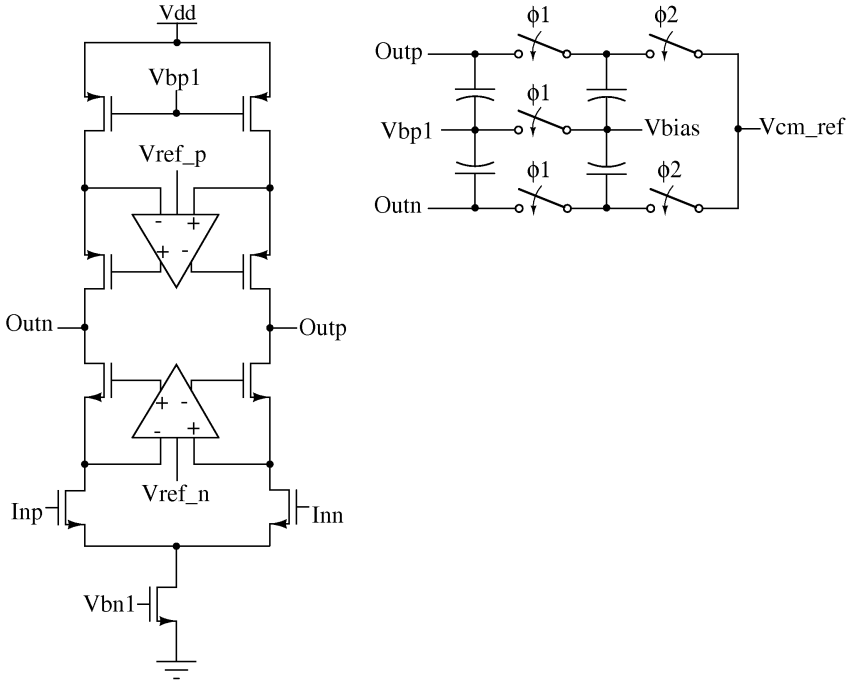


Figure 2.20: A gain boosted telescopic cascode opamp with switched capacitor common mode feedback loop

2.3.3 Sub-ADC

Sub-adc is the next important block in a pipelined ADC. Though the design of this block is relatively simpler, there are some important constraints that have to be taken care of for the proper functioning of the ADC. The important block in a sub-ADC is the comparator. A common implementation of it is shown in Fig. 2.21 where the inputs are coupled via capacitors. In $\phi 2$, reference voltages (Vrefp = Vref/4) and (Vrefn = -Vref/4) are sampled onto the capacitors. In $\phi 1$, while one end of the capacitors is connected to the input signal, the other end is connected to the input of the comparator. The effective differential voltage seen

at the comparator inputs is given by the Eqn. 2.3.

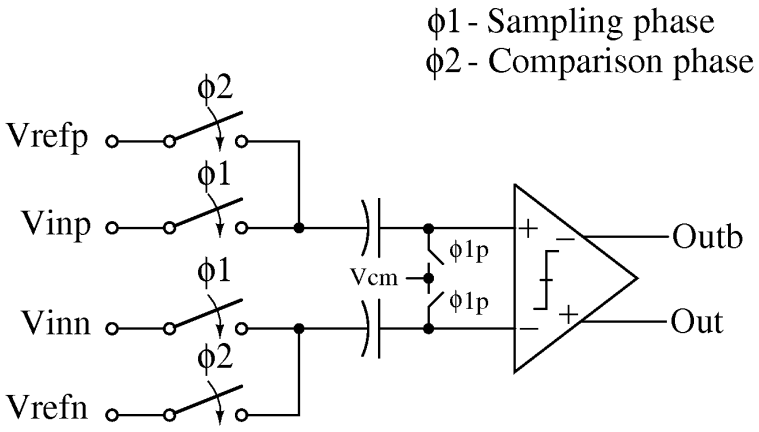


Figure 2.21: Block diagram of a comparator with capacitively coupled inputs

$$V_{in,diff} = (Vinp - Vinn) - (Vrefp - Vrefn) \tag{2.3}$$

The comparator is clocked at the falling edge of $\phi 1$ and is expected to latch a decision by beginning of $\phi 2$ giving it the non-overlap time to resolve. Sometimes to be on the safe side, the comparator is clocked using an advanced phase to give it more time to resolve. To achieve this high speed operation, cross coupled latches such as that shown in Fig 2.22 are popularly used.

Though the offset tolerance of a 1.5-bit stage obviates the need for a preamp, kickback issues sometimes necessitate it. Care has to be taken to ensure that the kickback coming from latch doesn't propagate to the sampling capacitors of the MDAC. This is done at design level by not using the same clock edge to sample the MDAC capacitors and to latch the comparator. Often, one of them is a delayed version of the other so that the kickback effects from comparator either subside or are not seen. In addition to this intentional clock skewing, a preamp is employed before the latch to act as a buffer between the signal and the latch. Though a low power block (∼25uA), it is still avoided because the number of preamps

used is large. A 10-bit converter uses roughly 20 comparators making the power consumption 500uA. This is a substantial current in some low power ADCs being reported today like [20].

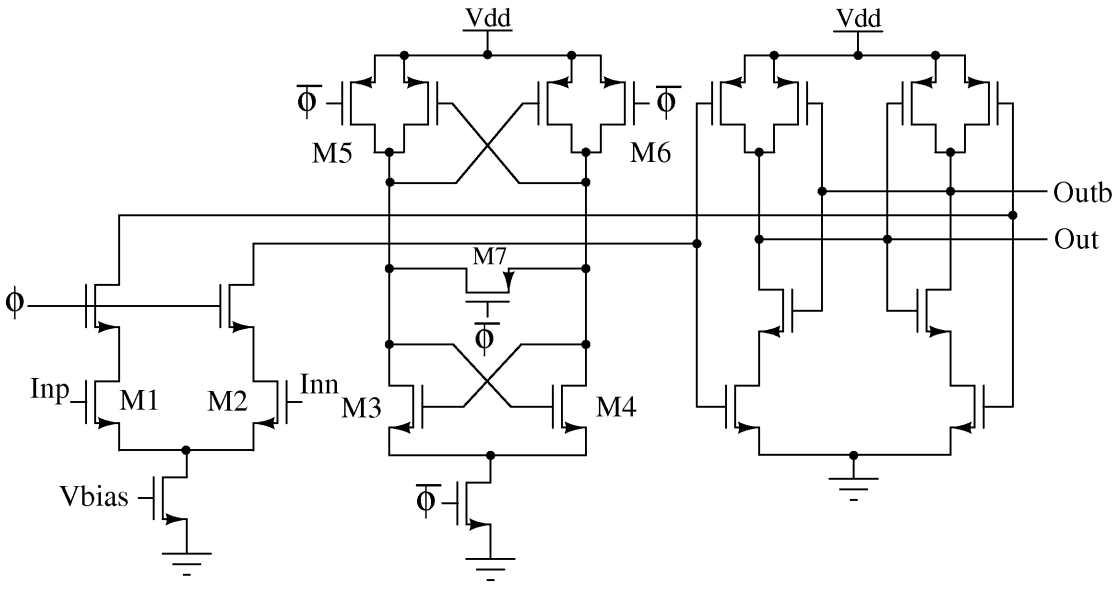


Figure 2.22: A cross coupled latch followed by a SR latch

Apart from the commonly used comparator structure discussed above, there are other structures like those shown in Figs. 2.23 & 2.24 each with its own advantages. The one in Fig. 2.23 doesn't need a separate set of references for the comparator [21]. The required voltages of ±Vref/4 are derived from the DAC references ±Vref. This saves power by avoiding the reference buffers needed to produce them. Comparator shown in Fig. 2.24 almost nullifies the load seen by references. This helps in Vrefp and Vrefn being reliably produced and used from a resistor ladder using ±Vref thereby saving power.

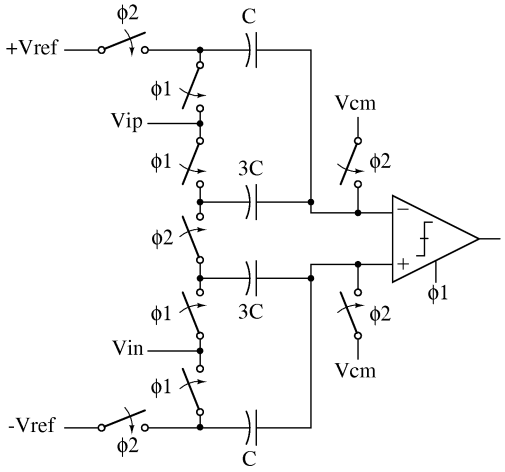


Figure 2.23: Comparator that uses the DAC references to generate the required thresholds

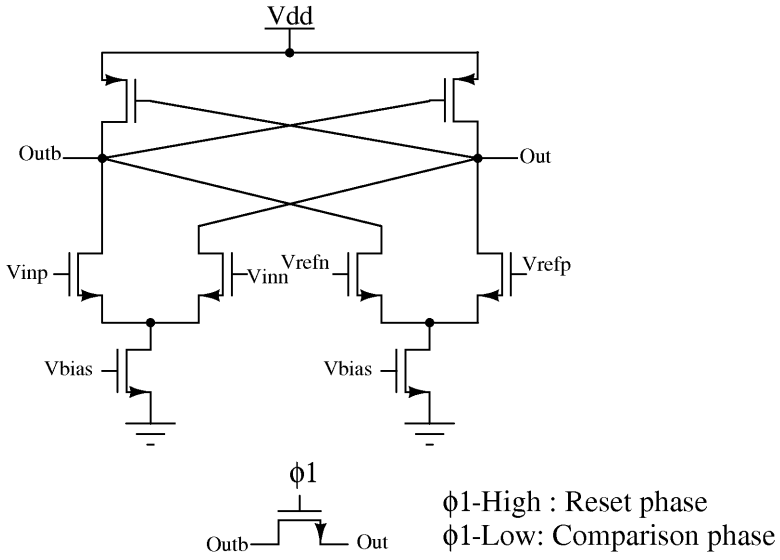


Figure 2.24: Latch that doesn't draw any current from references

2.3.4 Clock Generator

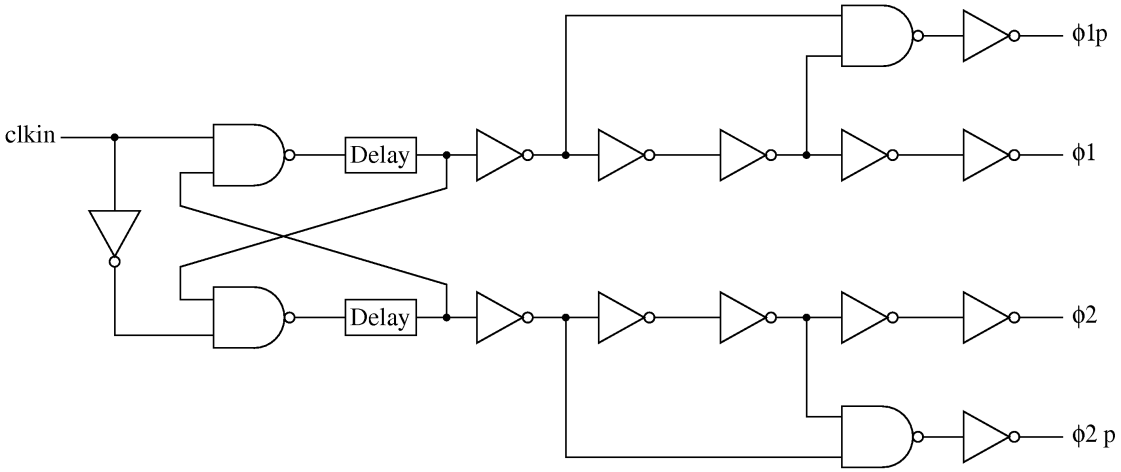


Figure 2.25: Commonly used clock generator to produce non-overlapping phases

This block takes in an external clock and generates all the required clock phases by the ADC. A commonly used clock generator is shown in Fig. 2.25. The non-overlap time desired is set as the delay of the 'delay' block. The design of clock generator might be tricky if not tough. Usually there is a central clock generator that produces all the required clock phases. At times this number of phases can exceed 10. From the generator to the actual load, the clocks go through a series of buffers to gain strength. A buffer chain is shown in Fig. 2.26. The scaling ratio between buffers is usually e ($\sim$2.7) to ensure optimal design. Simulation results show that the jitter induced by the clock generator or the buffers is negligible at least till 14-bit level. The allowable clock jitter is given by Eqn. 2.4.

$$\sigma_{RMS} = \frac{1}{2\pi f_{in} SNR_{ADC}} \tag{2.4}$$

The tricky part comes into picture when relative timing has to be maintained. The load seen by each clock phase is different. If the same buffer chain is used

for all phases, then the final rise and fall times can be substantially different, thus leading to undesired effects. This is dominantly seen in higher gate length processes such as 0.18μm where the intrinsic capacitance of the buffer can become substantially large with the buffer size. In processes such as 90nm, the buffers can be very powerful so as to give roughly the same rise and fall time irrespective of the load. While designing in deep submicron processes, care should also be taken to ensure that the connecting line parasitics don't influence the performance much as they can become comparable to the gate capacitance. Accounting for parasitic capacitors during design is very advisable for clock generator.

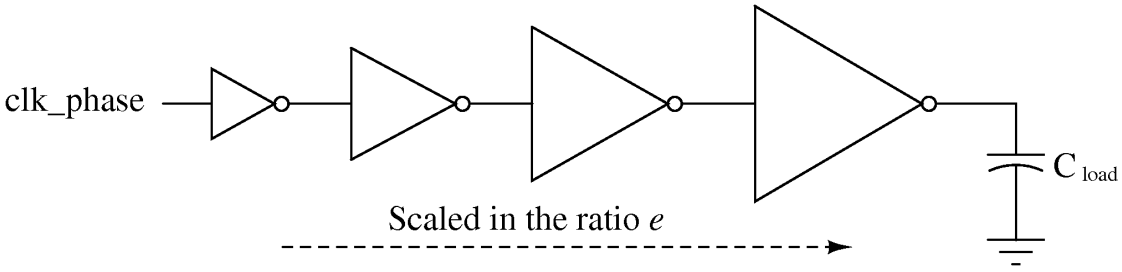


Figure 2.26: Clock buffer

2.3.5 Reference Buffer

Reference buffer generates the DAC reference voltages ±Vref. As with respect to other blocks like SAH and MDAC, this block is equally important and can determine the resolution achievable. Though a commercially available ADC will have this on chip along with the ADC core, research targeted at ADC core wouldn't necessarily have it on chip. Instead, the references are supplied externally for test purposes.

Ideally the references should settle to the same value every cycle. Implementation of this is done using two approaches: fast and slow. A fast buffer is shown

on the left in Fig. 2.27. The only load that this buffer drives is the ADC load. As the name suggests, this buffer is designed to operate at high speed so that it settles to the ideal reference value every cycle irrespective of the load seen. Thus it becomes a power hungry block as its settling behavior and noise have to be better than that of the ADC. An efficient implementation of this buffer is done using a class AB output stage.

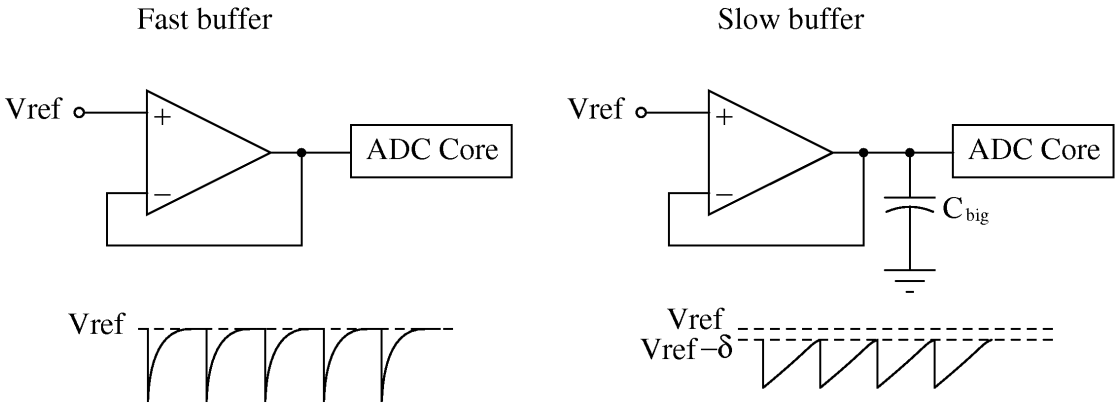


Figure 2.27: Fast and slow buffers along with their settling behavior

A slow buffer is shown on the right in Fig. 2.27. The main difference between this and a fast buffer is the bypass capacitor at the output. As the name suggests, this buffer is loaded with as much capacitance as possible to ensure that the output node doesn't move. In reality, the node does move but it is ensured that it settles to the same value every cycle. This may not be the ideal reference value desired as shown in the figure. The opamp practically sets the DC operating point of the node. All the desired charge comes from the capacitor. This huge capacitance filters out the noise from the opamp and hence is much easier to design.

The important trade off between the two approaches described above is the area. A fast buffer would occupy lot less area than a slow buffer because of the absence of any bypass capacitor but is a lot power consuming. This makes it dear

to many commercially available products where extra silicon die area is available only at a premium.

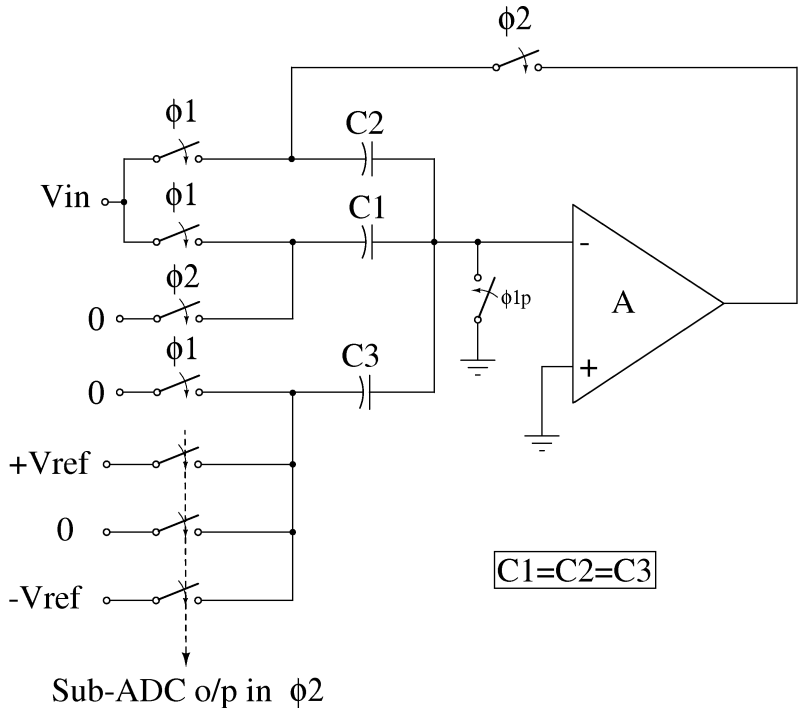


Figure 2.28: Modified MDAC in which a separate capacitor is used to inject references

Performance degradation is caused by the reference buffer because a regular MDAC stage shown in Fig. 2.17 presents a different load every cycle. The capacitors are charged to the input value before amplification phase making the amount of charge that the buffer has to transact different cycle to cycle. As a workaround, the regular MDAC stage is sometimes modified as shown in Fig. 2.28. In this case a separate capacitor is used to inject reference into the MDAC. This ensures that the load seen by the buffer is same every cycle ensuring that it settles to the same value every cycle irrespective of whether it is a fast type or slow type. The buffer now is best designed with just enough output capacitance to filter the noise. Disadvantage with this modified MDAC is its reduced feedback factor.

2.3.6 Switches

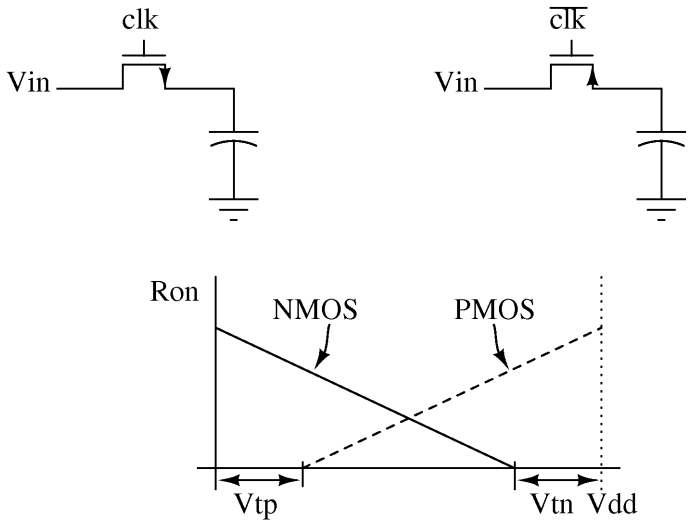


Figure 2.29: NMOS and PMOS switches

The simplest possible switch is a pass transistor shown in Fig. 2.29. In the case of NMOS, when the gate voltage is high, drain and source are electrically connected and conduction happens between them. It can be seen that the maximum voltage that can pass through is Vdd-Vt. Conversely in a PMOS switch, the minimum voltage that can pass through is Vt. For the conduction range to be 0 to Vdd, the switches are modified as shown in Fig. 2.30 to form the CMOS pass gate.

For applications where linearity of the output is not a concern, either a NMOS or a PMOS would just work fine in their conduction region. Fig. 2.29 shows the on resistance of NMOS and PMOS switches. These switches with varying on resistance would produce distortion at the output that is undesirable in analog applications. There are two popular ways of countering this and are described below.

a) CMOS transmission gate

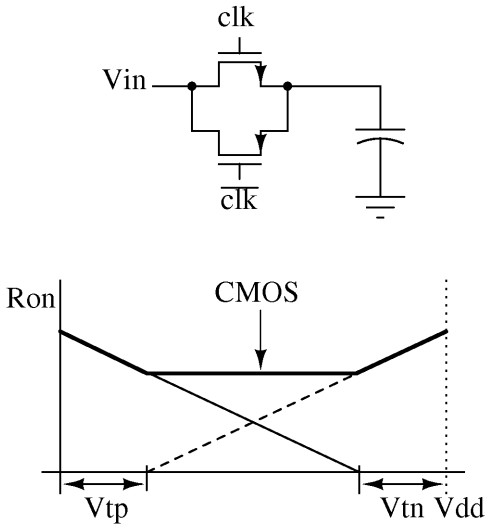


Figure 2.30: CMOS transmission gate

Close look at Fig. 2.29 would suggest that if both NMOS and PMOS switches are used in parallel, then the effective on resistance looks as shown in Fig. 2.30. This combination called the transmission gate works well in many applications. When putting the NMOS and PMOS in parallel, their relative sizing is in the ratio of their mobility to ensure equal on resistance. Apart from increasing linearity, this combination also helps in charge injection which is a big issue in switched capacitor circuits. The gate charge in NMOS and PMOS is of opposite polarity. When the switch is closed, these oppositely charged charge packets that come out cancel each other thus improving signal integrity to a certain extent.

b) Bootstrapped switch

The varying ON resistance of a transistor is because of its changing gate to source voltage (Vgs) during the sampling phase. If this Vgs can be held constant during the sampling period, then the cause of non-linearity is eliminated. This is done as shown in Fig. 2.31. A capacitor is pre-charged to a fixed voltage (>Vt). Because of its availability, this pre-charge voltage is usually Vdd.

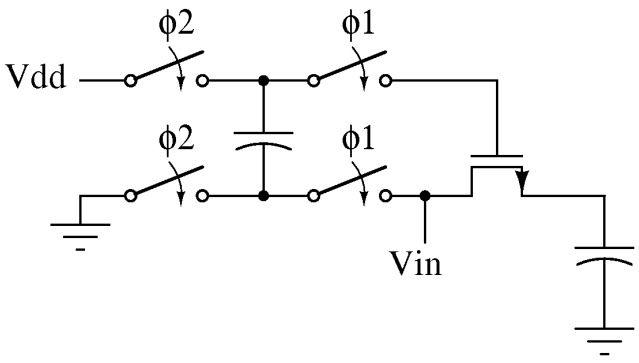


Figure 2.31: Bootstrapped switch

In the sampling phase one end of the capacitor is connected to the input whereas the other end is connected to the gate of the transistor. This makes the gate to source voltage independent of the signal applied ensuring highly linear performance. Though the concept is still the same, many versions of this circuit have come up. A version of it is shown in Fig. 2.32.

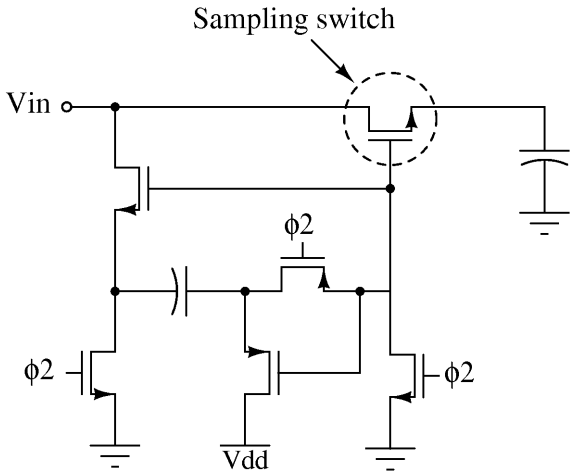


Figure 2.32: An implementation of bootstrapped switch

As the gate voltage can reach 2Vdd, the question of reliability comes up. It has been shown that the sampling switch is completely reliable as the gate to source voltage is still under Vdd [22]. This is the circuit of choice for all low voltage applications and for cases where linearity required is greater than 80 dB.

2.4 Noise

Thermal noise is an important limiting factor in high resolution ADCs. In a well designed ADC, this contributes to two-thirds of the noise budget. The rest comes from quantization noise which is fixed basing on the resolution. So the design effort goes into minimizing the thermal noise contribution.

In a switched capacitor pipelined ADC there are two main components of thermal noise: kT/C noise and opamp thermal noise. kT/C noise comes from the sampling operation. The integrated noise power sampled onto a capacitor of size C is kT/C irrespective of the switch resistance and hence its name. Because of the inherent sampling nature of the ADC, this noise comes about at every stage when the output of a MDAC is sampled by the next stage capacitors. As the ADC has a series of gain stages, the input referred noise contributed by the later stages is smaller as it gets divided by the gain of preceding stages. Eq. 2.5 shows the input referred kT/C noise of a 1.5-bit per stage pipeline. The first stage's noise remains as it is and hence is a significant portion.

$$V_{rms}^2 = \frac{kT}{C} + \frac{1}{2^2}\frac{kT}{C} + \frac{1}{2^4}\frac{kT}{C} + \frac{1}{2^6}\frac{kT}{C} + .. + \frac{1}{2^{2(N-1)}}\frac{kT}{C} \tag{2.5}$$

2.4.1 Scaling

Ideally we want the noise to be as small as possible. To minimize the kT/C noise, the capacitor has to be increased. But increased capacitor size means more power consumption. A trade-off exists between the two where the capacitor size is chosen for a certain noise level basing on the ADC resolution. The above equation also brings about an interesting concept of scaling. As evident from it, the noise

contributed by later stages gets divided by the gain stages. So the capacitor size can be scaled along the stages to reduce power consumption at the cost of little noise overhead. This has become a standard practice in present day products. With a scaling of α, the noise equation gets modified as shown in Eqn. 2.6.

$$V_{rms}^2 = \frac{kT}{C} + \frac{1}{2^2}\frac{kT}{\alpha^2 C} + \frac{1}{2^4}\frac{kT}{\alpha^3 C} + \frac{1}{2^6}\frac{kT}{\alpha^4 C} + .. + + \frac{1}{2^{2(N-1)}}\frac{kT}{\alpha^{N-1} C} \tag{2.6}$$

Though there is a consensus on benefits of scaling, the best scaling factor is something that is debated upon. A school of thought is that the capacitor size should be scaled so as to make the total noise contributed by all the stages beyond the first equal to that of the noise contributed by the first stage. Going by this argument, the noise contributed by a particular stage becomes equal to the total noise contributed by all the stages following it. Evaluating Eqn. 2.6 basing on this argument gives the scaling factor to be 0.5 and the total input referred noise to be 2kT/C instead of (4/3)kT/C when there is no scaling. Apart from increase in noise, a disadvantage with using 0.5 scaling factor is that the capacitor size in the later stages can get small enough to concern matching requirements. As the present day processes have become mature, capacitor size is dominantly chosen basing on kT/C noise requirement and not matching as the later is guaranteed to a certain extent. This was not the case in yesteryears when getting good matching was difficult to achieve. Assuming a capacitor of 2pF is chosen as the first stage sampling capacitor for a 12-bit pipeline and if scaling of 0.5 is implemented, the capacitor size of each stage is shown in table below. It can be observed that the size gets really small after 4th stage so as to risk the matching requirements. One practice to avoid this problem is to stop scaling after a certain stage and let the capacitor size remain constant from then on. In the example described, it

is optimum to stop the scaling at 5th stage and let the size be at 125fF for the following stages.

Stage	**Matching required in bits**	**Sampling Capacitor with scaling of 0.5 (in pF)**	**Sampling Capacitor with scaling of 0.75 (in pF)**
1	12	2	2
2	11	1	1.5
3	10	0.5	1.125
4	9	0.25	0.84
5	8	0.125	0.63
6	7	0.063	0.48

Table 2.2: Variation of capacitor size with scaling

Another school of thought regarding scaling is that the ratio should be around 0.7-0.8 to ensure power benefits as well as matching requirements. Many commercially available products are believed to employ this scaling factor. Using the same example as above, the capacitor size with scaling of 0.75 is also shown in the table. Arriving at the proper scaling ratio involves many trade offs as described above and can be a topic of exclusive study as in [23].

2.4.2 Thermal Noise of OTAs

Thermal noise from the OTA is the next significant component of noise budget. Same as in the case of kT/C noise, OTA noise also gets scaled down by the gain stages. Due to the large device sizes that an OTA usually has, 1/f noise is insignificant compared to thermal noise. The input referred noise of an OTA is inversely proportional to the Gm of the OTA. Increasing Gm means increased power consumption. So a trade off exists between the power burned and noise. In a telescopic cascode opamp, ideally we want the noise from other transistors to be small compared to the noise from input pair. Noise from cascode devices is negligibly small

compared to other devices because of source degeneration. To minimize noise from the load transistors, gm of those devices is made as small as possible.

In a good design, noise from input and feedback switches is filtered by the opamp bandwidth as the RC time constant of the switches is made larger than the opamp bandwidth hence making the noise contributed small. But when it comes to practice, it is always good to account for noise from switches too and the best way to do that is by using PSS and PNOISE analysis in spectre or its equivalent in other simulators.

2.5 Opamp gain and bandwidth

Opamp gain and bandwidth are the important parameters for OTA design. Both of them are determined by the number of bits that are to be resolved following the OTA. These requirements are best explained using an example. Consider that a N-bit Fs MSPS pipelined ADC has to be designed using 1.5-bit per stage architecture. The first stage MDAC output is used to resolve (N-1)-bits by the stages that follow it. The OTA gain has to be high enough to ensure (N-1)-bit accurate output.The gain A required is derived using the following relation:

$$
\begin{aligned}
V_o\left(\frac{1}{\beta}-\frac{A}{1+A\beta}\right) &< \frac{V_o}{2^N} \\
\frac{1}{\beta(1+A\beta)} &< \frac{1}{2^N} \\
\beta(1+A\beta) &> 2^N
\end{aligned}
$$

β=$\frac{1}{2}$ in a 1.5-bit stage. Substituting this in the above equation yields

$$A > 2^{N+2} \tag{2.7}$$

Bandwidth determines the settling accuracy of the opamp. Using the same example as above, the bandwidth required can be determined using the following equation.

$$\begin{aligned} V_o - V_o\left(1 - e^{\frac{-t}{\tau}}\right) = V_o e^{\frac{-t}{\tau}} &< \frac{V_o}{2^N} \\ e^{\frac{-t}{\tau}} &> \frac{V_o}{2^N} \\ \tau &< \frac{t}{N.ln(2)} \end{aligned}$$

Substituting τ=$\frac{1}{\beta\omega_t}$, β=$\frac{1}{2}$ and t=$\frac{1}{2F_s}$ yields

$$\omega_t > 4Nln(2)F_s \tag{2.8}$$

Chapter 3 . LOW POWER TECHNIQUES

Low power design techniques can fall into two categories, direct and indirect. The direct techniques are those in which either the pipeline architecture or the MDAC architecture is modified to reduce power. Indirect techniques are those in which the accuracy of the ADC is improved using calibration techniques that indirectly help in power reduction. Many such techniques exist and the popular ones are described below.

3.1 Direct Techniques

3.1.1 Opamp sharing

The first three stages of a pipelined ADC are shown in Fig. 3.1. It can be noticed that adjacent stages amplify the residue during opposite clock phases. The first MDAC amplifies the residue during $\phi 2$ where as the second MDAC amplifies the residue during $\phi 1$. It means that the opamp in each stage is idle for half clock cycle. The first stage opamp which is idle during $\phi 1$ can be used for residue amplification in stage 2 thus eliminating the need for a dedicated opamp in stage 2. In [2], it has been proposed that an opamp can be shared between two consecutive stages and it has proved to be an efficient technique to reduce power as the number of opamps in the ADC becomes half. A disadvantage with this technique is the memory effect. At the end of amplification phase there is a finite voltage at the input of the opamp which is stored on the input capacitors of the opamp. When it is transfered to the

next stage for amplification, this residual charge on the inputs causes distortion thereby causing 'memory' effect. If the opamp sharing was not taking place, the opamps are reset during the idle period thereby eliminating the issue. The amount of voltage at the input capacitors is inversely proportional to the opamp gain. As the opamps in a pipeline inherently have high gain, this effect is tolerable in many situations.

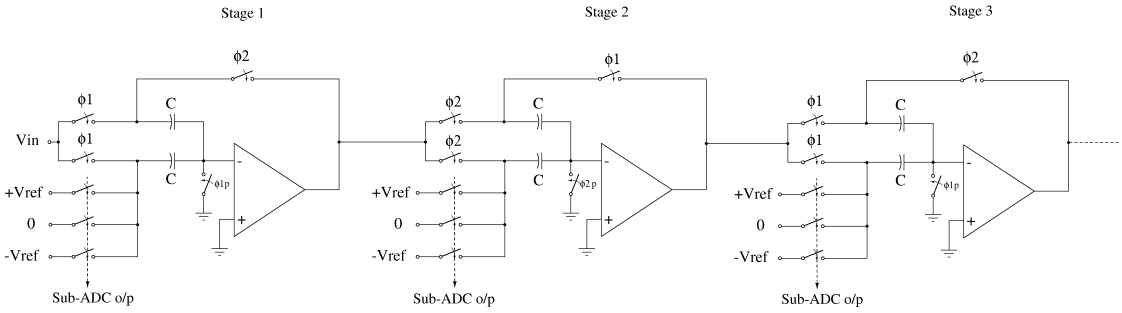


Figure 3.1: First three stages of a pipeline ADC

3.1.2 CDS & CLS

The power required to design an opamp reduces if the gain requirements of the opamp can be reduced. CDS and CLS are two techniques that enable it to be done [24, 25]. Both the techniques require an additional clock phase and square the given opamp gain.

Correlated double sampling

Fig. 3.2 shows an MDAC using CDS technique during amplification phase. At the end of $\phi 2$, the voltage at node Vx is -Vo/A. If the opamp gain A is infinite, this voltage goes to 0. During $\phi 2$ this voltage is sampled onto a capacitor Ccds as shown in the figure. In $\phi 3$, the MDAC is reconfigured resulting in an output residue that is now as accurate as from an opamp of gain A^2. This residue is passed

onto the following stage. CDS is modified to time shifted CDS and time aligned CDS in [26, 27] where the gain squaring operation is done in two phases.

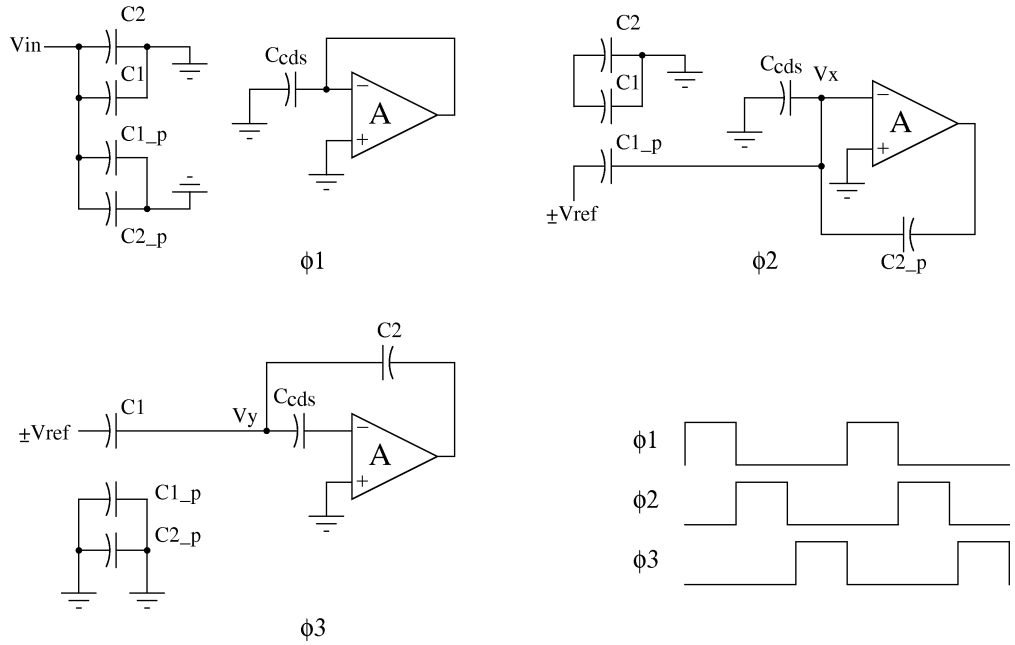


Figure 3.2: CDS operation

Correlated level shifting

Fig. 3.3 shows an MDAC using CLS technique during amplification phase. In $\phi 2$ the output residue is sampled onto a Ccls capacitor. In $\phi 3$, the MDAC is reconfigured resulting in an output residue that is now as accurate as from an opamp of gain A^2. This residue is passed onto the following stage. A big advantage with CLS technique is its reduced swing requirement of the opamp. After the first amplification phase $\phi 2$, the opamp generates an approximate residue. This is captured on the Ccls capacitor and used to get accurate residue in the critical phase $\phi 3$ during which the opamp swing is negligible. Though the opamp does have to swing in $\phi 2$, the actual residue generation is done in $\phi 3$ during which the swing requirements are relaxed hence pushing to MDAC to rail to rail operation.

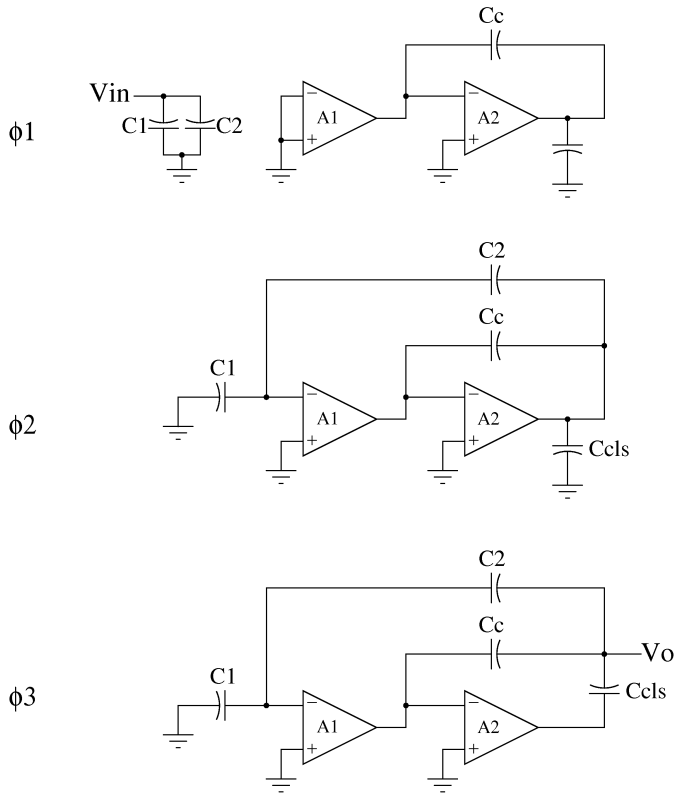


Figure 3.3: CLS operation

In references [25, 26], the above mentioned techniques were used to design a 10-bit pipeline from a low power 30-dB opamp. The techniques boost the opamp gain to 60dB which is required of a 10-bit opamp.

3.1.3 Reference scaling

The output residue of an MDAC is attenuated because of finite opamp gain and this causes missing codes which lead to distortion. In the reference scaling technique [28], the next stage's reference is also attenuated by the same factor that the signal gets attenuated by. This is done by passing the reference through the same MDAC and using the output as next stage's reference. The scheme is illustrated in Eqns.3.1. This ensures that the ratio between signal and reference remains

constant thereby eliminating the need for a high gain opamp. A 12-bit pipeline has been built using a low power 45-dB opamp in [28].

$$\begin{aligned} G_i(V_{in}^i - D_i V_{ref}^i) - D_{i+1} V_{ref}^{i+1} &= G_i(V_{in}^i - D_i V_{ref}^i - D_{i+1}\frac{V_{ref}^{i+1}}{G_i}) \\ &= G_i(V_{in}^i - D_i V_{ref}^i - D_{i+1}\frac{Vref^i}{2}) \end{aligned} \tag{3.1}$$

where

$$G_i = 2(1 + e_i)$$

$$V_{ref}^{i+1} = V_{ref}^i(1 + e_i)$$

3.1.4 Rail to rail input

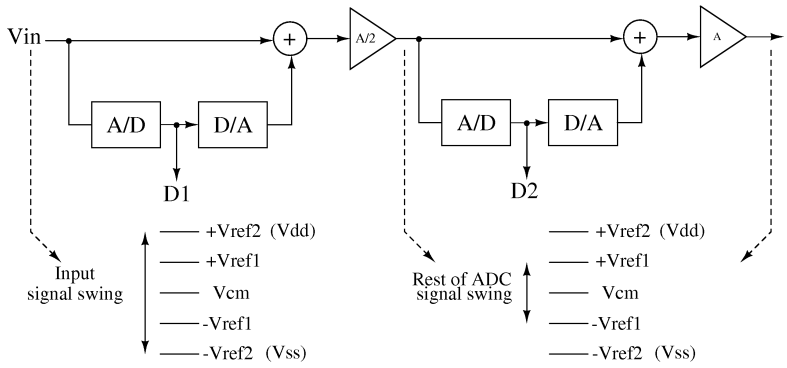


Figure 3.4: A rail to rain input pipeline ADC

The signal to noise ratio increases if the signal range can be increased. But the opamp linear range sets a limit on the maximum allowable swing limit. As a work around to that, the input swing to the opamp is allowed to be rail to rail but the output swing is compressed to the nominal linear range of the opamp as shown in Fig. 3.4. This compression is achieved by reducing the MDAC gain.

A disadvantage with this structure is the requirement of two sets of references. The first MDAC operates on a different reference than that of the rest of the ADC. Mismatch between the two sets of references causes distortion. Reliable operation of the ADC necessitates the references to be calibrated. Methods to operate on single set of references exist but they come at the cost of increased power consumption.

3.2 Indirect Techniques

3.2.1 Commutative Feedback Capacitor Switching technique

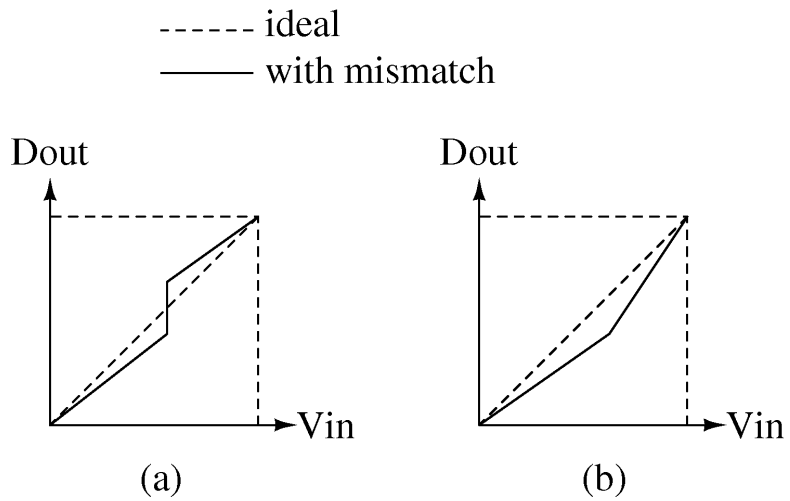


Figure 3.5: (a) Transfer curve with capacitor mismatch (b) Modified transfer curve with CFCS technique

In a gain of 2 stage, the capacitor that is used at the input and the one that is used for feedback are fixed during design. In the presence of mismatch the transfer curves looks as shown in Fig. 3.5(a) where there are missing codes resulting in increased DNL. A straightforward solution to this is to increase capacitor size to reduce DNL as both of them are related by Eqn. 3.2 [29] where N is the ADC reso-

lution, m is the number of bits resolved in first stage, C_{total} is the total capacitance of first stage and λ is a constant related to random variation of capacitance. CFCS technique minimizes DNL without having to increase the capacitor size and hence power [5]. In this technique, the input and feedback capacitors are chosen basing on the digital code from sub-ADC and the modified transfer curve looks as shown in Fig. 3.5(b). It can be noticed that there are no missing codes thus decreasing DNL substantially. The operation is shown in Fig. 3.6.

$$DNL = \frac{\lambda.2^{M-\frac{m}{2}}}{\sqrt{C_{total}}} \tag{3.2}$$

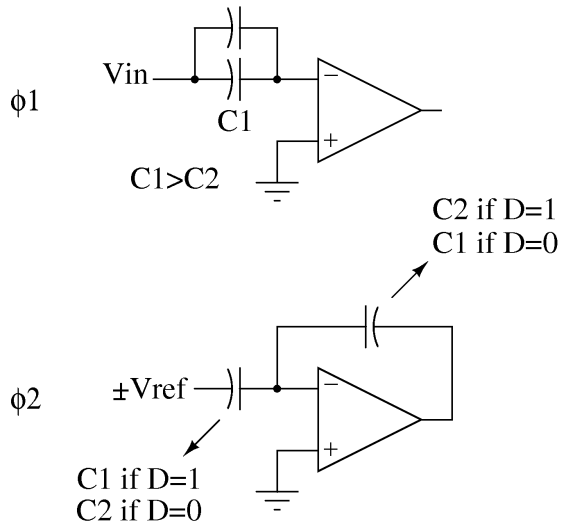


Figure 3.6: CFCS scheme

3.2.2 Passive Capacitor Error Averaging technique

Similar work is done in [30] where the capacitor mismatch is reduced using Passive Capacitor Error Averaging thereby facilitating use of a smaller capacitor. This technique has two amplification phases making it a 3 phase system. In the first am-

plification phase $\phi 2$, the input and feedback capacitors are in their usual positions and the residue is sampled onto next stage capacitors. In the second amplification phase $\phi 3$, the input and feedback capacitors are swapped allowing the output to settle again and this time the next stage is reconfigured as shown in Fig. 3.7. Error due to capacitor mismatch gets averaged out on the next stage thus resulting in very good linearity. This technique allows choosing the capacitor size basing on kT/C noise requirements and still not having any matching issues.

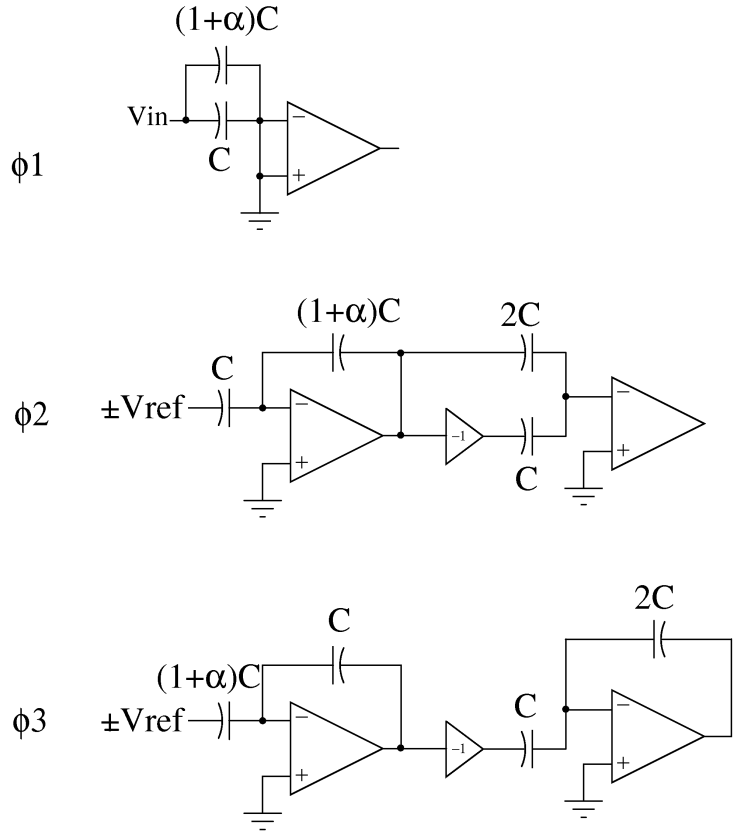


Figure 3.7: PCEA technique

3.2.3 Ratio independent multiplication

Fig. 3.8 illustrates the ratio independent multiplication technique. This scheme needs four clock phases at the end of which the residue value is independent of the capacitor ratio thus making it immune to capacitor mismatches. In $\phi 1$ the input is sampled onto the capacitor C where as the other capacitor $(1+\alpha)$C is reset. In $\phi 2$ the sampled charge is transfered from C to $(1+\alpha)$C. In $\phi 3$ input is again sampled on to C again. In $\phi 4$, the charge on $(1+\alpha)$C is sent back to C thus accumulating 2Vin$\pm$Vref on it that is not dependent on the capacitor ratio.

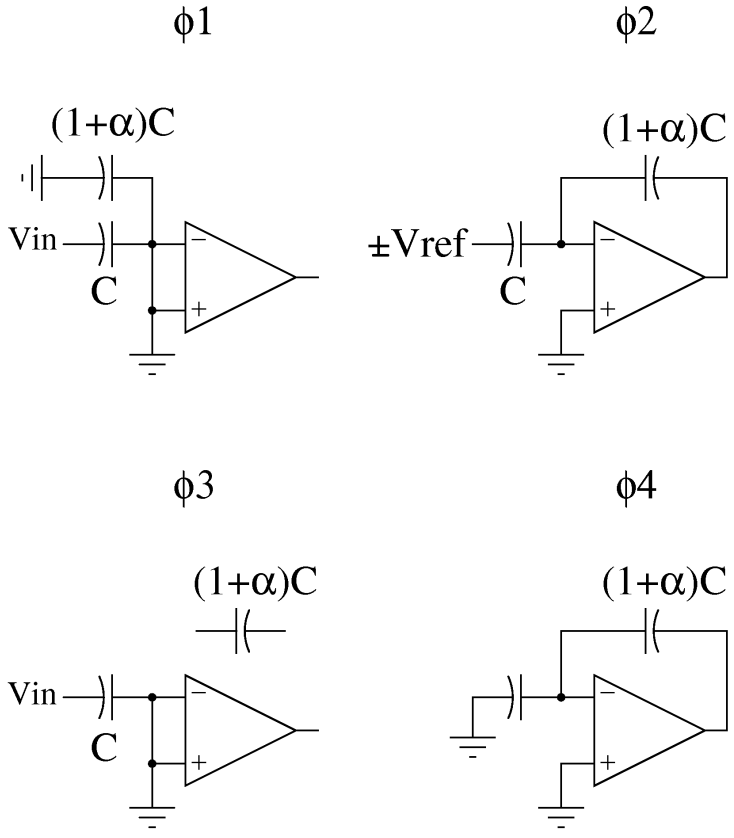


Figure 3.8: Ratio independent multiplication

3.2.4 Radix calibration

In an ideal N bit pipeline ADC, the reconstructed ADC output is given by Eqn. 3.3. If the opamp gain was finite the output residue of an MDAC stage is related to input as shown in Eqn. 3.4. The coefficient of Vin is no longer 2 but ra=(2+α)(1+δ) which is the new radix. Updating Eqn. 3.3 with the new radix gives Eqn. 3.5. If the radix ra of each stage is found, then the output digital codes can be calibrated to get back the performance. Several methods exist to extract the radix [31–33]. The extraction mechanism sometimes involves modifying the MDAC or injecting a test signal along with the input in background or instead of the input in foreground.

$$D_{out} = \sum_{k=0}^{n-1} D_{n-k}.2^k \tag{3.3}$$

$$V_{out} = (2+\alpha)(1+\delta)(V_{in} + D\frac{1+\alpha}{2+\alpha}V_{ref}) \tag{3.4}$$

$$D_{out} = \sum_{k=0}^{n-1} D_{n-k}.(ra_0.ra_1...ra_k) \tag{3.5}$$

Chapter 4 . Capacitor and Opamp sharing technique with a scheme to cancel signal dependent charge kickback

4.1 Introduction

Pipelined analog-to-digital converters (ADCs) are considered most suitable for low-power/high-speed applications [34–37]. Because the accuracy requirements gradually decrease to the later stages of the pipeline architecture, properly scaling the capacitor size and opamp design/bias can efficiently reduce power consumption while maintaining the same ADC resolution [38, 39]. Sharing an opamp between two consecutive stages can further reduce power and has been demonstrated to give good performance for low power operation [2, 40]. In a pipelined ADC it is well known that maximum power is consumed in the first stage. To reduce power in it, a capacitor sharing technique was recently proposed [41–43] where the residue held on the feedback capacitor is used for the next stage MDAC operation thereby reducing the opamp load. This means that every alternate stage in the ADC can be made load-free. Our proposed technique simultaneously applies both capacitor and opamp sharing thereby gaining a two fold reduction in power. To further reduce power, sample and hold (S/H) is removed [17]. This would cause signal-dependent kick-back into the input source. In the presence of source impedance this kick-back would cause distortion. Simulations show a reduction in SNDR of about 6 dB near Nyquist input. One solution to mitigate this is to reset the capacitors before sampling phase. But that would mean adding an additional phase and hence making the ADC slow. A novel reset scheme which fits in well

with capacitor sharing technique has been used, which would reset the capacitors without the need of an additional clock phase or extra set of capacitors [18, 44]. A 11-bit 80MSPS pipelined ADC is designed in 0.18μm process using the above mentioned techniques. Measurement results that show the efficiency of the proposed techniques are presented.

4.2 Capacitor and Opamp sharing technique

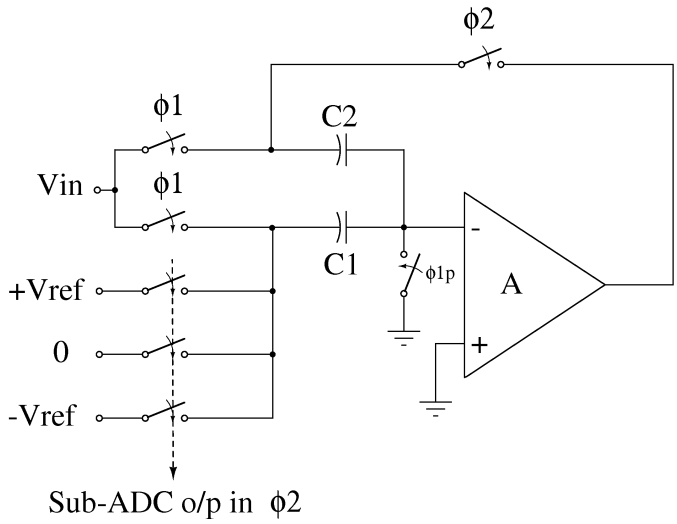


Figure 4.1: Typical switched capacitor MDAC

One of the simplest implementations of pipelined ADCs incorporating digital redundancy is based on the 1.5-bit-per-stage architecture. This architecture is widely used to maximize conversion speed [16]. Fig. 4.1 shows a typical multiplying digital-to-analog converter (MDAC) used in this type of pipelined ADC architecture. Fig. 4.2 shows an MDAC in amplification phase. At the end of the phase, it can be observed that the same residue value is present on both the load and feedback capacitors. It is assumed that the virtual ground node is close to 0 and this assumption is valid as long as the opamp gain is high enough. As the

information we want is available on the feedback capacitors, the load capacitor can be eliminated altogether and the feedback capacitor can act as next stage's load capacitor. The feedback capacitor is split into two halves and these two halves become the input and feedback capacitor of next stage thereby obviating the need for a dedicated set of load capacitors and hence saving power. This capacitor sharing technique goes well with opamp sharing technique and the whole operation is explained in detail in the rest of this section.

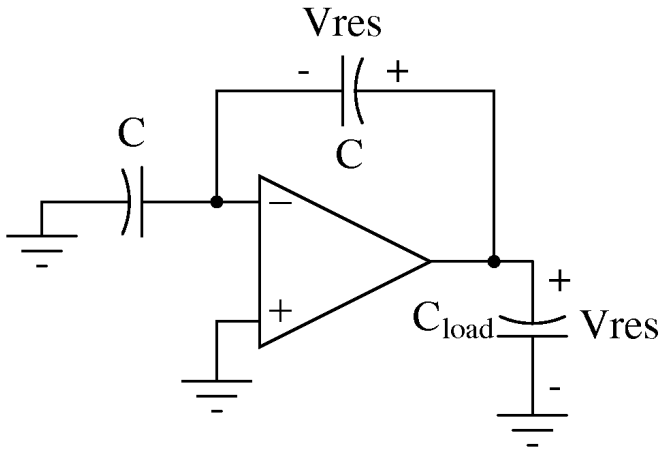


Figure 4.2: MDAC during amplification phase

Fig. 4.3 shows first two stages of a conventional 1.5-bit stage pipeline incorporating only the opamp sharing technique. During $\phi 1$, input differential signal is sampled by the capacitors $C^{+}_{1(i,f)}$ and $C^{-}_{1(i,f)}$. During this phase, the opamp generates the residue value Vres2 which is transferred to the third stage (to the third stage sampling capacitors $C^{+}_{3(i,f)}$ and $C^{-}_{3(i,f)}$). During $\phi 2$, capacitors C^{+}_{1f} & C^{-}_{1f} are connected in the feedback path and C^{+}_{1i} & C^{-}_{1i} are connected to one of three possible DAC voltages, ±Vref or 0, depending on the sub-ADC output D1. The generated residue value Vres1 is sampled by the second stage capacitors, $C^{+}_{2(i,f)}$ and $C^{-}_{2(i,f)}$. It is apparent that this technique needs only one opamp to generate residues Vres1 and Vres2 of the two consecutive stages. In this configuration, it is

worthy to note here that when Vres1 is transferred to $C^{+}_{2(i,f)}$ & $C^{-}_{2(i,f)}$, the same information is also already stored on C^{+}_{1f} & C^{-}_{1f}, respectively.

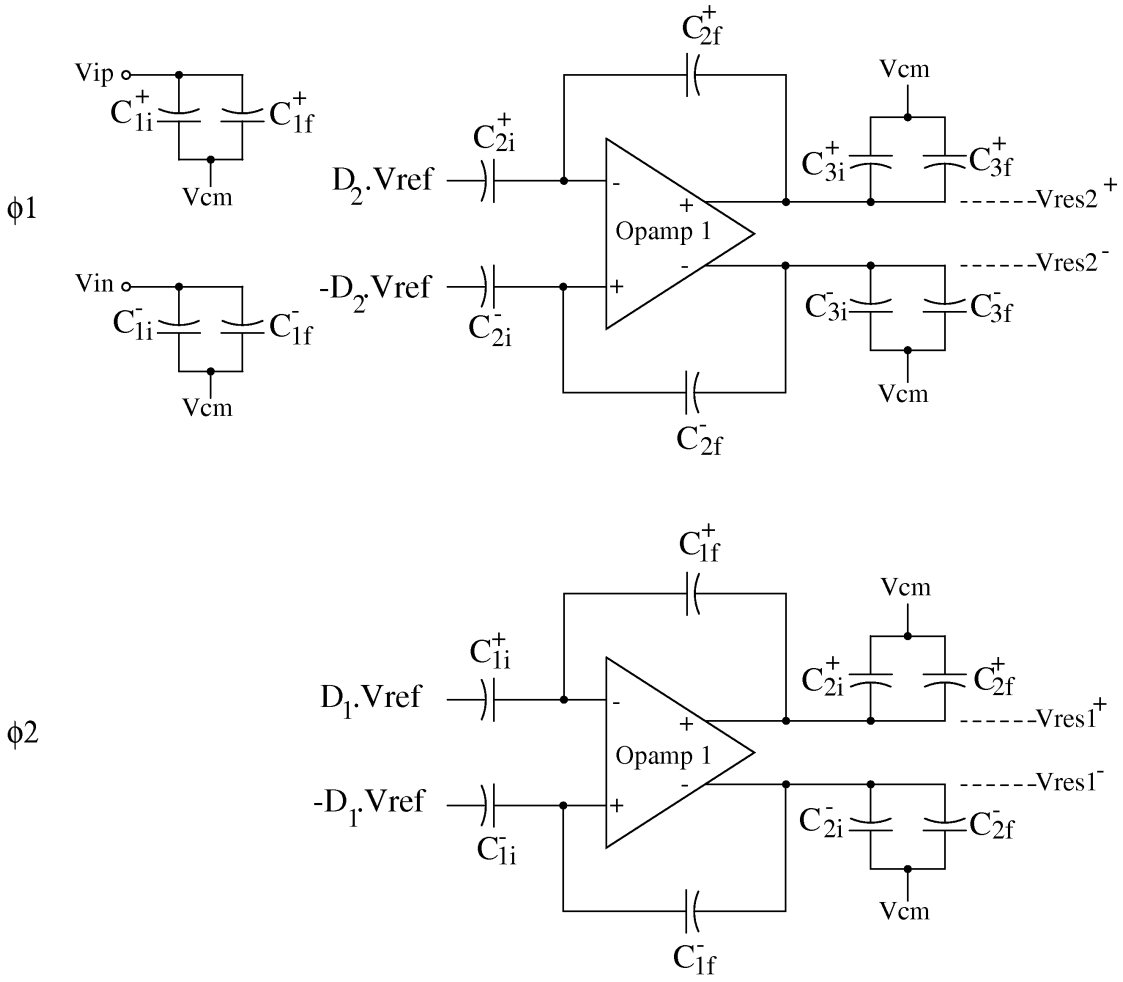


Figure 4.3: Residue generation using opamp sharing technique

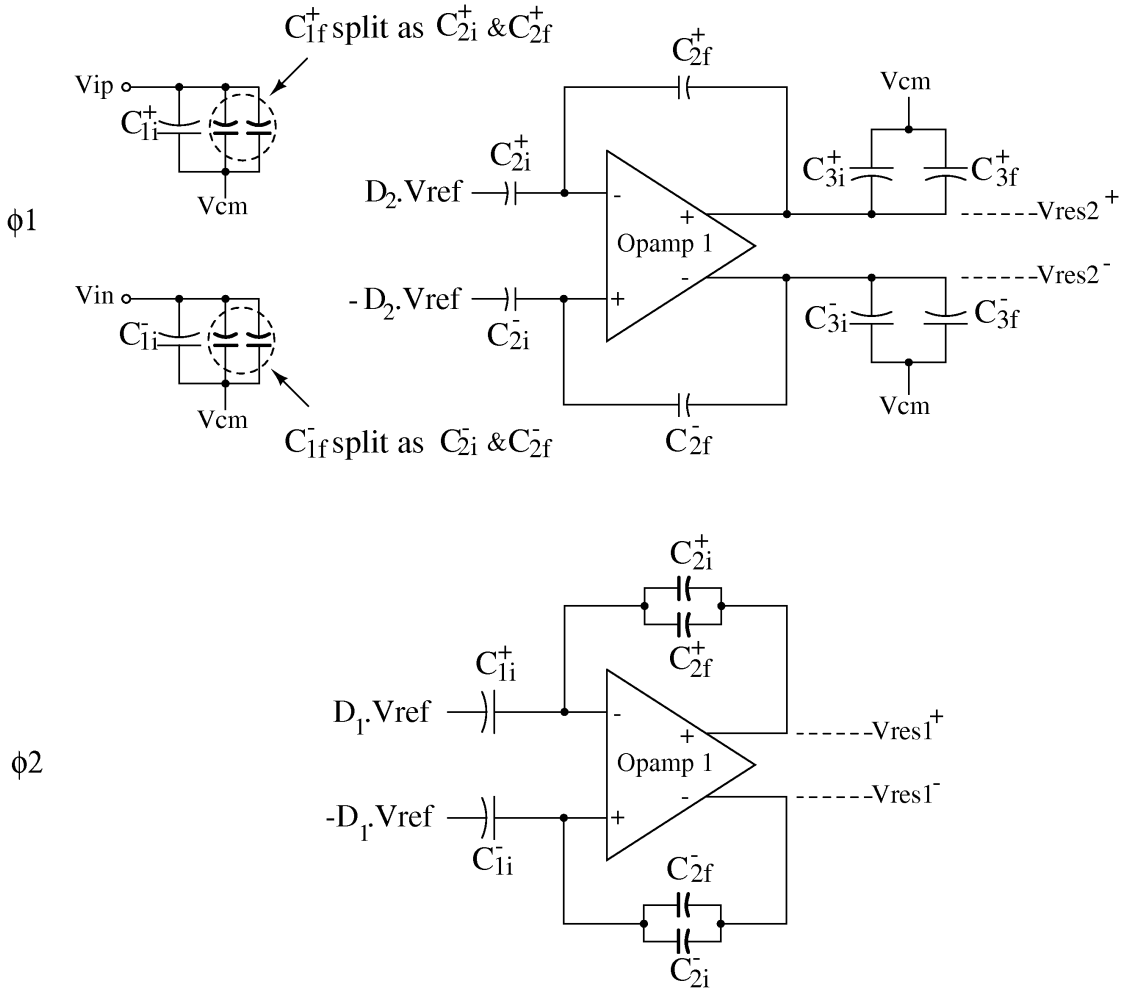


Figure 4.4: Residue generation using capacitor and opamp sharing technique

Fig. 4.4 shows the proposed capacitor *and* opamp sharing technique. Here, C^+_{1f} and C^-_{1f} are composed of two equal parts each, C^+_{2i} & C^+_{2f} and C^-_{2i} & C^-_{2f}, respectively. During $\phi 1$, input value is initially sampled on to the capacitors, $C^+_{1(i,f)}$ and $C^-_{1(i,f)}$. During $\phi 2$, the opamp generates the residue value but this is not transferred to sampling capacitors of the second stage. It should be noted here that the residue value is held on the feedback capacitors C^+_{1f} & C^-_{1f} that have been split into equal halves as shown in the figure. During the next phase $\phi 1$, using the stored value on the feedback capacitors, second residue value is generated and

transferred to sampling capacitors of the following/third stage, $C^{+}_{3(i,f)}$ and $C^{-}_{3(i,f)}$. Since the next input value has to be sampled while generating the second stage residue, two sets of feedback capacitors distinguished by thick and thin lines for the capacitors (see Fig. 4.4 during $\phi 1$ where thick ones are being sampled and thin ones are in feedback), an even set and odd set, are used alternately. Given the consideration that the most power hungry operation in a pipeline ADC is the very first stage, this capacitor and opamp sharing technique efficiently reduces the overall power consumption because the effective capacitive load of the opamp is significantly reduced. In the conventional pipeline operation, the effective loading capacitance on each side of the opamp is $C_{2i} + C_{2f} + (1\text{-}\beta)C_{1f}$, as seen in Fig. 4.3, where β is the feedback factor due to capacitor voltage divider feedback. In the proposed capacitor sharing technique, the effective loading capacitance reduces to just $(1\text{-}\beta)C_{1f}$ as seen in Fig. 4.4. Simulation results show that input referred offset of the MDAC stage remains the same as that of a regular 1.5-bit per stage architecture.

4.2.1 Scaling and kT/C noise

The kT/C noise plays an important role in choosing the proper sampling capacitor value, and it strongly defines the fundamental limit (along with opamp noise) of the overall ADC. In a standard 1.5-bit-per-stage pipelined ADC, if a 75% scaling is applied from one stage to the next, which is considered a conservative scaling ratio, the input referred kT/C noise is about 1.5 kT/C. With the capacitor sharing technique, as proposed, the scaling factor is inherently 50% since the feedback capacitor is used to sample the residue value. When applying 50% scaling, the input referred kT/C value increases to about 1.9 kT/C. Compared with the 75% scaling case, the

capacitor sharing technique increases the input referred kT/C noise by about 27%. Because this result is normalized to input sampling capacitor, simply increasing the size of the sampling capacitor by the same amount (27%) would make the noise same. Increasing the capacitor size may initially seem disadvantageous. However, in the capacitor sharing technique, because the capacitor values scale so quickly (by 50% from one stage to the next), the capacitance loading at each MDAC stage decreases significantly. In the conventional case, for example, applying 75% scaling, the effective loading capacitance is $2C_1(=2\times0.75C_1+0.5\times C_1)$, as shown in Fig. 4.5, assuming low opamp input capacitance (simplified discussion here). On the contrary, the corresponding value with capacitor sharing technique, even after 30% increase (over estimating 27%), is $0.65C_1(=0.5\times1.3C_1)$. The implied best case improvement is a three fold power saving.

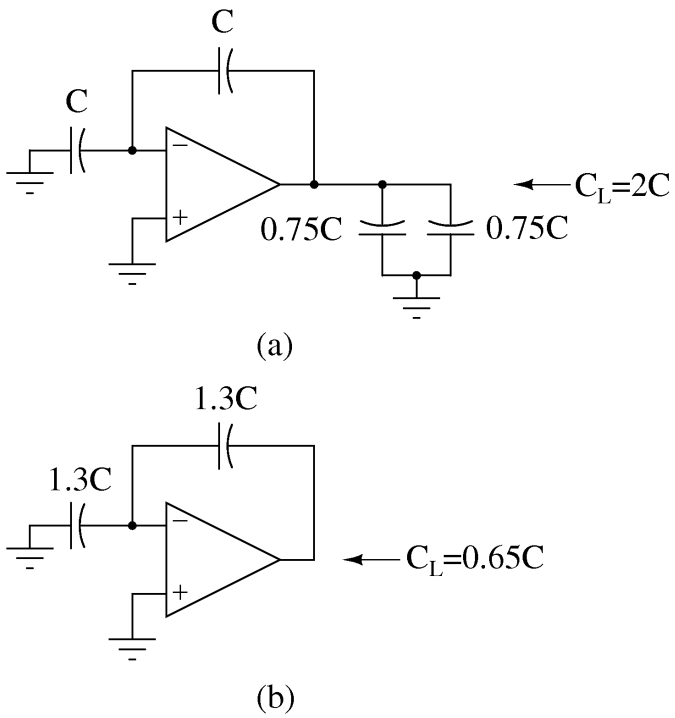


Figure 4.5: (a) Conventional amplification phase (b) Amplification phase with capacitor sharing

4.3 Reset without extra phase

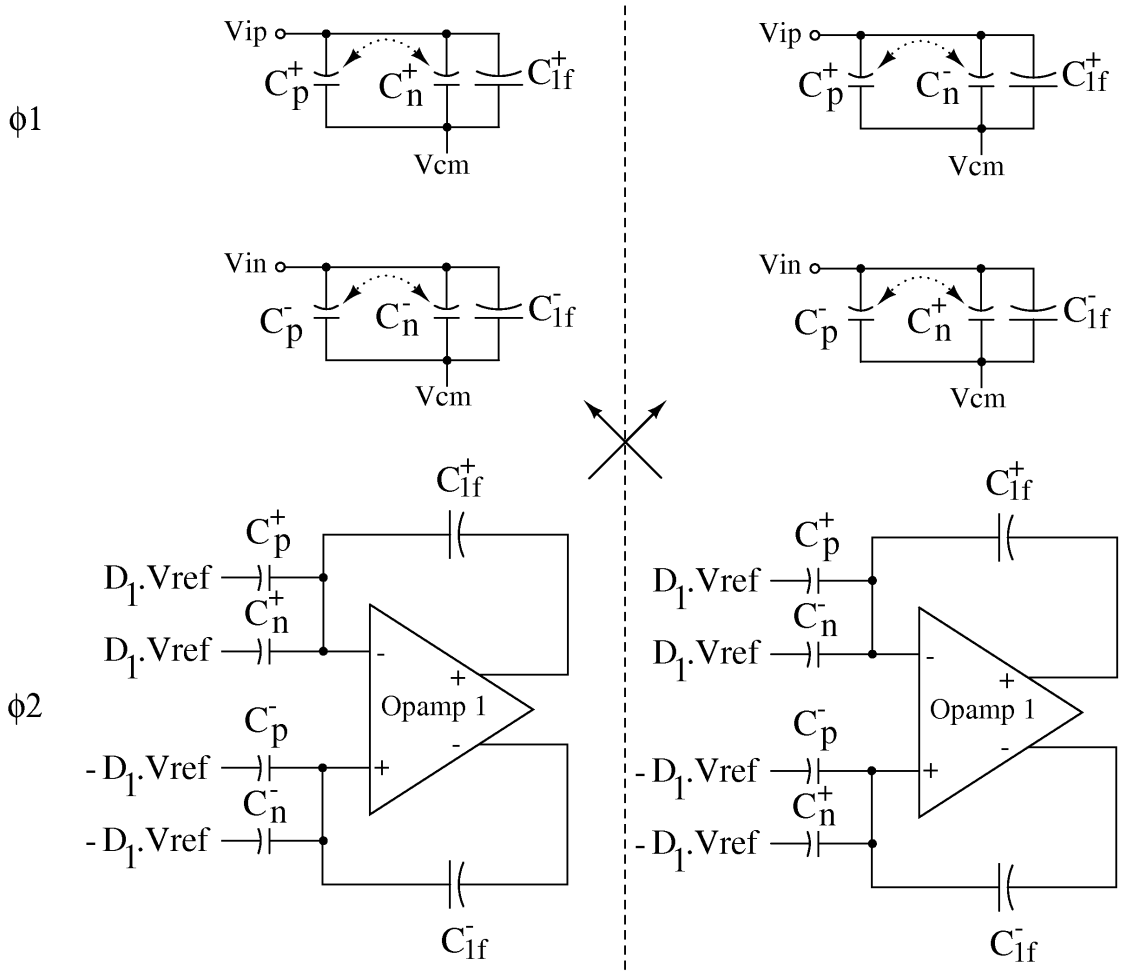


Figure 4.6: Resetting without extra clock phase

The capacitors C1 and C2 in Fig. 4.1 have some charge on them at the end of amplification phase $\phi 2$. When they return to sampling in the next phase, the input source should charge these capacitors with the new input voltage after absorbing the residual charge on them. In the presence of source impedance, this operation becomes a challenging task, and the sampling does not happen accurately, leading to distortion. This problem is magnified at high speed operation due to reduced time available. Prior techniques to overcome this problem include using an ad-

ditional clock phase to reset the capacitors before they return to sampling. This solution works at the cost of decreased conversion speed. A technique which would reset the capacitors without extra clock phase is described below. Fig. 4.6 shows the differential picture on how the input capacitors C_{1i}^{+} & C_{1i}^{-} are reset. On both positive and negative sides, C_{1i}^{+} and C_{1i}^{-} are split into two halves C_{p}^{+} & C_{n}^{+} and C_{p}^{-} & C_{n}^{-}, respectively. Consider the left half of the figure. At the end of amplification phase ($\phi 2$), C_{p}^{+} & C_{n}^{+} and C_{p}^{-} & C_{n}^{-} would have been charged either to the same common mode voltage or to equal and opposite polarity voltages ($\pm$Vref) based on sub-ADC code D1. In the following sampling phase C_{n}^{+} and C_{n}^{-} swap positions as shown. This would cause charge sharing between C_{p}^{+} & C_{n}^{-} and C_{p}^{-} & C_{n}^{+}, hence resetting them. On the other hand, as described before, there are two sets of feedback capacitors as indicated in Fig. 4.4 by thick and thin lines that are used alternately. In phase $\phi 2$ when one set is used for amplification, the other set is idle. The idle set goes to sampling in the next phase. So the idle time is used to reset them. This way the reset is implemented without requiring an extra clock phase. Simulations with the reset scheme show no performance degradation because of the source impedance, which otherwise went down by 6 dB with Nyquist input at 80MSPS operation.

4.4 Circuit Design

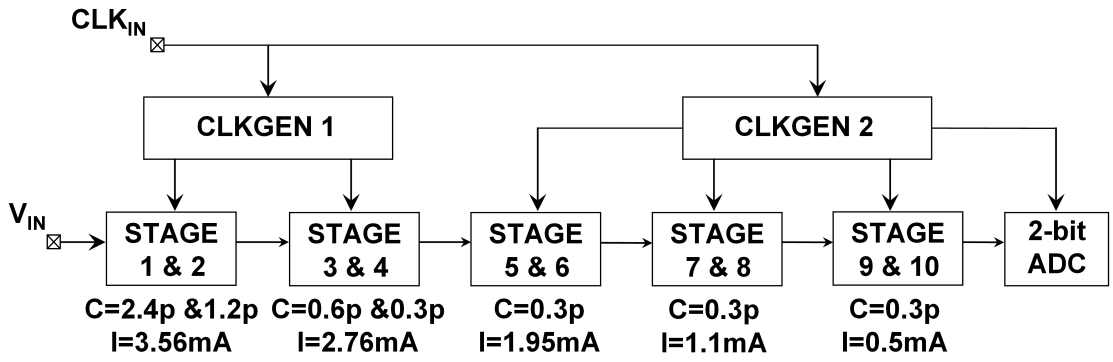


Figure 4.7: Block diagram of the ADC

A 1.5-bit per stage architecture is chosen to maximize speed. Capacitor and opamp sharing technique is used only for first four stages as the sampling capacitor becomes very small after that. Opamp sharing is still used in all stages. The size of sampling capacitors and opamp current of each stage are shown in Fig. 4.7. Because our initial intent was for a higher resolution ADC, the capacitor values were over designed (and much more power consumed) in this prototype IC.

4.4.1 Capacitor size

Capacitor size is an important design parameter in a pipeline ADC. For a signal swing of V, the signal to kT/C noise ratio (considering first 4 stages) is given by the following equation:

$$\frac{\frac{V^2}{2}}{\frac{kT}{C} + \frac{1}{2^2}\frac{kT}{\alpha C} + \frac{1}{2^4}\frac{kT}{\alpha^2 C} + \frac{1}{2^6}\frac{kT}{\alpha^3 C}} \tag{4.1}$$

where α is the scaling factor. In this case, α=0.5 because of capacitor sharing. A capacitor size of 2.4pF is chosen based on a swing of 1.6V and SNR of 70 dB.

4.4.2 Opamp

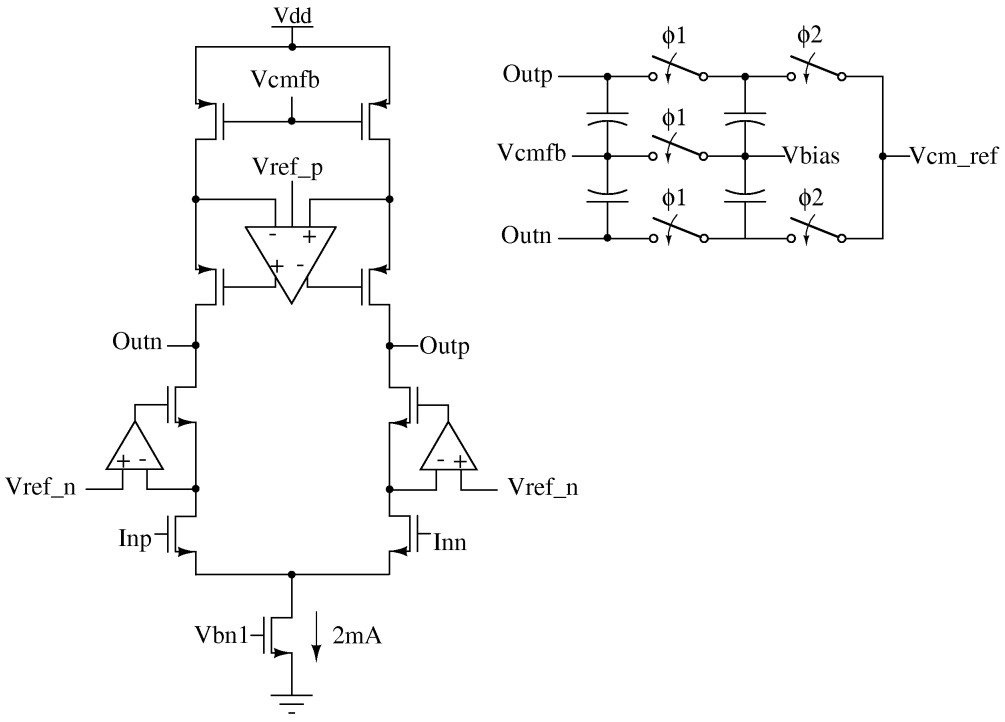


Figure 4.8: First stage opamp

Going by the speed advantage it has, a telescopic opamp with gain boosting is chosen for the ADC [45]. In 0.18μm process and 1.8V supply, this opamp offered a signal swing of 1.6Vpp differential. The opamp is shown in Fig. 4.8. The simulated gain is 80 dB. Current consumed in the main opamp is 2mA. The gain achieved from the main section of the opamp is 50 dB. Gain boosting amplifiers help to increase this gain to 80 dB. A switched capacitor CMFB loop is chosen to minimize power consumption. This CMFB loop does not have any limitations on the signal swing hence making it best suited for applications which can tolerate the glitches it brings because of its clocked nature.

There are two ways of implementing the gain boosting amplifier. Single ended and differential, each with its own advantages. A single ended amplifier's main

advantage is its ease of layout. As the two single ended amplifiers don't have to interact with each other, they can be put with their respective branch of the main amplifier in layout. This helps in having a clean layout with no wires running across. The advantage with differential implementation is its slightly reduced power consumption. The same amplifier is used to boost the impedance on both the branches of the main amplifier hence making it power and area efficient. Using the advantages of both the implementations, the n-side gain boosting is done using two single ended amplifiers so as to keep the layout on the signal side clean. The p-side gain boosting is done using a differential amplifier. This also helps to stabilize CMFB by reducing CMFB gain.

4.4.2.1 N-side gain boosting amplifier

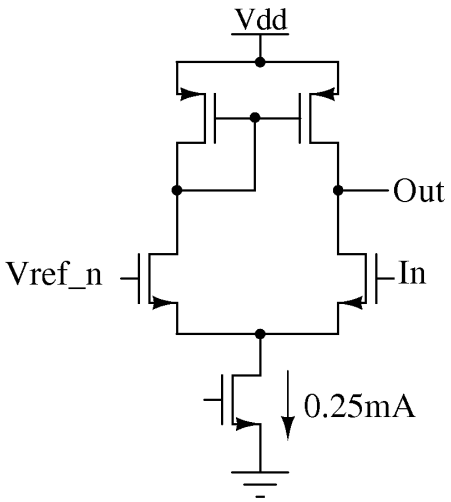


Figure 4.9: N-side gain boosting amplifier

This technology offered low Vt devices and we took advantage of them in designing the gain boosting amplifiers. Conventional n-side gain boosting amplifier would have a pmos input which makes it power hungry to get enough bandwidth

to ensure stability. But this technology facilitated the use of nmos input pair as shown in Fig. 4.9. The n-side gain boosting amplifier has a common mode of 0.4V which was enough to operate it satisfactorily. This amplifier has simulated gain and UGB of 30 dB and 1.1GHz, consuming 0.25mA [19].

4.4.2.2 P-side gain boosting amplifier

The amplifier is chosen to be single stage to ensure low power operation. The quiescent voltage of nodes between which the gain boosting amplifier is placed is shown in Fig. 4.10. Consider a standalone differential amplifier that is a potential candidate for gain boosting shown in the figure. With the required voltages marked, it can be noticed that the input pair is driven to triode region thus making it tough to get useful gain from it. A workaround for this is shown in Fig. 4.11. The level shifters are used to obtain high gain from the opamp while retaining the high speed benefits. The currents in each branch are shown and the whole amplifier consumes 0.7mA, giving gain and UGB of 30 dB and 1.1GHz. To save power, a separate common mode feedback loop is avoided and a self biased loop is used.

4.4.3 Sampling switch

Both the bootstrapped [21, 29] and transmission gate structures were explored for the input sampling switch. The bootstrapped switch can easily give a SNDR of 90 dB. But for an SNDR of 70 dB with 1.6V signal swing, a transmission gate structure was found to be sufficient.

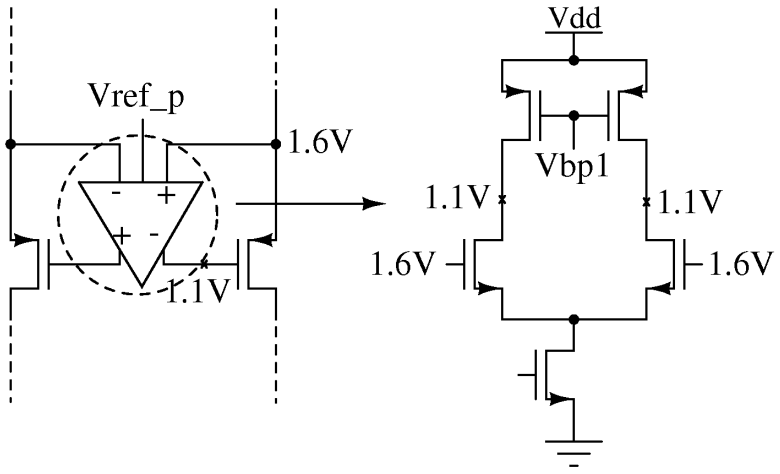


Figure 4.10: Quiescent voltages on the p-side

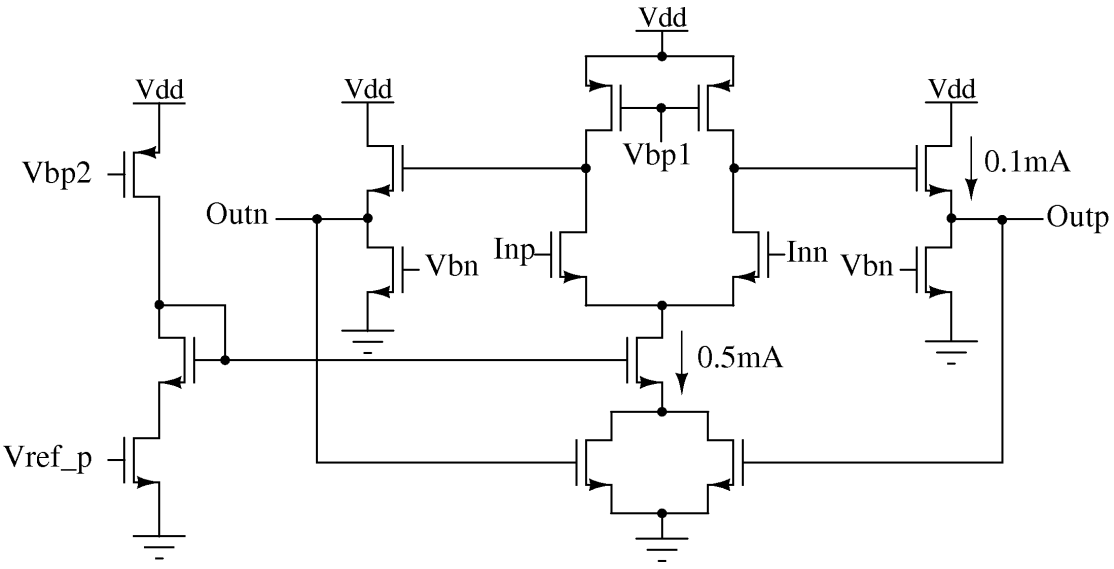


Figure 4.11: P-side gain boosting amplifier

4.4.4 Comparator

Comparator used in the sub-adc is shown in Figs. 4.12 and 4.13 [26]. A coupling capacitance of 25fF is chosen to sample the references. In $\phi 2$ the references are sampled onto the capacitors. In $\phi 1$, the capacitors are placed in series between the input signal and the input of the comparator. The first stage of latch comprised of M1 & M2 acts as a preamp, tracking the input during $\phi 1$, building a differential current in the branches. The latch is reset during this phase with its nodes pulled to Vdd using M5 and M6. M7 helps to reduce the mismatch in the latch during reset phase. At the end of $\phi 1$ the preamp is turned off and the latch turned on. The output of latch is valid only for half of the clock cycle. To make it available for the entire clock cycle, a SR latch follows the comparator. It also helps to minimize the meta-stability of the whole block. The main purpose of the preamp in the comparator is to prevent kickback from the latch to the input. No offset cancellation scheme has been used as a 1.5-bit per stage architecture is chosen and the offset tolerance is high.

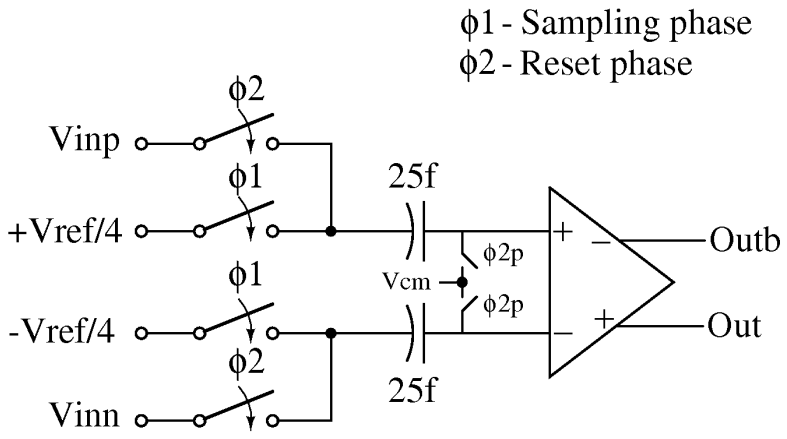


Figure 4.12: Comparator

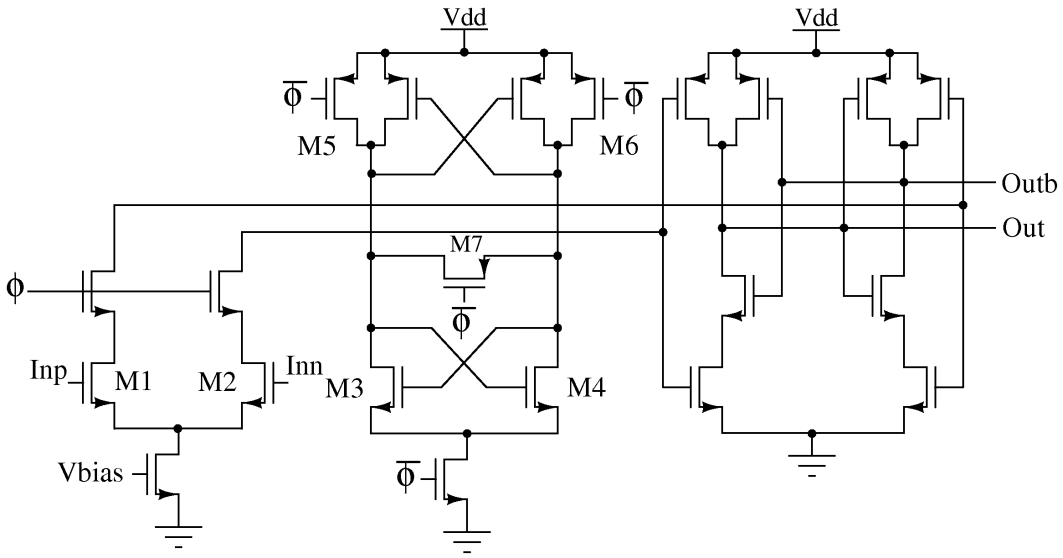


Figure 4.13: Latch used in comparator

4.4.5 Clock generator

A distributed clock generator is used as shown in Fig. 4.7. In 0.18μm process the inherent capacitance of the buffer can get comparable to the load capacitance thus limiting the size of the buffer that can be used. To maintain 100ps rise and fall time, the clock generator is split to make sure that the load driven is small enough to maintain the clock skews. The non-overlap time is chosen to be 200ps at 80MHz.

4.5 Experimental Results

The prototype ADC was fabricated in a 0.18μm CMOS process. The die photograph is shown in Fig. 4.14. The active die area is 1.2mm x 1.8mm. The total power consumption is 36mW at 1.8V supply and 80-MHz sampling frequency. The analog portion consumes 24mW. The measured DNL and INL are -0.92/1.3 LSB and -3.11/3.06 LSB, as shown in Fig. 4.15.

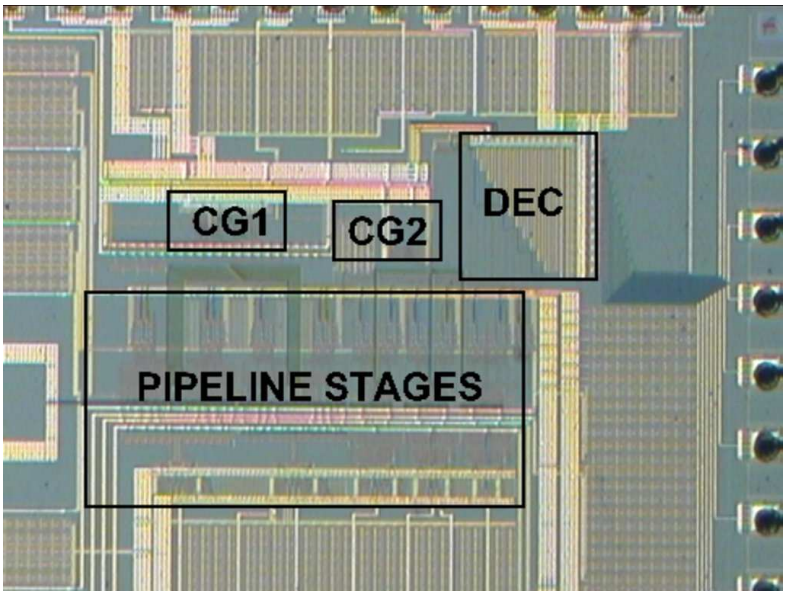


Figure 4.14: Die photograph

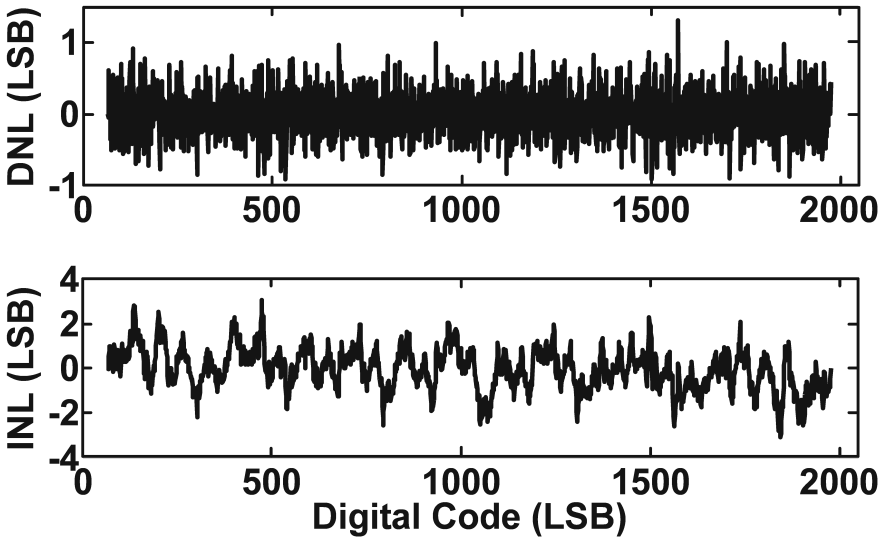


Figure 4.15: DNL and INL plots

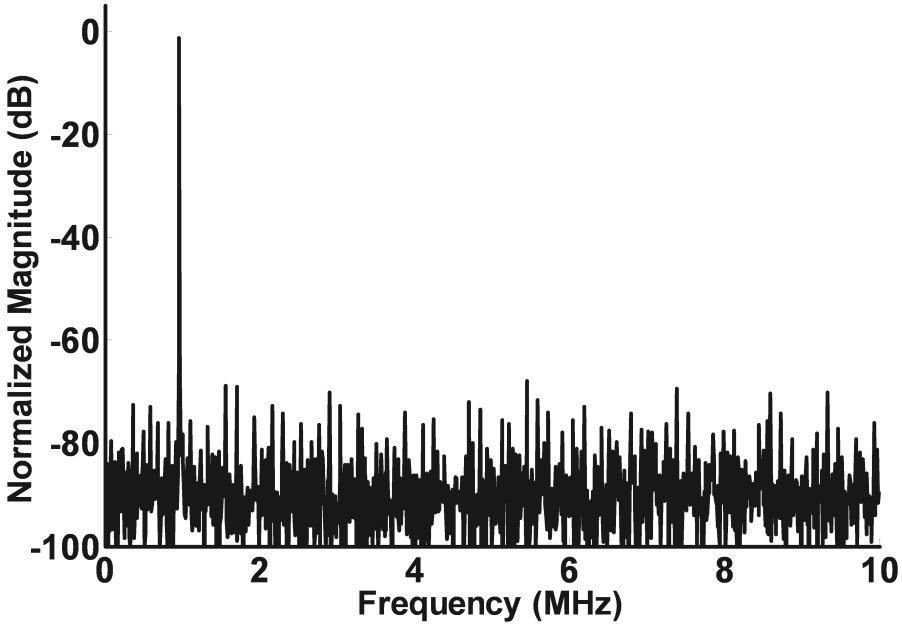


Figure 4.16: Measured output spectrum at 80MS/s

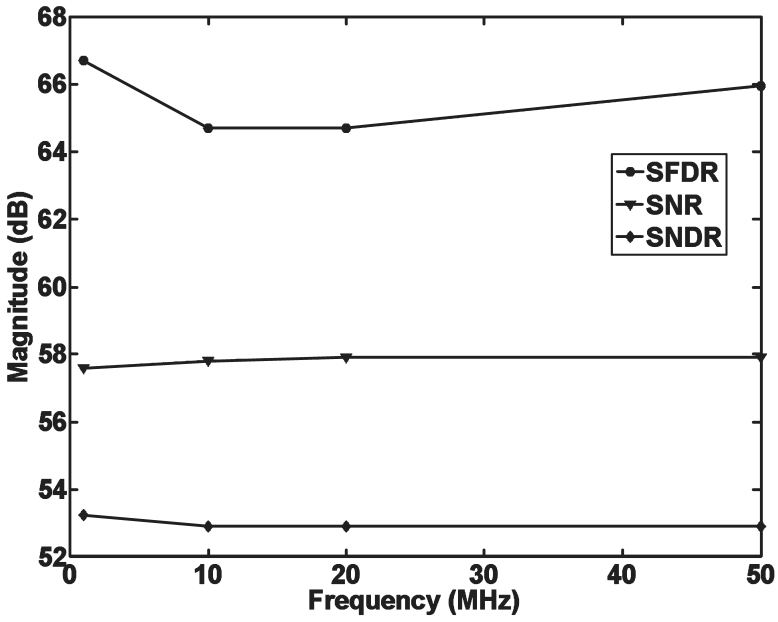


Figure 4.17: Measured dynamic performance versus input signal frequency

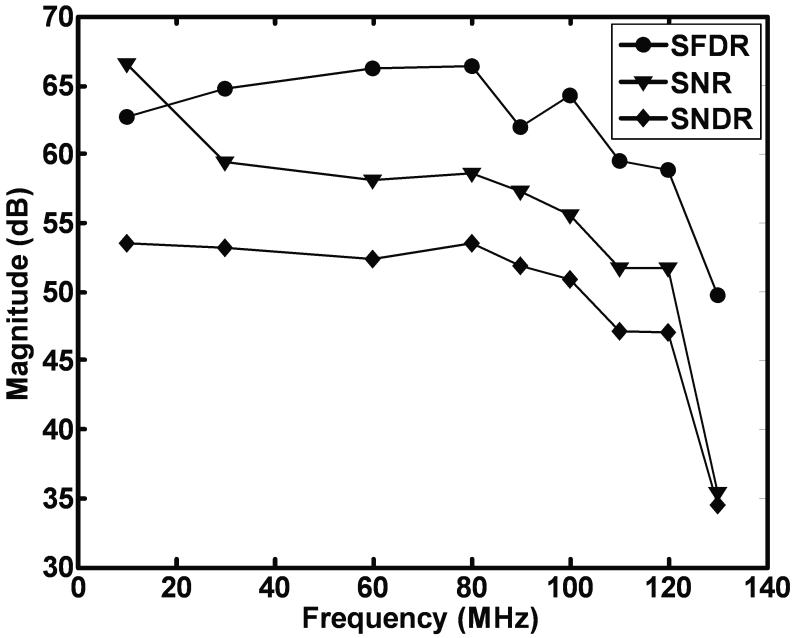


Figure 4.18: Measured dynamic performance versus conversion rate

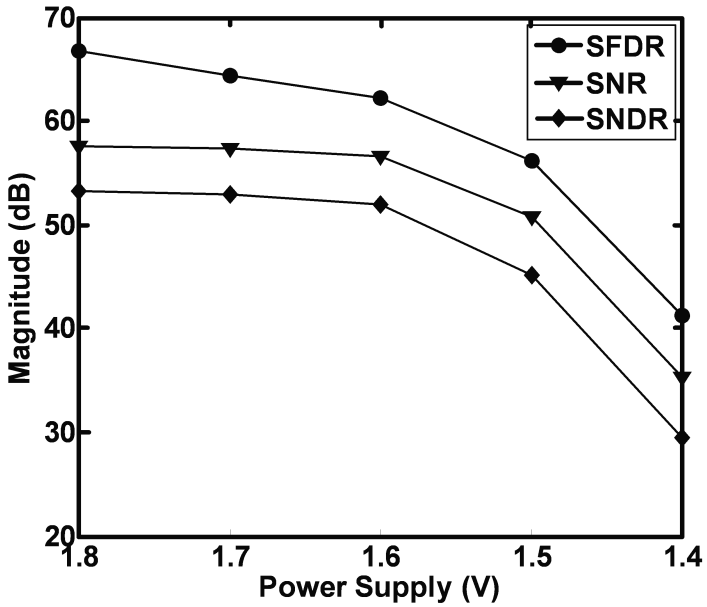


Figure 4.19: Measured dynamic performance versus power supply

Supply voltage	1.8V
Technology	0.18μm CMOS
Resolution	11 bits
Conversion rate	80MS/s
Active area	$2.2mm^2$
Power dissipation	36mW
DNL	-0.92/1.3 LSB
INL	-3.11/3.06 LSB
SFDR (50MHz input)	66.7 dB
SNDR (50MHz input)	53.2 dB

Table 4.1: Performance Summary

With 1MHz input at 80MS/s, the measured SFDR, SNR, and SNDR are 66.7 dB, 57.6 dB, and 53.2 dB, respectively (see Fig. 4.16). The digital output of the ADC is decimated (downsampled) by 4 on chip for testing purposes. Fig. 4.17 shows the dynamic performance versus input frequency at 80MS/s. The measured SFDR, SNR, and SNDR are 66 dB, 58 dB, and 53 dB, respectively over the whole input range (1MHz to 50MHz). Fig. 4.18 shows the dynamic performance versus conversion clock rate with 1MHz input signal. Fig. 4.19 shows the dynamic performance versus power supply with 1-MHz input signal. The ADC works well down to 1.6V. The performance has been summarized in Table 4.1.

4.6 Conclusions

Capacitor sharing technique significantly reduces the effective load capacitance, thereby reducing the power consumption of an opamp. It is found to be a suitable partner for opamp sharing. A new method to cancel the effect of signal-dependent charge kick-back in the absence of sample and hold was also presented.

Chapter 5 . RAIL TO RAIL INPUT PIPELINED ADC WITH ASYNCHRONOUS SAR BACKEND

In this chapter two low power design techniques for high speed pipelined ADCs are described. The proposed new rail to rail input swing MDAC stage takes advantage of the full swing available at the input to resolve a bit. The resolved bit and the sampled input value are used by the new MDAC to generate the equivalent of second stage residue thus saving an opamp. This elimination of an opamp at the input stage gives huge power savings.

Recent trends have shown that regular SAR ADCs can be modified to operate asynchronously achieving high speed (>100MSPS) at medium resolution (<8bits) with extremely low power [10–12]. But to achieve resolution greater than 9 bits, a pipeline ADC is the optimum choice. Using these two observations, a new hybrid architecture has been developed. The first 5 bits are resolved using MDAC stages of a pipeline and the last 5 bits are resolved using an asynchronous SAR backend. A 10-bit, 125 MSPS ADC is designed in 90nm CMOS process and simulation results are presented showing the efficacy of the scheme. Active die area occupied is $0.052mm^2$ showing huge area savings of this architecture.

5.1 Introduction

Pipeline ADCs have become the choice in many communication systems. Owing to their mobile applications, the components are expected to burn as little power as possible to maximize battery life. ADC being one of the power hungry blocks in

the signal chain has become the interest of research. Typical resolution required by many communication systems is ∼10-bits with a signal bandwidth of 20-40MHz at a sampling rate of about 100MSPS for which pipeline is the best suited architecture. Apart from power reduction, area reduction is also of utmost interest to keep the cost low.

The input swing that can be taken in by the ADC is determined by the opamp's linear range which directly determines the power consumed. Large swing facilitates use of smaller capacitors thereby minimizing power. Very few reported ADCs use the full swing available at the input [8, 9].

In a pipeline ADC, capacitors dominantly decide the power and hence area required. Large capacitors require large transistors to drive them hence increasing area. The regular pipeline ADC structure doesn't benefit from the process scaling. Capacitor size still remains the same because of kT/C noise limitation. On the other hand there are ADC architectures like SAR which take complete advantage of scaling both in terms of speed and area.

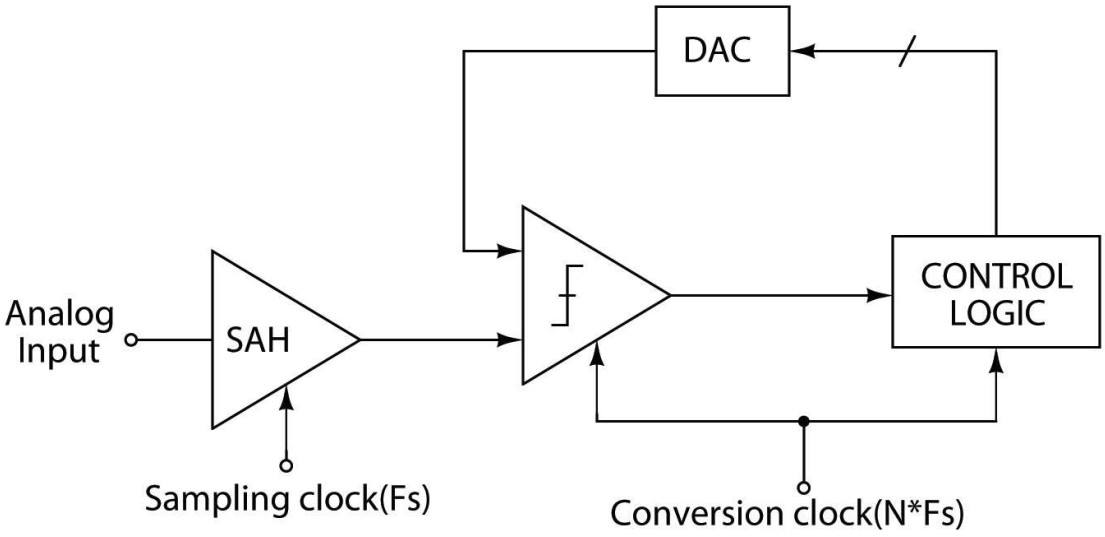


Figure 5.1: Block diagram of a typical SAR ADC

The block diagram of a typical SAR ADC is shown in Fig. 5.1. Accuracy and speed are important specifications of an ADC. In a SAR, the accuracy is limited by component mismatch in the DAC. This is unrelated to the reduction in transistors output impedance that is an effect of scaling which limits accuracy in other structures that require higher transistor gain. Scaling increases speed and a SAR ADC benefits from it as half of its critical path is constituted by digital gates. Traditionally SAR ADCs have been used at low speed and medium resolution. But a modification of the regular structure has been reported where the conversion clock is replaced by the clock signal produced internally as shown in Fig. 5.2. The new asynchronous architecture is very promising for high speed operation (∼500MSPS) and medium resolution.

The above observations are used to propose a new pipeline ADC architecture that suits well for deep sub-micron processes. The MSBs are resolved using pipeline structure whereas the LSBs are resolved using SAR. The ADC takes in the full swing of 2Vdd getting huge power benefits from it. Apart from burning very little power, the backend SAR occupies tiny area.

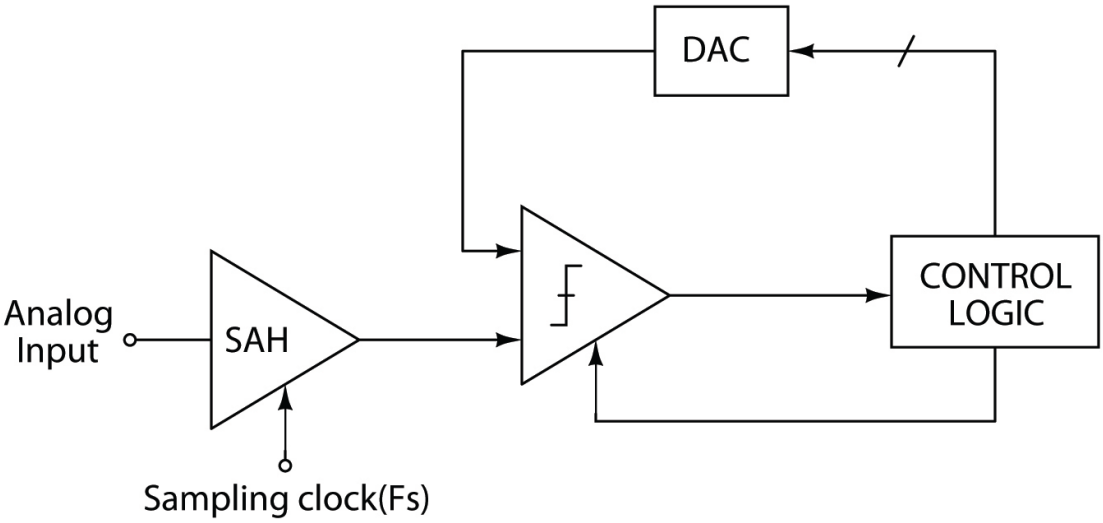


Figure 5.2: Block diagram of an asynchronous SAR ADC

5.2 Rail-to-rail input swing MDAC

Fig. 5.3(a) depicts the allowed swing at the input and output of first stage opamp. The input can swing rail to rail resulting in a differential swing of 2Vdd with ESD setting the limits. In the case of output swing, the limit is set by the opamp linear range. Speed and power benefits often make us choose the telescopic cascode opamp for the MDAC. To get reasonable gain, a Vdsat of about 100mV is optimum in low voltage designs. With five transistors stacked up between the rails, the head room lost to keep the transistors in saturation is (=5×100mV) 500mV. Allowing another 100mV margin, the allowable single ended swing in a 1.2V supply is (=1.2V-0.6V) 0.6V which makes the differential swing 1.2V (Vdd).

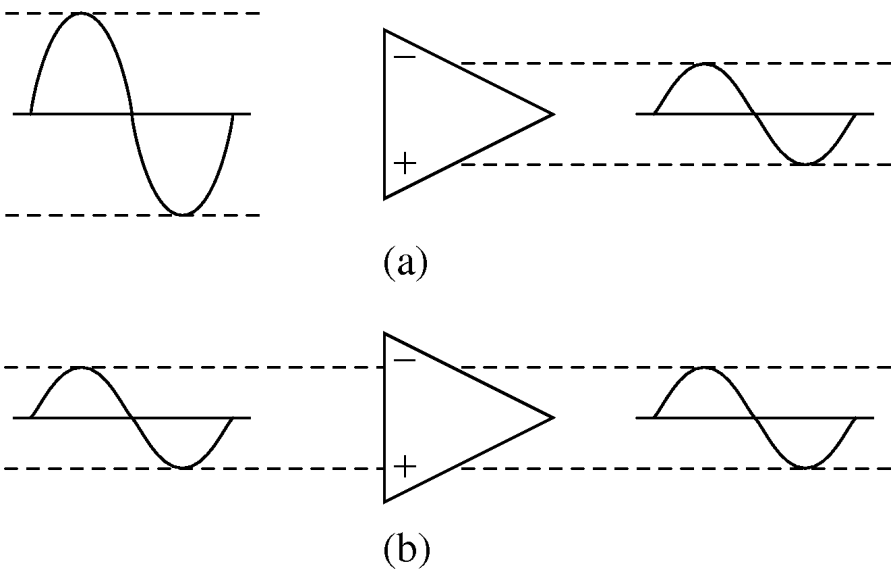


Figure 5.3: (a) Maximum swing possible at input and output of opamp (b) Restricted swing at input to match output

In regular implementations because of the lower swing limits at the output, the input swing is also restricted to be equal to that of output as shown in Fig. 5.3(b). This is because of the fact that in a regular MDAC stage both of them have to be the same. In a 1.5-bit MDAC the residue is calculated by amplifying the sampled

input value (Vin) by 2 and then subtracting the appropriate reference as shown in Eqn. 5.2. This amplification operation needs an opamp.

$$\begin{aligned} Vres &= 2Vin + Vref; \quad if \quad D = 00 \\ &= 2Vin; \quad if \quad D = 01 \\ &= 2Vin - Vref; \quad if \quad D = 10 \end{aligned} \tag{5.1}$$

Observing the allowable swing numbers of 2Vdd at the input and Vdd at the output show that they are in a ratio of 2:1. First two MDAC stages of a pipeline using 1.5-bit per stage architecture are shown in Fig. 5.4. The residue voltage at the output of each MDAC is marked in the figure. The second stage residue in terms of the input (Vin) is given by Eqn. 5.2.

$$V_{res2} = 4Vin \pm 2.D1.Vref \pm D2.Vref \tag{5.2}$$

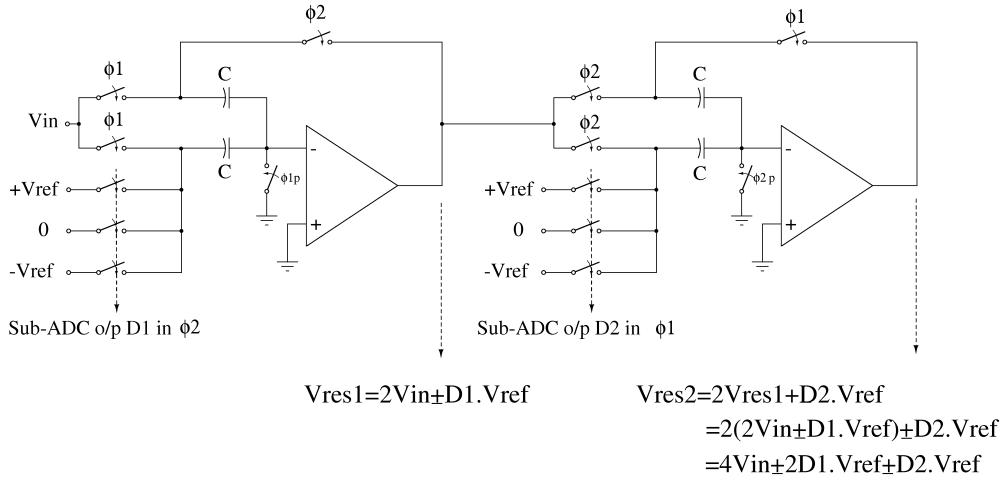


Figure 5.4: First two stages of a pipeline ADC

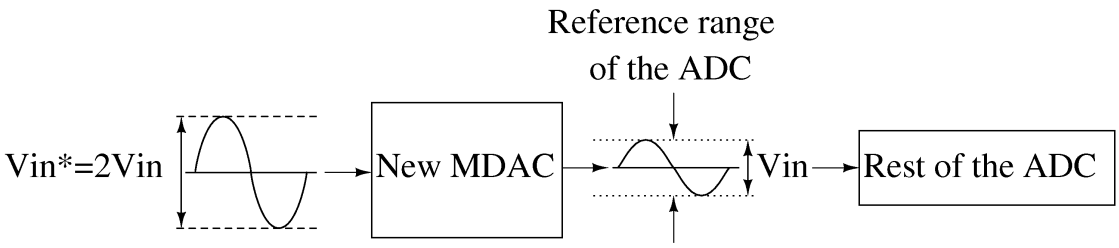


Figure 5.5: Illustration of different swing at the input

Now let us assume that instead of fixing the input swing to match the output swing as is done traditionally, we allow an input swing that is twice that of the output swing. We call the new input swing Vin* and the output swing Vin where Vin*=2Vin as shown in Fig. 5.5. Replacing 2Vin by Vin* in Eqn. 5.2 gives Eqn. 5.3.

$$V_{res2} = 2Vin^{*} \pm 2.D1.Vref \pm D2.Vref \tag{5.3}$$

The above equation can be inferred in the following way. If we sample Vin* (=2Vin) and some how find out D1 and D2 from it, then the second stage residue can be calculated in one step using one MDAC. Fig. 5.6 shows this operation in the new MDAC. Input Vin* (=2Vin) is sampled on to C1 and C2 during $\phi 1$. During this same time, C3 and C4 remain idle. All the four capacitors C1, C2, C3 & C4 are equal sized. In the non-overlap time between $\phi 1$ and $\phi 2$, D1 and D2 which are the digital codes of regular first and second stage MDACs are evaluated. This evaluation operation will be explained later. For now, assuming that we have D1 and D2 by the beginning of $\phi 2$, the residue is calculated using one opamp thus saving a whole MDAC stage. It should be noted that the entire ADC including the first stage modified MDAC operates on one set of references. Significance of this new MDAC becomes clearer once it is known how D1 and D2 are calculated. The explanation follows.

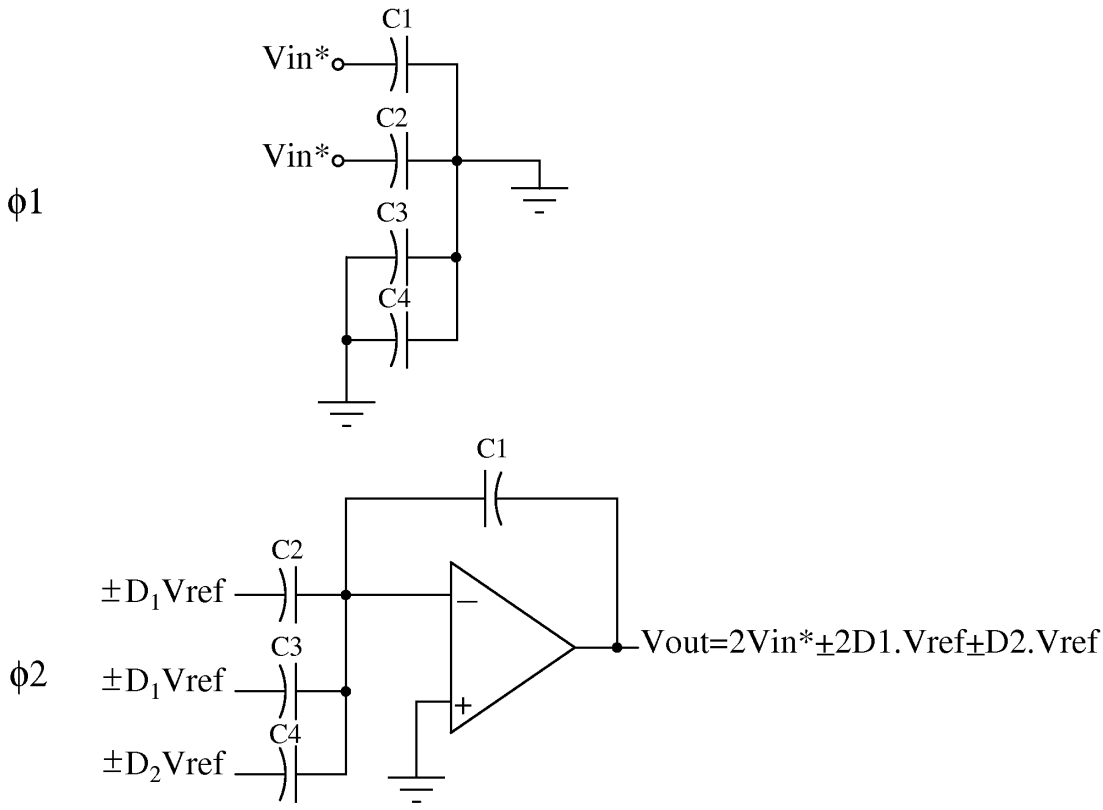


Figure 5.6: Modified MDAC

In a regular 1.5-bit stage, the sampled input Vin is compared to ±Vref/4 and the resultant output code is D1. In the new case as the sampled input is 2Vin (Vin*), it is compared to ±Vref/2 (±Vref/4×2) to get D1. It should be noted that 2Vin being compared to ±Vref/2 is equivalent to Vin being compared to ±Vref/4. Once D1 is obtained, in a regular architecture it is used to evaluate the residue as shown in Fig. 5.4. This residue evaluation requires an opamp and is done to calculate D2. Alternately, this residue can also be obtained as shown in Fig. 5.7. Cc is the comparator sampling capacitor. After calculating D1, the bottom plate of capacitor Cc is connected to the reference voltage ±Vref or 0 basing on D1. The voltage at the top plate now is 2Vin±D1.Vref which is same as the first stage residue voltage. This voltage is now compared to ±Vref/4 to give D2. This passive

evaluation of first stage residue will not be accurate. But as we are dealing with 1.5-bit stage architecture, the redundancy levels are high enough to tolerate any possible error due to parasitic capacitors. Once D1 and D2 are obtained, the equivalent residue of second stage can be calculated using one MDAC as shown in Fig. 5.6. The whole operation is shown in Fig. 5.8. Thus at the end of one clock cycle, we have obtained D1 and D2 and the equivalent of second stage residue using one MDAC. This is facilitated by the higher input swing possible that is used here.

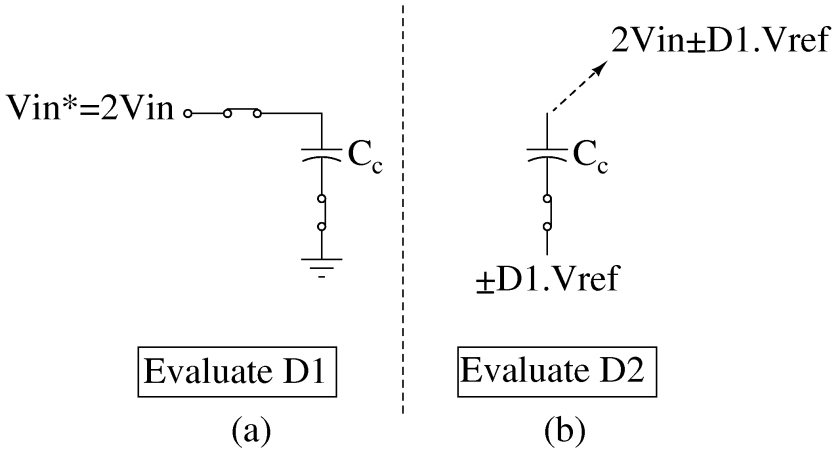


Figure 5.7: Passive residue generation scheme

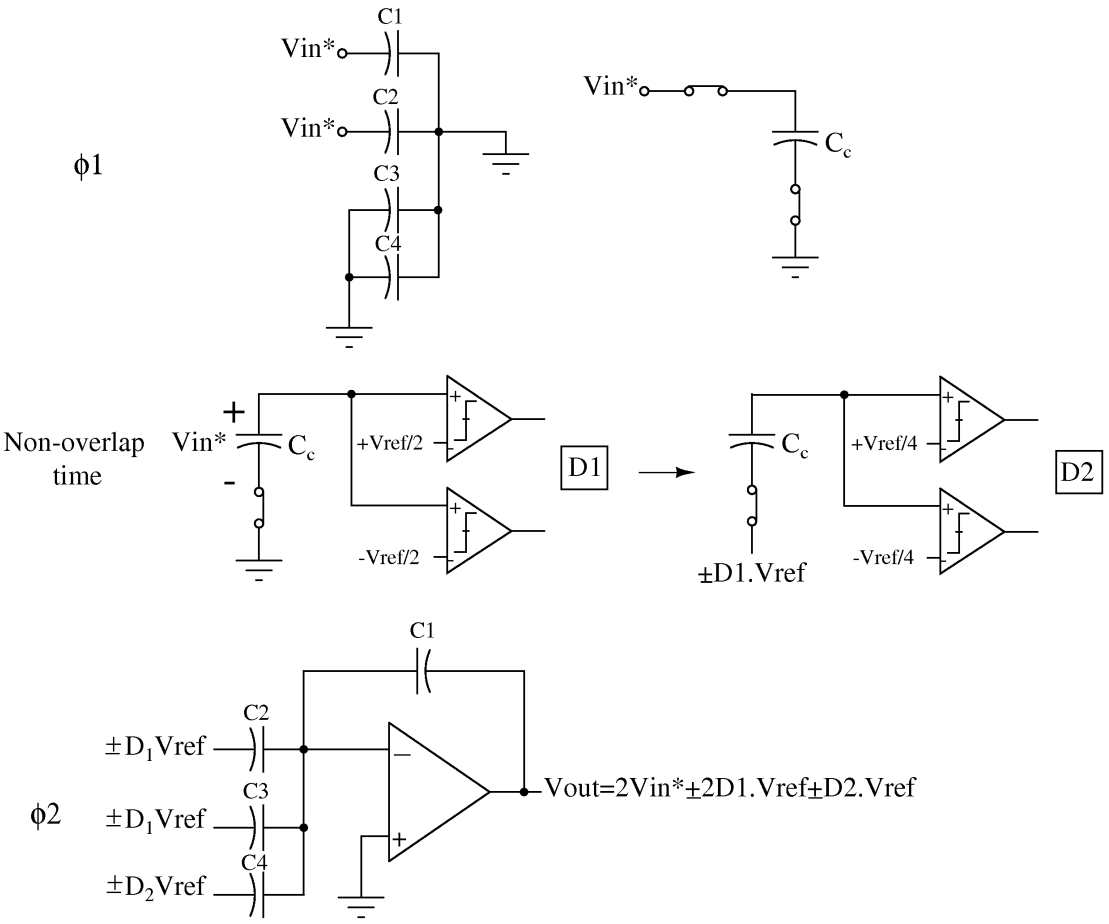


Figure 5.8: The new first stage

5.2.1 Comparison to 2.5-bit per stage MDAC

A regular 2.5-bit per stage MDAC is shown in Fig. 5.9. The input Vin is sampled onto all the four capacitors in $\phi 1$. During the non-overlap time, the digital code corresponding to the transfer curve shown is calculated. In $\phi 2$, one capacitor is flipped over where as the other three are connected to references. Though structurally the newly proposed MDAC looks similar to the 2.5-bit stage and except for the same feedback factor that both of them have, there is no other similarity between them.

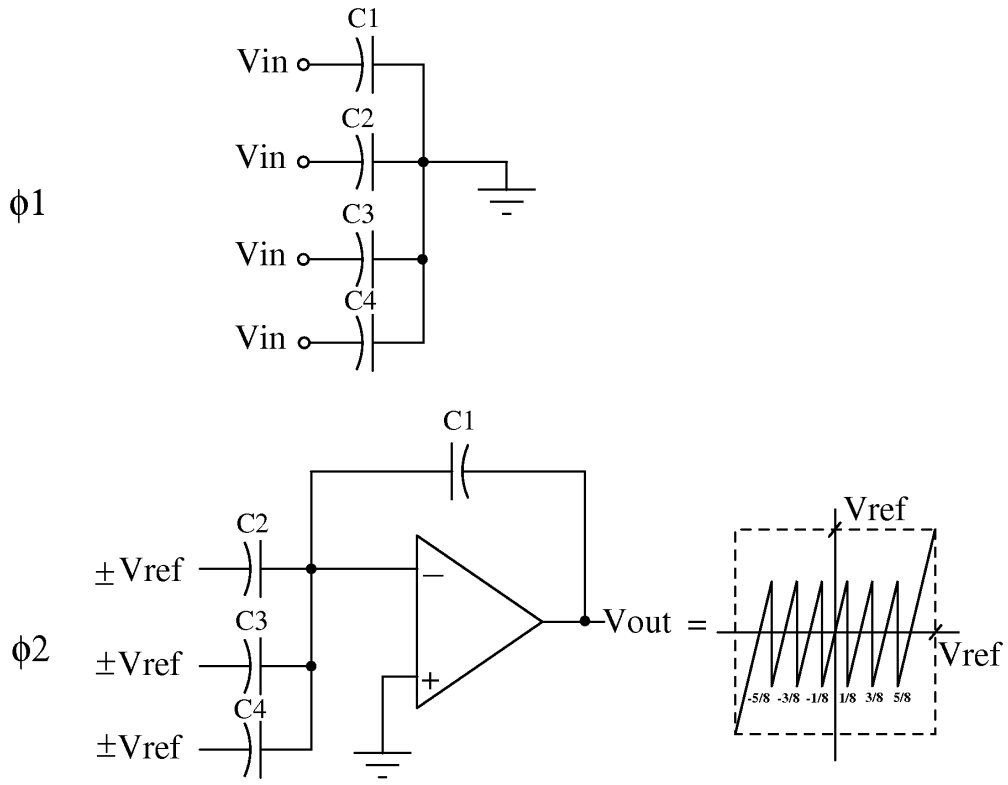


Figure 5.9: A 2.5-bit MDAC stage

To begin with, let us consider the number of comparators in the sub-ADC. In the newly proposed structure there are four comparators that are either placed at ±Vref/2 or ±Vref/4. In a 2.5-bit stage there are seven comparators and they are placed at the references shown in transfer curve. The redundancy margin in a 2.5-bit stage is ±Vref/8 whereas in the new MDAC, the redundancy margin is still equal to that of a 1.5-bit stage of ±Vref/4. Having the same redundancy range of that of a 1.5-bit stage is important in low voltage processes where threshold margins available are small. Behavioral simulations show that the matching requirements of the capacitors in the new MDAC are as same as that of a 2.5-bit stage.

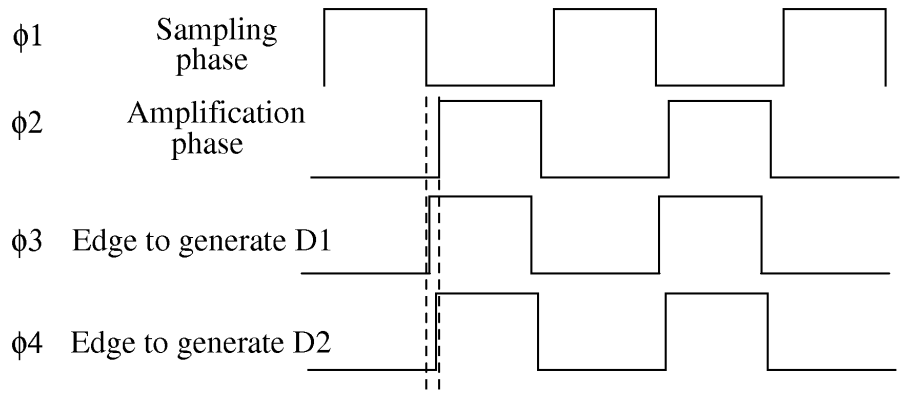


Figure 5.10: Desired clock phases

5.2.2 Asynchronous sub-ADC

As mentioned before, D1 and D2 have to be resolved during the non-overlap time. A timing diagram indicating the clock phases required is shown in Fig. 5.10. The gap between $\phi 3$ and $\phi 4$ is determined by the comparator resolution time. The clock $\phi 4$ is an extra phase that has to be generated just for the purpose of D2 calculation. Both in terms of timing and power, having a dedicated $\phi 4$ phase is not optimal. Before setting on to resolve D2, it has to be made sure that D1 is resolved. Letting a safe margin for $\phi 4$ means eating away into the amplification time. Moreover generating a high speed clock phase for use in one place is not power optimal. A workaround for this is to make the sub-ADC asynchronous.

Fig. 5.11 shows the modified sub-ADC. The problem of timing is solved using asynchronous clocking. $\phi 3$ is used to clock the comparators that resolve D1. Once D1 has been found, the transition information of D1 is used to produce an edge clk_D2 that clocks the comparators that resolve D2. The edge generation scheme is also shown in the figure. The output of comparators that resolve D1 is differential. When $\phi 3$ is low, the comparator is reset and both the output nodes of the comparator are low. These outputs go to a XOR gate giving an output of 0.

When $\phi 3$ goes high clocking the comparators, D1 is resolved and the outputs of the comparator change state. One output goes high and the other remains low. This input to the XOR gate gives an output of 1 thus producing an edge that can clock the D2 comparators. The asynchronous fashion in which D2 is generated ensures that D2 is resolved well after D1 has been resolved. In terms of power, the clock generation circuitry has been replaced by a single XOR gate that does the job efficiently.

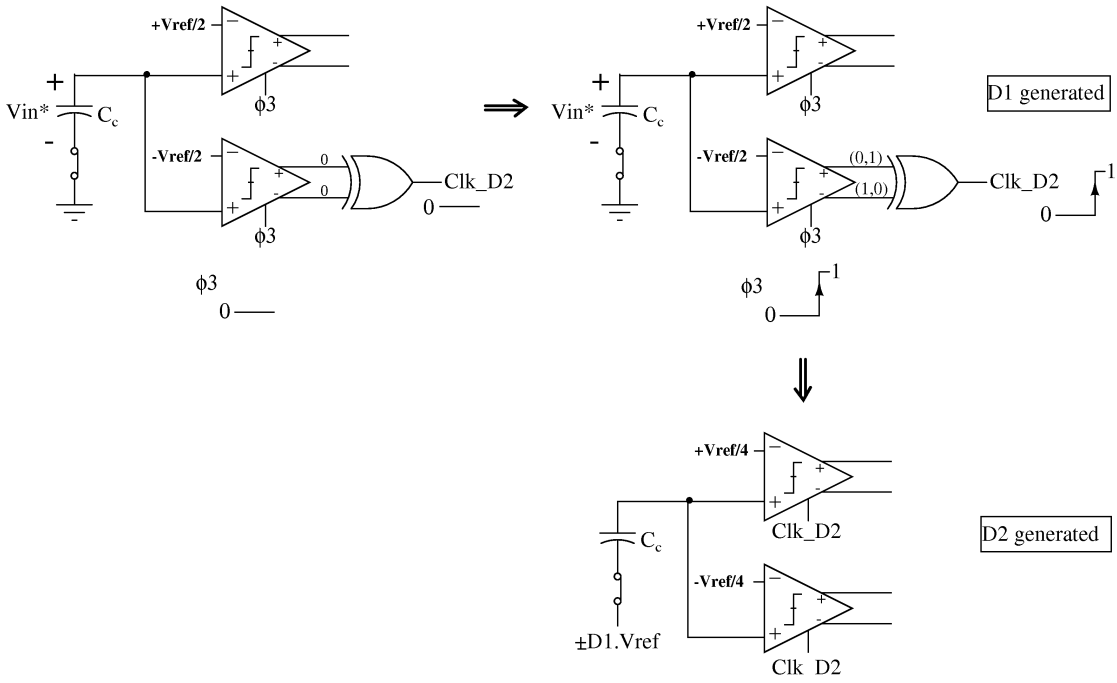


Figure 5.11: Asynchronous sub-ADC

5.3 SAR ADC

Successive approximation register (SAR) is an interesting structure in terms of the way it resolves the final digital code. In contrast to the flash based structures, a SAR uses binary search operation to arrive at the final digital code. Fig. 5.1 shows the block diagram of a basic SAR ADC. The main components are the comparator and DAC. Comparator is clocked at N times the conversion rate where N is the number of bits to be resolved.

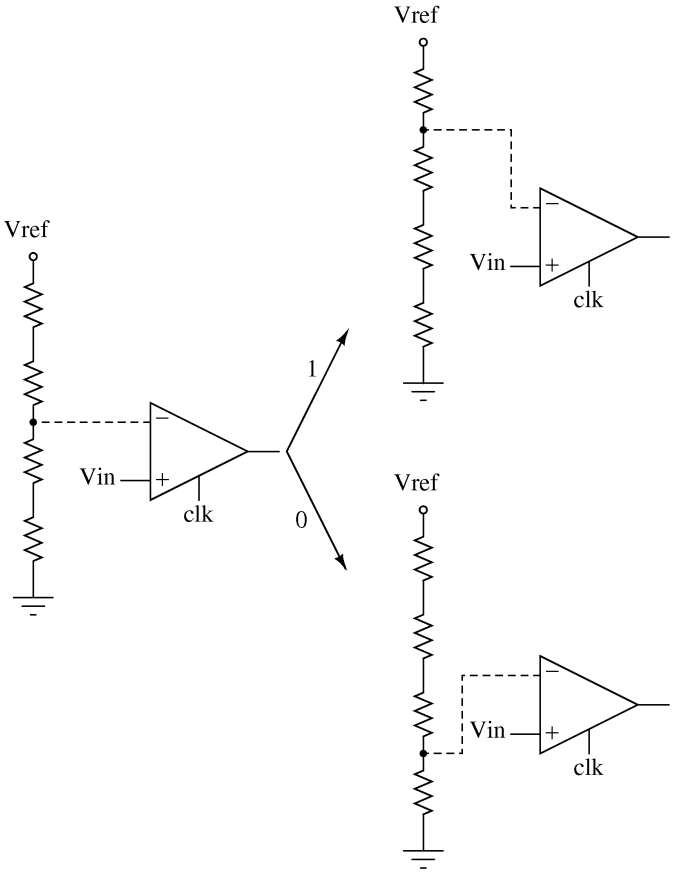


Figure 5.12: A 2-bit SAR ADC

Input signal is sampled by the SAH and held for the comparator for the whole conversion period. The DAC provides reference to the comparator. Fig. 5.12 shows a 2-bit SAR ADC operation. The conversion process begins by comparator

comparing the input to mid reference level Vref/2 provided by the DAC at the start. In this example, the DAC is a resistor ladder. If the output of the comparator is a 0, then the DAC switches the reference to Vref/4 which is the mid level reference of the bottom half. If the output is a 1, then the new reference value would be 3Vref/4. Likewise, the decision of the comparator is used to determine the next reference level with each time the reference getting closer to the input than before in a binary search fashion. Fig. 5.13 shows some example patterns in which the reference can move in a 3-bit SAR ADC for different inputs. An N bit ADC needs N decisions to be made by the comparator each with a different reference. The bits are stored in a register and given out at the end of conversion cycle. Offset of the comparator comes out as the ADC offset. So unless there is a specification on the maximum allowable offset, offset cancellation schemes are not used.

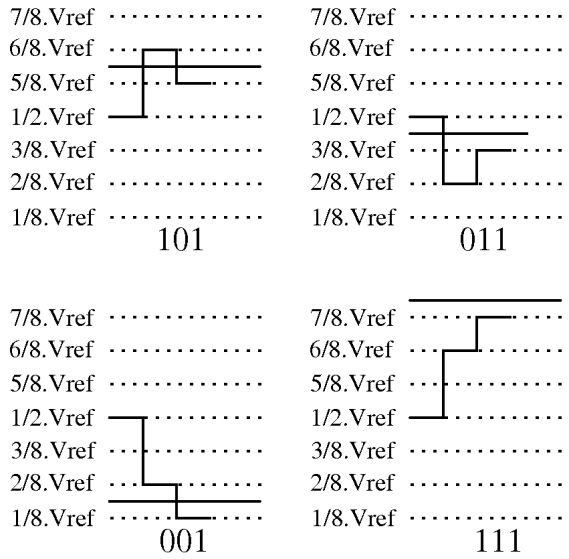


Figure 5.13: Patterns in which the reference can move

The main disadvantage of a SAR is its requirement of a high frequency clock. A 10-bit ADC operating at 100MSPS would require 1GHz clock for the comparator. Generating and propagating such clock frequency is a power intensive operation

[10]. This has traditionally limited SAR to low speed applications not exceeding 10MHz conversion rate. But a recent improvement [10–12] in the SAR architecture is making it possible to get high conversion rate at low power.

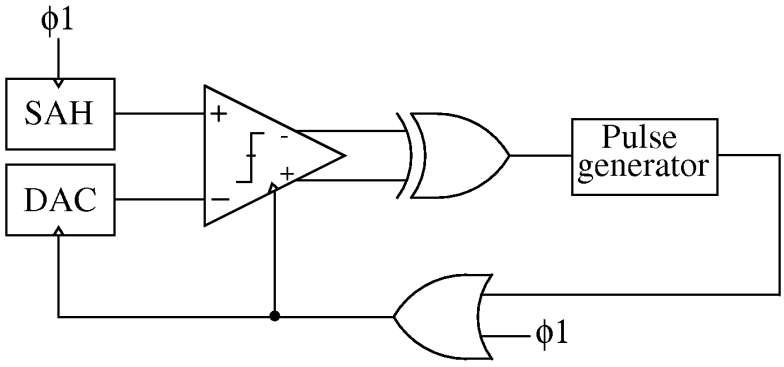


Figure 5.14: Asynchronous SAR ADC

Block diagram of the new architecture called the Asynchronous SAR (ASAR) is shown in Fig. 5.2. A possible implementation is shown in Fig. 5.14. It works as follows. When clock is high, the input is sampled by the SAH. When clock goes low, the sampled value is held at the input of the comparator just like in a traditional SAR. The power intensive high frequency clock that is supposed to clock the comparator is gotten rid of here. The clock edge for the first comparison is provided by the conversion clock when it goes from high to low at the end of sampling phase $\phi 1$. This triggers off the comparator thus enabling it make the first decision. The comparator is reset before being triggered off. The output of the comparator goes to a XOR gate. When the comparator is in reset mode, both its outputs are pulled to ground thus making the XOR gate output 0. When triggered off, the outputs of the comparator are no longer the same. One node goes to 0 where as the other goes to 1. This makes the XOR gate change state thus producing a 0 to 1 transition at its output. This edge goes into a pulse generator circuit that produces a pulse at the end of every comparison. This pulse then loops back and

changes the DAC reference, resets and clocks the comparator enabling it make the next comparison which is used by the pulse generator to generate the next pulse and so on. It goes on and on from there asynchronously. The conversion clock acts as a start and stop signal for the asynchronous conversion process. The power overhead for the pulse generator is negligible making ASAR a popular architecture for speeds exceeding 100MSPS and >6-bit resolution.

5.4 Hybrid Architecture

An asynchronous SAR ADC is an efficient implementation for resolution in the range of 5-bits and speed of up to ∼150MSPS. Apart from the power benefits, it also gives tremendous area savings. As seen in its block diagram, the main components are the sample and hold, comparator, DAC and the digital logic. SAH at 5-bit level doesn't necessitate an active structure. A simple CMOS transmission gate followed by a capacitor as shown in Fig. 5.15 acts as a track and hold providing good linearity. So eliminating the SAH, area occupied by other blocks is tiny.

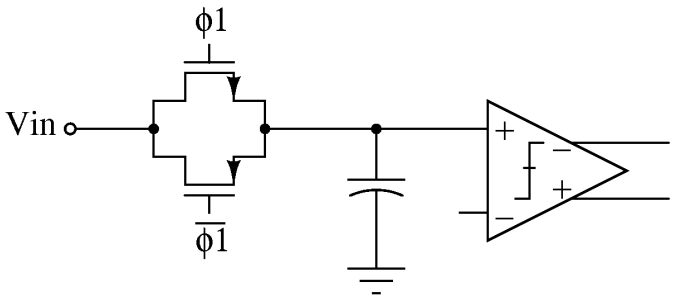


Figure 5.15: Track and hold of a 5-bit ADC

But to achieve resolution beyond 8-bits, pipeline ADC is probably the best structure in terms of speed and power. These observations have led to the new architecture shown in Fig. 5.16. The target is to build a 10-bit, 125MSPS ADC.

The first five bits are resolved using MDAC stages and the last five bits are resolved using an ASAR. The first MDAC is the special MDAC described earlier that takes in full signal swing of 2Vdd. The other MDACs are regular 1.5-bit stages. Opamp is shared between MDACs 1&2 and 3&4. Though there are four MDACs, the number of bits resolved between them is five indicating the extra bit being resolved at the very first MDAC using the available full swing. The residue of the fourth stage MDAC that should be digitized to 5-bits is sampled onto capacitors using the network shown in Fig. 5.15. The capacitor holds the residue for the ASAR that follows. The ASAR replaces three 1.5-bit stages and a 2-bit backend flash thus saving three opamps and the capacitors associated with them. The power consumed in each block is also shown in the figure.

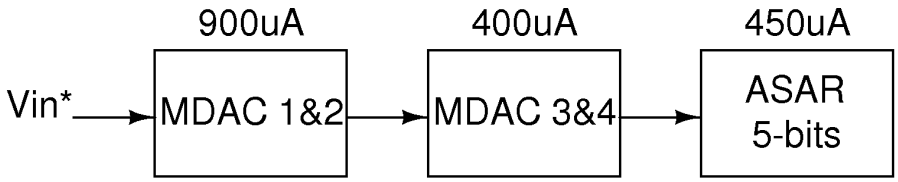


Figure 5.16: Block diagram of the newly proposed ADC

5.5 Circuit Design

5.5.1 Pipeline Stages

5.5.1.1 MDAC

The differential range of the input is $2.4V_{pp,diff}$ and is called Vin* to differentiate it from the swing at the output of the MDAC which is Vin=$1.2V_{pp,diff}$. The reference levels of the ADC are corresponding to Vin. Reference levels Vref+ and Vref- are at 900mV and 300mV making the range $1.2V_{pp,diff}$. In $\phi 1$, the input Vin*(=2Vin)

is sampled onto capacitors C1 & C2 as shown in Fig. 5.6. During this time C3 & C4 are reset. Parallelly the input is also sampled onto the comparator capacitor Cc. This sampled value on Cc is compared to ±Vref/2 (Vref/4×2) by sub-ADC1 giving D1. D1 is then used to generate an approximate residue using passive method. The voltage 2Vin±D1.Vref is compared against ±Vref/4 by sub-ADC2 to give D2. D1 and D2 are used by the MDAC to generate the accurate residue Vres1= 4Vin±2D1.Vref±D2.Vref that is the same as second stage residue. This residue is passed on to the next stage MDAC which is a regular 1.5-bit stage. The important circuit blocks in this chain are capacitors, sampling switch, comparators and opamp.

5.5.1.2 Capacitors

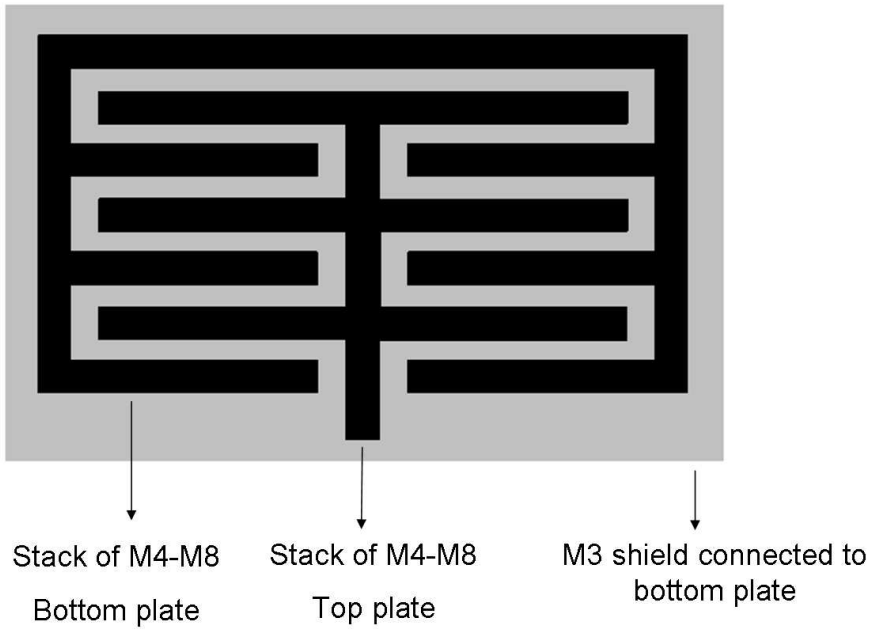


Figure 5.17: Capacitor layout

Capacitor size at 10-bit level is dominantly decided basing on kT/C noise re-

quirement rather than on matching. Matching is assumed to be good to the accuracy required. The signal to noise ratio is given by the Eqn. 5.4.

$$V_{rms}^2 = \frac{kT}{C} + \frac{1}{2^2}\frac{kT}{\alpha^2 C} + \frac{1}{2^4}\frac{kT}{\alpha^3 C} + \frac{1}{2^6}\frac{kT}{\alpha^4 C} \tag{5.4}$$

For a reference level of $1.2V_{pp,diff}$, the unit capacitor size for 60 dB SNR turns out to be 200f with a scaling factor of 0.5. This aggressive scaling has been implemented only till the 3rd stage till the capacitor reaches 50f. kT/C noise applies only till 4th stage as the backend is a SAR ADC.

This process didn't have provision for regular capacitors like poly-poly or metal-insulator-metal. So the capacitors are realized using metal finger based structure as shown in Fig. 5.17. Metals 4-8 are used for the fingers. This structure would have equal top and bottom plate parasitic capacitance. To minimize the top plate parasitic capacitance, a metal 3 shield is placed at the bottom and is tied to the bottom plate node. This helps in two ways. Firstly it increases the capacitor density by converting all the top plate parasitic to capacitance between top and bottom plate. Secondly, it reduces top plate parasitic to less than 1%.

5.5.1.3 Comparator

There are two sub-ADCs in the first stage MDAC as shown in Fig. 5.11. Sub-adc1 that compares the input to ±Vref/2 to generate D1 and sub-ADC2 that compares the passive residue to ±Vref/4 to generate D2. The schematic of the comparator used in these sub-ADCs is shown in Fig. 5.18. The sub-ADCs in rest of the MDAC stages compare the input to ±Vref/4 as in a regular 1.5-bit stage. Instead of generating ±Vref/2 required just by one sub-ADC in the first MDAC, it

is realized using scaled devices. The reference transistors are scaled by factor of 4 compared to the input devices according to the square law model hence effectively comparing the input to ±Vref/2. The comparator operates as described below.

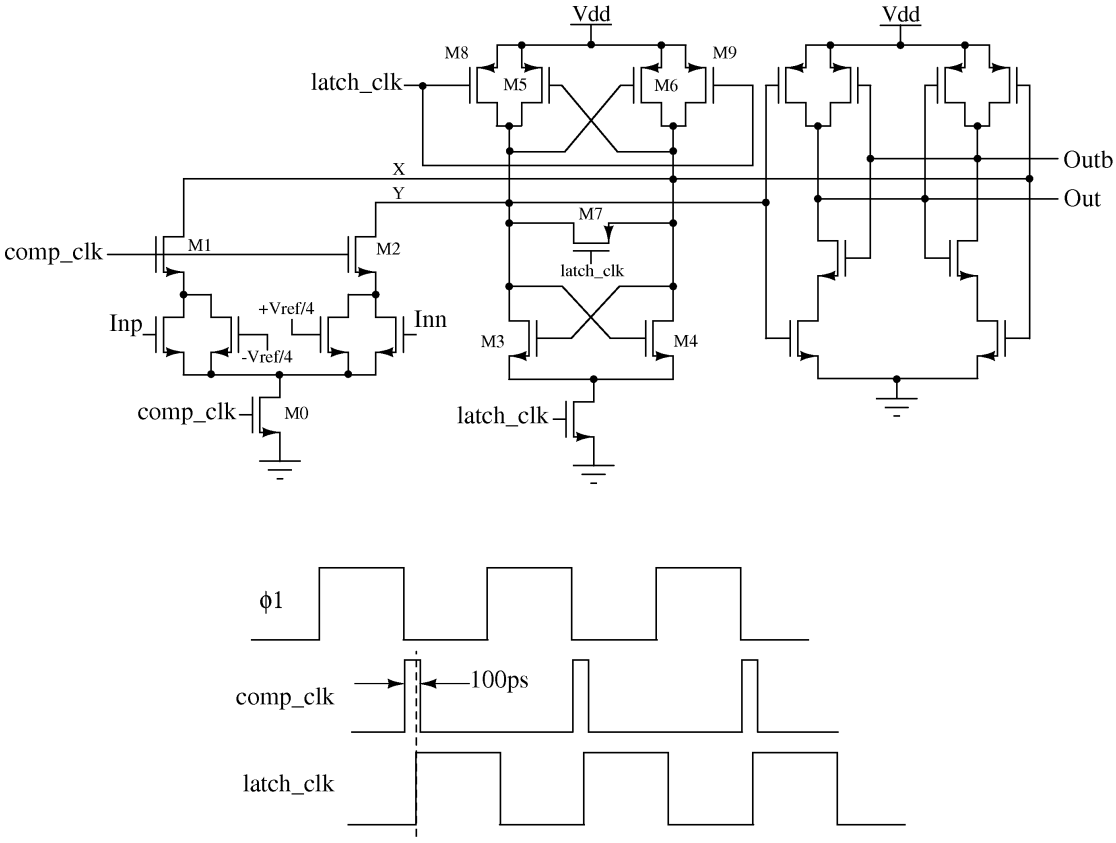


Figure 5.18: Comparator

During $\phi 1$, input is sampled onto the capacitor Cc. As $\phi 1$ goes low, *comp_clk* goes high turning on M0-M2 thereby causing current addition at nodes X & Y. This phase is similar to pre-amplification where the reference is subtracted from the input and the resultant held at the latch's input. *Comp_clk* is high for 100ps giving enough time for the current addition to take place. Just before *comp_clk* goes low, *latch_clk* goes high turning on the latch comprised of devices M3-M6. Nodes X & Y that have differential voltage built up on them by now decide the direction in which the latch trips. *Comp_clk* is taken low right after *latch_clk* goes

high to ensure prevention of kickback. When *latch_clk* is low, the latch is reset by pulling the nodes X & Y to Vdd using switches M8 & M9. M7 helps in mitigating any mismatch in the reset switches. The output of the comparator is valid only for half clock cycle as it is reset during the other phase. To ensure availability of the output for the entire cycle, a SR latch is used following the comparator. The SR latch also helps in reducing the metastability of the comparator.

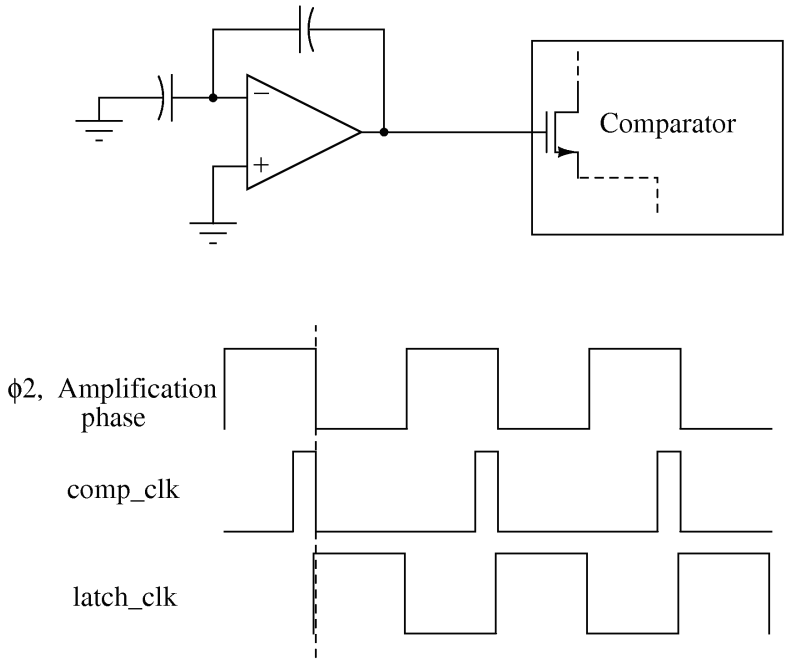


Figure 5.19: Opamp directly driving next stage's comparator input

Though the comparator structure in the sub-ADCs of later stages is the same, there is a slight difference in the way the input signal is dealt with. An illustrative diagram is shown in Fig. 5.19. The comparator input is directly driven by the previous stage MDAC getting rid of the comparator sampling capacitors. This helps in saving power which can be substantial in later stages because of scaling. Conventionally, the sampling capacitor for MDAC stage is scaled down whereas the comparator capacitor size is held constant at a nominal value of 25f usually. With

the type of aggressive scaling that is adopted in the design, this 25f capacitor can become comparable to the MDAC capacitor leading to unnecessary power overhead. The clocking scheme for the new structure is shown in Fig. 5.19. M0 is turned on using *comp_clk* just before the end of amplification phase $\phi 2$ as by then the residue would have settled to considerable accuracy. *Comp_clk* goes low along with $\phi 2$ to ensure that there is no kickback coupled to the input from the latch. The rest of the latch operation is similar to that described before.

5.5.1.4 Opamp

The opamp is the most important block in the ADC. It determines the accuracy and power of the ADC. Hence it is desirable to get high gain and bandwidth with as little power as possible. The capacitor size is determined to be 200f. The first stage MDAC has a feedback factor of 1/4 during amplification phase as shown in Fig. 5.6. The residue of this MDAC is used to resolve 8 bits by the backend ADC as 2 bits would have been resolved by then. For the residue to be 8-bit accurate, the loop gain of the opamp has to be at least 2^9(54 dB). Considering process variation, this is chosen to be 60 dB. With a feedback factor of 1/4, the required opamp gain turns out to be 72 dB. The opamp has to settle to this accuracy in 4ns time as the ADC is intended to be operated at 125MSPS. The intrinsic gain of the transistor gm.ro in this process is found out to be 10. A single stage amplifier is not sufficient to obtain the gain required. Two possibilities were evaluated. One is a two stage amplifier and the other is a telescopic opamp with gain boosting. The later is chosen owing to its high bandwidth with low power. The schematic of the opamp is shown in Fig. 5.20. The main stage burns 900uA giving a gain of 34 dB with a loop UGB of 375MHz. Vdsat of 100mV is chosen as a trade off between signal

swing and gain. Leaving 5.Vdsat for the stacked transistors, the available swing is 0.7V single ended. Allowing for margin, the ADC has been designed to operate at a single ended swing of 0.6V or $1.2V_{pp,diff}$. A switched capacitor common mode feedback loop is used to set the output common mode.

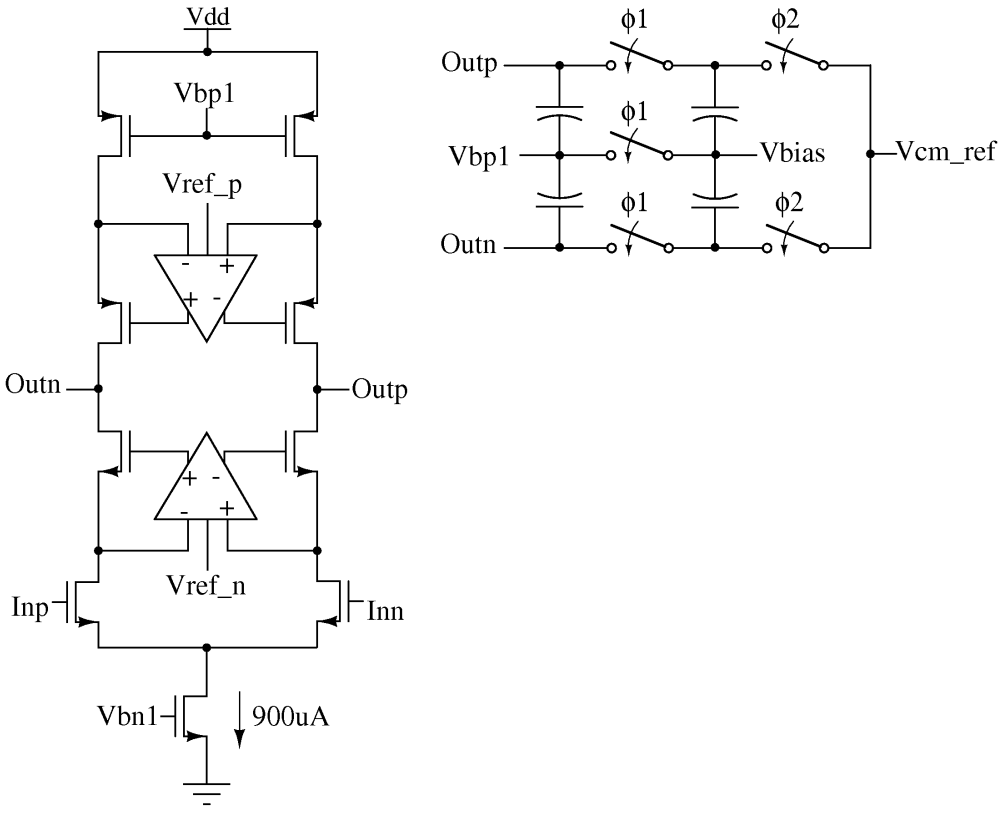


Figure 5.20: First stage opamp

5.5.1.5 Gain boosting amplifiers

The gain required from these amplifiers is 40 dB. With a gm.ro of 10, a cascode structure is required to meet the gain specifications. A differential structure is chosen to minimize power and area. On the n-side, with an input common mode of 0.2V, the optimum structure would be a folded cascode amplifier with p-input,

as shown in Fig. 5.21. On the p-side, with an input common mode of 1.1V, the optimum structure would be a folded cascode amplifier with n-input, as shown in Fig. 5.22. The unity gain bandwidth of the main amplifier is 375MHz. To ensure stability, the UGB of the gain boosting amplifiers should be greater than that of the main amplifier [19]. It is chosen to be 500MHz. Gain boosting amplifiers don't have to slew as their input nodes are always held constant by the gain boosting loop. This means that the current in the branches of the folded cascode amplifier can be made tiny enhancing output impedance. In the design, current through the tail current source is chosen basing on the Gm required. The current in the branches is nominally kept at 10uA. This approach made it possible to design the boosting amplifiers with about 20% of the overall opamp power. A four transistor type CMFB loop shown in Fig. 5.23 is used to set the output common mode in both the amplifiers.

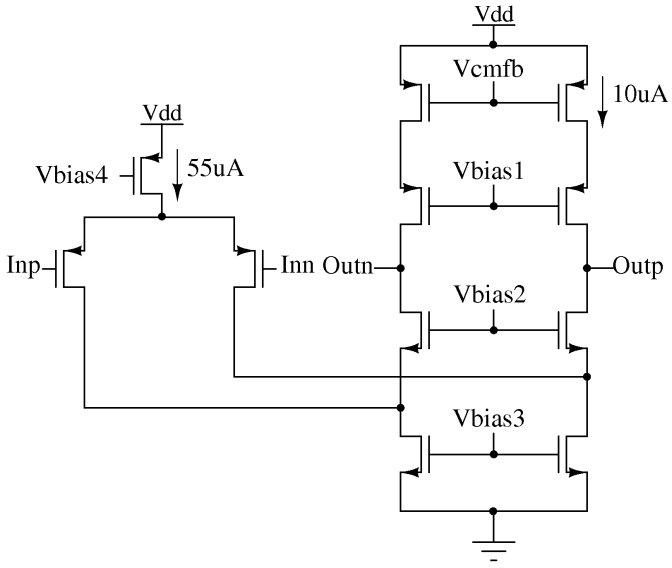


Figure 5.21: N-side gain boosting amplifier

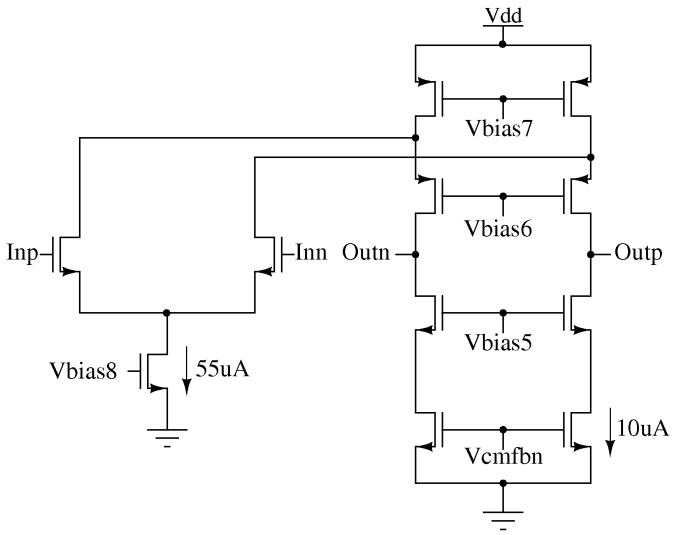


Figure 5.22: P-side gain boosting amplifier

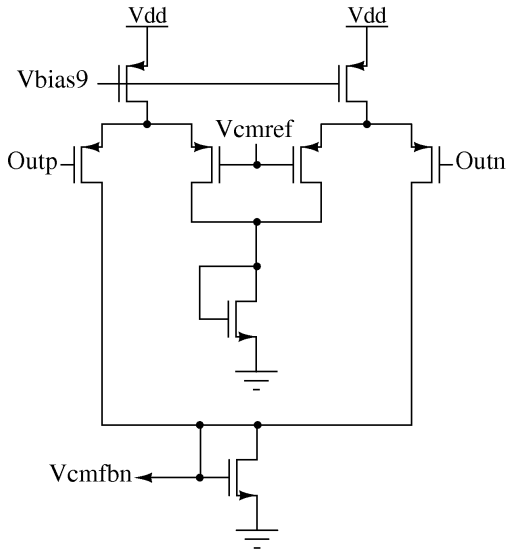


Figure 5.23: CMFB amplifier

5.5.2 Asynchronous SAR ADC

5.5.2.1 Comparator

The most important components of a SAR ADC are comparator and DAC. Single ended implementation of a SAR is much simpler compared to differential structure. One input of the comparator is the sampled input signal that is held constant whereas the other is the reference signal that moves. Implementation becomes difficult for differential structures. The comparator now has to compare a differential input to a differential reference. Possible implementations are shown in Figs. 5.24 & 5.25. It is assumed that the binary capacitor weighted structures are not feasible here as this SAR is the backend of a pipeline ADC and driving such huge capacitances is a power intensive operation.

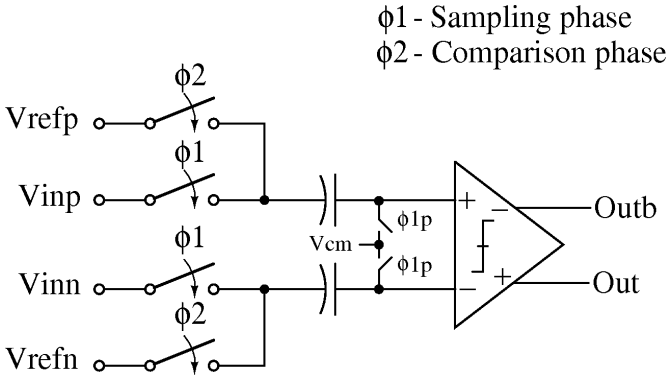


Figure 5.24: Comparator with capacitively coupled inputs

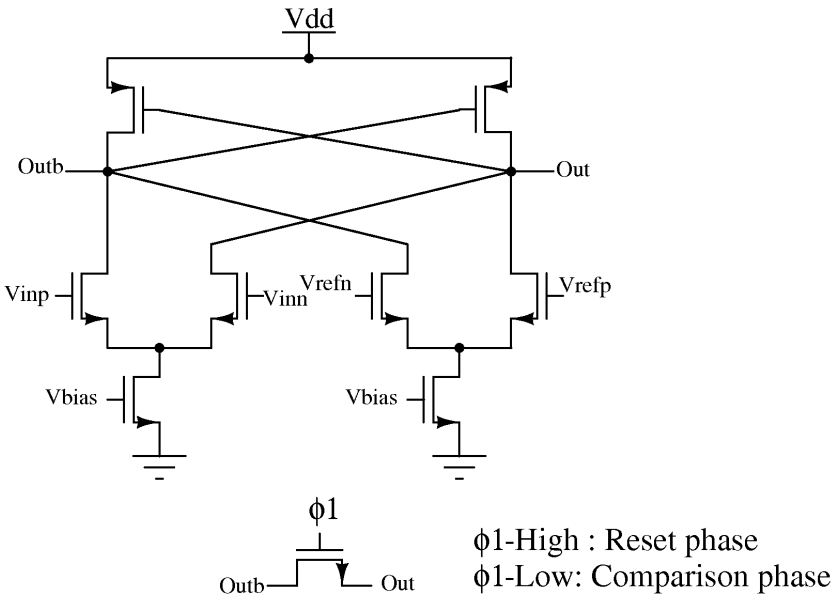


Figure 5.25: A two differential pair comparator

The comparator shown in Fig. 5.25 is chosen for its ease of operation. The entire comparator is shown in Fig. 5.26. As only 5-bits are to be resolved from the SAR, the sample and hold block is implemented using just capacitors. The input is sampled onto capacitors and held at the input of the comparator as shown in Fig. 5.15. The comparator is implemented as a cascade of stages. This is done for two reasons: speed and metastability. The comparator is expected to resolve the decision in as little time as possible. The first latch essentially acts as a preamp. When *latcha* is high, the first latch is reset. During this time, a new reference is set at its input. As *latcha* goes low, the latch starts regeneration. As much as it is desired for this regeneration time to be small, it is also necessary to ensure that the sampled input on the capacitors doesn't get corrupted because of latch kickback whose effect grows with decreasing regeneration time. To minimize kickback, the speed of the latch has to be minimized thus making it slow. This slows down the ADC conversion speed. To overcome this problem, a second latch is added in series

to the first latch. This latch is turned on 100ps after turning on the first latch. The first latch would have amplified the signal considerably in that time allowing the second latch to take off from that point. There are no speed limitations on the second latch and hence it is designed to operate at the maximum speed. A high conversion speed is achieved using this cascade technique.

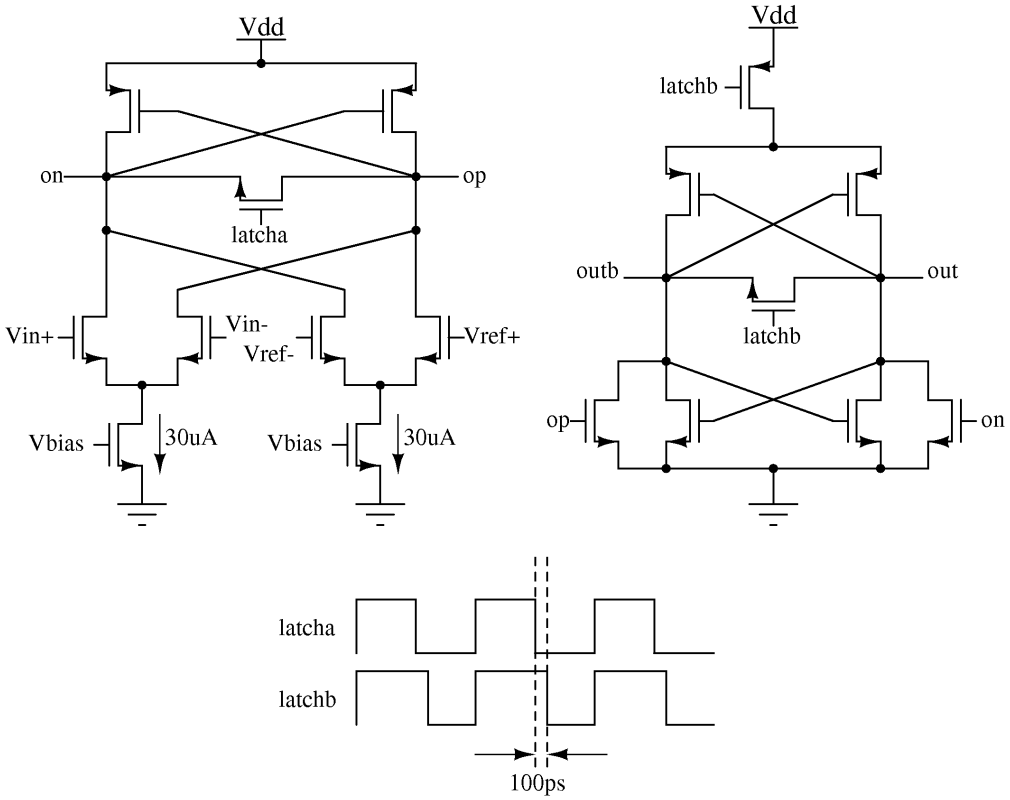


Figure 5.26: A two differential pair comparator

An important design consideration for the first latch is common mode mismatch between the input signal and the reference. The two differential pairs of the latch are intentionally separated to obtain common mode rejection. The structure with differential pairs joined by shorting the drain nodes of the current sources works fine as long as there is no common mode mismatch between the input and reference signals. In the presence of common mode error, the error gets converted

to differential signal thus corrupting the decision process. Though not completely foolproof, the selected comparator can reject some amount of common mode errors and is designed to tolerate 75mV of mismatch. This is considered to be good enough for the design.

5.5.2.2 DAC

DAC is the most critical block in a SAR ADC. The settling accuracy of the DAC should be as good as the ADC resolution desired. At the same time it has to be low power. A simplest implementation is using the resistor string shown in Fig. 5.27(a). The select signal has to be thermometer coded. Advantage with this structure is that the DAC output voltage is proportional to a simple ratio of the resistor values. Though popular for speeds of around 100MSPS and 5-bits, it is tough to make it operate at specifications beyond that. One of the major disadvantages is its varying time constant for different output voltages. This is because of output impedance dependance on the DAC input code. The impedance is maximum at the center code and minimum at the extremes. For proper functionality, the resistor values have to be chosen for worst case time constant. Another disadvantage with this structure is its output loading. All the code select switches are joined together at the output node thereby increasing the capacitance at that point. In implementations where the DAC drives the gate of a transistor, the load is dominated by the self capacitance of the DAC. This is undesirable for high speed applications where the reference is desired to settle in very little time. A workaround for this is shown in Fig. 5.27(b) where the control mechanism is binary. Total number of switches still remains the same as a regular ladder but all of them don't join at a point. Instead, they are connected as a binary

tree which eventually lets the proper DAC voltage out. Though this structure is successful in reducing the output loading it does little to reduce the time constant at that point. The DAC voltage now has to travel through N switches in series before appearing at the output as against one switch in the regular ladder. This can be as much speed limiting as loading at the output.

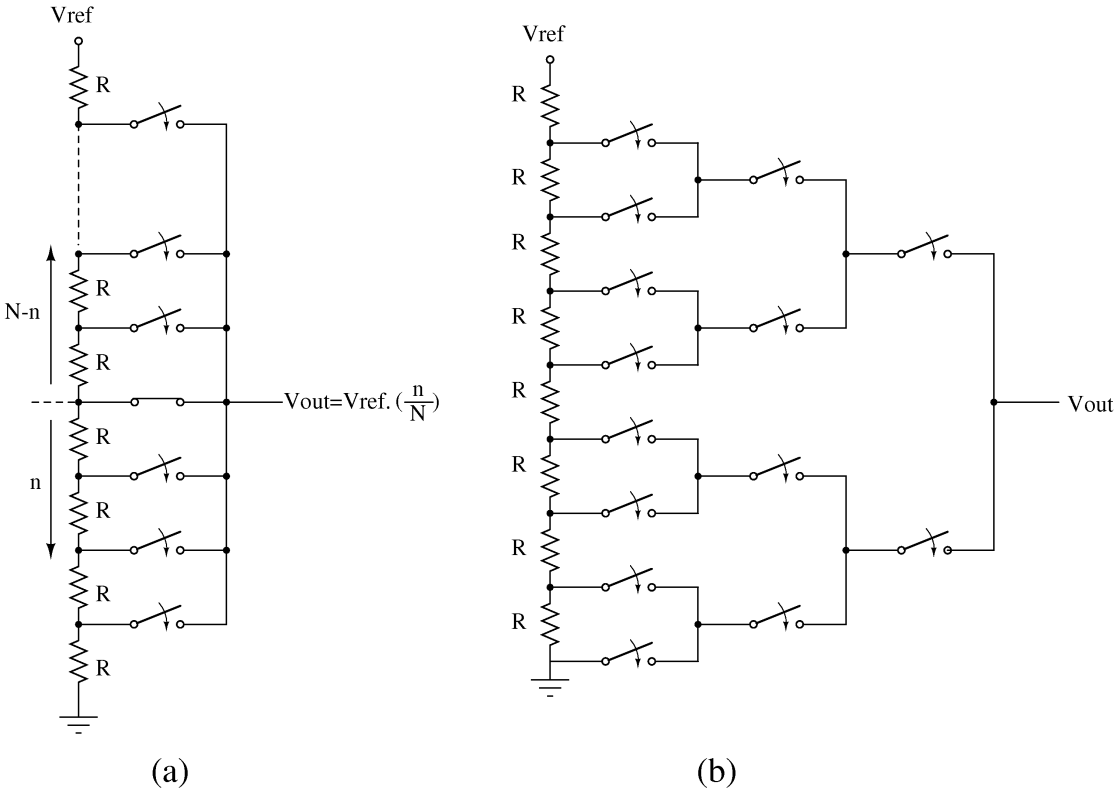


Figure 5.27: (a) A regular resistor string (b) Modified resistor string

A solution to the varying time constant as well as speed is the R-2R ladder shown in Fig. 5.28. This DAC has been used in the SAR ADC design. The control signal is binary. Basing on the control code the 2R resistors are either switched to the positive or the negative reference. This means that the output impedance of the structure always remains constant irrespective of the code chosen. Another advantage with this structure is its high speed of operation. The loading at the

output node is just due to the parasitics associated with the resistors which can be tiny. This enables reference being switched at high frequency without any problems. This structure also fits in well with the SAR ADC because of its binary nature of the control signal. As discussed before, a SAR ADC is a binary search ADC whose output codes appear in binary format starting from the MSB. This output code is the control signal for the DAC and hence no post processing is required. If a resistor ladder is used for the DAC, then a binary to thermometer converter is required. Two issues that have to be taken care of when designing a R-2R DAC are matching and glitches.

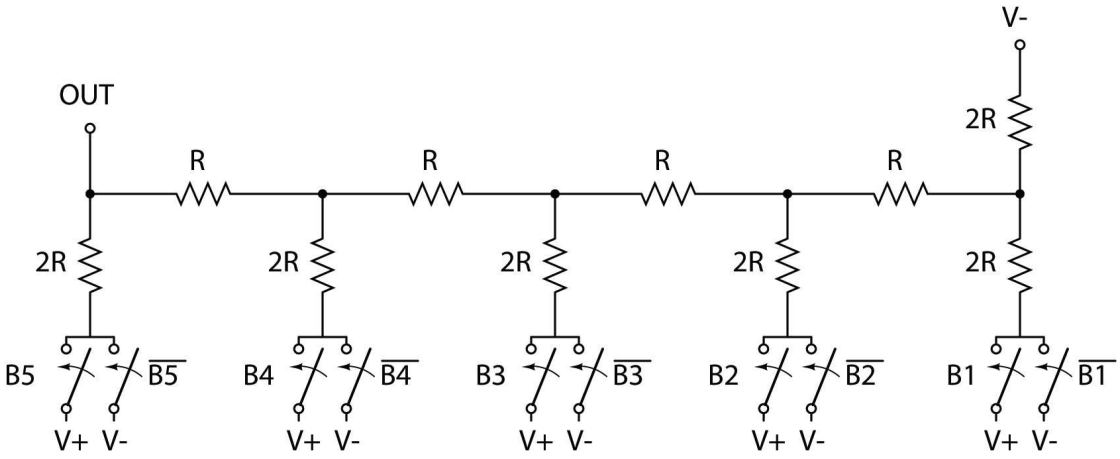


Figure 5.28: A 5-bit R2R DAC

Switches in a resistor string don't carry any DC current in them. The switch resistance only influences the DAC settling time but not the actual voltage. This is not true in the case of a R-2R ladder. The switches connect resistors to references and hence have DC current flowing in them. In an ideal situation, the switch resistance is 0 and only the actual resistor values decide the output voltage. But in reality, the switches have some non-zero on resistance that influences the output voltage. A design approach to overcome this problem is to make the switches as large as possible so that their on resistance becomes negligible compared to R. But

this comes at the cost of increased power consumption in the drivers that drive these switches. Another solution is to account for the switch resistance in the total resistance. This approach tries to match the resistance of switches to the resistance of resistors which holds valid only to a certain extent. Both the above described techniques have been adopted in the design to increase linearity of the DAC.

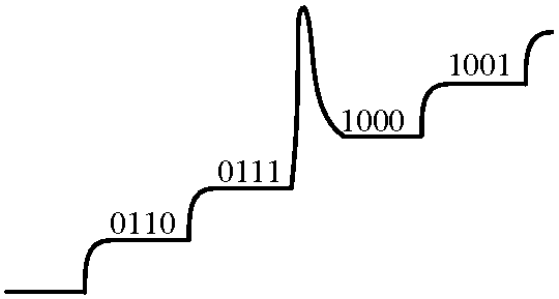


Figure 5.29: Example code transition that causes a glitch

Another issue associated with R-2R is its glitches. When the control code switches from 0111.. type of pattern to 1000.. type of pattern, all the resistors are reconnected to a different reference. The switches take some finite time to do this switching operation during which the resistors are left floating unconnected to any source. Though the output is supposed to move only by an LSB, it first glitches and then settles to the new value as shown in Fig. 5.29. These glitches can sometimes increase the settling time required and it has to be taken care of during design. A common approach to minimize the glitches is to place a capacitor at the output node. But this is not a good solution as it reduces the speed of operation. In the present design no bypass capacitors have been employed to minimize glitches. The settling time required is estimated basing on the glitch width.

5.6 Simulation Results

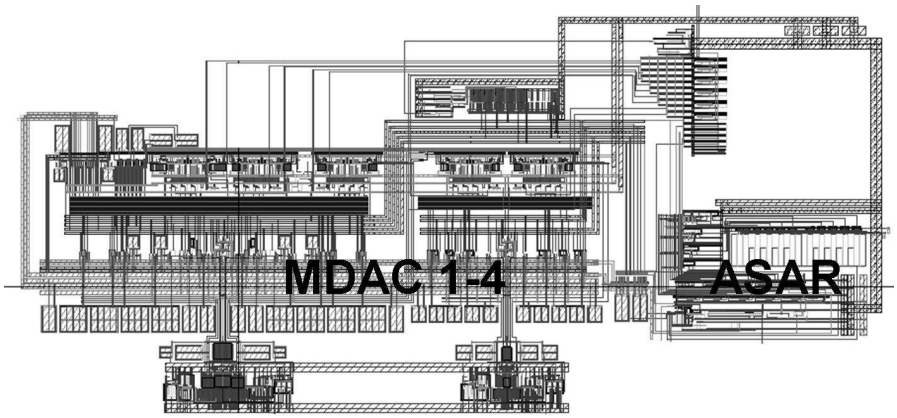


Figure 5.30: Layout of the ADC

The 10-bit ADC has been implemented in TSMC 90nm CMOS process at 1.2V supply. Layout snapshot is shown in Fig. 5.30. The active die area occupied is $0.052mm^2$. Power consumed at 125MSPS operation is 3mW. FFT plot of the output with a Nyquist input is shown in Fig. 5.31. SFDR and SQDR are 67 dB and 60 dB respectively.

5.7 Summary

A rail to rail input hybrid pipelined ADC has been implemented in TSMC 90nm CMOS. The ADC makes use of the entire signal swing available to get rid of an opamp thereby ensuring low power operation. The last 5 bits are resolved using an Asynchronous SAR ADC. This hybrid technique helped in replacing three 1.5-bit stages with a SAR that just has a comparator, a DAC and digital logic. The efficacy of the scheme can be seen in the low power operation and the little active die area the ADC occupies.

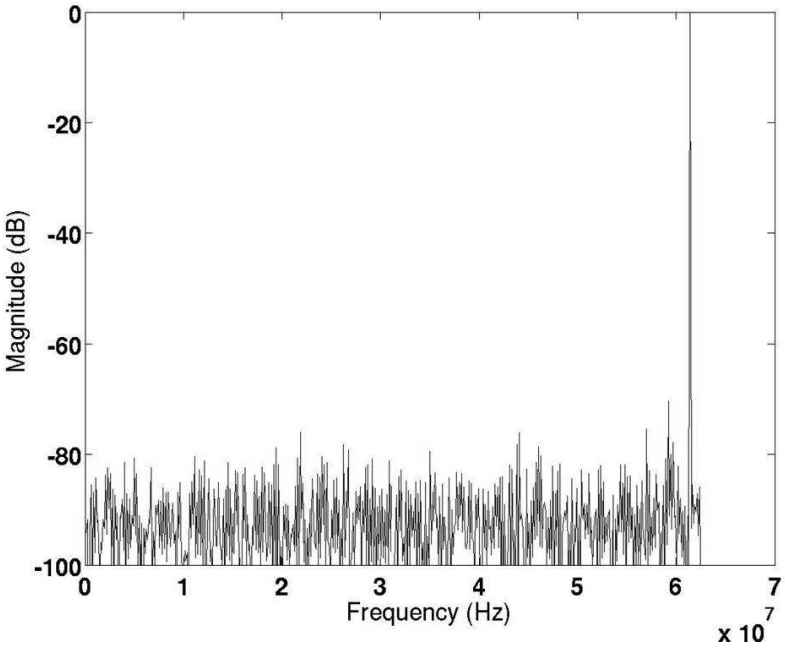


Figure 5.31: Simulated output spectrum at 125MSPS

Chapter 6 . CONCLUSIONS

Four low power techniques that enable low power design of ADCs are presented. The capacitor and opamp sharing technique that reduces load on the first stage opamp is described. Further power reduction is obtained by eliminating the sample and hold. The kickback effect due to absence of SAH is suppressed using the capacitor reset technique. A technique to handle rail-to-rail input swing is also presented. This enables in saving an opamp and thus reducing power. Another power reduction scheme proposed is to replace the backend of the pipelined ADC with an asynchronous SAR ADC thus achieving huge power and area benefits. The efficacy of the techniques is proved by the simulation and measurement results presented.

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