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Title: Design Of High-Speed Low-Power Analog CMOS Decision Feedback Equalizers.

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David Allstot

Decision feedback equalizer (DFE) is an effective method to remove inter-symbol interference (ISI) from a disk-drive read channel. Analog IC implementations of DFE potentially offers higher speed, smaller die area, and lower power consumption when compared to their digital counterparts.

Most of the available DFE equalizers were realized by using digital FIR filters preceded by a flash A/D converter. Both the FIR filter and flash A/D converter are the major contributers to the power dissipation. However, this project focuses on the analog IC implementations of the DFE to achieve high speed and low power consumption. In other words, this project gets intensively involved in the design of a large-input highly-linear voltage-to-current converter, the design of a high-speed low-power 6-bit comparator, and the design of a high-speed low-power 6-bit current-steering D/A converter.

The design and layout for the proposed analog equalizer are carried out in a 1.2 μm n-well CMOS process. HSPICE simulations show that an analog DFE with 100 MHz clock frequency and 6-bit accuracy can be easily achieved. The power consumption for all the analog circuits is only about 24mW operating under a single 5V power supply.

Design Of High-Speed Low-Power Analog CMOS Decision Feedback Equalizers

by

Wenjun Su

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TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

Page

LIST OF FIGURES

Figure Page

LIST OF FIGURES (Continued)

Figure Page

Design Of High-Speed Low-Power Analog CMOS Decision Feedback Equalizers

1 4

Chapter 1. Introduction

This thesis presents the design of an analog Decision Feedback Equalizer (DFE) used in hard disk-drive read channels. Circuits which realize the major and key function blocks in the DFE are discussed in detail. The layout for all the circuits has been completed in 1.2 μm CMOS technology, and the entire DFE will be fabricated very soon.

1.1 System Introduction

An analog decision feedback equalizer (DFE) has advantages over a digital implementation of a DFE in terms of speed, power consumption, and chip area [1],[2],[3]. Fig.1 shows a simplified block diagram of a hard-disk drive read channel with a DFE included. The channel signal suffers from the causal and non-causal intersymbol interference (ISI). The forward filter is responsible for removing the non-causal ISI. An all-pass continuous-time filter with more phase delay at higher frequency can be used to

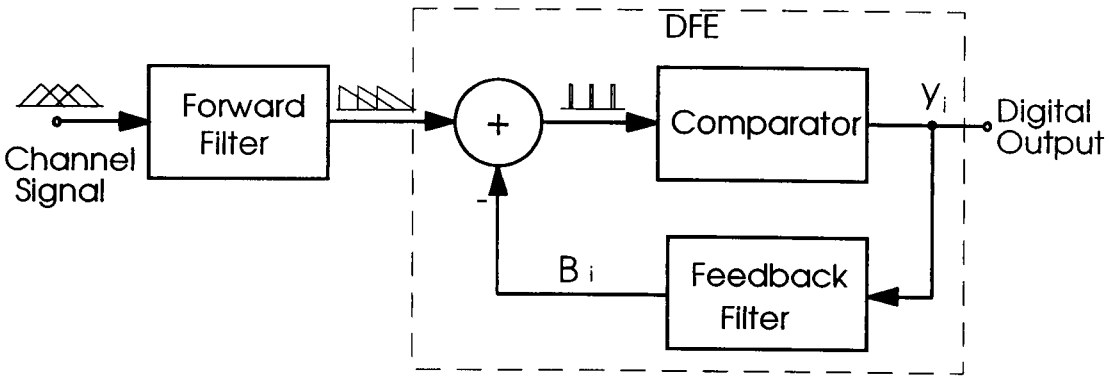

Fig 1.1 Simplified disk-drive read channel block diagram

meet the specification. The output of the forward filter is only with causal ISI. The DFE stage will be responsible to remove this causal ISI by using a linear combination of the past decisions at the output of the comparator.

The feedback filter in the DFE performs a weighted summation of the past output decisions of the comparator, that is,

$$B_i = \sum_{i=1}^{n} C_i y_{n-i} \qquad (n-taps)$$

where y_i is the decision output of the comparator and C_i is the coefficient of the linear combination. This summing result B_i is subtracted from the output of the forward filter to cancel the causal ISI. The weighted coefficients C_i are determined by the channel characteristics and are referred to as ISI factors. This project only concentrates on the DFE design.

The block diagram of the proposed analog DFE is shown in Fig 1.2. The output of the forward filter is a differential voltage signal. In order to achieve high speed, the voltage signal has been changed to a current signal via a transconductor with a large input range. A fully differential-mode signal processing has been chosen in order to reject the noise in the system. The summing circuit is an analog current summation circuit which performs the subtraction between the feedback and the converted input current signal. An 8-tap FIR filter is the only digital part remaining in the DFE and is used to perform the linear weighted combination function. High accuracy and zero offset are the advantages by using the digital FIR filter.

Because the output of the feedback FIR filter is digital, a D/A converter with differential current output must be included in the system. The main clock frequency for

the DFE system has been set at 100 MHz. The LSB current value is set at 3 μA. This is based on the power-speed tradeoff. For example, the value of the LSB current must be larger than the smallest identifiable input current in the comparator.

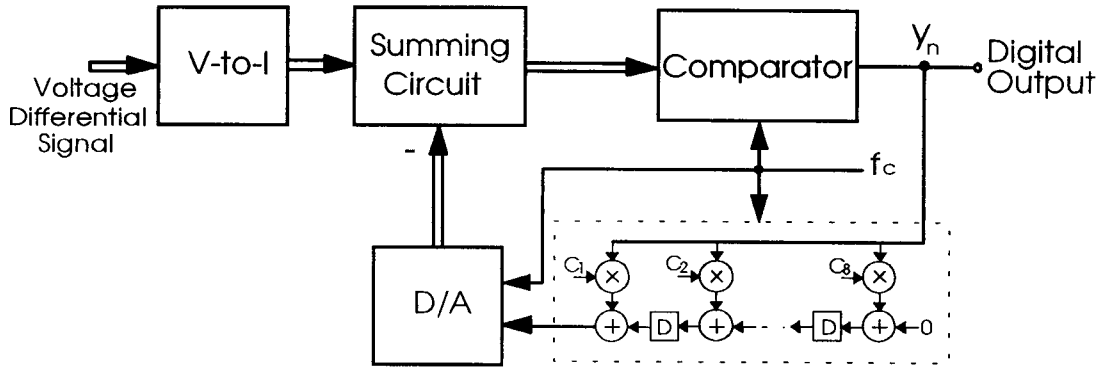

Fig 1.2 Block diagram of the analog DFE

1.2 Thesis Outline

This thesis presents a design for an analog DFE, which includes an large-input V-to-I converter, current summing stage, a high speed comparator, and a 6-bit D/A converter. All the circuits are operated under a 100 MHz clock and a single 5V power supply. Chapter 2 introduces the design of the highly linear V-to-I converter and the current summing stage with at least 6-bit accuracy. Both circuits exhibit more than 35 MHz bandwidth. Chapter 3 considers the high speed comparator design. Speed limitations and clock settling are the major concern in the design. Chapter 4 focuses on the design of the 6-bit 240 MHz D/A converter. A new differential switch driver has been proposed, and the tradeoff between speed and power consumption is also considered. Finally, Chapter 5 gives the simulation results of the DFE, conclusions, and directions for the future work.

Chapter 2. High Linear Large Input V-to-I Converter

This chapter discusses the design of the high linear large-input V-to-I converter (transconductor) and the current summing circuit. It will be shown that the overall accuracy can be enhanced by combining both circuits in one stage.

2.1 Input Range and Linearity Considerations

The simplest and most widely used V-to-I converter is the source-coupled differential pair [5]. The basic circuit is shown in Fig 2.1. By using the simplified square-law relationship for the MOSFET in saturation region and assuming M_1 and M_2 are matched, the difference of the output currents is given by,

$$I_1 - I_2 = \begin{cases} \sqrt{2\beta I_{ss}}\, V_{in} \sqrt{1 - \dfrac{\beta}{2 I_{ss}} V_{in}^2} & |V_{in}| < \sqrt{\dfrac{I_{ss}}{\beta}} \\ I_{ss}\,\mathrm{sgn}(V_{in}) & |V_{in}| \geq \sqrt{\dfrac{I_{ss}}{\beta}} \end{cases}$$

where $ß=K_pW/L$ and I_{ss} is the biasing current. It can be seen from the above equation that in order to maintain a good linearity the input voltage should be smaller than $(I_{ss}/ß)^{0.5}$ which is typically about 50mV. That is much smaller than the input of the proposed DFE. Therefore, the simple source-coupled differential pair can not be used here.

A simple way to increase the input signal range while maintaining a good linearity is by using source degeneration technique [5]. A typical circuit is shown in Fig 2.2. Transistors M_1 and M_2 work as a source follower and most of the input signal voltage

is applied to the resistor R. The resistor R can be replaced by a MOSFET biased in triode region and hence the transconductance g_m of the V-to-I converter becomes tunable.

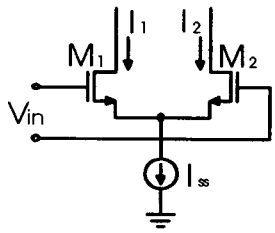

Fig 2.1 Source-coupled differential-pair

This circuit works well with a large input signal, up to 1V peak to peak. However, its output current harmonic distortion is not as small as the DFE requires. The high harmonic distortion is mainly contributed by the back-gate effects in M_1 and M_2. From Fig 2.2 we can see that the source to the substrate voltage V_{SB} of M_1 and M_2 is approximately equal to $\pm V_{in}/2$. This large V_{SB} makes the threshold voltages V_{T1} and V_{T2} in M_1 and M_2 have a nonlinear relationship with the input V_{in}. Therefore, although the signal gate to source voltage V_{gs} is much smaller than V_{in}, the drain current I_d ($= \beta(V_{gs} - V_T)^2$) still has a severely nonlinear relationship with V_{in} because of the V_T variation.

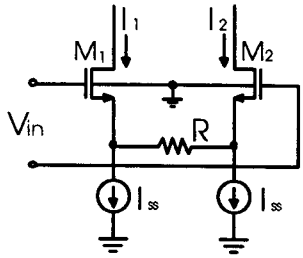

Fig 2.2 Large input-range transconductor

In order to avoid the back-gate effect and reduce the harmonic distortion, a PMOS-pair transconductor can be implemented in our n-well CMOS technology. The circuit is shown in Fig 2.3. The bulk terminals in both M_1 and M_2 have been connected to the corresponding sources and hence $V_{SB} = 0$ in both M_1 and M_2. The main concern with a PMOS transistor is its lower speed. However, our simulations based on the 1.2μm CMOS parameters and the BISM level-28 model show that the PMOS-pair transconductor's bandwidth can reach to as high as 60 MHz, which is good enough in the proposed DFE application.

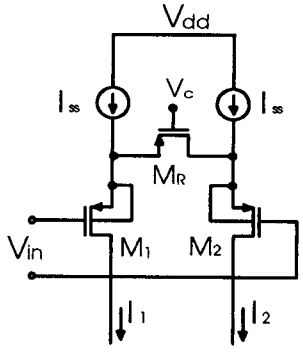

Fig 2.3 High-linear PMOS transconductor

The PMOS transconductor has been chosen to design our V-to-I converter. The simplified schmematic is shown in Fig 2.4. Transistor M_3 simulates the degeneration resistance, while M_4 and M_5 are the biasing current sources for the PMOS pair M_1 and M_2. Transistors M_6 and M_7 are used here to isolate the current summing node d_1 and d_2 from the switching noises in the comparator. Diode-connected transistors M_8 and M_9 convert the summing current into a differential voltage which in turn is sampled and compared in the comparator.

Fig 2.5 gives the simulated output currents I_{d1} and I_{d2} when a 35 MHz 1V peak-peak sinewave input signal is applied. The measured total odd-order harmonic distortion in I_{d1} (I_{d2}) is about -38 dB. The even-order harmonic distortion is not a big concern in our design because it appears as an additional common-mode signal to both I_{d1} and I_{d2}, and it will be rejected by the comparator. From Fig 2.5 we can see that with a fully differential input voltage shown in the upper subplot the output currents I_{d1} and I_{d2} are not fully differential but with a small difference between their corresponding absolute amplitudes. This is because the asymmetrical structure introduced by the connection of the substrate to the source of the transistor M_3. In order to obtain a symmetrical structure, an additional transistor should be added, as will be shown in section 2.3.

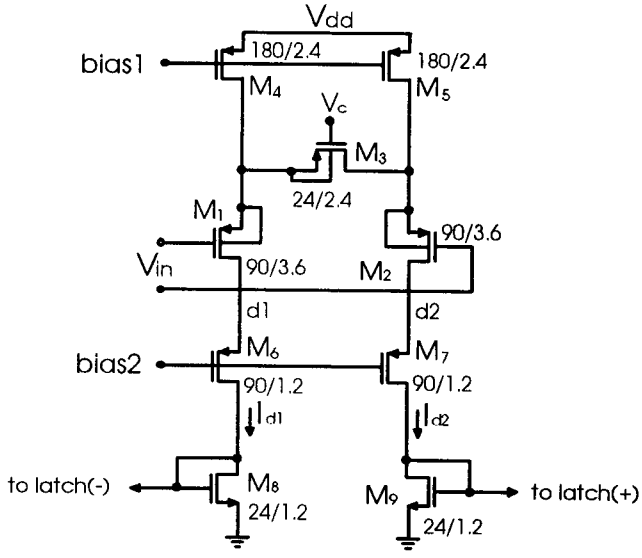

Fig 2.4 The proposed PMOS V-to-I converter

Another major concern in the V-to-I converter is its accuracy. Because the biasing current sources M_4 and M_5 in Fig 2.4 are not a perfect constant current source but with a finite output resistance induced by the transistor channel-length modulation, an error

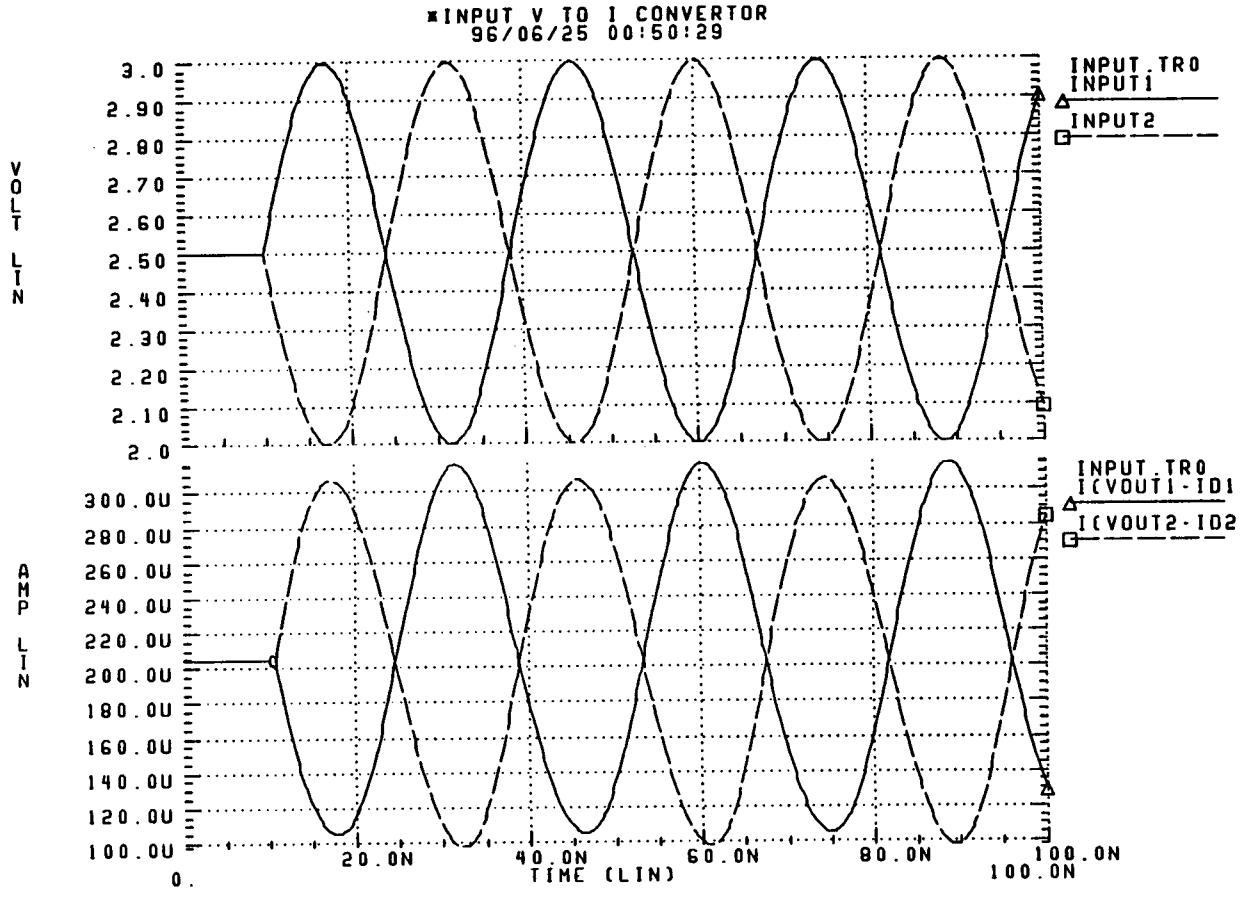

Fig 2.5 Simulated output currents in the transconductor

current exists in the output currents I_{d1} and I_{d2}. Simulations show that with 0.5V to 1V input V_{in} applied, the error currents introduced by the finite output resistances in the biasing current sources range from 10μA to 20μA, which are larger than 3μA (LSB). In order to achieve the required accuracy, these error currents must be reduced to less than 1.5μA (0.5LSB). This can be realized by combining the PMOS transconductor with the current summing circuit, as will be explained in the next two sections.

2.2 Current Summing Circuit

We use a simple current-mirror to mirror the output current of the D/A converter to the transconductor stage. The simple current-mirror also works as a low-pass filter to filter out part of the high frequency glitch noise from the D/A converter. By a proper combination of the PMOS transconductor and the summing circuit, the output current from the D/A converter is subtracted from the output current of the PMOS transconductor. At the same time, the error current in the PMOS transconductor mentioned in Section 2.1 is cancelled by the similar error current in the simple current-mirror, and thus the accuracy in both simple current-mirror and the transconductor is increased. This will be explained in detail in the next section.

2.3 A High Accuracy V-to-I Converter

The error current in the PMOS transconductor mentioned in Section 2.1 can be cancelled by combining the transconductor with the current summing circuit together, as is shown in Fig 2.6. The V-to-I converter is composed by transistors M_3 to M_8 plus M_{1A}, M_{2A} and M_{R1} (M_{R2}), while M_9 to M_{12} plus M_{1B} and M_{2B} construct the current summing circuit in which M_9 and M_{10} (or M_{11} and M_{12}) work as a simple current mirror. Two transistors M_{R1} and M_{R2} are used here to make the V-to-I converter structure

symmetrical. It also should be noted that the transistors M_{1B} and M_{2B} are used here not only to bring the DAC output currents to the V-to-I converter to be subtracted but also to work as a voltage source follower.

Because the input signal is a fully differential voltage, the error currents introduced by M_3 and M_{10} due to the channel length modulation are opposite in phase to the error currents introduced by M_4 and M_{11} due to their channel length modulation effects. If we assume the voltage gains in the source followers $M_{1A}(M_{2A})$ and $M_{1B}(M_{2B})$ are the same, and make the channel length $L_{3(4)}$ of the transistor M_3 (or M_4) and the channel length $L_{10(11)}$ of the transistor M_{10} (or M_{11}) satisfying with the following equation,

$$\frac{I_1}{L_{3(4)}} = \frac{I_2 \quad (or\, I_3)}{L_{10(12)}}$$

all of the error currents will have the same amplitude. Currents $I_1(I_{11})$ and $I_2(I_3)$ are the total currents flowing through the corresponding transistors. The simulated result shown in Fig 2.7 confirms the above analysis. By cross-connecting the drain terminals between the transistor pairs of $M_{1,2\,(A)}$ and $M_{1,2\,(B)}$, the error currents which have the same amplitude but with opposite phase will be added together at the current summing nodes. Therefore, the error components induced by the transistor channel length modulation will be exactly cancelled in the final output currents. In practice, a complete cancellation is not easy to achieve because the output currents I_2 and I_3 of the D/A converter change at each clock period. Fortunately, the changes in I_2 and I_3 are small once the read channel becomes stable. Therefore, most of the error currents will be cancelled.

The simple current-mirror accuracy has also been improved. One of the main error sources in the current-mirrors comes from the unbalanced voltages between the

current driving terminal and the current output terminal. By virtue of the transistor channel length modulation effect, the unbalanced voltage at the output terminal generates an error current which is not controlled by the gate-source voltage of the transistor. However, in our circuit given in Fig 2.6, this error current in the current-mirror has been used to cancel the error current in the transconductor. Relatively large transistor size has also been chosen for the transistors in the current-mirrors in order to reduce the error introduced by transistor mismatch. Therefore, the current-mirrors used in the circuit shown in Fig 2.6 can achieve a high accuracy.

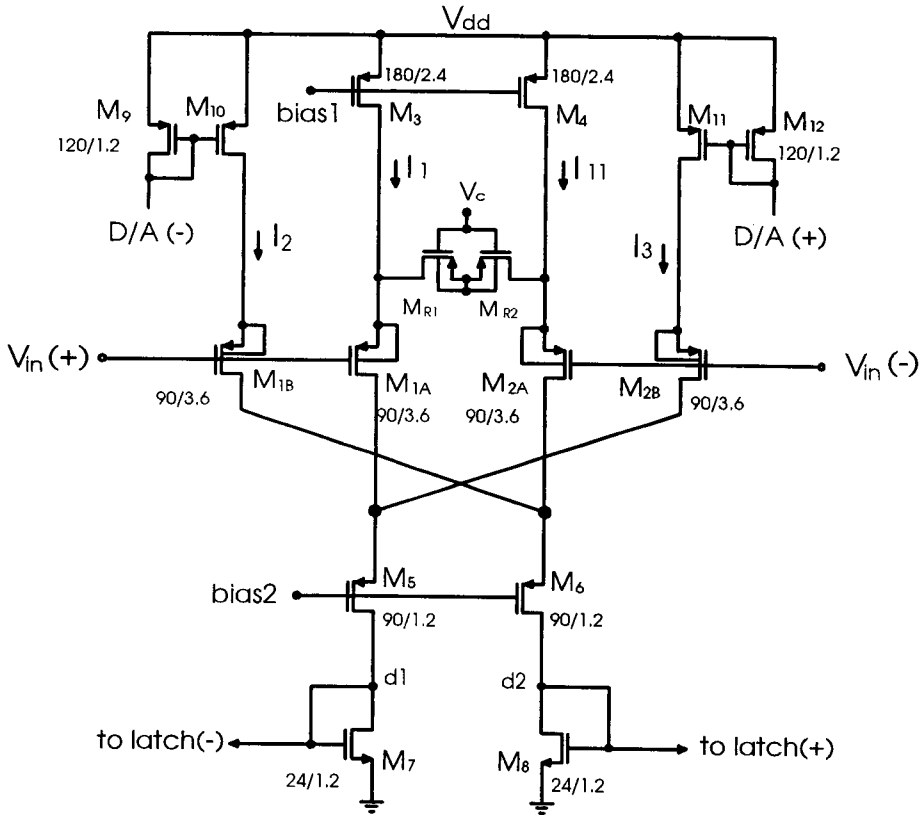

Fig 2.6 High accuracy V-to-I converter and summing circuit

The total harmonic distortion in the output currents at nodes d_1 and d_2 shown in Fig 2.6 remains at the same level as the PMOS transconductor if the transistors M_5 and M_6 have been properly biased. Our simulations with 1% parameter mismatches show that the total odd-order harmonic distortion in the circuit shown in Fig 2.6 is about -35.5dB. The total power dissipation has been found as 5.6 mW.

2.4 Summary

The proposed source degenerated PMOS differential pair overcomes the tradeoff between the signal input range and the output current linearity. Simulations with 1% parameter mismatches in the transistors have shown that the total odd-order harmonic distortion in the output current is about -35.5dB when a 1V peak-peak sine wave input voltage is applied. This result is good enough to be applied in the proposed DFE application. However, a higher accuracy DFE might require harmonic distortion smaller than -35dB. In this situation, an additional PMOS transistor pair can be added to cross-coupling with the circuit shown in Fig 2.4. By properly scaling the transistor sizes and the biasing currents, a further cancellation of the remaining odd-order nonlinearities can be achieved [6].

Accuracy is another major concern in the V-to-I converter. The MOSFET channel length modulation limits the accuracy of the PMOS transconductor. However, in the circuit shown in Fig 2.6, by cross-coupling the current summing circuit with the PMOS transconductor the error currents in both current summing circuit and the PMOS transconductor cancel each other. Hence, the overall accuracy has been enhanced.

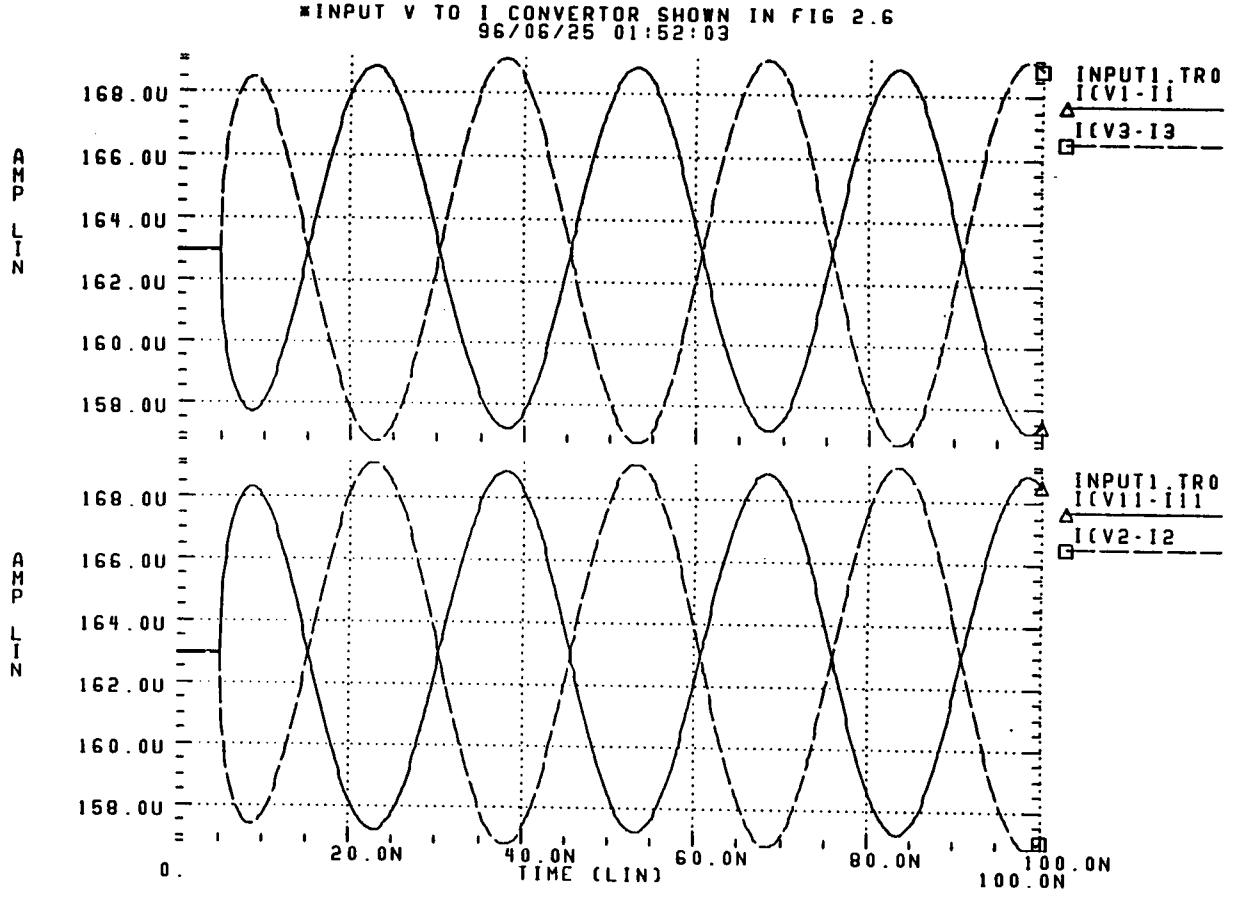

Fig 2.7 Error currents in I_1 and I_3 (I_{11} and I_2)

Chapter 3. High Speed Comparator with 6-bit Resolution

The design of a high speed comparator achieving 6-bit resolution is presented in this chapter. The comparator is operated under a 100MHz single phase clock without employing the offset cancellation technique. The requirement for achieving high operating speed is highlighted in the overall design.

3.1 Speed Considerations

The conventional high speed CMOS comparators are all based on the simple latch structures, as is shown in Fig 3.1 [7],[8],[9]. This circuit consists of an NMOS flip-flop composed of M_3 and M_4 , a pair of NMOS transfer gates for strobing, and a PMOS flip-flop composed of M_7 and M_8. Capacitor C_A is the total stray capacitance connected to the drain terminals of M_3 and M_4, while C_B is the total stray capacitance connected to

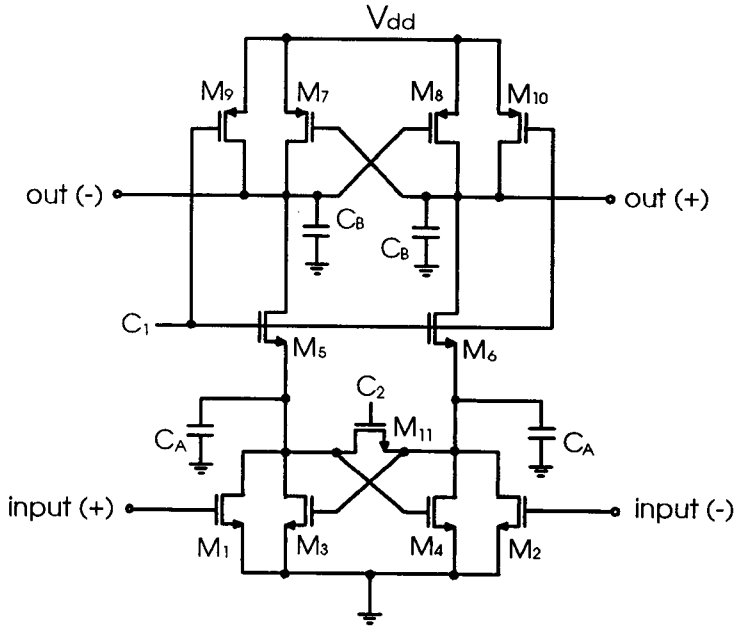

Fig 3.1 Conventional high speed CMOS comparator

the output nodes. Because C_A consists mainly of the drain capacitances of the small size NMOS transistors M_1 to M_6 while C_B is contributed by the drain capacitances of the transistors M_5 and M_6 and by the drain and gate capacitances of the large PMOS transistors M_7 to M_{10}, C_B is at least 3 times larger than C_A [7], [8].

The dynamic operation of this circuit is divided into reset interval during phase C_2 and comparison (regeneration) interval during phase C_1 . At the reset interval (C_2 is high), transfer gates M_5 and M_6 are 'off'. The output will be precharged up to power supply voltage level by the precharge transistors M_9 and M_{10}, while the NMOS flip-flop will be discharged to ground level by the two input transistors M_1 and M_2. During the comparison interval (C_1 is high), the transfer gates M_5 and M_6 are turned 'on' and currents will flow from the PMOS flip-flop down to the NMOS flip-flop. The small difference in the input will be amplified to a voltage swing nearly equal to the power supply voltage by the positive feedback in both the NMOS and PMOS flip-flops. The input offset voltage comes from the mismatch between the input transistors M_1 and M_2 and between transistors M_3 and M_4. The differential errors caused by charge injection when turning on the transfer gates M_5 and M_6 also increase the input offset voltage.

Based on the above explanation, the speed characteristic in the comparator can be divided into the resetting speed and the regeneration speed. The resetting speed is determined by the precharge rate in the precharge transistors M_9 and M_{10} and the capacitor C_B, and by the recovery rate in the switch transistor M_{11} and the capacitor C_A, depending on which one is slower. From the circuit shown in Fig 3.1, the precharge time constant is approximately equal to,

$$\tau_{pre} \approx R_{on,M_9} C_B$$

while the recovery time constant is roughly equal to,

$$\tau_{rec} \approx 2R_{on,M_{11}}C_A$$

where $R_{on,M9}$ and $R_{on,M11}$ are the equivalent resistances when the corresponding transistors are in linear region. Because $R_{on,M9}$ is larger than $R_{on,M11}$ under the same biasing conditions, and C_B is larger than C_A, τ_{pre} is larger than τ_{rec} and the resetting speed is limited by the precharge rate.

In the same way, the regeneration speed is determined by both the gain in the NMOS flip-flop and the gain in the PMOS flip-flop. The time constant related with the NMOS flip-flop can be found as,

$$\tau_{reg,NMOS} \approx C_A / g_{m3,4}$$

while the time constant related to the PMOS flip-flop is,

$$\tau_{reg,PMOS} \approx C_B / g_{m7,8}$$

where $g_{m3,4}$ and $g_{m7,8}$ are the transconductances in their corresponding flip-flop. It is well known that the transconductance in an NMOSFET is about two times larger than a PMOSFET's under the same bias. Also, we already know that the capacitance C_B is larger than C_A. Hence, the regeneration speed is mainly limited by $\tau_{reg,\,PMOS}$.

From the above analysis, we can conclude that the speed of the comparator shown in Fig 3.1 is limited by the PMOS flip-flop because of its larger stray capacitances and its relatively smaller transconductance. The conclusion has also been verified by HSPICE

simulations. The simulated results based on the 1.2μm CMOS parameters have shown that the maximum clock frequency in which the comparator can be operated with 0.1PF load is only about 69 MHz.

3.2 An Improved High Speed Comparator

Based on the analysis in the above section we know that the comparator speed is limited by the PMOS flip-flop because of its large stray capacitance contributions to the output nodes. By checking the circuit shown in Fig 3.1, we also know that the major contributions of the stray capacitances come from the large gate capacitances in the cross-coupling PMOSFET pair M_7 and M_8. In order to reduce the stray capacitances at the output nodes, we can simply eliminate the PMOS flip-flop and replace it with two PMOS biasing current sources. The two precharge transistors are also abandoned. This finally results in our improved high speed comparator, as is shown in Fig 3.2.

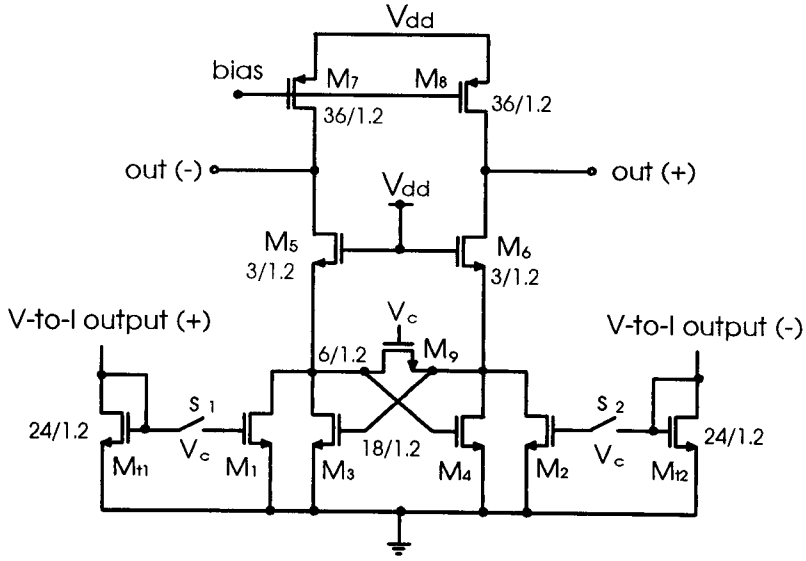

Fig 3.2 The proposed high speed comparator

It can be seen from Fig 3.2 that only drain stray capacitances in the biasing current sources M_7 and M_8 are connected to the output nodes, and only an NMOS flip-flop is used to regenerate the output. The transfer gates M_5 and M_6 are small-size transistors and are always turned 'on' to keep the capacitance loads to the NMOS flip-flop small. Because M_5 and M_6 are always 'on', there is no charge injections from M_5 and M_6 and the input offset voltage in the improved circuit is smaller than the circuit in Fig 3.1. The NMOS flip-flop amplifies the input difference and the amplified result is directly transmitted to the output nodes via transistors M_5 and M_6. Hence, a higher operating speed in the improved comparator can be expected.

The biasing current supplied by the transistors M_7 and M_8 must be large enough to avoid the slew limitation occurring at the output nodes. If the comparator works at 100 Mhz clock frequency and the output voltage swing is about 5V, the slew-rate at the output nodes must be larger than 1000V/μs. Assuming that the total capacitance at the output nodes is about 0.2 PF, then the biasing current must be at least equal to or larger than 200μA. The increased power consumption is the price paid for increased speed.

Fig 3.3 gives the simulated results for the improved comparator shown in Fig 3.2. The clock frequency is set at 120MHz, and the biasing current is set at about 400μA. The fully differential output currents from the V-to-I converter are changed into differential voltages in the diode connected transistors M_{t1} and M_{t2}, which in turn are sampled when the switches S_1 and S_2 are closed and are held in the gate capacitances of the transistors M_1 and M_2. When S_1 and S_2 are opened, the difference in the input differential currents which come from the V-to-I converter has been set at about 4μA, which is less than 1LSB in the DFE (1LSB = 2×3 μA). From Fig 3.3, we can see that the comparator has made the right decisions based on the input differential currents. The simulated total power dissipation in this circuit has been found as 6.2 mW.

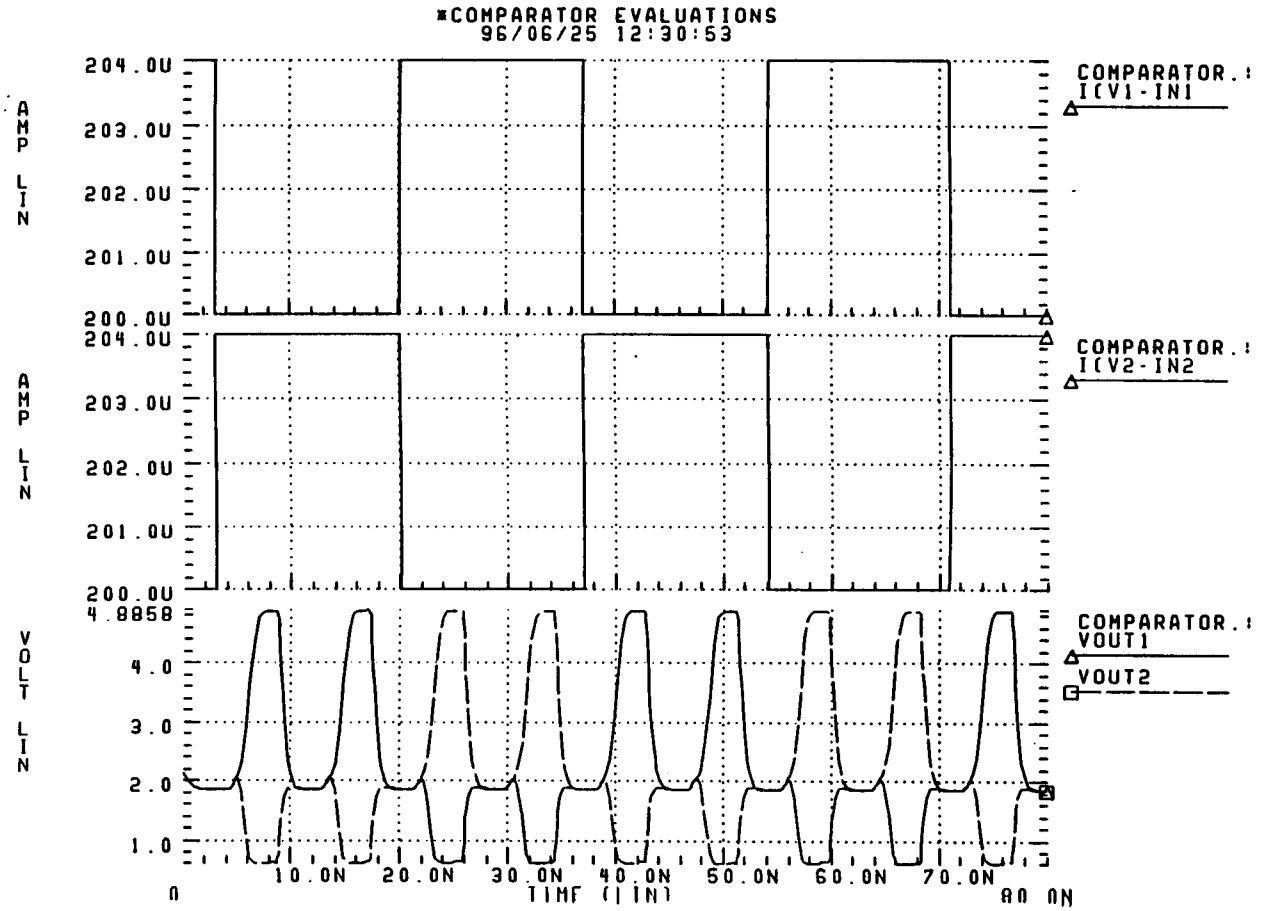

Fig 3.3 Simulations of the proposed comparator with 120MHz clock

3.3 Consideration in DFE Application

The proposed comparator shown in Fig 3.2 can be directly used in our analog DFE. However, there are two additional considerations worth mentioning. First, the output decision of the comparator in the DFE must be brought out of the chip. In order to release the design of the pin drive circuit, the decision of the comparator must be held longer enough until the next decision. Because the proposed comparator works under a single phase clock and its output decision only valid during the regeneration half period (only 5nS if clock frequency is 100MHz), additional digital gates have been added to the comparator, as is shown in Fig 3.4. It can be seen that the phase of the clock C_2 is a little bit ahead than C_1, and C_2 is used as an enable/disable control logic to the R-S latch.

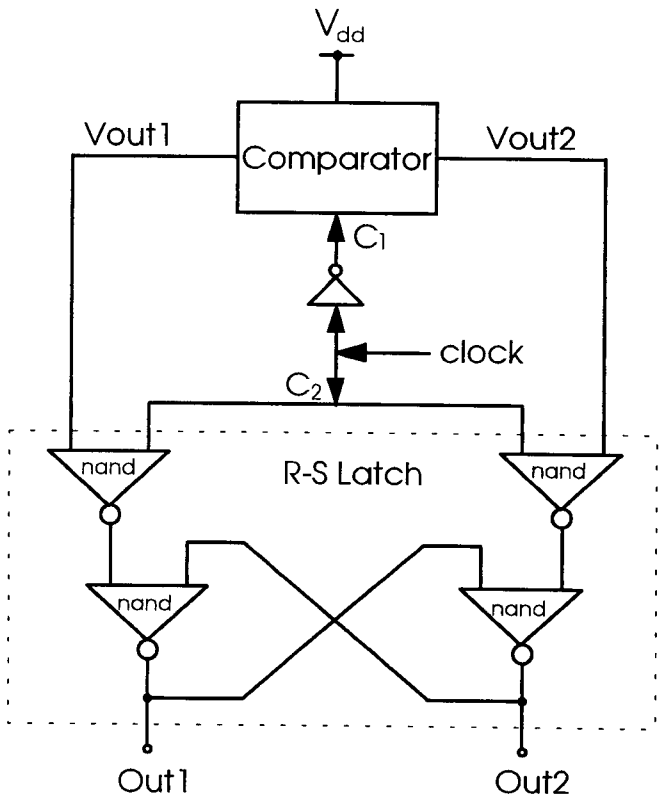

Fig 3.4 The comparator applied in DFE

After a decision has been made by the comparator and right before the reset clock C_1 is in effective, the control clock C_2 disables the R-S latch. Therefore, the decision will be continuously stored in the R-S latch until the next decision is generated. Hence, each output decision will be held for about 10nS with 100 MHz clock.

The second consideration regards the input sampled signals in the comparator. From Fig 3.2 we can see that the control clocks of the sampling switches S_1 and S_2 are the same as the resetting clock. Because of the clock feedthrough and the charge injections in the switch transistors S_1 and S_2 , the sampled signals stored at the gates of M_3 and M_4 are not stable at the beginning when the switches S_1 and S_2 are turned 'off'. Therefore, if we turn off the switches S_1 and S_2 at the same time with the resetting switch turning off, the comparator will make its decision based on the unstable sampled signals and an error decision could be made. To overcome this problem, we make the switches S_1 and S_2 turned off a little earlier than the resetting switch turned off. This will give some free time to allow the sampled signal settling.

A simulated result for the circuit shown in Fig 3.4 is given in Fig 3.5. It can be seen that the output decision has been held for 10nS instead of 5nS at a 100 MHz clock frequency.

3.4 Summary

The comparator is a key part in the analog DFE because it limits the DFE operating speed. The speed limitations in the existing comparators have been thoroughly investigated. Based on this, an improved comparator was obtained with an operating speed up to 120 MHz and well fitted in the DFE system. Because the comparator only

needs a single-phase clock, the clock generating circuit is much simpler than other circuits in comparators which need multi-phase non-overlapping clocks.

For a further improvement, the input transistors M_1 and M_2 in the comparator shown in Fig 3.2 may be replaced by a differential amplifier. This will result in a comparator with higher resolution and lower input offset.

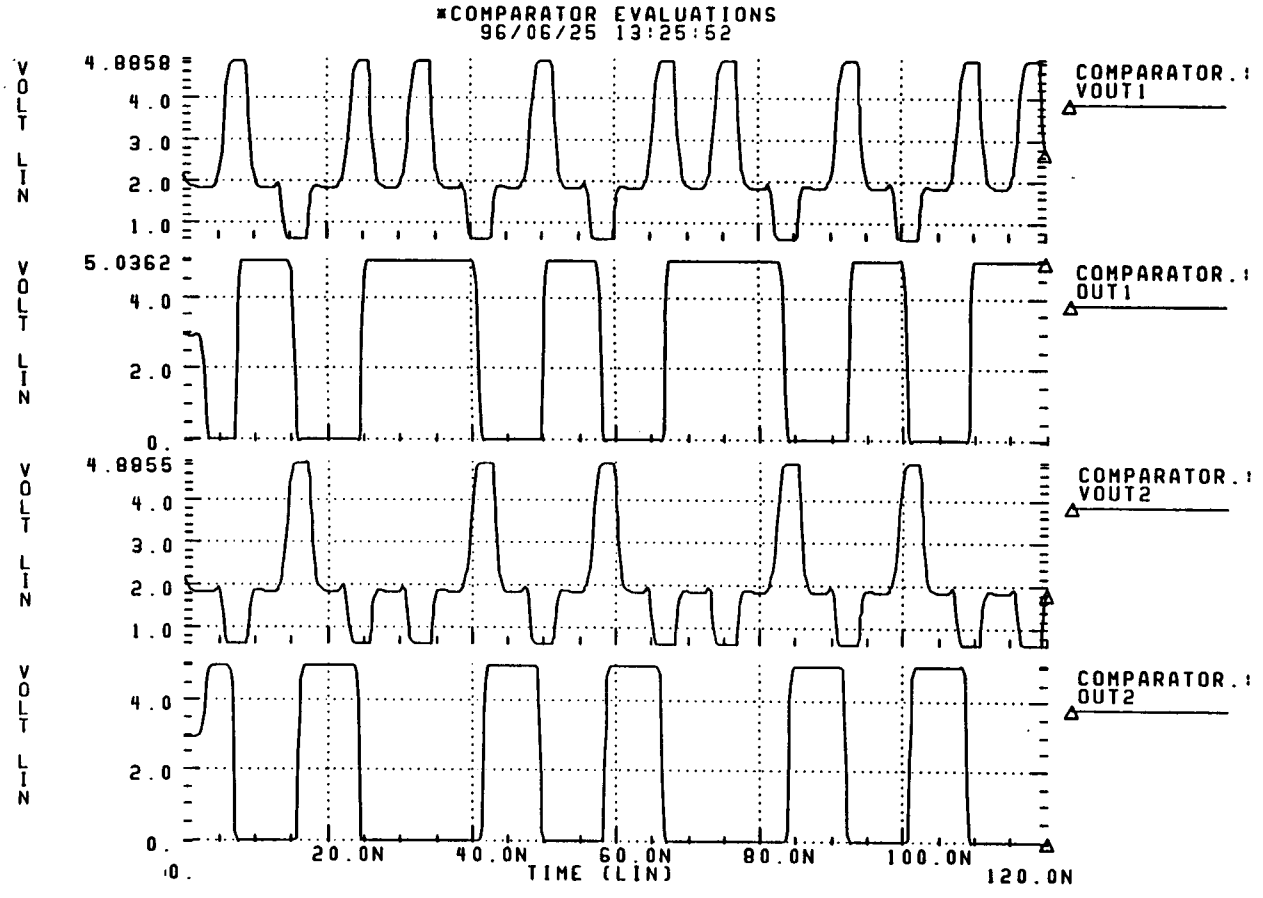

Fig 3.5 Simulated Outputs of the Proposed Comparator

Chapter 4. 6-bit 240MHz D/A Converter

The D/A converter (DAC) required in the analog DFE must operate at more than 100 MHz clock frequency and with at least 6-bit resolution. By studying the existing DACs, an improved high speed DAC which is well compatible with the other blocks in the DFE is obtained. Special attentation is paid to improving the current switch driving circuit, and reducing the power consumption.

4.1 Basic Structure

Almost all of the high speed DACs are based on the current-steering technique [11]-[14]. The proposed DAC is also based on this technique. The basic 6-bit structure of the current-steering technique is shown in Fig 4.1. The lower part is a set of binary-weighted cascode current sources in which the transistors in the higher line have smaller sizes than the transistors in the lower line. This will make the stray capacitances connected to the common-source terminals of the switches small.

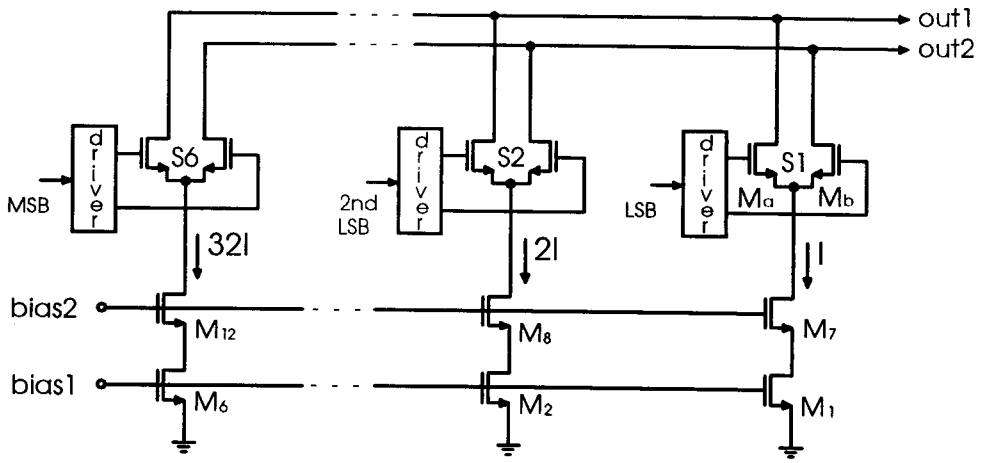

Fig 4.1 Basic structure of the current-steering DAC

The binary-weighted current sources will be switched towards to the outputs by the differential switches S_1 to S_6, depending on the value of the input digital data which controls the switch driving circuits.

In order to achieve fast operation, several effects have to be taken into account. First, the time that the current differential switching transistors M_a and M_b are simultaneously in 'on' or 'off' states must be as small as possible. This is because if both switches are off the output nodes of the binary-weighted current sources are rapidly discharged, bringing the current sources themself into the nonsaturation region. The following recharging of the output nodes slows the operation of the circuit. On the other hand, if the differential switches are simultaneously turned on, the current division between the two paths is out of control. If the situation occurs for a relatively long time, a glitch in the output current results. To make the simultaneously 'on' and 'off' time small, the transition time of the driver's output must be kept as small as possible, and the transition point should be located in the middle transition region.

Second, the driver's output voltage must be restricted to such levels that the tail currents of the differential switches are just switched to the different output lines. There are four reasons for this requirement:

(a) The voltage excursions at the output terminals of the binary-weighted current sources will slow down the operation of the circuit due to the continuous charging and recharging of the parasitic capacitances present at these nodes.

(b) A large voltage excursion at the output terminals of the binary-weighted current sources will make the cascode transistors in the current sources operate in the nonsaturation region and degrade the binary current accuracy.

(c) The transistors used in the differential switches have a large width in order to carry a large current, thus their gate capacitance, which makes up the load of the driver, is large. In order to increase the switching speed, the driver's output swing should be clamped to the minimum allowed value (about 0.5V).

(d) The feedthrough of the digital input data to the output, which is proportional to the digital input swing, should be minimized.

From the above explanation, we know that the major task in achieving high speed DAC is to design the differential switch driver to meet the above requirements. Since the distortion performance of the DAC can be severely limited by the accuracy of the individual bit currents, special attention is also required to keep all of the binary-weighted currents accurate to within half an LSB current.

4.2 Differential Switch Driver Design

From the above section, we know that the driver is a critical part for the high speed DACs. Several driver schemes already exist [11]-[14]. Fig 4.2 shows a typical driver circuit and a differential switch for a single bit section given in reference [11]. It can be seen that the differential switch is connected to the output of the driver at the left-hand side of the diagram. The driver is built out of an NMOSFET differential pair M_3 and M_4, controlled by the digital input data and loaded by the diode-connected transistors M_5 and M_6. The output level and swing are determined by the values of the current sources I_1 and I_2, and the size of the transistors M_5 and M_6. The use of the current source I_2 is to obtain a well-defined switching level and to guarantee the speed since the load transistors M_5 and M_6 always stay active.

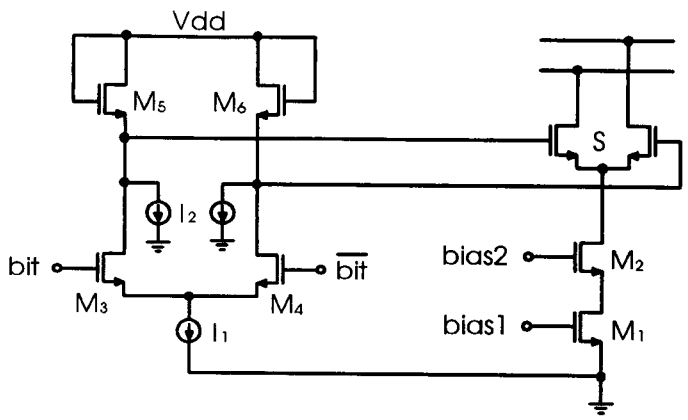

Fig 4.2 A driver circuit given in reference [11]

This driver works well at a clock frequency up to 50 MHz, but can not be used at higher frequencies. The reason is that its output has a relatively large transition time because of the limited slew-rate at its output. It's true that the slew-rate can be increased by increasing the biasing current I_1 and using larger transistors M_5 and M_6. Unfortunately, the output level is also related to these components. Changing the values in these components also changes the output level which should be kept at about the same value for all of the drivers. Furthermore, the power consumption will also be largely increased.

In order to make the DAC operate at a speed larger than 100MHz, we generate a new driver circuit by using a positive feedback at its output nodes, as shown in Fig 4.3. The input digital data is applied to the gates of M_3 and M_4. The input difference will be amplified by the cross-coupling transistors M_8 and M_9 which form a positive feedback loop. Therefore, the output during the transition period will quickly sweep over the transition state and clamped to the pre-set stable levels. The current sources I_2 are added for the same reason as the current sources I_2 in the circuit shown in Fig 4.2. The current

sources M_5 and M_6 are used here to limit the power dissipation based on the required operating speed and to set the required output level. Obviously, to achieve higher operating speed the current sources have to be larger. The required output level and swing can be obtained by properly setting the current sources I_2 , M_5 and M_6 together with the size ratios of the transistors M_3 ,M_4 , M_5 , M_6 , and M_7.

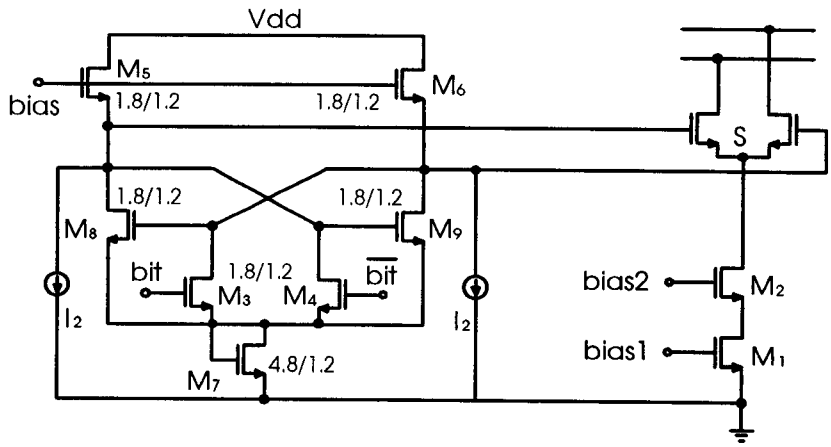

Fig 4.3 The proposed high-speed driver circuit

The proposed driver works very well at clock frequencies up to 240 MHz. The simulations show that transition point in the output is almost located at the middle of the transition even if the digital input data has a skew. The power consumption can be easily controlled by the current sources M_5 and M_6 based on the required operating speed. Fig 4.4 gives the simulated output of the proposed driver (labeled by out1 and out2) when putting it in the DAC. For comparison, the simulated output of the driver shown in Fig 4.2 (labeled by out11 and out22) is also given. Both drivers have the same input in which a small skew exists. It can be seen that the output of the circuit in Fig 4.2 has a larger transition time and its transition point is not in the middle position but in the higher voltage level instead. This will result in a relative longer simultaneously 'on' period in the

Fig 4.4 Simulated outputs of the proposed driver and the driver in [11]

differential switch, and hence a larger glitch noise will appar at the output of the DAC. However, the output of the proposed driver meets the requirements. The transition point is about in the middle of the transition region and its level is about 2.35V. The output swing can be found from 2.1V to 2.6V.

4.3 Accuracy Consideration in the Binary-Weighted Current Sources

The DAC linearity depends on the matching and on the output impedance of the binary-weighted current sources. Because the voltage level and swing at the output terminals of the current sources have been set to the proper level, the cascode transistors in the current sources can be guaranteed to work in the saturation region. Therefore, the output impedance of the current sources are very large (typically more than 200KΩ) and their effects can be neglected.

The matching among the current sources can be improved by using large transistors and by using a symmetrical layout. As mentioned in Section 4.1, the transistors M_1 to M_6 in the current sources shown in Fig 4.1 have large size. The current accuracies mainly rely on the matching among these transistors.

The symmetrical layout configuration of the 6-bit binary-weighted current sources is given in Fig 4.5. The effects of the doping gradients or the oxide thickness gradients on the accuracy of the bit currents are eliminated by the symmetrical distribution of the unit current sources that make up each bit current across the line. In a geometric sense, the centroid of the composite current sources is located at the center of the line. Simulations show that both integral and differential linearities are less than 0.5LSB with the symmetrical layout. Fig 4.6 gives the simulated DAC output with a large swing. The upper-level subplot is one of the driver's outputs, and the lower-level

subplot is the output of the DAC. The simulated total power dissipation in the DAC is about 14.2 mW.

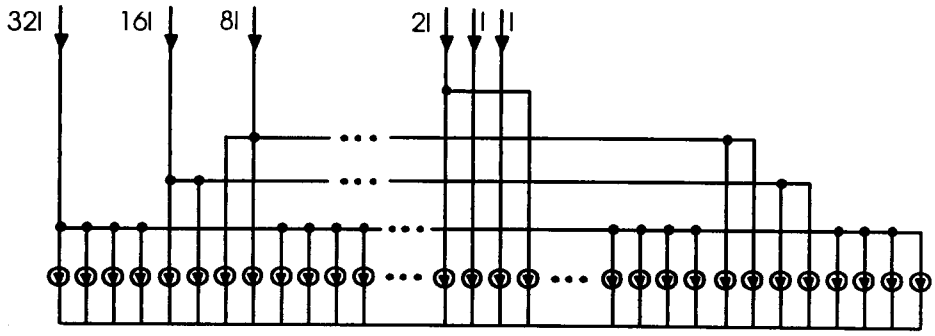

Fig 4.5 Symmetrical layout configuration of the 6-bit current sources

4.4 Summary

The design of a high speed DAC has been presented. The key point is to drive the differential switches in the proper way. A new driver circuit with positive feedback has been proposed. Compared to the other driver schemes, the proposed driver gives an optimized driving waveform, and thus higher speed can be achieved.

The accuracy of the binary-weighted current sources has been guaranteed by using the cascode structure and the symmetrical layout. Based on the simulations, the nonlinearity of the DAC is less than 0.5LSB.

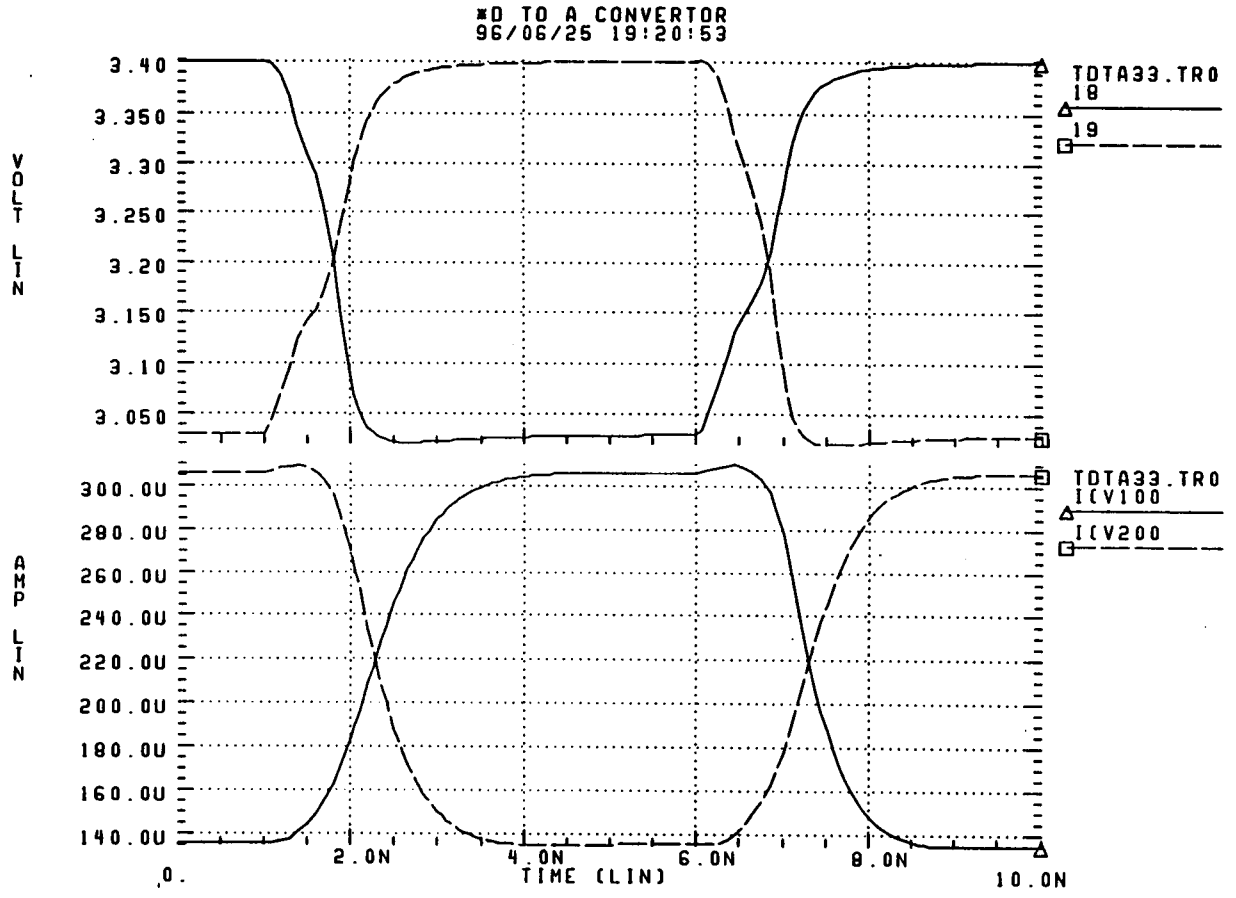

Fig 4.6 Simulated Large swing Current Outputs of the Proposed DAC

Chapter 5. Results and Conclusions

The DFE system has been built by using the circuits presented in the previous chapters. The corresponding layout has also been completed, while the layout of the digital FIR filter has been carried out separately by another student.

5.1 Simulations of the DFE Circuits

The DFE system shown in Fig 1.2 has been built by inserting the proposed circuits to the corresponding blocks. One-tap of the FIR filter has been included. A 1V peak-peak 35 MHz differential sine wave signal is applied to the input of the V-to-I converter. The clock frequency has been set at 100 MHz. Comprehensive simulations have been conducted based on the built DFE in which the DAC has been switched from its full output range to an LSB output range. Simulations have shown that the right decisions have been made for all the different DAC outputs. Fig 5.1 gives the simulated results of the output of the DAC (second subplot), input signals to the comparator (third subplot), the decisions made by the comparator (fourth subplot), and the final output of the DFE (the last subplot). The DAC output switches between 2nd MSB current in this simulation. Fig 5.2 presents the similar simulated results when the DAC output switches between the 1LSB current. It can be seen that the right decisions have been made and each decision can be kept for about 10 nS at the DFE output. The total simulated power dissipation in the DFE is about 24.32 mW.

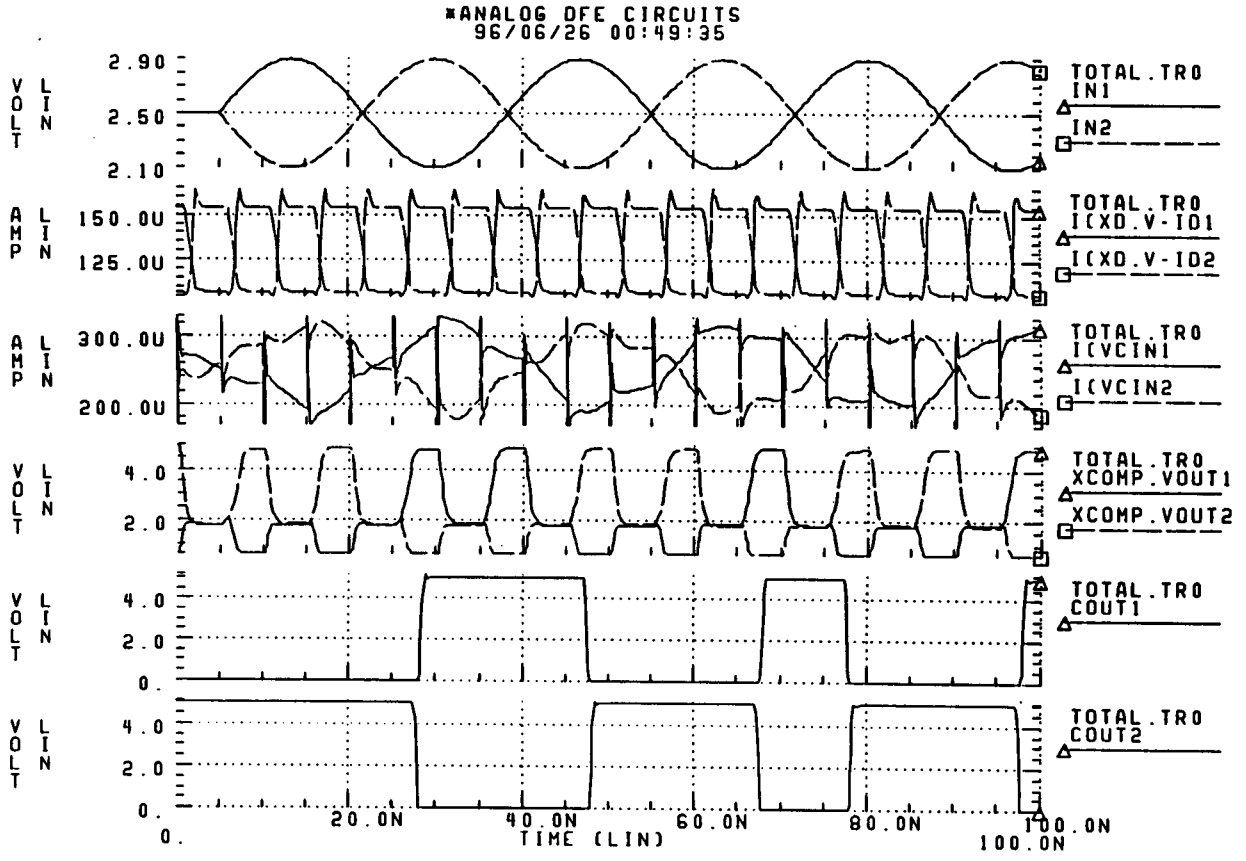

Fig 5.1 Simulated results of the DFE with a large DAC output

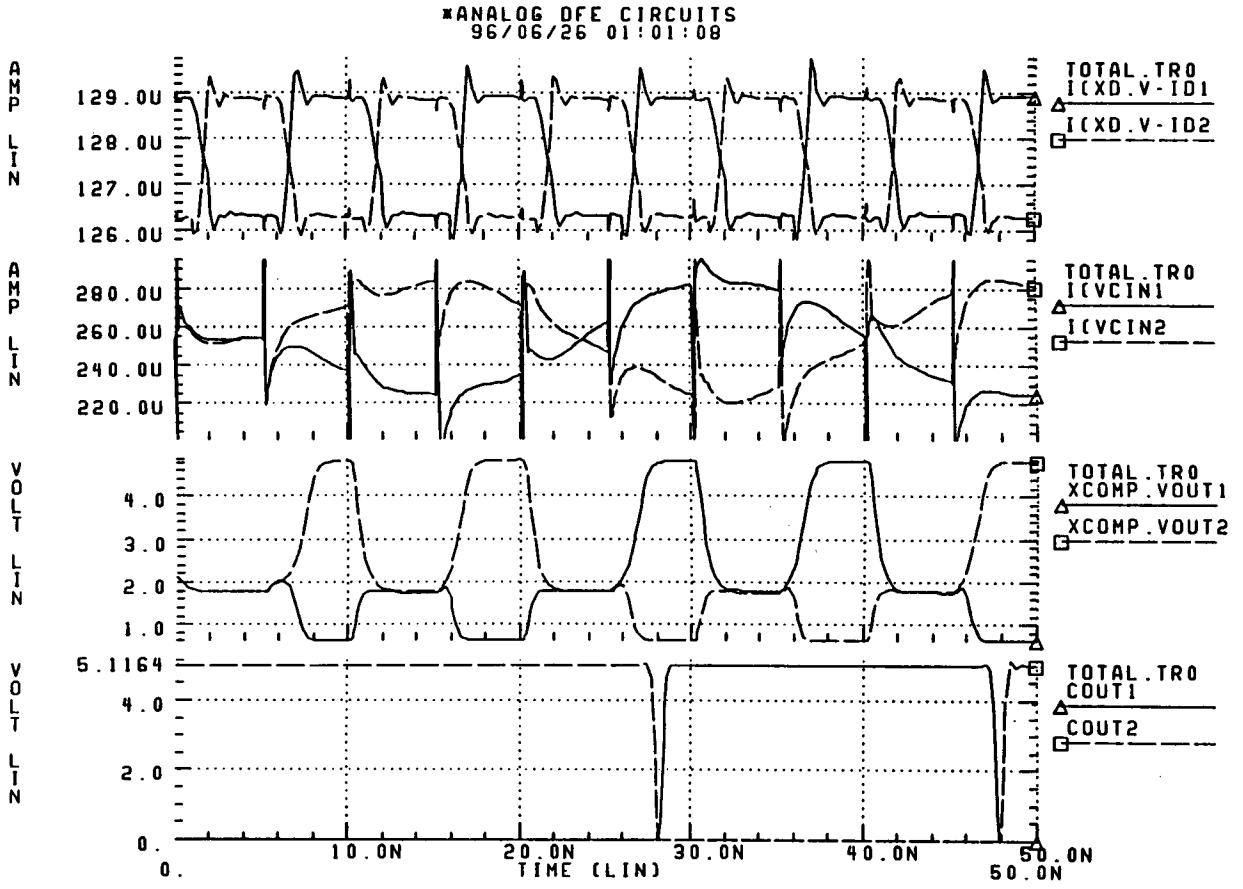

Fig 5.2 Simulated results of the DFE with a small DAC output

5.2 Layout

The layout of the presented circuits has been carefully conducted. An inter-digitized technique has been frequently used to make the matched transistors. Appendix 1 presents the layout of the V-to-I converter and the summing circuit. Appendix 2 gives the layout of the comparator. Appendix 3 shows the layout of the DAC. The overall layout of the proposed circuits is given in Appendix 4.

5.3 Summary

The design and layout of the analog DFE has been presented in this thesis. The performance of the DFE system based on the building blocks has been simulated, and a set of optimized feedback coefficients have been obtained. The overall performance of the DFE can be checked by simply using the optimized coefficients directly when the chip is ready for test.

5.4 Future Work

The DFE system built here is a simplified version. A complete DFE should include the forward filter implemented by using a biquard continuous-time filter, and the feedback equalizer coefficients must be adaptable based on the LMS algorithm.

The system accuracy may be increased by inserting a differential current amplifier between the V-to-I converter and the comparator. This will increase the resolution in the comparator while the power dissipation remains at the same level.

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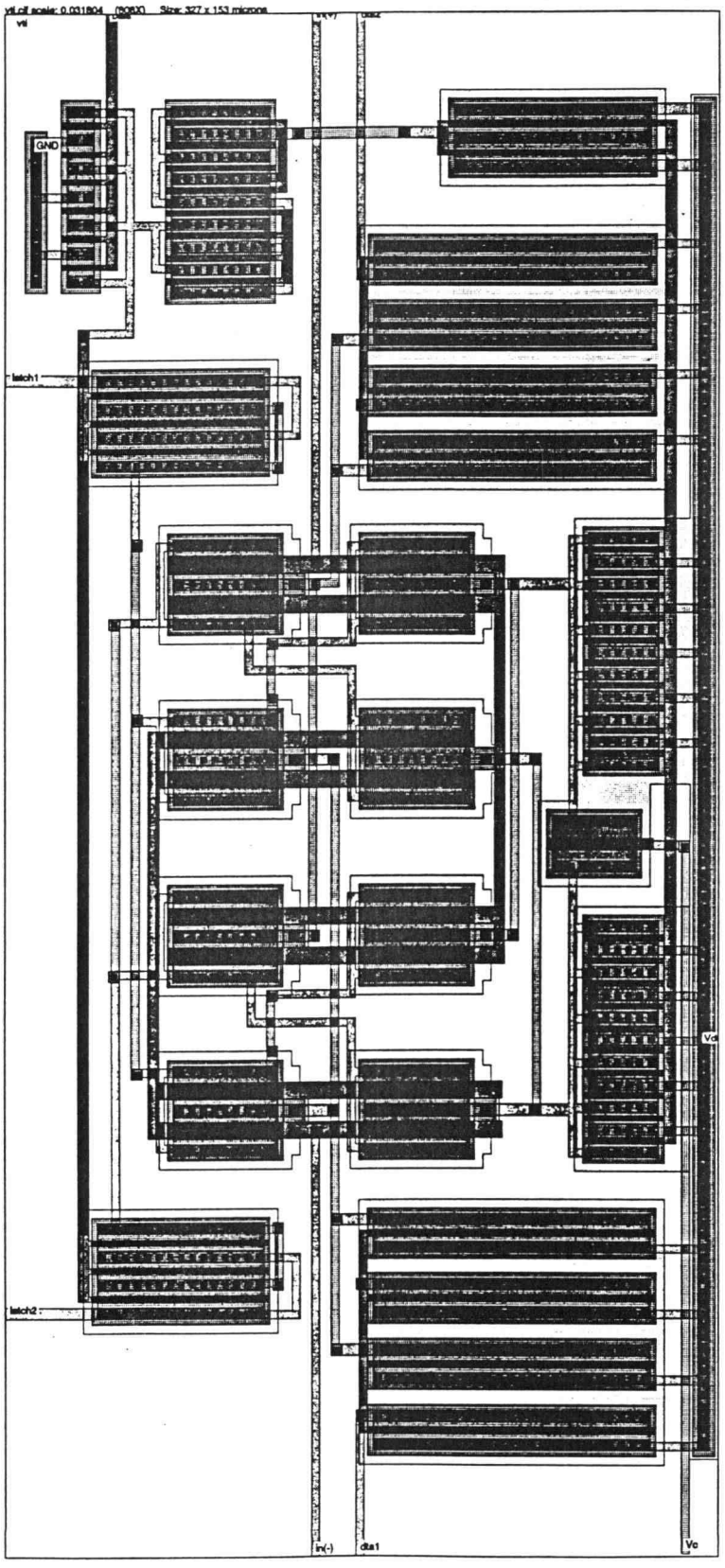
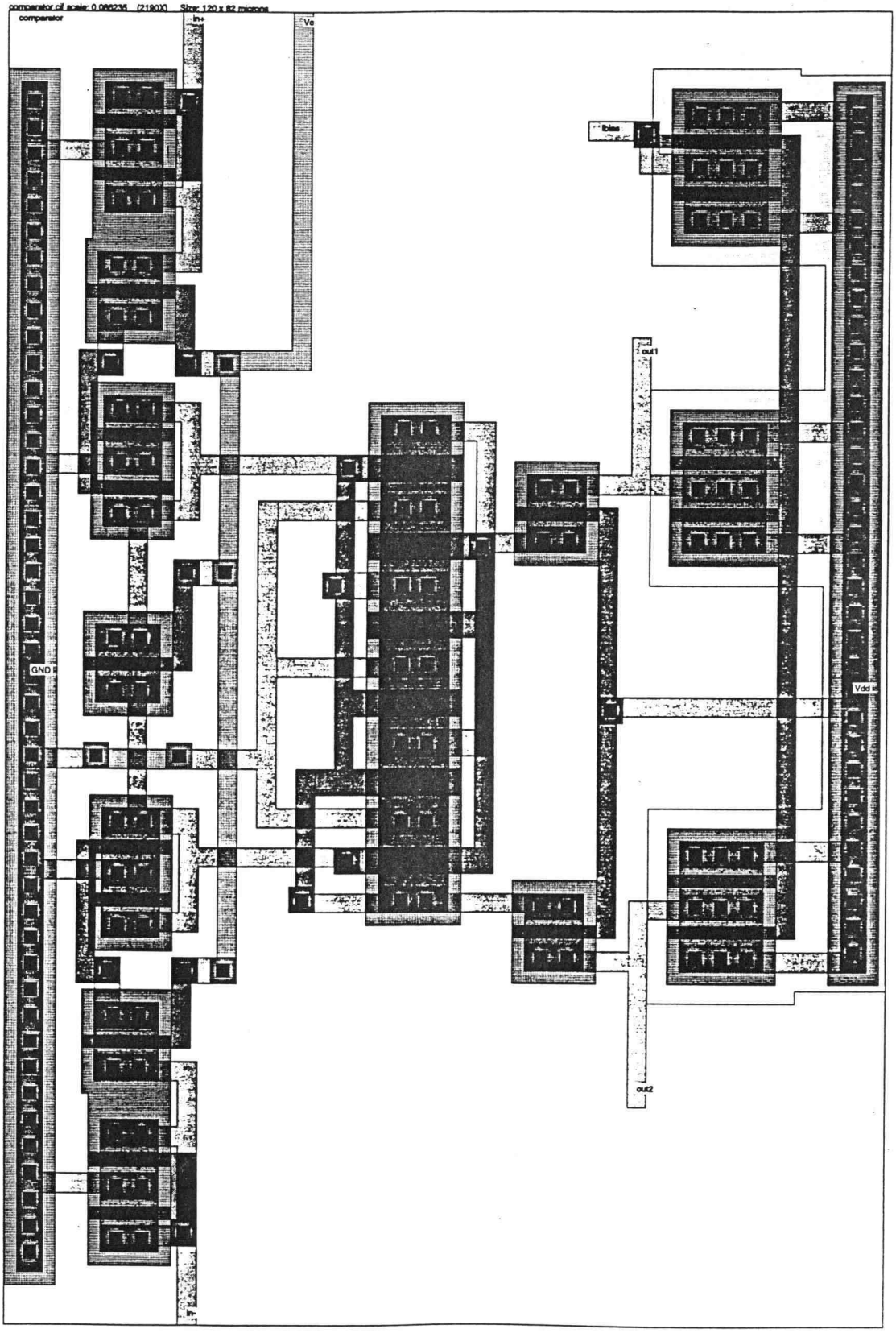
Appendices

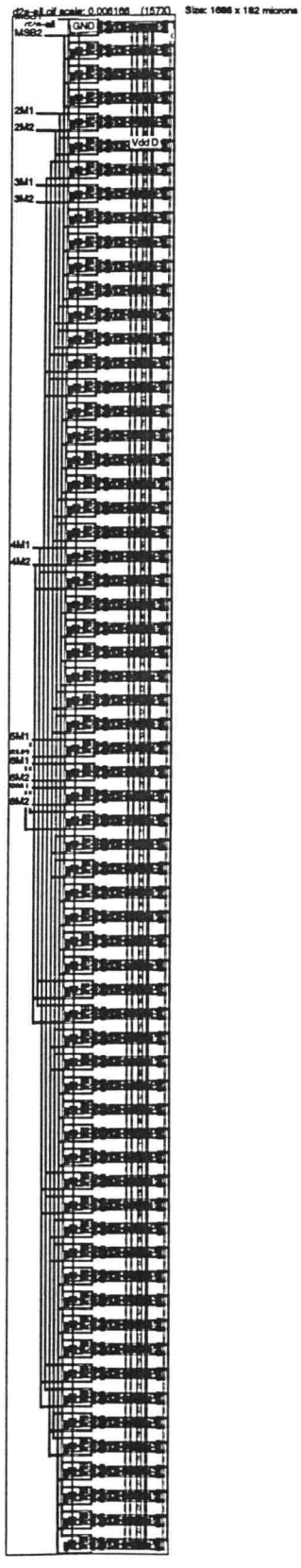
Appendix 1. Layout of the V-to-I Converter and the Summing Circuit



Appendix 2. Layout of the Comparator



Appendix 3. Layout of the DAC



Appendix 4. Layout of the Analog Circuits in the DFE