AN ABSTRACT OF THE THESIS OF

Donald W. Schulte For the degree of Master of Science in Electrical and Computer Engineering presented on August 14, 1992.

Title: Growth, Fabrication and Testing of Pseudomorphic P-channel GaAs/InGaAs/AlGaAs MODFETS.

Redacted for Privacy

Approved: _____
John R. Arthur, Advisor

Redacted for Privacy

_____
Stephen M. Goodnick, Co-Advisor

This thesis reports on the growth and characterization of p-type pseudomorphic AlGaAs/InGaAs/GaAs modulation doped field effect transistor (MODFET) structures. A series of different p-type MODFET structures were grown with a systematic variation of the indium mole fraction and quantum well width of the InGaAs channel region. Extensive characterization of these samples using van der Pauw Hall and photoluminescence measurements showed clear trends in carrier mobility and quantum well quality with respect to the structure of the InGaAs region. From this an optimal indium mole fraction and quantum well width were obtained.

Subsequent to material characterization, MODFET devices were fabricated and characterized. The measured DC device performance was reasonable and suggests that high quality p-type MODFETS should be obtainable with a properly optimized device structure and fabrication process.

Growth, Fabrication and Testing of Pseudomorphic P-channel GaAs/InGaAs/AlGaAs MODFETS.

by

Donald W. Schulte

A THESIS

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Master of Science

Completed August 14, 1992

Commencement June 1993

APPROVED:

Redacted for Privacy

Professor of Electrical and Computer Engineering in charge of major.

Redacted for Privacy

Professor of Electrical and Computer Engineering, Co-Advisor.

Redacted for Privacy

Head of Department of Electrical and Computer Engineering.

Redacted for Privacy

Dean of Graduate School

Date thesis is presented August 14, 1992

Typed By Donald W. Schulte

ACKNOWLEDGEMENTS

I would like to extend my thanks to a number of people who have helped me attain this goal. Special thanks to my major professor John Arthur and to my Co-advisor Stephen Goodnick, both of whom have provided me with guidance and insight. Equally important was the patient guidance of Leon Ungier and John Ebner who taught me the art of epitaxial crystal growth.

I would also like to thank my mother and family who have supported and encouraged me throughout my studies.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Growth, Fabrication and Testing of Pseudomorphic P-channel GaAs/InGaAs/AlGaAs MODFETS.

1. Introduction

The rapid advancement of semiconductor technology and ever greater complexity of semiconductor devices have placed increasing demands upon the materials used in their manufacture. These increased demands have driven the search for new semiconductor materials.

One important area in the field of semiconductor materials research is that of epitaxial growth. Epitaxial growth of semiconductor materials can be divided into two distinct categories. The first category is the epitaxial growth of a crystalline semiconductor upon a substrate of the same material to form a homogenous semiconductor material. An example of this would be the epitaxial growth of silicon upon a silicon substrate. The second category is the growth of one semiconductor material upon a substrate of a dissimilar material, commonly referred to as heteroepitaxy. An extremely important subcategory of heteroepitaxy, and principle area of interest for the present work, is the heteroepitaxial growth of III-V compound semiconductors.

When two dissimilar semiconductors are grown upon each other, the interface between the two materials is referred to as a heterointerface. Since the material properties of different semiconductors are not the same, abrupt changes in material properties can occur at a heterointerface. This can be used to create a new class of materials with properties unavailable in homogenous semiconductors.

One of the most important material properties that can be altered by heteroepitaxy is the bandgap of a semiconductor. Since differing semiconductor materials normally have different bandgaps, a potential discontinuity must appear in the conduction and valence bands at the heterointerface in order to accommodate the bandgap difference between the two materials. By growing semiconductor materials with one or more heterointerfaces, the bandgap discontinuities which result at each heterointerface can be used to create new semiconductor structures with novel bandstructures and new properties.

The study of the material properties of AlGaAs/GaAs and AlGaAs/InGaAs/GaAs heterostructures is the primary concern of this work. The principle heterostructure investigated in this work is the structure used for the Modulation Doped Field Effect Transistor or (MODFET), also referred to as a Two Dimensional Electron Gas Field Effect Transistor (TEGFET), Selectively Doped Heterostructure Transistor (SDHT), or High Electron Mobility Field Effect Transistor (HEMT). The MODFET structure takes advantage of the excellent transport characteristics of carriers confined at a heterointerface between two materials such as GaAs and AlGaAs. The carriers confined at such an interface form a quasi two dimensional system, and through proper design of the heterostructure, extremely large mobilities and carrier velocities can be obtained.

The existence of a charge accumulation layer at a heterointerface was first predicted by Anderson in 1960[1]. Esaki and Tsu[2] later predicted that carrier mobility could be enhanced by modulation doping which would result in spatially

separating carriers from their parent impurity atoms. It was not until 1978 that Dingle et al.[3] first observed enhanced electron mobilities in a two dimensional electron gas confined in a GaAs-AlGaAs superlattice structure. The first transistor to utilize this enhanced mobility was later fabricated by Mimura et al.[4] in 1980. Since that time, several groups have fabricated similar devices with increasingly improved performance, and HEMT circuits are now commercially available.

Even though large advances have been made in MODFET technology, almost all successful results have been obtained with n-type MODFETS, and thus MODFET circuits are still primarily limited to enhancement depletion technology. Since enhancement depletion technology has several undesirable characteristics such as low output voltage swing and high static power dissipation, much research has been done to design a complementary circuit technology to overcome some of these problems.

In order to design complementary logic circuits, which have several advantages such as reduced power consumption and increased voltage swing, a high quality p-type MODFET which relies on confinement of holes in the valence band is needed. The first observation of a confined two dimensional hole gas at a heterointerface was reported by Störmer and Tsang[5] in 1980 in an AlGaAs-GaAs heterojunction. In 1984 Störmer and his coworkers managed to fabricate the first AlGaAs-GaAs MODFET based upon a two dimensional hole gas.[6] Since this time, several other groups have successfully fabricated p-type MODFETS and the performance of these devices continues to improve.

Unfortunately the performance of p-type MODFETS fabricated to date is

significantly inferior to n-type MODFETS. The current performance of p-type MODFETS severely limits their use in circuit applications. One of the primary limiting factors of p-type MODFETS based on the AlGaAs-GaAs materials system is the low hole mobility in GaAs. Since InGaAs has a much larger hole mobility and smaller bandgap than GaAs, the AlGaAs\InGaAs\GaAs material system has been extensively studied in an attempt to improve p-channel MODFET performance.

InAs and GaAs have a lattice mismatch of approximately 7%. However, it has been shown by Matthews and Blakeslee[7][8][9] that high quality interfaces can be grown between mismatched semiconductors if the thickness of one layer is below a critical thickness which depends on the mismatch. If an $In_YGa_{1-Y}As$ layer is grown thin enough, the lattice mismatch will be absorbed as strain in the $In_YGa_{1-Y}As$, causing the $In_YGa_{1-Y}As$ lattice constant to conform to the lattice constant of the GaAs substrate, yielding a pseudomorphic $In_YGa_{1-Y}As$ layer. The uniaxial distortion in the pseudomorphic InGaAs layer causes a splitting of the normally degenerate valence band light and heavy hole bands, raising the light hole band above the heavy hole band. This splitting should allow a large number of carriers to reside in the light hole band and an increase in mobility should be possible due to the much lighter effective mass of holes in this band.

The present goal of this research is to investigate the dependence of hole mobility and material properties upon the indium mole fraction Y in p-type pseudomorphic $In_YGa_{1-Y}As$ MODFETS. To accomplish this goal, several samples containing varying indium concentrations and layer thicknesses were grown using the

Molecular Beam Epitaxy (MBE) facility at Oregon State University. The material quality of these samples was then characterized using photoluminescence and van der Pauw Hall measurements. Concurrent with the growth and testing of the sample material, a device process and photolithographic mask set were designed to allow fabrication of p-type MODFETS from this material. Using this process and mask set, several working p-type MODFETS have been fabricated using the facilities at Oregon State University and further device fabrication and testing is ongoing.

2. MODFET Design and Relevant Literature

The work done for this project can be separated into two major areas of importance. These are the design of MODFET device structures, and the growth of III-V compound semiconductors by Molecular Beam Epitaxy (MBE). The area of device design is clearly of great importance since the desired device properties dictate the layer structure that must be grown. Once the layer structure has been designed, the material growth must be carefully considered in order to insure that a high quality sample may be grown.

As outlined in the introduction, the first n-type MODFET was fabricated by Mimura et. al. in 1980[4], followed shortly by the first p-type MODFET made by Störmer and his coworkers in 1984[6]. Since this time, many groups have fabricated MODFETs and studied their device structures. These studies have yielded a variety of MODFET device structures and an abundance of information about MODFETs. Therefore, it is necessary to analyze carefully the relevant literature to optimize the MODFET structure to obtain the desired device performance. In this section, the particular device structure used for this work and the relevant literature used to arrive at this structure will be reviewed.

2.1 Design of MODFET Device Structures

The general structure of a MODFET consists of four basic regions, the active region or channel, the spacer layer, the barrier and doping layers, and the cap layer. The active region of a MODFET consists of a small bandgap material which is undoped. A heavily doped material of larger bandgap is then grown upon the active region. Due to the discontinuity in charge present at the heterointerface, carriers will transfer from the doped side into the active region in order to align the equilibrium fermi level. The result is a charge accumulation layer near the heterointerface as was predicted by Anderson[1]. The ionized impurities in the doped layer and the charge in the active region create large internal electric fields, and pronounced band bending occurs. This large bandbending in conjunction with the bandgap discontinuity at the heterointerface results in quantum mechanical size confinement. The quantum confinement causes the formation of discrete energy levels which the carriers occupy. This effect confines the charge in the active layer to a region which is only a few tens of angstroms in width in the direction perpendicular to the heterointerface, forming a quasi two dimensional system.

Since the active region is undoped and the charge is well confined in this region, scattering due to impurities is greatly reduced and large carrier mobilities can be achieved. This mobility enhancement is much more pronounced at low temperatures where ionized impurity scattering is a dominant factor limiting carrier mobility. As predicted by Esaki and Tsu[2], the addition of a spacer layer of undoped

material between the doping and the active region will increase the mobility of the carriers in the active region. This increase occurs due to the physical separation of the parent impurity atom and carrier, which reduces the strength of the scattering potential. This enhanced mobility was first shown by Dingle et. al.[3] for electrons in a AlGaAs/GaAs heterostructure and later Störmer and Tsang[5] demonstrated a similar mobility enhancement for holes in a AlGaAs/GaAs heterostructure.

It has been clearly shown that the carrier mobility in MODFET structures increases as the spacer layer thickness increases[10]. However, for device applications, large carrier mobility is not the only factor which must be considered. It has been shown that in addition to the spacer width affecting the carrier mobility, the transconductance of a MODFET is also affected by the spacer width[11]. The peak transconductance in a MODFET decreases as the spacer layer thickness increases due to the onset of parallel conduction in the AlGaAs, a trend which is opposite to the trend in mobility versus spacer layer width. Therefore, there is a tradeoff which must be made between mobility and achievable transconductance.

Another important consideration in MODFET design is the thickness and doping concentration needed in the doping layer. Two specific variations are currently used to form the doping layer in MODFETs. The first is the uniform doping method in which the impurity concentration in the entire doped region is a constant. In this type of doping scheme, the thickness and concentration of the layer need to be designed to allow adequate charge transfer to the active region while minimizing the amount of charge trapped in the doped region itself, since charge

trapped in the doped region leads to undesirable parasitic effects. In the second method, a very narrow spike of highly doped material is used to provide carriers to the active region. This method is called pulse or delta doping, and in the extreme limit, a partial monolayer of impurity atoms at the edge of the spacer layer is used. When delta doping is used, the charge transfer efficiency into the active layer is improved, and higher carrier concentrations in the active region can be obtained than can be achieved with uniformly doped structures. This effect was first shown in delta doped MODFETs by Schubert et al.[12] where it was shown that the two dimensional carrier concentration in the active region could be increased from $1.04x10^{12}/cm^2$ to $1.96x10^{12}/cm^2$ by using a delta doping technique. It was also shown in a later work by Jaffe and Singh[13] that parasitic effects due to excess charge in the doping and barrier layer could be reduced by using a delta doped MODFET instead of a uniform doped MODFET.

2.2 MBE Growth of MODFET Structure

For this work, AlGaAs/GaAs and AlGaAs/InGaAs/GaAs MODFET structures were fabricated. In these structures, the spacer and doping layers are $Al_XGa_{1-X}As$, and the channel is either GaAs or $In_YGa_{1-Y}As$, where X and Y are the mole fraction of aluminum and indium respectively. Due to the highly reactive nature of AlGaAs, a cap of GaAs is grown on top of the AlGaAs to protect the structure, and facilitate ohmic contact formation.

A typical n-type MODFET structure consists of an undoped GaAs active layer, followed by a 50-150Å spacer layer of undoped $Al_{0.3}Ga_{0.7}As$. A 400-500Å layer of $1x10^{18}$ Si doped $Al_{0.3}Ga_{0.7}As$ is grown followed by a thin highly Si doped GaAs cap layer. The first p-type MODFET structure was an AlGaAs/GaAs MODFET fabricated by Störmer and his coworkers[6], and is very similar to the n-type MODFET structure. Their device structure consisted of an active region of undoped GaAs, followed by a 200Å layer of undoped $Al_{0.7}Ga_{0.3}As$, a 450Å thick layer of $2x10^{18}$ Be doped $Al_{0.7}Ga_{0.3}As$, and a 50Å cap layer of Be doped GaAs. The first apparent difference between the two structures is the mole fraction of aluminum present in the spacer and doping layers. This difference is due to the fact that n-type AlGaAs exhibits serious trap problems due to deep level DX centers for aluminum mole fractions exceeding approximately 30%. A similar trap level has not been observed in p-type AlGaAs, and thus allows a larger mole fraction of aluminum to be used. Since the bandgap of $Al_XGa_{1-X}As$ increases with the mole fraction X, better quantum

confinement of carriers at a heterointerface can be achieved by increasing the mole fraction of aluminum. This fact is especially important in p-type MODFET structures since the valence band offset is much smaller than the conduction band offset, and thus quantum confinement effects are weaker for holes than for electrons at a given aluminum mole fraction.

Another important difference between n and p type MODFETS is the relatively poor mobility of holes in GaAs. In an attempt to improve the hole mobility, the use of strained InGaAs for the channel layer has been investigated. The growth of InGaAs on GaAs is much more difficult than the growth of AlGaAs on GaAs, since InAs has a larger lattice constant than GaAs while the lattice constant of AlAs is very well matched to that of GaAs. The mismatch in lattice constants between $In_YGa_{1-Y}As$, and GaAs can lead to the formation of dislocation defects which may seriously degrade device performance. However, high quality crystals of $In_YGa_{1-Y}As$ can be grown based on the theory of Matthews and Blakeslee[7][8][9]. This theory states that high quality epitaxial crystal material can be grown on a substrate having a significantly different lattice constant if the thickness of the epitaxial layer is thin enough. Thus, if the layer of material is sufficiently thin, it is energetically favorable for the mismatch in lattice constants to be absorbed as layer strain rather than in misfit dislocation formation. The presence of strain in the InGaAs layer causes the lattice constant of the InGaAs to conform to the lattice constant of the GaAs in the directions parallel to the interface and elongate in the direction perpendicular to the interface as shown in figure 1. Since the strained

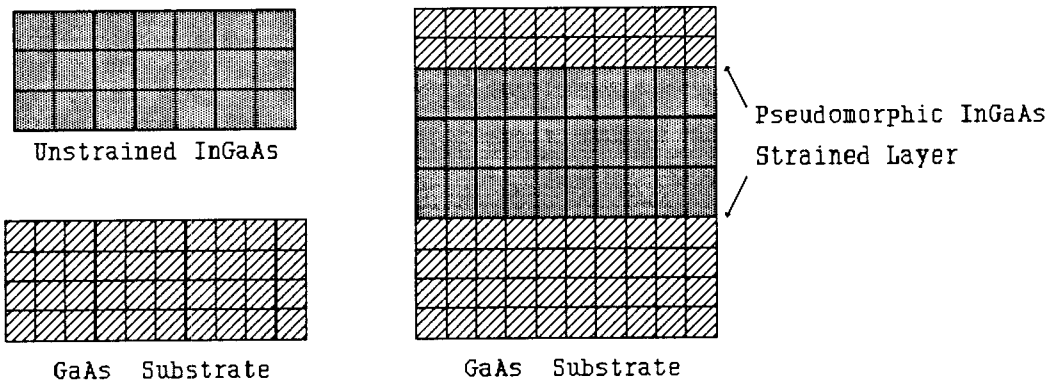

FIGURE 1
Pseudomorphic InGaAs

InGaAs lattice constant conforms to the lattice constant of the substrate, this material is referred to as pseudomorphic material. If the thickness of the layer becomes too large, misfit dislocation formation becomes energetically favorable, and the lattice constant of the InGaAs will relax to its unstrained value. The critical thickness at which the relaxation of strain occurs is dependant upon the mole fraction Y of indium present in the layer. As the indium mole fraction increases, the critical thickness for misfit dislocation formation decreases. Based on the work of Anderson[14], a curve showing the dependance of critical thickness upon indium composition is shown in figure 2 on page 13.

Due to the strain present in pseudomorphic InGaAs, the band properties of the valence band are altered. The normally degenerate light hole and heavy hole states in the valence band are split when strain is present raising the light hole band above the heavy hole band. This splitting can lead to mobility enhancements due to greater occupancy of the light hole band which has a significantly smaller hole mass

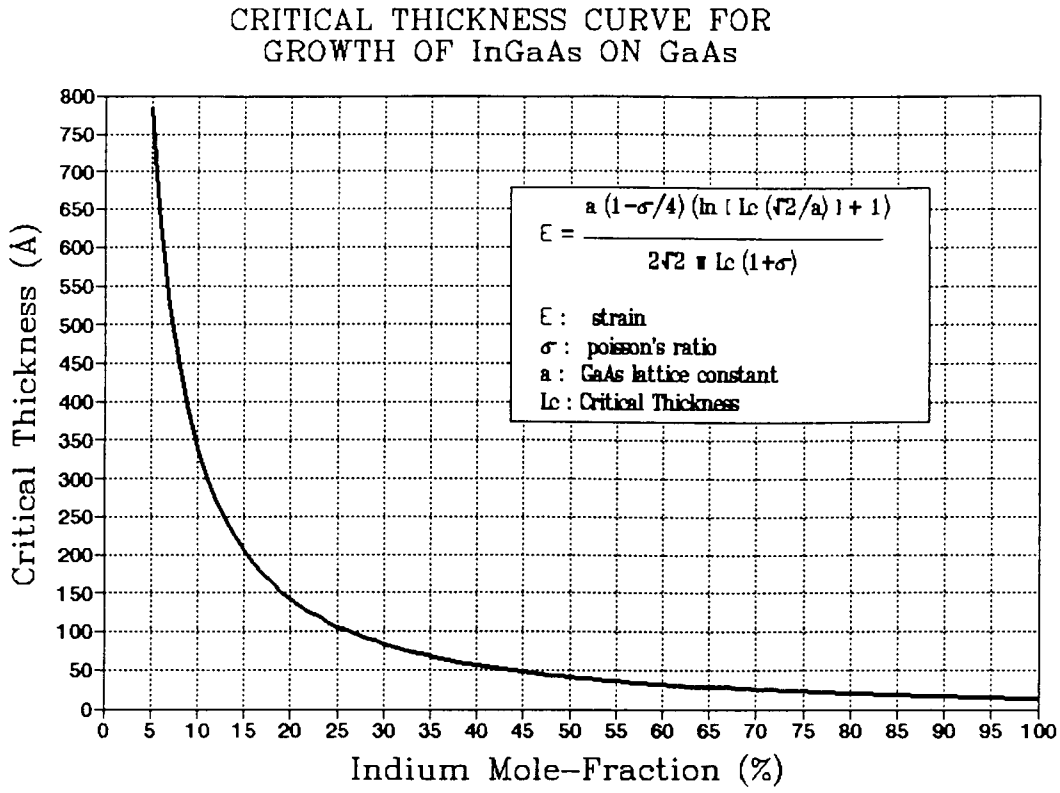

FIGURE 2
Critical Thickness Curve For Growth of InGaAs on GaAs

than the heavy hole band. The enhancement of mobility due to strain effects in InGaAs was first observed by Schirber et al.[15] in an InGaAs/GaAs structure. In addition to the strain splitting in pseudomorphic InGaAs, the hole mass of InGaAs is smaller than the hole mass of GaAs, and the bandgap of InGaAs is smaller than the bandgap of GaAs. Therefore, quantum confinement is improved with the use of an InGaAs channel due to the reduced bandgap, and the lighter hole masses and strain effects present in InGaAs make this a promising material for p-channel MODFETs.

In the present work, it was decided to investigate the dependance of p-type

MODFET material properties upon the mole fraction of indium present in the active region and the thickness of this layer. In order to accomplish this goal, eight samples were grown with differing indium compositions and layer widths. The widths and mole fractions used were 10% In and 50Å, 100Å and 150Å quantum wells, 20% In and 50Å, 100Å and 150Å quantum wells, 30% In and a 50Å quantum well and a control sample with a GaAs active layer.

For the spacer layer and doping layer, $Al_{0.5}Ga_{0.5}As$ was used to improve quantum confinement of holes at the heterointerface. After carefully considering the tradeoff between transconductance and mobility versus spacer layer thickness, and a careful review of the previous structures fabricated it was decided to use a 50Å spacer layer for these devices. It was then decided to use a delta doping technique for these devices due to the reduction of charge storage in the barrier layer and increased charge transfer efficiency that this doping technique yields. In order to aid the formation of Schottky barriers and reduce gate leakage, it was decided to grow another 400Å of undoped $Al_{0.5}Ga_{0.5}As$ on top of the delta doping plane. Finally, in order to protect the $Al_{0.5}Ga_{0.5}As$ surface and aid ohmic formation, a 200Å layer of undoped GaAs was grown on top of the AlGaAs layer. This 200Å GaAs cap layer was grown undoped in order to prevent excessive gate leakage current. Although the layer was undoped, it was assumed that fabrication of ohmic contacts would not be a problem since the active channel was only 650Å from the GaAs surface.

3. Experimental Work

For this work, a series of AlGaAs/$In_YGa_{1-Y}As$/GaAs p-type modulation doped heterostructures were grown, and characterized. The mole fraction of indium and quantum well width used in each structure was systematically varied in order to determine the effects of these variables on material properties. Subsequent to the characterization of these heterostructures, one sample was processed into MODFET devices and tested to demonstrate the viability of fabricating useful transistors from this heterostructure material. This work can be divided into four main stages:

1) Epitaxial growth of the substrate material.
2) Characterization of the epitaxially grown material.
3) Fabrication of devices from this material.
4) Characterization of the completed devices.

Each of these topics will be discussed in detail in the following pages.

3.1 Material Growth

The MODFET material used in this work was grown by Molecular Beam Epitaxy (MBE) using a Perkin Elmer Phi model 425-B Molecular Beam Epitaxy system. This system consists of two ultra high vacuum chambers and an introduction chamber to facilitate transfer of samples between atmospheric conditions and the ultra high vacuum environment of the analysis and growth chambers. The analysis chamber contains a heater for outgassing samples previous to growth, and a Phi 545 Scanning Auger Microscope for surface characterization. The Growth chamber

contains seven source ovens (2 Ga, 1 Al, 1 In, 1 Be, 1 Si, and 1 As), Reflection High Energy Diffraction (RHEED), a UTI 100C Quadropole Mass Spectrometer and an IRCON optical pyrometer to allow in-situ characterization of the material and growth conditions.

To insure that quality epitaxial material can be grown, it is necessary to use extremely pure source material, since even small amounts of impurities in the sources can render the epitaxial material useless. Therefore, the source materials used in the MBE system are the purest available to us at the present time. The manufacturer and purity of each source is listed in table 1 below.

Table 1 - MBE source materials and purity.

Material	Manufacturer	Purity
Indium	- United Mineral & Chemical Co.	99.99999%
Gallium	- Alcam Electronic Materials	99.999999%
Aluminum	- Johnson Matthey	99.9999%
Arsenic	- Furokawa Inc.	99.999999%
Beryllium	- Atomergic Chemical Company	99.9999%
Silicon	- SEH America (seed cryst. matl.)	Unknown

The source material is evaporated thermally from solid source crucibles and the flux rates are controlled by the crucible temperature. Each source oven is shuttered to enable the flux from each oven to be rapidly turned off or on. Since the operation time for the shutters is small compared to the growth rates used, abrupt interfaces can essentially be made in either doping or material composition. More gradual changes in composition can be made by slowly ramping the temperature of a source oven to change its flux. The oven temperature and flux rate to obtain a

specific growth rate is calibrated using the standard method of Reflection High Energy Electron Diffraction (RHEED) oscillation measurement[16]. This is accomplished by measuring the intensity of the RHEED diffraction pattern, which has been shown to oscillate with a period equivalent to the growth of one atomic monolayer.

All layers, except for the InGaAs layers, were grown at a growth rate of one monolayer per second, where one monolayer is defined as a combined layer of gallium and arsenic atoms. The indium layers were grown at growth rates less than one monolayer per second in order to control the In mole fraction in the $In_YGa_{1-Y}As$ layers, due to the difficulty in calibrating the $In_YGa_{1-Y}As$ growth rates for larger indium mole fractions than $Y=0.05$.

The growth rate of indium was calibrated at 0.05 monolayer/sec by monitoring the RHEED oscillations during growth. This growth rate was obtained by calibrating the GaAs growth rate at 0.95 monolayer/second and then finding the indium set point that increased the growth rate to 1 monolayer/second when the indium shutter was opened. Once the growth rate of indium was set to 0.05 monolayer/second, the gallium flux was then adjusted to give the desired indium composition. For example, a 0.05 monolayer/second indium growth rate and a 0.45 monolayer/second Gallium growth rate yields $In_{0.1}Ga_{0.9}As$ at a 0.5 monolayer/second overall growth rate.

The actual layer structure used for fabrication of p-channel MODFET devices is shown in figure 3 on pg 18. First, a 0.5um GaAs buffer was grown at 585°C to improve the surface quality of the substrate. Two minutes before the end of the

GaAs CAP – UNDOPED 200Å
$Al_{0.5}Ga_{0.5}As$ BARRIER – UNDOPED, 400Å
Be PLANAR DOPING ~ 6E12/cm^2
$Al_{0.5}Ga_{0.5}As$ SPACER – UNDOPED, 50Å
$In_XGa_{1-X}As$ QUANTUM WELL, 50Å, 100Å, 150Å
SUBSTRATE – SI GaAs

FIGURE 3
P-type MODFET device structure.

buffer layer growth, the substrate temperature was lowered from 585°C to 510°C in preparation for the growth of the InGaAs quantum well. At the end of the buffer layer one of the series of $InGa_{1-Y}As$ quantum wells was grown at 510°C. The actual widths (W) and compositions of the indium quantum wells were as follows: X=0 (control); X=0.1, W=5nm, 10nm, & 15nm; X=0.2, W=5mn,10nm, & 15nm; and X=0.3, W=5nm (see figure 4, pg. 19). These values were selected such that all quantum well widths were less than the critical thickness for misfit dislocation formation as determined by the theory of Matthews and Blakeslee[7][8][9]. After the InGaAs quantum well layer, a 5nm undoped $Al_{0.5}Ga_{0.5}As$ spacer layer was then grown. 1.6nm of this spacer were grown at 510°C and then growth was stopped and the substrate temperature was raised to 585°C before the remaining 3.4nm of the AlGaAs spacer were grown. No further growth interruptions were used and the growth temperature

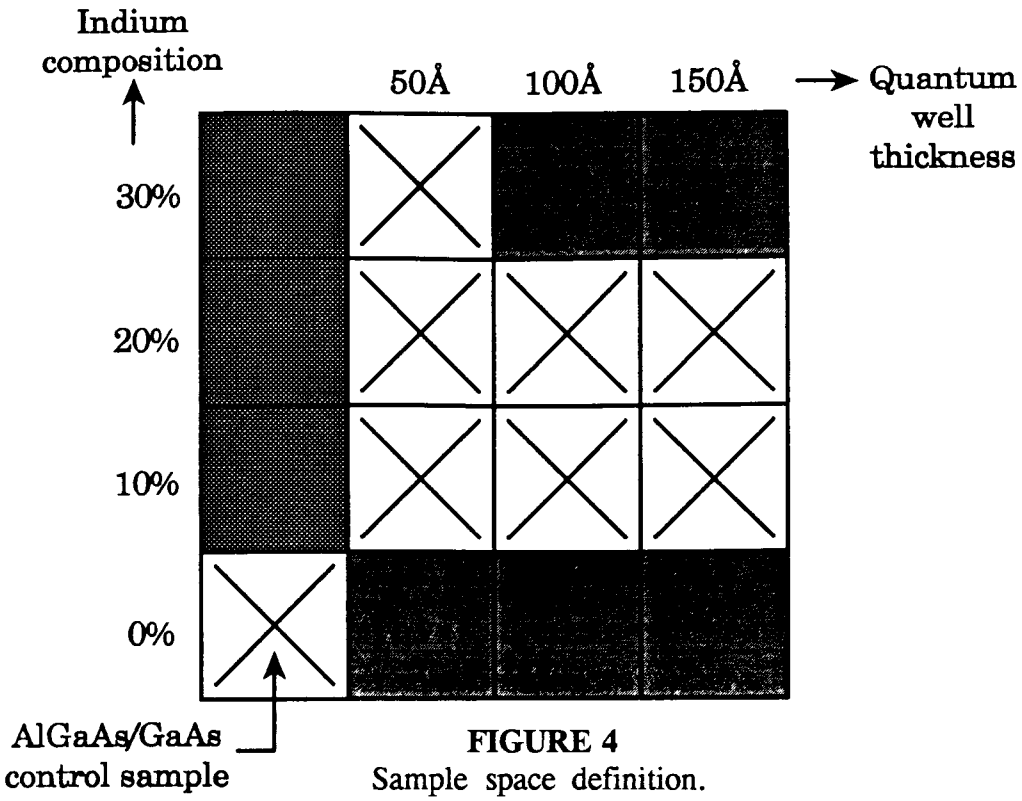

FIGURE 4
Sample space definition.

was kept at 585°C for the remainder of the growth. After the 5nm AlGaAs spacer was completed a doping layer was grown. A planar doping technique (also called delta doping) was used for the doping in this structure. This growth was accomplished by closing all shutters except for the beryllium and arsenic shutters, which were left open for 0.3 minutes at a temperature which would yield a doping density of $7x10^{18}$ cm^{-3} during normal growth of GaAs at one monolayer per second growth rate. These conditions resulted in a plane of acceptor atoms with a sheet density of approximately $4x10^{12}$ cm^{-2}. After the delta plane was grown, another 40nm of undoped $Al_{0.5}Ga_{0.5}As$ was grown as a barrier layer. The structure was then finally capped with 20nm of undoped GaAs to passivate the surface and protect the AlGaAs from degrading.

3.2 Material Characterization

After the MBE sample growth was completed the sample quality of each sample was characterized using the photoluminescence and van der Pauw Hall measurement facilities at Oregon State University.

3.2.1 Photoluminescence Characterization.

In photoluminescence, an optical source having an emission energy larger than the bandgap of the material to be characterized is used to illuminate the sample. This illumination causes electron-hole pairs to be generated in the sample. These carriers then rapidly thermalize to various allowed states in the semiconductor (ie. conduction band minima, valence band maxima, impurity levels, etc.), where they then can recombine. When this recombination occurs radiatively, the emitted photons have an energy which is equal to the difference between the energy levels involved in the transition. Therefore, peaks in the luminescence spectrum emitted by a sample indicate what energy levels are present in the sample. Since the quality of the crystal greatly affects the nonradiative recombination rate, the relative brightness, spectral width, and energy of the emitted peaks are good indicators of the material quality.

In heterostructures, the presence of bandgap discontinuities allows quantum confinement of carriers in the direction perpendicular to the interface. Using

elementary quantum mechanics, it can be shown that quantum confined structures (i.e. square or triangular potential wells) cause discrete allowed energy levels to form. For example, in the classic quantum mechanics problem of an infinitely deep square potential well of width a (figure 5a), the energy levels are given by $E=n^2\pi^2h^2/2m^*a^2$ [17]. The actual energy levels for quantum wells which do not have infinite potential barriers and are more complicated in shape such as finite square[18] and triangular[19] potential wells (figure 5b), usually must be solved using numerical methods since no closed form analytical solution exists for these.

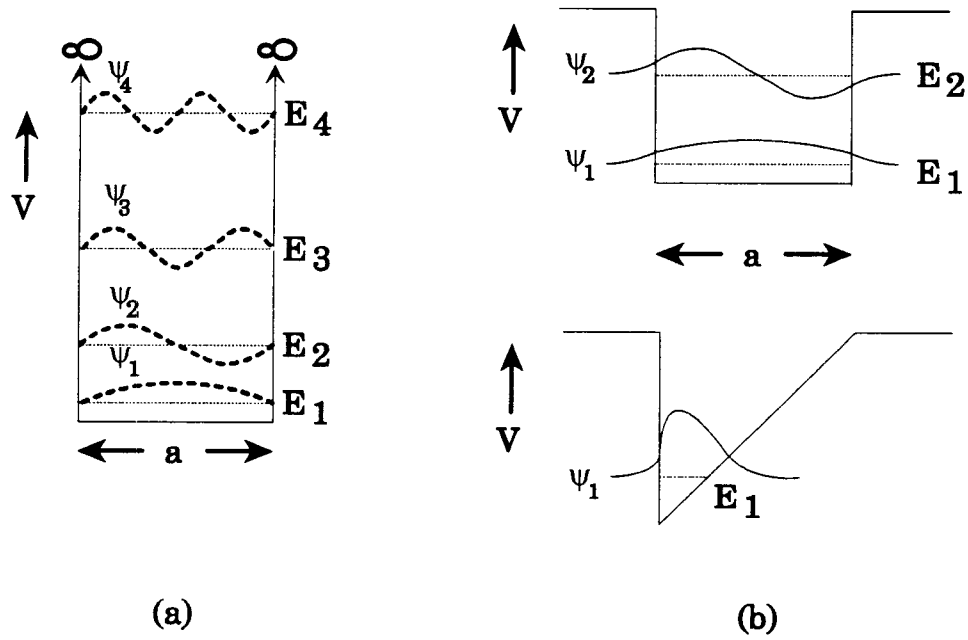

FIGURE 5
Various quantum well structures.

Radiative transitions also occur between the discrete energy levels present in quantum confined structures. The luminescence peaks emitted from a quantum confined energy level usually have a very narrow full width at half maximum due to the two dimensional density of states which is nonzero at k=0. The relative brightness of luminescence from quantum structures is usually much brighter than luminescence from bulk semiconductor material for this same reason. However, the linewidth and intensity of the emitted light can be affected adversely by roughness at the heterointerfaces, poor material quality, or weak quantum confinement.

Since the many nonradiative processes, such as phonon emission or absorption, are strongly temperature dependent, samples are usually cooled as near to 0K as possible. In addition to reducing nonradiative effects, cooling the sample reduces the thermal noise ($\approx 4k_bT$) and allows observation of shallow transitions which may not be observable at room temperature. For example, many donor and acceptor levels are only 5 to 30 meV from the respective band edge and would not be visible in a room temperature photoluminescence measurement.

The photoluminescence system at OSU consists of an American Laser Corporation argon ion laser with a peak emission of 40mW at 488nm. The samples are cooled to a temperature of approximately 20K with an Air Products closed cycle helium refrigeration system. This system consists of a cold finger where samples are mounted, a cryoshroud which can be evacuated to prevent condensation formation, and a temperature controller for monitoring and adjusting sample temperature. The cryoshroud contains optical ports to allow laser access to the sample. The laser is

focused on the sample using an optical rail with appropriate mirrors and lenses. The emission from the sample is then focused into a Jarrel-Ash 0.5m monochrometer which is connected to a photomultiplier for light detection. The photomultiplier is cooled using liquid nitrogen to eliminate thermal noise and improve efficiency. Data is then gathered with a leading edge IBM compatible computer outfitted with an A/D conversion board. A chopper and lock-in amplifier are used to reduce noise and improve measurement efficiency, and appropriate filters are used in the optical path to remove unwanted laser lines from the sample emission spectrum. Typical operating conditions are a sample temperature of 20K, laser power of 10 to 25 mW, and a 100V bias on the photomultiplier tube cooled to a temperature of -90°C.

3.2.2 Van der Pauw Hall Mobility Measurement

The MBE grown material was further characterized using the van der Pauw method to determine the sheet resistivity and Hall mobility. The van der Pauw method allows calculation of sheet resistivity to an arbitrarily shaped sample provided that the sample is uniformly thick, singly connected, and has sufficiently small contacts located on the periphery of the sample.[20] In addition to the sheet resistivity, this method can also be used to determine the Hall mobility of a sample.[21] Once mobility and sheet resistivity have been determined, the Brooks-Herring approximation can be used to find the concentration of ionized impurities.

Our test facility consists of an electromagnet capable of producing up to 8000

Gauss, a specially designed sample holder, and a small dewer which can be used to cool the sample to liquid nitrogen temperature. A Keithley model 220 programmable current source, and a model 181 nanovoltmeter interfaced through HPIB to a Hewlett Pacakrd 9836C computer were used for sample bias and voltage measurement. The test equipment was connected to the sample through a small external switch box designed to connect the contacts appropriately for the van der Pauw Hall measurement.

The samples used for testing were small squares (approximately 5mm square) of MBE grown MODFET material. Contacts were made using an indium-zinc alloy which was applied to each corner of the sample with an Antex soldering iron with an ultra fine 0.012 inch diameter tip in order to keep contact area as small as possible. The contacts were then annealed in a 450°C annealing oven in a forming gas ambient. The contacts were then checked to insure good ohmic contacts had been achieved. If ohmic contacts were judged too poor, a subsequent annealing was performed to attempt to improve the contact resistance. Samples which were annealed further were remeasured and discarded if the resistance of the ohmic contacts was still too large. After determining that a sample had adequate ohmic contacts, a van der Pauw Hall measurement was performed at 300K and 77K. This is accomplished by passing a known current through contact A and B, and measuring the resulting voltage at contacts C and D (see figure 6, pg. 25). This measurement is then repeated three more times by passing current through contacts C and D, A and C, and B and D, and measuring voltage at contacts A and B, B and D, and A

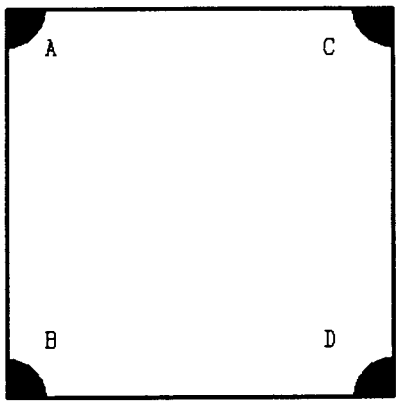

FIGURE 6
Van der Pauw test structure.

and C respectively. From these four measurements the resistivity of the sample can be determined. The hall mobility is then determined by applying a known current through contacts A and D, and B and C, and measuring the resulting voltage at contacts B and C and A and D respectively. This measurement is performed for both a positive and negative current in no magnetic field and then is repeated for both current polarities in a both a positive and negative magnetic field oriented perpendicularly to the sample. From the Hall mobility measurement and resistivity measurement, the sheet carrier concentration can then be determined.

3.3 Device Fabrication

The GaAs semiconductor processing done in this work involved two basic types of lithography. The first type of lithography is a liftoff metalization process. In the liftoff process, photoresist is spun onto the sample and then processed such that developing yields a profile like that shown in figure 7a. The sample is then exposed and developed, opening windows in the photoresist to define where metal is to be placed. After development the sample is cleaned and placed into a metal evaporator where metal is deposited over the entire surface. Due to the profile of the photoresist, the metal on the surface of the photoresist is not connected to metal deposited in the photoresist windows, as shown in figure 7b. Therefore, all metal on the photoresist surface is removed when the photoresist is removed, and only the metal deposited in the windows remains as shown in figure 7c. The second type of

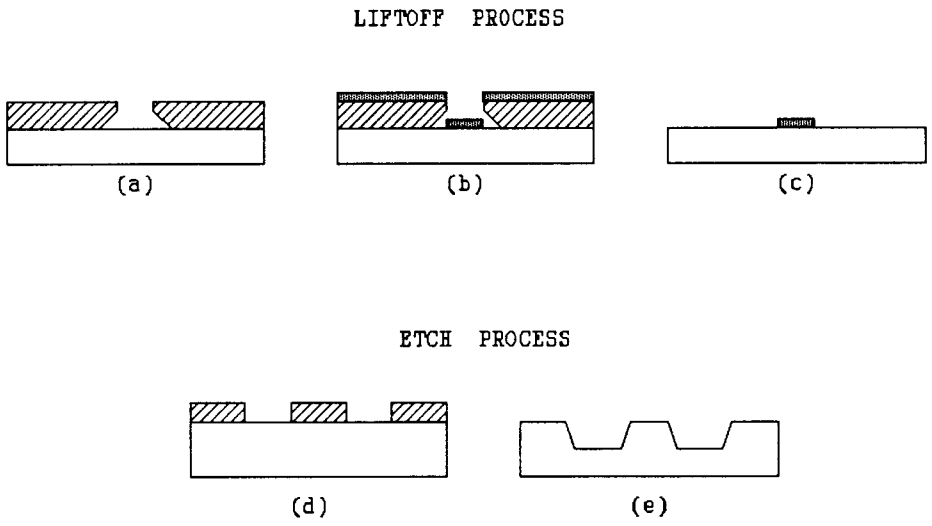

FIGURE 7
Liftoff and etch process.

lithography is a wet chemical etch mask. In this mask step photoresist is spun onto the sample and windows are opened where the sample is to be etched as shown in figure 7d. After wet chemical etching, the photoresist is removed and the sample will appear as shown in figure 7e. The fabrication of the p-channel MODFET substrate material was accomplished using a six mask level process. In the first mask step, mesas were etched on the substrate for device isolation. The mesas were masked with photoresist and the remaining material was etched to a depth of approximately 200nm using a NH_4OH solution. All devices were then fabricated on the surface of the remaining mesas.

In the second mask level a liftoff process was used to define ohmic contacts to the source and drain using a thermally evaporated Au/Zn/Au p-type ohmic metal. Immediately prior to evaporation of the contacts, the sample was dipped in an NH_4OH solution to clean the surface. The samples were then placed into the evaporation system as quickly as possible to minimize surface contamination problems. 15nm of Au, 50nm of Zn, and 150nm of Au were evaporated and a liftoff was performed. Subsequent to evaporation and liftoff, the contacts were annealed in forming gas at 470°C for 5 minutes. The contacts were then probed and the checked. If the contacts were Schottky an additional anneal was performed in an attempt to improve the contacts. If the contacts still showed Schottky behavior after subsequent annealing, they were discarded.

The third mask level was a gate recess etch. The area under the gate was etched using a citric acid solution with a 20nm/min etch rate for GaAs and a

2nm/min etch rate for $Al_{0.3}Ga_{0.7}As$. This etch rate was slow enough to allow adequate control of etch depth and threshold voltage, therefore, either enhancement or depletion mode devices could be fabricated.

In the fourth mask level a liftoff process was used to define Schottky gates and make contacts to the source and drain. The gate and contact metalization was thermally evaporated Ti/Au. Immediately prior to the evaporation, the sample was dipped in an NH_4OH solution to clean the surface. After cleaning, the sample was placed in the evaporator as soon as possible in order to avoid surface contamination. 50nm of Ti and 50nm of Au were then evaporated and the liftoff process was completed.

After the gate metal deposition, 100nm of SiO_2 was deposited over the entire sample surface for passivation and bonding pad isolation. The SiO_2 was deposited using a plasma enhanced chemical vapor deposition system. A wet etch mask was then put over the SiO_2 and windows were etched through the SiO_2 to allow contact to the gate metal. An etch solution of buffered hydrofluoric acid was used to etch the SiO_2.

Once contact windows were opened a final liftoff mask was applied to the sample. The sample was then dipped in an NH_4OH solution to clean the surface. After surface cleaning, the sample was placed into the thermal evaporator as quickly as possible to avoid contamination. 50nm of Ti and 200nm of Au were then evaporated onto the surface and liftoff was completed. The devices were then completed and ready for testing at this point.

3.4 Device Testing

Once fabrication of the MODFET devices was completed, preliminary DC characterization was performed using a Hewlett Packard 4145B parametric analyzer and a probe station with three micromanipulator probes. The preliminary measurements made using the 4145B were DC FET curves and were measured to find working devices that could be cleaved and packaged for further testing. Once working devices were found, the sample was cleaved into individual devices and the best of these devices were then mounted into a 28 pin leadless chip carrier with silver epoxy. After curing the silver epoxy, connection between the device and chip carrier was made using a gold wire bonder. Once packaged, the device characteristics were measured using a special test fixture designed to allow connection between the packaged device and the 4145B, both at room temperature and while immersed in liquid nitrogen. A full DC characterization could be performed at both 300K and 77K using the 4145B.

4. Experimental Results

The systematic study of AlGaAs/$In_YGa_{1-Y}As$/GaAs p-type MODFET material properties versus indium mole fraction Y and quantum well width yielded several valuable results. Van der Pauw Hall mobility measurements showed a good correlation between hole mobility and the indium quantum well composition and width at both 300K and 77K. In addition, this measurement showed that the carrier density in the quantum well varied only slightly as the well composition and width changed. The trends seen in the Hall mobility data were also well correlated with the photoluminescence data taken from the samples. Finally, the feasibility of producing devices from this material was demonstrated by fabricating one of the samples into a MODFET, which was then characterized for DC device performance.

4.1 Van Der Pauw Measurement Results

The van der Pauw Hall measurements described in section 3.2.2 were performed at 300K and 77K for each p-type MODFET that was grown. The results of these measurements are shown in Table II on pg. 31. From the graphs of mobility versus quantum well width and indium content, shown in figures 8 and 9 on pgs. 31 and 32 respectively, it can be seen that the mobility of holes generally increases as the percent of indium in the quantum well and the well thickness increase. The samples containing 10% In show a clear increase in mobility as the quantum well

Table 2 - Van der Pauw measurement results.

In%	T QW (Å)	300K Mobility ($cm^2/V \cdot s$)	300K Ns ($1/cm^2$)	77K Mobility ($cm^2/V \cdot s$)	77K Ns ($1/cm^2$)
0	ϕ	162	2.66E12	1926	2.20E12
10	50	185	1.85E12	860	1.81E12
10	100	189	2.69E12	1127	2.58E12
10	150	195	1.93E12	1751	1.96E12
20	50	207	1.94E12	1464	2.28E12
20	100	256	1.75E12	2186	1.91E12
20	150	237	1.71E12	1879	1.90E12
30	50	144	2.07E12	706	0.53E12

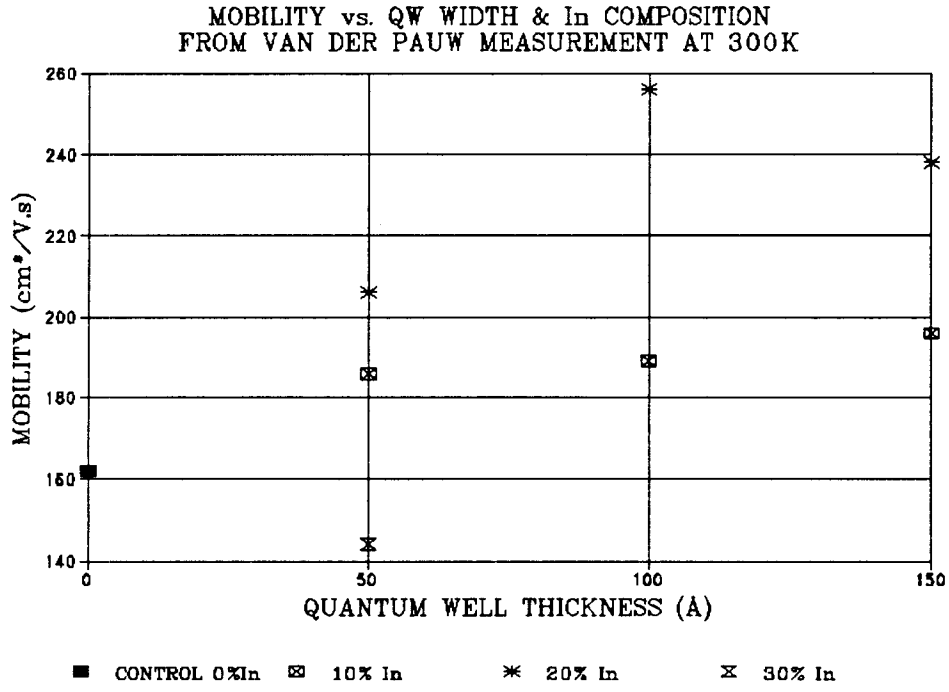

FIGURE 8
300K Hall mobility measurement results.

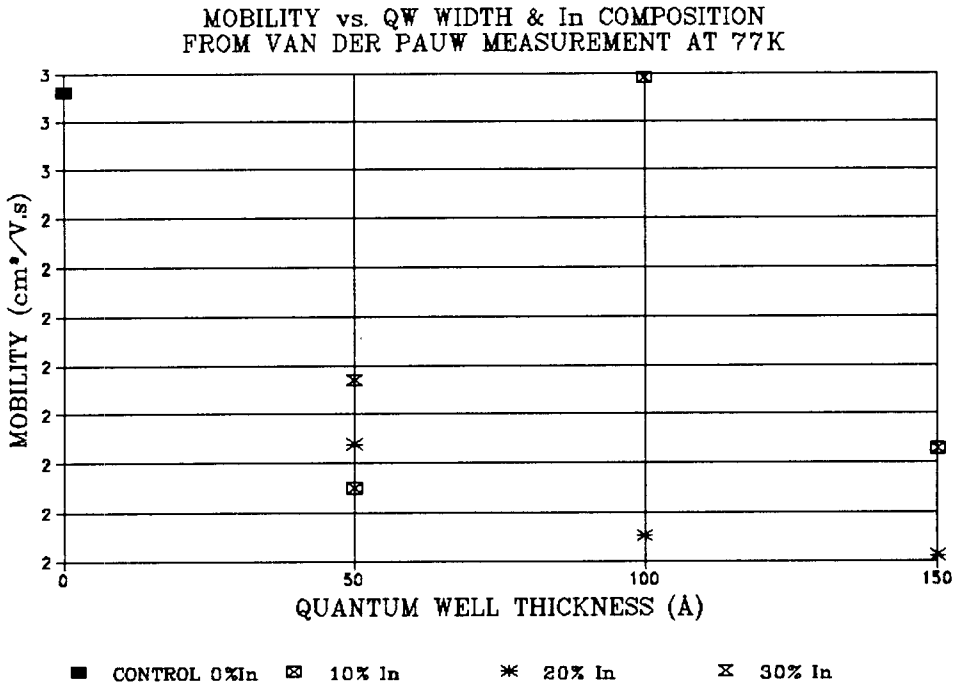

FIGURE 9
77K Hall measurement results.

thickness increases. All of the samples containing 20% In have higher mobilities than the 10% In containing samples of the same well thickness, and a trend of increasing mobility as quantum well width increases can also be seen in the 20% In samples. The 20% In, 150Å quantum well structure does not follow this trend, however, and a reduction of mobility in the 20% In, 150Å quantum well structure compared to the 20% In, 100Å quantum well structure can be seen. This decrease in mobility may be due to excessive defect formation in the InGaAs layer caused by relaxation of strain in the quantum well. However, the relatively small degradation in mobility in this sample seems to indicate that the InGaAs may only be partially

relaxed and have only a moderately increased defect density. The total relaxation of strain in the InGaAs quantum well results in very poor mobility due to the excessive defects present in a relaxed layer. This effect can be clearly seen in the 30% In, 50Å quantum well structure, which shows an extremely poor mobility due to the InGaAs quantum well being completely relaxed. Further evidence for assuming the 30% In, 50Å quantum well structure is relaxed can be seen in the sheet carrier densities this structure has at 300K and 77K. This structure is the only sample which shows a dramatic drop in carrier concentration in the quantum well when the sample is cooled from room temperature to 77K. This drop in carrier concentration is good evidence that a large number of traps probably exist in the quantum well, and thus indicates that the material quality of this sample is poor. Since all the samples were grown during a short time period, and the 30% indium sample is the only sample to show evidence for severe trap effects, the poor quality of this sample is most likely the result of excessive defect formation due to relaxation of strain in the InGaAs quantum well.

The data in table II on pg. 31 also show only a slight variation in sheet carrier concentration in the quantum well as indium composition and well width change. In this figure it can be seen that the 0% indium, and 10% indium, 100Å quantum well structures show a substantially higher 300K sheet carrier density than the other samples. This difference is due to the fact that these two samples were grown with a sheet density of $6x10^{12}$ /cm^2 instead of $3.6x10^{12}$ /cm^2 as was used in the other samples. This decrease in sheet doping density resulted in a decrease in sheet carrier

density in the well from about $2.6x10^{12}/cm^2$ in the these two samples, to about $2x10^{12}/cm^2$ in the remaining samples. To first order, mobility has only a small dependence upon the number of carriers present in the well, thus it was expected that this change would have only a small effect on the overall mobility of the samples. The data showing mobility versus quantum well composition and width in figures 8 & 9 on pgs. 31 and 32 show that this change did not seem to affect the mobility of any of the samples significantly, and that the mobilities of these samples were very consistent with the mobilities seen in the other samples. From the data in Table II on pg. 31, with the exception of the 30% In, 50Å quantum well structure, it can also be seen that the sheet carrier concentration in the quantum wells did not change significantly when the samples were cooled from 300K to 77K.

4.2 Photoluminescence Measurement Results

In addition to van der Pauw measurements, photoluminescence (PL) measurements were performed for each sample. The PL spectra for all samples were taken using the apparatus described in section 3.2.1,at a sample temperature of 20K, with a laser output power of 15mW for optical excitation of the sample. All PL measurements were performed in one lab session to reduce experimental error, and allow for easier comparison of the data obtained. The PL spectra taken were also normalized to a standard value to allow comparison of the relative intensity of the various spectra.

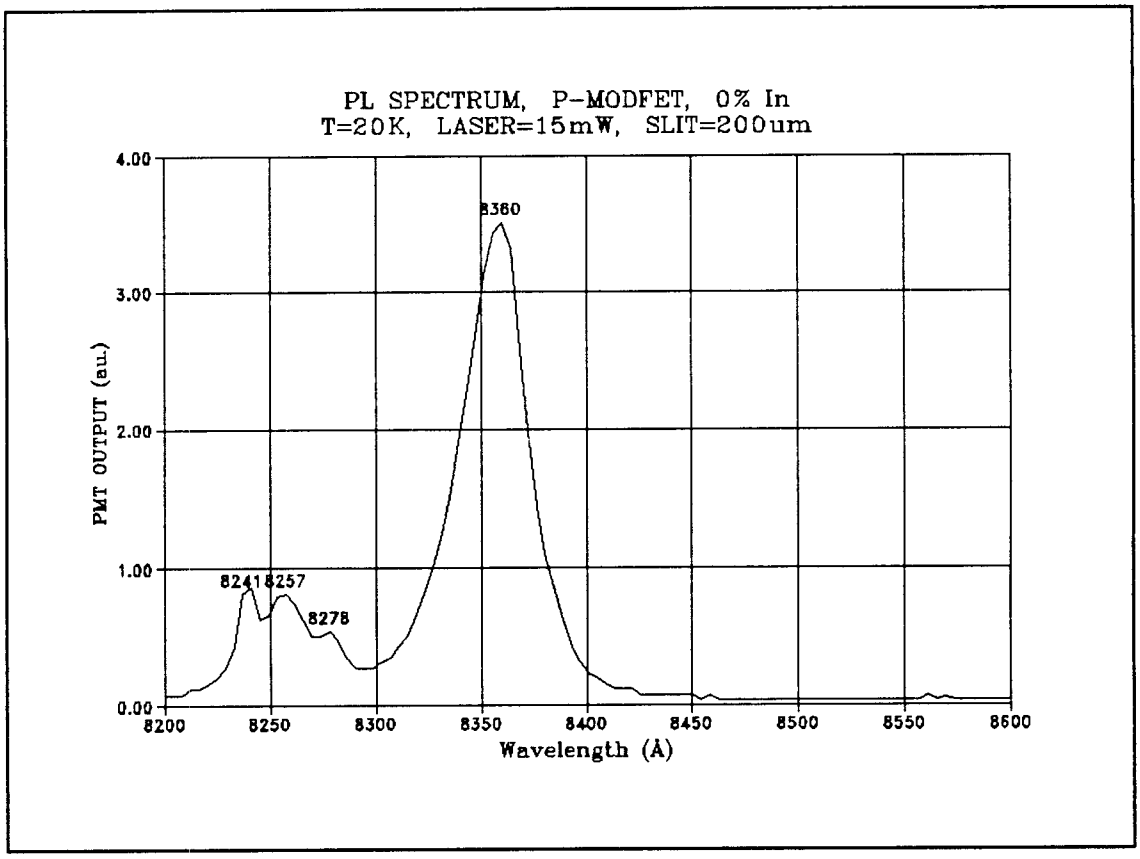

FIGURE 10
PL spectrum of an AlGaAs/GaAs p-MODFET structure.

The PL spectrum for the 0% indium containing control sample is shown in figure 10 above. In this graph, four predominant peaks at 8241Å, 8257Å, 8278Å, and 8360Å can be seen. The peak at 8360Å is due to a donor to carbon acceptor transition in GaAs and the cluster of peaks around 8257Å is due to excitons bound to neutral acceptor-like point defects in GaAs. This cluster of peaks actually consists of 15 sharp lines, however, all 15 peaks can only be seen if the sample temperature is 1-2K. In this sample, due to the sample temperature of 20K, only three of these peaks can be seen around 8257Å.

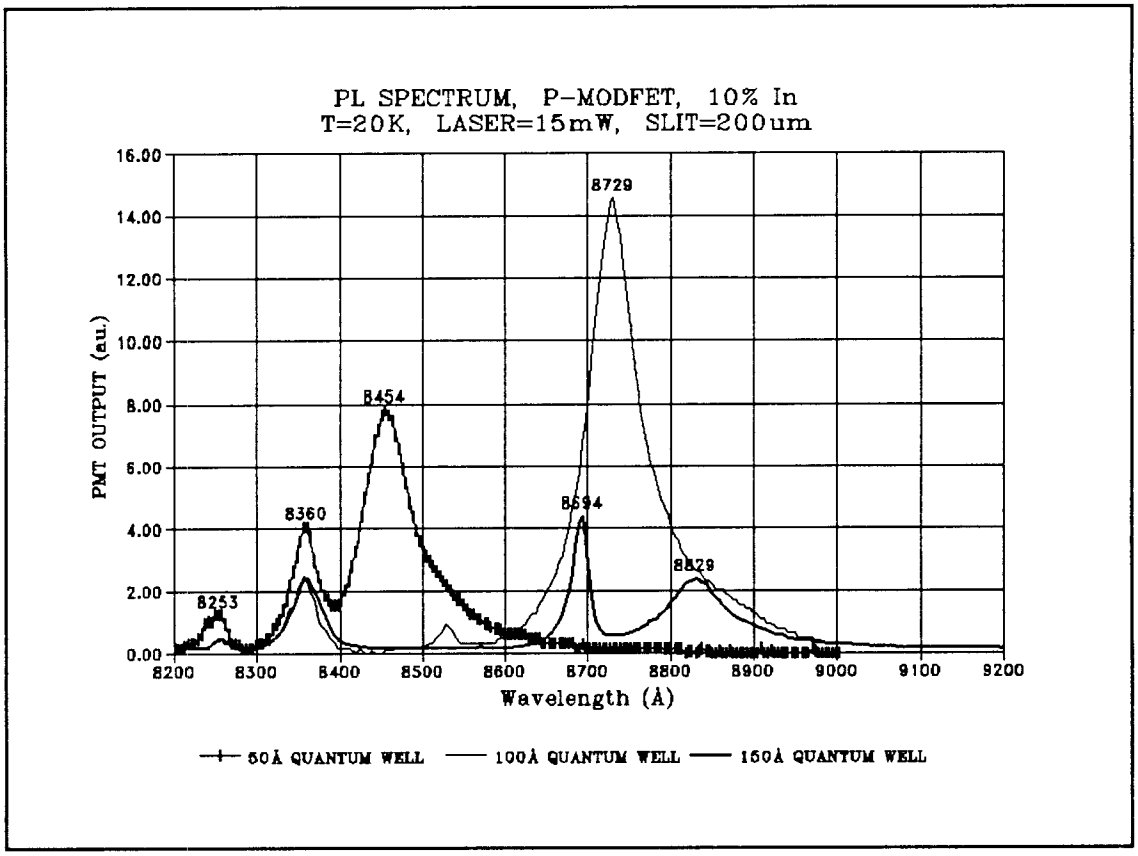

FIGURE 11
PL spectrum of a 10% indium p-MODFET structure.

In figure 11 above, the PL spectra for the samples containing 10% indium in the active region are shown. In this figure, it can clearly be seen that the peak at 8360Å and the cluster of peaks at 8260Å present in the 0% indium sample can also be seen in each of the 10% indium samples. This fact is due to the GaAs present in both the buffer layer and cap layer of the samples, and since these GaAs layers are present in all the samples grown, the peaks at ≈8260Å and 8360Å are present in all the samples grown. It can be seen, however, that the cluster of peaks around 8260Å appears as one broader peak in the 10% indium samples due to increased luminescence from the InGaAs and lower resolution of the graph. The remaining

peaks in the spectrum are due to the E_1^{CB} to E_1^{VB} ground state confined energy levels in the InGaAs quantum well. From elementary quantum mechanics it can be shown that a narrower quantum well will have confined energy levels at higher energies than a quantum well of the same depth and larger width. Thus the narrowest InGaAs quantum wells will have the highest energy transitions, or correspondingly, the shortest wavelength transitions. In figure 11, the first peak corresponding to an InGaAs quantum well occurs at 8454Å and arises from the 50Å quantum well. The next InGaAs peak is from the 100Å quantum well and occurs at 8729Å. The final plot in this graph is the spectrum for the 150Å quantum well structure and shows an interesting feature of two peaks from the InGaAs quantum well. From the general shape and width of the peak at 8829Å, and from the position of this peak above the 8729Å peak for the 100Å quantum well sample, it is believed that the 8829Å peak is the E_1^{CB} to E_1^{VB} ground state transition for the 150Å quantum well. The second peak at 8694Å is much narrower than the other InGaAs peaks and has an energy which is too large to correspond to a light to heavy hole splitting and too small to correspond to a second confined level transition. Due to the position of this peak with respect to the fundamental peak, and the narrow linewidth of this peak, it is possible that this peak is due to a bound exciton which has an allowed confined level in the quantum well only if the quantum well width exceeds the exciton radius. The binding energy of an exciton, E_{XN}, can be calculated from equation 4.1[22] and the radius of an exciton, r_{XN}, can be calculated from equation 4.2[22] shown on pg 38. In equations 4.1 and 4.2, m_r is the reduced mass of an electron, m_h is the effective mass

$$E_{xn} = 13.6\left(\frac{1}{n\epsilon_r}\right)^2\left(\frac{m_r}{m_o}\right) eV \quad (4.1) \qquad r_{xn} = 0.53n^2\epsilon_r\left(\frac{m_o}{m_r}\right) \text{Å} \quad (4.2)$$

$$\text{where } m_r \text{ is given by} \qquad \frac{1}{m_r} = \frac{1}{m_e} + \frac{1}{m_h}$$

of a hole, and m_e is the effective mass of an electron. For 10% InGaAs the exciton radius can be calculated to be approximately r_{XN}=130Å with a binding energy E_{XN}=4.1 meV. Although the calculated exciton radius is consistent with the observed results, further research is still needed to isolate the exact cause of the second peak in this structure, and possible experiments to accomplish this goal will be discussed in the conclusions section at the end of this work.

From figure 11 it can also be seen that the peaks corresponding to the E_1^{CB} to E_1^{VB} ground state transitions for each well are quite narrow with a full width at half maximum (FWHM) of roughly 70Å in each case. This narrow linewidth is indicative that the InGaAs in the quantum wells has not relaxed during growth and is consistent with the Hall mobility data which shows relatively good mobility in each of these samples.

The PL spectra for the samples containing 20% indium are shown in figure 12, on page 39. In this figure, the peaks due to the GaAs at 8360Å and 8257Å can be seen in each of the spectra as expected. The remaining peaks are due to the E_1^{CB} to E_1^{VB} ground state transitions in each of the 20% InGaAs quantum wells. The peak at 8912Å is from the 50Å quantum well sample, the peak at 9282Å is from the 100Å quantum well sample, and the remaining peaks at 9368Å and 9553Å are from the

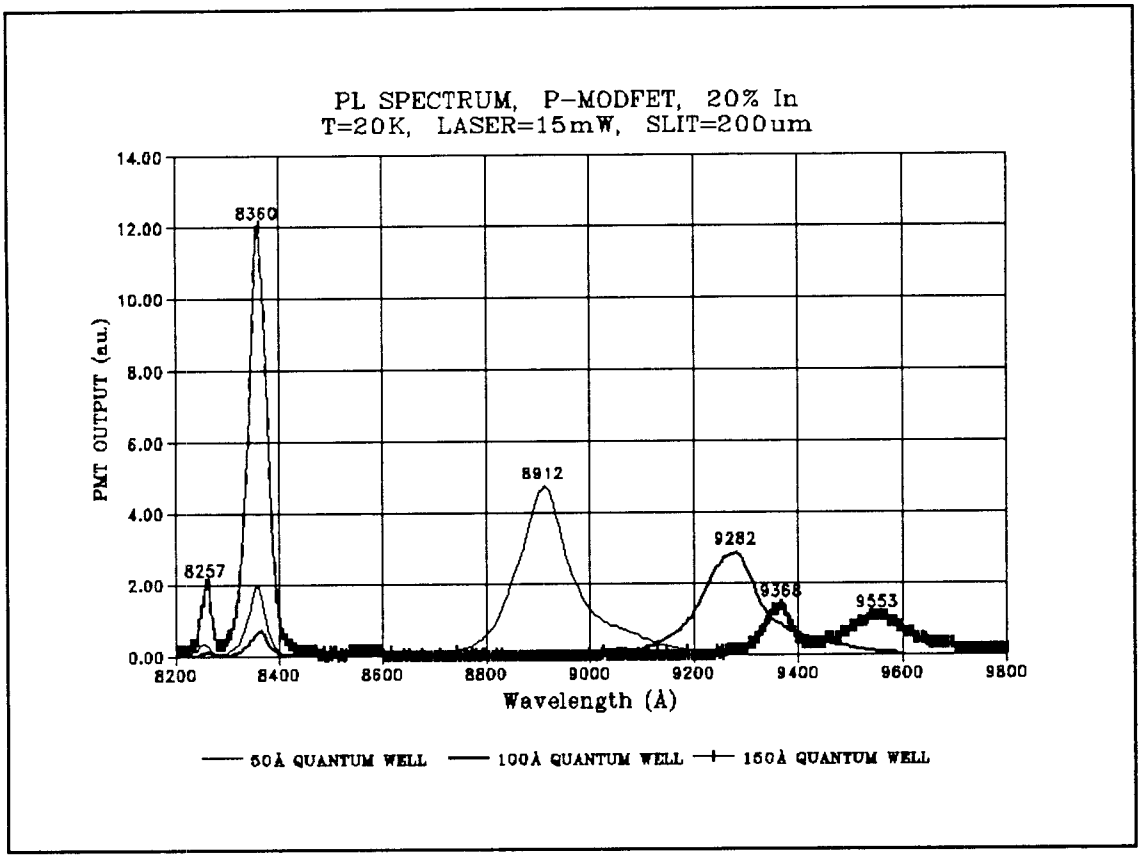

FIGURE 12
PL spectrum of 20% indium p-MODFET structures.

150Å quantum well sample. In this figure the 150Å quantum well sample shows the same double peak feature that was observed in the 10% indium, 150Å quantum well sample. Since all of the samples with 150Å quantum wells exhibit this double peak feature, this fact supports the theory of the second peak being related to a bound exciton which is only allowed to reside in the quantum well if the well width becomes larger than the exciton radius. The peaks from each of the InGaAs quantum wells have fairly narrow widths of about 100-110Å, indicating that the InGaAs has not relaxed during growth.

The spectrum from the 20% indium, 150Å quantum well device shows that the

peak from the InGaAs has very low intensity compared to the other InGaAs peaks and the 8360Å peak from the GaAs is extremely bright in comparison to the other indium containing samples. This poor luminescent efficiency from the InGaAs indicates that the InGaAs quantum well may have some sort of defect or trap center present which is inhibiting radiative recombination in the quantum well. Since the quantum well width in this sample is close to the critical thickness, the poor luminescent efficiency may be due to partial relaxation of the strain in the InGaAs layer and defect formation or excessive surface roughness. However, since the width of the 9553Å peak is almost the same as the peak width seen in the spectra of the other 20% indium samples, it is not likely that the InGaAs in this sample is completely relaxed, since total relaxation of strain in InGaAs would lead to a much broader peak in the spectrum. This observation agrees well with the Hall mobility data which showed a unexpected drop in mobility for the 20% indium, 150Å quantum well sample, indicating that the InGaAs quantum well may have had excessive defects present. The mobility for this sample was high enough to indicate that the indium was not completely relaxed, which also corresponds well to the narrow linewidth of the PL peak for this sample.

The PL spectrum for the 30% indium containing sample is shown in figure 13 on pg. 40. In this figure three peaks can be seen. The expected GaAs peaks at 8257Å and 8360Å are both present and the remaining peak at 9141Å is due to the E_1^{CB} to E_1^{VB} ground state transition in the InGaAs quantum well. The luminescent efficiency of this well is extremely good and is the second brightest peak measured

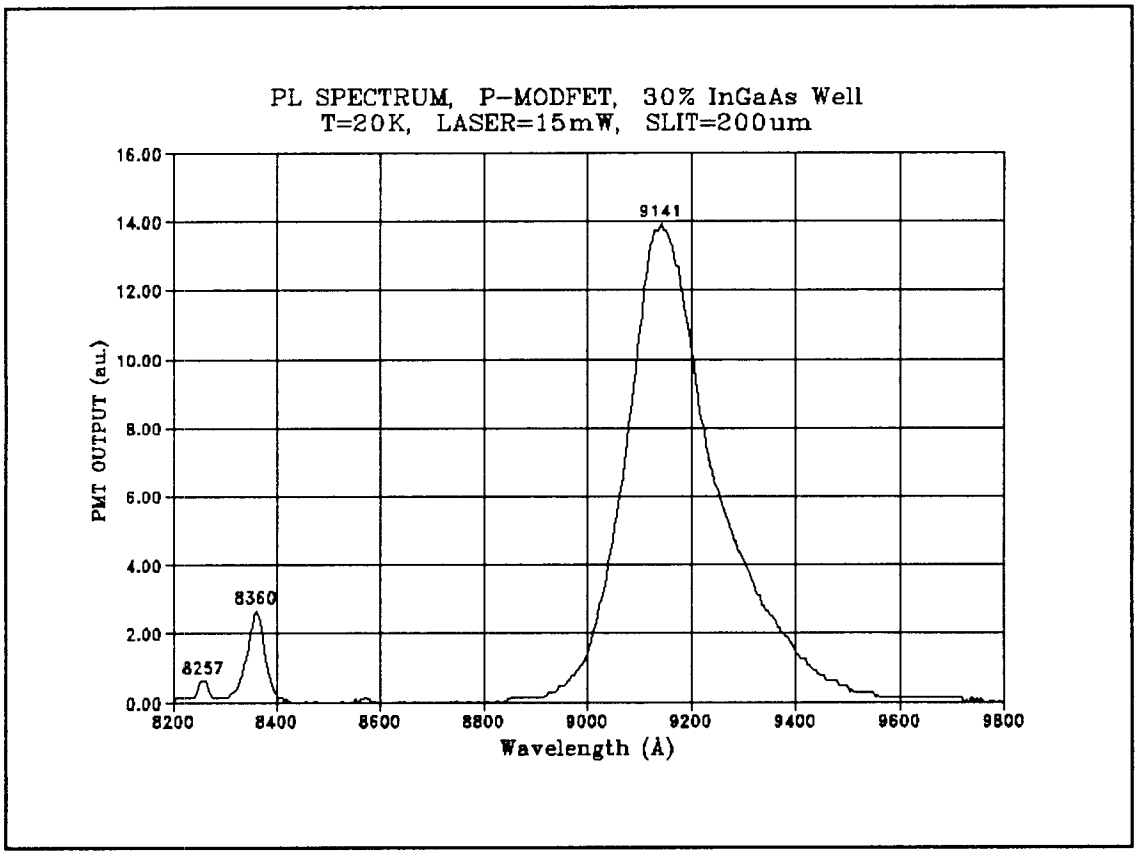

FIGURE 13
PL spectrum of a 30% indium p-MODFET structure.

in all of the samples. However, this peak is quite wide, measuring approximately 190Å at FWHM, which indicates that the InGaAs in the quantum well has probably relaxed during growth. This supposition agrees well with the Hall mobility data, which showed poor mobility in this sample.

The previous PL spectra compare quantum wells with constant indium composition and varying well widths. In addition to this, it is useful to compare the PL spectra for quantum wells with a constant quantum well width and varying indium composition. Since the bandgap of $In_YGa_{1-Y}As$ decreases as the mole fraction Y of indium increases, an InGaAs quantum well of constant width will become deeper and

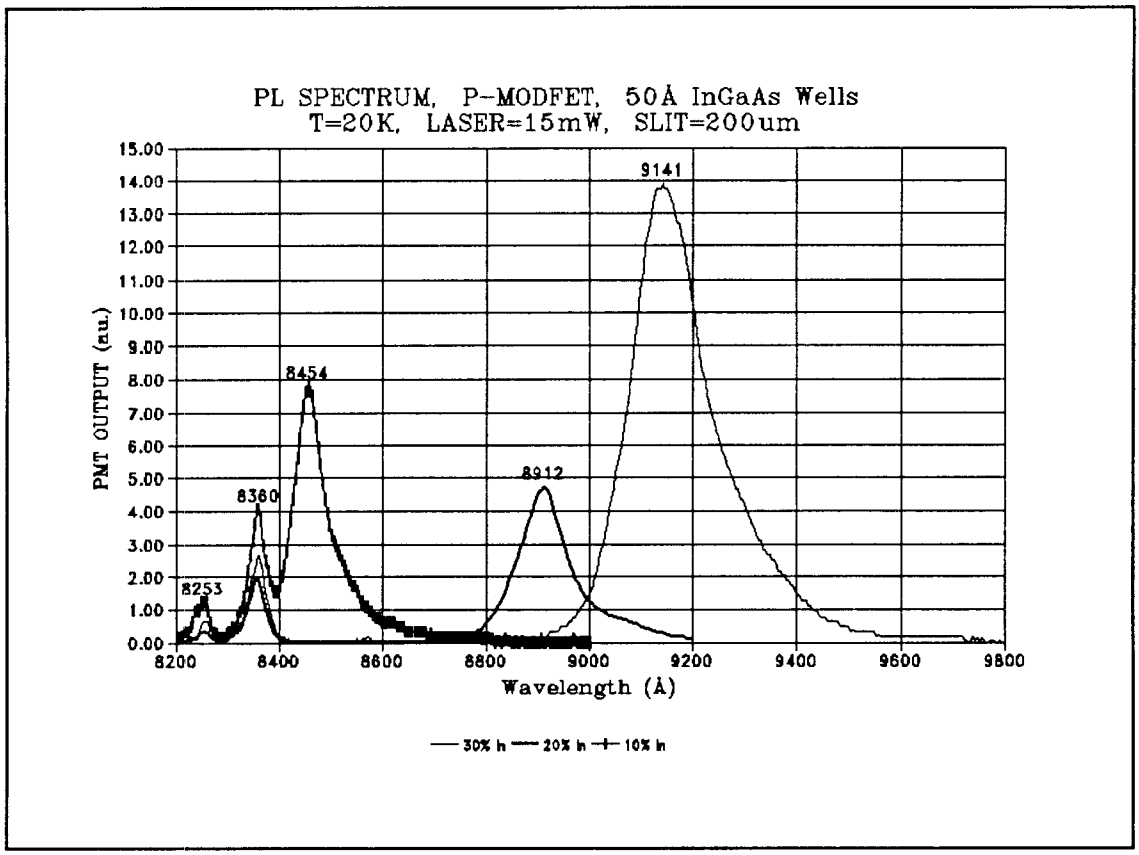

FIGURE 14

PL spectrum of 50Å InGaAs quantum well p-MODFET structures.

the energy of the E_1^{CB} to E_1^{VB} ground state energy transition will decrease as indium composition in the well increases. In figure 14 above, samples with 50Å quantum well widths and 10%, 20%, and 30% indium content are shown. In this graph the GaAs peaks at 8360Å and 8257Å are present for each sample and the remaining peaks are due to the InGaAs quantum wells. The lowest energy transition, or correspondingly the longest wavelength transition, occurs for the 30% indium quantum well at 9141Å. The highest energy transition, or correspondingly the shortest wavelength transition, occurs for the 10% InGaAs quantum well at 8454Å.

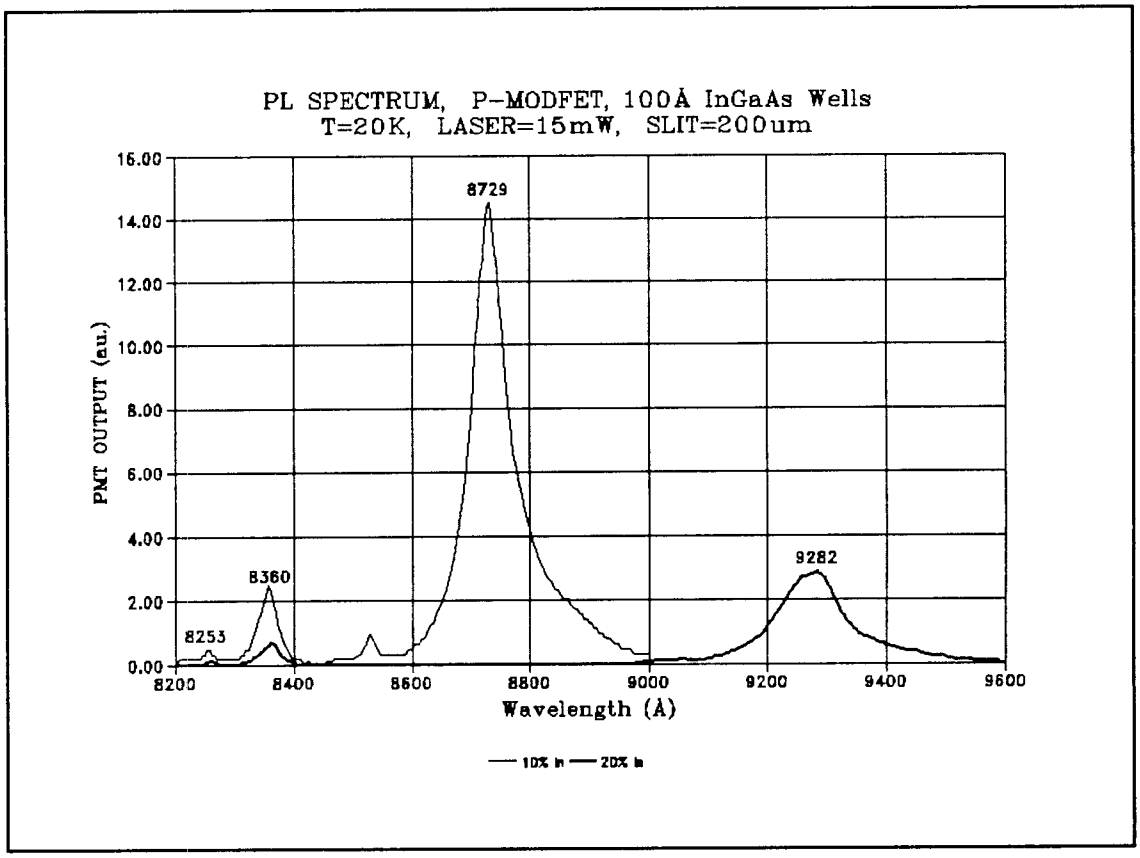

FIGURE 15

PL spectra of 100Å InGaAs quantum well p-MODFET structures.

Finally, the peak at 8912Å is due to the 20% indium quantum well, and occurs at an energy that is in between the energies of the 10% and 30% quantum well peaks.

Similar trends can be seen in the PL spectra for the samples containing 100Å quantum well widths shown in figure 15 above. In this figure, two peaks at 8729Å and 9282Å due to the InGaAs quantum wells can be seen in addition to the GaAs peaks at 8360Å and 8257Å which are present in each sample. The longest wavelength peak at 9282Å is due to the 20% indium quantum well, and the shortest wavelength transition occurs at 8729Å, and is due to the 10% indium quantum well.

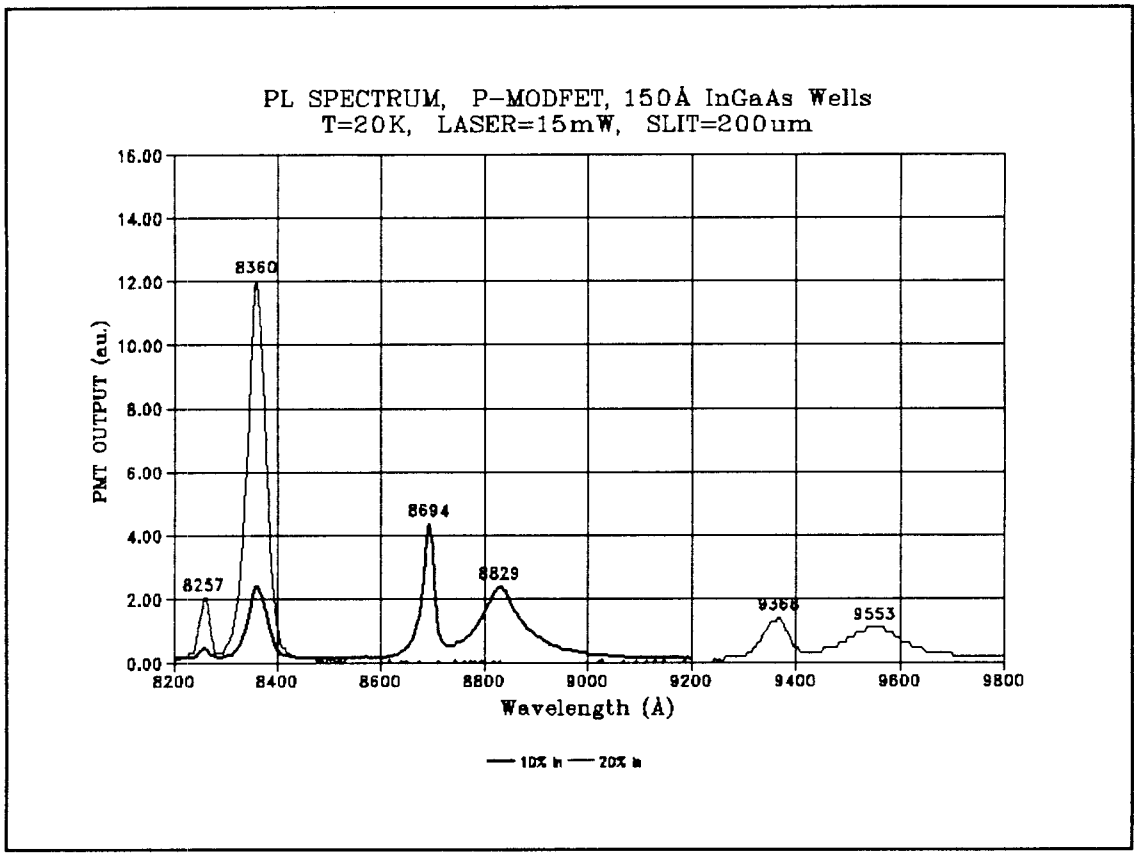

FIGURE 16
PL spectra of 150Å InGaAs quantum well p-MODFET structures.

PL spectra for the samples containing 150Å quantum wells are shown in figure 16 above. The expected GaAs peaks at 8257Å and 8360Å are again present in each sample. In this graph, it can clearly be seen that each of the 150Å quantum wells luminesce in two peaks, unlike the other InGaAs quantum wells with smaller quantum well widths which only luminesce in a single peak. It can also be seen that the spacing between the two peaks in the 10% sample is approximately the same as the spacing between the two peaks in the 20% sample, indicating that the origin of the second peak in each of the 150Å quantum wells is most likely due to a common cause. Figure 16 also shows that the higher energy peak in each sample is much

narrower that the low energy peak in each sample. Since the other InGaAs quantum well samples (which only luminesce in a single peak) have linewidths which are comparable to the low energy peaks in the 150Å quantum well samples, this indicates that the wider, low energy peak is most likely from the E_1^{CB} to E_1^{VB} ground state energy transition in the 150Å InGaAs quantum well. Also, since excitonic PL peaks are usually very narrow, the narrow line width of the high energy transition tends to support the proposed theory that the origin of this peak may be excitonic in nature.

4.3 DC Device Characterization Results

Once material characterization had been performed on all of the samples, the feasibility of producing devices from this material was demonstrated by processing some of the material into devices as described in section 3.3. These devices were then tested and packaged as described in section 3.4. The sample chosen for processing was the 10% indium, 50Å quantum well structure, since the Hall and photoluminescence data indicated that the material quality was good and this sample contained the smallest indium quantum well. The dimensions of the device tested were 2.5um gate length in a 6.5um channel, and a gate width of 95um. The DC device curves taken are shown in figures 17, 18, 19 and 20 on pgs. 47-50 respectively.

Figure 17 on page 47 shows the 300K current voltage curves for this device. This figure clearly shows that a working p-type MODFET has been fabricated. It can be seen that the gating characteristics are very good and that the device can be

completely turned off, indicating that there are not any significant leakage paths around the gate. The slope of the saturation region of the curves is fairly small, indicating that the output resistance is large. From this graph is can also be seen that the threshold voltage of this device is approximately 1V and therefore exhibits enhancement mode behavior. The transconductance of this device at 300K with respect to gate voltage is shown in figure 18 on page 48. This figure shows that the transconductance of this device increases as the gate voltage becomes more negative and reaches a maximum of about 7 mS/mm at a gate voltage of about -1V. As the gate voltage becomes more negative than -1V, the transconductance can be seen to drop again, due to parasitic effects in the device.

Figure 19 on page 49 shows the 77K current voltage curves for this device. The curves at this temperature are clearly much less ideal than the curves at 300K. The more gradual slope of the triode region and the small dead region near the 0V VDS axis indicate that there is a serious leakage problem in this device at 77K. The threshold voltage in this device is still about -1V at 77K and the channel can still be shut off completely. From figure 20 on page 50, it can also be seen that the transconductance of this device increases to a maximum of about 21 mS/mm clearly indicating the effect of mobility enhancement in these structures at 77K. It can be seen that the drop off in transconductance as gate voltage continues to become more negative, is much more pronounced at this temperature than at 300K, and is an indication that parasitic effects are more important at low temperatures in this device.

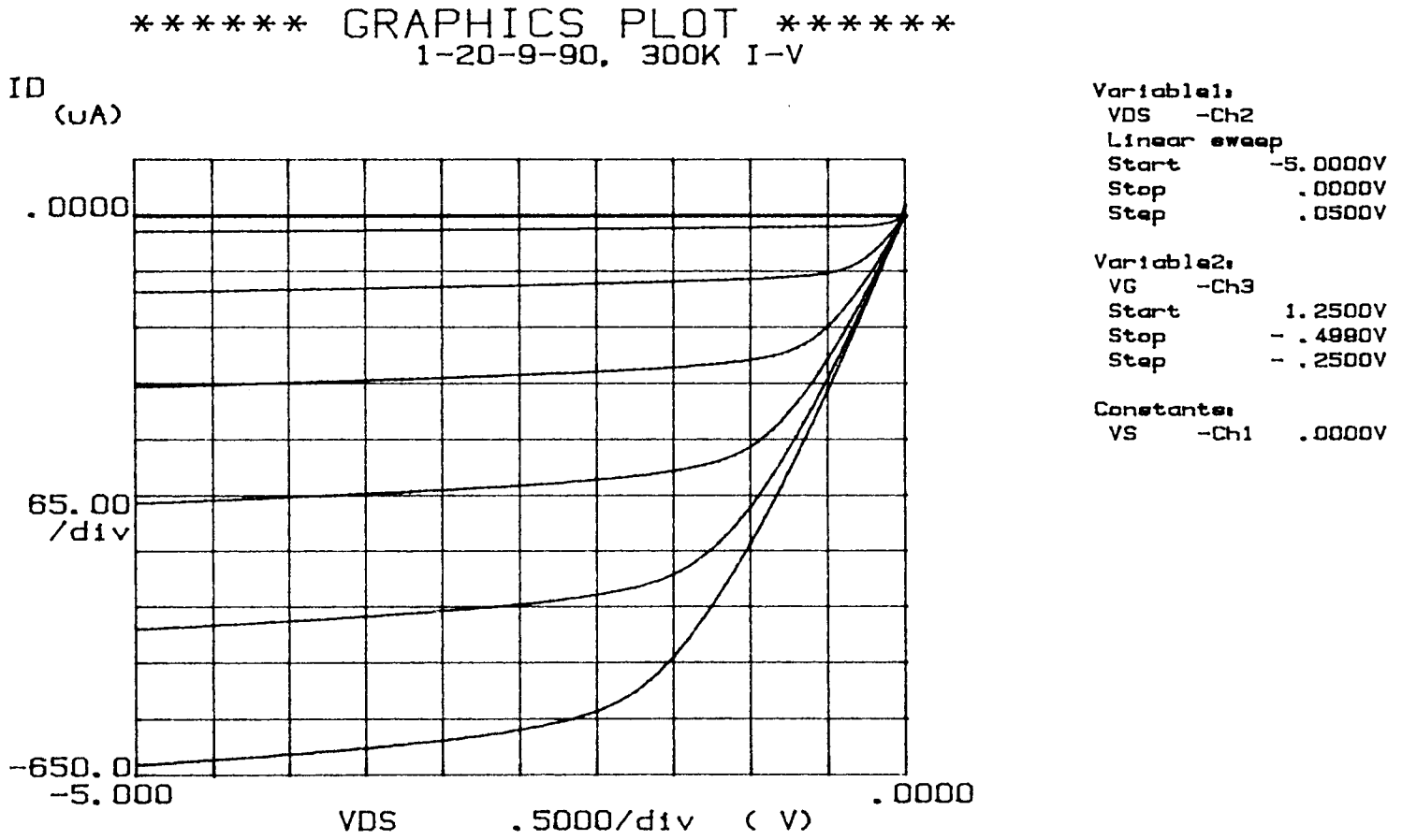

FIGURE 15
300K Current-Voltage Curves for a 2.5um gate length p-type MODFET

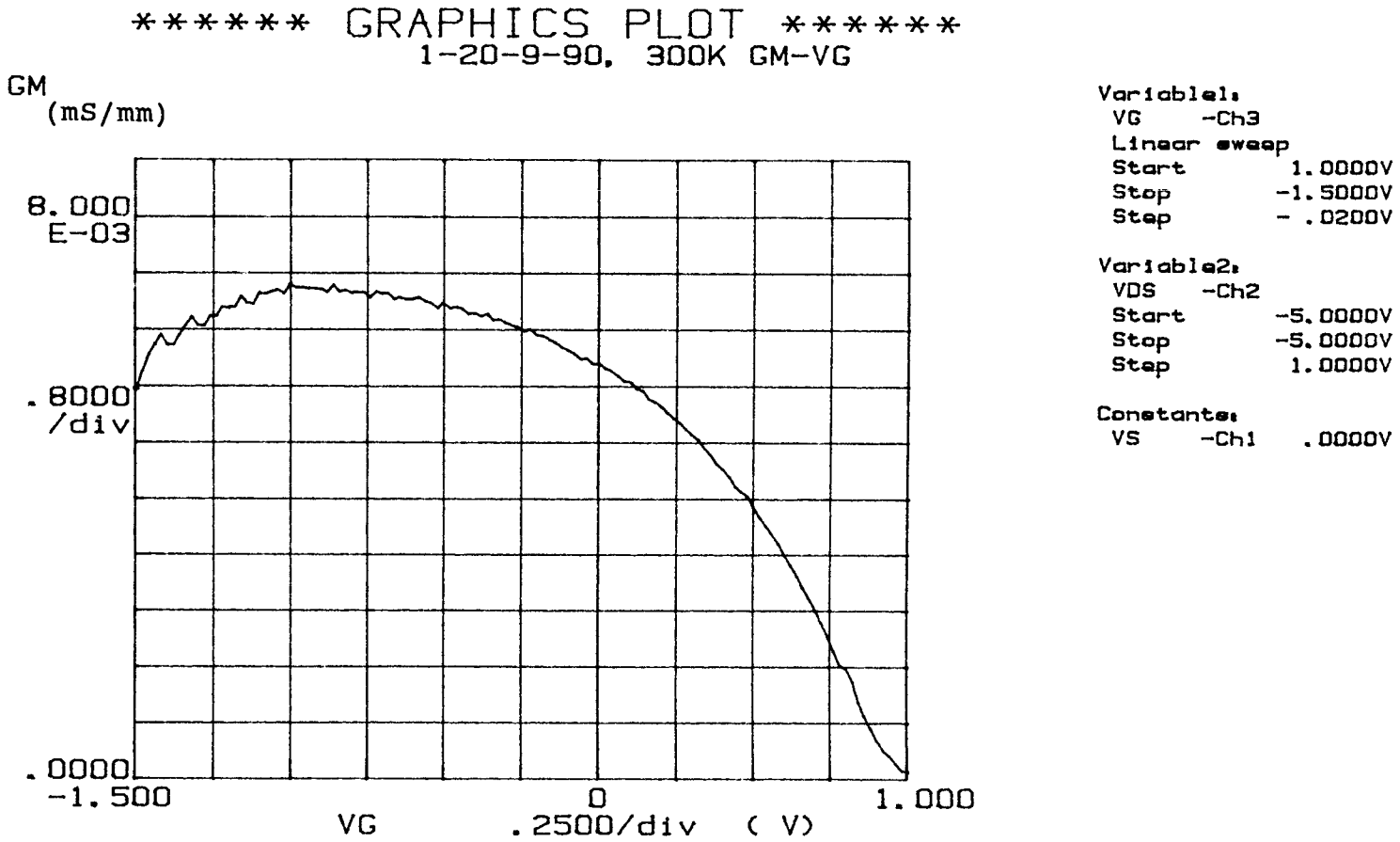

FIGURE 16
300K Transconductance vs Gate Voltage Curves
for a 2.5um gate length p-type MODFET

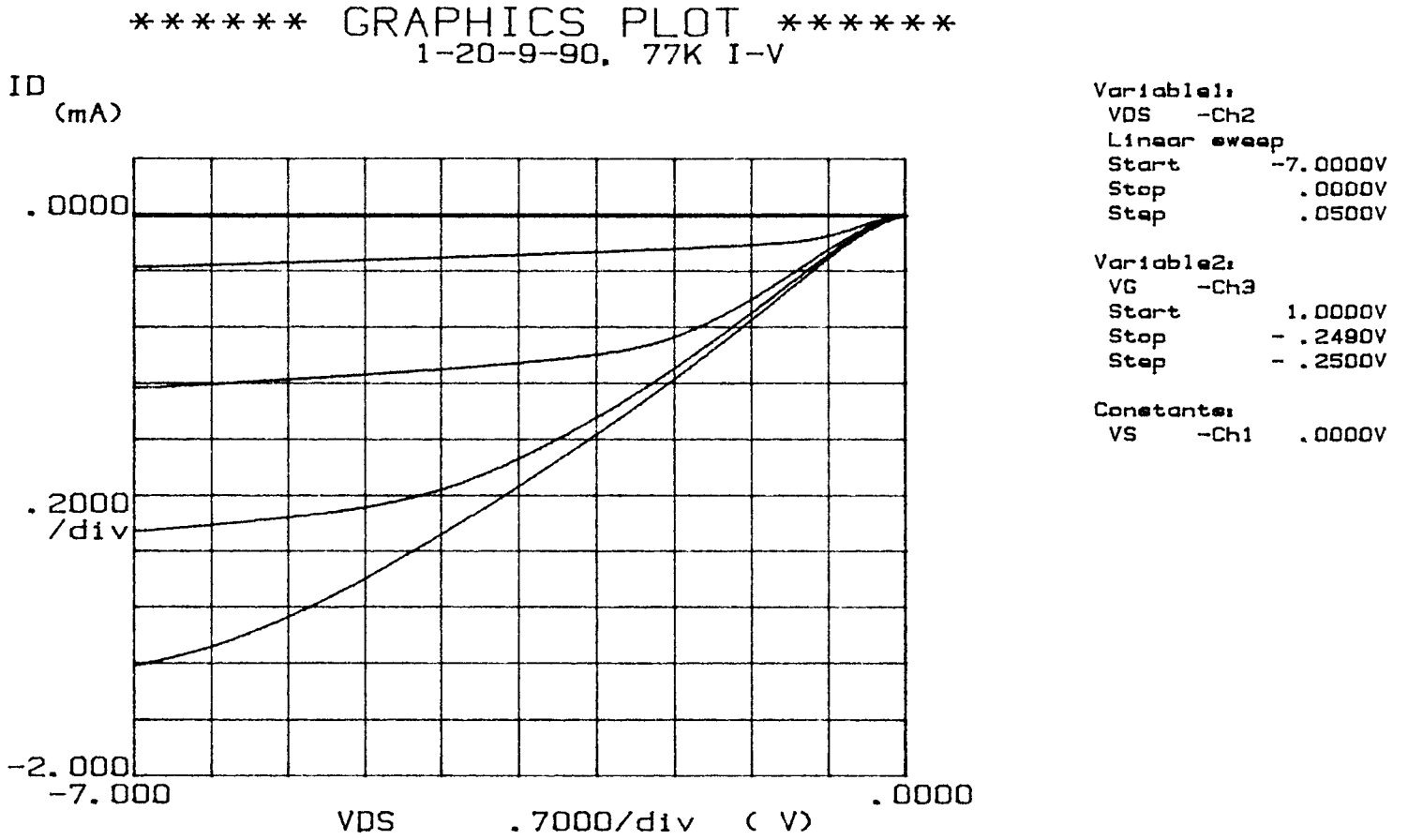

FIGURE 17
77K Current-Voltage Curves for a 2.5um gate length p-type MODFET

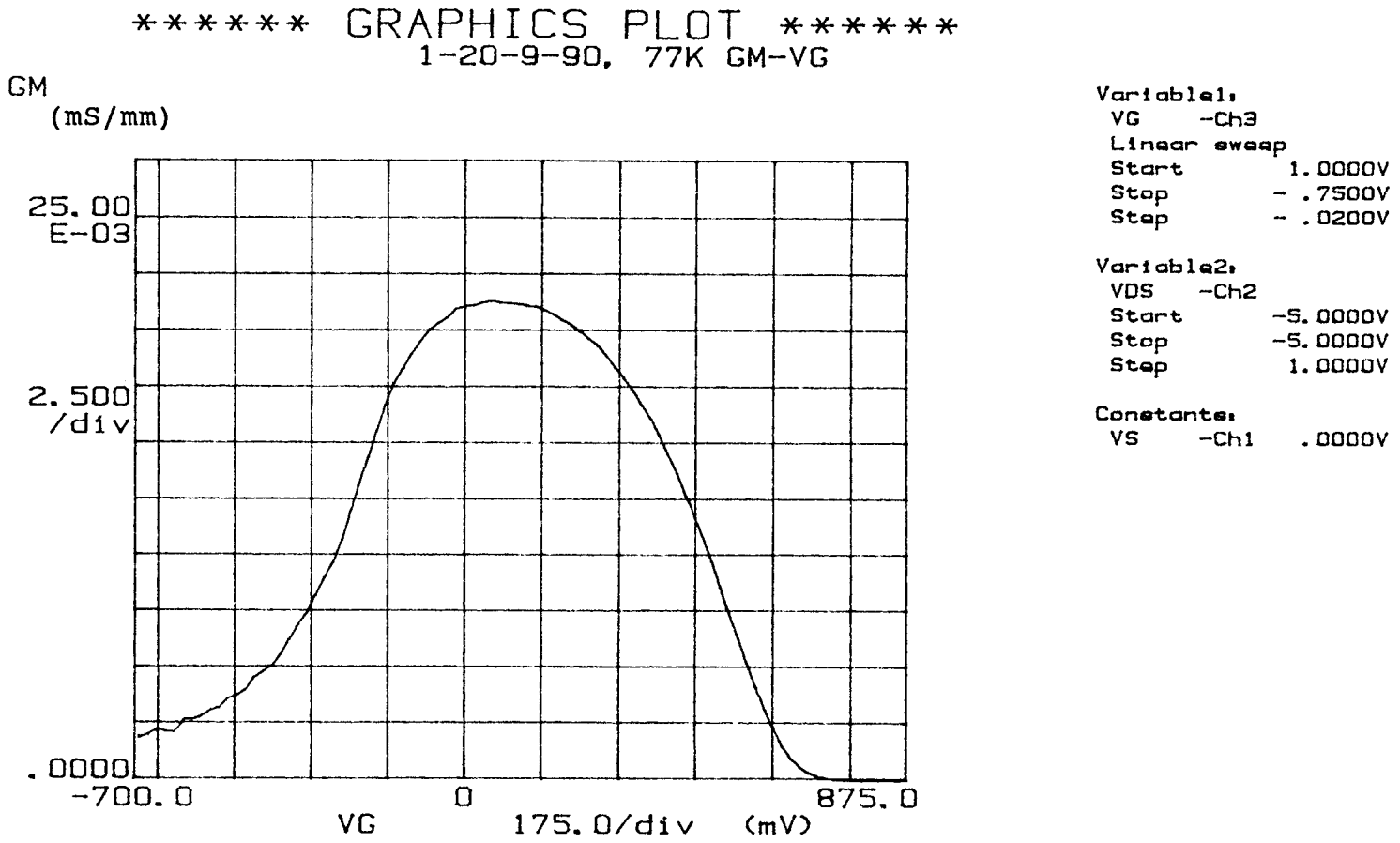

FIGURE 18
77K Transconductance vs Gate Voltage Curves
for a 2.5um gate length p-type MODFET

5. Discussion, Conclusions, and Further Work

5.1 Discussion

The use of strained pseudomorphic $In_YGa_{1-Y}As$ as an active region in p-channel MODFETS has been investigated by growing a series of p-channel MODFET structures with varying $In_YGa_{1-Y}As$ mole fraction Y and quantum well width. Samples containing 10% indium and 50Å, 100Å, and 150Å quantum wells, 20% indium and 50Å, 100Å, and 150Å quantum wells, and 30% indium with a 50Å quantum well were grown. These samples were then extensively characterized using van der Pauw Hall mobility measurements and photoluminescence (PL) characterization. The Hall data showed that hole mobility tends to increase as both the indium mole fraction and quantum well width of pseudomorphic InGaAs increase. In addition the Hall data provided evidence that mobility is degraded in InGaAs layers which are not pseudomorphic.

In order to fully understand the PL results a brief summary of the important features of PL spectra is reviewed here. The position of the peaks in a PL spectrum indicate the energy of the transition and the width of a peak is indicative of the material quality and type of transition. Narrow PL peaks are generally emitted from layers with good uniformity and high quality heterointerfaces, while poor layer uniformity or rough heterointerfaces tend to broaden PL peaks considerably. The luminescence peaks emitted from a quantum confined energy level usually have a

very narrow full width at half maximum due to the two dimensional density of states which is nonzero at k=0. Another important indicator of material quality is luminescent efficiency. Poor material quality generally leads to reduced luminescent efficiency since excessive nonradiative traps are often present in this material.

The photoluminescence data from these samples is consistent with the Hall measurement results. The samples which showed high measured mobility have relatively narrow peaks in their photoluminescence spectra. This result indicates that the material quality, layer uniformity, and heterointerfaces in these samples were very good. These observations lead to the conclusion that the InGaAs in these samples was most likely a high quality pseudomorphic layer. The luminescence efficiency also supports this conclusion since the samples with good mobility also have relatively bright InGaAs peaks in their spectra. The samples which showed degraded mobilities produced PL spectra that indicated the material quality of these samples was inferior to the other samples. The spectrum from the 20% indium, 150Å quantum well sample had a InGaAs peak which was quite dim and about 10-20Å wider than InGaAs peaks in the other 20% indium samples. The poor PL response indicates that this sample had excessive defects present in the InGaAs which may have been due to partial relaxation of the pseudomorphic InGaAs layer. The 30% indium sample had a very bright InGaAs peak; however, the width of this peak was almost twice the width of the other InGaAs peaks. This result indicates that the InGaAs may have been fairly free from nonradiative traps, but that the

heterointerfaces in the sample may have been quite rough. This leads to the conclusion that the InGaAs in this sample may have been a relaxed and no longer a pseudomorphic layer.

5.2 Conclusion

Both the mobility data and the photoluminescence data show clearly that the highest hole mobilities at any given mole fraction of indium should be obtained when the quantum well width is made as large as possible without allowing the pseudomorphic InGaAs layer to relax. From the data obtained in this work, an optimum concentration of 20% indium and 100-150Å is suggested.

The feasibility of fabricating devices has also been demonstrated by fabricating one sample into working p-channel MODFETS. These devices were characterized for DC performance at both 300K and 77K, and transconductances for a 2.5um gate length, 6.5um channel device were measured to be 7mS/mm and 21mS/mm at 300K and 77K respectively. It is anticipated that these results will improve as processing and material growth parameters are optimized.

5.3 Suggested Further Work

In photoluminescence spectra from the samples containing 150Å InGaAs quantum wells, two peaks due to the quantum well were observed. In all other samples with quantum wells narrower than 150Å, only one peak from the quantum well was observed. The exact cause of the second peak observed in the 150Å quantum wells is unknown at this time. In order to isolate the cause of this phenomenon, several additional experiments need to be done. First, the dependence of this phenomenon upon quantum well width should be studied by growing and characterizing samples with 10% indium and 100Å, 125Å, 150Å, 175Å and 200Å well widths. The PL data obtained from these samples should allow determination of the quantum well width at which the second peak appears and whether this peak is present in quantum wells with widths greater than 150Å.

It is also suggested that the dependence of this phenomenon upon doping type and profile be investigated by growing and characterizing a series of five 10% indium, 150Å quantum well samples with different doping layers. The five suggested samples are a delta doped p-MODFET, a delta doped n-MODFET, a uniformly doped p-MODFET, a uniformly doped n-MODFET, and a MODFET structure with no doping. From these samples it should possible to determine several important effects of doping upon the second PL peak. First, it should be possible to determine if the second peak is related to the type of doping impurity (silicon or beryllium) used in the structure. Second it should be possible to determine whether the second peak

is related to the use of delta doping or if this effect is also observed in uniformly doped structures. Finally from the undoped sample it may be possible to determine whether the second peak is due some other effect not associated with the doping of the structure.

From the suggested samples, much valuable information about this effect should be obtained and hopefully it should be possible to ascertain the cause of the second peak observed in the samples containing 150Å quantum wells.

6. Bibliography

1. R. A. Anderson, IBM J. Res. Dev. 4, p.283, 1960.

2. L. Esaki, R. Tsu, IBM J. Res. Dev., Vol. 14, p.61, 1970.

3. R. Dingle, G.L. Störmer, A.C. Gossard, and W. Wiegmann, Appl. Phys. Lett. 33(7), p.665, October 1, 1978.

4. T. Mimura, S. Hiyamizu, T. Fujii, and K. Nanbu, Jap. J. App. Phy., Vol. 19, #5, p.L225, May 1980.

5. H. L. Störmer and W. T. Tsang, Appl. Phys. Lett., 36(8), p. 685, April 15, 1980.

6. H. L. Störmer, K. Baldwin, A. C. Gossard, and W. Wiegmann, Appl. Phys. Lett., 44(11), p.1062, June 1, 1984.

7. J. W. Matthews, and A. E. Blakeslee, J. Cryst. Growth, 27, pp.118-125, 1974.

8. J. W. Matthews, and A. E. Blakeslee, J. Cryst. Growth, 29, pp.273-280, 1975.

9. J. W. Matthews, and A. E. Blakeslee, J. Cryst. Growth, 32, pp.265-273, 1976.

10. M. Shur, GaAs Circuits and Devices, p.539, Plenum Press, New York, 1987.

11. M. Shur, GaAs Circuits and Devices, pp. 566-570, Plenum Press, New York, 1987.

12. E.F. Schubert, J.E. Cunningham, W.T. Tsang, G.L. Timp, Appl. Phys. Lett., 51(15), p. 1170, October 12, 1987.

13. M. Jaffe and J. Singh, J. Appl. Phys., 65(1), pp.329-338, January 1, 1989.

14. T.G. Anderson, Z.G. Chen, V.D. Kulakovskii, A. Ukkin and J.T. Vallin, Appl. Phys. Lett., 51(10), pg. 752, 7 September 1987.

15. J.E. Schirber, I.J. Fritz, L.R. Dawson, Appl. Phys. Lett., 46(2), p. 187, January 15, 1985.

16. J. Ebner, MS Thesis, Department of Electrical & Computer Engineering, Oregon State University, 1987.

17. C. Cohen-Tannoudji, Bernard diu, Frank Laloë, Quantum Mechanics, pg. 77, John Wiley and Sons, 1977.

18. C. Cohen-Tannoudji, Bernard diu, Frank Laloë, Quantum Mechanics, pg. 74, John Wiley and Sons, 1977.

19. C. Weisbuch, and B. Vinter, Quantum Semiconductor Structures, pg. 19, Academic Press, 1991.

20. D. K. Schroder, Semiconductor Material and Device Characterization, pp. 9-14, Wiley & Sons, New York, 1990.

21. D. K. Schroder, Semiconductor Material and Device Characterization, pg. 201, Wiley & Sons, New York, 1990.

22. C. M. Wolfe, N. Holonyak, Jr., and G. E. Stillman, Physical Properties of Semiconductors, pg. 223, Prentice Hall, New Jersey, 1989.