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The increasing popularity of cellular phones with integrated cameras in the recent past has led to major improvements in its image quality. However, integration of new features, such as mobile email, video streaming, MP3 etc. tend to put the limitation on image quality as camera phone designers struggle to manage multiple features while maintaining healthy battery life time.

In this research, a novel efficient power management scheme for camera phones with flash for better image/video quality is discussed. A prototype power management circuit comprising of a 2 MHz Buck-and-Boost DC-DC converter driving up to 1.2A flash light emitting diode (LED) in 500nm CMOS process is implemented. The converter achieves high efficiency over the entire Li-On battery voltage range of 3.0V to 5.2V by operating in buck, buck-and-boost and boost mode based on the input/output voltage and load current requirements. The proposed pulse width modulator (PWM) controller operates continuously over the entire Li-On battery range while providing constant LED current. The converter shows peak efficiencies of 87% and 83% for LED current of 0.6A and 1.2A, respectively.

Design Techniques for High Efficiency LED Drivers

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Sarvesh Jagdish Bang, Author

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CHAPTER 1. INTRODUCTION

The modern day cellular phone has become a pocket media center, containing a digital still camera, MP3 player with hi-fi audio system, internet browser with video streaming, 3-D gaming capability, thumbprint sensors for security and many more features. The most recent cellular phones include high resolution cameras with flash attachments for increased image and video quality. The popularity of camera phones has encouraged developers to increase the resolution from 1.3 mega pixel to 3.3 - 4.4 mega pixel which in turn require auto-focus mechanisms and sophisticated brighter flash sources. Loading of cell phones with an array of such consumer features while operating with a single lithium-ion (Li-On) battery as a power source has produced numerous engineering challenges in the field of handheld power management. One such challenge lies in the power management of flash Light Emitting Diode(LED) to ensure cost and power efficient brightness for better image quality. In general the power management of flash LED can be broken into two main parts, namely, optimization of LED light output and efficient supply of power to the LED's. First, based on the LED characteristics and LED configuration different level of brightness could be obtained for the same amount of power. Hence, the term Luminous Efficiency which is defined as the ratio of luminous flux emitted from a light source to the electric power consumed by the source plays an important role governing overall efficiency. Second, an efficient

conversion of the limited battery power to the useful form for LED's to emit proper amount of light is of significant importance. This conversion of power is often achieved using voltage regulators as LED drivers and present enormous system and circuit level issues which have been a topic of interest to the researchers [1][2][3]. The following sections provides introduction to optimization of light output and LED drivers, the two fundamental issues in flash Power Management.

1.1 Optimization of Light Output

The demand of cellular phones with LCD screen and cameras prompted manufacturers to use white LEDs for backlighting and flash. There are various types of LEDs used in cellular phones, based on the end application, cost and power effectiveness. Picking the LED with high Luminous efficiency can help minimizing the power drawn from the battery during a flash event. Hence, LED selection plays an important role in LED power management.

In general, LED luminance is found to be directly proportional to its drive current [5] and hence in some applications like backlight, and flash the desired LED brightness is achieved by controlling the LED drive. Under the condition where desired brightness cannot be obtained using a single LED, additional LEDs can be placed either in parallel or series [6]. This arrangement of multiple LEDs plays a significant role in defining the amount of current drained from the battery. as is discussed in the Luminous Efficiency section in Chapter 2.

1.2 LED Driver

For many years, the key concern for cellular power management was to optimize the voltage regulator efficiency while converting the nominal 3.6V provided by the Li-On battery to the 3.3V required by the baseband processor. But, as the cell phone manufacturers driven by consumer market began to load their products with additional features and functions new challenges in cellular power management were realized.

The power management of early generation white LEDs required a nominal 4.5V threshold for desired brightness. Quality of the first generation LEDs had the tendency to vary as some devices would be dim at 4.5V; while others were exceptionally bright owing to the exponential relation between LED luminance and forward voltage. This prompted LED driver designers to evolve constant-current LED regulators, along with the ability to drive arrays with LEDs in parallel and series for better luminance [6]. These regulators were required to step up the nominal 3.6V provided by Li-On battery to 4.5V. Hence the early generations of LED drivers were step up voltage regulators with constant output current drive.

Over the years, technological improvements have resulted in lowering of the LED forward voltages while achieving similar luminance. Most recent Flash LEDs have threshold voltage in the range of 3.0V to 4.0V for a current drive of about 1A [5]. For an optimized LED power management, this essentially means that the driver has to step up or step down the nominal 3.6V battery voltage to the desired LED threshold voltage. Achieving this optimal step-up and step-down functionality has been the primary motivation in the design of high efficiency flash LED drivers. This major shift in Flash LED driver design becomes even more desirable considering the decreasing trend of LED forward voltages. Moreover the

future generation of batteries would behave more capacitive having its life time distributed uniformly from 3.0V to 5.2V rather than being concentrated at 3.6V like in today's Li-On battery. In view of these current and future trends in flash LED power management, the focus of this research is to investigate novel and highly efficient LED driver topologies and control, providing extended battery life time and hence allowing the integration of additional features and functions in modern day cellular phones.

1.3 Thesis Organization

Chapter 2 illustrates various characteristics of flash LED's and their performance parameters helpful in achieving the desired light output in the most efficient way. Based on the end application various LED configurations are also discussed.

A through study and development of various LED driver topologies and control strategies is done in Chapter 3. Each topology is presented with its advantages and disadvantages. The chapter also identifies the need of a novel Flash LED driver architecture for current and future use in cellular camera phones.

Since the goal of this thesis is to realize a highly efficient Flash LED power management scheme, Chapter 4 provides the sequential development of a novel flash LED driver architecture and its control strategy. Circuit design and experimental results are presented in Chapter 5 and 6, respectively.

CHAPTER 2. LIGHT EMITTING DIODE (LED)

The Light emitting diode (LED) is a solid-state component which emits light when current is passed through it. Physically, the LED resembles a p-n junction diode typically based on the mixture of n-type and p-type semiconductor material. An n-type semiconductor has electrons as the majority charge carriers while the p-type semiconductor has holes as the majority charge carriers. When these p-type and n-type semiconductors are fused the electrons from the negatively doped (n-type) semiconductor move to the positively doped (p-type) semiconductor. These migrating electrons from the n-type region and holes from the p-type region recombine in the vicinity of the junction to form the depletion region, in which no charge carriers remain [7]. Thus, a static charge is established in the depletion region that inhibits current flow, unless an external voltage is applied. When sufficient positive and negative voltages are applied to the p-type and n-type regions respectively, the electrons from the n-type region and the holes from the p-type region gain sufficient energy to overcome the change in the depletion region and combine. This recombination of an electron with a hole releases energy. Based on the physical properties of the p-n junction materials, the released energy can be either non-radiative, as for the typical diode, or in the form of photonic emissions as in the Light Emitting Diodes (LEDs). For an LED, the wavelength of the emitted light (i.e., its color) depends on the band gap characteristics of its p-n junction material [7]. Fig. 2.1 illustrates the operation of an LED.

There are many factors which make LEDs eye-catching for high-performance modern electronics. For example, their higher light output per watt than com-

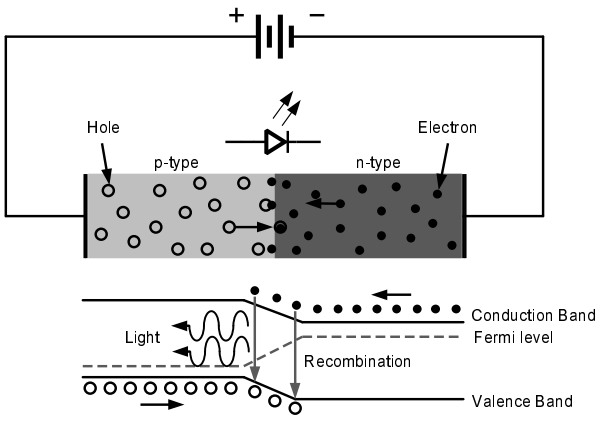


Figure 2.1: Operation of an LED.

peting technologies extends battery life and thus they are well suited for portable applications. In addition, an LED's fast turn-on/turn-off characteristics perfectly fit with the needs of automotive tail lights, especially the brake lights, since it improves safety by providing drivers more response time. LEDs have an exceptionally long lifespan, which enables their use in applications where long-term reliability is highly desirable, such as traffic lights. Machine vision systems require a focused, bright, and homogeneous light source-LEDs are a great match. LEDs, with their simple-to-implement dynamic light-tuning feature are also being used for home lighting and dimming [8].

Featuring small size, long battery life and high durability, LEDs are expected to be used in a variety of new applications as a next-generation lighting source. Nevertheless, engineers are faced with numerous challenges in LED lighting like optimizing LED light output, selecting the LED configuration, designing high efficiency LED drivers, achieving uniform light emission, LED thermal management etc. [9]. To maximize the benefits of LEDs, it is critical to understand its characteristics and select appropriate driving circuits according to the applications.

As the focus of this thesis is to realize a novel power efficient Flash LED driver, the rest of the section discusses some of the important selection criteria to obtain maximum light output per unit power for flash application in camera phones.

2.1 Flash Output Light Optimization.

In order to quantify the LED selection procedure it is important to understand the terms *Luminous flux* and *Luminous Efficacy*.

Luminous flux is defined as the rate of flow of light per unit of time and its units are Lumens. Luminous flux is the quantitative measure of the brilliance of a source of visible light. More the luminous flux, brighter the LED source appears.

Luminous efficacy is defined as the ratio of *luminous flux* (in lumens) to *power* (in watts) and thus describes how well the source provides visible light from a given amount of electricity.

$$\text{Luminous efficacy} = \frac{\text{Luminous flux}}{\text{Power}} \left(\frac{\text{Lumens}}{\text{Watt}}\right) \tag{2.1}$$

In order to optimize the light output of a Flash LED it is important to answer two main questions. The questions being how much illumination is required and how much power can be used to provide the illumination. Based on the luminance target and the power budget three major ways could be identified to increase and optimize the brightness of the Flash event. These three ways as discussed below are LED selection, LED current drive, and LED configuration; all playing significant role in the optimization of LED light output [10].

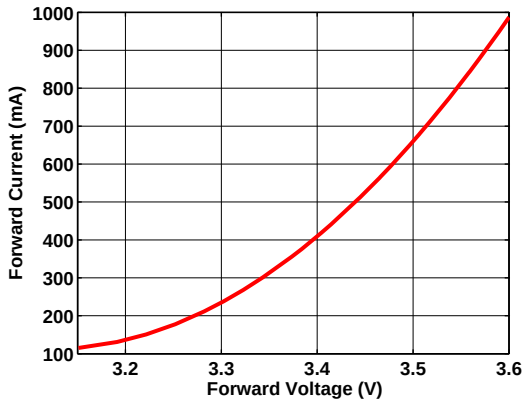


Figure 2.2: Forward Current vs. Forward Voltage of LED.

2.1.1 LED Selection

As discussed earlier, brightness of the LED depends on its luminous flux (lumens). An LED with a higher luminous efficiency emits a higher amount of luminous flux for a given power. Hence, the LED with higher lumens per watt should be selected. Fig. 2.2 shows LED forward current vs. forward voltage while Fig. 2.3 shows luminous flux vs. LED forward current of a Philips luxon flash part LXCL-PWF3 LED [5]. Luminous efficiency could be obtained by dividing the luminous flux by the product of drive current and the corresponding forward voltage. Apart from the optical performance of the LED, size, cost and complexity of the lens required to maximize the illuminance also need to considered for the selection of flash LED for camera phone application.

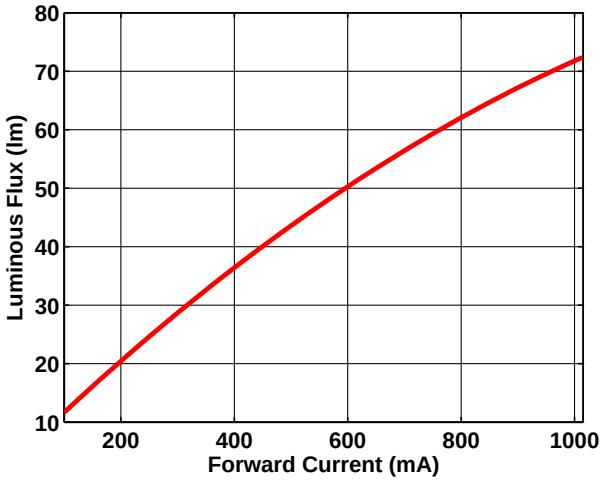


Figure 2.3: Luminous Flux vs. Forward Current of LED.

2.1.2 LED Drive Current

The light output of a Flash LED could be increased by increasing the actual drive current. As indicated from luminous flux vs. LED forward current curve in Fig. 2.3, increasing the diode current from 500mA to 1A makes the LED brightness to increase by approximately 30 lumens. But,this increase in LED luminance by increasing LED drive current comes at the expense of decreasing LED luminous Efficiency. As can be seen from Fig. 2.2, increasing the diode current also increases its forward voltage. This essentially means that Luminous efficiency of the LED decreases with increasing drive current as indicated in Fig. 2.4. This increase in LED power in turn requires higher input power from the limited battery source and lays the foundation of various LED configurations as will be discussed next.

Hence, to optimize the light output for given LED driver current within a system, combination of data from Fig. 2.2, Fig. 2.3, and Fig. 2.4 has to be used.

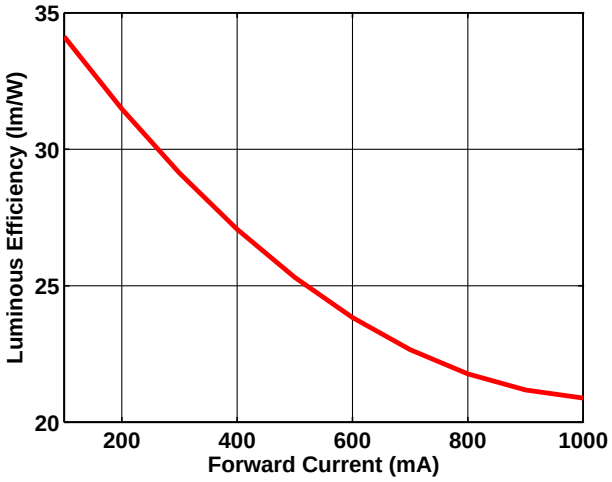


Figure 2.4: Luminous Efficiency vs. Forward Current of LED.

2.1.3 LED Configuration

Based on the illumination target sometimes multiple LEDs are required. If the output light obtained after the drive current optimization of a high luminous flux and efficacy LED is not sufficient then additional LED's are needed to achieve the desired luminance. After a visual inspection of the Luminous flux vs. LED forward current of a Philips luxon flash in Fig. 2.3. it can be concluded that the relation between luminous flux and LED forward current is non-linear. Increasing the diode current from 500mA to 1A changes luminous flux from 45 lumens to 75 lumens. Hence, two LED's running with half the flash current produce better luminance than a single LED with twice the drive current. This also helps in reducing total LED power as the forward voltage of the LED's also reduce with the reduction in its drive current. Multiple LED's are hence connected either in series or parallel each having its own advantages and disadvantages. Figure 2.5(b) and (c) show series and parallel connected LED's respectively.

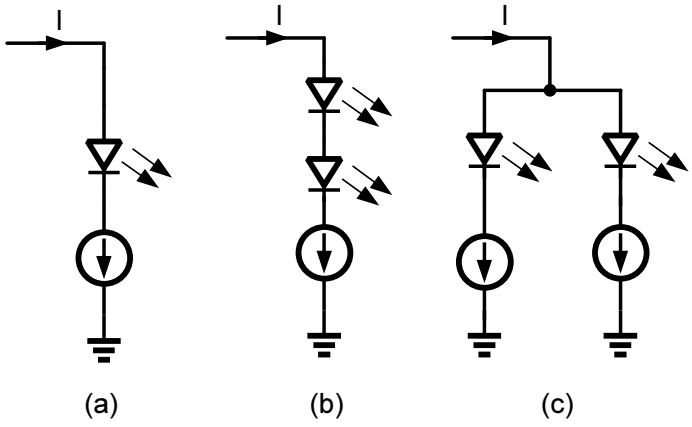


Figure 2.5: (a) Single LED. (b) Series LED. (c) Parallel LED.

Connecting multiple LED's in series ensures that all the LED's carry the same drive current and hence produce similar luminance. Series connection also requires lesser number of routes from the driver to the LED. However, as the number of series connected LED's increase so does their cumulative voltage drop eventually limiting the number of LEDs that can be put in series [6]. Additionally, a series connected LED driver may also need higher voltage processes.

Parallel connected LEDs can be used either in common cathode or common anode configuration. All the common terminals could be tied to a large ground or supply plane resulting in better thermal management. Parallel connection of LED's also permit lower voltage processes to be used. Parallel connection of LEDs provide additional flexibility for the product manufacturers to use the same LED driver to drive any given number of LED's required for particular application hence making LED driver more versatile. However, in order to ensure similar current flow in all the LEDs additional matched circuits are required [6][11].These additional circuits increase the chip area and also require multiple routes from the driver to the LEDs.

2.2 LED for the Research

As discussed earlier, the two main constraints in the design of a flash LED driver are the required light output and peak current consumption from the battery. There are severe peak current restrictions on batteries in mobile phones, as too much current drawn from the battery during the flash event can cause the phone to shut down [12]. On the other hand, as camera resolution doubles or triples, the pixel size is reduced to accommodate the larger number of pixels. This reduction in pixel size in turn require more light for better image quality. To support good image quality in today's camera phones an LED current of 1.2A was chosen for the purpose of this project [12]. Based on the analysis of LED drive current and LED configuration with high luminous flux and efficacy, further increase in the luminance is achieved by connecting two LED's in parallel rather than using a single LED. With two LEDs connected in parallel each carrying 600mA current, maximum luminous flux of 100 lumens could be obtained for the flash event. Parallel connection was chosen to provide the flexibility of using either one or two LEDs as per the illumination requirement. This also enables the usage of a low voltage 5.5V, 500nm CMOS process for the purpose of this project. Additionally, flexibility is provided to change the LED flash current level from 0.1A to 1.2A in 32 steps. Further, the LEDs could be used in torch mode (constant current flowing through the LED) for better video recording quality.

2.3 Summary

Light Emitting Diodes are semiconductor devices which emit light on application of forward voltage across them. Present day LED's feature small size, high durability and low power consumption making them highly suitable for various applications. These properties of LEDs make them suitable for driving illumination in mobile handsets. For a given input power budget, there are three main ways to increase and optimize the brightness of a flash event to help the designer reach the illumination target. LED selection, LED current drive, and LED configuration all play a huge role in optimizing the light output of a given flash LED driver. For the purpose of this research two LED's connected in parallel each carrying up to 600mA of current are used.

CHAPTER 3. FLASH LED DRIVER

As discussed in Chapter 2, Luminance of a flash LED could be controlled by its drive current. Hence the objective of an LED driver is to convert the battery power in to a fixed accurate current to achieve the desire brightness levels. Due to limited battery power and desire to integrate more features in today's handheld devices it is required that this conversion takes place as efficiently as possible. Apart from efficiency, cost and size of the LED driver also play an important role. Most of the present day camera phones are operated using a Li-On battery providing varying voltage from 3.0V to 5.2V over its recharge cycle. For good image quality, LED driver needs to provide about 1A of current to the LEDs from the above mentioned Li-On battery to achieve desired illumination during the flash event. Flash drive current of 1A may requires LED forward voltages to be in the range of 3.0V to 4.0V depending on the manufacturer. Based on these Input/Output specifications for an LED driver this chapter discusses various kinds of Flash LED driver architectures. The three important parameters i.e. efficiency, cost, and area are used to identify the advantages and disadvantages of each topology. These short-comings of the present day LED drivers is the primary source of motivation of this thesis work which leads to the development of a new architecture and control strategy of the LED driver as described later in Chapter 4.

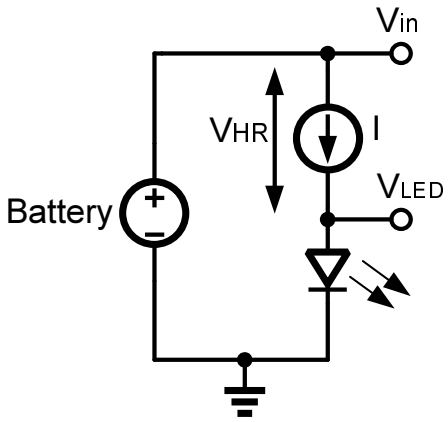


Figure 3.1: Current LED Driver Topology.

3.1 Current Source LED driver

Fig. 3.1 shows the simplest and the most basic LED driver. Fundamentally, a constant current is provided directly to the LED from the battery. However, this LED driver suffers from several drawbacks. First, in order to provide output current, I, the architecture requires the battery voltage to be always greater than the LED forward voltage plus the minimum headroom voltage required to support the current source. Second, efficiency of the driver decreases as the difference between the battery voltage, V_{in}, and the LED forward voltage, V_{LED}, increases. This difference is dissipated as the headroom across the current source. To quantify the driver efficiency, consider the following representative example.

Li-On Battery Voltage = V_{in} = 3.0 V - 5.2 V

LED Drive Current = I = 1 A

LED Forward Voltage = V_{LED} = 3.1 V

Minimum Current Source Headroom = V_{HRmin} = 0.3 V

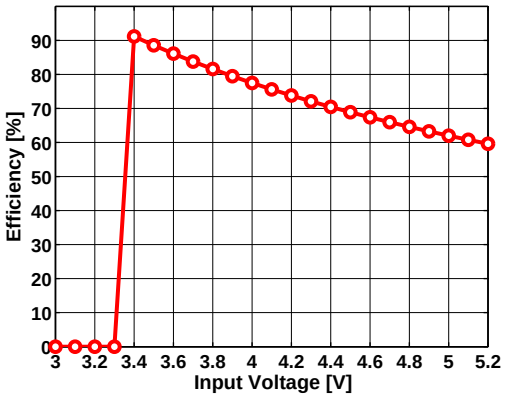


Figure 3.2: Efficiency Vs. Battery Voltage of Current LED Driver Topology.

The efficiency, η, when $V_{in} \geq (V_{LED} + V_{HRmin})$ is given by

$$\eta = \frac{\text{LED Power}}{\text{Input Power}} \tag{3.1}$$

$$= \frac{P_{out}}{P_{in}}$$

$$= \frac{V_{LED} \times I}{V_{in} \times I}$$

$$= \frac{V_{LED}}{V_{in}} \tag{3.2}$$

Figure 3.2 shows the efficiency of the cu8rrent source LED driver. The driver provides good efficiency ($> 85\%$) when V_{in} is equal to $(V_{LED} + V_{HRmin})$. Efficiency at higher V_{in} decreases, as the voltage drop (V_{in} - V_{LED}) across the current source also increases. On the other hand, the efficiency hit at low input voltages is caused by the reduced headroom across the current source, forcing the current source to be inactive. In view of these observations, the efficiency of the LED driver could be vastly improved by satisfying the following two conditions,

1) Efficiently step up the input voltage when $V_{in} \leq (V + V_{HRmin})$.

2) Ensuring reduced voltage headroom across the current source when $V_{in} \geq (V_{LED} + V_{HRmin})$.

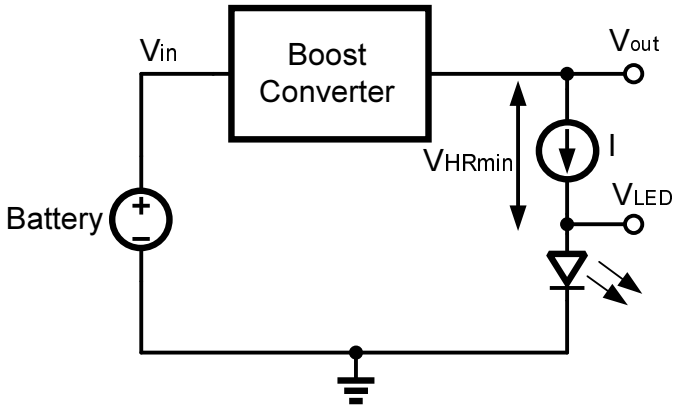


Figure 3.3: Block Diagram of Boost LED Driver.

These requirements for an efficient LED driver could be achieved by employing a step-up DC-DC conversion of the battery voltage. The battery voltage should be be stepped up by the factor represented in equation 3.3 in order to achieve reduced current source headroom.

$$\text{Step} - \text{up Factor} = \frac{\text{V}_{\text{LED}} + \text{V}_{\text{HRmin}}}{\text{V}_{\text{in}}} \tag{3.3}$$

Step-up DC-DC converters are also called Boost Converters [4]. Fig. 3.3 conceptually shows boost converter driving a Flash LED. The following section discusses various ways of implementing a Boost converter and presents efficiency analysis for each implementation.

3.2 Boost Converter: LED driver

Step up or Boost DC-DC converters can be implemented in two basic configurations: Capacitive and Inductive. The following section describes the architecture, advantages and disadvantages of each converter.

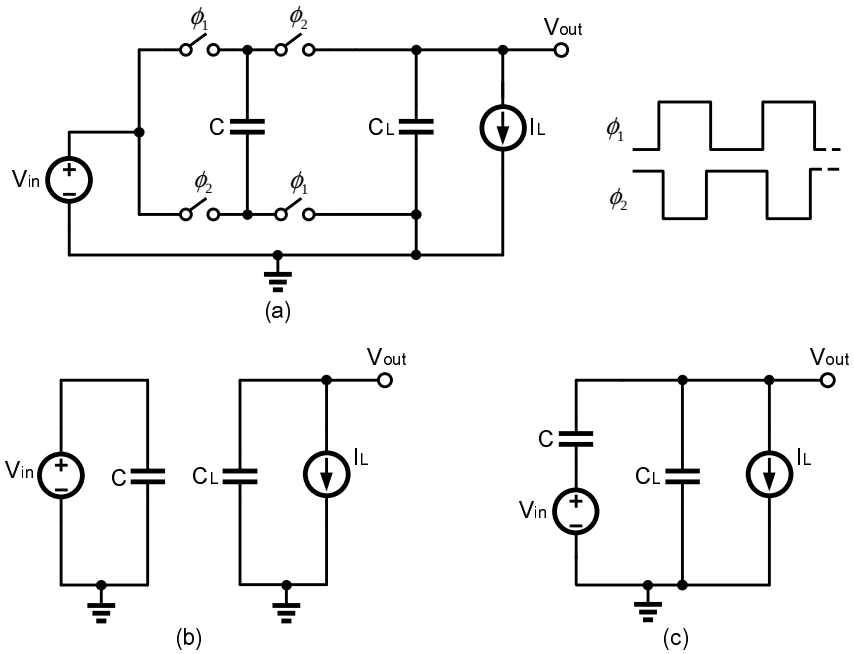


Figure 3.4: (a) Capacitive voltage doubler. (b) Voltage doubler during Phase 1. (c) Voltage doubler during Phase 2.

3.2.1 Capacitive Boost Converter

A capacitive Boost converter provides a voltage that is higher than the voltage of the battery. Capacitive boost converters operates by switching on and off a large number of MOS switches which charge and discharge a large number of capacitances connected either in series or in parallel, transferring energy to the output load. The switches can be easily implemented on CMOS technology and based on the required size, the capacitors can be on or off chip.

A switched-capacitor organization of a two phase DC-DC voltage doubler is shown in Fig. 3.4. It contains two out of phase clocks controlling the switches and one capacitor C. For a simple operation, during phase 1 the capacitor C is connected in parallel to the input supply. This charges C to input battery voltage

V_{in} and the capacitor holds the charge CV_{in}. In phase 2 capacitor C is connected in series with the input supply. The voltage across the capacitor changes from V_{in} to $(V_{out}-V_{in})$. The charge stored in the capacitor is given by $C(V_{out}-V_{in})$. Assuming an ideal lossless stable system and applying the principal of charge conservation, capacitor charge in phase 1 should be equal to capacitor charge in phase 2.

$$CV_{in} = C(V_{out} - V_{in}) \tag{3.4}$$

$$V_{out} = 2V_{in} \tag{3.5}$$

Thus the output voltage is boosted two times the input voltage. This output voltage V_{out} also has a ripple component due to discharging of the load Capacitor C_L while providing the load current I_L. The charging and discharging of the capacitors will always be performed through a series switch resistance resulting in energy dissipation. No matter what the size of the series resistance is, the energy loss depends only on the capacitance, making the loss inevitable. As a result, the peak efficiency of capacitive converters is limited by their equivalent output resistance, given by $1/(fC)$ where f is the switching frequency and C is the charge transferring capacitor [13]. As a result of their conversion technique, capacitive Boost converters can only generate specific fractions of the supply voltage and the output. Generally, a larger number of capacitors is required to generate output voltages that are fractions of the input supply. For example, to generate output which is 1.5 times the input, two capacitors are required as shown in Fig. 3.5. The capacitors are charged in series during the first clock phase, and stacked in parallel on top of V_{in} on the second clock phase. The charge conservation in the two phases leads to the output equal 1.5 times the input.

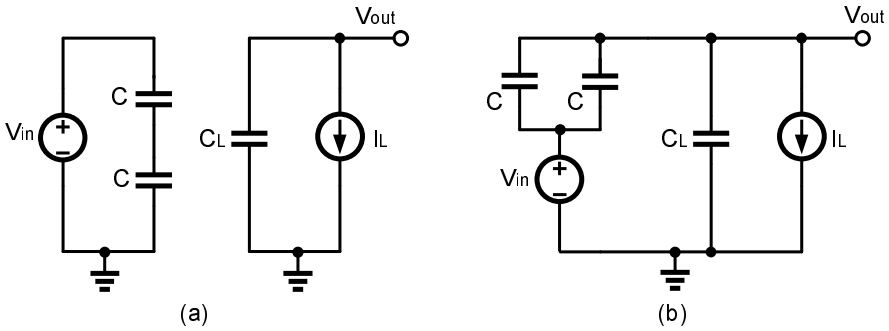


Figure 3.5: (a) 1.5x capacitive boost in Phase 1. (b) 1.5x capacitive boost in Phase 2.

$$\frac{C}{2}V_{in} = 2C(V_{out} - V_{in}) \tag{3.6}$$

$$V_{out} = 1.5Vin \tag{3.7}$$

Referring to Fig. 3.3 and the two conditions for improving the efficiency of an current source LED driver i.e.

1) Efficiently step up the input voltage when $V_{in} \leq (V + V_{HRmin})$.

2) Ensuring reduced voltage headroom across the current source when $V_{in} \geq (V_{LED} + V_{HRmin})$.

it can be inferred that capacitive boost LED driver has better efficiency compared to current source LED driver over the entire battery voltage range. When the input voltage is lower than the sum of LED forward voltage, V_{LED}, and minimum current headroom, V_{HRmin}, the capacitive LED driver boosts the input to satisfy condition 1). However, as capacitive boost converter can only step up the output to a fraction of the input, condition 2) is rarely satisfied. The extra boosted voltage is dropped across the output current source causing efficiency degradation. This extra voltage headroom across the current source could be reduced by having the flexibility to boost the input voltage by various fractions like 1.5x and 2x

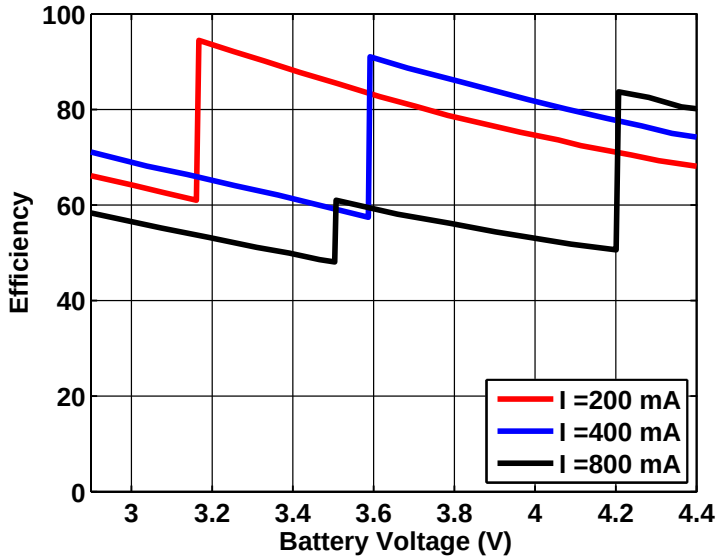


Figure 3.6: Efficiency Vs. Battery Voltage of Capacitive LED Driver Topology LTC3216.

as is done in the capacitive boost flash LED driver part LTC3216 from Linear Technology Corporation [14].

Optimization of efficiency in LTC3216 is achieved by using three modes, namely 1x, 1.5x, and 2x. The part operates in 1x mode which basically is shorting input to the output. As the input battery voltage decreases, the voltage headroom across the current source reaches the minimum required to sustain the LED output current. At this point, the part switches to 1.5x mode providing output 1.5 times the input voltage. The extra output voltage is dropped across the current source which provides constant current to the LED. As the input voltage decreases further the part enters the 2x mode of operation where output is boosted to twice the input. Fig. 3.6 shows efficiency of a capacitive boost flash LED driver part LTC3216 from Linear Technology Corporation [14]. As discussed earlier, increasing the number of fractions requires a larger number of charge transfer capacitors and switches

thus increasing the cost of the solution. Capacitive Boost LED drivers have better efficiencies compared to current source LED drivers. But, the efficiency is not optimum as the capacitive LED driver does not always guarantee minimum headroom across the current source. Unlike capacitive Boost LED drivers, inductive Boost LED drivers can boost the input by any desired fraction thereby ensuring minimum headroom across the LED current source. The inductive boost converter is discussed next.

3.2.2 Inductive Boost Converter

An inductive boost converter provides a voltage that is higher than the battery voltage by utilizing the inductor and the capacitor as energy storage elements. The inductive Boost converter works on the principle that inductor has the tendency to resist changes in current. During charging, inductor acts like a load and absorbs energy which is later utilized during the discharge phase where it acts like an energy source. The voltage it produces during the discharge phase is related to the rate of change of current, and not to the original charging voltage, thus allowing different input and output voltages. Fig. 3.7 shows an inductive boost LED driver implemented using switches, inductor and load capacitor.

During Phase 1, the inductor is connected between the input battery source V_{in} and the ground by switch s1 for the time DT, where, D is the duty cycle and T is the period of the switching cycle. This results in an increase in the inductor current and the energy gets accumulated in the inductor. During Phase 2, the inductor is connected between V_{in} and V_{out} using switch s2, and the stored energy in the inductor is delivered to the output causing the inductor current to decrease. In order to have a stable system, the net change of inductor current over one

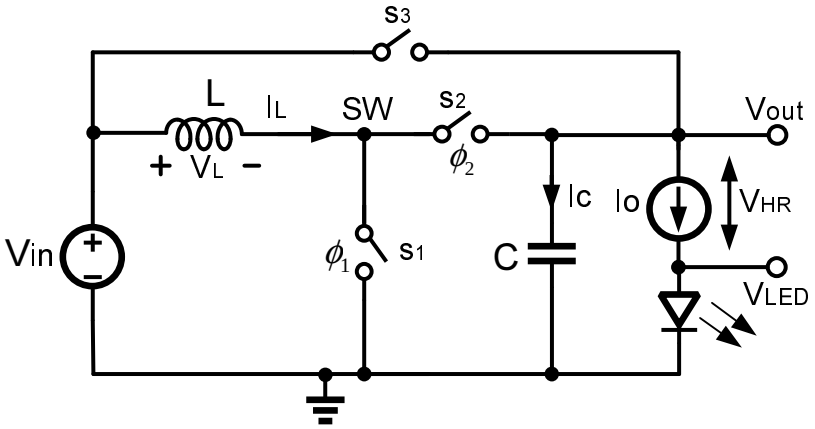


Figure 3.7: Inductive boost LED driver.

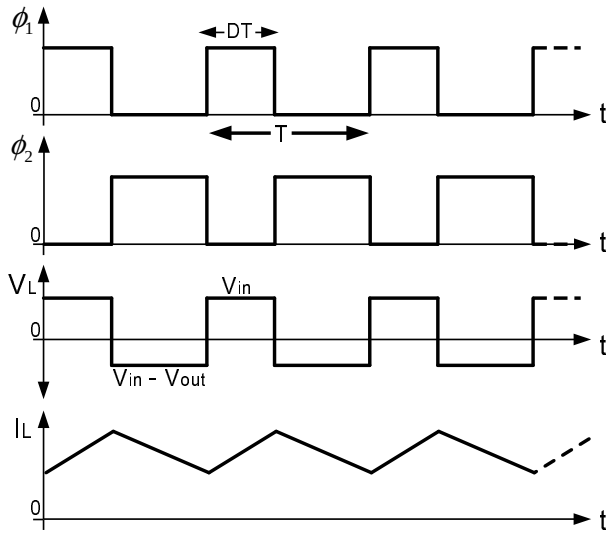


Figure 3.8: Inductive boost LED driver waveforms.

switching cycle of period T will be zero [4] leading to Eqn. 3.8.

$$i_L(T) - i_L(0) = \frac{1}{L}\int_0^T v_L(t)dt \tag{3.8}$$

$$0 = \int_0^T v_L(t)dt \tag{3.9}$$

Where the right hand side of Eqn. 3.9 is the area under the inductor voltage

waveform over one period. Eqn. 3.9 could be further solved to provide the relation between V_{in} and V_{out} as shown in Eqn. 3.10.

$$0 = DTV_{in} - (1-D)T(V_{in} - V_{out}) \tag{3.10}$$

$$V_{out} = \frac{1}{1-D}V_{in} \tag{3.11}$$

Similarly, under equilibrium condition, net change of voltage across capacitor C over one switching period will be zero leading to Eqn.3.12

$$v_c(T) - v_c(0) = \frac{1}{C}\int_0^T i_c(t)dt \tag{3.12}$$

$$0 = \int_0^T i_c(t)dt \tag{3.13}$$

$$0 = (1-D)T(I_L - I_o) - TI_o) \tag{3.14}$$

$$I_o = (1-D)I_L \tag{3.15}$$

As can be seen from Eqn. 3.11 by changing the duty cycle D of the switching cycle different fractions of output V_{out} greater than the input voltage V_{in} could be obtained. Hence, the minimum voltage headroom across the output current source could be maintained, ensuring better efficiency compared to capacitive boost converters. Inductive Boost regulator is used as an LED driver by boosting the input voltage V_{in} whenever V_{out} is greater than V_{in}. As a boost regulator cannot step down the input voltage, once the required V_{out} is sufficiently lower than V_{in}, input and the output are shorted using switch s3 and the extra voltage V_{in} - V_{out}, is dropped across the current source. With variations in input voltage, diode forward voltage, drive current, temperature and process, the headroom across the current source is regulated to the minimum by controlling the duty cycle using a Pulse Width Modulated (PWM) controller in negative feedback across the Boost converter [4].

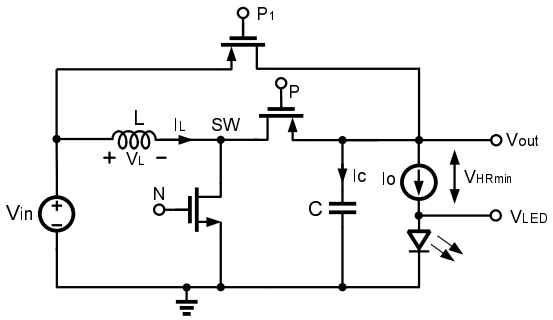


Figure 3.9: Inductive boost LED driver.

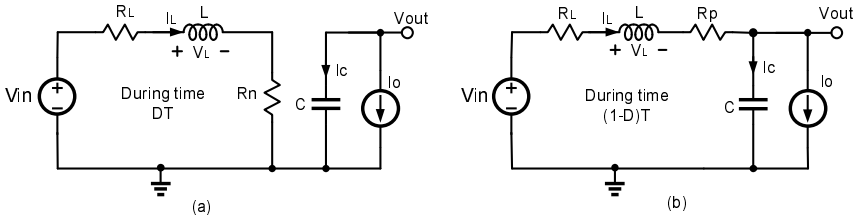


Figure 3.10: Equivalent Inductive boost LED driver in two phases.

In CMOS process the switches are implemented using N and P MOSFET, also known as power FETS, as shown in Fig. 3.9. During the turn off time the MOSFET operates in cut off region providing large resistance (ideally infinity), while during the turn on time it operates in linear region with small resistance [4][15]. The ON resistance of the FET is often optimized to maximize the overall efficiency of the driver. Fig. 3.10 shows the equivalent circuits with inductor equivalent resistance and MOS ON resistance when the switches are conducting [4], where R_p, R_n, and R_L represent PMOS, NMOS and inductor series resistances, respectively. Referring to Fig. 3.10 and applying Eqn. 3.9, the input to output voltage transfer function could be recalculated as in Eqn. 3.17.

$$0 = \mathrm{DT}(\mathrm{V_{in}} - \mathrm{I_L}(\mathrm{R_L} + \mathrm{R_n})) - (1 - \mathrm{D})\mathrm{T}(\mathrm{V_{in}} - \mathrm{V_{out}} - \mathrm{I_L}(\mathrm{R_L} + \mathrm{R_p})) \quad (3.16)$$

$$\mathrm{V_{out}} = \left(\frac{\mathrm{V_{in}}}{1 - \mathrm{D}}\right)\left[\frac{1}{1 + \left(\frac{\mathrm{R_L} + \mathrm{DR_n} + (1-\mathrm{D})\mathrm{R_p}}{(1-\mathrm{D})^2\mathrm{R}}\right)}\right] \quad (3.17)$$

$$\mathrm{V_{out}} = \left(\frac{\mathrm{V_{in}}}{1 - \mathrm{D}}\right)\eta \quad (3.18)$$

where, $\mathrm{R} = \frac{\mathrm{V_{out}}}{\mathrm{I_o}}$ and $\eta = \left[\frac{1}{1+\left(\frac{\mathrm{R_L} + \mathrm{DR_n} + (1-\mathrm{D})\mathrm{R_p}}{(1-\mathrm{D})^2\mathrm{R}}\right)}\right]$.

η in Eqn. 3.18 represents the efficiency of the boost converter [4]. As can be seen from Eqn. 3.18, the efficiency of the boost converter can be increased by decreasing the NMOS and PMOS turn on resistances R_n and R_p, respectively. A decrease in Power FET turn on resistance is obtained by increasing its aspect ratio (W/L)[15]. However, increasing the aspect ratio also increases the parasitic capacitors associated with MOS, gate, source and drain terminals. In order to charge and discharge these parasitic capacitors during the power FET turn on and turn off events, high aspect ratio power FET drivers are needed. The power FET driver is implemented as an inverter chain with the inverter drive strength increasing as the chain progresses towards the power FET. Charging and discharging of these high aspect ratio driver chain leads to significant switching power consumption which finally puts the upper bound on the power FET aspect ratio [4][16]. The minimum time required to charge and discharge the driver chain and power FET sets the limit on the minimum and the maximum duty cycle D(pulse width) at which the inductive boost converter can operate [4] [17] [18]. The maximum and minimum duty cycles are limited to about 90% and 10%, respectively. The efficiency at the node $\mathrm{V_{LED}}$ is lower than the boost converter efficiency because of the voltage headroom across the current source. The boost LED efficiency, η_{LED}

is given by Eqn. 3.22.

$$V_{out}I_o = (V_{LED} + V_{HRmin})I_o \tag{3.19}$$

$$\frac{V_{out}I_o}{V_{in}I_L} = \frac{V_{LED}I_o}{V_{in}I_L} + \frac{V_{HRmin}I_o}{V_{in}I_L} \tag{3.20}$$

$$\eta = \eta_{LED} + \frac{V_{HRmin}(1-D)}{V_{in}} \tag{3.21}$$

$$\eta_{LED} = \eta - \frac{V_{HRmin}(1-D)}{V_{in}} \tag{3.22}$$

The inductive boost LED driver operates with the LED efficiency as represented in Eqn. 3.22 when the desired output voltage, V_{out}, is greater than the input voltage, V_{in}. As the input voltage, V_{in}, decreases below the required output voltage, V_{out}, the input and the output are shorted and the current source provides the desired constant LED current. Consequently, the extra voltage drop across the output current source, V_{in} - V_{out}, makes the inductive boost LED driver grossly inefficient when V_{in} is greater than V_{out} [19].

For example,

Li-On Battery Voltage = V_{in} = 3.0 - 5.2 V

LED Drive Current = I = 1.2 A

LED Forward Voltage = V_{LED} = 3.1 V

Minimum Current Source Headroom = V_{HRmin} = 0.3 V

PMOS turn on resistance = R_p = 0.25 Ohms

NMOS turn on resistance = R_n = 0.25 Ohms

Inductor equivalent series resistance = R_L = 0.1 Ohms

The inductive boost LED driver, LED efficiency is as shown in Fig. 3.11. From the discussion above, boost LED driver could be concluded to have following drawbacks,

1) Inability to provide output voltage, V_{out}, lower than the input battery voltage, V_{in}.

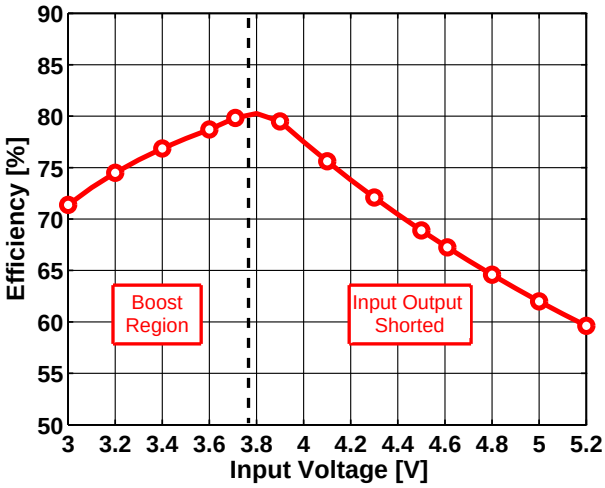


Figure 3.11: Inductive boost LED driver Efficiency.

2) Poor LED efficiency when V_{out} is lower than V_{in}.

In order to eliminate the above mentioned drawbacks of an inductive boost LED driver, the LED driver should be able to operate continuously over the entire input battery voltage range and still maintain minimum headroom across the output current source. This could be achieved by stepping up the input voltage when V_{out} is greater than V_{in} and stepping down the input voltage when V_{out} is lower than V_{in}. This operation could be achieved by using a conventional non-inverting Buck-Boost LED driver [4] as discussed in the following section.

3.2.3 Non-inverting Buck-Boost Converter

Figure 3.12 shows a Non-inverting Buck-Boost converter operating with a switching cycle of period T [4]. During the time DT switches s1 and s3 are on, while the switches s2 and s4 are off. This results in an increase in the inductor current and the energy gets accumulated in the inductor. During the time (1-D)T

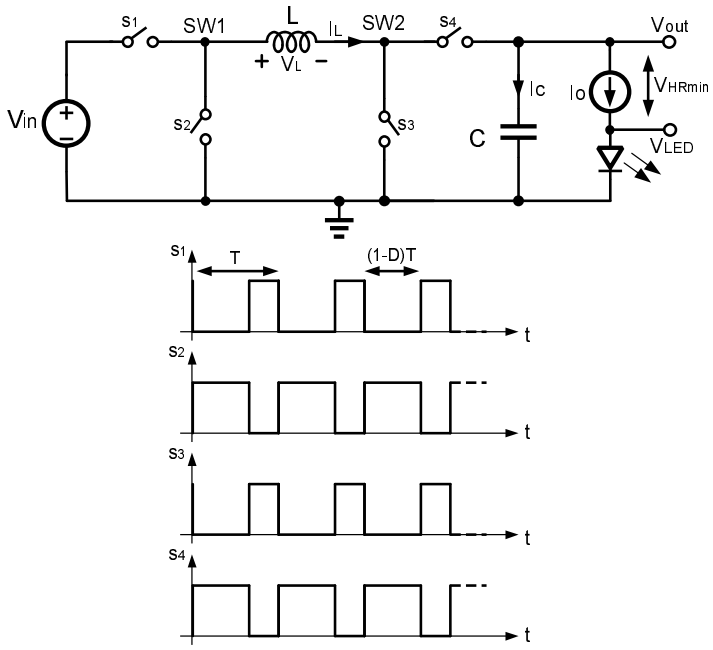


Figure 3.12: Conventional Non-inverting Buck-Boost converter.

switches s2 and s4 are on, while the switches s1 and s3 are off. During this time the stored energy in the inductor is delivered to the output causing the inductor current to decrease. The input output voltage transfer function and the relation between the inductor current and the output LED current for a conventional non-inverting buck-boost LED river are shown in Eqn. 3.23 and Eqn. 3.24, respectively.

$$V_{out} = \left(\frac{D}{1-D}\right) V_{in} \tag{3.23}$$

$$I_L = \left(\frac{1}{1-D}\right) I_o \tag{3.24}$$

The non-inverting buck-boost converter can both step-up and step-down the input battery voltage, V_{in} in order to obtain the desired output voltage, V_{out}. From Eqn. 3.23, for D lower than 0.5, V_{in} is greater than V_{out}. While, for D greater than 0.5, V_{in} is lower than V_{out}. At D = 0.5, both V_{in} and V_{out} are equal. The conventional non-inverting buck-boost converter however requires much larger

average inductor current, I_L compared to the inductive boost converter. This is due to the fact that buck-boost converter requires much larger duty cycle, D, compared to boost converter for obtaining the same V_{out} for a given V_{in} (see Eqn. 3.11 and Eqn. 3.23). For Example, in order to obtain V_{out} around V_{in}, buck-boost converter requires $D = 0.5$ while the boost converter required $D = 0$, leading to twice as much inductor current in buck-boost converter compared to the boost converter (see Eqn. 3.15 and Eqn. 3.24). This increase in the average inductor current increases the conduction loss across the switches and the inductor series resistance making the conventional non-inverting buck-boost converter grossly inefficient compared to the boost converter.

The efficiency of the non-inverting buck-boost converter could be greatly enhanced by keeping the average inductor current close to the one obtained in the inductive boost LED driver, but still being able to step-up or step-down the input voltage so as to obtain the desired output voltage. The proposed buck-and-boost LED driver strives to achieve the above mentioned conditions for an highly efficient LED driver as discussed next.

3.2.4 Buck-and-Boost Converter

The proposed Buck-and-Boost converter employs three modes of operation namely, Buck, Buck-and-Boost, and Boost, and maintains high efficiency over the entire operating range of the Li-On battery. By operating in the above mentioned modes the converter strives to keep the average inductor current, I_L as low as possible so as to achieve the highest possible efficiency. The architecture of the Buck-and-Boost converter is shown in Fig. 3.13. It comprises of four switches s1, s2, s3, s4 and an inductor, L, and output capacitor, C. Switch combination s1 and

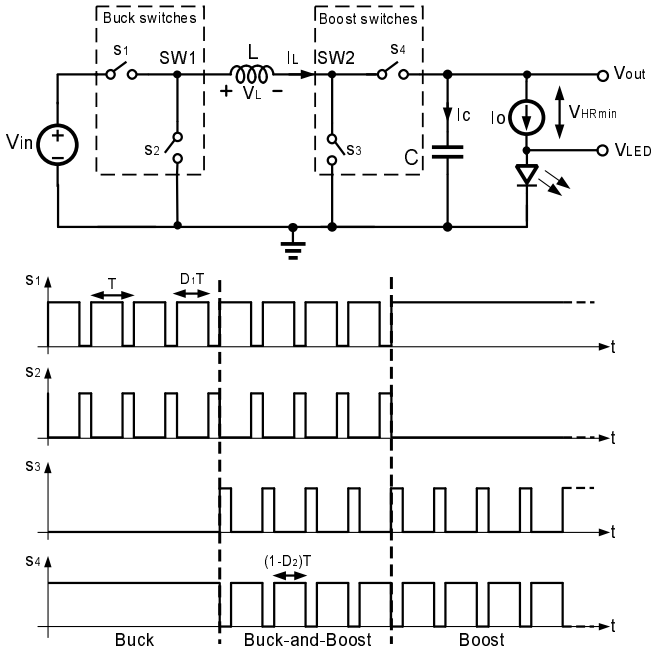


Figure 3.13: Proposed Buck-and-Boost Converter.

s2 is called Buck switches while the combination s3 and s4 is called Boost switches. The operation of the converter is explained next.

When V_{in} is greater than the desired V_{out}, the converter operates in the Buck mode during which s3 is off and s4 is always on. Switches s1 and s2 are controlled by a pulse-width modulated (PWM) control signal with a duty cycle D1 such that V_{out} equals $D1V_{in}$ and the inductor current I_L equals LED current I_o, like in a conventional buck converter [4]. On the other hand, when V_{in} is lower than the desired V_{out} the converter operates in the Boost mode. In this mode, s2 is off and s1 is always on and switches s3 and s4 are controlled by a PWM control signal with a duty cycle D2 such that V_{out} equals $V_{in}/(1 - D2)$ and I_L equals $I_o/(1 - D2)$. As discussed earlier in the section of inductive Boost converters that in practice, the maximum and minimum duty cycles are limited to about 90% and

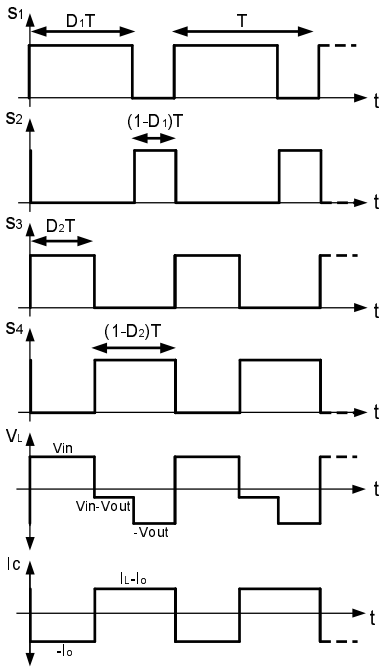


Figure 3.14: Timing waveforms during Buck-and-Boost operation.

10%, respectively. Hence, neither the Buck-mode nor the Boost-mode can regulate V_{out} when V_{in} is in the vicinity of the desired output voltage. Under this condition, in the proposed architecture, the converter operates in the Buck-and-Boost mode where PWM signals are applied to all the four switches s1, s2, s3, and s4. Buck switches, s1 and s2 are controlled independently by a PWM signal with duty cycle D1, while, the boost switches, s3 and s4 are controlled independently by a PWM signal with duty cycle D2. The input output transfer function and the average inductor current are derived next.

Figure 3.14 shows the inductor voltage, V_L, and the capacitor current, I_c, waveforms. The input output transfer function shown in Eqn. 3.26 is derived by applying inductor volt second balance principle while inductor current shown in

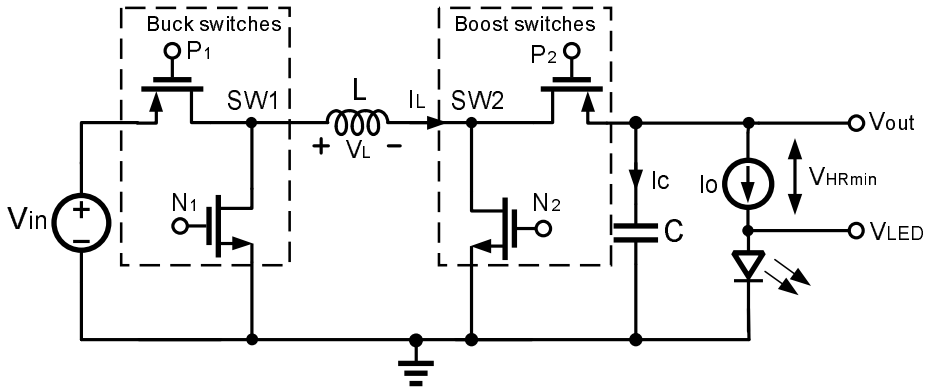


Figure 3.15: Buck-and-Boost Converter.

Eqn. 3.28 is derived by applying capacitor charge balance equation [4].

$$0 = \mathrm{D2TV_{in}} + (\mathrm{D1} - \mathrm{D2})\mathrm{T}(\mathrm{V_{in}} - \mathrm{V_{out}}) + (1 - \mathrm{D1})\mathrm{T}(-\mathrm{V_{out}}) \tag{3.25}$$

$$\mathrm{V_{out}} = \left(\frac{\mathrm{D1}}{1 - \mathrm{D2}}\right)\mathrm{V_{in}} \tag{3.26}$$

$$0 = \mathrm{D2T}(-\mathrm{I_o} + (1 - \mathrm{D2})\mathrm{T}(\mathrm{I_L} - \mathrm{I_o}) \tag{3.27}$$

$$\mathrm{I_L} = \left(\frac{1}{1 - \mathrm{D2}}\right)\mathrm{I_o} \tag{3.28}$$

As seen from Eqn. 3.26 and Eqn. 3.28, by independently controlling D1 and D2 and keeping D1 large and D2 as small as possible, the average inductor current is kept nearly equal to the Boost mode of operation as opposed to the conventional Buck-Boost converter. For example to obtain $\mathrm{V_{out}}$ equal to $\mathrm{V_{in}}$, D1 is set to the maximum value of 90%, while D2 is set to the minimum value of 10%, leading to $\mathrm{V_{out}} = \mathrm{V_{in}}$ and $\mathrm{I_L} = 1.11\ \mathrm{I_o}$ as opposed to $2\mathrm{I_o}$ in the case of conventional buck-boost converter. As a consequence, the proposed architecture offers a considerable efficiency advantage.

In CMOS process the switches are implemented using N and P MOSFET and the corresponding buck-and-boost LED driver is shown in Fig. 3.15. Following a

similar procedure as in the derivation of efficiency for inductive boost converter, the output efficiency and the LED efficiency of Buck-and-Boost converter are given by Eqn. 3.29 and Eqn. 3.30, respectively.

$$\eta = \left[\frac{1}{1 + \left(\frac{R_L + D1R_{p1} + (1-D1)R_{n1} + D2R_{n2} + (1-D2)R_{p2}}{(1-D2)^2 R} \right)} \right] \tag{3.29}$$

$$\eta_{LED} = \eta - \frac{V_{HRmin}}{V_{in}} \left(\frac{1 - D2}{D1} \right) \tag{3.30}$$

where,

R_{p1} = Buck PMOS switch turn on resistance.

R_{n1} = Buck NMOS switch turn on resistance.

R_{p2} = Boost PMOS switch turn on resistance.

R_{n2} = Boost NMOS switch turn on resistance.

R_L = Inductor equivalent series resistance.

D1 = Buck duty cycle.

D2 = Boost duty cycle.

$R = V_{out}/I_o$.

η = Output Efficiency.

η_{LED} = LED Efficiency.

The LED efficiency of the proposed buck-and-boost converter is shown in Fig. 3.16 indicating significant improvement over the Boost converter.

In order to control the duty cycles D1 and D2 with variations in input voltage and diode forward voltage but still provide constant LED drive a PWM controller is used. The PWM controller for the proposed Buck-and-Boost LED driver is discussed in the following chapter.

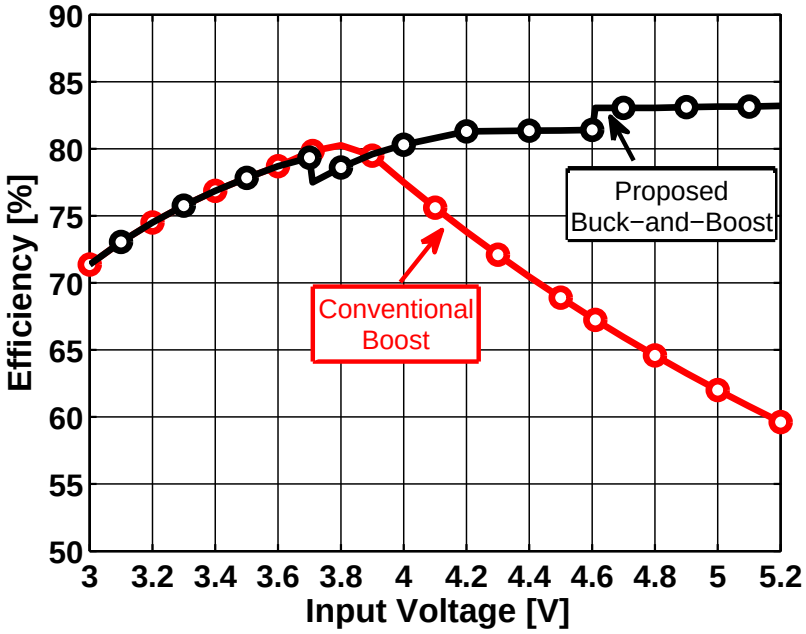


Figure 3.16: Buck-and-Boost and Boost converter efficiency.

CHAPTER 4. PWM CONTROLLER

For a Buck-and-Boost converter the controller has to operate in three modes, namely, Buck, Buck-and-Boost, and Boost. The controller has to ensure stability in all the three modes and provide smooth transitions between them. In order to achieve high efficiency in Buck-and-Boost mode, the controller has to keep the buck duty cycle (D1) large and boost duty cycle (D2) as small as possible. The controller also needs to keep the headroom across the output current source minimum, while providing the desired constant LED current. To achieve the above mentioned requirement of the controller, one of the simplest control schemes, the voltage-mode control is utilized. Voltage-mode control, controls the converter by generating the duty cycles, by amplifying the difference between the headroom across the current source and the reference. Voltage-mode control was preferred over other control schemes due to its simplicity [20].

The proposed voltage mode PWM controller is shown in Fig. 4.1. The controller regulates the drain-to-source voltage, V_{ds}, of the current source transistor Mc so as to bias it in saturation region. The first stage compares the drain-to-source voltage, V_{ds} of Mc to the reference voltage, V_{ref}. The error (V_{ds} - V_{ref}) thus generated is amplified/integrated using a Gm-C integrator in the second stage. The Gm-C integrator also serves to stabilize the loop for a dominant pole response. The choice of dominant pole compensation is explained in Section 4.1. The third stage comprises of a subtractor and a comparator which provides a smooth transition from buck duty cycle control to boost duty cycle control and vice versa while in Buck-and-boost mode. It also serves to provide smooth transition while chang-

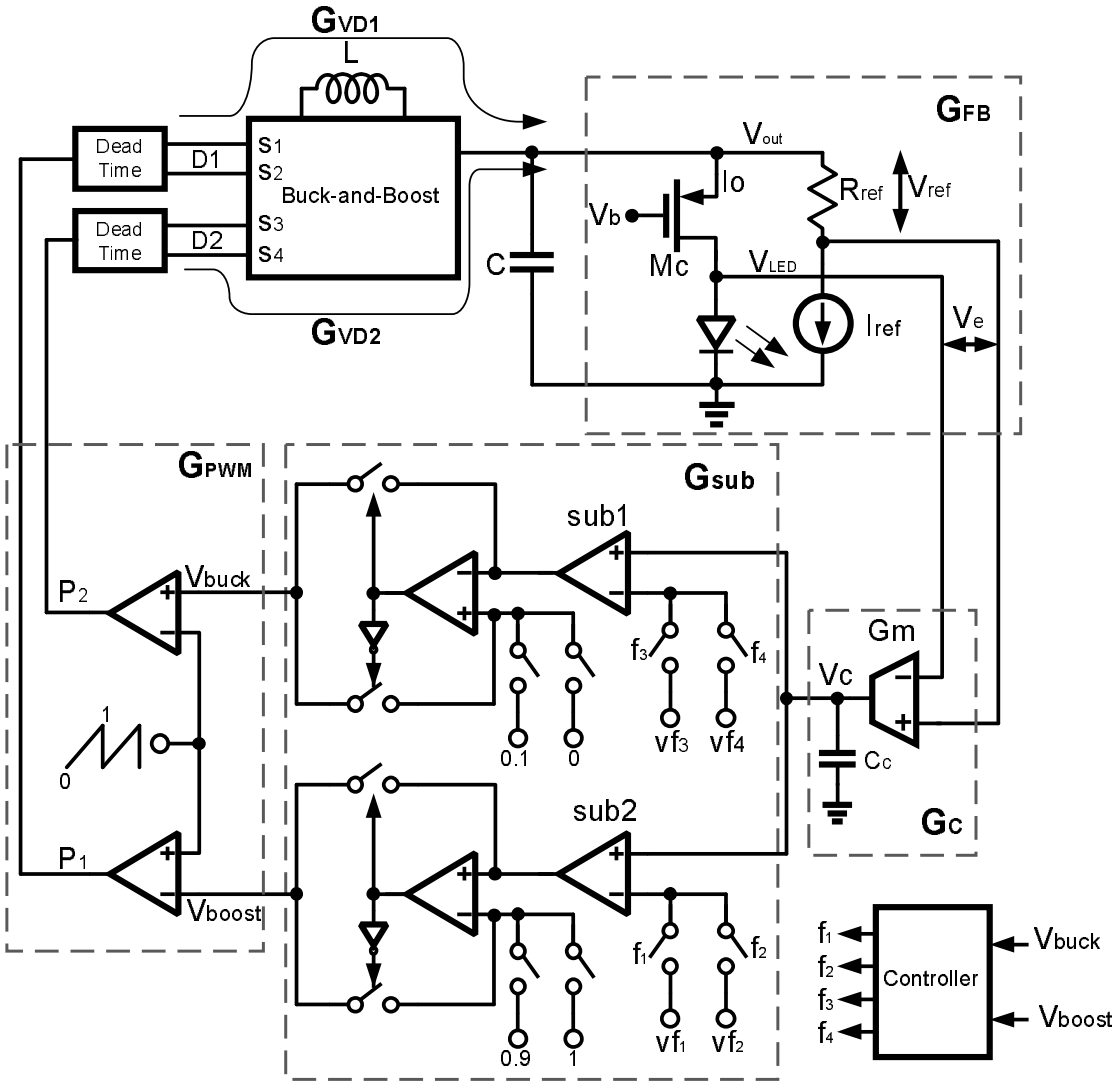


Figure 4.1: Simplified PWM controller schematic.

ing modes. The final stage, PWM comparator in Fig. 4.1 generates appropriate PWM signals P1, and P2 to drive the power switches s1, s2, s3 and s4. The mode-switching operation of the controller is described next.

The converter operates in the Buck mode when V_{in} is greater than the desired V_{out} and the controller generates PWM signals with duty cycle D1 to drive

switches s1 and s2, similar to a conventional Buck converter. As the input voltage decreases the buck duty cycle D1 increases and saturates once it reaches 85% and the controller enters the Buck-and-Boost mode. In this mode, PWM pulse P1 controls the Buck switches s1 and s2 while the PWM pulse P2 controls the boost switches s3 and s4 (see Fig. 3.10). The Boost duty cycle D2 is initially set to its minimum value of 10% and only the Buck duty cycle D1 is varied. Consequently, during this transition, D1 has to rapidly change from its 85% in the Buck mode to a lower value in Buck-and-Boost mode. As the rate of change in the duty cycle depends on the bandwidth of the overall converter, the mode transition invariably leads to a large overshoot in V_{out}. To mitigate any such overshoot and to make the mode transition smooth and independent of the regulator bandwidth a fast feed-forward path is employed as explained in section 4.3. By subtracting an appropriate feed-forward voltage, vf1 or vf2, the D1 is instantaneously changed from 85% to the desired value. Further decrease in the input voltage causes D1 to increase while keeping D2 at 10%. Once D1 increases and saturates at 90% the control shifts to Boost side causing D2 to increase from its minimum value of 10%. As the input voltage decreases further, D2 increases and the converter eventually enters Boost mode when it reaches 25%. The choice of a duty cycle threshold of 25% was based on the conduction losses in the switches and to provide continuous operation of the LED driver as explained in Section 4.2. Finally, in the Boost mode, a further decrease in the input voltage leads to increase in the Boost duty cycle similar to a conventional Boost converter.

The choice of the compensation scheme and implementation of the feed-forward path using the subtractors are discussed next.

4.1 System Transfer Function and Compensation

In order to have a stable system and understand its AC response each component in the control system is linearized and modelled by a single transfer function, using techniques presented in [4]. The objective behind finding various transfer functions is to obtain an appropriate compensation network represented by transfer function, G_c. Two control loops exist in the Buck-and-Boost converter as both the buck duty cycle D1 and the boost duty cycles D2 need to be controlled. First control loop, namely Buck loop has the loop transfer function, G_{LBuck}, as shown in Eqn. 4.1, while the second loop called the Boost loop has the loop transfer function, G_{LBoost}, given by Eqn. 4.2.

$$G_{LBuck} = G_{VD1}G_{FB}G_cG_{sub}G_{PWM} \tag{4.1}$$

$$G_{LBoost} = G_{VD2}G_{FB}G_cG_{sub}G_{PWM} \tag{4.2}$$

where,

G_{VD1} = D1 to V_{out} transfer function.

G_{VD2} = D2 to V_{out} transfer function.

G_{FB} = V_{out} to Gm-C integrator input, V_e transfer function.

G_c = Gm-C integrator input output transfer function.

G_{sub} = V_c to V_{buck} or V_{boost} transfer function.

G_{PWM} = V_{buck} or V_{boost} to D1 or D2 transfer function.

Buck duty cycle, D1, to output, V_{out}, transfer function, G_{VD1}, is given by second order Eqn. 4.3. While, the boost duty cycle, D2, to output, V_{out}, transfer

function, G_{VD2} is given by second order Eqn. 4.4 [4].

$$G_{VD1} = \frac{V_{in}}{D1} \frac{1}{\left[1 + s\left(\frac{L}{R}\right) + s^2 LC\right]} \tag{4.3}$$

$$G_{VD2} = \frac{V_{in}}{(1 - D2)} \frac{\left[1 - \frac{sL}{(1-D2)^2 R}\right]}{\left[1 + s\left(\frac{L}{(1-D2)^2 R}\right) + s^2\left(\frac{LC}{(1-D2)^2}\right)\right]} \tag{4.4}$$

where,

$R = V_{out}/I_o$.

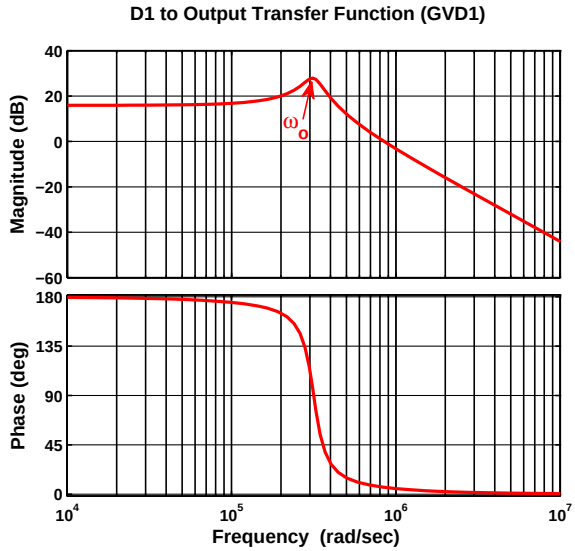
The buck transfer function G_{VD1} has a complex pole pair at $\omega_o = 1/\sqrt{LC}$ [4]. While, the boost transfer function G_{VD2} in addition to the complex pole pair at $\omega_o = (1 - D2)/\sqrt{LC}$ has an right half place zero at $\omega_z = (1 - D2)^2 R/L$ [4].

It is important to note that the right half plane zero ω_z is directly proportional to R. Hence for heavy current levels of the order of 1.2A, ω_z tends to approach the complex pole, ω_o as the duty cycle D2 increases. The right half plane zero ω_z, thus makes the phase of G_{VD2} to drop by more than 180° around the complex pole, ω_o (see Fig. 4.2(b)), making G_{VD2} as the critical function as far as stability of the converter is concerned [4].

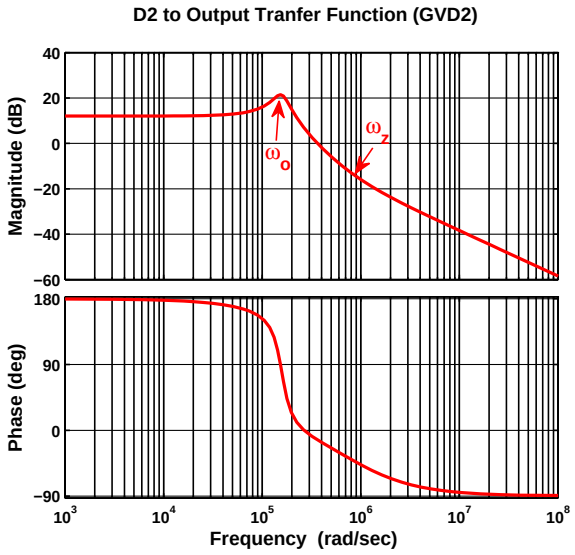
Fig. 4.2(a) and Fig. 4.2(b) shows the bode magnitude and phase plot of G_{VD1} and G_{VD2}, respectively for L = 1 μH, C = 10 μF, V_{out} = 4V and I_o = 1.2A. For G_{VD2}, the phase drops by more than 180° quickly around ω_o. Hence, to achieve the converter stability a dominant pole at a frequency much lower than ω_o was used.

Transfer function, G_{FB}, from V_{out} to V_e is equal to unity as the block only serves to subtract a fixed reference voltage, V_{ref}, from V_{out}. V_{ref} is generated using a known current source I_{ref} and a resistor R_{ref}. Hence,

$$G_{FB} = 1 \tag{4.5}$$



(a) G_{VD1}



(b) G_{VD2}

Figure 4.2: Duty cycle to output transfer functions (a) G_{VD1} and (b) G_{VD2}.

The next block serves as an amplifier as well as the loop compensator. The error generated is amplified using the Gm-C integrator whose transfer function, G_c is given by Eqn. 4.6. The integrator provides the needed dominant pole compensation for stability of the converter.

$$G_c = \frac{G_m}{sC_c} \tag{4.6}$$

The subtractor block with transfer function G_{FB}, serves the purpose of level shifting the Gm-C integrator output, V_c, by fixed voltages V_{f1}, V_{f2}, V_{f3} or V_{f4}. Hence,

$$G_{sub} = 1 \tag{4.7}$$

The last block in the control circuitry, the PWM comparator, translates the control voltage, V_{buck} and V_{boost}, into a duty-cycle of a fixed frequency. This is accomplished by comparing the control voltage with a triangle waveform and can be linearized by modelling the translation gain. This gain is essentially the amplitude of the triangle wave, V_r, as shown in Eqn. 4.8.

$$G_{PWM} = \frac{1}{V_r} = \frac{1}{1V} = 1 \tag{4.8}$$

Substituting Eqn. 4.3, Eqn. 4.4, Eqn. 4.5, Eqn. 4.6, Eqn. 4.7 and Eqn. 4.8 in Eqn. 4.1 and Eqn. 4.2, the buck and boost loop gain transfer functions are given as in Eqn. 4.9 and Eqn. 4.10, respectively.

$$G_{LBuck} = \frac{V_{in}}{D1}\frac{G_m}{sC_c}\frac{1}{\left[1 + s\left(\frac{L}{R}\right) + s^2LC\right]} \tag{4.9}$$

$$G_{LBoost} = \frac{V_{in}}{(1-D2)}\frac{G_m}{sC_c}\frac{\left[1 - \frac{sL}{(1-D2)^2R}\right]}{\left[1 + s\left(\frac{L}{(1-D2)^2R}\right) + s^2\left(\frac{LC}{(1-D2)^2}\right)\right]} \tag{4.10}$$

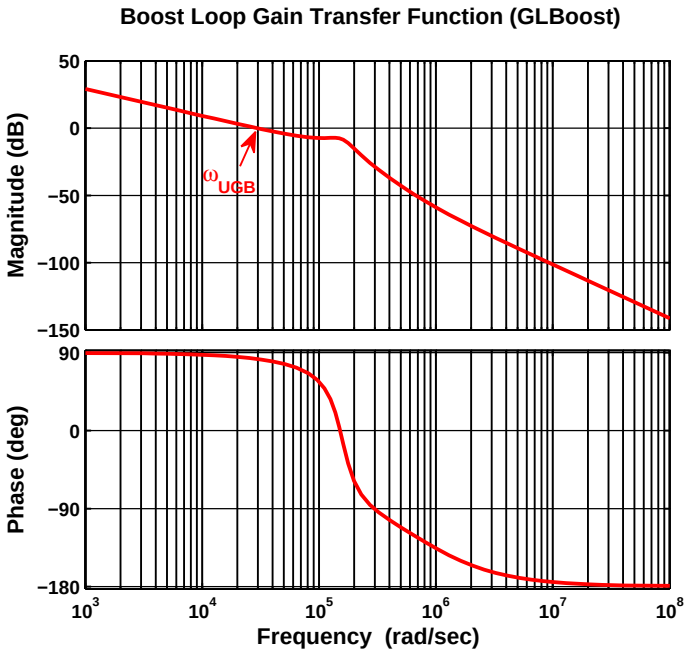


Figure 4.3: Compensated Boost Loop Gain transfer function G_{Lboost}.

In order to ensure stability of the boost loop (G_{Lboost}) with the output voltage (V_{out}), capacitor (C) and inductor (L) with process, temperature and the LED forward voltage the boost loop transfer function bandwidth was nominally set to $\omega_{UGB} = 30K$ rad/sec using a $G_m = 50\mu$mohs and $C_c = 5$ nF. Figure 4.3 shows the compensated loop gain transfer functions G_{Lboost}.

4.2 Controller

For the proposed buck and boost converter to provide continuous constant LED current, I_o, with the change in the input voltage, V_{in}, the controller should ensure smooth transition between the three modes Buck, Buck-and-Boost and Boost. Figure 4.4 shows the state diagram of the controller. The control parameter

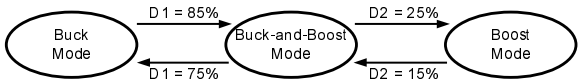


Figure 4.4: Controller State Diagram.

for transition between the modes is either the buck duty cycle D1 or the boost duty cycle D2.

As mentioned earlier the transition from Buck-and-Boost mode to Boost mode is done at D2 = 25%. A rough estimate of the value of control parameter D2 during this transition could be made by equating the output voltage equation, V_{out}, for the Buck-and-Boost and Boost mode as shown in Eqn. 4.11. Where, $D1_{bb}$ and $D2_{bb}$ are buck and boost duty cycles, respectively in Buck-and-Boost mode while D2 is the boost duty cycle in Boost mode. During the Buck-and-Boost mode to Boost mode transition, $D1_{bb}$ will be already saturated at 90% and the converter when starting in Boost mode should start at minimum duty cycle of D2 = 10% to have lesser average inductor current. Thus, the control parameter $D2_{bb}$ is found to be 19% after substituting the values of $D1_{bb}$ and D2 in Eqn. 4.11. Hence, ideally the Buck-and-Boost mode to Boost mode transition should be done when the boost duty cycle reaches 19% in Buck-and-Boost mode. However, the conduction losses in the converter causees the required $D2_{bb}$ to increase from its ideal value of 19%. Hence, the conduction losses in both Buck-and-Boost mode and Boost mode are included as shown in Eqn. 4.14 and a recursive matlab simulation is used to find the value of the desired control parameter $D2_{bb}$. Figure 4.5 shows the required boost duty cycle, $D2_{bb}$, in the Buck-and-Boost mode during the transition point for two load current settings of 1.2 A and 0.6 A. As the required boost duty cycle is always less than 25%, this particular threshold was chosen for the Buck-and-Boost

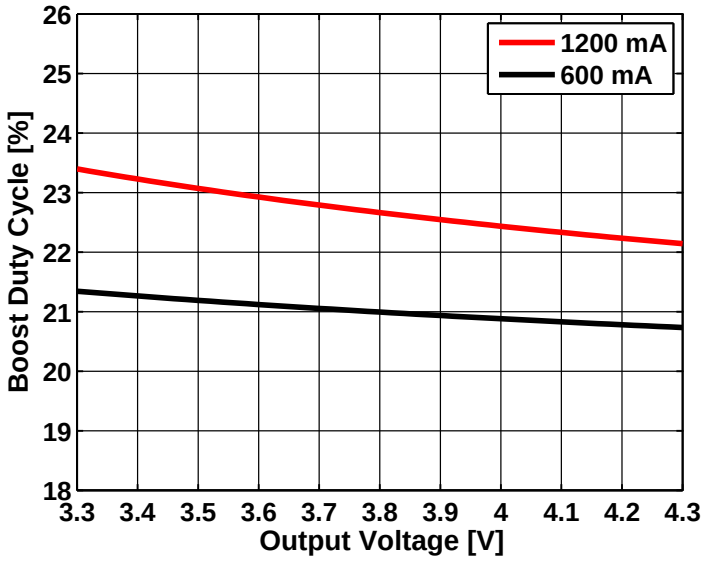


Figure 4.5: Buck-and-Boost to Boost mode: Boost duty cycle threshold.

to Boost mode transition. Similarly, the transition from Buck-and-Boost to Buck mode is done using buck duty cycle, D1 as the control parameter. This transition is done when the D1 reaches 75% in the Buck-and-Boost mode.

$$V_{in}\left[\frac{D1_{bb}}{1-D2_{bb}}\right] = V_{in}\left[\frac{1}{1-D2}\right] \tag{4.11}$$

$$\frac{0.9}{1-D2_{bb}} = \frac{1}{1-0.1} \tag{4.12}$$

$$D2_{bb} = 0.19 \; or \; 19\% \tag{4.13}$$

$$V_{out}\left(\frac{1-D2_{bb}}{D1_{bb}}\right) + \frac{I_o[R_L + D1R_{p1} + (1-D1)R_{n1} + D2R_{n2} + (1-D2)R_{p2}]}{D1_{bb}(1-D2_{bb})} \tag{4.14}$$

$$= V_{out}(1-D2) + \frac{I_o[R_L + R_{p1} + D2R_{n2} + (1-D2)R_{p2}]}{(1-D2_{bb})}$$

4.3 Buck-and-Boost Mode

As mentioned earlier in Chapter 3, to achieve high efficiency during Buck-and-Boost mode the average inductor current is set close to the one in the Boost mode. This is achieved by first keeping the boost duty cycle, D2, at its minimum possible value and controlling the buck duty cycle, D1, till it saturates to its maximum. Once D1 saturates the control is transferred to D2 causing it to increase and reach a value where Buck-and-Boost to Boost mode transition could be made. In order to achieve a smooth transition from buck duty cycle control to boost duty control in the Buck-and-Boost mode a subtractor based circuit is used.

In the proposed PWM controller, the output of the Gm-C integrator, V_c, serves to provide both the buck and the boost duty cycle D1 and D2, respectively. In other words, V_c acts as the summation of the two duty cycles D1 and D2. In Buck-and-Boost mode, at the boundary condition of buck duty cycle control to boost duty cycle control, the corresponding D1 and D2 will be 90% and 10%, respectively. For a ramp amplitude, $V_r = 1V$, at the boundary condition the Gm-C integrator output, V_c will be equal to 1V so as to provide D1 = 90% and D2 = 10%. This value of $V_c = 1V$ at the boundary condition is hence used as the parameter to move between the buck duty cycle control to boost duty cycle control while in buck-and-boost mode as indicated below.

Control D1: If (V - 0.1) $<$ 0.9: D1 = V - 0.1 and D2 = 0.1.

Control D2: If (V - 0.9) $>$ 0.1: D2 = V - 0.9 and D1 = 0.9.

This functionality is achieved using a subtractor circuit shown in Fig. 4.6 and forms the part of the control loop.

The subtractor circuit is further utilized to improve the transient response of the converter while transiting between the modes. As mentioned earlier, while

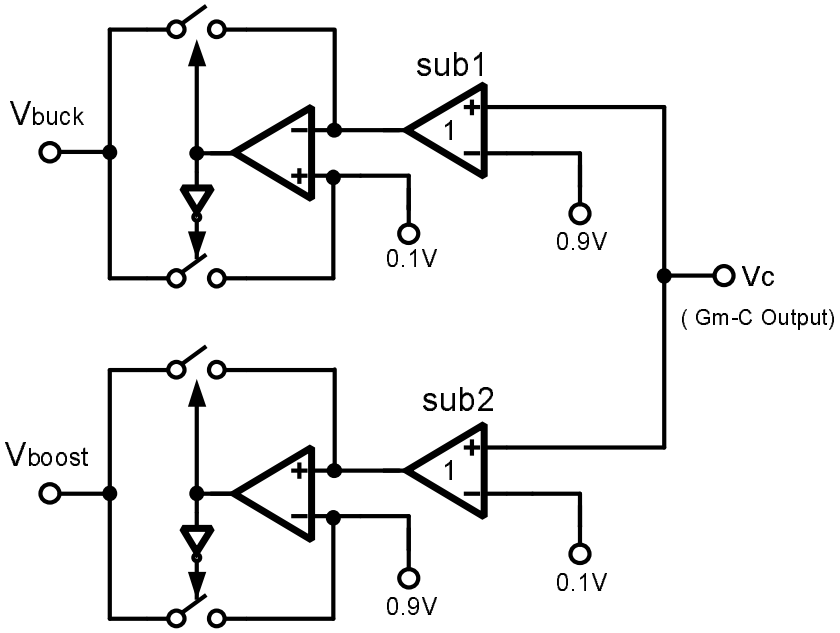


Figure 4.6: Subtractor Circuit.

transiting from the Buck mode to Buck-and-Boost mode, D1 has to rapidly change from its 85% in the Buck mode to a lower value of around 75%in Buck-and-Boost mode (see Fig. 4.4). In order to mitigate any overshoot in the output voltage, V_{out}, during the transition, an appropriate feed-forward voltage vf2 corresponding to 75% buck duty cycle is subtracted causing D1 to change instantaneously to the desired value. Similar feed-forward mechanism is used to reduce the overshoot during the Buck-and-Boost to Boost mode transition. The modified subtractor circuit is shown in Fig. 4.7.

The following chapter presents the circuit level implementation of the prototype. Gm block, subtractor circuit, PWM comparator and the dead-time circuit are discussed.

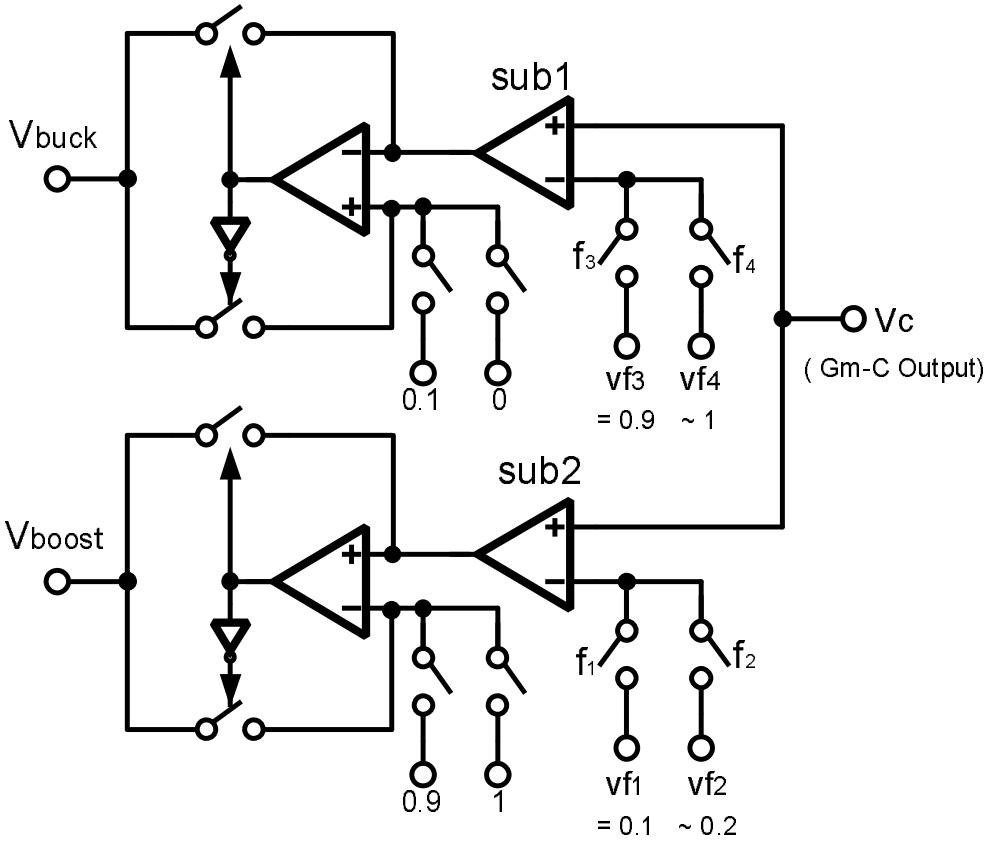


Figure 4.7: Subtractor Circuit with Feed-forward arrangement.

CHAPTER 5. CIRCUIT DESIGN

The section below discuss the circuit design of various blocks in the PWM controller.

5.1 Gm-C Integrator

The voltage applied to the input terminals of the Gm-C integrator is equal to the LED forward voltage, V_{LED} ranging from 3.0V to 4.0V based on the LED manufacturer. The transconductor amplifier has to operate with a varying input battery voltage of 3.0V to 5.2V while supporting the output voltage range of 0.6V to 2.2V based the converters mode of operation. Based on the above mentioned input/output and the supply requirements, the folded cascode architecture with NMOS input pair is utilized to implement the Gm block as shown in Fig. 5.1. In order to satisfy the stability requirements of the converter as explained in Section 4.1 of Chapter 4, the transconductor amplifier is designed to provide transconductance, G_m of 50μmohs with an output capacitor C_c of 5 nF. It is important that the transconductor offers a low input referred offset as it adds to the current source headroom thereby making the driver less efficient. The transcondcutor was designed to offer a nominal 6 mV input referred offset which is much lesser than the current source headroom of 300 mV, hence causing negligible drop in efficiency.

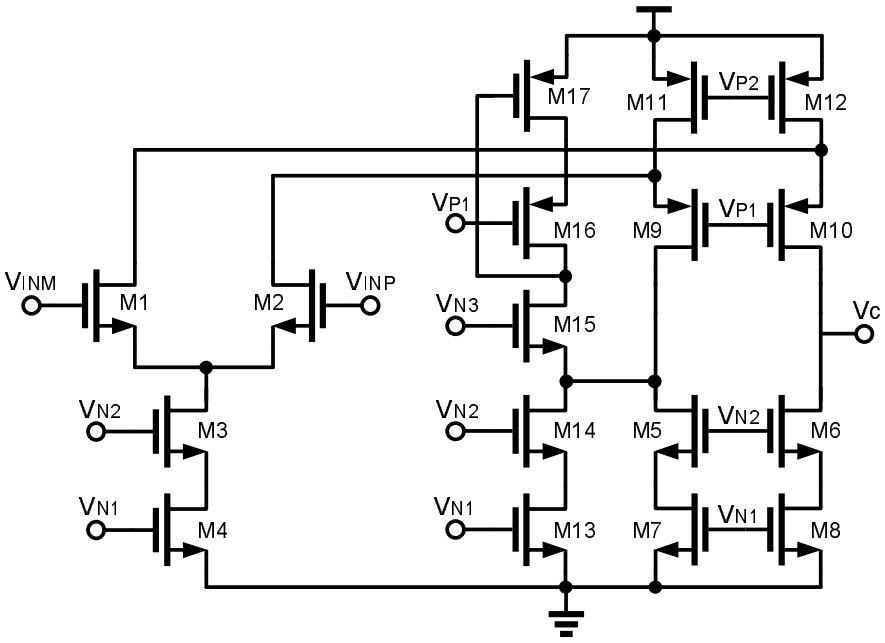


Figure 5.1: Gm-C Integrator.

5.2 Subtractor

Figure 5.2 shows the subtractor architecture comprising of an operational amplifier (OPAMP) and a negative feedback using resistors. One of the input to the subtractor comes from the Gm-C integrator output, V_c, while the other is a reference voltage, $_{f1}$. Operating from a battery supply of 3.0V to 5.2V, the OPAMP needs to support the input voltage range of 0.6V to 2.2V which is the same as Gm-C integrator output. The output of the subtractor corresponds to the duty cycle generated by the PWM comparator and hence can be as low as 100 mV to achieve 10% duty cycle. In order to support output voltage as low as 100 mV, a two stage OPAMP is utilized. The first stage of the OPAMP provides most of the gain required to ensure accuracy of subtraction, while the second stage

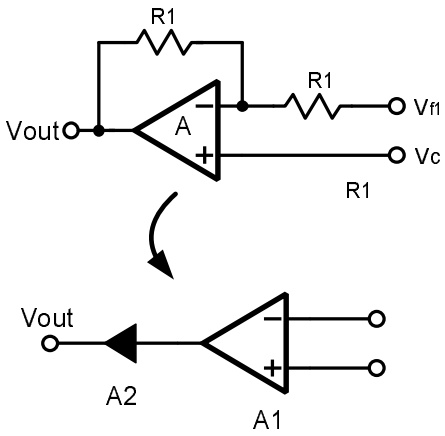


Figure 5.2: Subtractor Architecture.

provides low gain while supporting an output voltage of 100 mV. It is desired that the OPAMP offers a low input referred offset for a better subtraction accuracy. The OPAMP was designed to offer a nominal 5 mV input referred offset which is much lesser than the minimum output voltage of 100 mV. The subtractor Unity Gain Bandwidth (UGB) is kept much larger than the converter loop bandwidth of 5 KHz to avoid any additional poles in the converter loop transfer function [21]. The OPAMP architecture is shown in Fig. 5.3. Figure 5.4 shows the performance parameters like UGB, Gain, phase and gain margin with process and temperature variation at the subtractor output of 100 mV.

5.3 PWM Comparator

The PWM comparator serves to generate the required buck and the boost duty cycles, D1 and D2, respectively, by comparing the buck and the boost control signals, V_{buck} and V_{boost} with a ramp signal of amplitude V_r (see Fig. 4.1). Two important requirements for a PWM comparator operating with a 2 MHz ramp signal

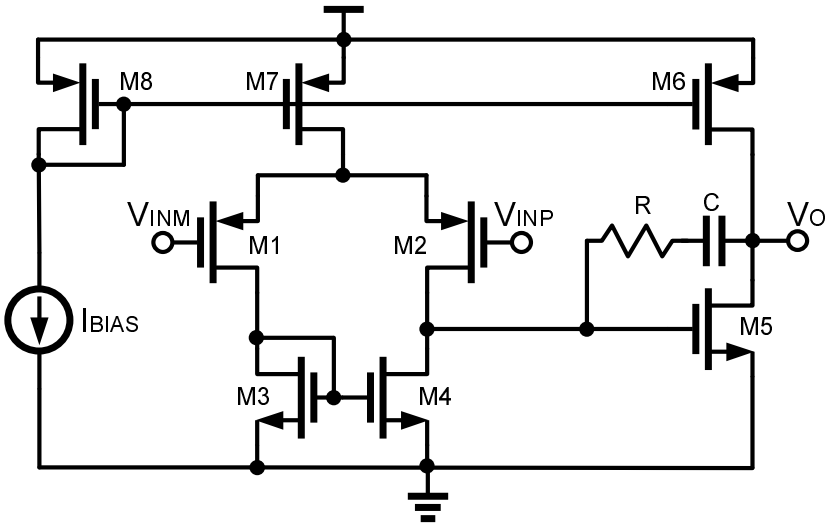
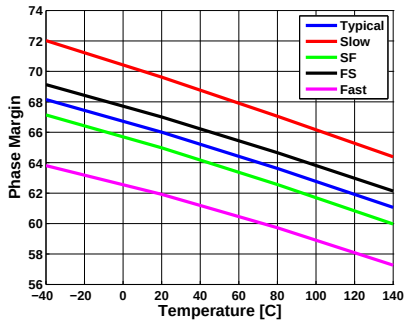
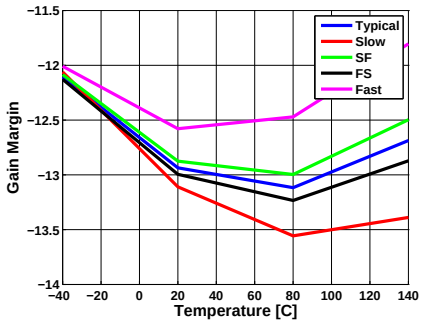


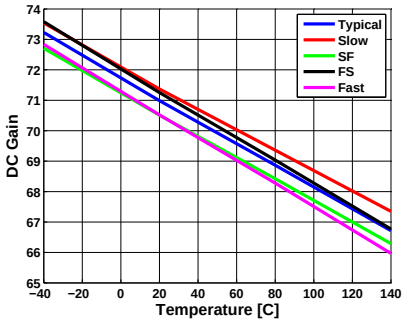
Figure 5.3: OPAMP for subtractor.



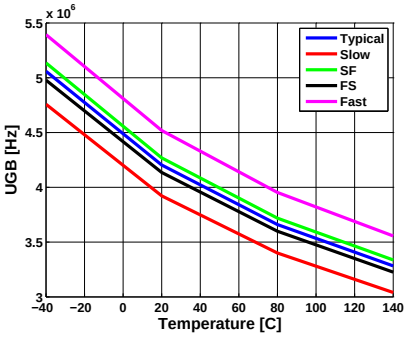
(a) Phase Margin



(b) Gain Margin



(c) DC Gain



(d) Unity Gain Bandwidth

Figure 5.4: Subtractor (a) Phase margin (b) Gain margin (c) DC gain (d) Unity Gain Bandwidth Vs Temperature.

are high resolution and low propagation delay. High resolution of the comparator improves the control signal (V_{buck} and V_{boost}) to duty cycle (D1 and D2) conversion accuracy by changing the comparator output state with a small difference between the comparator inputs. The low propagation delay helps to synchronize the PWM comparator output with a 2 MHz reference clock. This is important as in the prototype implementation the duty cycle as well as the controller signals are generated at the rising edge of the reference clock. In order to achieve high resolution and low propagation delay, multiple high bandwidth stages are used. A three stage PWM comparator is designed. As the first stage signal swing is low, the important parameter is to have high bandwidth so that there is little delay in amplifying the signal to a sufficient value and passing it to the next stage. For the next two stages, it is important to have a high slew rate capability so that the voltage across the interstage capacitors rises and falls quickly. Thus, multiple stages combined together provide high gain for good resolution while reducing propagation delay [22][23]. The three stage architecture of the PWM comparator is shown in Fig. 5.5. PMOS inputs are chosen since the input to the comparator is always less than 1V. Additionally, the two inverters act as buffers and square up the PWM signal which is sent to the dead-time circuit.

5.4 Dead-time circuit

The PMOS and NMOS power FET turn on signals should be non-overlapping to prevent heavy shoot through current. The shoot through current reduces the overall efficiency of the converter and can be prevented by using a dead-time circuit. A fixed dead-time circuit shown in Fig. 5.6 is utilized to generate non-overlapping signals for the power FETs. Here the inverters are used as delay blocks to ensure

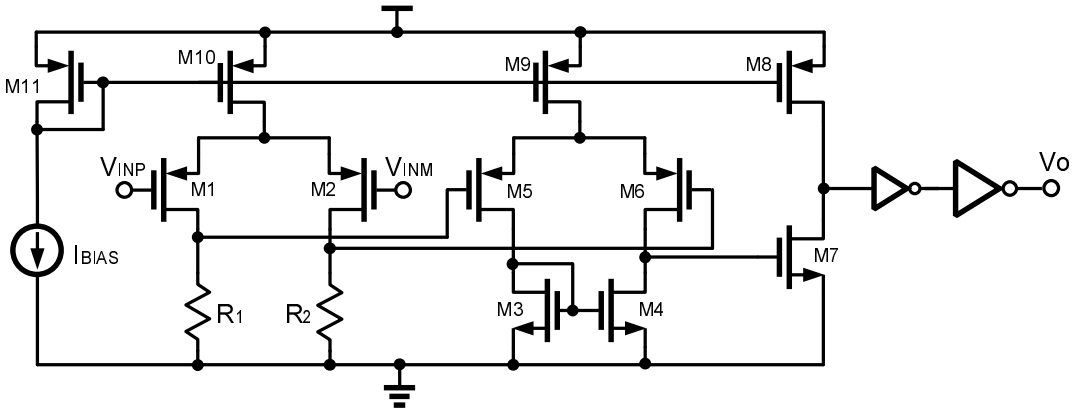


Figure 5.5: PWM comparator Architecture.

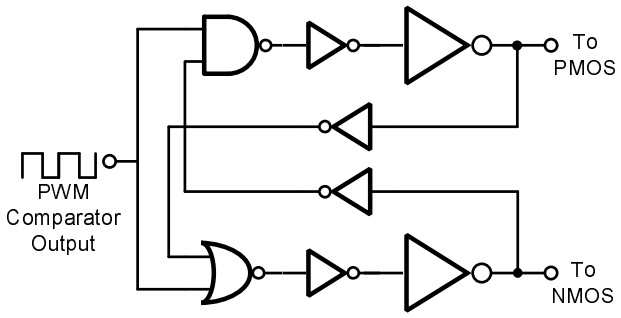


Figure 5.6: Dead-time Circuit.

that the clocks remain non-overlapping. The same inverter chain is used as a driver for the power FETs. Figure 5.7 shows the achieved dead-time across corners using cadence simulations.

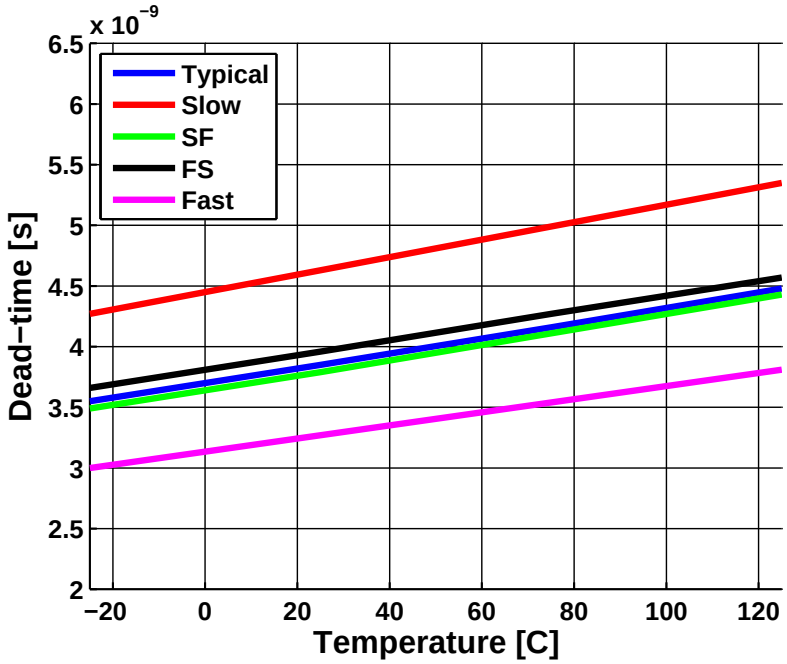


Figure 5.7: Simulated dead-time across corners.

CHAPTER 6. EXPERIMENTAL RESULTS

A prototype Buck-and-Boost converter with the proposed control scheme was fabricated in a 0.5μm CMOS process. Driving an LED with a forward voltage of about 3.1V and a current of up-to 1.2A, the converter operates at a frequency of 2MHz with an off-chip 1μH inductor and a 10μF capacitor. The chip micrograph is shown in Fig. 6.1 and occupies about 5mm^2 of die area. The die was packaged in a 20 bump -SMD package offering low package inductance and resistance. Low package inductance are highly desirable considering the need of heavy switching currents to provide LED forwards current of up-to 1.2A. In order to further reduce the effective inductance on high switching current carrying lines like, ground, input supply and output, were each provided with two internally shorted bumps. The packaged chip was mounted on a four layer test board for testing the performance of the prototype.

6.1 Measurement Results

With just boost converter as an LED driver, due to extra headroom across the output current source the LED efficiency decreases as the input voltage increases beyond the LED forward voltage. Given this, to show the effectiveness of the Buck-and-Boost LED driver the efficiency of the prototype converter was measured for two LED current of 0.6A and 1.2A. The efficiency is calculated as the ratio of output power to input power. Input and output power was determined by measuring the current and voltage at each end using high accuracy multi-meters.

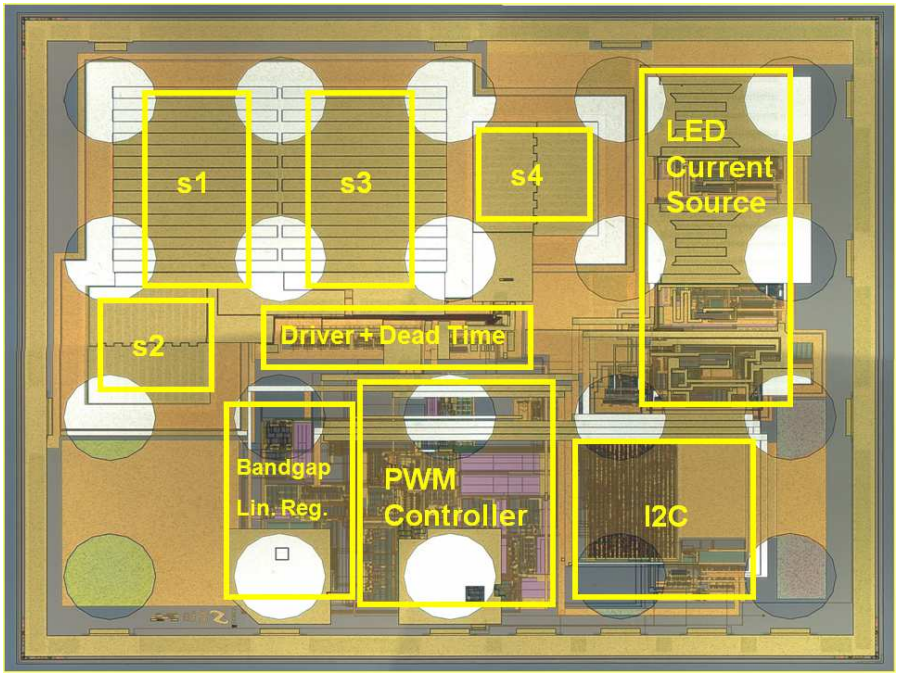


Figure 6.1: Buck-and-Boost chip micrograph.

Figure 6.2 shows the measured efficiency of the converter for LED currents of 0.6A and 1.2A. The converter keeps high efficiency over the entire Li-On battery range of 3.0V to 5.2V and shows peak efficiencies of 87% and 83% for LED current of 0.6A and 1.2A, respectively.

The converter presents high efficiency in the middle range of the battery voltage by operating in Buck-and-Boost mode. To keep the efficiency high in Buck-and-Boost mode the controller should keep the buck duty cycle, D1, large and the boost duty cycle, D2, as small as possible. To verify the proper functioning of the controller, buck duty cycle, D1, and boost duty cycle, D2, were measured over the input voltage range of 3.0V to 5.2V. Figure 6.3 shows the measured Buck and Boost duty cycle variation as the input voltage ramps down from 5.2V to 3.0V. As expected, during the Buck-and- Boost mode, first the Buck duty cycle

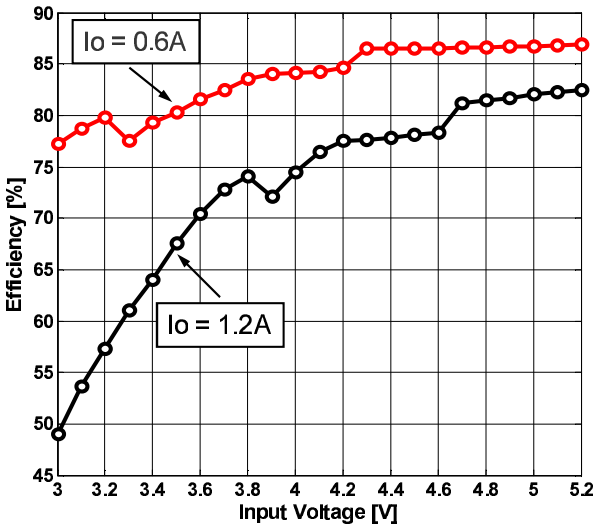


Figure 6.2: Measured efficiency versus input voltage for load currents of 0.6A and 1.2A.

increases to its maximum value of around 90% before the control shifts causing the Boost duty cycle to increase from its minimum value of 10%.

To verify the continuity of the controller operation over the entire Li-On battery range, LED voltage was monitored with the input voltage ramping down from 5.2V to 3.0V. Figure 6.4 indicates that the converter operates over the range of 3.0 to 5.2V. While the converter makes a smooth transition from Buck-and-Boost to Boost mode, it toggles between the modes during the Buck to Buck-and-Boost mode transition. This is caused due to the excess feed forward voltage in this prototype. Nevertheless, the LED voltage shows only a small peak-to-peak ripple of 12 mV and the LED current is constant resulting in uniform illumination.

Thus, comparing with other LED drivers till date, the LED driving technique developed in this research makes it the first to offer high efficiency and continuous operation over the entire Li-On battery range.

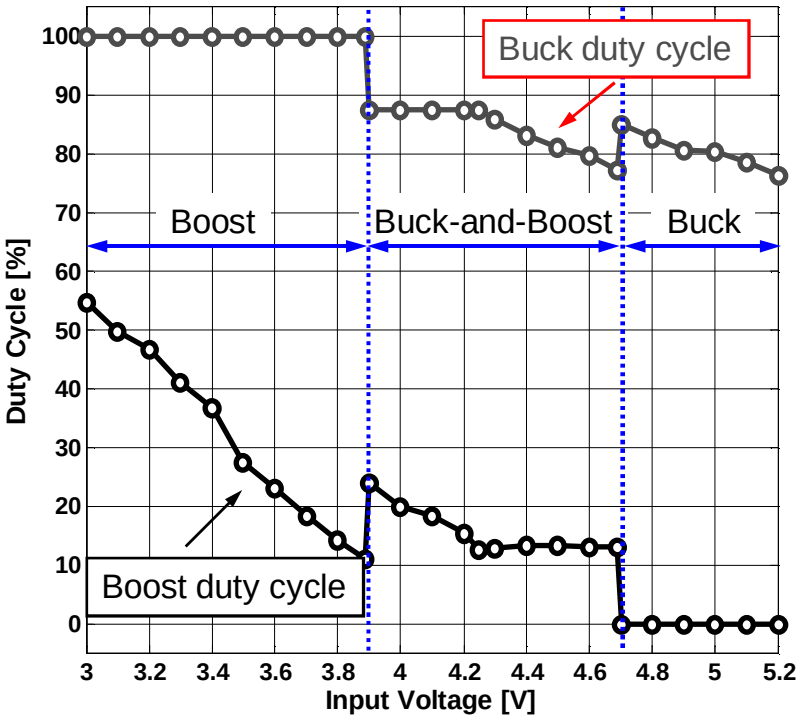


Figure 6.3: Measured Buck and Boost duty cycles over the entire input range.

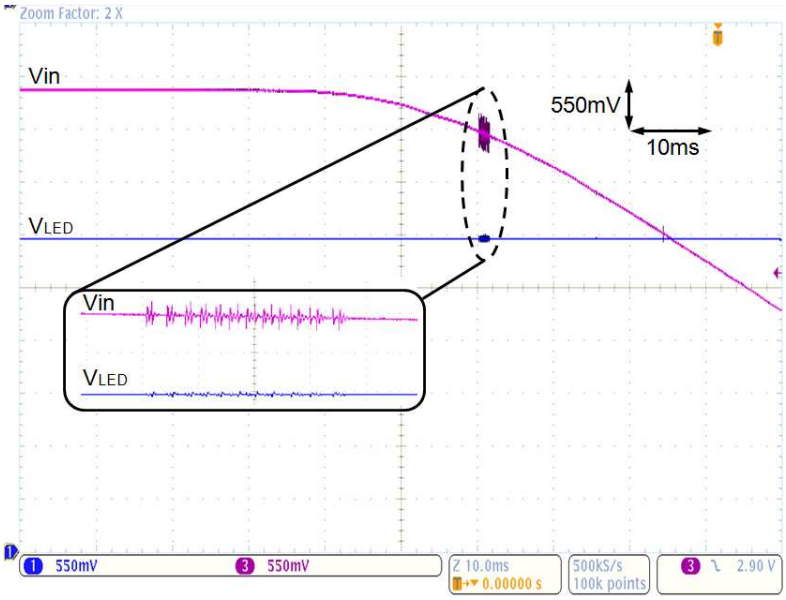


Figure 6.4: Measured LED voltage versus input voltage. Small mode-switching ripple induced by excess feed-forward in illustrated in the inset.

CHAPTER 7. CONCLUSION

A new power management scheme for camera flash, the Buck-and-Boost driving scheme is developed to provide high efficiency over the Li-On battery range. The architecture optimizes the efficiency by keeping the average inductor current as low as possible. The low average inductor current is obtained by operating the LED driver in three different modes, namely, Buck, Buck-and-Boost and Boost. A new PWM controller is developed to regulate the output LED current with the supply, temperature, process and LED forward voltage variation. The Buck-and-Boost converter with the proposed control scheme is implemented in a 0.5μm CMOS process and the chips performance is measured to verify the functionality of the converter. The converter operates at 2MHz and drives up-to 1.2A of LED current with a off-chip 1μH inductor and a 10μF capacitor. The PWM controller achieves continuous operation over the entire Li-On battery range and provides constant LED current. The converter achieves peak efficiency of 87% and 83% for LED current of 0.6A and 1.2A, respectively.

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