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CHENG-WEN LAI (Name) for the MASTER OF SCIENCE (Degree)

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G. C. Alexander

The power dissipation of microstrip transmission-line on gold-doped silicon substrates was investigated. The gold-doping was applied to a regular n-type silicon substrate with resistivity of 5 to 10 ohm-cm. Insertion-loss tests were employed to measure the power dissipation of the microstrips. Power dissipation somewhat less than that for intrinsic silicon with resistivities in the order of 1000 ohm-cm were obtained. For application, band-pass filters, of the parallel-coupled microstrip-line type were also built on silicon substrates and tested. The performance of the filters showed that a great deal of care should be taken in the design and fabricating process if a good result is to be obtained.

Microstrips on Gold-Doped Silicon Substrates

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Cheng-Wen Lai

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Associate Professor of Electrical and Electronics Engineering

in charge of major

Redacted for Privacy

Head of Department of Electrical and Electronics Engineering

Redacted for Privacy

Dean of Graduate School

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Typed by Clover Redfern for Cheng-Wen Lai

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

MICROSTRIPS ON GOLD-DOPED SILICON SUBSTRATES

I. INTRODUCTION

With the rapid development of transistors and other semiconductor devices in the microwave frequency regions, the microstrip line structure, in which a flat conductor is desposited atop a dielectric and ground plane, is finding increasing use in microwave integrated circuits.

The basic microstrip structure can be represented as shown in Figure 1. The conductor (W = width, T = thickness) is on one side of a dielectric substrate (H = substrate thickness) with a ground plane on the opposite side.

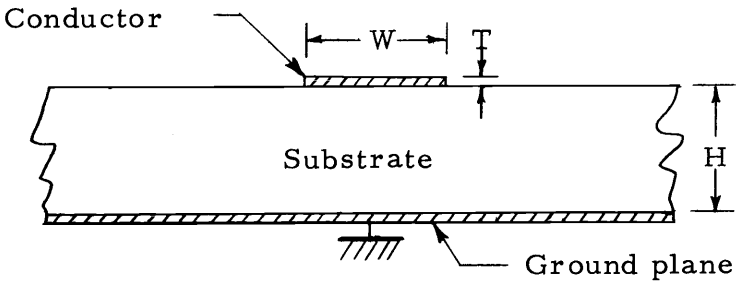


Figure 1. Microstrip structure.

By using the transmission line approach, many studies have been done previously (8, 9, 37, 38, 39, 41, 42) for the microstrip structure. In a lossless transmission line with homogeneous dielectric

characteristic impedance can be calculated by the equation:

$$Z_c = \frac{1}{vC_o} \qquad \text{with} \qquad v = \frac{c}{\sqrt{\epsilon_r}} \; ;$$

where

Z_c = characteristic impedance,

C_o = capacitance of the transmission line per unit length,

v = the velocity of wave propagation down the line,

c = light speed in free space,

ϵ_r = dielectric constant of the surrounding material.

However, the surrounding material is not uniform for a microstrip and the velocity of wave propagation is slightly modified by using an effective dielectric constant of the substrate material, ϵ_e, instead of ϵ_r in the formula for a transmission line. The relationship between the microstrip wavelength λ_m, which is derived from the phase velocity, and the free space wavelength λ_o for substrates with different dielectric constants can be found in several papers (22, 34, 42).

There are many conventional microwave circuits, such as switches, couplers, circulators, filters, mixers, oscillators, etc. which can be microminiaturized by using the microstrip concept. A hybrid microwave integrated circuit is usually constructed on a dielectric substrate with deposited microstrip lines and certain ready made, discrete microwave components. In a monolithic microwave

integrated circuit, a semiconductor material such as silicon or gallium arsenide is employed as the dielectric substrate for the purpose of fabricating active devices (e.g., diodes, transistors, etc.) and/or passive elements (resistors, capacitors, etc.) directly on it together with the microstrip lines.

In order to avoid large power dissipation, a high resistivity substrate must be used in microstrip circuits. Because of its high resistivity, intrinsic silicon has been extensively employed as the substrate material for monolithic, microwave integrated circuits. Normally, the resistivity of the intrinsic silicon employed is in the order of 1000 ohm-cm (16, 23). Because intrinsic silicon is unstable, the long periods of high temperature processing required for active element formation always degrades the resistivity. Several ohm-cm may result; even though the initial resistivity was high (3). Therefore, special care must be taken with high resistivity silicon, if a long time is needed to fabricate some solid-state devices on it.

Many properties of gold diffusion in silicon have been studied by several scientists (2, 4, 6, 33, 40). One of the most significant results of such diffusion is that the resistivity of the silicon can be raised to as high as 10^5 ohm-cm after gold doping. Therefore, it is possible to obtain a low-loss silicon substrate for monolithic microwave integrated circuitry simply by applying gold-doping. This gives the great advantage that intrinsic silicon is not always necessary as a starting

substrate for the fabrication of some integrated circuits. Most n- or p-type, low resistivity silicon substrates (1 ohm-cm to 10 ohm-cm) can be employed as a starting material; and an extremely high resistivity can be obtained after the gold doping, providing that the diffusing temperature is high enough and the concentration of the active gold molecules at that temperature is greater than the impurity concentration in the silicon.

The objectives of this study were to investigate the power dissipation of microstrip lines on gold-doped silicon substrates and to check the feasibility of application of microwave integrated circuits on such a silicon substrate. A parallel-coupled bandpass filter was constructed and tested.

II. SUMMARY OF MATERIAL CHARACTERISTICS PRESENTLY AVAILABLE FOR MICROSTRIPS

Substrate Materials

The ideal substrate materials for microwave integrated circuits should have the following characteristics (29):

1) high dielectric constant,
2) low dissipation factor or loss tangent,
3) dielectric constant should remain constant over the frequency range of interest and over the temperature range of interest,
4) high purity and constant thickness,
5) high surface smoothness,
6) high resistivity and dielectric strength,
7) high thermal conductivity.

If a monolithic, integrated circuit is desired, a semiconductor material should be employed as the substrate. Silicon and gallium arsenide are the mostly used materials for this purpose. The dielectric constants for many broadly used substrate materials are listed in Table 1. Note that silicon and gallium arsenide provide the highest dielectric constants among the listed substrate materials.

Since the resistivity of a semiconductor depends largely on its impurity concentration, we can control the resistivity by controlling the concentration of the impurity. Figure 2 shows the resistivity of

both p- and n-type silicon at room temperature as a function of acceptor or donor concentration, respectively (24).

Table 1. Dielectric constants and dissipation factors of substrate materials as listed in the technical literature.

Substrate Material	Dielectric Constant at 25°C	Dissipation Factor at 25°C
96% Alumina	8.9	0.0006
99% Alumina	9.0	0.0001
99.5% Alumina	9.5	0.0002
99.9% Alumina	9.9	0.000025
99% Beryllia	6.1	0.0001
99.5% Beryllia	6.1	0.0001
Quartz	3.78	0.0015
Borosilicate glass	5.74	0.0036
Sapphire	11.0	0.0002
Silicon	11.7	--
Gallium arsenide	13.3	--

The variation of resistivity with temperature for lightly doped p-type silicon which was computed by Runyan (32, p. 168) is given in Figure 3. As shown in Figure 3, the impurity concentration should be lower than 10^{13} per cubic centimeter in order to obtain a resistivity higher than 1000 ohm-cm.

High resistivity, p-type silicon undergoes resistivity changes and type conversion during high temperature processing. In Figure 4, we note that the resistivity increases during early phases of the thermal cycle; while further heat exposure results in conversion to n-type with an ultimate resistivity of 1 to 10 ohm-cm. Hence a

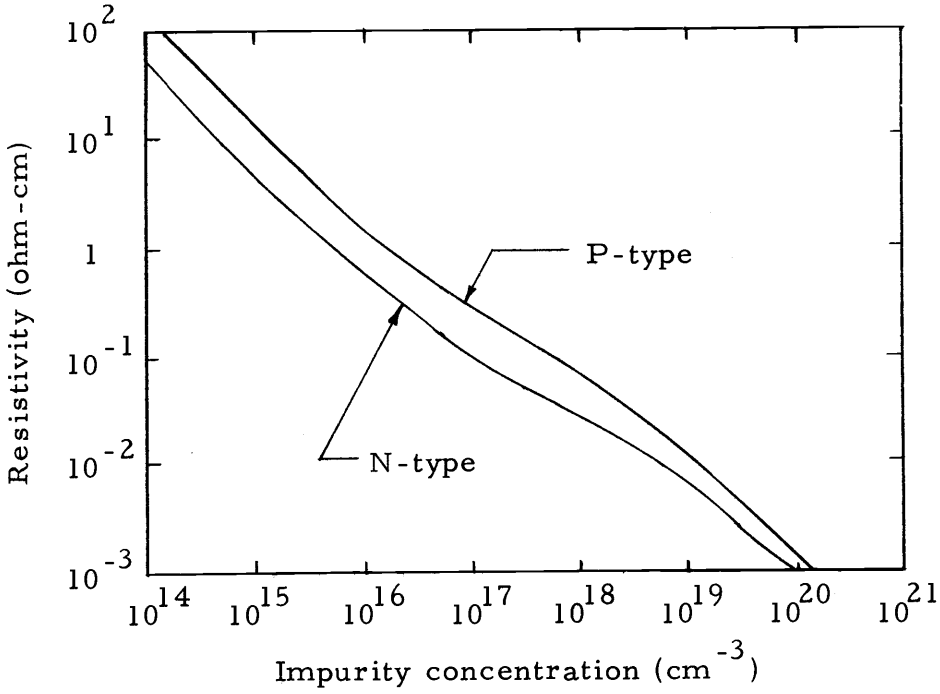


Figure 2. Resistivity of silicon at 27°C as a function of acceptor or donor concentration (24).

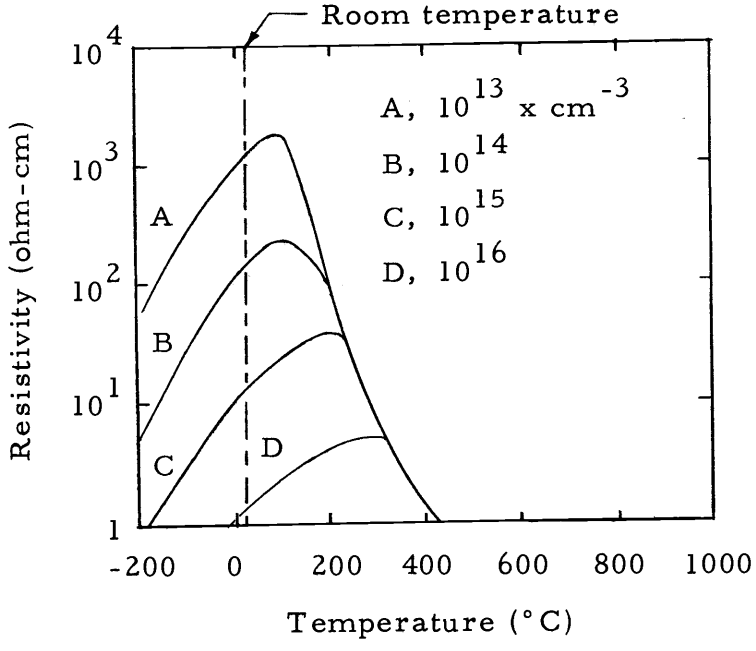


Figure 3. Resistivity versus temperature for boron-doped silicon (32, p. 168).

long-period, high-temperature processing should be carefully handled in order to avoid this undesirable effect.

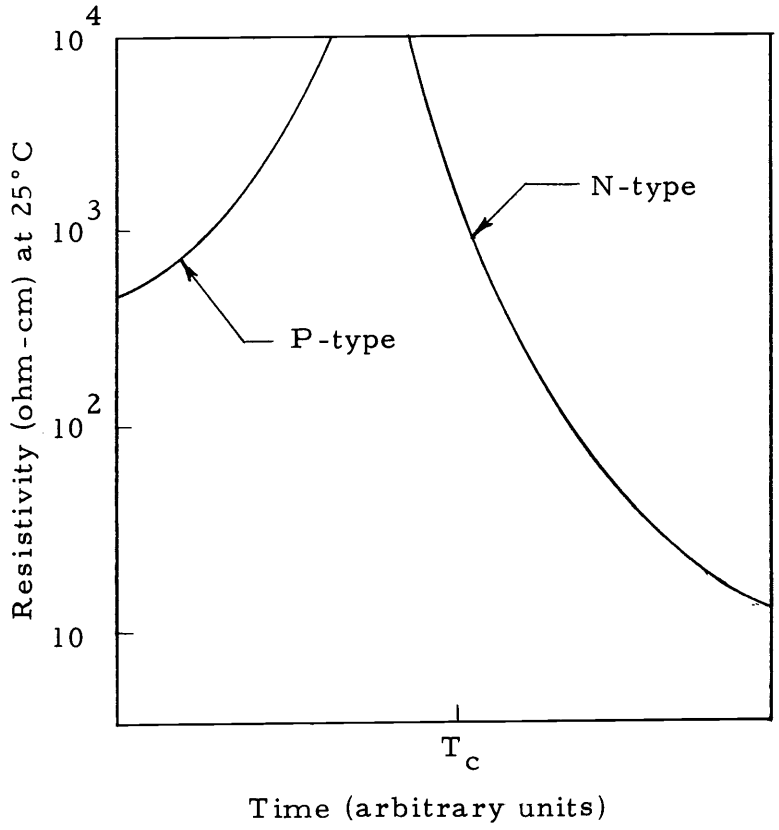


Figure 4. Behavior of high-resistivity silicon during high temperature processing. T_c is approximately six hours at 1100°C in O_2 ambient (3).

Conductor Materials

The ideal conductor materials for microwave integrated circuits should have the following characteristics:

1) high conductivity,

2) low temperature coefficient of resistance,

3) good adhesion to the substrate,

4) good etchability,

5) easily deposited or electroplated.

Some materials which have excellent conductivity and can also be deposited by a number of methods are listed in Table 2. They usually are used to form both the conductor pattern and the bottom ground plane.

Table 2. Properties of excellent conductors.

Conductor Material	Resistivity at 20°C	One Skin-Depth at 10 GHz
Silver	1.59×10^{-6} ohm-cm	6.2×10^{3} Å
Copper	1.72	6.7
Gold	2.44	8.1
Aluminum	2.65	8.6

III. RESULTS OF GOLD DIFFUSION INTO SILICON

Position of the Gold Energy Levels

Gold can be introduced into silicon by diffusion or as an impurity during growth from the melt. The maximum solubility of gold in silicon is about 10^{17} atoms/cm^3. The solubility appears to be affected by other impurities present in silicon. Because gold diffuses by an interstitial-substitutional mechanism, gold diffusion is strongly influenced both by crystal perfection and by the presence of other impurities (6).

Collins, Carlson, and Gallagher (13) have made a detailed study of the electrical properties of gold in silicon. They found two levels, a donor level 0.35 eV above the valence band edge and an acceptor level 0.54 eV below the conduction band edge. Figure 5, replotted from Bullis' paper (6), shows the levels for different doping conditions. At low temperatures, the levels are many kT apart and they may be treated independently of each other. In other words, we may apply an approximation by considering only the acceptor level in n-type, and the donor level in p-type silicon.

Resistivity

As the gold concentration in a silicon sample is increased sufficiently to become comparable to the concentration of the donor or

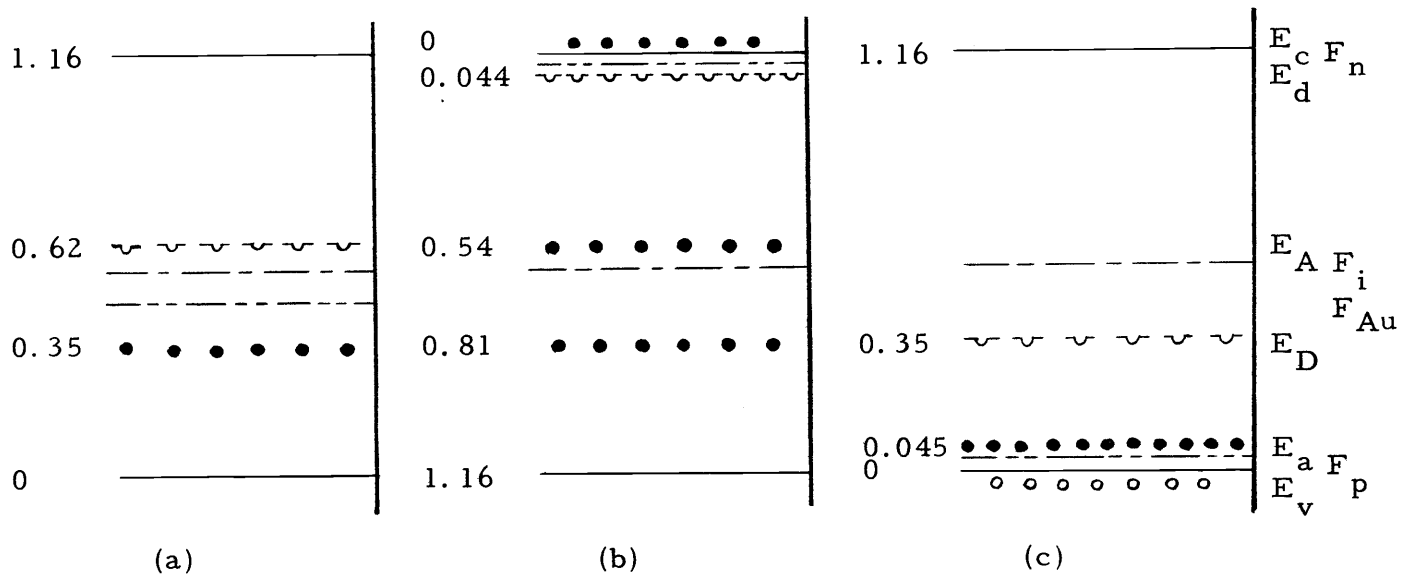


Figure 5. Energy band diagram for silicon doped with gold. (a) No other impurity present, (b) shallow donor present, (c) shallow acceptor present. In cases (b) and (c) it is assumed that the shallow impurity concentration is much greater than the gold concentration. Note that in case (c) the acceptor level does not exist since the donor levels are empty (6).

acceptor impurity, each of the deep lying energy levels associated with the gold atoms will, in effect, remove one majority carrier from the conduction-band in the case of an n-type semiconductor, or from the valence band in the case of a p-type semiconductor. Thus, for example, in an n-type silicon the electron concentration will become $n = N_D - N_{Au}$. As a result, the resistivity of the sample will increase with the addition of gold. A similar phenomenon takes place in the case of p-type silicon. However, this simple description loses its validity once the concentration of deep-lying levels approaches or exceeds the donor or acceptor concentration. In these cases the calculation of the resistivity of silicon as a function of gold concentration becomes more complicated.

The relationships between resistivity and gold concentration for both n- and p-type silicon are given in Runyan's book (32, p. 171-172); and are also shown in Figures 6 and 7, respectively. The trend of resistivity for both n- and p-type silicon is apparent from these curves. In the case of n-type silicon, the resistivity increases sharply when the gold concentration becomes comparable with the shallow donor concentration. As the gold concentration is further increased, the resistivity becomes that typical of intrinsic silicon. With a further increase in gold concentration, the resistivity reaches a maximum and the material becomes distinctly p-type. When gold becomes the dominant impurity, the position of the Fermi level is

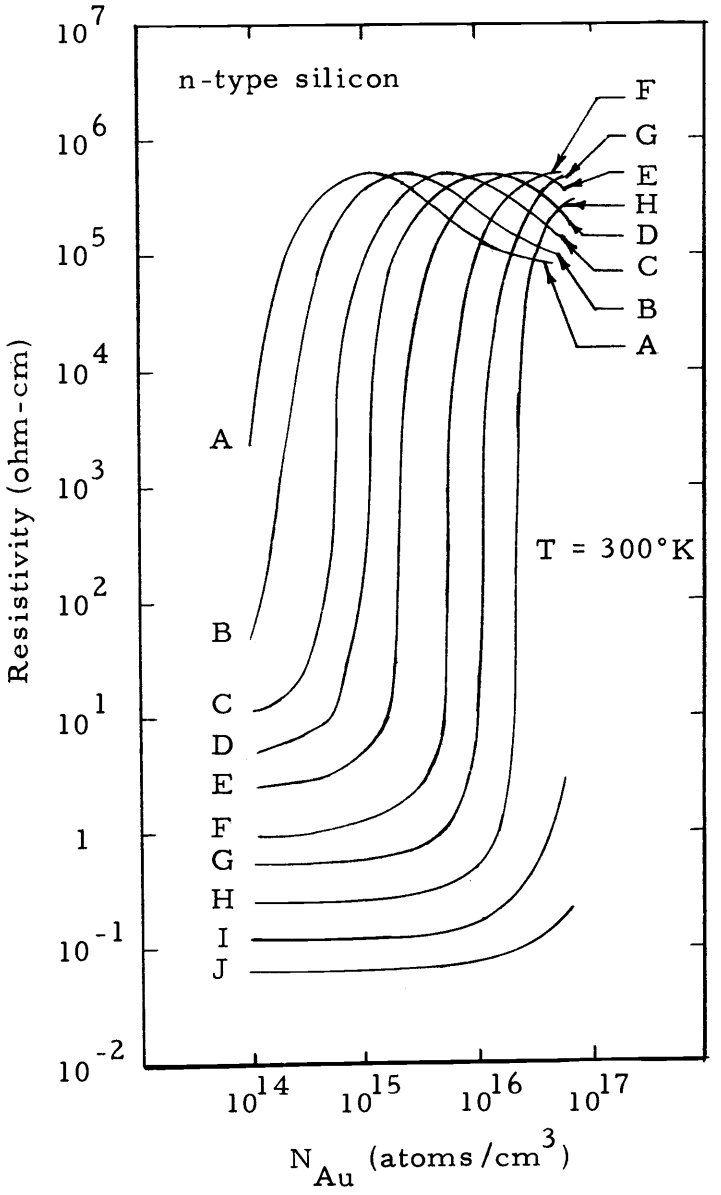


Figure 6. Calculated values of resistivity versus gold concentration in phosphorus-doped silicon at T = 300°K. Primary phosphorus concentrations (cm^{-3}) assumed are: A, 1×10^{14}; B, 2×10^{14}; C, 5×10^{14}; D, 1×10^{15}; E, 2×10^{15}; F, 5×10^{15}; G, 1×10^{16}; H, 2×10^{16}; I, 5×10^{16}; J, 1×10^{17}. At the bar on each curve, $n = p = n_i$. To the right of this bar, $p > n$ (32, p. 171).

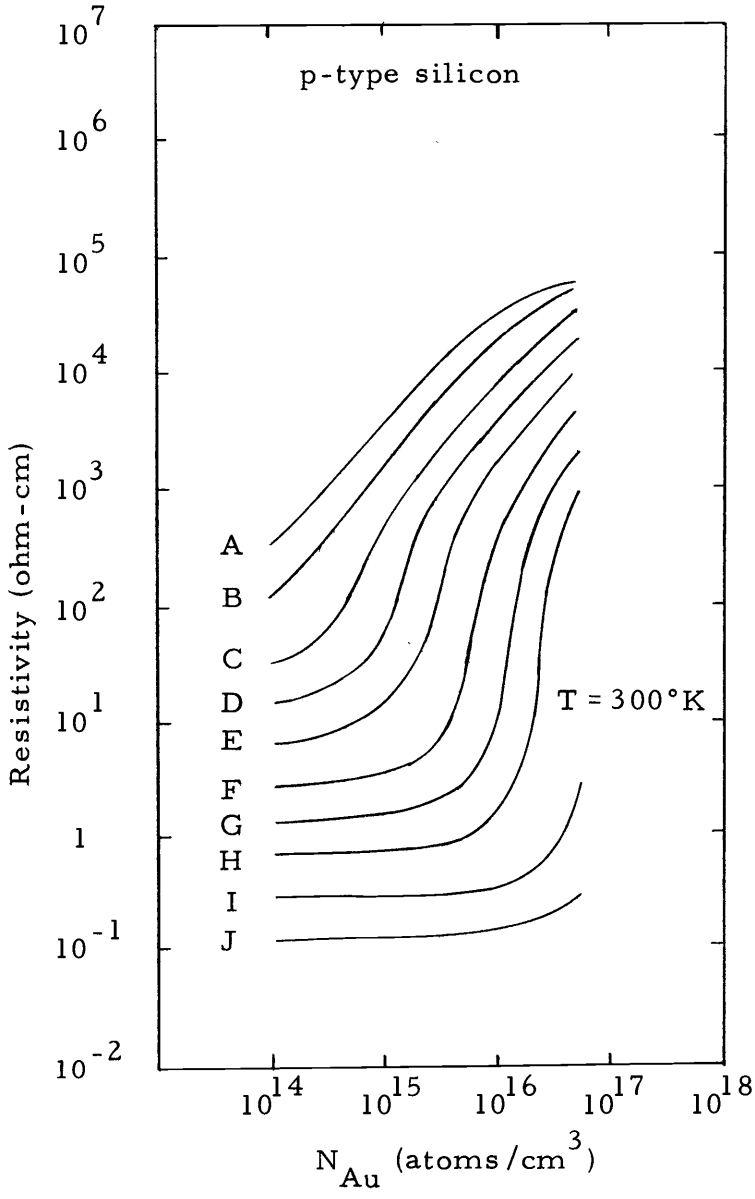


Figure 7. Resistivity versus gold concentration in boron-doped silicon at T = 300°K. Primary boron concentrations (cm^{-3}) assumed are: A, 1×10^{14}; B, 2×10^{14}; C, 5×10^{14}; D, 1×10^{15}; E, 2×10^{15}; F, 5×10^{15}; G, 1×10^{16}; H, 2×10^{16}; I, 5×10^{16}; J, 1×10^{17} (32, p. 172).

determined principally by the relative occupancy of the gold levels, and the resistivity reaches a limiting value. In the case of p-type silicon, the resistivity also begins to increase as the gold concentration approaches the shallow acceptor concentration. However, in this case the increase is monotonic and reaches the limiting value when the gold concentration significantly exceeds the shallow acceptor concentration.

Since neither the positions of the gold energy levels nor the degeneracy factors associated with them are known exactly and the calculated value for the limiting resistivity depends strongly on both, there still exists a certain degree of uncertainty in the curves.

Solubility and Diffusion Coefficient

Since the maximum available active gold concentration in silicon depends on its solubility at different temperatures, the solubility is therefore very important to the control of diffusion of gold in silicon. The solubility of gold in silicon, both for substitutional and interstitial cases, is shown in Figure 8. The substitutional solubility was calculated by R. C. Wackwitz as cited by Bullis (6); while the interstitial solubility was calculated by Wilcos and LaChapelle (40).

Because the interstitial solubility is so much lower than the substitutional solubility, Wilcox and LaChapelle (40) have suggested that the substitutional solubility is very nearly equal to the total gold

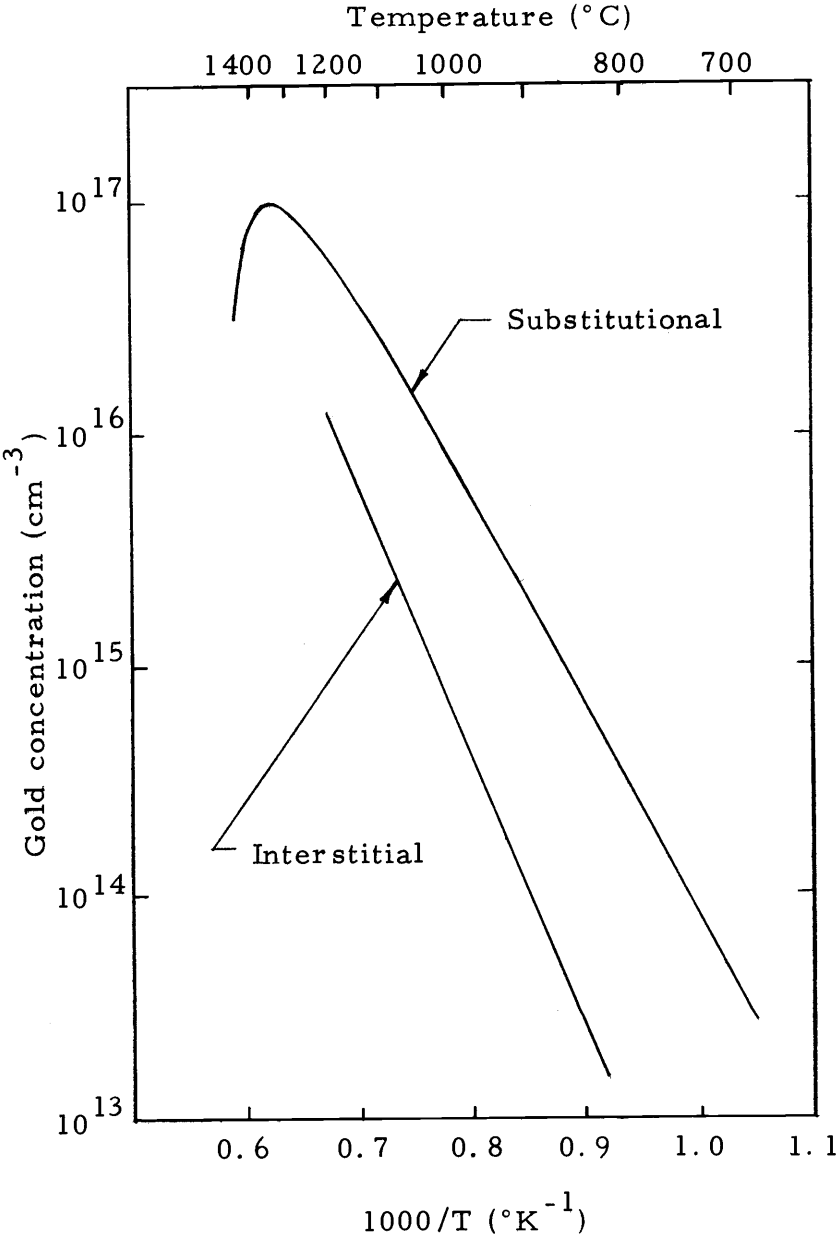


Figure 8. Solubility of gold in silicon. The substitutional curve is calculated by Wackwitz (6). The interstitial curve is calculated by Wilcox and LaChapelle (40).

solubility. They have also made calculations for the diffusion coefficients of gold by assuming these diffusion coefficients are varying according to the Arrhenius law, which provides a plot of straight line for log D versus 1/T. The equations of these lines in cm^2/sec are as follows:

$$\text{Curve I} \quad D_{IC} = 1.78 \times 10^{-2} \exp(-\frac{1.118}{kT}) \tag{3-1}$$

$$\text{Curve II} \quad D_{VC} = 1.15 \times 10^{3} \exp(-\frac{3.087}{kT}) \tag{3-2}$$

$$\text{Curve III} \quad D_{S} = 2.75 \times 10^{-3} \exp(-\frac{2.04}{kT}) \tag{3-3}$$

$$\text{Curve IV} \quad D_{I} = 2.44 \times 10^{-4} \exp(-\frac{0.387}{kT}). \tag{3-4}$$

These lines are shown in Figure 9, and represent the coefficients of (I) interstitital controlled dissociative diffusion, (II) vacancy controlled dissociative diffusion, (III) substitutional diffusion and (IV) interstitial diffusion respectively.

Diffusion Time and Penetration Depth

Sprokel and Fairfield (36) have found that the gold concentration throughout the silicon slice is nearly independent of position. As the diffusion time is increased, the gold concentration in the slice gradually increases as shown in Figure 10. Note that the experimental values have the tendency to approach the solubility of gold after an

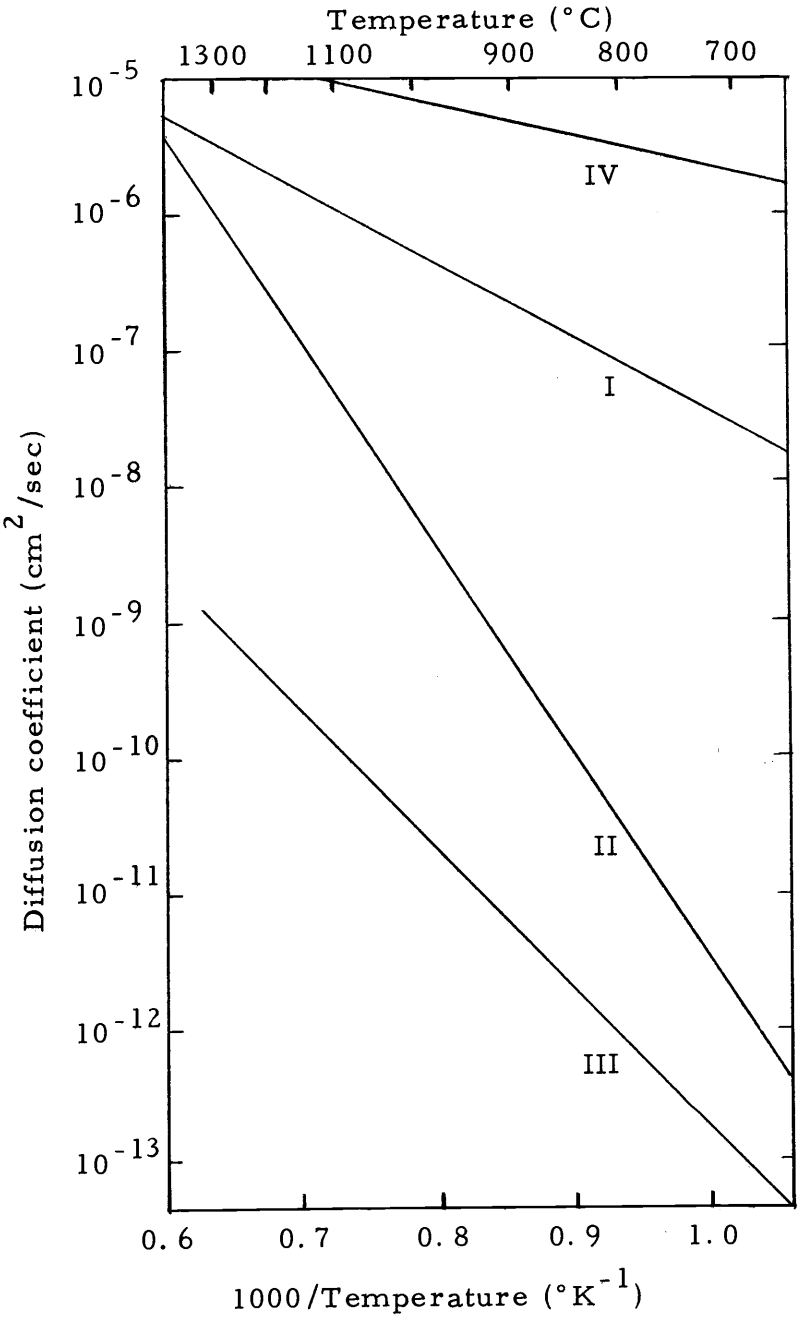


Figure 9. Diffusion coefficients calculated from experimental diffusion concentration profiles as a function of inverse temperature (Arrhenius plots). Curve I: interstitial controlled dissociative diffusion; Curve II: vacancy controlled dissociative diffusion; Curve III: substitutional diffusion; Curve IV: interstitial diffusion (40).

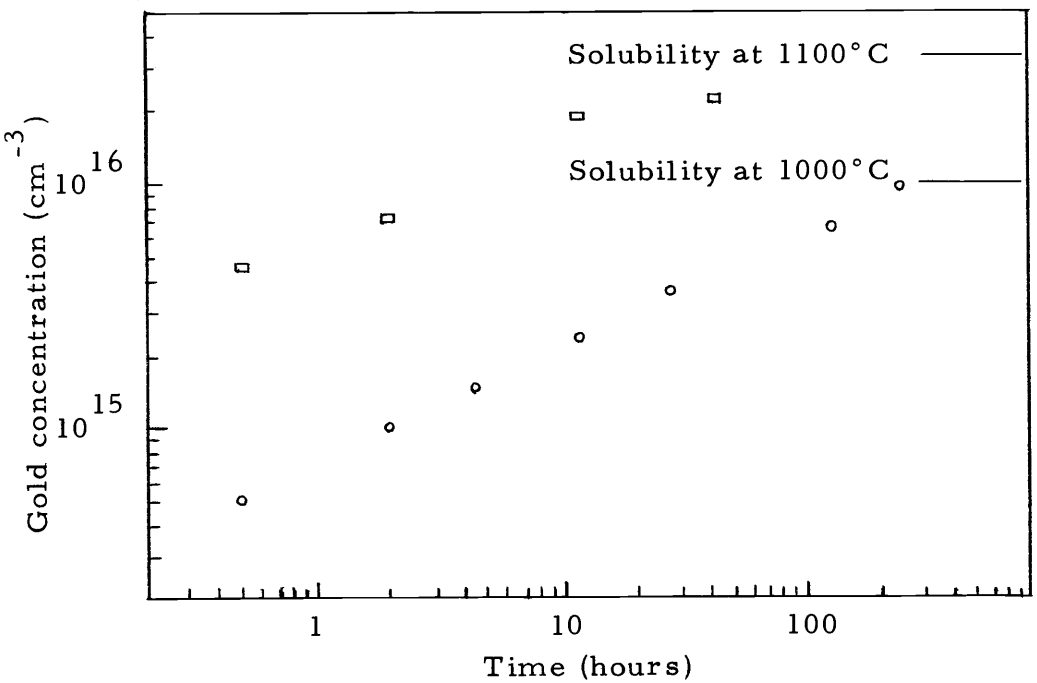


Figure 10. Gold concentration in the uniform concentration region versus time for diffusion into relatively thin, low dislocation, high resistivity p-type slices. Data are from Sprokel and Fairfield (36).

extremely long-time diffusion.

In diffusing gold into device structures, it is usually desired that the gold concentration be nearly uniform throughout the wafer thickness. In the simple case where it can be assumed (a) that the diffusion profile is a complementary error function, (b) that the density of shallow impurities is so low the solubility enhancement can be neglected, (c) that the gold is deposited on one side of the slice and (d) that no gold diffuses across the back surface, the time required to diffuse a slice of thickness H so that the concentration at the back surface is b times the concentration C_S at the front surface is given by Fabricus (17).

$$t = \frac{4H^2}{\pi^2 D} \ln\left[\frac{4}{\pi(1-b)}\right] \tag{3-5}$$

when $\pi^2 Dt/4H^2 > 0.5$, and D is the diffusion coefficient of gold in silicon.

If the silicon slices have a large density of dislocations, the diffusion coefficient in the above equation is appropriately found by using the following formula (6):

$$D = \frac{C_I'}{C_S'} D_I ; \tag{3-6}$$

where D_I is the coefficient of interstitial diffusion obtained by Wilcox and LaChapelle's equation, C_I' and C_S' are the solubility

of interstitial and substitutional diffusion, respectively. However, if the dislocation density is relatively low, considerably longer diffusion times are required to approach the solubility limit; because the gold concentration also depends on the vacancy generation rate. The profile shown in Figure 10 was of this type diffusion, and the diffusion-time equation (3-5) is not appropriate now.

Cooling After High Temperature Diffusion

There is another very important factor which will affect the gold concentration in silicon. The concentration of electrically active gold in silicon is affected greatly by the manner in which the silicon slices are cooled to room temperature. The concentration ranges from a maximum value by quenching, to a minimum value by slow cooling (1, p. 11).

Permittivity

Effort has been made to find the effect of gold-doping on the permittivity in silicon. Unfortunately, no information related to this topic was found. Therefore, the silicon substrate will be assumed to suffer no change in the permittivity value under gold-doping.

IV. MICROSTRIP FABRICATION AND GOLD-DOPING AS USED FOR TEST

Many processes were required to complete microstrip test-patterns on a gold-doped silicon substrate when starting with a regular silicon wafer. In this chapter, a test-pattern was assumed available for application. Materials, facilities and special techniques required for each step in the process will be introduced first, then follows the description of all steps in sequence for the entire process.

Silicon Substrate Preparation

In order to make the final resistivity of the silicon substrate after gold diffusion as high as can possibly be obtained, the temperature and diffusion time for gold diffusion must be appropriately selected. By using the equations given in the previous chapter, the approximate temperature and diffusion time for gold diffusion can be calculated; providing that the primary impurity concentration and thickness of the silicon substrate are known.

All silicon wafers employed in the experiment were n-type, one and one quarter inch in diameter and with an average value of 0.0082 inch in thickness. The resistivities measured using a 4-point probe (20, p. 58) ranged from three to eight ohm-cm which gave an approximate impurity concentration of 2×10^{15} to 5×10^{14} cm^{-3}, respectively. Calculations with the equations (3-4) to (3-6) showed that a diffusion

time of about 15 minutes at 1100°C was long enough to obtain the maximum available resistivity with gold diffusion.

Silicon-Dioxide and Aluminum Etching

Since the silicon substrate was proposed to be passivated with silicon-dioxide on its top surface to simulate the case for fabrication of some solid-state devices, silicon-dioxide etching was as necessary as aluminum etching. The solution used to etch the silicon-dioxide from the silicon wafer was 4:1 buffered HF, which was made by adding HF to buffering NH_4F solution in the volume of 1:4. Eight parts by weight of NH_4F to 15 parts by weight of deionized water was the buffering NH_4F solution. The etching speed in the 4:1 buffered HF solution is about 1000 Å per minute.

The solution usually employed for aluminum etching is made by mixing 80 parts of H_3PO_4 (concentration 85%) to 16 parts of deionized water to five parts of HNO_3 (concentration 70%). Normally, a 10,000 Å thick aluminum layer can be etched off completely with this solution in about two minutes, if the temperature of the solution is 70°C.

Aluminum and Gold Deposition

Both the aluminum and gold depositions were made in a Micros Automatic-Valving Vacuum Evaporator. The main components of this

evaporator are vacuum glass jar, filament for heating evaporating materials, wafer holder, vacuum pumping system, and control units. When the air pressure in the vacuum jar is pumped down to 0.1 micron, electric current may be applied to the filament to heat the evaporating materials to melt.

For evaporating aluminum, a small piece of aluminum can be hung in the loop of a tungsten filament, shaped as shown in Figure 11a. Since gold normally wets tungsten readily, a filament shaped like that for aluminum usually works well. However, a particularly shaped filament was used to save the evaporating gold. Figure 11b shows the V-shaped bowl in the center of a heater which was used to prevent the melting gold from evaporating in all directions. Aluminum-oxide was primarily coated on the spirally curled tungsten-wire to form the V-shape bowl.

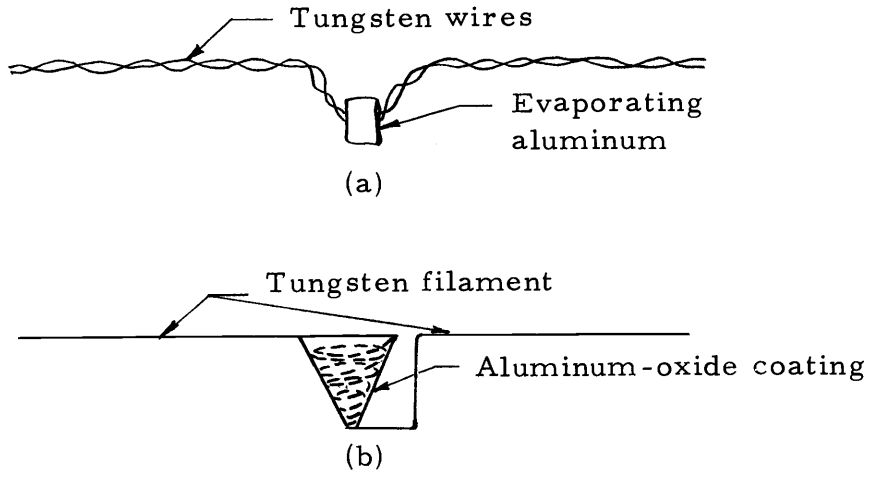


Figure 11. Filaments for evaporating metals. (a) For aluminum evaporation, (b) for gold evaporation.

The thickness of the evaporated aluminum and gold layer can also be measured with a 4-point probe. Although the exact amount of gold required for diffusion can be calculated. A series of experiments showed that a layer of 50 to 200 Å of vacuum-deposited gold would give an excellent result in diffusion for the wafers.

Gold Diffusion and Quenching

The gold diffusion was done in a furnace held at 1100°C. After diffusion for the necessary time period, the wafer was pulled out and cooled rapidly by laying it directly on a clean, cold, stainless steel plate. In order to obtain the most rapid heat dissipation, the wafer was moved slowly around on the steel plate. This rapid cooling was necessary in order to retain the highest possible gold concentration in the substrate.

Mask-Making for Test-Patterns

In order to etch the unnecessary portion of the aluminum layer off the silicon surface, a mask with the actual test-pattern size was necessary. Due to the tiny size of the actual test-patterns, the design work was done in a larger scale first. By reducing the image of the test-patterns to an actual size on an emulsion-coated glass-plate with a reduction camera, the final mask could be obtained after developing of the exposed glass-plate. Depending on the refinement of the

test-patterns to be obtained, a reduction between 20- and 60-fold could be applied.

Sequential Steps for Microstrip Making

The microstrips were to be fabricated on the top of the polished surface of the silicon wafer, which was first passivated with a layer of silicon-dioxide. The main steps for the complete process are shown schematically in Figure 12. Details in each step are described below:

a) Before applying or growing anything on the surface the wafers were cleaned with trichlorethylene, acetone, 4:1 buffered HF, and deionized water. The surface contamination and residual silicon-dioxide were thereby removed. The resistivity of each wafer was also checked in this step right after the cleaning process.

b) Silicon-dioxide films were grown on both sides of the wafer in wet oxygen (0.4 cfh oxygen bubbled through 95°C deionized water) at 1100°C for two and one-half hours in the oxidation furnace. A silicon-dioxide layer about 8500 Å thick was obtained on each side.

c) A photo-resist (AZ 1350) layer was applied on the top surface to protect the silicon-dioxide layer from 4:1 buffered HF etching. The wafer was baked on a 150°C hot-plate for 10

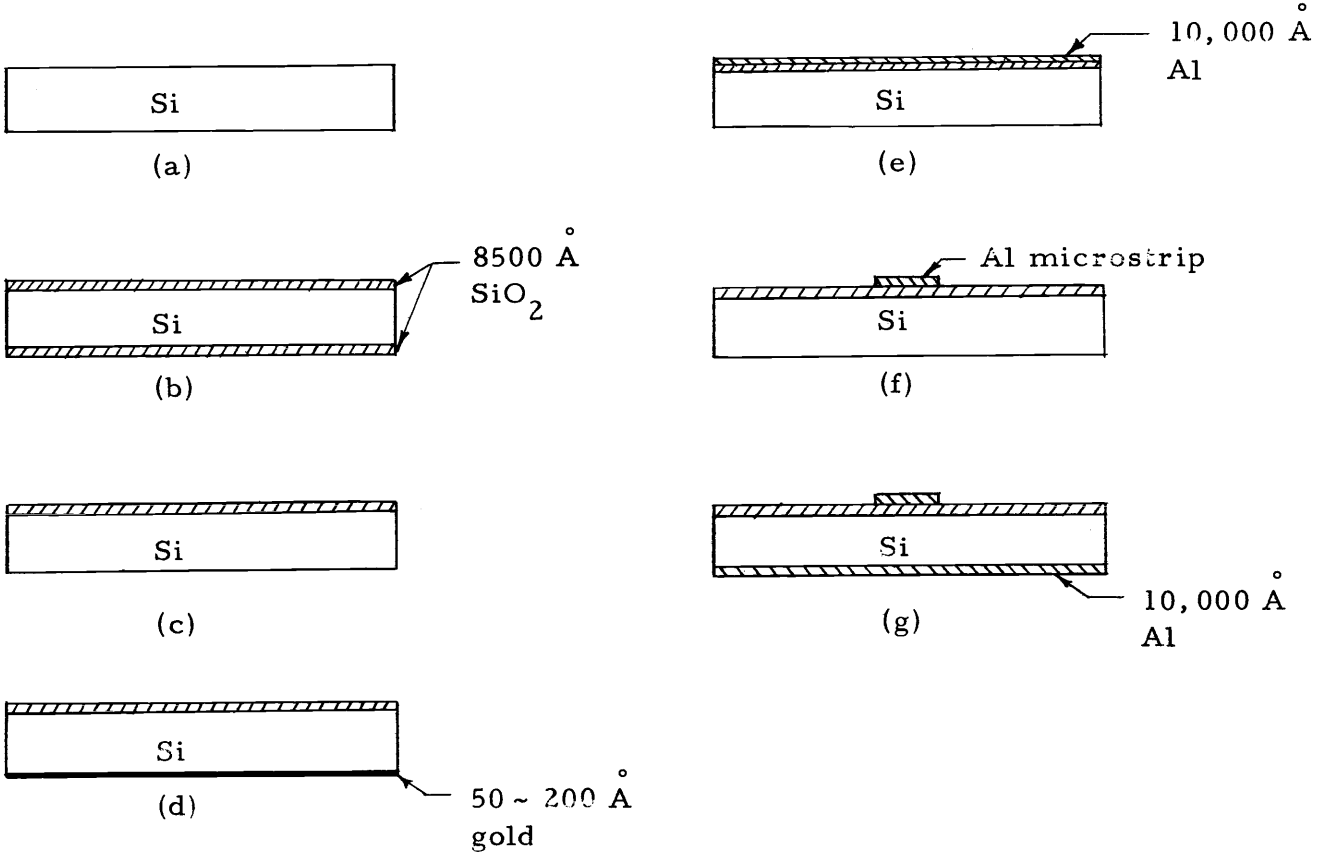


Figure 12. Schematic view of main process steps in microstrip fabrication on a gold-doped silicon substrate. (a) Wafer cleaning, (b) SiO_2 growing, (c) back-side SiO_2 etching, (d) gold deposition and diffusion, (e) aluminum deposition, (f) microstrip masking and etching, (g) aluminum ground-plane deposition.

minutes then dipped into 4:1 buffered HF solution for etching. It took about seven and a half minutes to etch off the 8500 Å thick silicon-dioxide layer on the back of the wafer.

d) In the Micro Automatic-Valving Vacuum Evaporator, a thin film (50 to 200 Å) of gold was evaporated onto the wafer surface from which the silicon-dioxide had been removed, the wafer was then put into the 1100°C furnace for gold diffusion. After 15 minutes diffusion in the furnace, with a nitrogen atmosphere, the wafer was pulled out rapidly and quenched. A small portion of silicon-dioxide on the top surface was etched off to permit resistivity measurement. Since the resistivity of the wafer after gold diffusion was very high and a good ohmic contact for the probes could not be made, the exact value of the resistivity was difficult to obtain. However, a value greater than 10^4 ohm-cm was measured for all wafers. This value is reasonable to represent the bulk resistivity. Since a capacitance-voltage characteristic measurement (20, p. 271) taken on the wafers showed that the wafers were still n-type and no inversion layer was formed at the surface, hence the 4-point probe was measuring the bulk resistivity. Frescura (19, p. 18) has suggested that good ohmic contacts could be made by alloying to the silicon small contacts of gold doped with antimony. Unfortunately,

this method was not used in this experiment.

e) An aluminum film about 10,000 Å in thickness was vacuum evaporated directly on the top of the silicon-dioxide layer.

f) By applying photo-resist masking, the aluminum layer was etched off the substrate except for the desired microstrip test-patterns, i.e., the mask used in this step had the test-patterns on it.

g) Again, vacuum evaporation was employed to deposit a 10,000 Å-thick aluminum layer on the back of the substrate as the ground plane.

Finally, the completed substrate was cut by a diamond-tipped scriber to fit the size of the test frame. In order to compare the results of the substrates with and without silicon-dioxide passivation, step (b) in Figure 12 was skipped for some substrates during the process.

V. POWER-DISSIPATION TESTS OF MICROSTRIPS ON A GOLD-DOPED SILICON SUBSTRATE

Test Fixture

In order to electrically test the microstrip test patterns, it was necessary to assemble the substrate to a specially designed test frame and attach special connectors to each end of each test pattern. Figure 13a shows the schematic view of the test frame, which was made of a brass block. Horizontal slots in each wall provided a movable mounting for the connectors to facilitate matching with the end of each microstrip test pattern.

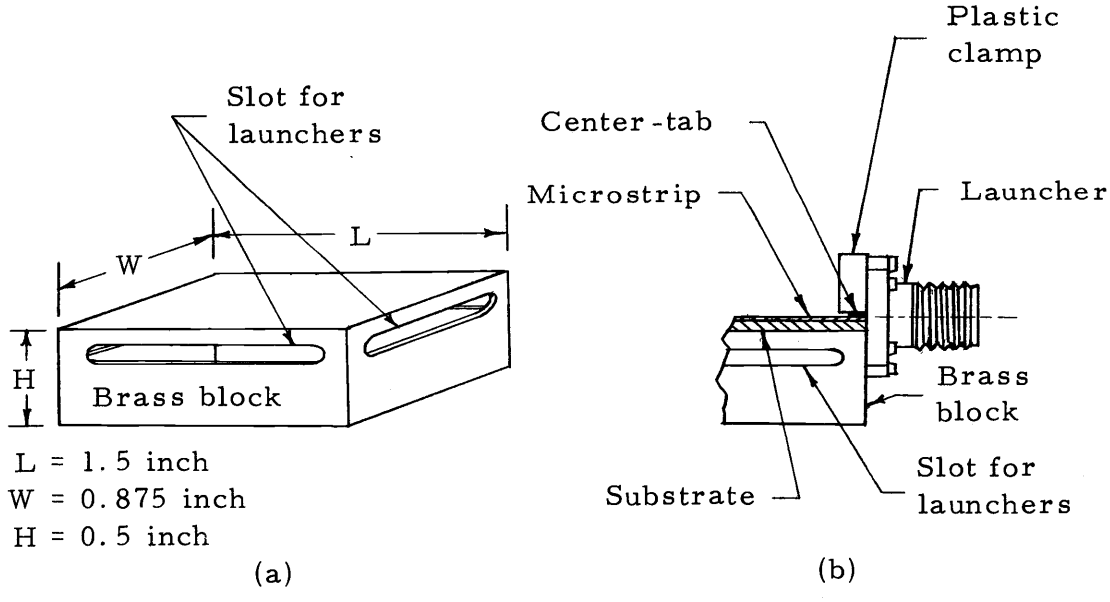


Figure 13. Test fixture for microstrips. (a) Main body of test frame. (b) Coaxial-to-microstrip transition.

Assembly was done by first laying the substrate on the brass block, then mounting the connectors on the side walls. Tek Wave Model 10-1001-0000 launchers were used as the connectors. A cross-sectional sketch of one end of the coaxial-to-microstrip transition is shown in Figure 13b. Whenever the launcher is placed with the center-tab on top of one end of the microstrip, the clamp-block, which is located above the center-tab, can be pressed not only to make the transition of microstrip-to-center-tab tight, but also to keep the whole substrate positioned on the brass block.

Mismatch at the Launcher

The launchers used for the connectors were primarily designed for 0.010 inch thick alumina substrates. Since a 0.010 inch wide microstrip on a 0.010 inch thick alumina substrate performs about 50-ohm in characteristic impedance, so the center-tab was also designed with 0.010 inch in its width to have a 50-ohm characteristic impedance to match the 50-ohm coaxial terminal. Nonetheless, in this case, the launcher still performs a mismatch about 1.15 in VSWR according to the specification provided by the manufacturer. If a 0.0082 inch thick silicon substrate is used, which was the case in the experiment, instead of 0.010 inch thick alumina substrate, the additional mismatch caused by the differences in thickness and dielectric constant can be calculated. A 0.010 inch wide center-tab on a

0.0082 inch thick silicon substrate yields a characteristic impedance of 40-ohm. Now the 50-ohm-to-40-ohm mismatch at the transition of coaxial-to-center-tab will cause 1.25 in VSWR which is about 0.05 db if converted into insertion-loss. This is the additional mismatch that inherently exists whenever a 0.0082 inch thick silicon substrate is employed, but does not exist in the case when alumina substrates are used. If the primary mismatch given by the manufacturer is also considered, then the total mismatch will cause as much as 0.1 db in loss.

Characteristic Impedance of Microstrips

As discussed in the first chapter, the characteristic impedance of microstrips, similar to that of transmission lines, is inversely proportional to the capacitance between microstrip and the ground plane. Since the capacitance varies with the width of microstrip, the value of characteristic impedance can be controlled by varying the width of microstrip for substrates with a fixed thickness.

Relationship between the characteristic impedance and microstrip dimensions for substrates with different dielectric constants is given in the literature (5, 22, 37, 42). The dimensions for the most used characteristic impedance in the power-dissipation test design are given below:

substrate material: silicon,

substrate thickness: 0.0082 inch,

microstrip width: 0.023 inch for Z_c = 25 ohm,

0.0059 inch for Z_c = 50 ohm;

where Z_c is the characteristic impedance.

The above values were obtained for a regular silicon substrate with dielectric constant $\epsilon_r = 11.7$. For a gold-doped silicon substrate, since no information has yet been found on the permittivity change caused by gold-doping, we assumed that the dielectric constant was the same as that of regular silicon. Under this assumption, the values given above will also be valid for gold-doped silicon substrate.

Introduction of Microstrip Design for Power-Dissipation Tests

In a lossy transmission line system, the variation of the input impedance Z_{in}, with a distance ℓ along the transmission line from a load Z_L, can be expressed with the formula (12, p. 94),

$$Z_{in} = Z_c \frac{1+\Gamma_L e^{-2j\beta\ell - 2\alpha\ell}}{1-\Gamma_L e^{-2j\beta\ell - 2\alpha\ell}}, \qquad (5\text{-}1)$$

where

Γ_L = voltage reflection coefficient at the load terminal,

$\beta = 2\pi/\lambda$ = phase constant,

Z_c = characteristic impedance of the transmission line,

α = attenuation factor,

λ = wavelength of the propagation wave.

If the input power P_{in} and the power transmitted to the load P_L are expressed, they have the following relation,

$$P_L = P_{in} e^{-2\alpha \ell} . \qquad (5-2)$$

There are two methods used for the power-dissipation test, based on either formula (5-1) or formula (5-2). The methods are discussed together with the test results in the following two sections.

Q-Measurement

One method used to measure the power dissipation of microstrips on a gold-doped silicon substrate was the Q-measurement of a transmission-type microstrip cavity. A full-wavelength of 25-ohm microstrip was used as the resonant transmission-line section. The Q-measurement was based on the half-power bandwidth of the transmitted power curve. Figure 14 shows the resonant microstrip section and its equivalent circuit. The two ends of the full-wavelength section are coupled by a tapered microstrip to match the center-tab of the launcher. The coupling capacitances are designated as C in the equivalent circuit. The attenuation constant α for the full-wavelength section was to be calculated from the measured Q. The

relationship between α and the Q, when $Z_c/\omega C$ for the coupling capacitance is not small, can be derived from the equivalent circuit. First, consider the imput impedance Z_2 and the voltage reflection coefficient Γ_2 at reference 2,

$$Z_2 = Z_c + \frac{1}{j\omega C},$$

$$\Gamma_2 = \frac{Z_2 - Z_c}{Z_2 + Z_c} = \frac{\frac{1}{j\omega C}}{2Z_c + \frac{1}{j\omega C}} = \frac{1}{2jZ_c\omega C + 1}.$$

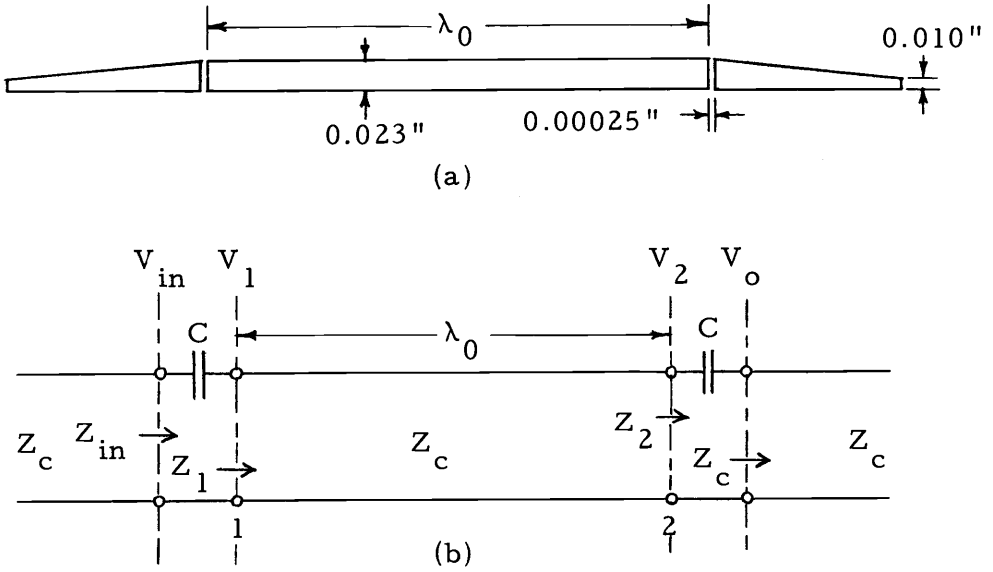


Figure 14. Microstrip for Q-measurement test. (a) Physical lay-out, λ_0 = 0.422 inch for 10 GHz and λ_0 = 0.437 inch for 9 GHz. (b) The equivalent circuit, Z_c = 25 ohm.

Secondly, consider the input impedance Z_1 at reference 1. By formula (5-1), given in the previous section,

$$Z_1 = Z_c \frac{1+\Gamma_2 e^{-2\alpha\lambda_0 - 2j\beta\lambda_0}}{1-\Gamma_2 e^{-2\alpha\lambda_0 - 2j\beta\lambda_0}}$$

$$= Z_c \frac{e^{\alpha\lambda_0 + j\beta\lambda_0} + \Gamma_2 e^{-\alpha\lambda_0 - j\beta\lambda_0}}{e^{\alpha\lambda_0 + j\beta\lambda_0} - \Gamma_2 e^{-\alpha\lambda_0 - j\beta\lambda_0}} .$$

If V_2^+ is the positively traveling voltage at reference 2, then the voltage at each reference point is

$$V_2 = V_2^+ + \Gamma_2 V_2^+ = (1+\Gamma_2)V_2^+ ,$$

$$V_o = V_2 \frac{Z_c}{\frac{1}{j\omega C} + Z_c}$$

and

$$V_1 = V_{in} \frac{Z_1}{\frac{1}{j\omega C} + Z_1}$$

$$= V_2^+ e^{\alpha\lambda_0 + j\beta\lambda_0} + \Gamma_2 V_2^+ e^{-\alpha\lambda_0 - j\beta\lambda_0}$$

$$= V_2^+ (e^{\alpha\lambda_0 + j\beta\lambda_0} + \Gamma_2 e^{-\alpha\lambda_0 - j\beta\lambda_0}) .$$

By canceling V_2, V_2^+ and Z_1 among the above equations, we have

$$V_o = V_{in} \frac{(1+\Gamma_2)Z_c^2}{(\frac{1}{j\omega C}+Z_c)[\frac{1}{j\omega C}(e^{a\lambda_0+j\beta\lambda_0} - \Gamma_2 e^{-a\lambda_0-j\beta\lambda_0}) + Z_c(e^{a\lambda_0+j\beta\lambda_0} + \Gamma_2 e^{-a\lambda_0-j\beta\lambda_0})]} .$$

Since $a\lambda_0 < 1$, we may take the following approximations:

$$e^{a\lambda_0} \cong 1 + a\lambda_0 + \frac{a^2\lambda_0^2}{2}$$

and

$$e^{-a\lambda_0} \cong 1 - a\lambda_0 + \frac{a^2\lambda_0^2}{2} .$$

Let ω_0 be the radian frequency that has the wavelength λ_0, then for frequency at the neighborhood of ω_0, $\omega = \omega_0 + \Delta\omega$,

$$\beta\lambda_0 = \frac{2\pi}{\lambda}\lambda_0 = \frac{2\pi\omega}{\omega_0} = 2\pi(1+\frac{\Delta\omega}{\omega_0}) .$$

Hence

$$e^{j\beta\lambda_0} = \text{Cos } \beta\lambda_0 + j \text{ Sin } \beta\lambda_0$$

$$= \text{Cos } 2\pi(1+\frac{\Delta\omega}{\omega_0}) + j \text{ Sin } 2\pi(1+\frac{\Delta\omega}{\omega_0})$$

$$\cong 1 + j2\pi\frac{\Delta\omega}{\omega_0} \quad \text{for small } \frac{\Delta\omega}{\omega_0} .$$

Similarly,

$$e^{-j\beta\lambda_0} \cong 1 - j2\pi\frac{\Delta\omega}{\omega_0} .$$

If we further assume that $\omega_0 C Z_c < 0.1$, then by substituting these approximations into the formula for V_o and after a tedious simplification, we have an approximate final form

$$V_o \cong -V_{in} \frac{\omega_0^2 C^2 Z_c^2}{A + jB}$$

where

$$A = a\lambda_0 - \omega_0^2 C^2 Z_c^2 - \omega_0 C Z_c \frac{2\pi\Delta\omega}{\omega_0} - 2Z_c \omega_0 a\lambda_0 \frac{2\pi\Delta\omega}{\omega_0},$$

$$B = 2Z_c \omega_0 C + a\lambda_0 \omega_0 C Z_c + \frac{2\pi\Delta\omega}{\omega_0} + 2Z_c \omega_0 C \frac{\Delta\omega}{\omega_0}.$$

The result shows that the transmitted voltage V_o is not uniformally affected by the attenuation constant a if the input voltage V_{in} is maintained constant over the neighborhood of ω_0. It can be calculated that the maximum value of V_o occurs at

$$\Delta\omega_{max} \cong \left(\frac{-\omega_0 C Z_c}{\pi + 2\omega_0 C Z_c} \right) \omega_0$$

for $\Delta\omega_{max} = \omega_{max} - \omega_0$, and the bandwidth of the half-power points is approximately

$$BW_{3db} \cong \left[\frac{a\lambda_0 + a\lambda_0 \omega_0 C Z_c / \pi + (1 + 5a\lambda_0)\omega_0^2 C^2 Z_c^2}{1 + 2\omega_0 C Z_c / \pi} \right] \frac{\omega_0}{\pi}.$$

If we define

$$Q = \frac{\omega_{max}}{BW_{3db}}$$

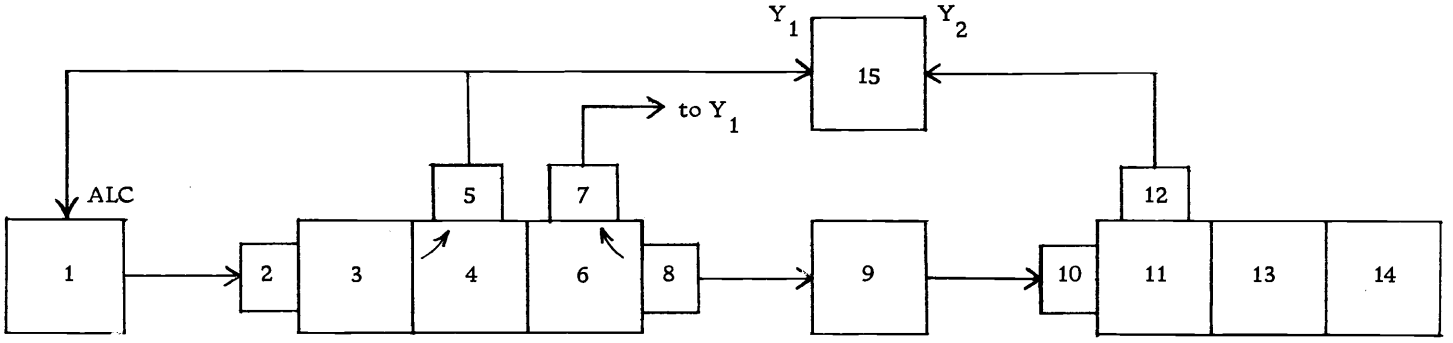
then $\frac{\omega_0}{BW_{3db}} \cong \frac{\omega_{max}}{BW_{3db}} = Q$ providing $\Delta\omega_{max}$ is small. Hence

$$Q \cong \frac{\pi + 2\omega_0 CZ_c}{a\lambda_0 + a\lambda_0\omega_0 CZ_c/\pi - (1+5a\lambda_0)\omega_0 CZ_c}.$$

This formula was applied under the assumption that the mismatches existing at the coaxial-to-microstrip transitions did not affect the profile of the transmitted power over the range of frequencies for which appreciable power was transmitted.

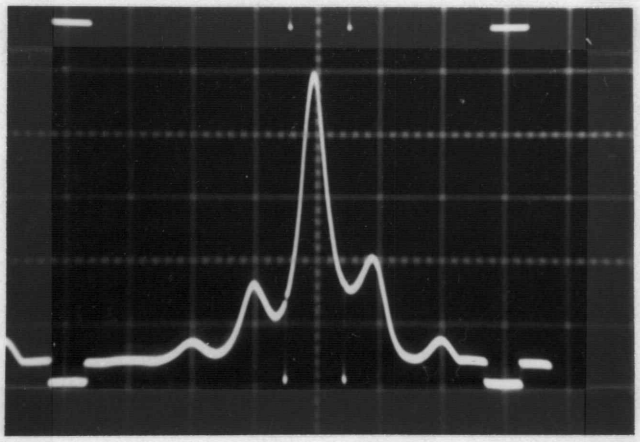
Resonant sections for nine and ten GHz were designed. The coupling capacitance consisted of a gap in the microstrip 0.023 inch wide and 0.00025 inch long. The resulting capacitance is estimated to be 0.05 pf (22, p. 72), which gives $\omega_0 CZ_c \cong 0.08$ at ten GHz, a result which is not negligible in the Q formula.

Figure 15 shows the block diagram of the equipment arrangement used for Q-measurement. A typical swept-frequency curve obtained from the Q-measurement and a picture of the test fixture with the resonant section on it are shown in Figure 16. The ripples existing along the swept curve were caused by mismatches at adaptors for waveguide-to-coaxial transition and launchers in the measuring system (30).

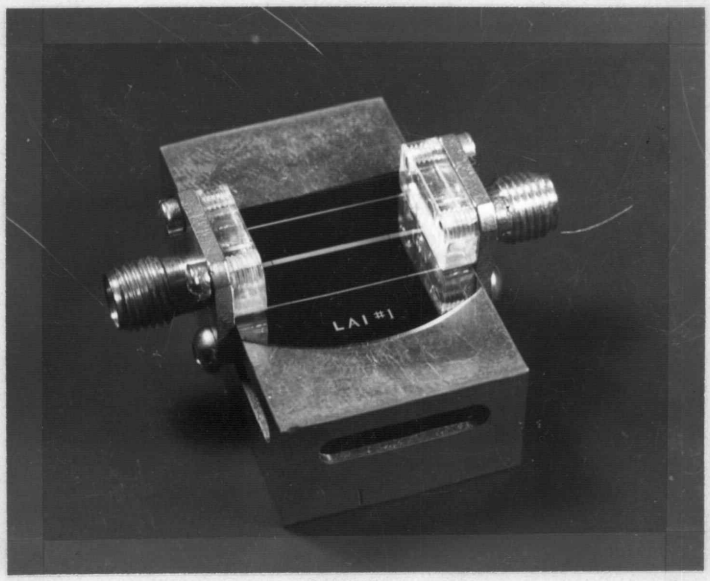


1. HP 8690A X-band sweep oscillator
2, 8, 10. Coaxial-waveguide adapter
5, 7, 12. Waveguide-type crystal detector
3, 13. Waveguide-type isolator
4. Waveguide-type 20-db directional coupler
9. Microstrip test-fixture
6, 11. Waveguide-type 10-db directional coupler
14. Waveguide-type termination
15. Dual-trace oscilloscope
——. Coaxial-cables

Figure 15. Block diagram of the entire test system for power-dissipation test.



(a) Transmitted power, arbitrary scale.
Marker frequencies, 8.88 and 9.05 GHz.



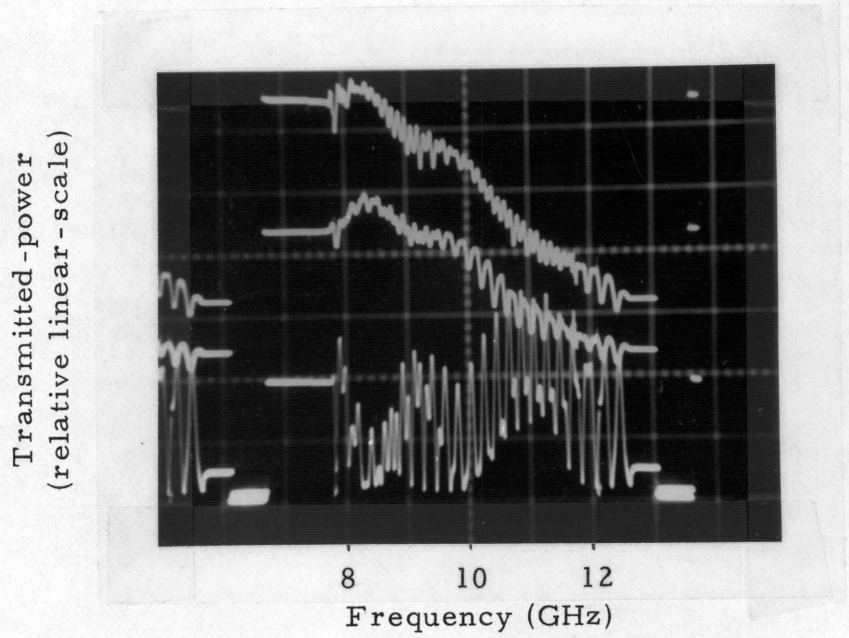
(b) Microstrips for Q-measurement (center) and for direct insertion-loss test (top and bottom).

Figure 16. Q-measurement response and the test fixture.
(a) Transmitted-power curve of Q-measurement.
(b) Test fixture with microstrips on the substrate.

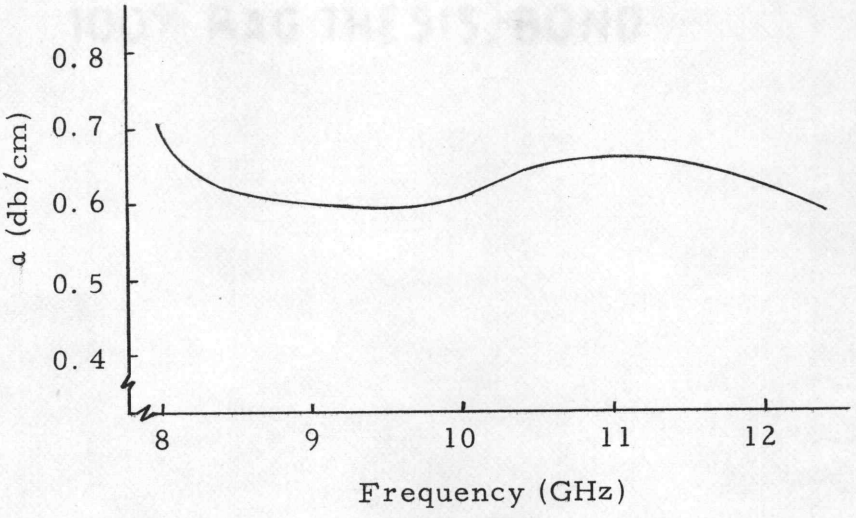
The measures Q ranged from 45 to 60. A Q of 60 gave about 0.28 db/cm for α according to the given formula. A similar measurement had been done by Emery and Noel (15) for a 1050 ohm-cm silicon substrate without gold-doping. In their work, a simpler formula, $Q = \pi/\alpha\lambda_0$ was used and the resonant transmission-lines were half-wavelength at 15 to 18 GHz. They obtained a value of about 0.56 db/cm for 25-ohm microstrip. If their formula were used for a Q of 60, then the value of α obtained from our tests would be 0.40 db/cm.

Direct Insertion-Loss Test

Another method for measuring the power dissipation for microstrips was to take the insertion-loss for a 0.875 inch long, 50-ohm microstrip by comparing the transmitted powers through the system with and without the 50-ohm microstrip. In the circuit without the 50-ohm microstrip, a straight, coaxial-to-coaxial adapter (OSM Model 217) was used in place of the microstrip test fixture. Two 50-ohm microstrip-lines used for the insertion-loss test were fabricated on the same substrate as the resonant section, as shown in Figure 16b. The frequency was swept from 7.8 to 12.4 GHz. The transmitted-power curves for the systems with and without the 50-ohm microstrip are shown in Figure 17a. Again, the ripples were caused by the mismatching in the adaptors and launchers. Since coaxial-cables



(a) Transmitted-powers, without 50-ohm microstrip (top), with 50-ohm microstrip (center), reflection at input terminal with 50-ohm microstrip (bottom).



(b) Converted attenuation factor.

Figure 17. Results of the direct insertion-loss test.
(a) Transmitted-power curves for X-band sweep.
(b) Attenuation factor α converted from (a).

were used to connect all waveguide-type components in the measuring system, their consumption of more power at higher frequencies caused the transmitted-power to decay along the low-to-high frequency sweep, which is apparent in the picture.

The attenuation constant α was also obtained by using the insertion-loss technique, i.e., in formula (5-2), by letting

P_{in} = power transmitted through the system without the 50-ohm microstrip, which was held at the same input level as the input power to the 50-ohm microstrip,

P_L = power transmitted through the system with the 50-ohm microstrip,

ℓ = 0.875 inch = 2.22 cm, length of the 50-ohm microstrip;

then α can be expressed as:

$$\alpha = \frac{10 \times \log_{10}(\frac{P_{in}}{P_L})}{(20 \times \log_{10} e)\ell}$$

or

$$\alpha(\frac{db}{cm}) = \frac{10 \times \log_{10}(\frac{P_{in}}{P_L})}{2.22} .$$

Figure 17b shows values for α after the above conversion from Figure 17a. These values are higher than the value of 0.45 db/cm

given by Hyltin (23), for 50-ohm microstrip on 1500 ohm-cm silicon substrate without gold-doping. However, the total insertion-losses included the effect caused by the mismatches existing at the launchers.

Theoretically, a very realistic value for the power loss resulting from the mismatches could be obtained by comparing the reflected powers at the input terminal in system with the 50-ohm microstrip, as shown in Figure 17a, and in that with only a straight coaxial-to-coaxial adapter, as shown in Figure 18. Unfortunately, due to the large ripples existing in both reflected powers, a significant value for the change in reflected power was not obtained. An alternative way was to use the value roughly calculated in the early section of this chapter, i.e., about 0.1 db for each launcher. Then the assumed mismatch-loss for both launchers would convert to 0.09 db/cm.

Since the power-loss in the conductor and that in the substrate could not be separated, the attenuation factor α obtained in the experiments represented the total power-loss factor for the microstrip system. Total power-loss of about 0.15 db/cm at 10 GHz for a 50-ohm microstrip on a 0.025 inch thick alumina substrate (21) may be applied as a rough upper-limit for the power-loss in the conductor only.

Microstrips on a similar silicon substrate without gold-doping have also been tested with both Q-measurement and direct insertion-loss tests. The transmitted powers were not detectable, which showed

that the gold-doping in the silicon substrate made a great improvement for sustaining wave-propagation.

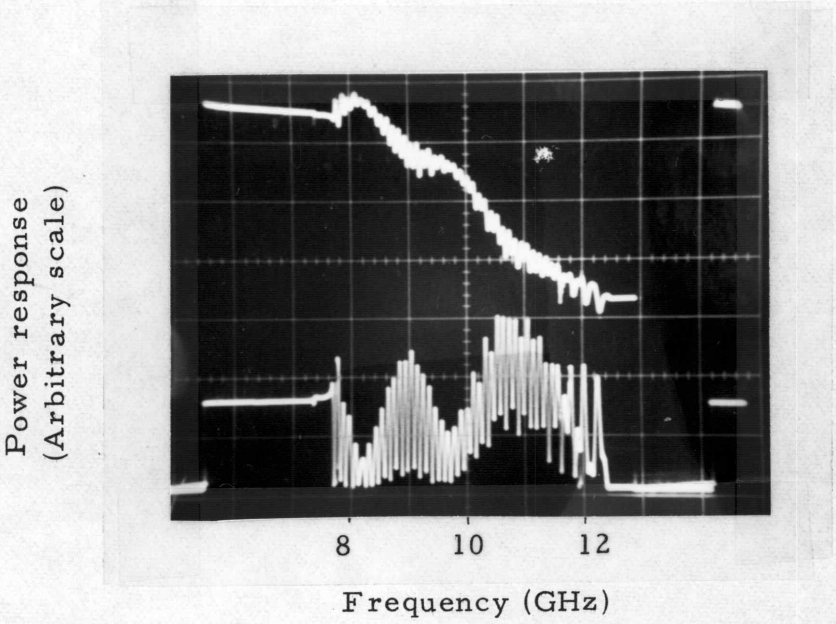


Figure 18. Responses of a system with only a straight coaxial-to-coaxial adapter. Transmitted-power (upper trace) and reflected-power (lower trace).

VI. BAND-PASS FILTER APPLICATION

Parallel-Coupled Transmission-Lines

Jones and Bolljahn (26) have described the behavior of a pair of shielded and coupled striplines by means of an impedance matrix. As shown in Figure 19, the coupled strip-lines, according to the direction of currents, can be characterized with two different characteristic impedances:

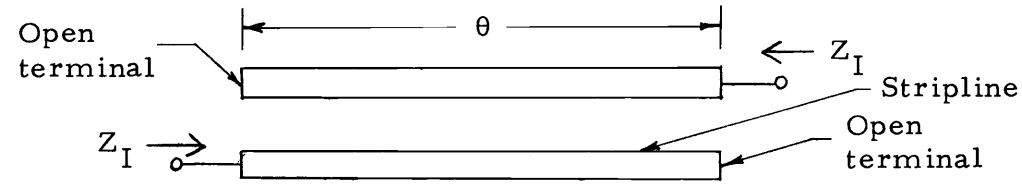
Z_{oe} = characteristic impedance of one stripline to ground with equal currents in the same direction (the even mode),

Z_{oo} = that of one stripline to ground with equal currents in opposite directions (the odd mode).

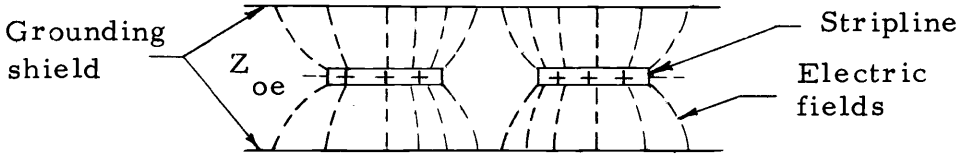
The image impedance Z_I and image phase-shift β_I were derived in terms of these even and odd-mode characteristic impedances and the electrical length of the coupled striplines θ:

$$Z_I = \frac{[(Z_{oe}-Z_{oo})^2-(Z_{oe}+Z_{oo})^2\text{Cos}^2\theta]^{1/2}}{2\ \text{Sin}\ \theta},$$

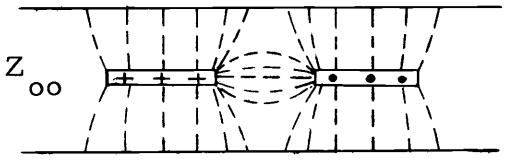
$$\text{Cos}\ \beta_I = \frac{Z_{oe}+Z_{oo}}{Z_{oe}-Z_{oo}}.$$



(a) Z_I, image-impedance



(b) Currents in the same direction



(c) Currents in opposite directions

Figure 19. Shielded coupled-striplines. (a) Top-view. (b) Cross-sectional view of even-mode. (c) Cross-sectional view of odd-mode.

Parallel-Coupled Band-Pass Stripline Filter

Since the shielded striplines could be dealt with as an ideal transmission-line set, Cohn (10) has developed a series of approximate equivalent circuits for these coupled striplines that would lead to a band-pass filter providing a proper electrical length of each coupled stripline were given. Figure 20 shows the equivalent circuits that leads to a band-pass filter. A single pair of coupled striplines is

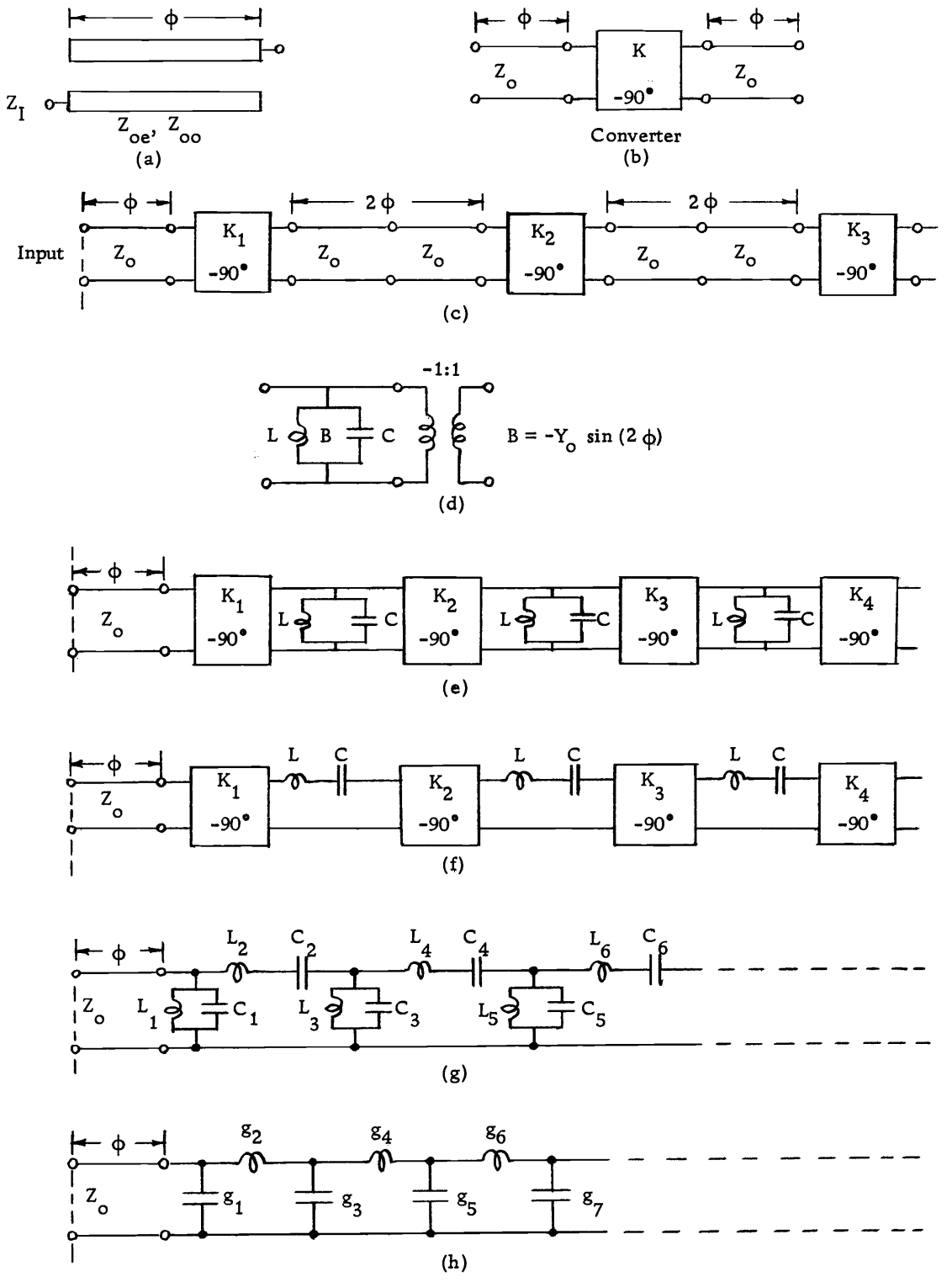


Figure 20. Development of equivalent circuit of the parallel coupled-stripline filter.

shown in (a), it is approximately equivalent to the circuit in (b) when ϕ is around 90°. Consequently, a cascade of these coupled-stripline pairs will form an equivalent circuit as in (c). While a single section with electrical length of 2ϕ in (c) can be approximated by the circuit of (d) providing ϕ is near 90°. The phase-reversing transformer in (d) actually has no effect on the insertion-loss response, hence it can be omitted for the approximation of a filter design. Therefore circuit (e) is approximately equivalent to (c). Since circuit (e) is the dual of circuit (f), it can be transformed (11) into a circuit as in (g). While (g) is a band-pass filter transformed from the prototype low-pass filter of (h), which can be either of equal-ripple or maximally flat.

If the specifications of a band-pass filter are given, the number of pairs of the coupled striplines should be chosen first, then the element values in Figure 20g can be calculated by frequency transformation of the prototype low-pass filter. All the formulas of this transformation and that of the rest of the equivalent circuits were given in Cohn's paper (10). Accordingly, the final even- and odd-mode characteristic impedances for each section of the coupled striplines can be obtained.

Z_{oe} and Z_{oo} of the Coupled Microstrip-Lines

Although the circuit transformation in the previous section can be applied to the microstrips as well as to the shielded-striplines providing the total length of the microstrip is not very long, the even- and odd-mode impedances are different in these two cases due to the different configurations.

The relationship between the physical dimensions and the characteristic impedances Z_{oe} and Z_{oo} for a pair of coupled microstrip-lines has been derived by several authors (5, 7, 25, 27, 28). Their calculations have provided data for many substrates of different dielectric constants. However, the data for a silicon substrate are still not available yet, though they may be calculated by the given equations. Due to the large amount of computer time required for these calculations, an alternative method was used. It was to deduce the data for silicon substrates from that available for other substrates with different dielectric constants. For example, the physical dimensions of a pair of coupled microstrip-lines with $Z_{oe} = 95.6$ ohm and $Z_{oo} = 37.7$ ohm on substrates of various dielectric constant could be obtained from the data given by Chen (7) and others (5, 25, 27). These values are plotted in Figure 21. By the property of continuity of these values, the value for the silicon substrate can be roughly deduced.

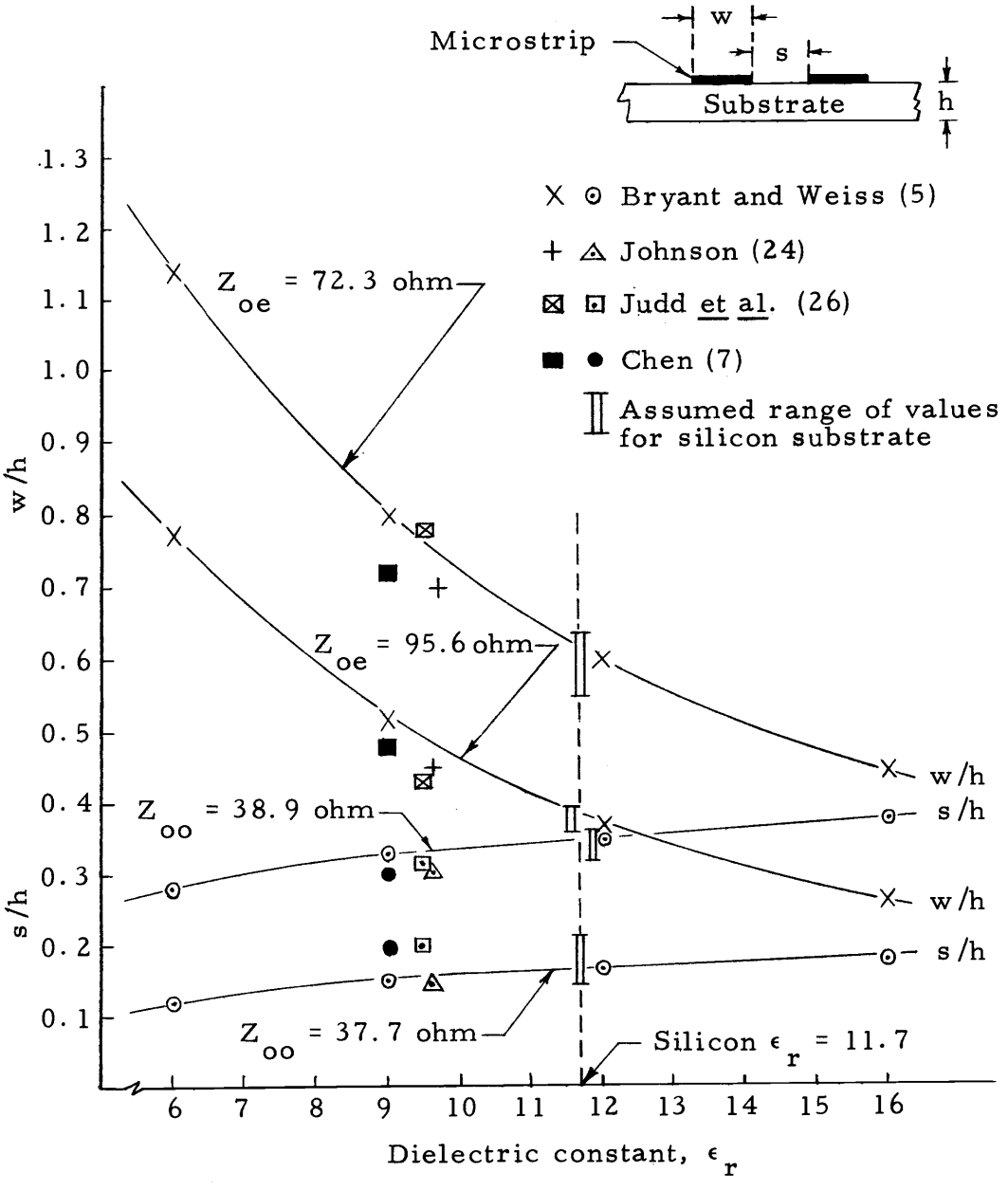


Figure 21. Width-to-height and spacing-to-height ratios for a coupled microstrip-lines with fixed even- and odd-mode impedances as a function of various dielectric constants for the substrate.

Microstrip Realization for the Band-Pass Filter

In order to compare with the results from that on an alumina substrate, the band-pass filters on the gold-doped silicon substrate were purposely designed with the same specifications as used by Johnson (25):

a) maximally flat, band-pass,

b) pole number $p = 2$,

c) center frequency $f_0 = 9.0$ GHz,

d) bandwidth $W = 30\%$,

e) number of sections of the coupled microstrip-lines $n = 3$,

f) element values in the prototype low-pass filter $g_0 = 1.00$, $g_1 = 1.414$, $g_2 = 1.414$, $g_3 = 1.00$,

g) matching impedance at the terminals $Z_o = 50$ ohm,

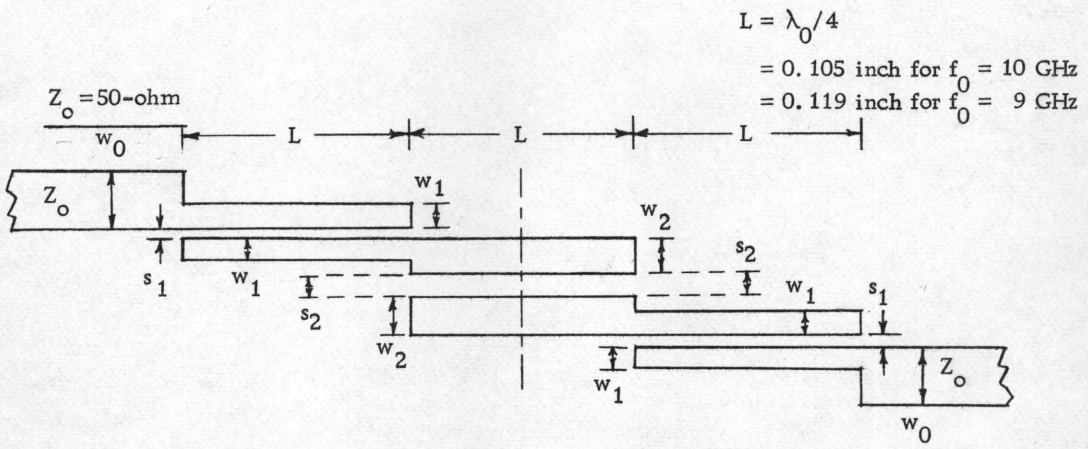
h) even- and odd-mode characteristic impedances for each section of the coupled microstrip-lines

$(Z_{oe})_1 = 95.6$ ohm $\quad (Z_{oo})_1 = 37.7$ ohm

$(Z_{oe})_2 = 72.3$ ohm $\quad (Z_{oo})_2 = 38.9$ ohm

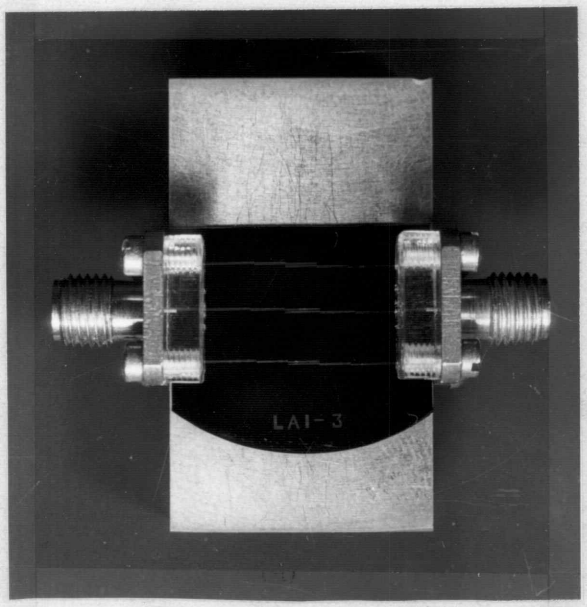
$(Z_{oe})_3 = 95.6$ ohm $\quad (Z_{oo})_3 = 37.7$ ohm.

The dimensions for those microstrip-lines with the above characteristic impedances were obtained from Figure 21 in the previous section and are given in Figure 22a. Figure 22 shows the layout of the entire filter and a picture of the test fixture with the filters on it.



Design Values	Measured Values
w_0 = 0.0059 inch	w_0 = 0.006 inch
w_1 = 0.0027 inch	w_1 = 0.003 inch
w_2 = 0.0048 inch	w_2 = 0.005 inch
s_1 = 0.00144 inch	s_1 = 0.001 inch
s_2 = 0.00308 inch	s_2 = 0.003 inch

(a)



(b)

Figure 22. Parallel-coupled microstrip-lines band-pass filters. (a) Dimensions in detail. (b) Filters on the test fixture, f_0 = 10 GHz (center), f_0 = 9 GHz (top and bottom).

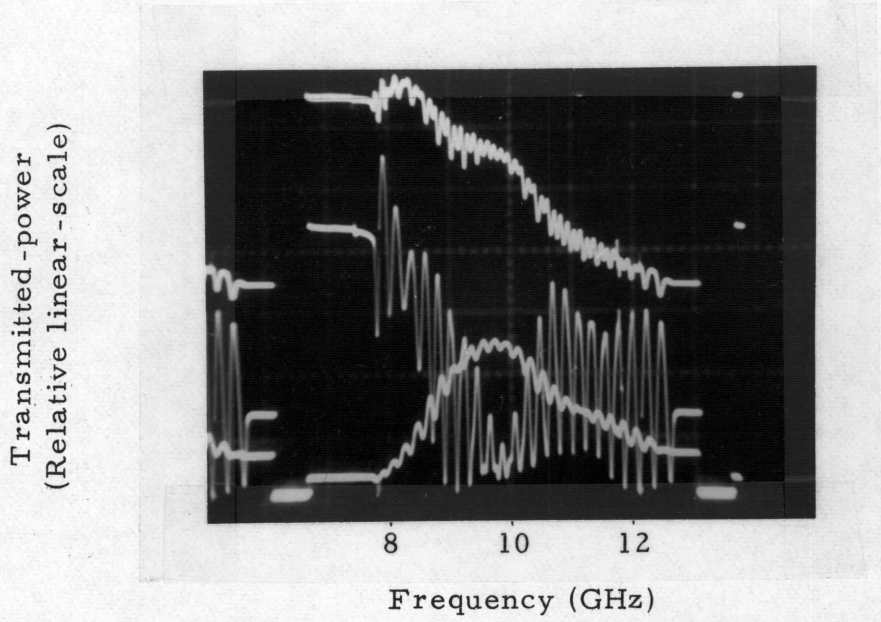
The response of the filter was measured with the same system as used for the direct insertion-loss test for microstrip power-dissipation. The transmitted-powers through the measuring system with and without the filter are shown in Figure 23a. Their difference is the insertion-loss of the filter and launchers. Figure 23b shows the insertion-loss expressed in decibels obtained from Figure 23a by using the following calculation:

$$\text{Insertion-loss} = 10 \times \log_{10}\left(\frac{P_2}{P_1}\right);$$

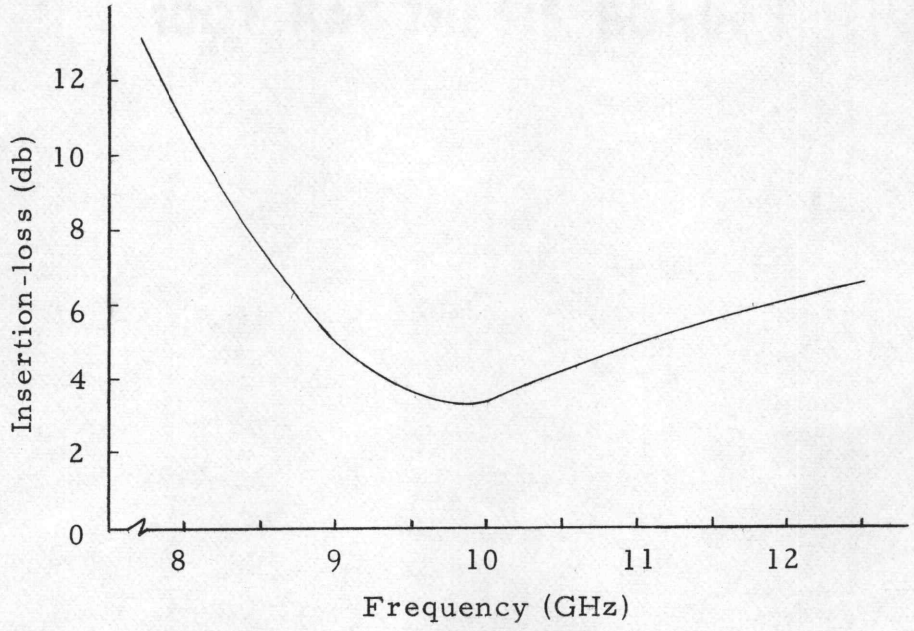
where P_1 and P_2 designate the power transmitted through the system with and without the filter, respectively.

It shows an insertion-loss of about 3.3 db at the center frequency and a bandwidth of about 36%. These results are rather unsatisfactory for a band-pass filter. However, if we take into account the power dissipated in the 1.5 cm extra 50-ohm connecting microstrips for the filter and the mismatches at the launchers, the actual insertion-loss at the center frequency is less than 2.3 db.

In Figure 23b, a frequency shift of about 0.2 GHz from the design center frequency of 10 GHz was noted. This frequency-shift and the rather high insertion-loss at the center frequency show the filter was not optimumly designed. The poor design may be attributed to the following factors: a) the value of substrate thickness used for



(a) Transmitted-powers, without the filter (top), with the filter (bottom); reflected-power from the filter (middle). Design center-frequency f_0 = 10 GHz.



(b) Insertion-loss vs frequency.

Figure 23. Responses of a parallel-coupled microstrip-lines band-pass filter. (a) Swept power responses. (b) Converted insertion-loss curve.

design was the average value of 0.0082 inch, while the actual value of the tested wafer was 0.0083 inch in thickness; b) the exact values for s/h and w/h in Figure 21 were unable to be determined; c) the fringing capacitance at the open end of each microstrip section was not compensated (10); d) the final dimensions after fabrication did not agree with the design values as shown in Figure 22a, the measured s_1 is 30% off the design value. This problem came from improper mask cutting before the reduction process. However, if efforts are made to eliminate the errors listed above, a more satisfactory performance can be expected to be attained.

VII. CONCLUSIONS

The experiments showed that the power-dissipation of microstrips on gold-doped silicon substrates was at least as low as that on intrinsic silicon substrates before the fabrication of solid-state devices.

In the filter application, the performance was not as good as hoped. There was no way to determine whether the rather unsatisfactory result was mainly due to the power-dissipation of microstrips or to the improper design of the filter. However, after investigation of the completed filter, it was found that the physical dimensions were very much off the design values (as high as 30%). Since the power-dissipation of a single microstrip line has been determined and it has been shown that it was good enough for practice, it can be believed that had the filter been more carefully designed and fabricated, e. g., more precise cutting in mask-making, a much better performance could be obtained.

Since gold-doping is applied only after the completion of the fabrication of all solid-state devices on a silicon substrate, the disadvantage of resistivity decrease that exists for the intrinsic silicon substrate does not appear for the gold-doped silicon substrate. Also, the gold-doping can be applied to the low resistivity silicon substrates which are relatively cheap and easier to obtain than the intrinsic

silicon substrate. From these facts it appears that the gold-doped silicon substrate is advantageous for microwave integrated-circuit application.

If a monolithic integrated-circuit application is desired, a change in processing technique in forming the active devices is required, because of the extra diffusion of impurities that is caused by the additional high temperature processing required for the gold-diffusion. However, the gold-diffusion time is fixed and short, so the required diffusion profile of the impurities can still be ultimately obtained by reducing the diffusion times for the impurities prior to the gold-doping by exactly the same amount of time which will be required to do the gold-diffusion.

The effects of gold-doping on the behavior of solid-state devices have been discussed by several authors (2, 18, 31, 33, 35). One of the most significant effects is that the reverse recovery-time of the p-n junction can be decreased by introducing gold-doping. Hence it can provide a good application for the design of high-speed switching circuits.

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