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The thesis presents a new algorithm and structure that is to be used in conjunction with a specially modified CMOS Gilbert cell mixer to remove time-varying DC offsets in direct conversion receivers. In our approach, the DC offset is detected at the output of the mixer using a dedicated coarse ADC and tracked using a low gate count digital structure. The estimated offset is then used to dynamically adjusting the bias of a specially modified Gilbert cell mixer to cancel the offset in the mixer. This prevents saturation and desensitization of the analog downstream stages. The presented approach is suitable for TDMA as well as continuous reception techniques such as W-CDMA and FH-SS while being fully integrable on-chip.

Adaptive Dual-Loop Algorithm for Cancellation of Time-Varying Offsets in Direct Conversion Mixers

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1. INTRODUCTION

The explosive growth in the demand for wireless products in recent years has resulted in intensifying efforts to develop single chip transceiver designs to reduce cost, power consumption and size. Of the many proposed architectures, direct conversion is perhaps the most promising for low complexity, low power and low cost monolithic integration. Additionally, direct conversion receivers are also well suited for use as an analog front end in software radio designs. However, the realization of direct conversion receivers in CMOS technology has thus far been limited mainly because of the problem of large, time-varying offsets created in the mixer as a result of self-mixing products. Self-mixing arises from insufficient on-chip isolation between the local oscillator (LO) port of the mixer and the input of the low noise amplifier (LNA) as well as the mixer RF port. Having the same signal present at the RF and the LO port of the mixer produces a DC component at the output of the mixer. The offset can be divided into a static and a time-varying component. Coupling of the LO to the LNA and RF port of the mixer resulting in so called LO self-mixing, causes a static or fixed DC offset at baseband. This offset only depends on the LO frequency. When a strong interferer leaks from the RF to the LO port (causing interferer self-mixing) or the LO couples to the antenna, radiates and then reflects off moving objects back to the antenna (causing LO leakage self-mixing), a time-varying or dynamic offset is created at the mixer output. The time-varying offsets of CMOS mixers are often 20 to 30dB larger than the desired signal level. A detailed description of the self-mixing effects occurring in direct-conversion receivers can be found in [1].

In addition to the self-mixing products, undesired DC offsetS are also produced by circuit mismatch in the mixer output stage and the baseband gain stages and filters.

Offsets due to mismatch are fairly static and change only with process, voltage and temperature variation. These offsets can therefore easily be removed by a narrow notch filter as long the baseband gain is keep constant. This is the case for conventional heterodyne receiver where the receiver gain is typically adjusted at intermediate frequency (IF) using a variable gain amplifier (VGA). No baseband gain stages are required.

However, in a homodyne architecture we have no IF to realize gain and the gain adjustment therefore has to be done either at RF or baseband. Since the achievable gain in the RF front end is generally limited we require baseband gain stages to achieve the required signal level for the detector. However, this causes the DC offset to change rapidly during receiver gain stepping which is required to account for the change in received signal power. If this DC steps are not removed quickly, the receiver performance is degraded drastically due to the potential saturation of the downstream stages.

The effects described above typically cause the offset to have a shape similar to that shown in Figure 1.1. The static DC component is created by LO self-mixing. This component only changes with the LO frequency and temperature. A piecewise constant DC is produced by circuit mismatch at baseband where the offset changes with the applied baseband gain. Finally the time-varying component of the DC is given by interferer and LO leakage self-mixing.

Approaches to remove the offset have so far mostly been focused on three methods. For modulation formats that have no or little spectral power at DC, AC coupling the mixer output, or some downstream stage, can be used to remove the offset. To avoid unacceptable distortion due to removing the lower frequency spectrum of the signal, AC coupling requires large capacitor values that are not realizable on-chip [2], [3]. Additionally, AC coupling using large capacitor values often results in a failure to track fast variations in the offset voltage due to fading and baseband gain stepping.

The second common approach to remove offsets is to apply a digital cancellation algorithm to the sampled signal before the decision device [4], [5]. In this approach the offset is detected and removed digitally by time-averaging or by using more complex methods such as differentiating the received signal [4]. However, digital cancellation

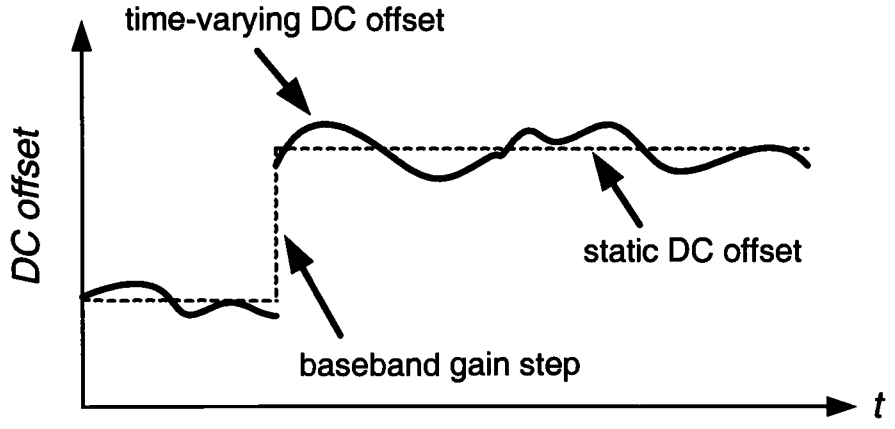

FIGURE 1.1: DC offset seen at baseband.

requires the analog baseband stages following the mixer to have enough spurious-free dynamic range (SFDR) to tolerate the DC offset. It also requires more bits in the ADC to achieve the same sensitivity and bit error rate (BER) as when the offset is not present.

For wireless standards that incorporate time-division multiple access (TDMA) another method has been proposed [1]. In TDMA each mobile phone spends some of its time in an idle mode so as to allow other users to communicate with the base station on the same channel. This idle time can be used to measure the offset and subtract the value during the reception of the next burst. This approach only works if the offset can be assumed constant during the reception of at least two bursts (the burst used to measure plus the consecutive reception burst). In GSM the Doppler spread of the offset is around 200Hz and can therefore be neglected due to the short burst time of 577μs. However, for the case of two unsynchronized TDMA system another problem occurs. During the reception of the desired burst, a burst from an alien system can start. This causes repeated jump changes in the offset due to interferer self-mixing, possibly in the middle of every burst. Thus, measuring the offset during idle time may not provide an accurate offset measurement.

To develop a robust monolithic direct conversion receiver new methods to remove the offsets must be found. The approach that we propose in this paper is a digitally controlled analog cancellation technique. A first approach in this direction was presented in [6]. In our approach, we stress that the analog offset cancellation in the mixer does not need to be perfect (we strive only to eliminate desensitization) — fine tuning the offset correction will occur in the digital domain before the decision device using methods such as those presented in [4] and [5].

2. OFFSET CANCELLATION APPROACH

To avoid having to overdesign the analog baseband stages to tolerate the offsets, it is best that adaptive cancellation takes place at the point of origin of the offset, in the mixer. As mentioned before, our goal is to suppress the offset down to the minimal detectable signal level, which can be up to 30dB smaller than the offset.

The cancellation scheme is shown in Figure 2.1. The output of the mixer is sampled by a dedicated ADC. A dual-loop algorithm, the contribution of this work, is the detector. The offset is then cancelled in the loads of a specially designed mixer [7]. The probably biggest advantage of this scheme is that it can be fully integrated on-chip requiring no additional off-chip components.

Using a dedicated, coarse ADC to sample the mixer output, instead of measuring the offset at the decision device, seems to require an unnecessary increase in complexity. However, there are two reasons for our approach: First, it decreases the feedback delay and thus improves the reaction time to jump changes in offset. Second, the additional ADC is decoupled from the downstream stages, especially from the VGA and AGC loop. This largely simplifies the overall design of the receiver. If the VGA is realized in the digital domain, the dedicated ADC is no more required and the dual-loop filter can be

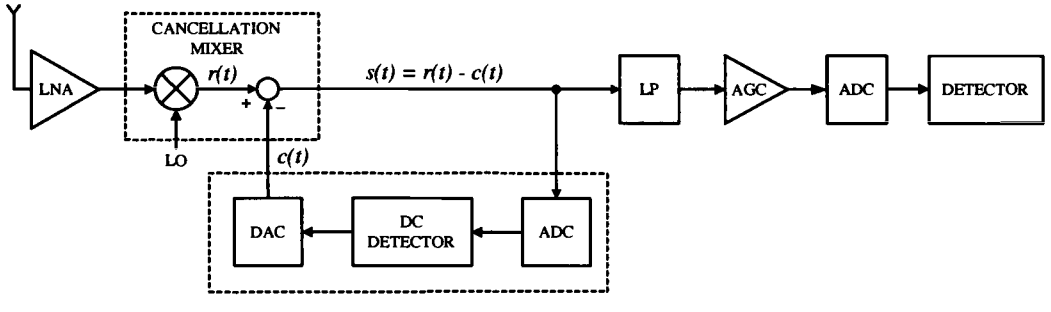

FIGURE 2.1: Receiver chain with cancellation mixer.

fed with the output of the detector ADC before the digital VGA. As mentioned above this might slow down the reaction time of the DC cancellation loop.

For our approach to be attractive, the digital offset estimation and the cancellation mixer must be simple. The following two sections describe the offset cancellation mixer and the offset detection algorithm, although the focus of this paper is on the digital DC detection algorithm.

3. OFFSET CANCELLATION MIXER

The CMOS offset cancellation mixer that was developed for use with our algorithm is based on a standard Gilbert cell mixer. The double balanced structure provides high port to port isolation and rejects common mode digital clock noise. But the mixer can still generate large offset currents, due to the reasons stated earlier. However, by using our algorithm to digitally control the bias of the active loads we can produce cancellation currents equal to the offset currents. Ideally, this will prevent offsets from appearing at the differential output of the mixer. A more detailed description of the offset cancellation mixer can be found in [7].

4. DUAL-LOOP ALGORITHM FOR OFFSET ESTIMATION

The heart of the offset cancellation is the manner in which we estimate the offset. Simple time-averaging of the mixer output signal to estimate the offset is inadequate due to the jump changes in offset as mentioned before. The adaptive offset measurement approach presented in this paper is therefore based on a dual-loop (modified gear shifting) filter as shown in Figure 4.1.

Our system, which is similar in idea to a dual-loop PLL, works as follows. The input $s(t)$ to the ADC as seen in Figure 2.1 is the data signal plus DC offset. However for the purpose of offset estimation, we note that the desired signal is the offset and that the data signal acts as a noise source. The ADC is designed to only respond to offsets greater than the minimum signal level, which results in an ADC with few bits of resolution [7]. This is sufficient since we are only trying to reduce the offset down to the minimum detectable signal level. The samples of the ADC, $x[n]$, as shown in Figure 4.1 are used to generate two estimates of the offset. The first estimate, called the "acquire" estimate is a wideband (short time constant) course estimate. The second estimate, called the

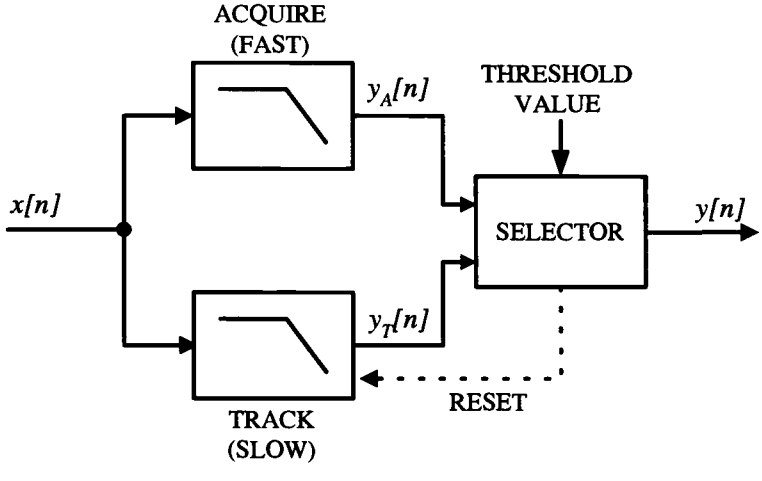

FIGURE 4.1: Block diagram of dual-loop filter.

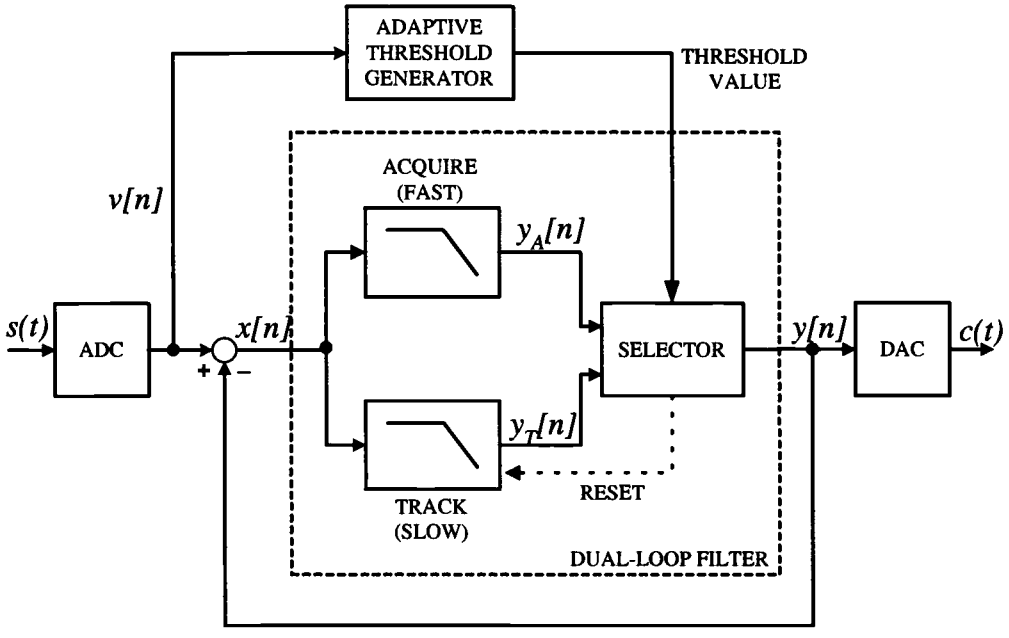

FIGURE 4.2: Block diagram of dual-loop DC detector.

"track" estimate, is a narrowband (long time constant) fine estimate. The algorithm works as follows, if the difference between these two estimates is reasonably close (to be quantified later) then the accurate track estimate is used as the offset estimate. However, when there is a jump change in the offset (someone touches the antenna or turns on a nearby device with a large amount of LO radiation, etc.) then the difference between the acquire and the track estimates will be quite large. If it exceeds a certain threshold level two things will happen. First, the selector switches the output of the dual-loop filter from track to acquire (fine to coarse). Second, the track estimator's data history is reset to the coarse estimator's data history to "trick" into thinking it has been tracking the new value all along. Thus, our system has excellent noise rejection, via the fine estimator, but can also react quickly to jump changes in the DC offset.

To implement our offset estimation scheme with a dual-loop filter a couple of things need to be added. Figure 4.2 shows the complete block diagram for the offset estimator including the ADC and DAC as shown in Figure 2.1. The adaptive threshold generator

produces the threshold value that tracks the desired signal level and sets the breakpoint for the tracking filter reset. This allow the dual-loop filter to be as sensitive to DC steps as possible without tracking the desired signal. A more detailed description of this problem together with a proposed circuit to build an adaptive threshold generator is described in the next Subsection. Following that is also a more specific description of the selector block.

Recall that once a jump change in offset is detected by the selector, the tracking filter has to be reset to the acquire filter output value. An analysis of how this can be done is presented in Subsection 4.3.. Using a feedback system to remove the offset in the mixer stage brings up the issue of stability. In Subsection 4.4. we describe the reason for having a unity gain feedback loop from the output $y[n]$ of the dual-loop filter to the input $x[n]$ and how this helps to improve the time response of the system without degrading stability. In Subsection 4.5. we discuss the choices for the filter coefficients of the tracking and acquire filter.

4.1. Adaptive Threshold

As mentioned above, the goal is to reduce static and time-varying offsets down to the level of the desired signal. This requires us to properly set the threshold value that triggers the track filter reset. Although we desire a small threshold, the threshold value has to be set such that the desired data signal by itself never causes the difference between the tracking and the acquire filter outputs to be larger than the threshold value. Otherwise the dual-loop algorithm will track the desired signal, constantly resetting the slow track filter to the value of the fast acquire filter. This has the same effect as using a simple LP filter with a bandwidth equal to that of the acquire filter to estimate the offset and results in unacceptable distortion of the desired signal since too much of the signal spectrum is removed. If on the other hand the threshold value is chosen to large, jump changes in offset are not detected which makes it impossible to continuously suppress the DC down to the signal level.

Since the desired signal level is not static but varies with receiver gain, distance to the transmitter and fading, the threshold value can not be set to a fixed value. Rather it has to track the desired signal value. A coarse signal level detector is therefore needed to constantly adjust the threshold value.

The fastest change in the signal level is due to fading and depends on the speed of the receiver relative to the transmitter and the carrier frequency band. For wireless outdoor systems the change rate can be up to several hundred Hertz [8]. For indoor systems or short distance communication systems like Bluetooth the change rate is on the order of several tens of Hertz.

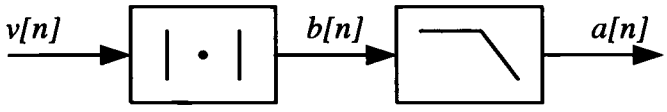

FIGURE 4.3: Adaptive threshold generator.

The adaptive threshold generator tracking the signal level is realized using a rectifier and a lowpass filter as shown in Figure 4.3. The sampled input signal $v[n]$ is rectified by removing the sign bit. Lowpass filtering the rectified signal results in a signal that tracks the input signal level. The bandwidth of the lowpass filter is given by the maximum expected fading rate. Figure 4.4 shows the signal level tracking output of the threshold generator given a Rayleigh-fading BPSK signal with a data rate of 200kbps and a fading rate of 20Hz.

The fading rate is calculated from the maximum Doppler shift f_d for a relative speed v of 10km/h and a carrier frequency f_c equals 2.4GHz. That is

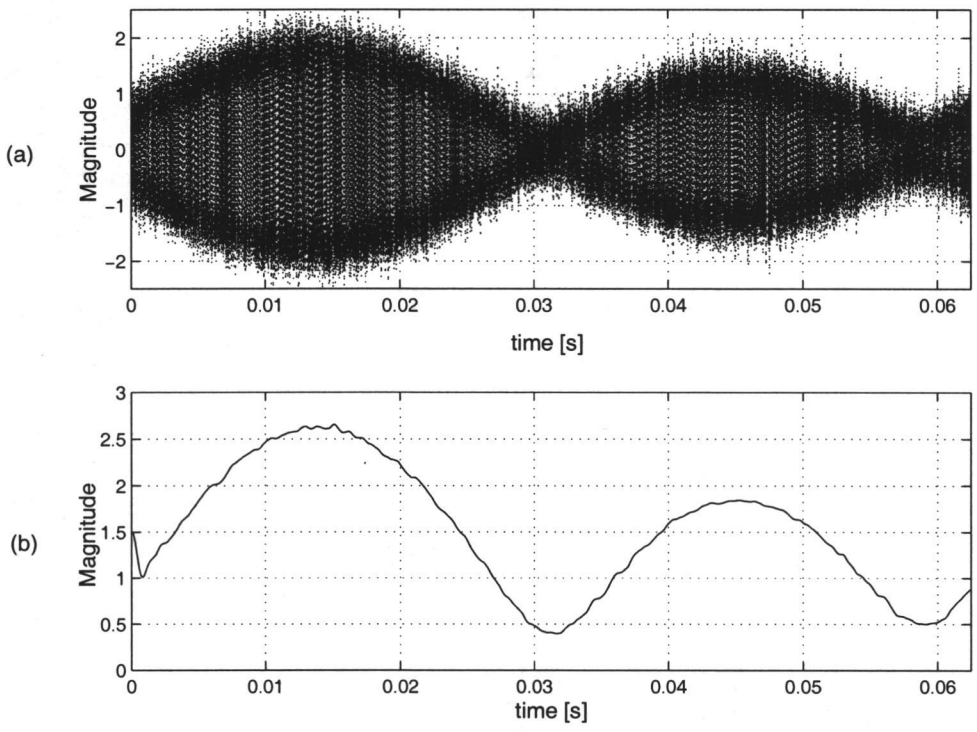

FIGURE 4.4: Adaptive threshold generator with (a) BPSK input signal s[n] and (b) level tracking output signal a[n]

$$f_d = \frac{v \cdot f_c}{c} \tag{4.1}$$

where c is the speed of light. For v equals 10km/h and a carrier frequency of 2.4GHz this results in a fading rate of 22Hz. The lowpass filter bandwidth is chosen to be around the fading rate. Using a 3rd order Butterworth filter results in a relatively sharp cutoff characteristic to suppress higher frequency content of the signal spectrum while keeping the group delay small enough to produce an accurate signal level tracking. The suppression of the higher frequency content is important, otherwise the threshold value starts tracking the instantaneous changes in the desired signal and consequently the dual-loop also removes parts of the desired signal rather than just the DC offset.

A problem occurs if a DC component is present at the input of the adaptive threshold generator since the DC component gets added to the threshold generator output. The output is therefore no more directly proportional to the desired signal level but includes

an offset. DC jump changes now have to be larger by the amount of this unwanted offset in order to cause a tracking filter reset. This slows down the acquire time for fast changing offset and therefore degrades the receiver performance.

Although this effect is undesired, the system will stay stable at all times. A remaining DC offset at the input causes the threshold level to increase. For a large offset the threshold value could therefore become large enough such that the difference between the the track and the acquire filter would never reach the threshold value. This effectively deactivates the reset mechanism of the dual-loop and the track filter is no more reset at DC jump changes. But the track filter is still actively removing the remaining DC and the threshold generator will therefore finally recover and produce an accurate signal level estimate. However, as long the dual-loop properly estimates the offset at baseband and removes it through the cancellation mixer, no DC is present at the adaptive threshold generator input.

4.2. Selector

In the previous Subsection we described how the signal level has to be tracked to produce an adaptive threshold value. The threshold value is now used in the selector to find out if a DC offset step has occurred. If the difference between the tracking and the acquire filter output is larger than our threshold value, we decide that a DC step has occurred and we therefore want to reset the tracking filter. An example for the selector circuitry is shown in Figure 4.5.

The difference of the two filter outputs $y_A[n]$ and $y_T[n]$ is compared to the threshold value by first subtracting $y_T[n]$ from $y_A[n]$. After that, rectification produces the unsigned filter output difference. This difference is then compared to the threshold value by another subtraction to generate the reset signal. The reset signal controls the track filter reset as well as a MUX between $y_A[n]$ and $y_T[n]$ as seen in Figure 4.5. The MUX is used to immediately switch the output of the DC detector to the newly acquired DC offset value during a reset. This speeds up the reaction time of the DC detector to

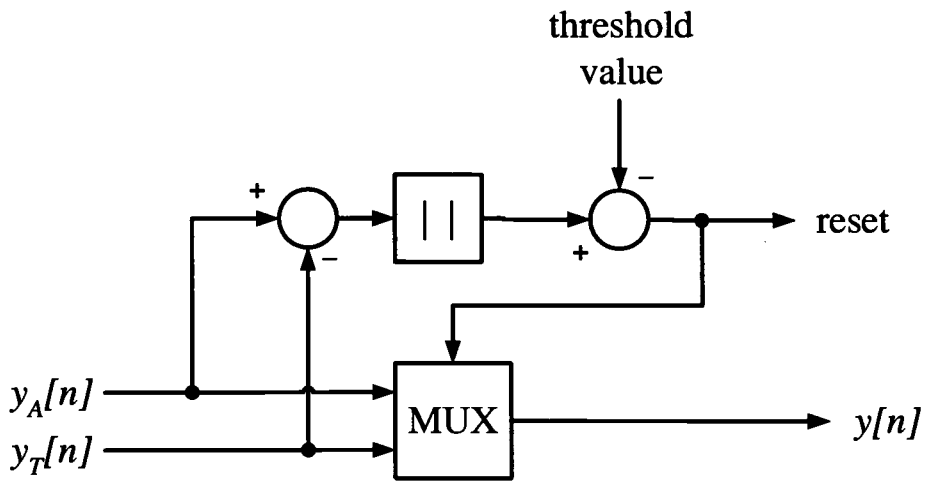

FIGURE 4.5: Selector block producing the reset signal

DC steps by one digital clock cycle. Depending on the clock rate of the circuitry this improvement might be negligible and instead of using a MUX, the output of the track filter $y_T[n]$ can be directly connected to $y[n]$.

As just mentioned the reset signal is mainly used to adjust the track filter to the new DC offset value. The reset signal is therefore routed from the selector block to the track filter as shown in Figure 4.2. How digital filters can be reset to any required value is described in the next Subsection.

4.3. Tracking Filter Reset

During rapid DC offset changes the track filter history has to be reset by the acquire filter data in order to quickly account for the new DC value as described previously. The following discussion shows how we can "trick" a given filter structure into thinking it has been tracking the new value all along.

Different digital filter realizations such as the cascaded form or direct form II [9] require different types of reset structures. The following analysis focuses on the transposed direct form II implementation of the tracking filter, although a parallel or cascaded form realization is generally much less sensitive to coefficient quantization and round-off

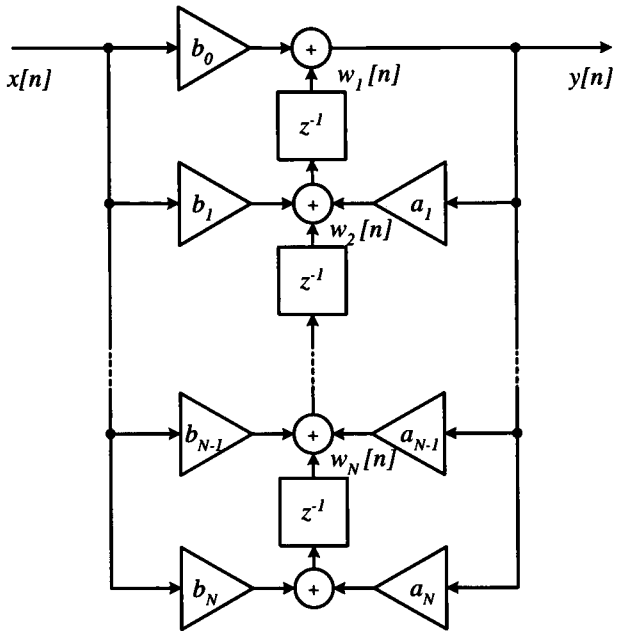

FIGURE 4.6: General flow graph for a transposed direct form II structure

noise due to a fixed-point implementation. The reason for showing the analysis for the transposed direct form II structure is its unique representation for a given difference equation. However, the derivation of the reset algorithm can easily be applied to other filter structures. Indeed the actual implementation of the fixed-point dual-loop filter is preferably done in the parallel form, especially if higher order filters.

Writing the linear constant-coefficient difference equation of the linear time-invariant track filter in the most general form, we have:

$$y_T[n] = \sum_{l=0}^{M} b_l x[n-l] \; + \sum_{k=1}^{N} a_k y_T[n-k] \tag{4.2}$$

Where $y_T[n]$ represents the track filter output at time n. Figure 4.6 shows the transposed direct form II structure for this difference equation when $M = N$.

Similar to the tracking filter equation we can write the linear constant-coefficient difference equation of the linear time-invariant acquire filter:

$$y_A[n] = \sum_{l=0}^{M} b_l x[n-l] + \sum_{k=1}^{N} a_k y_A[n-k] \tag{4.3}$$

As described above, the track filter history gets reset to the fast acquire filter data during a rapid offset change. This means that the output of the tracking filter $y_T[n]$ needs to be set to the acquire filter output $y_A[n]$. In addition, the filter states $w_1[n], w_2[n], \ldots, w_N[n]$ of the tracking filter from Figure 4.6 also need to be reset.

Recall that we want to "trick" the tracking filter into thinking that it has been tracking the new offset value all along. We therefore assume that the current input and all previous input values x are equal to the current acquire filter output.

$$x[n] = \ldots = x[n-N] = y_A[n] \tag{4.4}$$

If the tracking filter correctly estimates a constant offset, the output of the filter y_T is equal to the offset present at the input of the filter (assuming a filter gain of 1). The current output and all the previous outputs of the tracking filter can therefore also be assumed to be equal to the acquire filter output $y_A[n]$.

$$y_T[n] = \ldots = y_T[n-N] = x[n] = y_A[n] \tag{4.5}$$

From Figure 4.6 it can then be seen that the filter state $w_N[n]$ is given by:

$$\begin{aligned} w_N[n] &= b_N \cdot x[n-1] + a_N \cdot y_T[n-1] \\ &= b_N \cdot x[n] + a_N \cdot y_T[n] \end{aligned} \tag{4.6}$$

as $x[n-1] = x[n]$ and $y_T[n-1] = y_T[n]$ given by Equation 4.4 and 4.5. We can further simplify the expression.

$$\begin{aligned} w_N[n] &= b_N \cdot x[n] + a_N \cdot y_T[n] \\ &= y_A[n] \cdot (b_N + a_N) \end{aligned} \tag{4.7}$$

as $x[n] = y_T[n] = y_A[n]$. In the same fashion the state $w_{N-1}[n]$ is given by:

$$\begin{aligned} w_{N-1}[n] &= b_{N-1} \cdot x[n-1] + a_{N-1} \cdot y_T[n-1] + w_N[n-1] \\ w_{N-1}[n] &= b_{N-1} \cdot x[n] + a_{N-1} \cdot y_T[n] + w_N[n-1] \end{aligned} \tag{4.8}$$

However, $w_N[n-1]$ is equal to $w_N[n]$ since we assume $x[n-1] = x[n-2]$ and $y_T[n-1] = y_T[n-2]$ given by Equation 4.4 and 4.5. The state w_{N-1} can therefore be written as:

$$\begin{aligned} w_{N-1}[n] &= b_{N-1} \cdot x[n] + a_{N-1} \cdot y_T[n] + w_N[n] \\ &= b_{N-1} \cdot x[n] + a_{N-1} \cdot y_T[n] + y_A[n] \cdot (b_N + a_N) \\ &= y_A[n] \cdot (b_{N-1} + a_{N-1} + b_N + a_N) \end{aligned} \tag{4.9}$$

During a reset the state $w_i[n]$ of the track filter therefore is given by:

$$w_i[n] = y_A[n] \sum_{k=i}^{N} (a_k + b_k) \tag{4.10}$$

Once a jump change in offset is detected by the selector described above the dual-loop filter states are reset to the acquire filter data by simply multiplying the present acquire filter output by the constants given from Equation 4.10. This shows that the track and acquire filter can have a completely different filter order and even filter structure as the successful reset of the track filter only depends on the acquire filter output at the time of the reset.

Figure 4.7 shows an example of a dual-loop implementation with a second order track filter and a first order acquire filter realized in a transposed direct form II. k_1 and k_2 represent the multiplier values used to reset the track filter states during the reset and are given by Equation 4.10.

In connection with the reset mechanism described here, the direct form I has an interesting property. Instead of using a multiplication factor to define the filter states during the reset, all the states of a direct form I filter can be directly set to the acquire

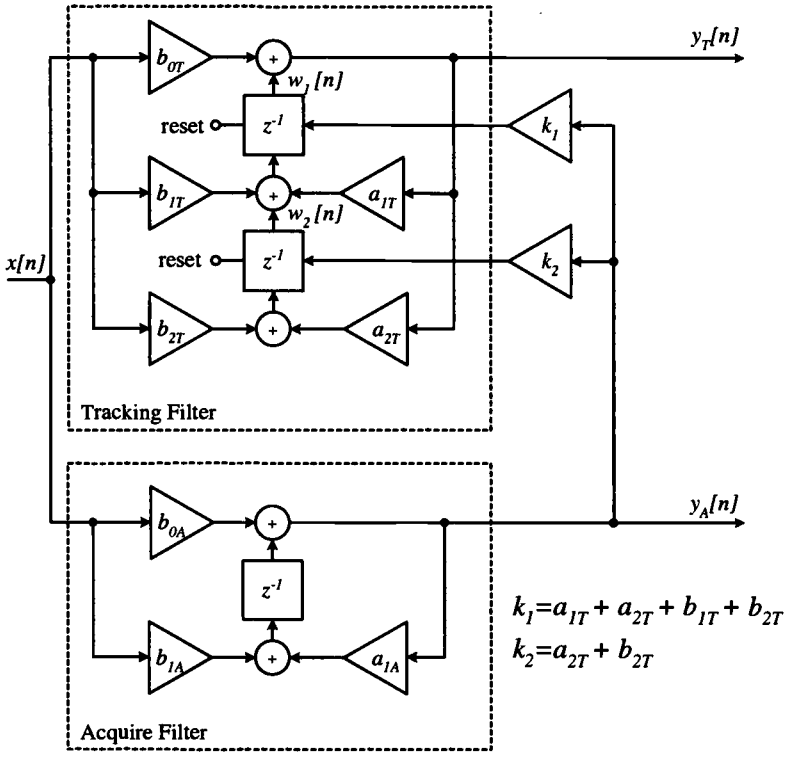

FIGURE 4.7: Dual loop implementation with a 2nd order track filter in transposed direct form II and a 1st order acquire filter

filter output value as seen in Figure 4.8. This is possible because the filter states at the input always carry the value of the last M inputs, no scaling is applied. The same is true for the states at the output. They carry the last N output and can therefore be reset by setting them to the acquire filter value. The direct form I can therefore provide a very simple realization of the reset mechanism at the cost of additional registers given by the direct form I realization and inaccuracy due to round-off noise as well as coefficient quantization. But for low filter orders this represents a viable solution.

As an example of the power of resetting the filter states we consider the response of a resettable lowpass filter versus a fixed filter, both having the same filter coefficients. A partially constant DC is applied to the input as seen in Figure 4.9. The input DC changes from 0 to 10 at t=50ms, from 10 to 2 at t=150ms and from 2 back to 0 at t=200ms.

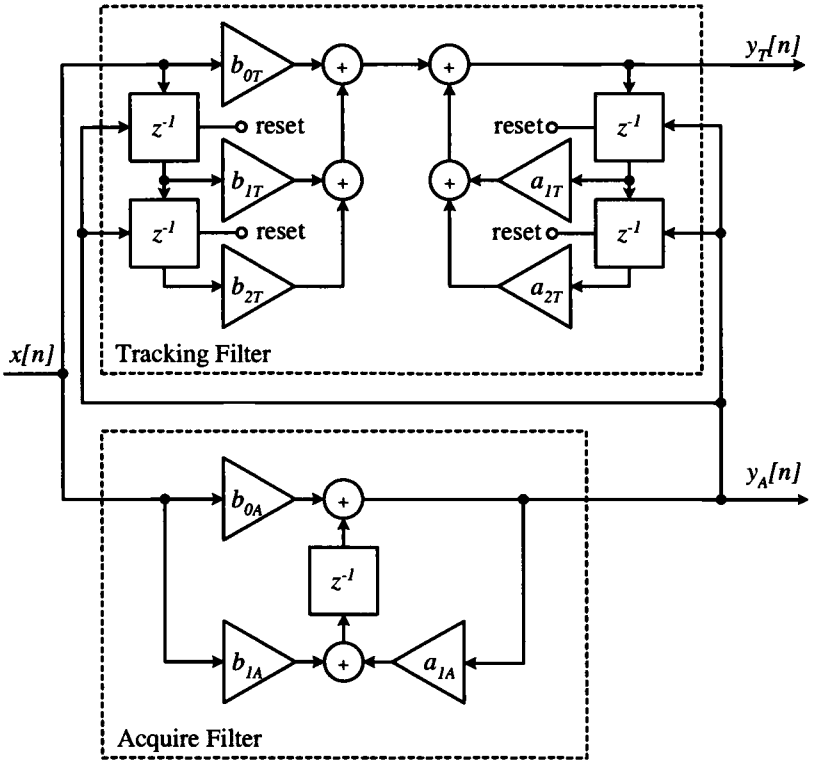

FIGURE 4.8: Dual loop implementation with a 2nd order track filter in direct form I and a 1st order acquire filter

The dashed line shows the lowpass filter output of a regular 3rd order Butterworth filter with a bandwidth of 20Hz . If the same filter realized in a transposed direct form II is reset to the given offset values at t=50ms, 150ms and 200ms using the reset mechanism described above, the filter output perfectly tracks the input DC. No settling is observed. We can therefore successfully set the lowpass filter to every desirable level within one clock cycle. In reality we do of course not know the exact offset value the filter has to be reset to and some settling will be observed. But as described above the fast acquire filter provides a relatively good estimate of the new DC offset and by resetting the filter, the settling time can be drastically reduced.

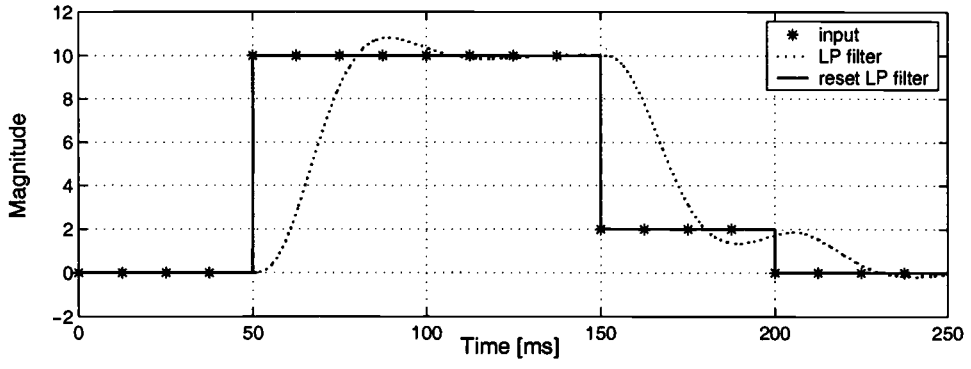

FIGURE 4.9: Lowpass filter output of a regular filter versus a reset filter

4.4. Loop stability

The dual-loop's function is to detect the DC offset at the output of the mixer. To be able to remove the offset at the mixer, we need to feed the detected DC back into the cancellation mixer. This results in a classical negative feedback loop whose stability can be determined by gain and phase margin. The nonlinearity of the feedback loop due to the reset mechanism of the dual-loop filter can be simplified by representing the loop as a time-variant linear system. As long as no reset occurs, the open loop transfer function is simply given by the slow track filter. During a track filter reset the acquire filter is switched into the feedback loop for one clock cycle. The open loop transfer function having the acquire filter in the feedback path therefore also has to meet the stability criteria.

For the moment we will focus on the case when the track filter is in the feedback loop. For the DC cancellation loop to work, we need to add an integrator at the output of the track filter as the offset detected by the dual-loop algorithm represents the residual DC that needs to be removed in addition to the present correction value $c(t)$ as seen in Figure 4.10. This additional integrator causes the open loop transfer function to have at least two poles, one at DC given by the integrator and one or more poles from the track filter. If we want to achieve a phase margin of 45 degrees having an open loop transfer

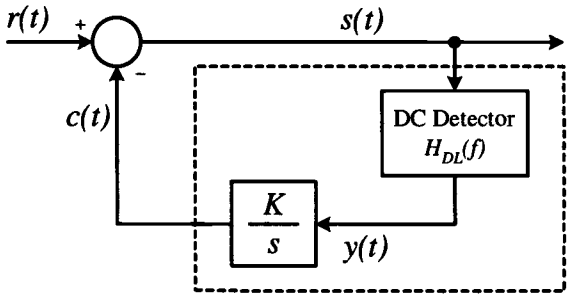

FIGURE 4.10: Simplified closed loop realization of dual-loop filter with integrator

function given by an integrator and a 1st order lowpass filter, the unity gain frequency is given by the first pole of the track filter. As will be described in Subsection 4.5., the bandwidth of the track filter is relatively narrow to avoid BER degradation. The unity gain bandwidth of the close loop system is therefore very small compared to the change rate of the offset.

S-domain simulations based on the model shown in Figure 4.10 (with a K factor of 1800 and a DC detector given by a first order Butterworth lowpass filter with a bandwidth of 200Hz and a gain of 1, resulting in -45 degree phase margin) show that it takes approximately 7.5ms for the loop to settle within 1% in response to a input step as shown in Figure 4.11. Making the filter bandwidth narrower to improve the phase margin would result in an even longer settling time. A typical power-up time for a transmitter is around 5μs. However, having a settling time in the range of 7 milliseconds would make it impossible for the dual-loop to detect and correct jump changes in DC offset caused by the power-up of transmitters. We therefore have to find another solution to implement the closed loop than using an additional integrator.

The reason we introduced an integrator was to have a latch storing the DC correction value. This was necessary because the dual-loop filters only detect the offset present at the mixer output, but are not able to account for the DC correction value already applied at the cancellation mixer. This means that the dual-loop filter produces a relative DC correction value rather than a fixed offset estimate needed in the cancellation

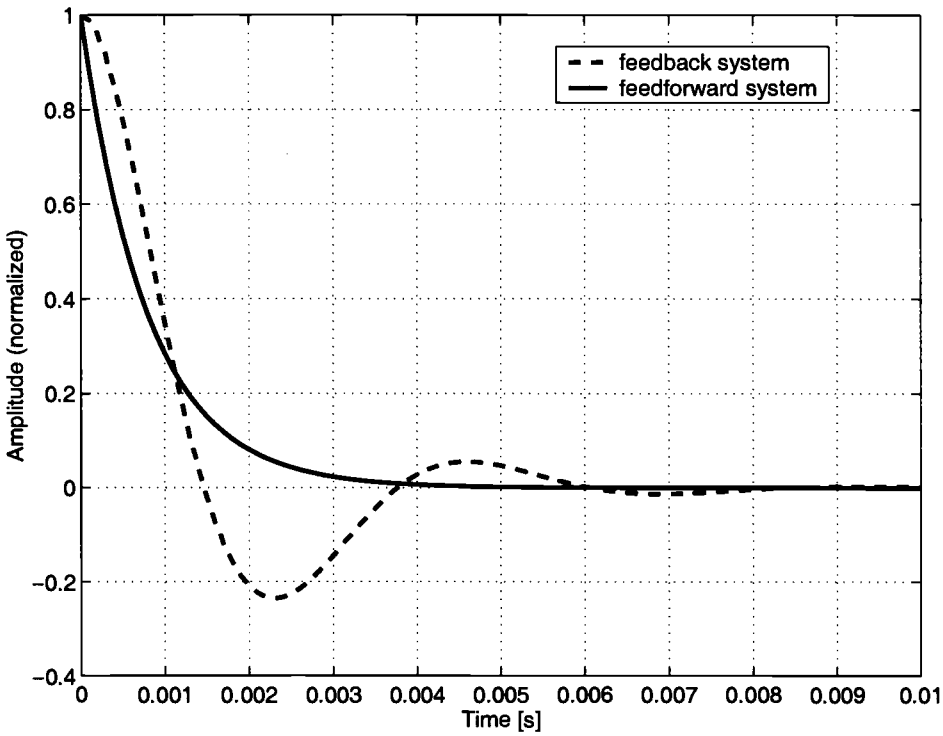

FIGURE 4.11: Step response of feedback and feedforward loop

mixer to null out the offset. The integrator can be dropped if we find a way where the dual-loop filter produces an absolute DC correction value instead of a relative one.

Figure 4.12 shows a way to achieve this. As we know what DC correction value is fed into the cancellation mixer, we can simply compensate for this value at the input of the dual-loop filter. To the dual-loop filter the mixer output now appears as if no DC correction would be applied. This can be seen from the following simple equation:

$$\begin{aligned} x(t) &= s(t) + c(t) \\ &= r(t) - c(t) + c(t) \\ &= r(t) \end{aligned} \tag{4.11}$$

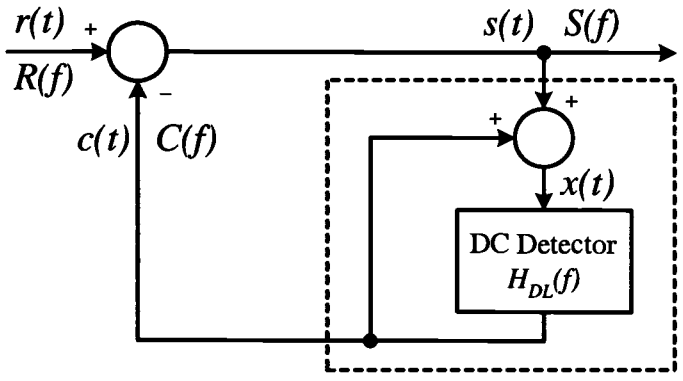

FIGURE 4.12: Simplified closed loop realization of dual-loop filter with offset compensator

The dual-loop DC detector therefore produces a DC correction value that can be directly applied to the cancellation mixer as the output represents the absolute DC offset value that would be seen in the baseband without having any offset correction. The frequency response $H_{TOT}(f)$ of the overall loop can then be expressed in terms of the dual-loop filter response $H_{DL}(f)$. Calculating first the frequency response $H_{FB}(f)$ of the feedback path,

$$\begin{aligned} H_{FB}(f) &= \frac{C(f)}{S(f)} \\ &= \frac{H_{DL}(f)}{1 - H_{DL}(f)} \end{aligned} \tag{4.12}$$

the overall frequency response is given by:

$$\begin{aligned} H_{TOT}(f) &= \frac{S(f)}{R(f)} \\ &= \frac{1}{1 + H_{FB}(f)} \\ &= 1 - H_{DL}(f) \end{aligned} \tag{4.13}$$

Adding the DC correction value to the baseband signal in front of the dual-loop filter therefore results in a overall system equivalent to the feedforward system shown in

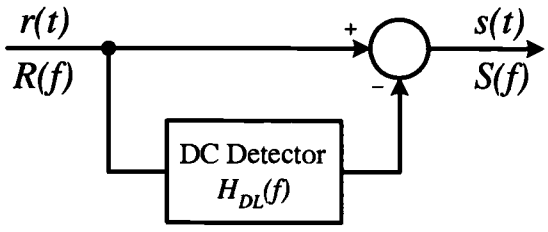

FIGURE 4.13: Feedforward system equivalent to offset compensated feedback system

Figure 4.13. This system has the advantage that it is always stable as there is virtually no feedback path. The dual loop transfer function no more affects the stability and settling time of the feedback loop. In reality the DC correction signal $c(t)$ experiences of course some non-unity gain and DC-shift due to circuit mismatch and other nonlinearities. However, this effects can be canceled out by calibrating the loop. The step response of the system in Figure 4.12 is shown in Figure 4.11. The settling time is reduced from 7.5ms given by a traditional feedback loop to 3.7ms and the phase margin is no more of concern. The settling time can be arbitrarily reduced by increasing the filter bandwidth of the notch filter and is only limited by the BER degradation due to removing an increased part of the signal spectrum. But in contrast to the feedback loop the stability of the system is not compromised.

Using the virtual feedforward structure as just described, the stability of the system having the acquire filter in the feedback path is also guaranteed since the stability of the system is not degraded by increasing the filter bandwidth. We can therefore skip the stability analysis for the acquire filter.

4.5. Dual-loop filter parameters

There are several tradeoff for choosing the filter parameters of the acquire and the track filter. First lets take a look at the track filter. The task of the filter is to track static offset. Depending on the filter bandwidth the track filter will also detect and

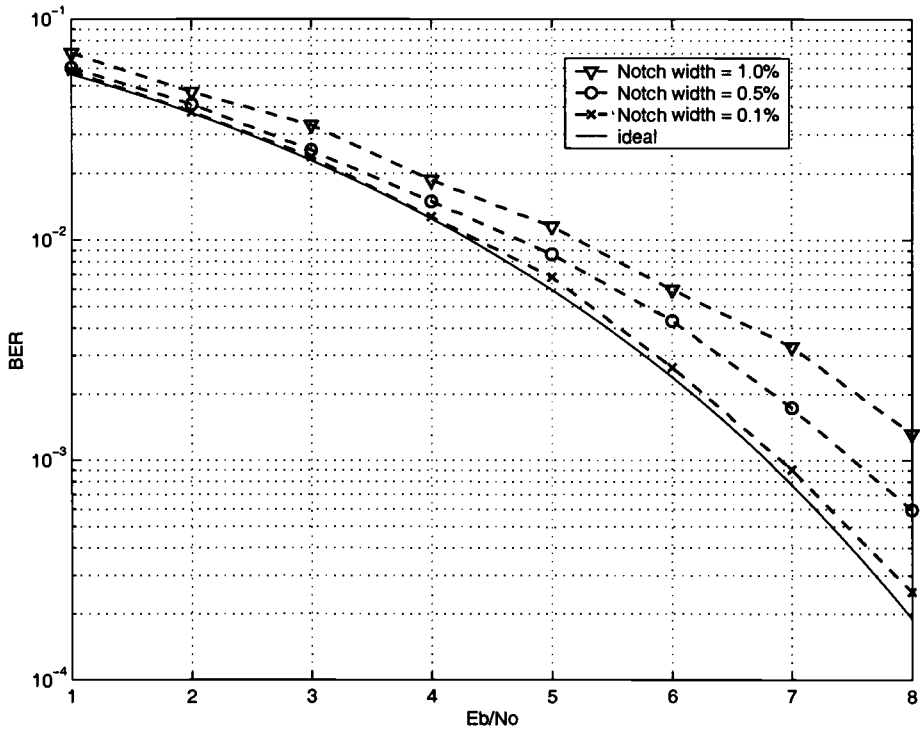

FIGURE 4.14: BER performance of a BPSK signal for different DC-notch bandwidth

remove part of the time-varying offset. But the filter type, order and bandwidth has to be chosen such that the BER performance of the system only degrades minimally if no offset is present and only the track filter is active. Figure 4.14 shows the degradation in BER performance for different lowpass notch bandwidths. The simulations are done using a BPSK signal pulse shaped by a RRC filter ($\alpha = 0.5$). The notching of the low frequency content is done using a first order LP filter in the feedforward system as shown in Figure 4.13. From the BER plot it can be seen that the 3dB-bandwidth of the track filter has to be less than 0.1% of the signal bandwidth to have minimal impact on the BER performance. This value was already reported in [1].

Depending on the expected fading rate of the DC offset, the track filter can also remove part of the time-varying DC given by Rayleigh fading. For a signal rate of 200kbps the 0.1% bandwidth to produce a negligible BER degradation would be 200Hz.

With a DC of up to 20dB larger than our desired signal we need a high-pass filter with 20dB rejection at our given fading rate to suppress the DC down to the signal level. Having a first order LP filter with a 3dB-bandwidth of 200Hz in the feedback path of a negative feedback system can therefore only sufficiently suppress fading offset up to around 22Hz (due to the 20dB/dec slope of the DC notch). DC offset that varies at a faster rate than 22Hz has to be removed by the dual-loop mechanism.

From a standpoint of response time to rapid offset cahnges, the acquire filter bandwidth should be in the order of the expected offset change rate. However this makes the acquire filter more sensitive to noise and produces large overshoots during tracking filter resets. The value for the acquire filter bandwidth therefore is a trade-off between the speed to detect rapid offset changes and the accuracy to predict and remove the new offset value. The filter parameters have to be optimized for a specific modulation scheme and signal bandwidth.

5. SIMULATION RESULTS

We have simulated the dual-loop algorithm using Matlab and Simulink. Putting all the blocks described in the previous Section together we get a system $H_{FB}(f)$ as shown in Figure 4.2. The signal $s(t)$ represents the output of the cancellation mixer and the dual-loop output signal $c(t)$ is fed into the mixer as shown in Figure 2.1.

The 3dB bandwidth of the adaptive threshold generator is set to 200Hz. The dual-loop filter is realized in transposed direct form II with the tracking filter being resettable as shown in Figure 4.7. The acquire filter is a first-order lowpass filter with a 3dB bandwidth of 40kHz. The track filter is realized as a first-order lowpass filter with a 3dB bandwidth of 200Hz. The difference of the two filter outputs is compared to the threshold value in the selector block as shown in Figure 4.5.

Figure 5.2 shows the performance of the dual-loop algorithm due to variable DC steps. A BPSK signal pulse-shaped with a root-raised cosine filter ($\alpha = 0.5$) and a bitrate of 200kbps was applied to the feedback system as shown in Figure 5.1. In addition a variable DC step was added to the input signal to produce a test vector as shown in Figure 5.3. After removing the offset using the dual-loop estimator or a LP filter we are left with narrow DC spikes due to the finite reaction time of the estimators to

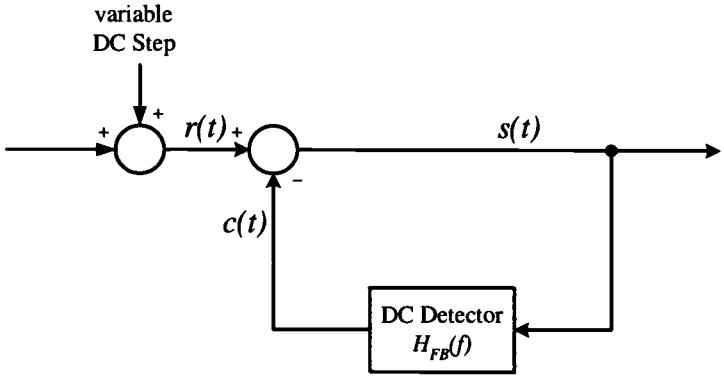

FIGURE 5.1: Simulation setup for DC cancellation loop

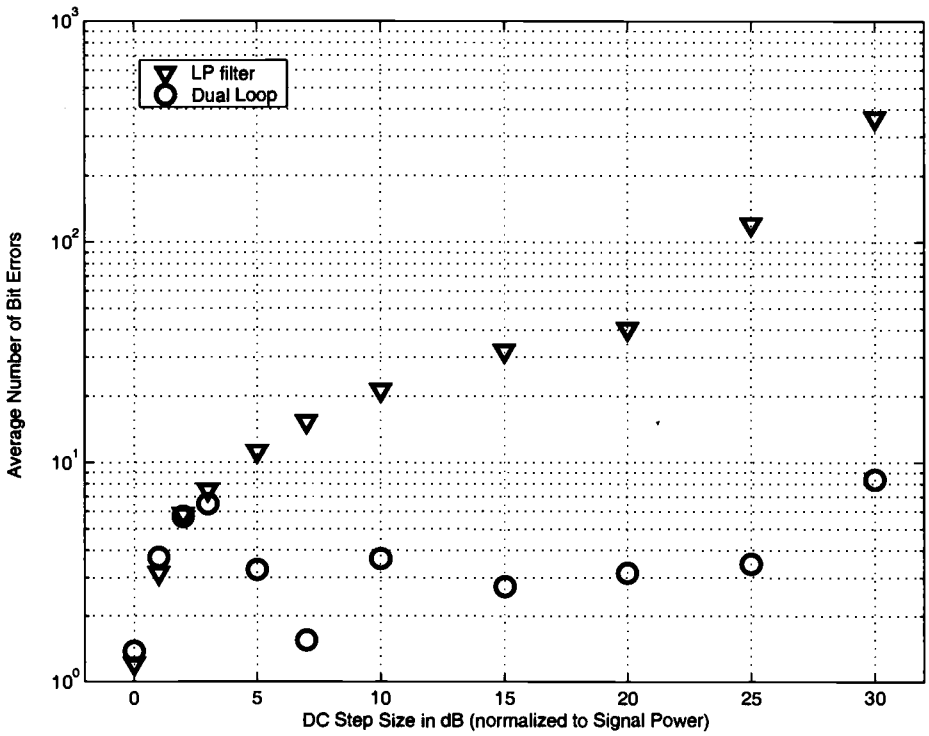

FIGURE 5.2: Average number of errors during a DC jump change

rapid offset changes as shown in Figure 5.4. The duration of this spikes determines the performance of the offset cancellation scheme. As longer it takes to detect and track out the offset during rapid transitions as more symbols are corrupted. The graph in Figure 5.2 shows the average number of bit errors over 1000 runs that occur until the dual-loop can detetect and track out a DC step of varying magnitude. For comparison the performance of a DC detector realized with a simple LP filter is shown. For a static DC offset both detectors would produce the same BER, but during DC jump changes the LP filter causes long burst of bit errors where the dual-loop detector produces less than 7 bit errors for jump changes up to 25dB above the signal power. Up to a DC step size of around 3dB the dual-loop curve closely follows the LP filter curve. This is because for small DC steps the difference between the tracking and the acquire filter output does not exceed the threshold value. Therefore no tracking filter reset occurs and

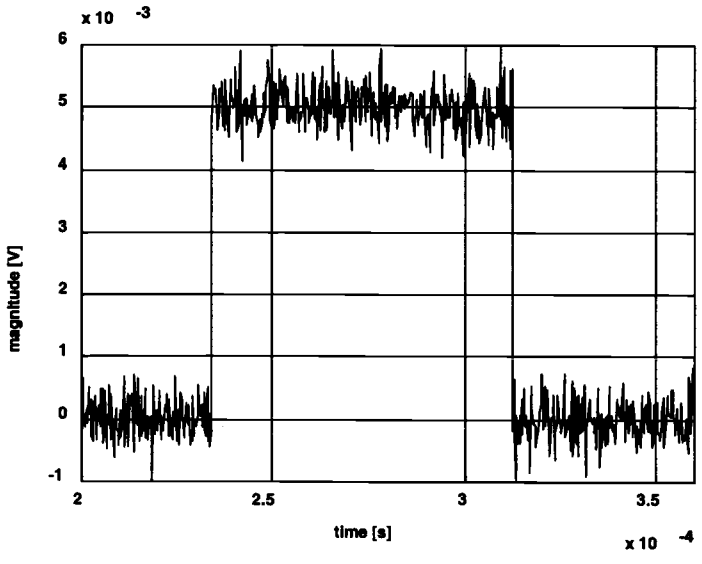

FIGURE 5.3: Input test vector for simulation

the dual-loop behaves exactly in the same manner as the simple LP filter. Once the DC step size becomes larger than 3dB the reset mechanism of the dual-loop starts to come into effect and the average number of errors during one DC steps dramatically improves compared to a simple LP filter.

To produce a more commonly used BER curve, the performance of the dual-loop filter having DC offset jump changes was measured in the presence of noise. In this simulation the offset at the output of the mixer is modeled as a DC that experiences variable jump changes every 50ms, implying an average of 20 rapid offset changes per second. The offset value is uniformly distributed between ± 25 times the desired signal power, representing DC that can be up to 28dB above the signal power. Jump changes in the offset occur with a finite transition time of 5μs, which reflects a typical warm-up time of a adjacent transceiver and this is assumed to cause the most rapid offset change. The desired BPSK input signal is again pulse-shaped with a root-raised cosine filter (α=0.5) and has a bitrate of 200kbps. We test the performance of a dual-loop filter having the exact same filter parameters as in the previous simulation.

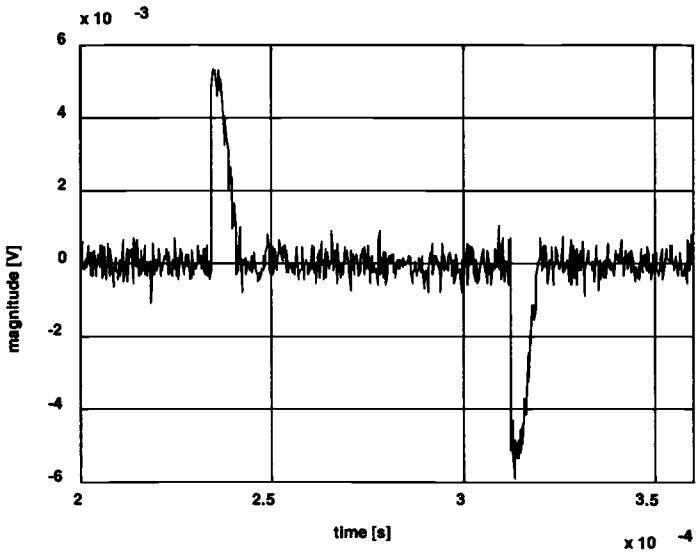

FIGURE 5.4: Output signal after offset correction

The desired signal plus noise with the superimposed DC offset is fed into the dual-loop filter as shown in Figure 5.1. From Figure 5.5 it can be seen that there is practically no degradation in BER at 10^{-2}, while at $2 \cdot 10^{-3}$ the BER is degraded by less than 1dB. The convergence of the curve to around 10^{-3} is due to the number of bit errors that occur during any rapid change in offset even in the absence of noise. Having 20 rapid offset changes per second and a bitrate of 200kbps we can see that the dual-loop approach compensates jump changes in offset within less than 10 bit periods which results in a BER floor below 10^{-3}. This corresponds to the performance seen in Figure 5.2 where the average number of bit errors during a DC jump change stayed below seven.

Applying a constant DC offset to the input, the BER closely follows the ideal BER curve. The small degradation is only due to the notched out signal spectrum at DC as seen in Figure 4.14. The dual-loop filter adds no additional degradation when compared to simple DC notching.

Comparing our results from the dual-loop having rapid DC offset changes with the performance given by a LP filter in the feedback path (simple DC notching) shows that

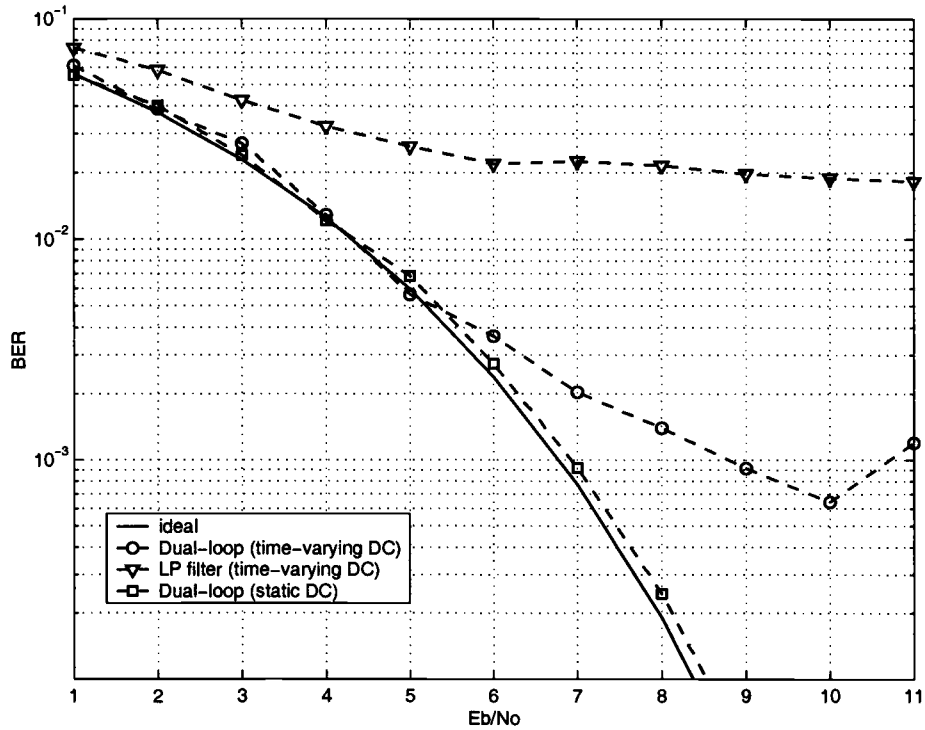

FIGURE 5.5: BER performance for time-varying offset given by 20 rapid DC offset changes per second.

highpass filtering the mixer output signal provides an unacceptable BER performance due to the time-varying character of the offset as predicted in Section I. The BER flattens out at around $2 \cdot 10^{-2}$. This implies that an average of around 200 bit errors occur during a DC jump change versus only around 10 bit errors for the dual-loop approach.

6. CONCLUSION

The simulation results show that the proposed dual-loop approach is well suited to detect and remove rapid changes in DC offset at the output of a direct conversion mixer. Compared to conventional DC notching the dual-loop is more than 20 times faster in tracking out fast changing DC offset of up to 25dB above the desired signal power level. With an average of less than 7 bit errors during a DC jump change the presented approach avoids long bursts of bit errors as experienced with conventional DC notching. This should allows us to use our method in combination with interleaving and convolutional channel coding to improve the BER performance even further.

The dual-loop approach therefore provides a mean to remove fast varying DC offset and can help to overcome one of the main obstacles in building direct conversion receivers in CMOS technology.

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