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Title: Electrical Characterization and Circuit Modeling of Interconnections and Packages for High Speed Circuits By Time Domain Measurements

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Vijai K. Tripathi

With edge rates of high speed digital devices pushing into the sub–nano second range, interconnections with the associated packages play a major role in determining the speed, size and performance of digital circuits and systems. The purpose of this study is to develop experimental techniques based on time domain peeling algorithms (dynamic deconvolution) for accurate electrical characterization and circuit modeling of general interconnection structures.

This thesis describes the basic principles and computational procedure of these time domain peeling algorithms, accompanied by many illustrations and examples of practical interconnection structures in high speed electronic packages. These include general single (isolated) interconnections with nonuniform cross section, general uniformly/nonuniformly coupled interconnection structures with discontinuities, power/ground systems with the associated parallel plane structures, resistive lossy interconnections in thin film single and multi–chip modules, and multilayer high–pin–count packages. It is shown that the distributed circuit models consisting of cascaded transmission line sections lead to an accurate evaluation of the time domain

response of high speed interconnection structures. These distributed models are synthesized from the time domain reflection and transmission (TDR/T) measurements, and the impedance profiles of the distributed model are extracted by using scattering matrix–based peeling algorithms.

By direct time domain integration or frequency domain optimization, the distributed circuit model can also be used to construct the lumped element circuit model as well as the proposed hybrid element model consisting of transmission lines and lumped elements. The hybrid model is intended to combine the efficiency of the lumped element model with the accuracy of the distributed circuit model leading to efficient accurate simulation of circuits in general CAD tools. The accuracy of these circuit models is also confirmed by comparing the simulated data with the measured data for the test fixtures on printed circuit boards (PCBs) and chip–to–chip level interconnections. The techniques developed in this thesis can help to assure the signal fidelity of high speed circuits in the early design stage by incorporating interconnect models into integrated circuit design and simulation.

Electrical Characterization and Circuit Modeling of Interconnections and Packages for High Speed Circuits By Time Domain Measurements

by

Jyh–Ming Jong

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TABLE OF CONTENTS

TABLE OF CONTENTS , continued

LIST OF FIGURES

LIST OF FIGURES , continued

LIST OF FIGURES , continued

LIST OF FIGURES , continued

LIST OF FIGURES , continued

LIST OF TABLES

ELECTRICAL CHARACTERIZATION AND CIRCUIT MODELING OF INTERCONNECTIONS AND PACKAGES FOR HIGH SPEED CIRCUITS BY TIME DOMAIN MEASUREMENTS

1. INTRODUCTION

With the advancements in high performance computers, the speed associated with the digital circuit families is increasing at a phenomenal rate. Figure 1.1 shows a survey of digital electronic development over the last two decades indicating that many high speed circuits are now available.

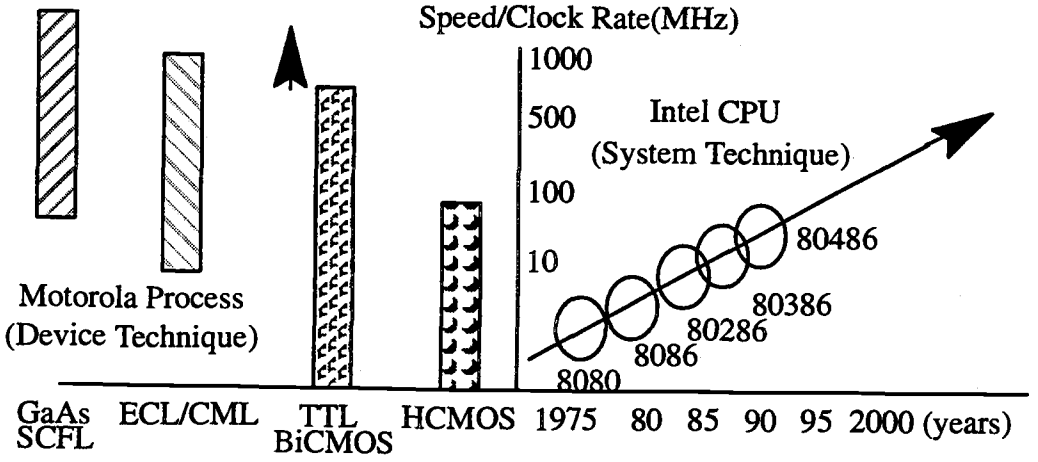


Figure 1.1, The trend of digital electronic development for the last two decades.

Since semi–conductor device process techniques have made remarkable advances, the packaging density and gate delay of integrated circuits have improved continuously. With edge rates of digital devices pushing into the nano–second range and clock rates of digital systems trending toward the GHz region, interconnections and packages play an important role that determines the speed and size of integrated circuits, the number of I/O in the packaged circuits as well as the ratio of signal and power/ground pins. Because of the high frequency harmonics of digital switching signal, many interconnection structures can no longer be treated as "short circuit" or "wire", since they may even behave as "transmission line". As we continue speeding up clock rates of the system, and number of transistors increase in a chip, to understand

the electrical characteristics of interconnection structures becomes a necessity in designing high speed/performance systems.

Interconnection structures have become the dominant factor that limit the performance of high speed circuits and systems due to interconnect parasitic effects which lead to degradation in system performance.[1–9,13–36,39–54,57–60] Figure 1.2 shows a typical digital circuit with the associated uniform low loss or lossless interconnection structure. A primary concern is that the propagation delay of interconnections becomes a large fraction of the system clock cycle time. In addition to interconnect parasitic effects, the transmission line behavior of interconnects becomes a major contributor to the signal degradation. Therefore, the transportation of high speed signal which involves getting data off the chip and transmitting data between the chips, is very much dependent on the electrical characteristics of interconnection structures as edge rates and gate delay of integrated circuits decrease. However, in order to ensure the signal integrity and guarantee the system functions that operate correctly at higher clock rates, accurate characterization and circuit modeling of interconnection structures are necessary for designers to incorporate interconnect effects during the design and simulation phase for high speed circuits and systems.

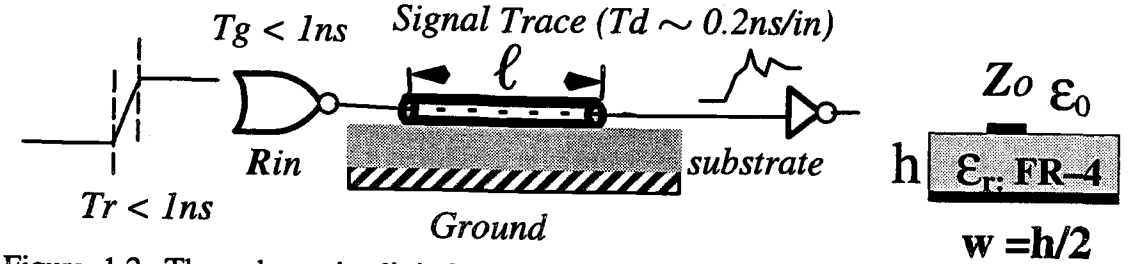


Figure 1.2, The schematic digital circuits with the associated interconnection structure.

A variety of interconnection structures are being used to package high speed circuits. Considering a microstrip line structure shown in Figure 1.2 having an electrically short length ℓ, the interconnection structure can be characterized by the lumped element model as shown in Figure 1.3 where an inductive element, a capaci-

tive element and LC element model can be used to describe the electrical characteristic of the structure in different conditions [5,21,22,57].

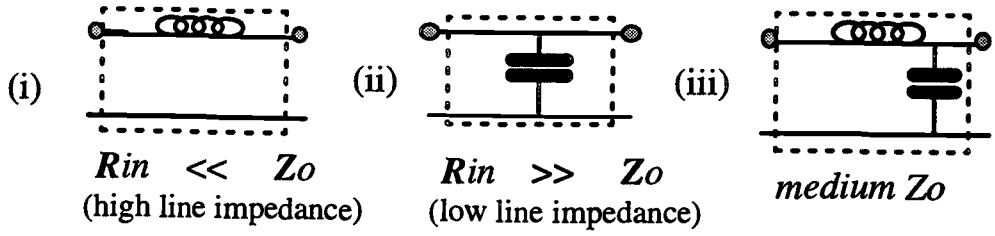


Figure1.3, The lumped element model for an electrically short interconnect.

For an electrically long interconnect, the structure in Figure 1.2 is then modeled by a transmission line where the model can be characterized in terms of the characteristic impedance and propagation delay from the measured time domain response as shown in Figure 1.4 [19,78].

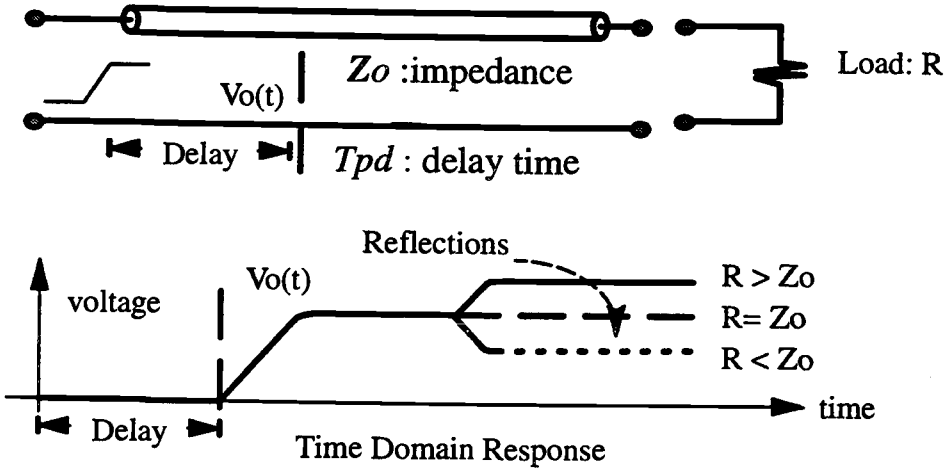


Figure 1.4, The transmission line model for an electrically long interconnect.

In practical electronic packages, most of interconnection structures are nonuniform interconnects, i.e, the cross section of conductor is not uniform along the signal transmission path as shown in Figure 1.5, such that discontinuities in line impedance result in multiple reflections leading to the reduction of noise immunity in high speed

circuits. In general, the nonuniform interconnect behaves as a nonuniform transmission line which can be characterized in terms of the nonuniform impedance profile and the propagation delay from the measured time domain response. In addition to nonuniform interconnects, multiconductor structures, resistive lossy interconnection structures and power/ground interconnect distribution systems are also playing a major role in determining the interconnect performance.

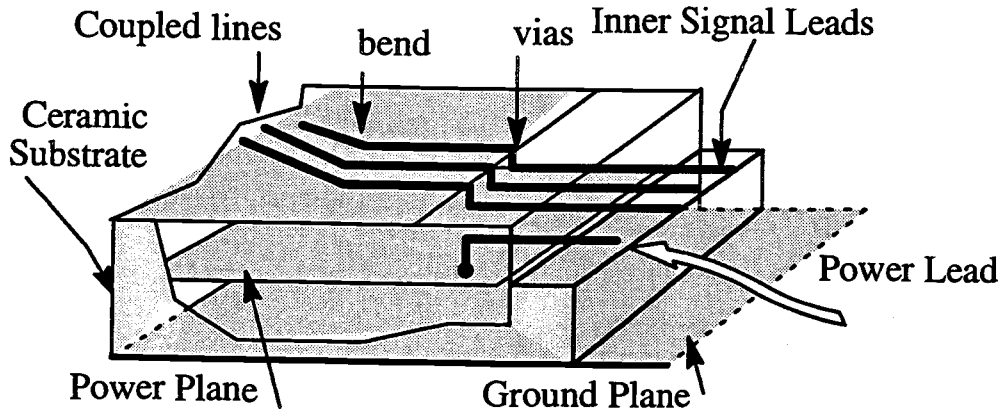


Figure 1.5, Interconnection structures in a practical electronic package.

When implementing a high performance system using high speed circuit families, several noise sources associated with interconnect parasitic effects must be considered and examined in order to assure acceptable system performance. These are described below:

Reflection

The fast edge rate digital signal transmitting through interconnection structures can result in ringing, e.g, undershoot and overshoot. Ringing is a result of reflections due to the discontinuities in line impedance, such as uniform/nonuniform interconnects with bends, steps and vias, and the impedance mismatch between the line impedance and the I/O impedance of integrated circuits. If the undershoot and overshoot voltage is larger than the noise margin of the circuit such that the designated signal level goes back through the threshold region of a receiving device, then false switching can occur on the receiving device output. In general, the nonuniform

transmission line model as shown in Figure 1.6 can be used as a vehicle to take into account multiple reflections due to nonuniform interconnection structures.

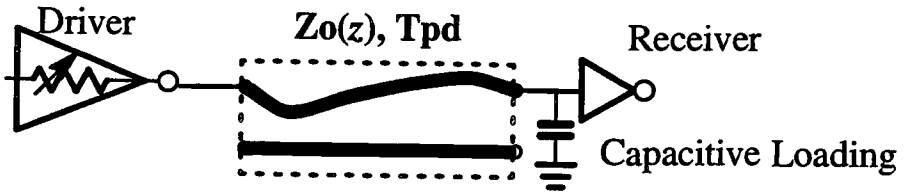


Figure 1.6, Digital circuits with the associated nonuniform transmission line for multiple reflection simulation.

Crosstalk (Coupled Noise)

Another noise source of signal transmission problems in high speed circuits is electromagnetic interference between multiple coupled interconnection structures. Consider two nonuniformly coupled transmission lines as shown in Figure 1.7, the high speed signal traveling on the active line will induce coupled noise to the quiet line due to mutual capacitances and inductances between adjacent lines. In general, the near–end noise and the far–end noise are used as a measure of the coupling effects between coupled lines. The amplitude of coupled noise is not only proportional to edge rates of the digital waveforms, but also dependent on the physical dimensions of the coupled interconnection structures, such as spacing between the lines and the length of parallel lines. To predict crosstalk, a simulation model must include these coupling effects.

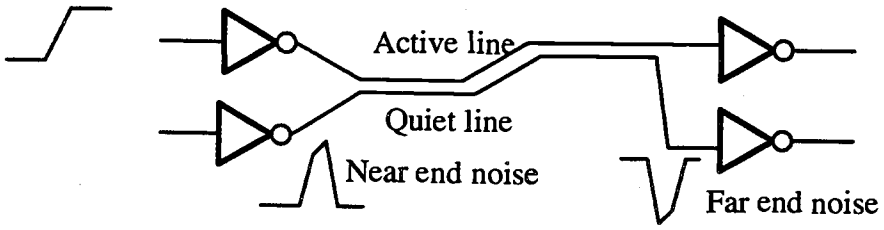


Figure 1.7, The schematic coupled interconnection structures in high speed circuits.

Switching Noise (Power/Ground Bounce, Delta–I Noise)

While a high speed circuits is switching from one logic level to another, the

noise caused by transient currents flowing into the non–ideal power/ground systems of electronic packages is known as switching noise as shown in Figure 1.8. Switching noise, also known as power/ground bounce and Delta–I noise, can lead to the reference voltage shift and the reduction of noise margin. Because of the interconnect parasitic effects inherent in the non–ideal power/ground distribution systems and the high speed circuits simultaneously switching, switching noise has been recognized as a significant factor that limits the performance of high speed circuits in high density packages such as multichip modules (MCMs). The most effective way to examine this problem is to provide a circuit model of the power/ground system for integrated circuit design and simulation such that design trade–off can be made to maintain system performance.

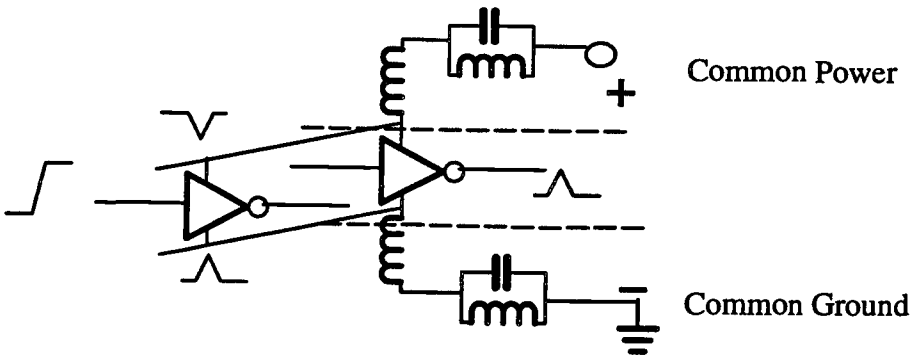


Figure 1.8, The circuit mode including the non–ideal power/ground model.

Voltage Drop And Attenuation:

Voltage drop and attenuation often occurs not only on the on–chip interconnects, but also on the off–chip level interconnects and packages. As integrated circuit packaging technologies evolve toward higher integration and smaller physical structures such as thin–film and MCM packages, the need for small dimensional interconnections also increases. The reduction of interconnect cross sections leads to an increase in line resistance, and hence high resistive line associated with nonuniform interconnection structure as shown in Figure 1.9 results in signal distortion and DC voltage drop in high speed circuits.

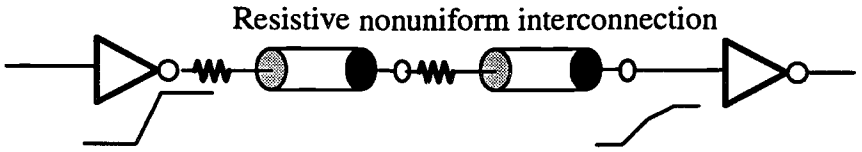


Figure 1.9, Resistive lossy interconnection in high speed circuits.

Accurate time domain simulation of high speed monolithic and hybrid integrated circuits must include the interconnects within the circuits and the associated packages. These simulations incorporating all the delay, distortion, DC voltage drop and attenuation, crosstalk and power/ground switching noise associated with interconnects and discontinuities can be facilitated by accurate equivalent circuit models for these passive elements. In general, there are two techniques for obtaining equivalent circuit models of high speed interconnects: the electromagnetic computational technique based on quasi–static and full–wave electromagnetic field solutions, and the experimental technique based on time and frequency domain algorithms.

The first approach is to solve the electromagnetic field equations in an interconnection structure for the given interconnect geometry information. Although, a lot of field solver tools based on electromagnetic computational techniques have been developed, full modeling of the complex interconnection structures in a practical package is somewhat beyond the capability of most of these interconnect modeling tools. Ultimately, the interconnect still must be characterized and verified by measurements after fabrication. The major advantage of field solver tools is that interconnect models can be obtained for structures not yet fabricated so that electrical design rules of a high performance system can be made to account for interconnect effects in the early design phase. The second approach involves creating circuit models of interconnection structures directly from the measured response of the interconnect. The accuracy of the extracted circuit model is readily confirmed by

comparing the simulation data with the measured data, and hence provide a verification path to the model.

In this dissertation, time domain measurement techniques based on peeling algorithms (dynamic deconvolution) are presented. The purpose of this research work aims at electrical characterization and circuit modeling of high speed interconnects and packages by using TDT/R measurements. The contents of these chapters are abstracted below:

. Chapter 2: A technique based on one–dimensional peeling algorithm for the equivalent circuit modeling of general single and symmetrical coupled interconnects with coupled bends in high–speed circuits and packages is presented. The circuit models are extracted from time–domain reflection and transmission measurements (TDR/T). The SPICE simulation results for these extracted circuit models for typical single and symmetrical coupled structures are compared with the measured data to validate the accuracy of the circuit models.

. Chapter 3: A two–dimensional peeling algorithm for electrical characterization and modeling of general coupled interconnects with discontinuities is presented in this chapter. The technique is validated by comparing the results obtained experimentally for the self and mutual equivalent circuit parameters with the theoretical predictions for a non symmetrical inhomogeneous coupled interconnect test structure. A practical case study for a plastic leadless chip carrier (PLCC) package is used to demonstrate the applicability of this technique.

. Chapter 4: Equivalent circuit models of resistive lossy interconnection structures are extracted from time domain reflection and transmission measurements based on an extended peeling algorithm, that includes losses. The simulated results compared with the measured data for interconnects associated with thin film packages are used to validate the accuracy of the algorithm and the model.

. Chapter 5: In this chapter, a frequency dependent nonuniform transmission line model is considered for modeling parallel power/ground planes in high performance electronic packages. The model is based on radial transmission line analysis, and is validated by comparing the calculated time domain response with TDR measured data. The transient effects due to transient sources placed at the different locations of parallel power and ground planes are also investigated. Alternative equivalent circuit models based on lumped circuit elements for power/ground plane structure in a practical package is also proposed. The model is then incorporated with a high speed digital driver model for switching noise simulations. In addition, switching noise with the associated packaging resonance vs different edge rates and clock rates in high speed digital circuits are also reported.

. Chapter 6: Multiport time domain measurement techniques based on one and multi–dimensional peeling algorithms are used to extract equivalent circuit models of a multilayer ceramic (MLC) package. Electrical characteristics of interconnect structures including signal lines and the power/ground system associated with the package are then evaluated by incorporating the

package model with high speed digital circuits for circuit simulations.

Finally, chapter 7 contains the conclusions and suggestions for further work in this area.

2. TIME DOMAIN CHARACTERIZATION AND MODELING OF GENERAL SINGLE (ISOLATED) AND SYMMETRICAL COUPLED INTERCONNECTION STRUCTURES

A technique based on one–dimensional peeling algorithm for the equivalent circuit modeling of general single and symmetrical coupled interconnects in high–speed circuits and packages, is presented. The circuit models are extracted from time–domain reflection and transmission measurement (TDR/T). The simulated results by SPICE for the extracted circuit models of typical single and symmetrical coupled structures are compared with the measured data to validate the accuracy of the algorithm and the resulting circuit models.

2.1 Introduction

High–speed digital and microwave hybrid and monolithic circuits include active and passive circuit elements interconnected by sections of strip, and other microstrip transmission lines having a wide range of characteristic impedances. The resulting junctions and discontinuities, and the electromagnetic coupling between the interconnects, contribute to reflections, signal delay and distortion, and crosstalk which can degrade the circuit and system performance. The same problems are encountered in printed circuit boards, single and multichip modules, and other packages. Therefore, design and simulation of high–speed circuits must incorporate these interconnections.

The time–domain simulation of high–speed monolithic and hybrid integrated circuits, incorporating all the crosstalk, distortion, and delay associated with interconnects and discontinuities such as bends, vias, and pads as shown in Figure 2.1, can be facilitated by accurate equivalent circuit modeling for these interconnects. Lumped equivalent circuits in the form of excess inductances and capacitances are available only for some of these structures, consisting of idealized isolated discontinuities [1–9]. For non-ideal arbitrarily shaped interconnects and coupled multiports, these excess reactance

models are in general not available. These models can, however, be extracted by utilizing the procedure presented in [5]. As shown in [5], the excess reactance parameters can be extracted from the characteristic impedance profile which is in turn derived from the reflection measurements by utilizing the basic layer peeling or deconvolution algorithm [10,11].

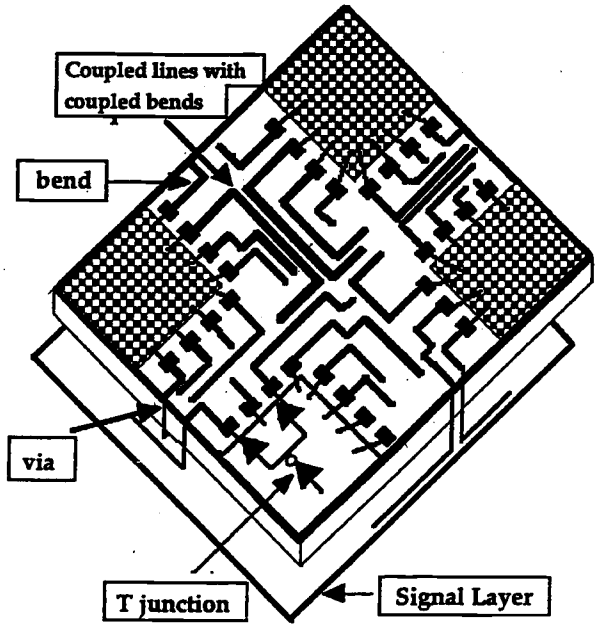


Figure 2.1, General circuit interconnects with the associated package features.

In this chapter, an alternate robust transfer scattering matrix–based algorithm for the extraction of the impedance profile is presented and applied to extract the equivalent circuit models of general single (isolated) and symmetrical coupled interconnection structures. For the case of symmetric coupled interconnects, the four port structure is modeled in terms of even and odd mode characteristic impedance profiles. These distributed models for isolated single as well as coupled interconnects derived from the measured time–domain reflection and transmission measurement (TDR/T) data are used to construct cascaded lumped and hybrid circuit models for these interconnects.

2.2 Circuit modeling of interconnection structures based on one–dimensional peeling algorithm

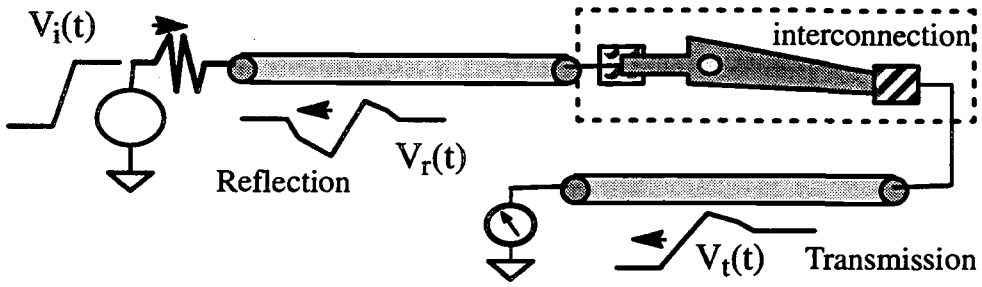


Figure 2.2, The schematic diagram of TDR/T measurements for an interconnection.

The TDR/T techniques have been used extensively in the characterization of interconnects, and applied to extract the equivalent circuits consisting of primarily lumped elements, such as inductors and capacitors for some interconnect structures [5–9]. For the general case of multiple nonuniform cross sections existing in an interconnection as shown in Figure 2.2, the resulting waveforms in time domain can be modelled by a time dependent nonuniform impedance prefile which in turn can be approximated by cascaded uniform transmission line sections as shown in Figure 2.3. For this piecewise uniform cascaded structure, the delay associated with each section, the continuity of voltage across the discontinuities and enegy conservation are readily expressed as,

(a) Timing Equations:

$$Vr'(k,t) = Vr(k,t)\, f(t-tp), \tag{2.1}$$

and $$Vl(k,t) = Vl'(k,t)\, f(t+tp). \tag{2.2}$$

(b) Continuity:

$$Vr'(k,t) + \rho\, Vr'(k,t) = \tau\, Vr'(k,t), \tag{2.3}$$

and $$Vl'(k,t) + \rho'\, Vl'(k,t) = \tau' Vl'(k,t), \tag{2.4}$$

(c) Energy Conservation:

$$y_1 (V_r'(k,t))^2 = y_1 (\rho V_r'(k,t))^2 + y_2 (\tau V_r'(k,t))^2 . \qquad (2.5)$$

Vr and *Vl* are the incident and reflected voltage parameters, respectively, and ρ and ρ' are the forward and backward reflection coefficients, τ and τ' are the corresponding transmission coefficients and y_i is the characteristic admittance of the ith uniform transmission line section.

Alternate descriptions for the cascaded layered medium may also be specified by giving the scattering matrix associated with the reflection coefficients at the intersection of the cascaded sections. The ultimate objective is then to formulate the cascaded transmission line sections with the development of a layer matrix, that is, a matrix which can be used to extrapolate the response observed in one layer to the response observed in the next layer. This process is continued so that we will be able to start with the initial reference impedance of the first layer and from it deduce all the other parameters for the cascaded transmission line sections.

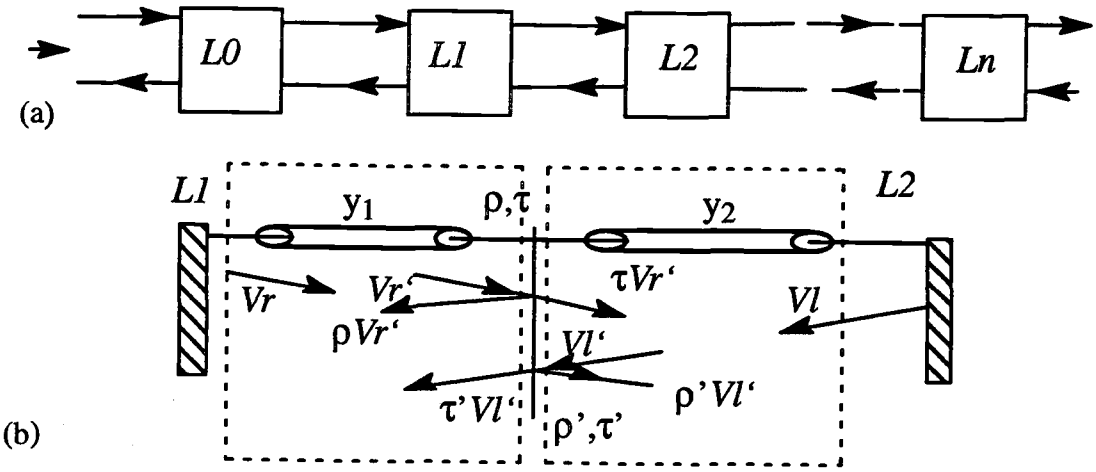


Figure 2.3, (a) Cascaded transmission line sections. (b) The incident and reflected voltage parameters in a cascaded transmission line sections.

2.2.1 Scattering Matrix–Based Peeling Algorithm

As shown in Figure 2.2, for a general interconnection, the impedance profile can be extracted from the measured time domain reflection response based on known inverse scattering techniques [10–12], such as the layer peeling algorithm. Another accurate robust algorithm can be formulated in terms of the transfer scattering matrix of the individual sections. This procedure also includes all the multiple reflections in the entire structure and is presented in this section. The impedances of the piecewise constant cascaded transmission line model consisting of a finite number of sections are extracted in a sequential order by using the characteristics of the reflected waveform for a given incident waveform.

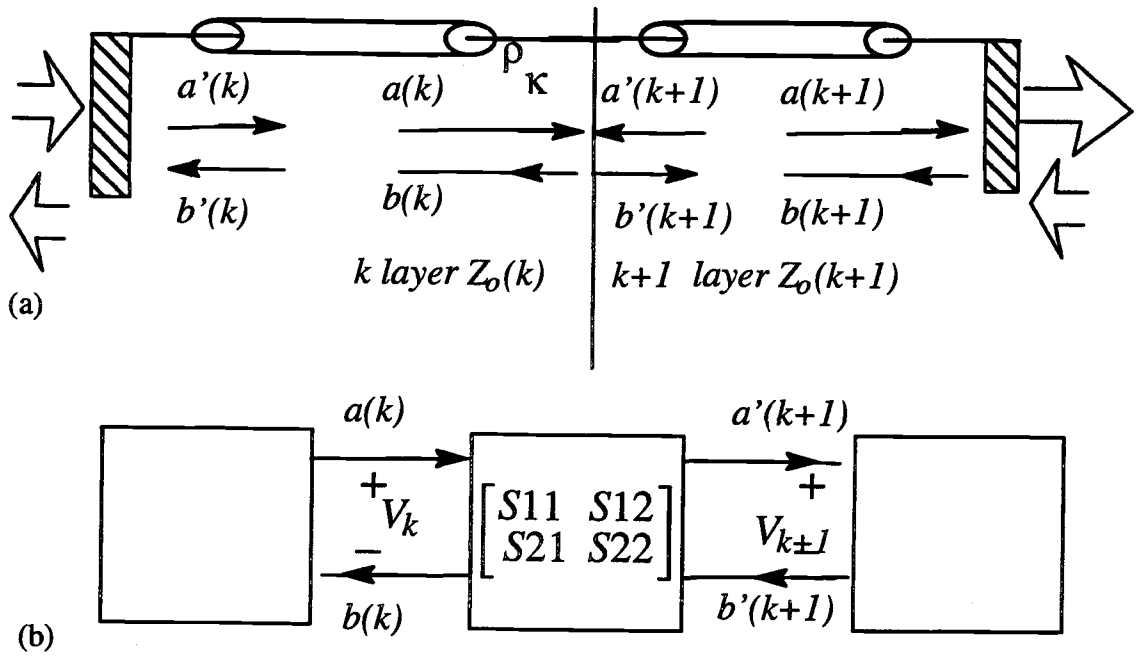


Figure 2.4, (a) The incident and reflection parameters in a cascaded piecewise uniform transmission line sections. (b) Scattering parameters of a two port network.

For a cascaded two port network as shown in Figure 2.4, the scattering matrix [S] is defined to relate two sets of incident and reflected parameters $\{a(k),b(k)\}$ at the input port, and $\{a(k+1),b(k+1)\}$ at the output port as,

$$\begin{bmatrix} b(k,t) \\ b'(k+1,t) \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a(k,t) \\ a'(k+1,t) \end{bmatrix} \tag{2.6}$$

where

$$a(k) = \frac{1}{2}\left[\frac{V_k}{\sqrt{Z_o(k)}} + \sqrt{Z_o(k)}I_k\right], \tag{2.7}$$

$$b(k) = \frac{1}{2}\left[\frac{V_k}{\sqrt{Z_o(k)}} - \sqrt{Z_o(k)}I_k\right], \tag{2.8}$$

$$a(k+1) = \frac{1}{2}\left[\frac{V_{k+1}}{\sqrt{Z_o(k+1)}} + \sqrt{Z_o(k+1)}I_{k+1}\right], \tag{2.9}$$

$$b(k+1) = \frac{1}{2}\left[\frac{V_{k+1}}{\sqrt{Z_o(k+1)}} - \sqrt{Z_o(k+1)}I_{k+1}\right], \tag{2.10}$$

where $Z_o(k)$ and $Z_o(k+1)$ are the reference impedance at the input and output ports, respectively.

Elements along the main diagonal of the scattering matrix are reflection coefficients, and the off–diagonal elements are transmission coefficients. Consider the general expressions for the nonuniform transmission line, which is modeled as the stepped impedance lines with an equal propagation delay unit as shown in Figure 2.4. The transfer scattering matrix for the impedance discontinuities relates the input incident and reflected parameters of any sections to the output parameters of the proceeding section and is expressed as

$$\begin{bmatrix} b(k,t) \\ a(k,t) \end{bmatrix} = \begin{bmatrix} T_{11}(k) & T_{12}(k) \\ T_{21}(k) & T_{22}(k) \end{bmatrix} \begin{bmatrix} b'(k+1,t) \\ a'(k+1,t) \end{bmatrix} \tag{2.11}$$

The elements of the [T(*k*)] matrix are readily derived in terms of the definition of the scattering parameters *a*'s and *b*'s and are found to be

$$[T(k)] = (1 - \rho^2_{k,k+1})^{(-\frac{1}{2})} \begin{bmatrix} 1 & \rho_{k,k+1} \\ \rho_{k,k+1} & 1 \end{bmatrix} \tag{2.12}$$

$$\text{with} \quad \rho_{k,k+1} = \frac{(Z_o(k+1) - Z_o(k))}{(Z_o(k+1) + Z_o(k))}, \tag{2.13}$$

where $Z_o(k)$ denote the characteristic impedance of the *k*th section.

The transfer matrix of each delay element can be expressed as

$$\begin{bmatrix} a'(k+1,t) \\ b'(k+1,t) \end{bmatrix} = \begin{bmatrix} f(t - t_{pd}) & 0 \\ 0 & f(t + t_{pd}) \end{bmatrix} \begin{bmatrix} b(k+1,t) \\ a(k+1,t) \end{bmatrix}$$

$$= [D] \begin{bmatrix} b(k+1,t) \\ a(k+1,t) \end{bmatrix} \tag{2.14}$$

where [D] is the delay element matrix and t_{pd} is the propagation delay unit of each transmission line.

Combining equations (2.11) and (2.14) gives the transfer scattering of each section including the discontinuities and the delay element as,

$$\begin{bmatrix} b(k,t) \\ a(k,t) \end{bmatrix} = [\mathrm{T}(k)][D] \begin{bmatrix} b(k+1,t) \\ a(k+1,t) \end{bmatrix}. \tag{2.15}$$

The overall transfer scattering matrix for the entire model structure consisting of *n* sections is then given by

$$\begin{bmatrix} b(1,*) \\ a(1,*) \end{bmatrix} = [\mathrm{T}(1)][D][\mathrm{T}(2)][D]$$

$$\cdots [\mathrm{T}(n-1)][D][\mathrm{T}(n)] \begin{bmatrix} b(k+1,t) \\ a(k+1,t) \end{bmatrix} . \tag{2.16}$$

From equation (2.16), it is seen that the reflection function $B(*,*)$ and the incident function $A(*,*)$ corresponding to the k+1th sections is related to that of the kth sections by

$$\begin{bmatrix} B(k+1,t) \\ A(k+1,t) \end{bmatrix} = ([D]^{-1})([T(k)]^{-1}) \begin{bmatrix} B(k,t) \\ A(k,t) \end{bmatrix}. \tag{2.17}$$

The above expression for the transfer matrix is iterative in nature and allows us to extract the reflection coefficients as given by

$$\rho_{k+1,k+2} = \frac{B(k+1,1)}{A(k+1,1)}, \tag{2.18}$$

and hence, the model impedance in a sequential manner. The procedure for extracting the characteristic impedances of the stepped impedance model is straightforward in that we consider the first section to be the same as the internal impedance of the TDR system. The schematic flow diagram of scattering matrix–based one–dimensional peeling algorithm is shown in Figure 2.5. This iterative process based on equations (2.17) and (2.18) is then repeated until $\rho_{n,n+1}$ is calculated and the distributed circuit model is completed.

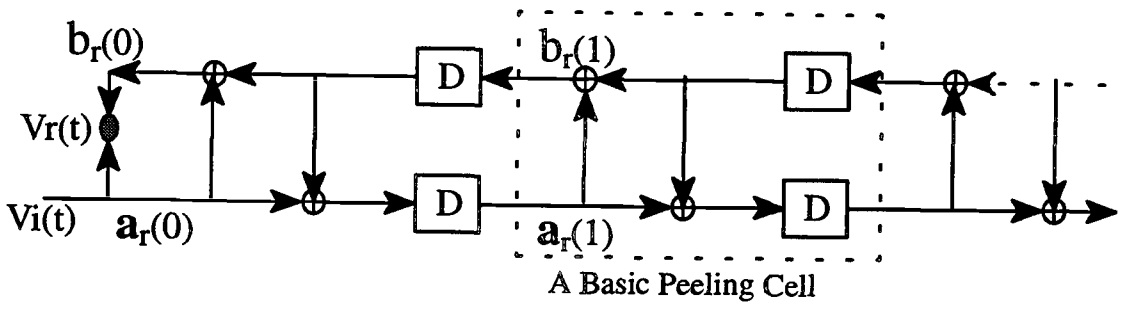


Figure 2.5, The signal flow diagram of one–dimensional peeling algorithm.

2.2.2 Lumped/Distributed Element Model Of Single (Isolated) Interconnection Structures

A transmission line can be defined as any structure that guides a propagating electromagnetic wave from one point to another. Figure 2.6–(a) shows a schematic uniform lossless transmission line based on the distributed element model. The voltage between the line and the reference and the current on the line can described by the transmission line equations as given by

$$\frac{\partial v}{\partial z} = - L\frac{\partial i}{\partial t} \tag{2.19}$$

$$\frac{\partial i}{\partial z} = - C\frac{\partial v}{\partial t} \tag{2.20}$$

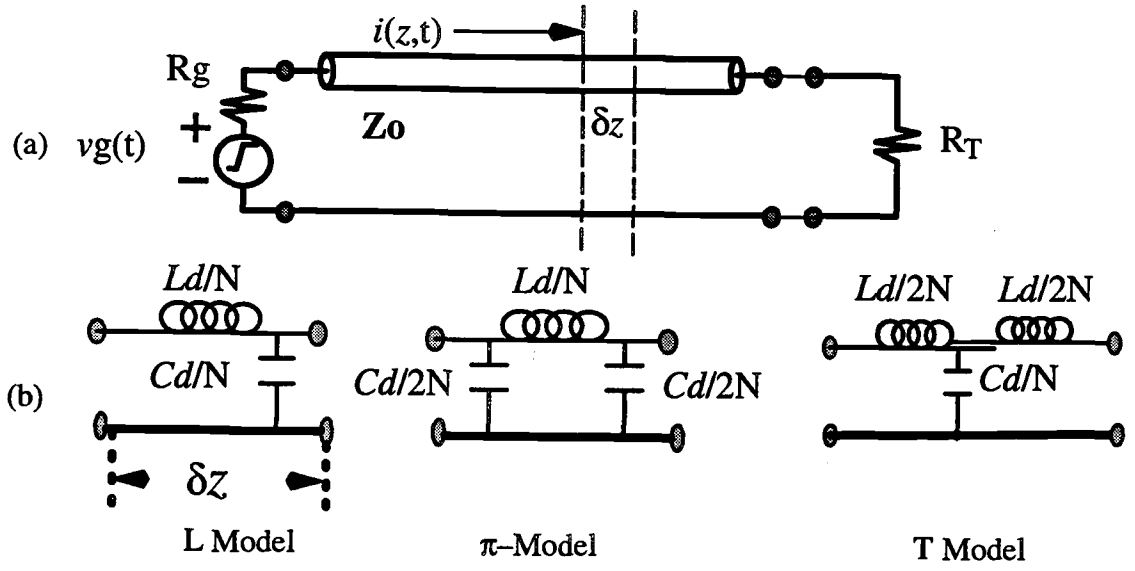


Figure 2.6, (a) The distributed model of the transmission line. (b) The lumped element models of the transmission line.

If the electrical length of the interconnection is electrically short, (i.e., the line length is much less than the wavelength of the signal on the line) then the interconnection can be represented by a lumped LC element model or the cascaded lumped element model with an appropriate number of sections. The various types of the lumped element model are shown in Figure 2.6–(b) including L–model, T–model and π–model. The accura-

cy of the lumped element model depends on the electrical parameters of the line (L, C), the number of the cascaded sections (N), the line length (d) and the frequency of interest (f). In general, the number of the cascaded lumped elements sections in the model can be determined by

$$N \geq Afd\sqrt{LC} \tag{2.21}$$

where A is a constant determined by the relative error for the difference between the input impedance of the distributed model and the input impedance of the cascaded lumped element model.

For the time domain analysis of a pulse–like digital waveform propagating down the line, the highest frequency harmonics of concern are dominated by the edge rate of the pulse, and the number of the cascaded sections is determined by

$$N \geq 5d\frac{\sqrt{LC}}{t_r} \tag{2.22}$$

where $t_r = \dfrac{1}{\pi f_{\max}}$ is edge rate and $f_{\max}$. is the maximum frequency harmonic of the pulse–like waveform. The relative error for the difference between the impedance of the cascaded lumped element and the impedance of the distributed model is less than 5% [79].

For a general isolated interconnect, a distributed element model is readily obtained by using the procedure described in the last section. The model consists of a number of cascaded uniform transmission line sections which can also be used to construct the lumped equivalent excess parameter model for these discontinuities [5,13] as well as a proposed hybrid or lumped/distributed model consisting of a optimum number of lumped elements and transmission lines. As the number of sections for distributed model becomes large, the simulation of the interconnect on programs like SPICE becomes time consuming and these alternate hybrid models consisting of lumped as well as distributed elements may be more compatible with these simulation

tools. The building blocks for hybrid models of these lossless structures are delay elements augmented with inductances and capacitances as shown in Figure 2.7. For this model, portions of the impedance profile near the maxima and their inverse near minima are integrated to obtain the equivalent lumped values, whereas the near flat portions are used as piecewise constant impedances. The equivalent lumped values are [5]

$$L = \int_{t_{l-}}^{t_{l+}} Z_o(t)\, dt, \tag{2.23}$$

$$\text{and } C = \int_{t_{c-}}^{t_{c+}} Y_o(t)\, dt \tag{2.24}$$

where t_{l-} to t_{l+} defines the time duration corresponding to a maxima and t_{c-} to t_{c+} corresponds to the time interval near a minima. This hybrid model is intended to combine the efficiency of the lumped models with the accuracy of the distributed models, leading to efficient accurate simulation of the circuits in the circuit simulator.

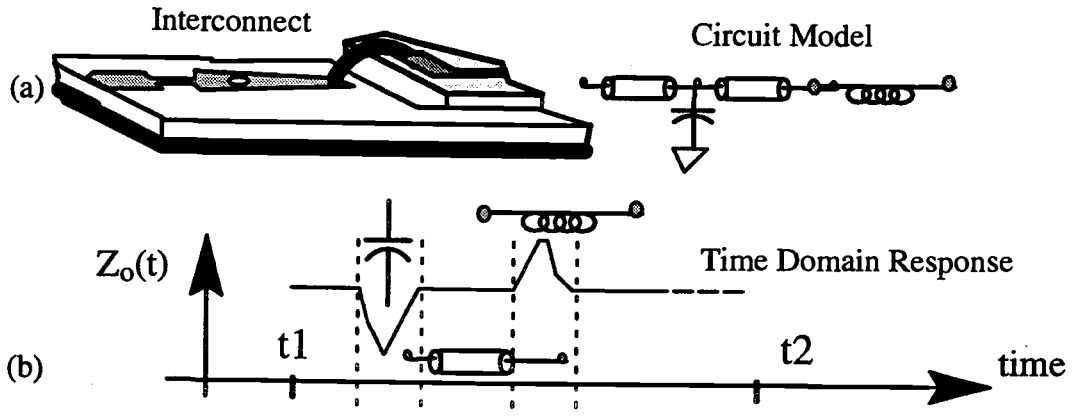


Figure 2.7, (a) Interconnect structures in electronic packages. (b) The schematic impedance profile of a typical interconnect structure with the corresponding circuit elements.

2.2.3 Decoupled Line Model of General Symmetrical Coupled Interconnection Structures

Consider a general lossless uniformly coupled n–line interconnect described by the multiconductor transmission line equations

$$\frac{\partial[v(z,t)]}{\partial z} = -[L]\frac{\partial[i(z,t)]}{\partial t}, \tag{2.25}$$

$$\text{and } \frac{\partial[i(z,t)]}{\partial z} = -[C]\frac{\partial[v(z,t)]}{\partial t}, \tag{2.26}$$

where the voltage and current vector on the multiple interconnects are represented by

$$[v(z,t)] = [v_1(z,t), v_2(z,t), \cdots\cdots, v_n(z,t)]^T, \tag{2.27}$$

$$\text{and } [i(z,t)] = [i_1(z,t), i_2(z,t), \cdots\cdots, i_n(z,t)]^T. \tag{2.28}$$

[L] and [C] are the n × n, per unit length inductance and capacitance parameter matrices of the multiple coupled lines, respectively. Note that the inductance and capacitance matrices can be obtained by using electromagnetic computational techniques [13–16] and experimental techniques [17] for general uniformly coupled lines..

By decoupling the multiple coupled transmission line equations [18], equations (2.25) and (2.26) lead to the uncoupled transmission line equation as given by

$$\frac{\partial[e(z,t)]}{\partial z} = -Diag[L_k]\frac{\partial[j(z,t)]}{\partial t}, \tag{2.29}$$

$$\text{and } \frac{\partial[j(z,t)]}{\partial z} = -Diag[C_k]\frac{\partial[e(z,t)]}{\partial t} \tag{1.30}$$

where $Diag[L_k]$ and $Diag[C_k]$ are diagonal matrices as given by

$$[L_k] = [M_v]^{-1}[L][[M_v]^T]^{-1} \tag{2.31}$$

$$[C_k] = [M_v]^T[C][M_v]. \tag{2.32}$$

[e] and [j] are the voltages and currents on the uncoupled transmission lines given by

$$[v(z,t)] = [M_v][e(z,t)] \tag{2.33}$$

$$[i(z,t)] = [M_i][j(z,t)] \tag{2.34}$$

where the voltage eigenvector $[M_v]$ and current eigenvector $[M_i]$ matrices are related by

$$[M_i] = [[M_v]^T]^{-1}. \tag{2.35}$$

The above equations (2.29)–(2.34) result in a mode characteristic impedances and phase velocities as given by

$$Z_k = \sqrt{\frac{L_k}{C_k}} \quad \text{and} \quad u_k = \sqrt{\frac{1}{L_k C_k}}, \text{ respectively.} \tag{2.36}$$

The uncoupled multiple transmission equations together with the orthogonality between the current and voltage eigenvectors lead to the equivalent circuit model of multiple coupled interconnect structures as shown in Figure 2.8 such that the model can be incorporated with the general circuit element models in circuit simulations by using general CAD tools.

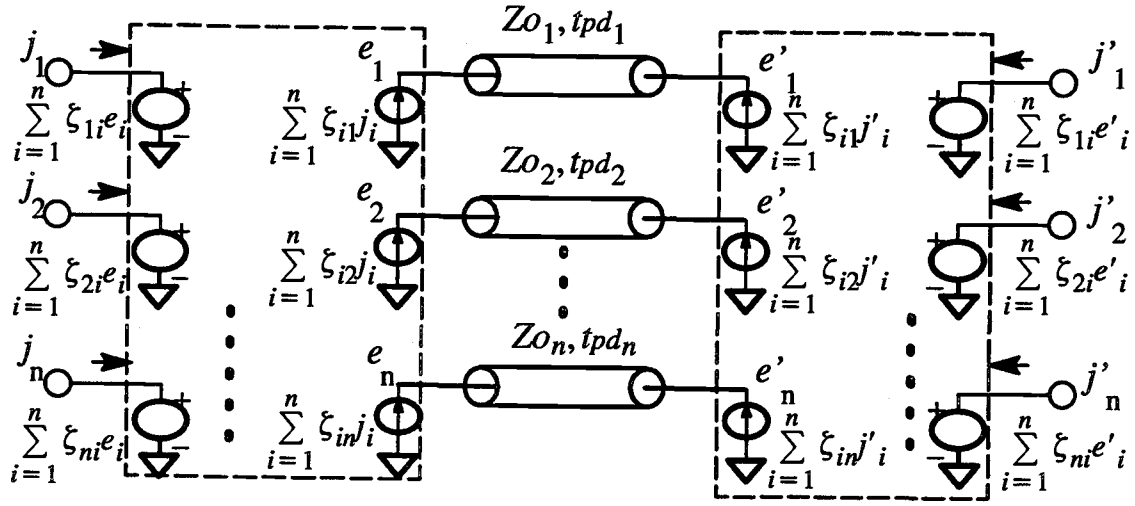


Figure 2.8, Equivalent circuit model of the multiple coupled interconnects.

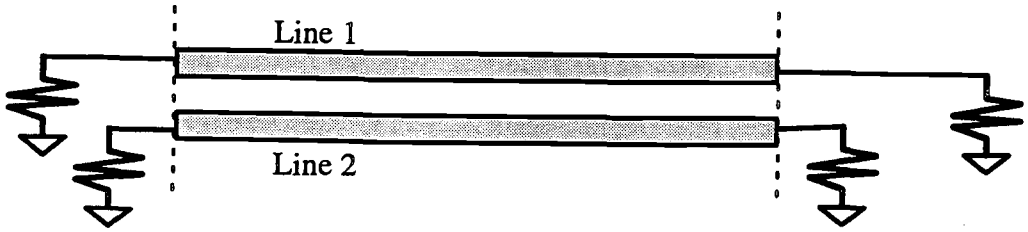


Figure 2.9, The schematic symmetric uniformly coupled interconnections.

The technique which has been developed for the multiple uniformly coupled interconnect structures is then applied to the typical case of two symmetrical coupled lines interconnections as shown in Figure 2.9. The inductance and capacitance matrices are given by

$$[L] = \begin{bmatrix} L_1 & L_m \\ L_m & L_1 \end{bmatrix} \text{ and } [C] = \begin{bmatrix} C_1 + C_m & -C_m \\ -C_m & C_1 + C_m \end{bmatrix}. \tag{2.37}$$

The two velocities defined as the even and odd modes are

$$u_e = \frac{1}{\sqrt{(L_1 + L_m)C_1}} \quad \text{and} \quad u_o = \frac{1}{\sqrt{(L_1 - L_m)(C_1 + 2C_m)}}. \tag{2.38}$$

The even and odd mode characteristic impedances are

$$Z_e = \sqrt{\frac{L_1 + L_m}{C_1}} \quad \text{and} \quad Z_o = \sqrt{\frac{L_1 - L_m}{C_1 + 2C_m}}, \tag{2.39}$$

and the characteristic impedance matrix is

$$[Z_o] = \begin{bmatrix} \frac{Z_e + Z_o}{2} & \frac{Z_e - Z_o}{2} \\ \frac{Z_e - Z_o}{2} & \frac{Z_e + Z_o}{2} \end{bmatrix}. \tag{2.40}$$

The normalized voltage eigenvector for this symmetric coupled lines is obtained as

$$[M_v] = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}. \tag{2.41}$$

The single interconnect model consisting of a stepped impedance transmission line structure will now be used to construct coupled interconnect models in terms of the two orthogonal normal modes. For general symmetric structures, these are even (symmetric or common) and odd (antisymmetric or differential) modes of propagation. The corresponding impedance profiles can be extracted by exciting these modes directly in the structure with a multichannel TDR/T system. That is,

$$\rho_1(t) = \rho_2(t) = \rho_e(t), \quad \text{for } V_{i1}(t) = V_{i2}(t) = U(t), \tag{2.42}$$

$$\rho_1(t) = -\rho_2(t) = \rho_o(t), \quad \text{for } V_{i1}(t) = -V_{i2}(t) = U(t). \tag{2.43}$$

The even– and odd– mode reflection coefficients corresponding to even– and odd–mode respectively can also be found by exciting input port of one interconnect and measuring the reflection at that port and transmitted signal at the other near end port . In terms of these $\rho_1(t)$ and $\rho_2(t)$ measured with $V_{i1}(t) = U(t), V_{i2}(t) = 0$,

$$\rho_e(t) = \frac{\rho_1(t) + \rho_2(t)}{2}, \tag{2.44}$$

$$\text{and } \rho_o(t) = \frac{\rho_1(t) - \rho_2(t)}{2}.. \tag{2.45}$$

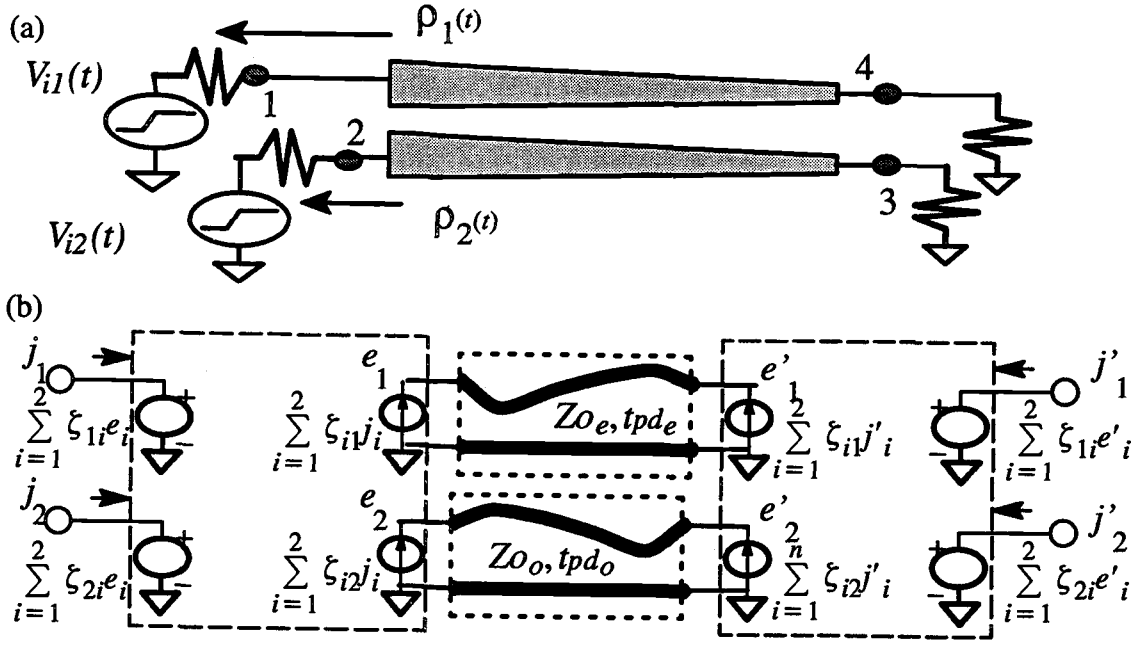


Figure 2.10, (a) General symmetrical coupled interconnects. (b) The equivalent circuit model for symmetrical coupled interconnects.

This is illustrated in Figure 2.10 together with the equivalent circuit for the coupled line structure which in general consists of the mode decoupling network, the even and odd mode impedance lines having corresponding propagation delays, and the mode coupling network [14]. The even and odd mode nonuniform transmission lines are synthesized in terms of the corresponding incident and reflected waveforms by using the same procedure as the one used for the single line presented previously.

The distributed model can also be used to construct the cascaded lumped equivalent circuit model of coupled lines by using the relationship between self and mutual line constants per unit length and the even and odd mode impedances and propagation constant [19]. For example, for the case of uniform coupled interconnects consisting of parallel traces having identical width and uniform separation, the total self and mutual inductances and capacitances associated with the interconnect are

$$L_1 = \frac{tpd_e\, Zo_e + tpd_o\, Zo_o}{2} \tag{2.46}$$

$$L_m = \frac{tpd_e\, Zo_e - tpd_o\, Zo_o}{2} \tag{2.47}$$

$$C_1 = \frac{tpd_e}{Zo_e} \tag{2.48}$$

$$\text{and } C_m = -\frac{tpd_o}{2\, Zo_o} + \frac{tpd_e}{2\, Zo_e} \tag{2.49}$$

where Zo_e and Zo_o are the even and odd mode characteristic impedances and tpd_e and tpd_o are the even and odd mode propagation delays. The corresponding lumped equivalent circuit is shown in Figure 2.11. For longer lines, we can construct a model by cascading a desired number of lumped element sections having the same topology as the circuit of Figure 2.8. For the nonuniform line case, the incremental lumped element values at a given cross section can be calculated by using the integral expression for $Zo_e(t)$ and $Zo_o(t)$ corresponding to that cross section as given by equations (2.46)

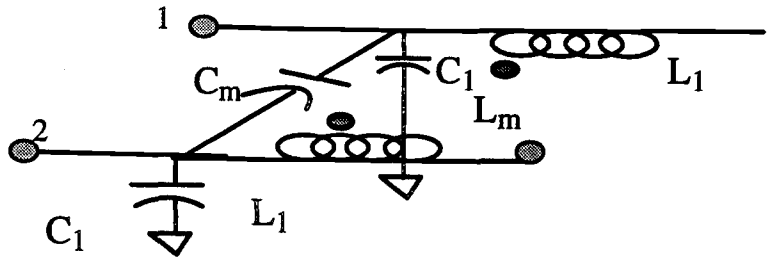
and (2.47). The total self and mutual inductances and capacitances associated with the nonuniform interconnection structure are given by

$$L_1 = \frac{\int Zo_e(t)\,dt + \int Zo_o(t)\,dt}{2} \tag{2.50}$$

$$L_m = \frac{\int Zo_e(t)\,dt - \int Zo_o(t)\,dt}{2} \tag{2.51}$$

$$C_1 = \int \frac{1}{Zo_e(t)} dt \tag{2.52}$$

$$\text{and } C_m = -\int \frac{1}{2\,Zo_e(t)} dt + \int \frac{1}{2\,Zo_o(t)} dt\,. \tag{2.53}$$



Total inductances and capacitances

Figure 2.11, Lumped equivalent circuit model of coupled interconnects.

2.3 Results

The above techniques have been applied to model a host of interconnect structures as well as some scaled models. Typical examples are included in this section to demonstrate the modeling techniques and validate the accuracy of the circuit models by comparing the measured data with SPICE simulation results for the models. The first structure is a nominal 50–ohms trace with three right angled bends as shown in Figure 2.12. The measured TDR data for the structure is shown in Figure 2.13–(a). The incident waveform was a 28–ps rise time pulse waveform and the impedance profile extracted from the TDR data by using the algorithm presented in the previous section is shown in Figure 2.13–(b). This impedance profile or stepped impedance distributed model was also used to construct a hybrid model. Figure 2.14–(a) shows the schematics of the two port network for the distributed mode and the hybrid model. In order to ascertain the accuracy of the modeling procedure, the simulated finite rise time response of the models on SPICE is compared with the measured data as shown in Figure 2.14–(b). For these SPICE simulations, the distributed circuit model was simulated with 36 line sections whereas the hybrid model consists of 6 transmission line sections and 5 lumped elements. The computational time of the distributed and hybrid models on HP–9000 workstation are 57s and 35 s, respectively.

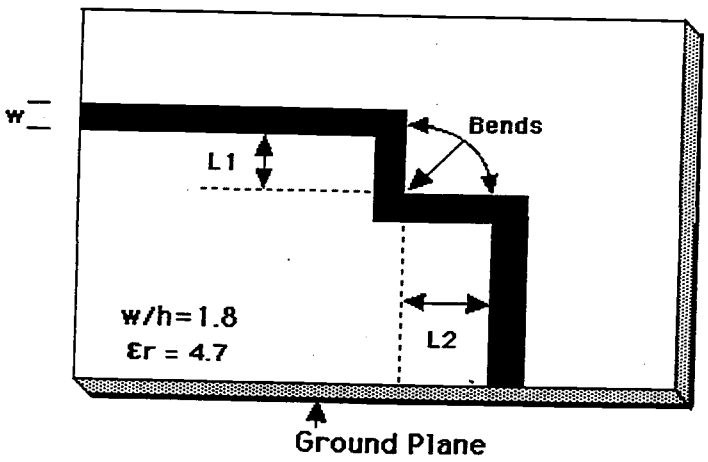
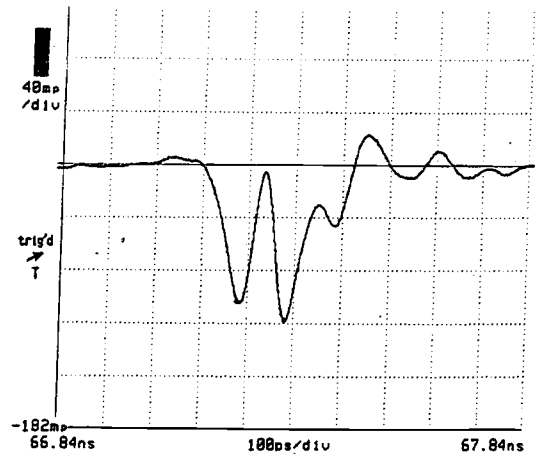


Figure 2.12, The schematic interconnect structure with multiple bends.

(a)



(b)

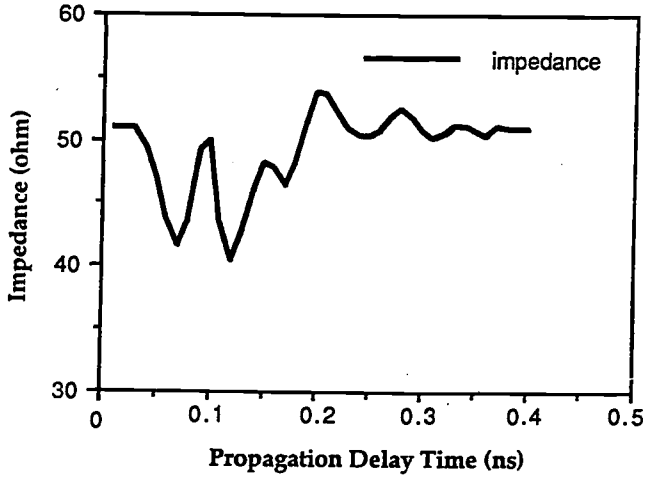


Figure 2.13, (a) The measured TDR data for the interconnect of Figure 2.11. (b) The measured nonuniform impedance profile extracted from the measured TDR data in (a).

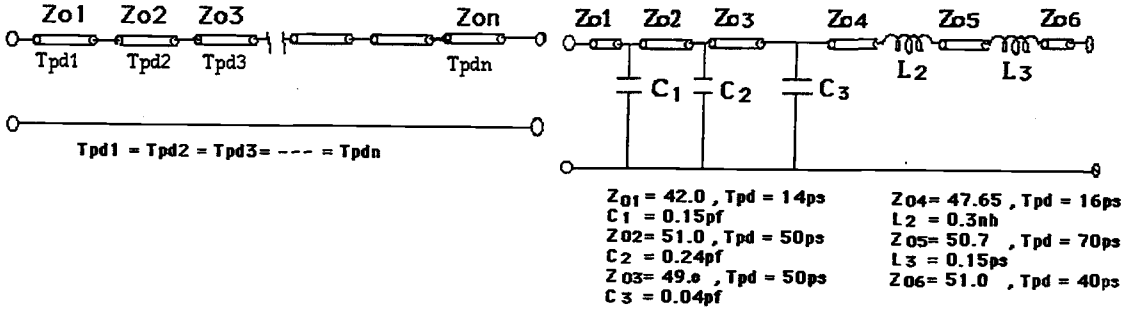


Figure 2.14, (a) The equivalent circuit models: (i) Distributed model, (ii) Hybrid model.

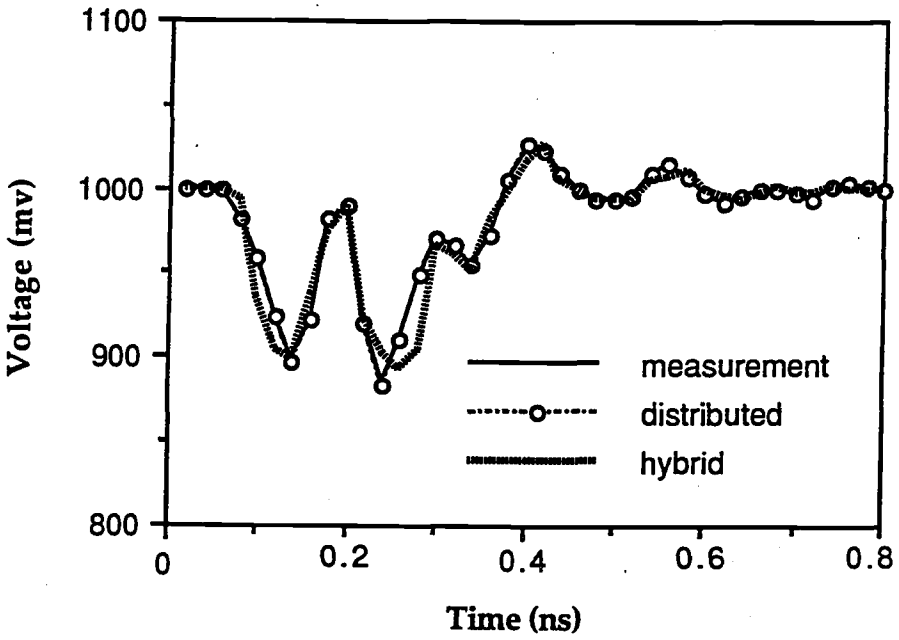
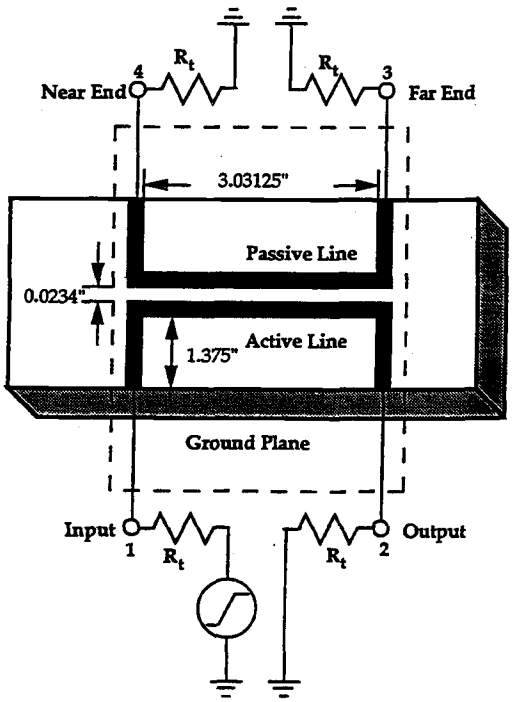


Figure 2.14, (b) The simulated response versus the measured data.

The second example is the symmetrical coupled lines with right angle coupled bends, which is quite common in PCB's interconnection, multichip packaging, and VLSI circuits. The test pattern which is sketched as a four–port network in Figure 2.15–(a), is made on the common epoxy glass substrate in which the dielectric constant = 4.7 and the substrate high $h = 0.05$ in. These line impedances are 50 ohms for matching the internal impedance of the TEK SD–24 sampling head. In order to accurately model this coupled line structures, the coupled bend effects have to be considered in the equivalent circuit model. Figure 2.15–(b) shows the even and odd mode impedance profiles where the overlap region at the beginning was formed by two uncoupled lines and the ripple waveforms at the beginning and end region of the even and odd mode impedances is due to the discontinuity effects of right angle coupled bends. These impedance profiles were evaluated by utilizing the time–domain reflected and transmitted waveforms by using the procedure given in the previous section. These even and odd mode impedance profiles extracted from the measured data are used to construct the SPICE compatible model shown in Figure 2.10–(b). The results of SPICE simulation

are compared with the measured waveforms for the input port and output port of the active line, and the near end coupled voltage and far end coupled voltage of the passive line, as shown in Figure 2.16.

(a)



(b)

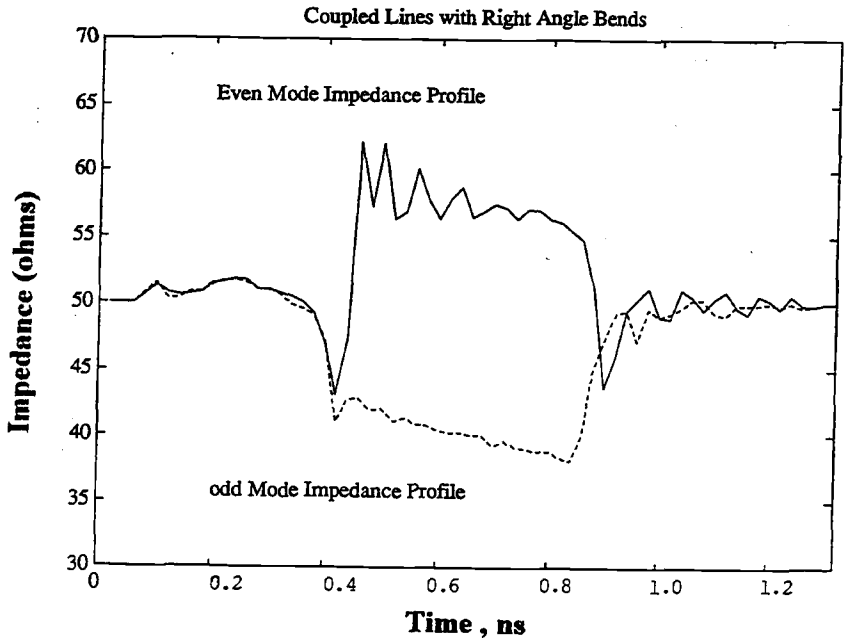
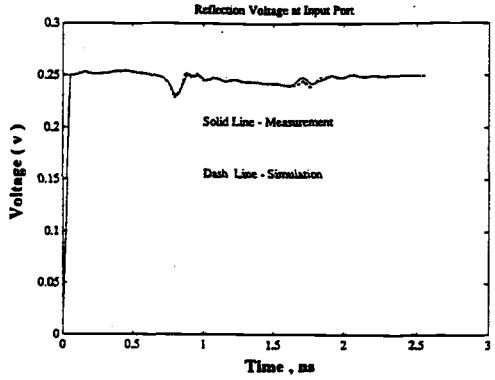
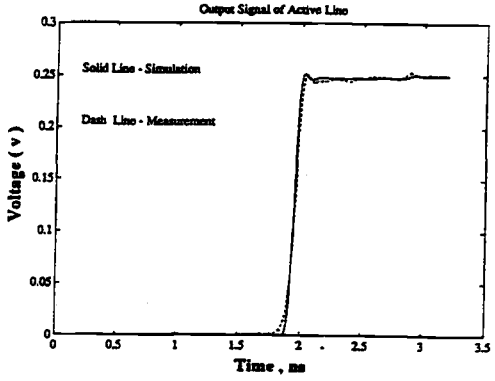


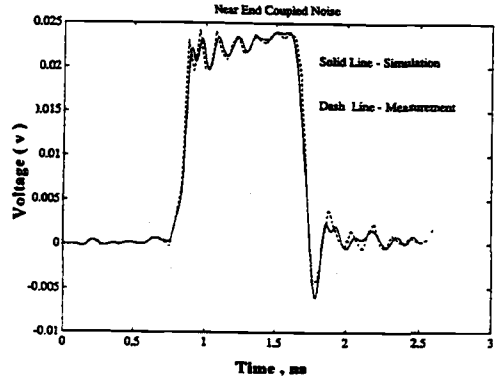
Figure 2.15, (a) The schematic coupled lines including right angle coupled bends. (b) The even and odd mode impedance profiles extracted from the measured data in (a).



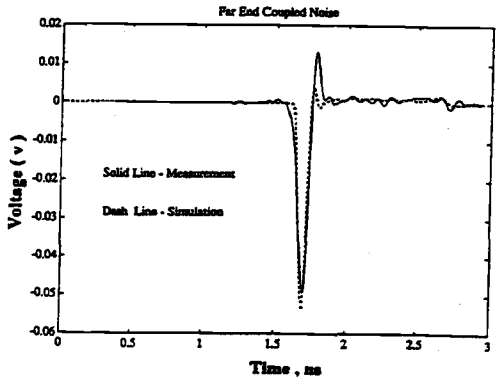
(a)



(b)



(c)



(d)

Figure 2.16, (a) The simulated and measured reflected waveforms at the input port of the active line. (b) The simulated and measured transmission waveforms of the active line. (c) The simulated and measured near end coupled voltages of the passive line. (d) The simulated and measured far end coupled voltages of the passive line.

2.4 Summary

Techniques based on time domain measurements for the circuit modeling of lossless single and symmetrical coupled interconnects in integrated circuits and chip modules have been presented. Calibration and de–embedding techniques formulated in [20,61–64] can be used to enhance the time domain measurements (Appendix A) and hence the accuracy of the models. The characteristic impedance profile of nonuniform transmission line model is extracted from TDR data by using a deconvolution algorithm based on the transmission scattering matrix of the discretized nonuniform transmission line model. The extension of the technique to symmetrical coupled interconnects and discontinuities has also been presented. These distributed models have been used to construct lumped as well as hybrid (lumped/distributed) equivalent circuits of various isolated and coupled interconnects. The accuracy of the circuit modeling procedure has been ascertained by comparing the simulated response of the circuit models with the measured data for typical single and coupled structures. The agreement between the simulated and measured waveforms affirms the validity of the TDR/T–based modeling techniques for the time–domain simulation of interconnects in high–speed digital circuits, multilevel PCB's, and single and multiple chip modules. These techniques should be useful in helping validate the circuit models based on electromagnetic computational techniques as well as provide an independent tool to synthesize circuit models for general nonuniform or interacting two– and three– dimensional interconnects.

3. TIME DOMAIN CHARACTERIZATION AND MODELING OF GENERAL COUPLED INTERCONNECTION STRUCTURES

A time domain experimental technique for the characterization and modeling of general coupled interconnects and discontinuities is presented in this chapter. The technique is based on a two–dimensional peeling algorithm and is validated by comparing the results obtained experimentally for the self and mutual equivalent circuit parameters with the theoretical predictions for a non symmetrical inhomogeneous coupled interconnect test structure. A practical case study for electrical characterization and modeling of a plastic leadless chip carrier (PLCC) package is also used to demonstrate the applicability of this technique.

3.1 Introduction

In recent years, several experimental techniques based on time and frequency domain measurements have been proposed to characterize coupled transmission line structures. The work on coupled interconnects has dealt primarily with uniformly and nonuniformly coupled interconnects in a homogeneous medium [17,23–25]. For general single (isolated) interconnects, including discontinuities, a method based on a layer peeling algorithm has been developed to characterize and model interconnects from TDR/T data. This technique has been applied to characterize discontinuities such as steps, bends, vias, and T junctions and symmetrical coupled microstrip lines [26,27]. In this chapter, a two dimensional peeling (dynamic deconvolution) algorithm is proposed to model general coupled interconnects from two port time domain scattering parameter measurements.

3.2 Circuit Modeling Procedure

3.2.1 Two–Dimensional Layer Peeling Algorithm

For the general case of single nonuniform interconnect having discontinuities, the resulting waveforms obtained from the TDR data is characterized by a time dependent impedance profile [26,27]. This nonuniform impedance profile can be approximated by cascaded uniform transmission line sections. The impedance of each uniform line section is extracted from TDR measurement by applying one dimensional peeling technique [26]. This algorithm based on dynamic deconvolution has been formulated in terms of the transfer scattering parameters of the piecewise uniform transmission line sections [27]. This procedure can be extended to two dimensional systems and can be used to characterize general coupled interconnects as shown in Figure 3.1.

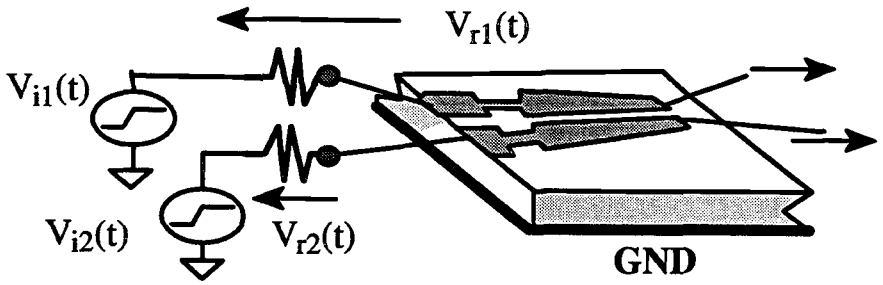


Figure 3.1, Coupled interconnection structure.

In general, two nonuniformly coupled lossless transmission lines as shown in Figure 3.2 is used to characterize the general coupled interconnection structure as shown in Figure 3.1, where Z_i (i=1,2) are the self impedance profiles, and Z_m is the mutual impedance profile. An alternative equivalent circuit model based on the cascaded uniformly coupled line sections is obtained by dividing the nonuniformly coupled transmission line model into N coupled line sections. The cascaded model consisting of uniform coupled sections is shown in Figure 3.3–(a).

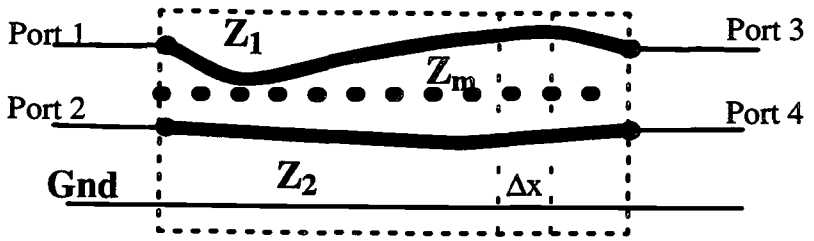


Figure 3.2, Nonuniformly coupled transmission line model.

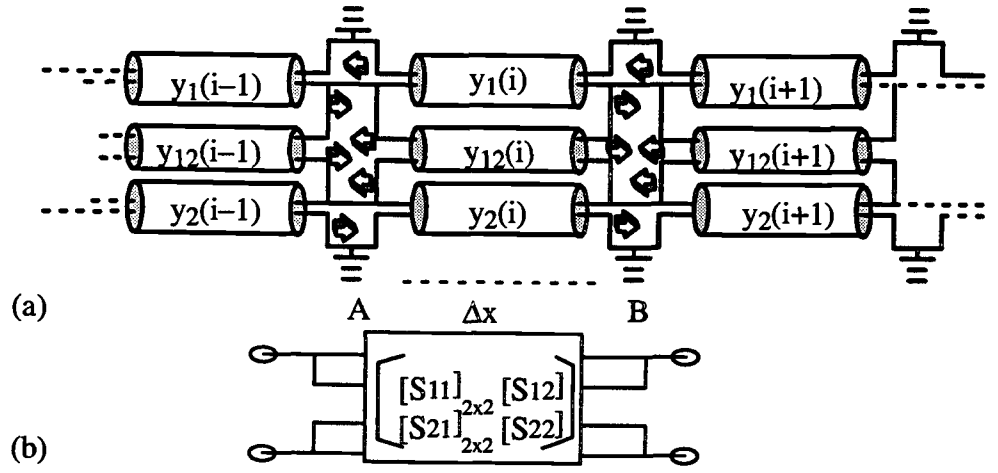


Figure 3.3, (a) The circuit diagram of the cascaded coupled transmission line sections. (b) Scattering parameter matrices of a four–port network.

For a four–port network in the cascaded coupled line model as shown in Figure 3.3–(b), the schematic incident and reflection parameters are shown in Figure 3.4. The scattering matrices [S] is defined as

$$\begin{bmatrix} [b_r(\mathrm{i},t)] \\ [b_\ell(\mathrm{i},t)] \end{bmatrix} = \begin{bmatrix} [\mathrm{S}_{11}(\mathrm{i})] & [\mathrm{S}_{12}(\mathrm{i})] \\ [\mathrm{S}_{21}(\mathrm{i})] & [\mathrm{S}_{22}(\mathrm{i})] \end{bmatrix} \begin{bmatrix} [a_r(\mathrm{i}+1,t)] \\ [a_\ell(\mathrm{i}+1,t)] \end{bmatrix}. \tag{3.1}$$

For this case, a 4x4 transfer scattering matrix interrelating the input incident and reflected parameter matrices of any coupled sections to that of the adjoining coupled sections is defined as

$$\begin{bmatrix} [b_r(\mathrm{i},t)] \\ [a_r(\mathrm{i},t)] \end{bmatrix} = \begin{bmatrix} [\mathrm{T}_{11}(\mathrm{i})] & [\mathrm{T}_{12}(\mathrm{i})] \\ [\mathrm{T}_{11}(\mathrm{i})] & [\mathrm{T}_{22}(\mathrm{i})] \end{bmatrix} \begin{bmatrix} [a_\ell(\mathrm{i}+1,t)] \\ [b_\ell(\mathrm{i}+1,t)] \end{bmatrix}. \tag{3.2}$$

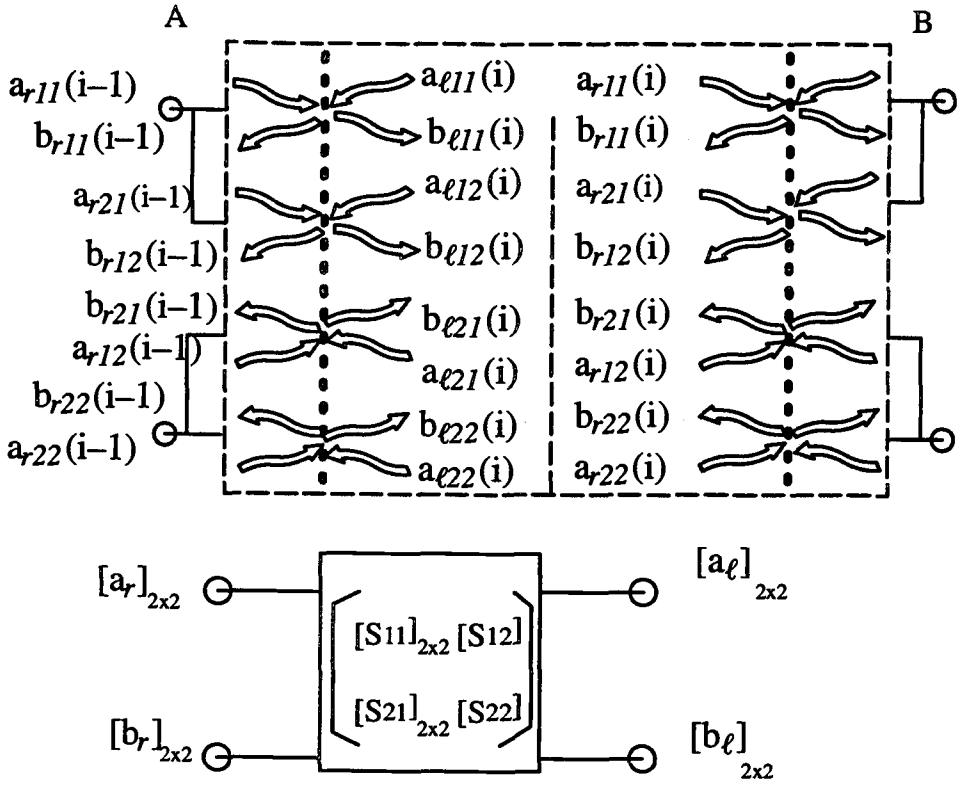


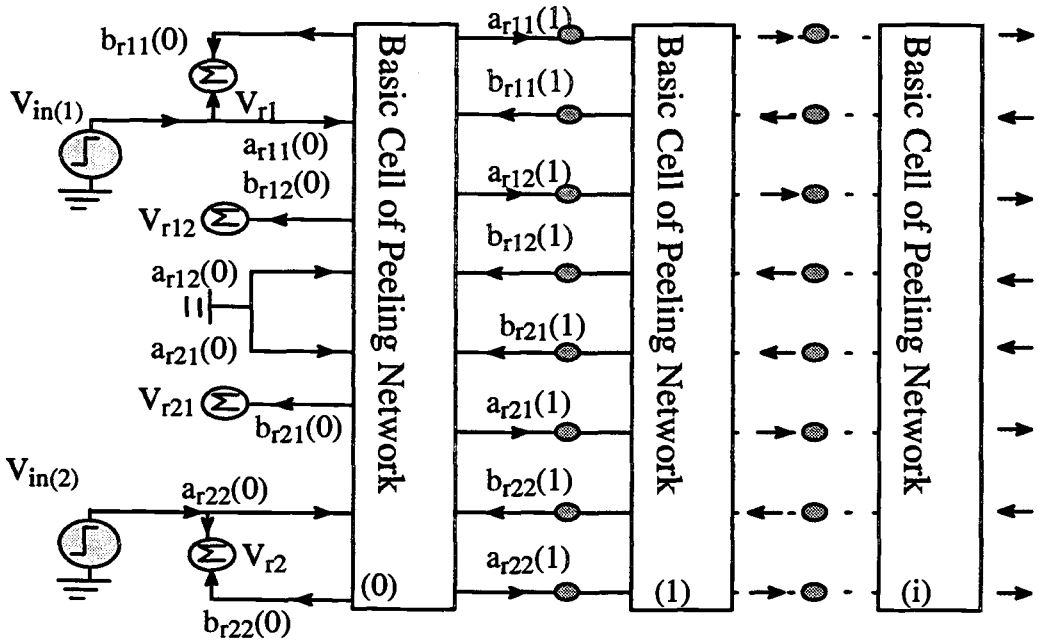
Figure 3.4, The incident and reflection parameters in the cascaded coupled line model.

By incorporating time shifted element matrix due to the propagation delay time of coupled line sections into equation (3.1), the transfer scattering matrix of each coupled line section including the impedance mismatch between two coupled line sections can be expressed as,

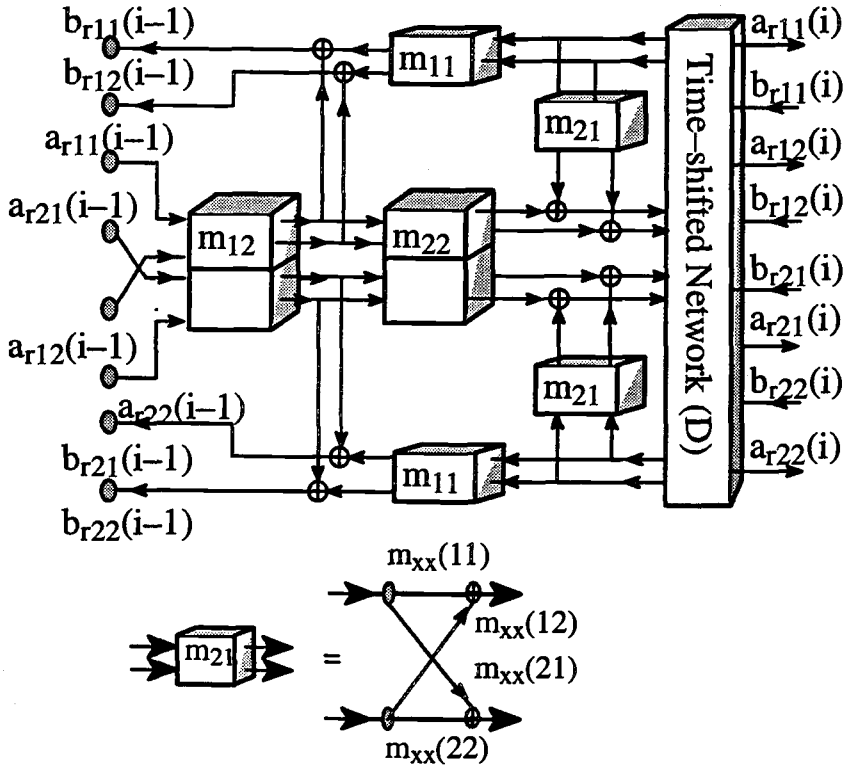
$$\begin{bmatrix} [b_r(i,t)] \\ [a_r(i,t)] \end{bmatrix} = \begin{bmatrix} [T'_{11}(i)] & [T'_{12}(i)] \\ [T'_{21}(i)] & [T'_{22}(i)] \end{bmatrix} \begin{bmatrix} [b_r(i+1,t)] \\ [a_r(i+1,t)] \end{bmatrix}, \tag{3.3}$$

$$\text{where} \begin{bmatrix} [T'_{11}(i)] & [T'_{12}(i)] \\ [T'_{21}(i)] & [T'_{22}(i)] \end{bmatrix} = \begin{bmatrix} [T_{11}(i)] & [T_{12}(i)] \\ [T_{21}(i)] & [T_{22}(i)] \end{bmatrix} \begin{bmatrix} [D] & [\emptyset] \\ [\emptyset] & [D^{-1}] \end{bmatrix}. \tag{3.4}$$

where $[D]$ and $[D^{-1}]$ represent the time delay and advanced element matrices.



(a) V_{rxx} : TDR/T measured waveforms



(b)

Figure 3.5, (a) The signal flow diagram of 2–D peeling algorithm.
(b) The signal flow diagram of control elements.

A basic cell of two–dimensional peeling algorithm is then expressed in terms of the transfer scattering matrix as,

$$\begin{bmatrix} [b_r(i,t)] \\ [a_r(i+1,t)] \end{bmatrix} = \begin{bmatrix} [I] & [\emptyset] \\ [\emptyset] & [D] \end{bmatrix} \begin{bmatrix} [m_{11}(i)] & [m_{12}(i)] \\ [m_{21}(i)] & [m_{22}(i)] \end{bmatrix} \times \begin{bmatrix} [D] & [\emptyset] \\ [\emptyset] & [I] \end{bmatrix} \begin{bmatrix} [b_r(i+1,t)] \\ [a_r(i,t)] \end{bmatrix} \tag{3.5}$$

The flow diagram of 2–D peeling algorithm including the scheme of multiport TDR/T measurements for the characterization of general coupled interconnect structures is shown in Figure 3.5–(a). The matrix elements for the ith section controller in Figure 3.5–(b) are given by

$$[m_{11}(i)]_{2x2} = [T_{11}(i)] - [T_{12}(i)][T_{22}(i)]^{-1}[T_{21}(i)], \tag{3.6}$$

$$[m_{12}(i)] = [T_{12}(i)][T_{22}(i)]^{-1}, \tag{3.7}$$

$$[m_{11}(i)] = -[T_{22}(i)]^{-1}[T_{21}(i)], \tag{3.8}$$

$$[m_{12}(i)] = [T_{22}(i)]^{-1}. \tag{3.9}$$

Further, the transfer scattering matrix element matrices can be expressed in terms of the normalized scattering element matrices as

$$[T_{11}(i)] = ([I] + [S_{11}(i)])^{-1}([I] + [S_{11}(i)] + [S_{22}(i)]), \tag{3.10}$$

$$[T_{21}(i)]_{2x2} = -[S_{22}(i)][[I] + [S_{11}(i)]]^{-1}, \tag{3.11}$$

$$[T_{12}(i)] = [S_{11}(i)]\,([I] + [S_{11}(i)])^{-1}, \tag{3.12}$$

$$[T_{22}(i)] = ([I] + [S_{11}(i)])^{-1} \tag{3.13}$$

where the normalized reflection scattering parameter matrices are defined by

$$[S_{11}(i)]_{2x2} = [b_r(i)][a_r(i)]^{-1}$$

$$= [Y(i)]^{(\frac{1}{2})}\{[[Y(i)] - [Y(i+1)]] \times [[Y(i)] + [Y(i+1)]]^{-1}\}[Y(i)]^{(\frac{-1}{2})}, \quad (3.14)$$

$$[S_{22}(i)]_{2x2} = [b_\ell(i)][a_\ell(i)]^{-1}$$

$$= [Y(i+1)]^{(\frac{1}{2})}\{[[Y(i+1)] - [Y(i)]] \times [[Y(i+1)] + [Y(i)]]^{-1}\}[Y(i+1)]^{(\frac{-1}{2})}, \quad (3.15)$$

$$[S_{21}(i)]_{2x2} = [Y(i)]^{(\frac{1}{2})}\{2[Y(i)] \times [[Y(i)] + [Y(i+1)]]^{-1}\}[Y(i)]^{(\frac{-1}{2})}, \quad (3.16)$$

$$[S_{12}(i)]_{2x2} = [Y(i+1)]^{(\frac{1}{2})}\{2[Y(i+1)] \times [[Y(i)] + [Y(i+1)]]^{-1}\}[Y(i+1)]^{(\frac{-1}{2})}. \quad (3.17)$$

The peeling algorithm is then formulated in terms of the 4x4 scattering transmission matrix of each section in a manner similar to the scalar case of a single line. This leads to the successive identification of each reflection coefficient matrix corresponding to change in admittance matrix from any section i to i+1 in cascaded coupled line model. The 2x2 characteristic admittance matrix elements of coupled piecewise uniform sections represented by $[Y(i+1)]$ for all value of i+1 are extracted in terms of the reflection coefficient matrix defined at each interface by,

$$[\rho_{i,i+1}]_{2x2} = \{[[Y(i)] - [Y(i+1)]] \times [[Y(i)] + [Y(i+1)]]^{-1}\}, \quad (3.18)$$

$$\text{where } [Y(i)] = \begin{bmatrix} y_{11}(i) & y_{12}(i) \\ y_{21}(i) & y_{22}(i) \end{bmatrix} \tag{3.19}$$

and the initial $[Y(i)]$ being diagonal representing the 50 Ω input terminations. The characteristic impedance matrix elements for each section are

$$[Z(i)] = \begin{bmatrix} z_{11}(i) & z_{12}(i) \\ z_{21}(i) & z_{22}(i) \end{bmatrix} = \begin{bmatrix} y_{11}(i) & y_{12}(i) \\ y_{21}(i) & y_{22}(i) \end{bmatrix}^{-1} \tag{3.20}$$

The above matrix elements characterize the coupled interconnect four ports. These elements can also be used to extract circuit models by using the same procedure as that for the single line case [27].

3.2.2 Lumped/Hybrid Element Modeling Of Coupled Line Structures

For the case of general two coupled lines, the coupled transmission line equations are given by

$$\frac{\partial}{\partial z}\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = -\begin{bmatrix} L_1 & L_m \\ L_m & L_2 \end{bmatrix}\begin{bmatrix} \frac{\partial i_1}{\partial t} \\ \frac{\partial i_2}{\partial t} \end{bmatrix} \tag{3.21}$$

$$\frac{\partial}{\partial z}\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = -\begin{bmatrix} C_1 + C_m & -C_m \\ -C_m & C_2 + L_{Cm} \end{bmatrix}\begin{bmatrix} \frac{\partial v_1}{dt} \\ \frac{\partial v_2}{\partial t} \end{bmatrix} \tag{3.22}$$

where L_1, L_2, C_1, C_2, L_m and C_m are all functions of position z.

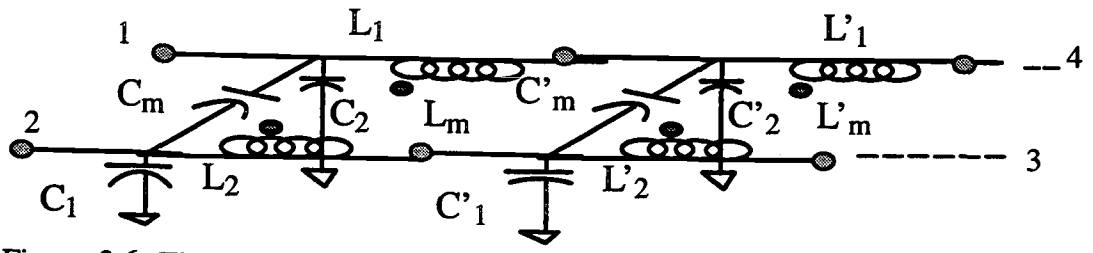


Figure 3.6, The cascaded lumped element model of a general coupled lines.

The incremental lumped element values are obtained from the cascaded coupled impedance line sections for a general coupled interconnection structure. The coupled line sections are extracted by two–dimensional peeling algorithm from two–port time domain measurements described at the last section, then the distributed elements of each coupled line sections are replaced by the coupled lumped element model with the corresponding self– and mutual–capacitances and inductances as shown in Figure 3.6. The transmission voltage at line 1 and the coupled voltage at line 2 can be readily obtained by computing the total [ABCD] matrix of the cascaded four–port network (Appendix B) or by using a general circuit simulators such as SPICE.

For the electrically short interconnection structure, the lumped as well as hybrid lumped/distributed model as shown in Figure 3.7 and Figure 3.8 can also be constructed from time domain profiles of the elements of the characteristic impedance and admittance matrices. The values of coupled lumped elements corresponding to a given time duration $[t_a, t_b]$ are found in the same manner as for single interconnects [27]. Integrating the characteristic impedance elements leads to self and mutual inductances whereas, integrating the characteristic admittance matrix elements gives self and mutual capacitance matrix elements, i.e.,

$$L_{ij} = \int_{t_a}^{t_b} Z_{ij}\, dt \quad \text{and} \quad C_{ij} = \int_{t_a}^{t_b} Y_{ij}\, dt \,. \tag{3.23}$$

Integration over the entire time period gives a single section lumped element model valid for short interconnections or low frequencies.

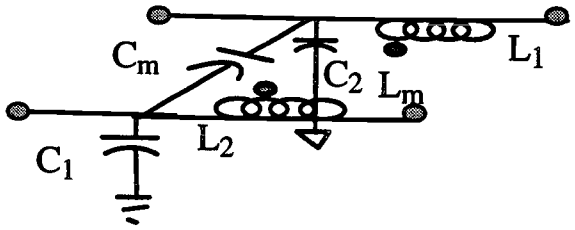


Figure 3.7, Lumped element model of coupled interconnects.

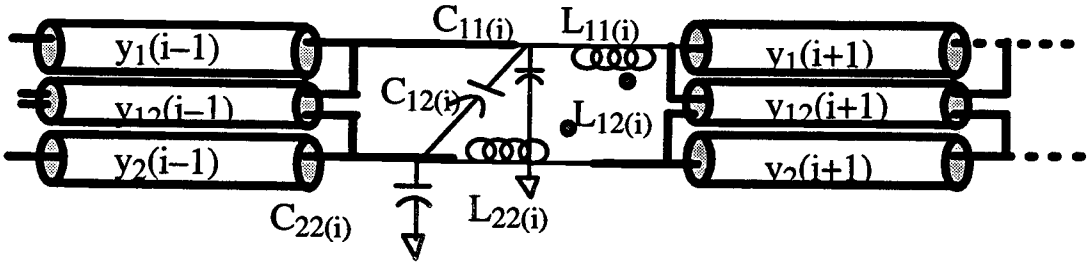


Figure 3.8, Hybrid lumped/distributed model of general coupled interconnects.

3.3 Experimental Results

An example is given here to illustrate the technique and the results. Figure 3.9 shows the layout of an asymmetrical coupled inhomogeneous interconnect structure. The test fixture was made on FR–4 epoxy glasses dielectric material.

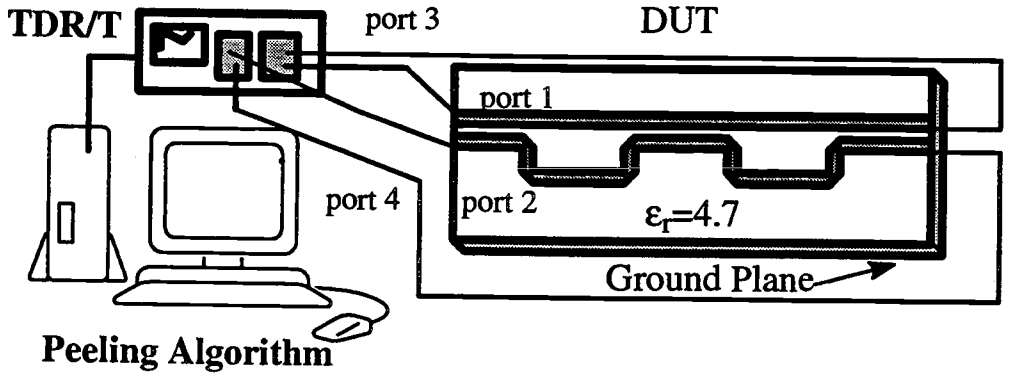
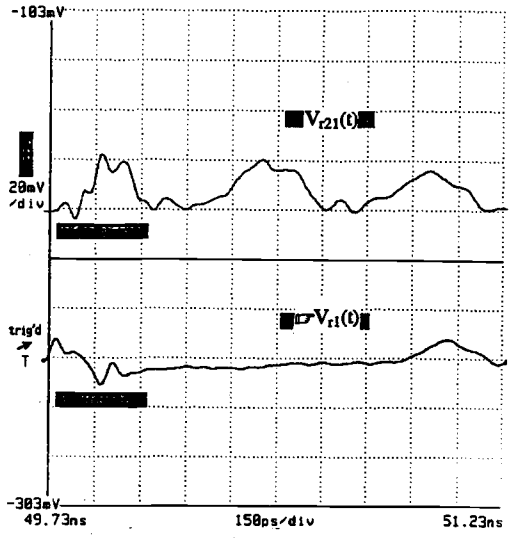
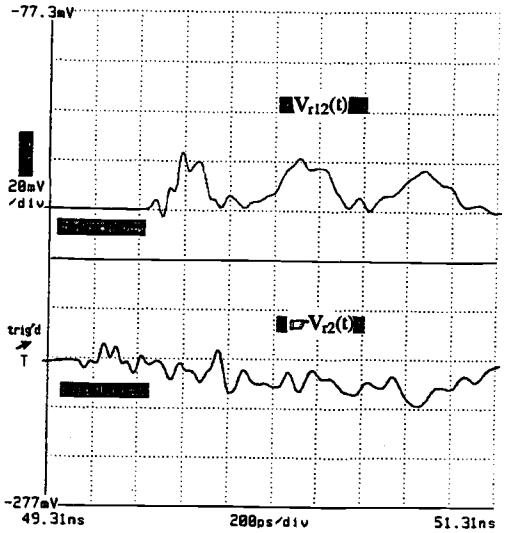


Figure 3.9, The test fixture of an asymmetrical coupled inhomogeneous interconnects.

A 28ps rise time step–like waveform is are measured as shown in Figure 3.10–(a). Figure 3.10–(b) shows the measured TDR/T results for $V_{r2}(t)$ and $V_{r12}(t)$ by exciting port 2 and measuring reflection at that port and transmission at port 1. It is noted that the reflected waveform $\rho_{21}(t)$ is identical to $\rho_{12}(t)$. The admittance matrix [Y(t)] and impedance matrix [Z(t)] are then extracted from the measured reflection coefficient matrix [ρ(t)] by using two dimensional peeling technique. These profiles are in a form of admittance/impedance vs. time in the wave propagation direction and are shown in Figure 3.11–(a) and Figure 3.11–(b), respectively.



(a)



(b)

Figure 3.10, (a) Excitation signal at port 1, and the reflected waveform ($V_{r1}(t)$) at that port and the transmitted waveform ($Vr_{21}(t)$) at port 2 terminated in 50 (ohms). (b), Excitation signal at port 2, and the reflected waveform ($V_{r2}(t)$) at that port and the transmitted waveform ($Vr_{12}(t)$) at port 1 terminated in 50 (ohms).

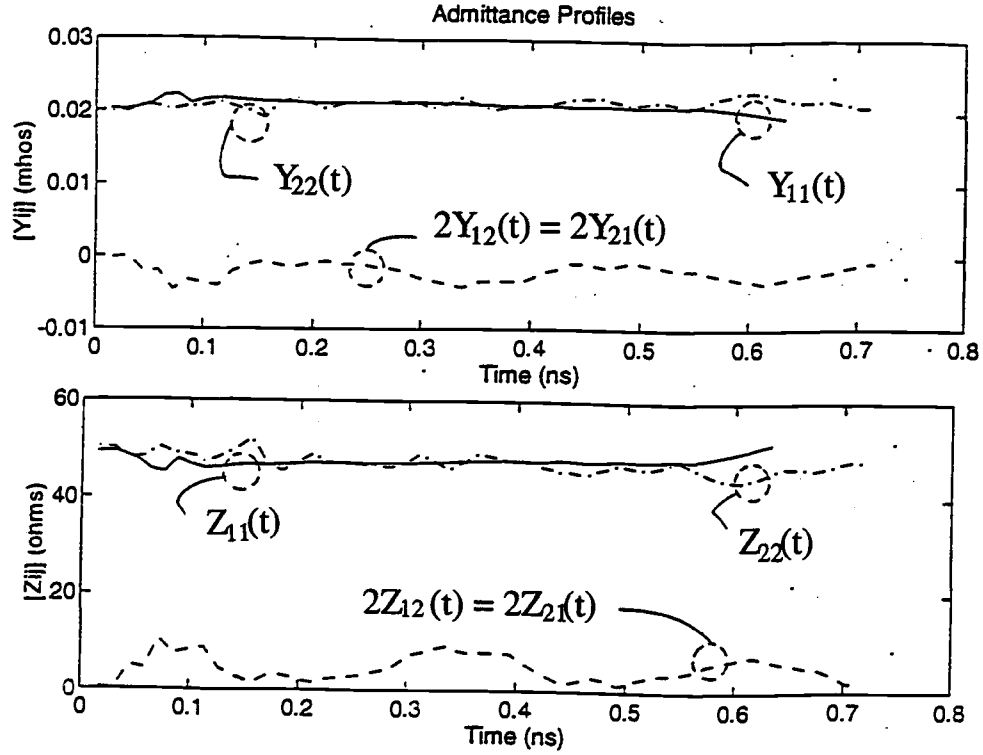


Figure 3.11, (a) Admittance profiles. (b) Impedance profiles of coupled interconnects.

The total self and mutual capacitances and inductances associated with the interconnects can be calculated from the extracted characteristic admittance and impedance profiles. These are given below together with the theoretical predictions based on coupled microstrip and bend models [28].

$$[L]_{exp.} = \begin{bmatrix} 30.92 & 1.44 \\ 1.44 & 35.72 \end{bmatrix} \text{nH}, \quad [C]_{exp.} = \begin{bmatrix} 12.66 & -0.39 \\ -0.39 & 15.98 \end{bmatrix} \text{pF},$$

$$[L]_{cal.} = \begin{bmatrix} 31.88 & 1.70 \\ 1.70 & 37.82 \end{bmatrix} \text{nH} \quad \text{and} \quad [C]_{cal.} = \begin{bmatrix} 11.92 & -0.36 \\ -0.36 & 16.61 \end{bmatrix} \text{pF}.$$

The second example is to characterize and model the coupled interconnection structures in a plastic leadless chip carrier (PLCC) package. The first task was to design or modify a test fixture consisting of controlled impedance interconnects as shown in Figure 3.12, so that the package parameters can be extracted from the

measurement of package–fixture assembly. After the transmission line stubs in the existing test fixture were removed, we could apply our deconvolution algorithm to extract the electrical parameters of PLCC package from the TDR/T data.

Figure 3.13 shows the TDR measured reflection voltage for Pin #1 of PLCC package. Lumped element model consisting of total inductance and capacitance is then readily computed from the extracted impedance profile. The coupling between interconnects is characterized by mutual terms which can be obtained by using a two–dimensional peeling algorithm. Figure 3.14 shows the self– and mutual impedance profiles extracted from two port time domain measured data for Pin #1 and #2. The simulated crosstalk for the extracted model compared with the measured crosstalk shown in Figure 3.15 is in a good agreement for the model of coupled interconnects which is based on the cascaded coupled transmission line model. The total self– and mutual–inductance and capacitance are then obtained from the extracted self–and mutual–impedance profiles and the resulting lumped element model is shown in Figure 3.16.

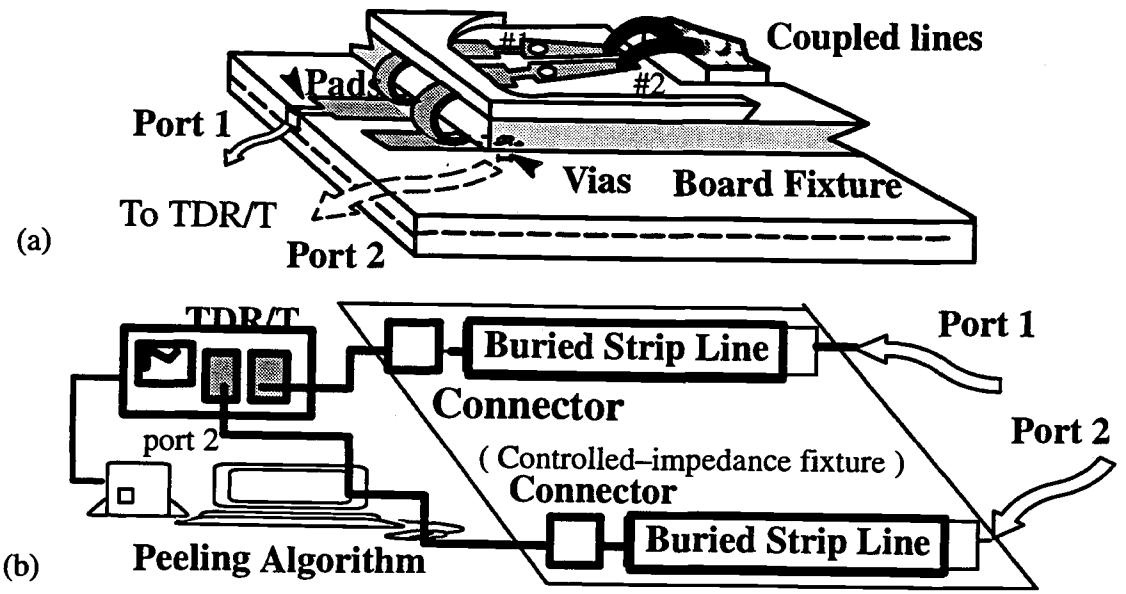


Figure 3.12, (a) Coupled lines in a PLCC package with the associated board fixture. (b) TDR/T set up with the controlled–impedance test fixture for PLCC package.

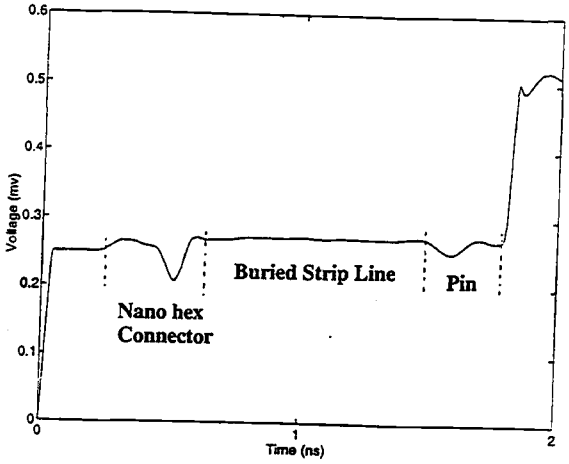


Figure 3.13, The measured TDR response for Pin #1.

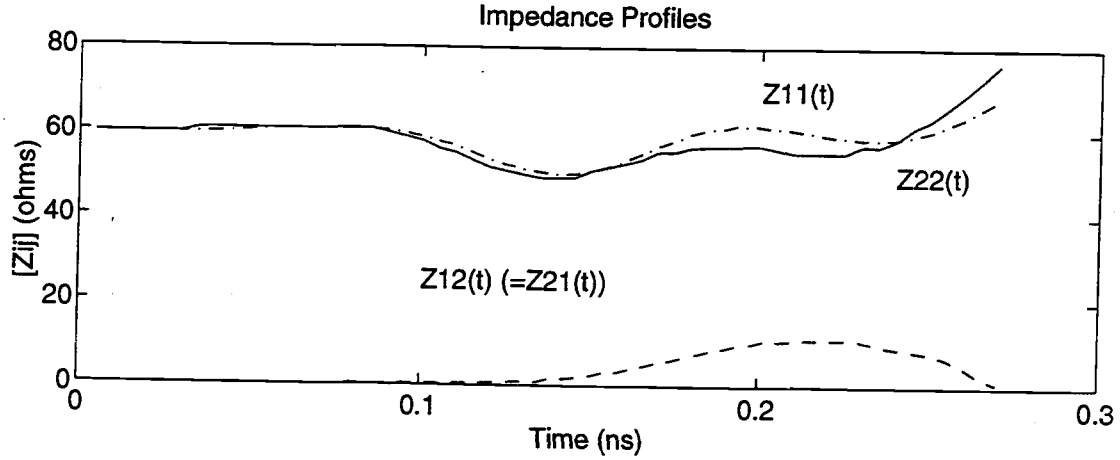


Figure 3.14, The self– and mutual–impedance profiles extracted from the TDR/T measured data by using two–dimensional peeling algorithm.

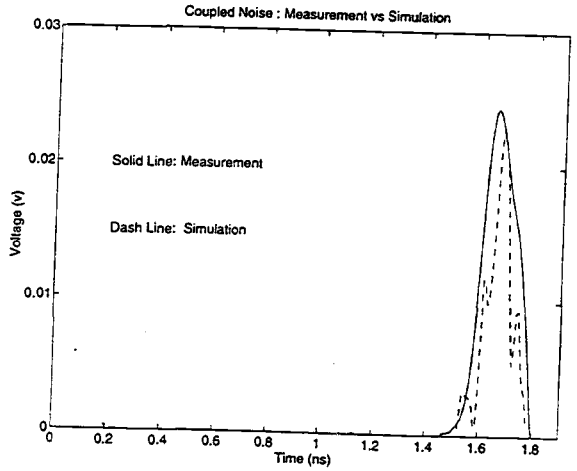


Figure 3.15, The simulated and measured crosstalk noise in a PLCC package.

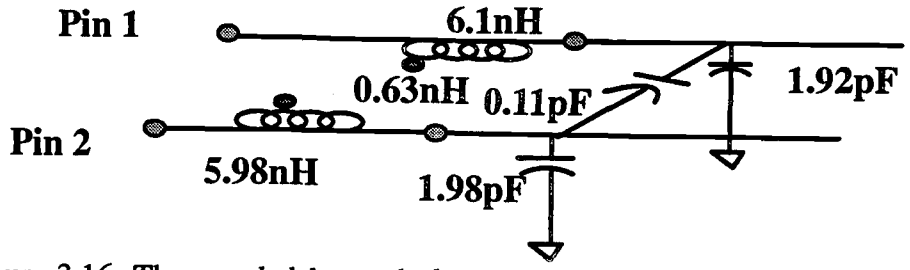


Figure 3.16, The coupled lumped element model.

3.4 Summary

In conclusion, a two dimensional layer peeling algorithm for the time domain modeling of coupled interconnects and discontinuities in terms of cascaded uniform coupled transmission line sections is presented. Lumped as well as hybrid lumped/ distributed models including the coupling elements are readily extracted from the impedance profiles facilitating the design of integrated circuits and chip modules.

4. IMPEDANCE–LOSS PROFILE CHARACTERIZATION OF INTERCONNECTION STRUCTURES

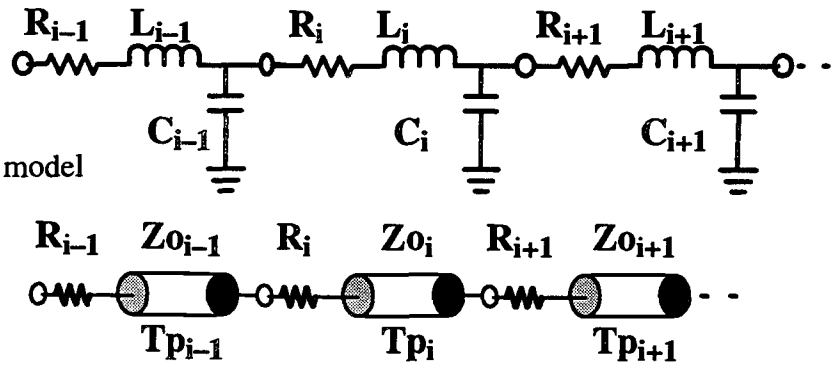
An experimental method for the time domain characterization and circuit modeling of lossy, nonuniform, interconnection structures is presented in this chapter. The technique is based on the extended dynamic deconvolution algorithm (peeling algorithm) which is modified to include loss elements. Equivalent circuit models for resistive lossy interconnection structures are extracted from time domain reflection and transmission measurements by using this extended algorithm. The simulated results for the extracted models compared with the measured data for interconnects associated with a thin film package are used to validate the accuracy of the model.

4.1 Introduction

As the modern integrated circuits and devices evolve toward higher operating frequencies and smaller physical structures, the need for small dimensional interconnections and high speed packaging technologies also increases in order to match the requirements for high performance system design. High density packages, such as small thin conductors on board level packages, and thin film single– and multi–chip modules (MCMs), offer alternative solutions to high performance electronic packaging [29]. This reduction in interconnect cross section, however, leads to an increase in line resistance. This high line resistance loss results in increased signal loss, delay, distortion and a decrease in noise immunity as the signal passes through the interconnections. In order to guarantee circuit functions that operate correctly, accurate characterization and circuit modeling of interconnection structures are necessary for designers to incorporate interconnect parasitic effects during the design phase for circuits and systems.

In recent years, several attempts at experimental techniques for the characteriza-

tion of interconnections and packages have been reported [30–35]. The technique based on one and two–dimensional peeling algorithms (dynamic deconvolution) have been developed to characterize general interconnection structures from time domain measurements [5,26,27,30,31]. However, this technique has been limited to impedance profile determination of low–loss or lossless structures, whereas other techniques focusing on precise characterization of uniform lossy transmission line have also been reported [32–35,67–70]. In this chapter, the lossless peeling algorithm is extended to extract impedance–loss profiles from the combination of reflection and transmission time domain measurements for a general nonuniform resistive lossy interconnects.



(a) RLC element model

(b) Resistive Transmission line model

Figure 4.1, Equivalent circuit models for a lossy interconnection.

4.2 Lossy Line Peeling Algorithm

4.2.1 Equivalent Circuit Model

Figure 4.1–(a) shows basic RLC element model for a lossy transmission line. The model is assumed to be a type of interconnection structures where the dielectric loss is small compared to line resistance loss. For this case, the resistive transmission line model with hybrid elements shown in Figure 4.1–(b) is used to characterize general lossy interconnections. The model is based on a ladder equivalent circuit consisting of RLC elements in which L and C elements are replaced by an ideal

transmission line [36]. A complete resistive transmission line model is then constructed by cascaded resistive transmission line sections consisting of resistance elements and uniform transmission line segments. The relationship between electrical parameters of the resistive transmission line model and the RLC element model are given by

$$L_i = Tp_i Zo_i \tag{4.1}$$

$$\text{and } C_i = \frac{Tp_i}{Zo_i} . \tag{4.2}$$

where L_i and C_i are inductance and capacitance per unit length respectively, corresponding to the ith section of the RLC element model, Tp_i and Zo_i are propagation delay time and the characteristic impedance respectively, corresponding to the ith section of the resistive transmission line model.

4.2.2 Peeling Algorithm

The schematic of a general interconnection structure consisting of lossless interconnections and a lossy interconnection is shown in Figure 4.2. The general structure is assumed to be a type that can be represented by cascaded distributed and hybrid models for general uniform and nonuniform interconnections (NUIs). The general nonuniform lossless interconnection portion is modeled by cascaded uniform transmission line segments as shown in Figure 4.3–(a), whereas the lossy interconnection portion is model by cascaded resistive transmission line segments with constant delay, loss and impedance elements as shown in Figure 4.3–(b). The delay of the segments is selected to adequately sample the structure and therefore its response.

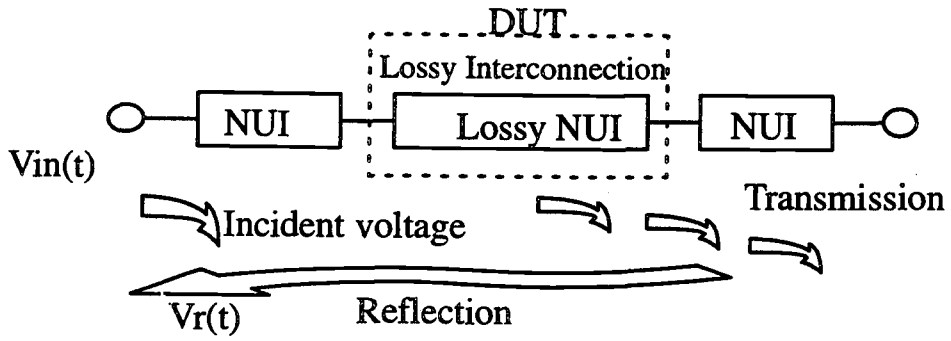


Figure 4.2, A general interconnection structure consisting of lossless and lossy interconnects.

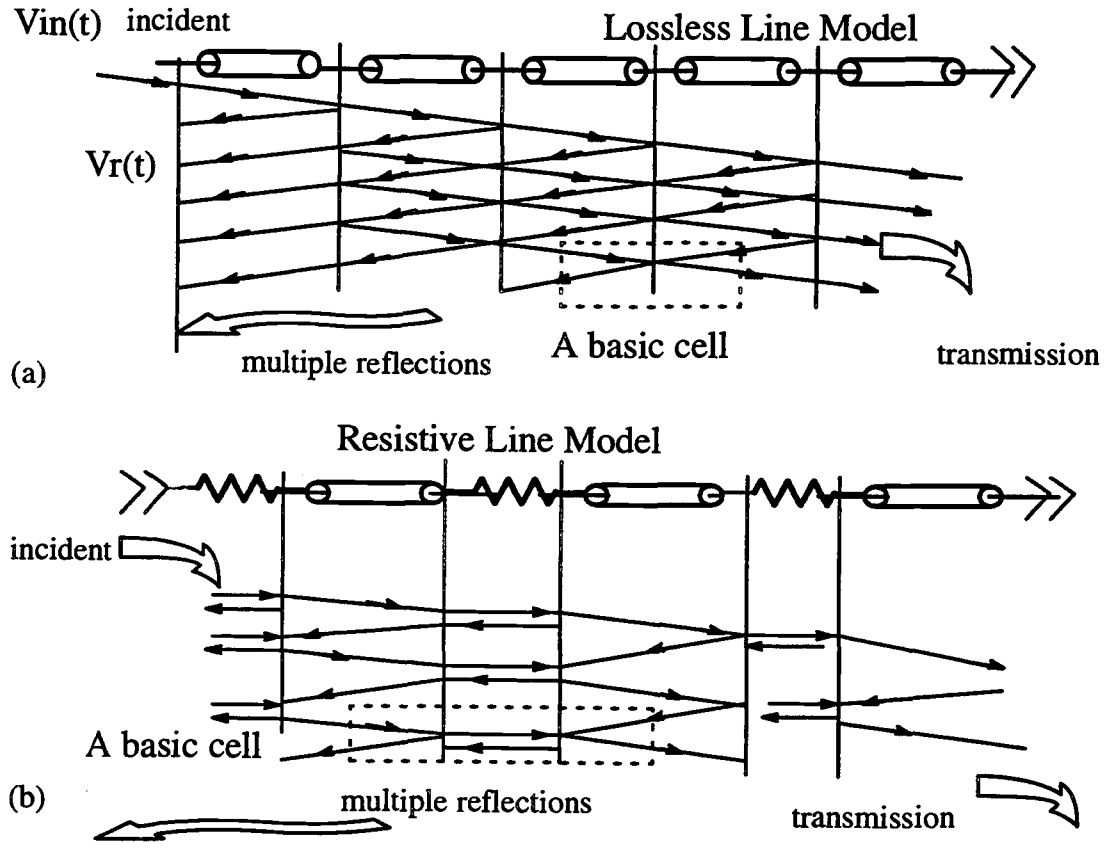


Figure 4.3, (a) Lossless interconnection modeled by cascaded transmission line sections. (b) Lossy interconnection modelled by cascaded resistive transmission line sections.

In a lossless structure the TDR response is used to obtain the impedance of an

initial segment. The effects of the initial segment are then removed, or de–embedded, from the measured initial reflection response leaving the data which is equivalent to the direct measurement of reflection response at the next segment. The procedure can be formulated in terms of the scattering parameters as shown in Figure 4.4–(a) and implemented by the transfer scattering matrix–based algorithm given in chapter 1. All calculations are performed in the time domain using scalar multiplication and time shift or delay. However, when losses are presented, the reflection data does not provide sufficient information to fully characterize the cascaded segments. Additional information is required from transmission measurements for the determination of characteristic impedances and resistance values.

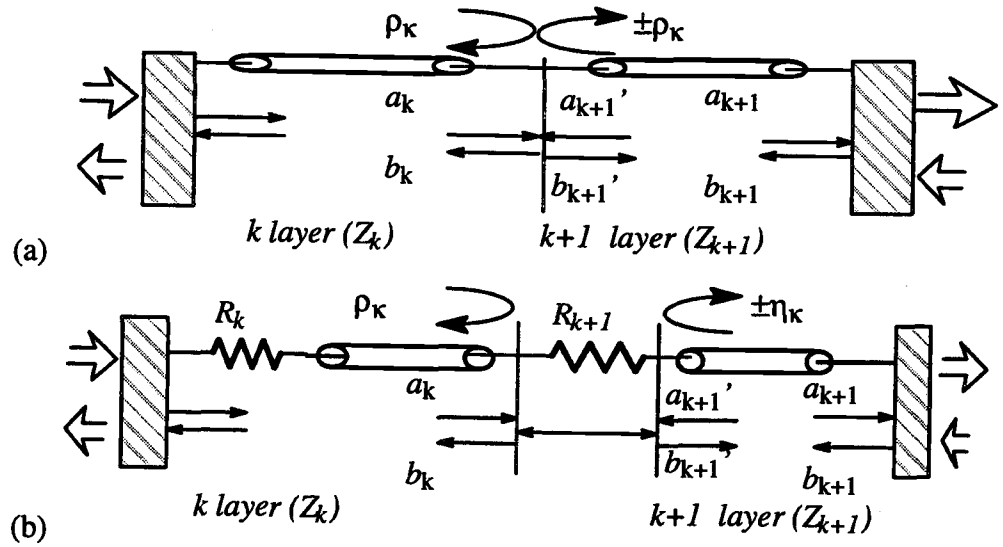


Figure 4.4, (a) The schematic scattering parameters for the cascaded transmission line model. (b) The schematic scattering parameters for the cascaded resistive transmission line model.

Figure 4.4–(b) shows a lossy interconnection modeled by cascaded resistive transmission line sections. A system equation derived from the general transmission line equation is used to describe such a section in terms of the local normalized incident "a" and reflected "b" parameters as given by (Appendix C)

$$\frac{\partial}{\partial x}\begin{bmatrix} a(x,t) \\ b(x,t) \end{bmatrix} = \begin{bmatrix} -\frac{\partial}{\partial t} & -\eta(x) \\ -\rho(x) & \frac{\partial}{\partial t} \end{bmatrix} \begin{bmatrix} a(x,t) \\ b(x,t) \end{bmatrix}, \tag{4.3}$$

where $\rho(x)$ and $\eta(x)$ are defined as the local forward and backward reflectivity parameters respectively, and are given by two functional relations between the local resistance R, impedance Zo and time delay constant Tp at the position x for a resistive lossy interconnection. This system equation is then used to derive the peeling algorithm in the same manner as that for the lossless case.

In a procedure similar to the peeling algorithm for lossless interconnections, a basic cell of resistive lossy line peeling algorithm can be obtained from equation (4.3) and is then cascaded repeatedly through the length of the structure as shown in Figure 4.5–(a), where D is the time delay operator, and the control elements m_{ij} of kth basic cell are obtained from the scattering matrix at the interface of the cascaded resistive transmission line sections as shown in Figure 4.6. The scattering matrix elements are given by

$$S_{11}(k) = \frac{[Zo(k+1) + R(k+1)] - Zo(k)}{[Zo(k+1) + R(k+1)] + Zo(k)} \tag{4.4}$$

$$S_{22}(k) = \frac{[Zo(k) + R(k+1)] - Zo(k+1)}{[Zo(k) + R(k+1)] + Zo(k+1)} \tag{4.5}$$

$$S_{12}(k) = \frac{2\,Zo(k)}{[Zo(k+1) + R(k+1)] + Zo(k)} \sqrt{\frac{Zo(k+1)}{Z(k)}} \tag{4.6}$$

$$S_{21}(k) = \frac{2\,Zo(k+1)}{[Zo(k+1) + R(k+1)] + Zo(k)} \sqrt{\frac{Zo(k)}{Z(k+1)}} \tag{4.7}$$

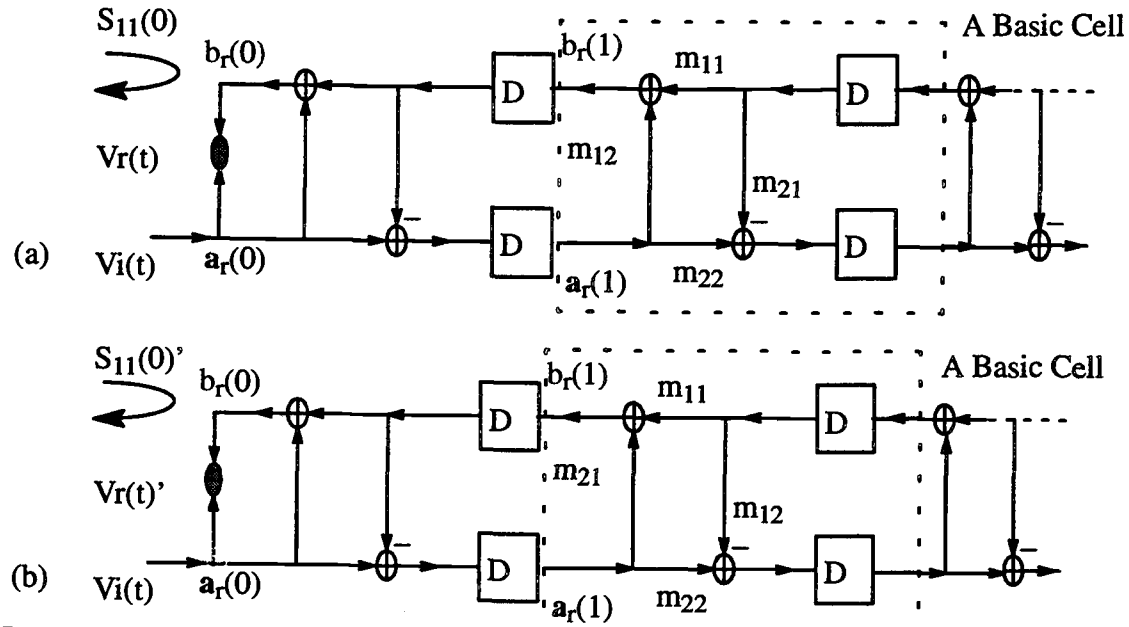


Figure 4.5, (a) The causal signal flow diagram of the peeling algorithm. (b) The causal signal flow diagram of the peeling algorithm for the virtual system.

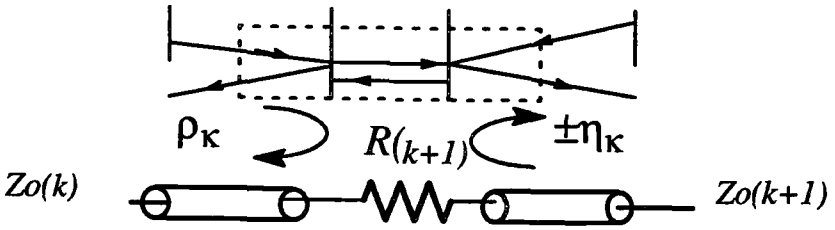


Figure 4.6, The reflection and transmission flow diagram.

The transfer scattering matrix is then given by

$$[T(k)] = \begin{bmatrix} T_{11}(k) & T_{12}(k) \\ T_{21}(k) & T_{22}(k) \end{bmatrix} = \frac{1}{S_{21}(k)} \begin{bmatrix} -\det|S(k)| & S_{11}(k) \\ -S_{22}(k) & 1 \end{bmatrix}$$

$$= \Delta \begin{bmatrix} \dfrac{[Zo(k+1)+Zo(k)]^2 - R^2(k+1)}{[Zo(k+1)+R(k+1)+Zo(k)]^2} & \dfrac{Zo(k+1)+R(k+1)-Zo(k)}{[Zo(k+1)+R(k+1)+Zo(k)]} \\ \dfrac{Zo(k+1)-R(k+1)-Zo(k)}{[Zo(k+1)+R(k+1)+Zo(k)]} & 1 \end{bmatrix} \quad (4.8)$$

$$\text{where } \Delta = \frac{Zo(k) + Zo(k+1) + R(k+1)}{2\sqrt{Zo(k) \times Zo(k+1)}}$$

Further, the inverse transfer scattering matrix is also obtained as

$$[T(k)]^{-1} = \Delta \begin{bmatrix} 1 & -\eta_k \\ -\rho_k & \dfrac{[Zo(k+1) + Zo(k)]^2 - R^2(k+1)}{[Zo(k+1) + R(k+1) + Zo(k)]^2} \end{bmatrix}$$

$$= \begin{bmatrix} \dfrac{Zo(k) + Zo(k+1) + R(k+1)}{\Lambda} & \dfrac{Zo(k+1) + R(k+1) - Zo(k)}{\Lambda} \\ \dfrac{Zo(k+1) - R(k+1) - Zo(k)}{\Lambda} & \dfrac{[Zo(k+1) + Zo(k)]^2 - R^2(k+1)}{\Lambda[Zo(k+1) + R(k+1) + Zo(k)]} \end{bmatrix} \tag{4.9}$$

$$\text{where } \Lambda = 2\sqrt{Zo(k) \times Zo(k+1)}\,. \tag{4.10}$$

In the above expression, the forward and backward reflection coefficients are:

$$\rho_k = \frac{Zo(k+1) - R(k+1) - Zo(k)}{[Zo(k+1) + R(k+1) + Zo(k)]} \tag{4.11}$$

$$\text{and } \eta_k = \frac{Zo(k+1) + R(k+1) - Zo(k)}{[Zo(k+1) + R(k+1) + Zo(k)]}\,. \tag{4.12}$$

The control elements m_{ij} of kth basic cell are then given by

$$m_{11(k)} = m_{22(k)} = \sqrt{1 - \eta_k \rho_k}\,, \tag{4.13}$$

$$m_{12(k)} = \rho_k\,, \tag{4.14}$$

$$m_{21}(k) = \eta_k\,, \tag{4.15}$$

for $Zo(k) + Zo(k+1) > R(k+1), k = 0, 1, 2, \ldots..n)$.

ρ_k and η_k are readily obtained at each step of the peeling process once the distributed series resistances given by TDT measured data or computation are assigned to the model.

Therefore, the extended peeling algorithm for the resistive line is summarized as,

[1] Compute $\rho_k \Rightarrow \quad \rho_k = \frac{B(k,1)}{A(k,1)}$,

where B(k) and A(k) denote the reflection and incident functions obtained from k+1 peeling step.

[2] Extract Zo(k+1) from equations (4.11) and (4.12),

where R(k+1) is the TDR/T measured resistance.

[3] Compute $[m_{xx}(k)]$ from ρ_k and η_k from equations (4.13) – (4.15).

[4] Propagate [B,A] by using equation (4.9) to the next section and go to step [1].

For the case of unknown resistances, ρ_k and η_k are computed from the measured reflection data $S_{11}(0)$ together with the computational reflection data $S_{11}(0)$' obtained from the TDR/T responses of the DUT as shown in Figure 4.4–(b). The relation between the scattering parameter matrix of the virtual system [S'] and the measured data of the DUT is given by [76]

$$S'_{11}(0) = [S']_{21} \tag{4.16}$$

$$\text{where } [S'] = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} [S]^{-1} \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}, \tag{4.17}$$

$$\text{and } \begin{bmatrix} b_2 \\ b_1 \end{bmatrix} = [S]^{-1} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}. \tag{4.18}$$

The computational process involves a coupled peeling algorithm that can be formulated in terms of the transfer scattering matrix [T] of each resistive transmission line model as given by

$$\begin{bmatrix} B'(k+1,t) \\ A'(k+1,t) \end{bmatrix} = [D^{-1}][T'^{-1}] \begin{bmatrix} B'(k,t) \\ A'(k,t) \end{bmatrix}, \tag{4.17}$$

$$\begin{bmatrix} B(k+1,t) \\ A(k+1,t) \end{bmatrix} = [D^{-1}][T^{-1}] \begin{bmatrix} B(k,t) \\ A(k,t) \end{bmatrix}, \tag{4.18}$$

$$\rho_k = \frac{B(k)}{A(k)} \text{ and } \eta_k = \frac{B(k)'}{A(k)'} . \qquad (4.19)$$

B(k) and A(k) denote the reflection and incident functions obtained from k+1 peeling step, respectively, and so B(k)' and A(k)' denote the reflection and incident functions corresponding to the virtual system, respectively. The recursive procedure is similar to the case of the lossless line [27] leading to the successive identification of each local forward and backward reflection coefficients with the associated impedances and resistances.

Therefore, the lossy peeling algorithm is:

(1) Compute ρ_k and $\eta_k \Rightarrow \quad \rho_k = \frac{B(k,1)}{A(k,1)}, \qquad \eta_k = \frac{B'(k,1)}{A'(k,1)}$.

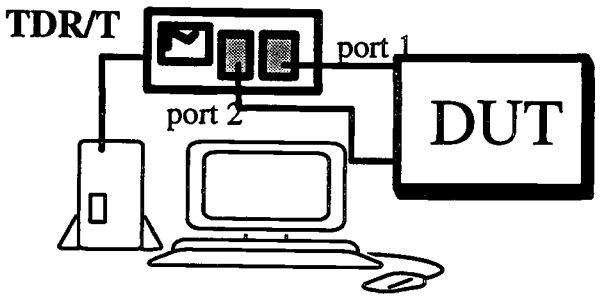
(2) Extract Zo(k+1), Rd(k) for the given initial Zo(0)
from equations (4.11) and (4.12).

(3) Compute $[m_{xx}(k)]$ from ρ_k and η_k by using equations (4.13) – (4.15).

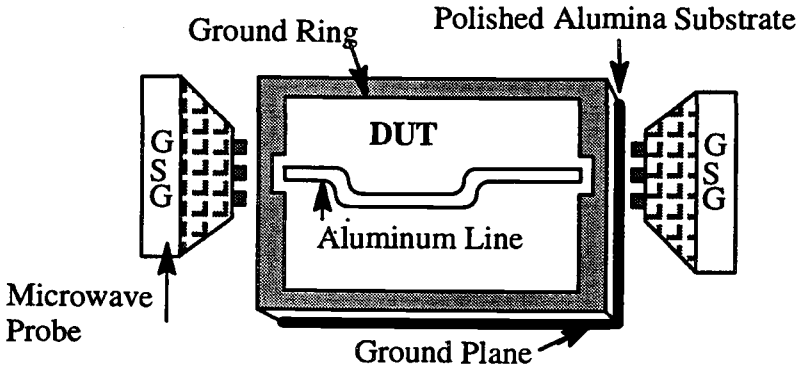
(4) Propagate [B,A] and [B',A'] by using equation (4.9) to the next section and go to step (1).

4.3 Results

The device under test (DUT) studied in this chapter is a thin film microstrip interconnection made on 99.5% polished and 0.01" thick alumina substrate. The conductor is aluminum with 4–8 μm thickness and 0.01" trace width, and the back of substrate is fully covered with aluminum to form a ground plane. To consider the requirement of high speed measurements, aluminum is also deposited on the substrate edges to create wraparound connection for ground probe pads. The TDR/T measurement set–up together with the test line is shown in Figure 4.7.



(a)



(b)

Figure 4.7, (a) The schematic TDR/T measurement set–up. (b) The schematic thin film microstrip line with the test probes.

The interconnection structure to be characterized and modeled shown in figure 4.7–(b) is a thin film microstrip line with 2 bends. Tektronix 11801A TDR/T system with TMP9625 Microwave Probe is used to measure the reflection and transmission responses. The measured resistance per unit length from TDT data is 1.48 (Ω/cm) and is then uniformly distributed in the lossy line model. The extracted impedance profile by using lossy line peeling algorithm for the cascaded resistive transmission line sections, together with the impedance profile obtained from lossless line peeling algorithm, are shown in Figure 4.8. The circuit model to be simulated consists of a microstrip line with the associated high frequency test fixture. The simulated reflection waveforms of lossy non uniform line model (Lossy NTL) and lossless non uniform line model (Lossless NTL) and the measured TDR data are shown in Figure 4.9–(a). However, the accuracy and the utility of the lossy NTL model is demon-

strated by comparing the simulated transmission data with the measured TDT data as shown Figure 4.9–(b).

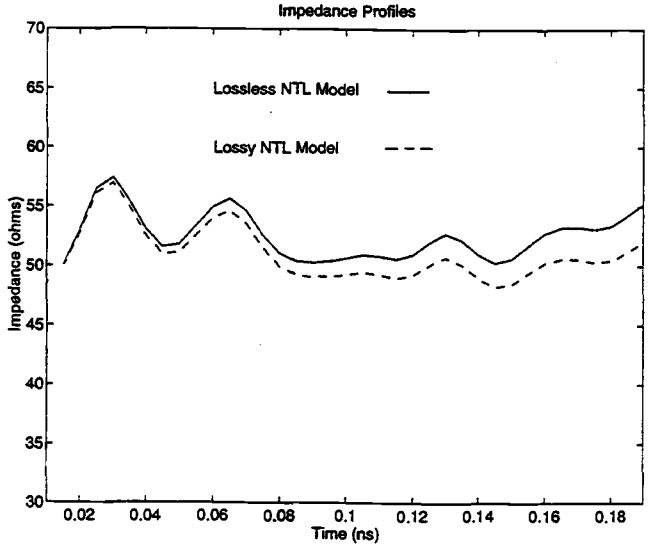


Figure 4.8, The extracted impedance profiles by using lossless and lossy peeling algorithms.

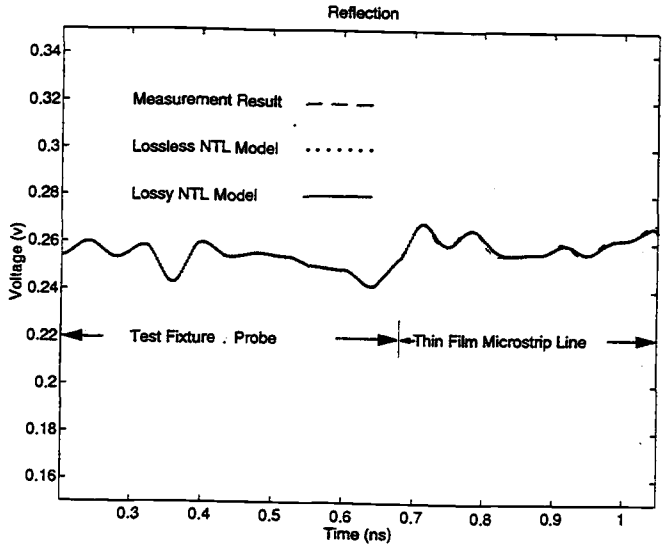


Figure 4.9, (a) The measured reflection data and the simulated reflection data of lossless and lossy nonuniform transmission line models.

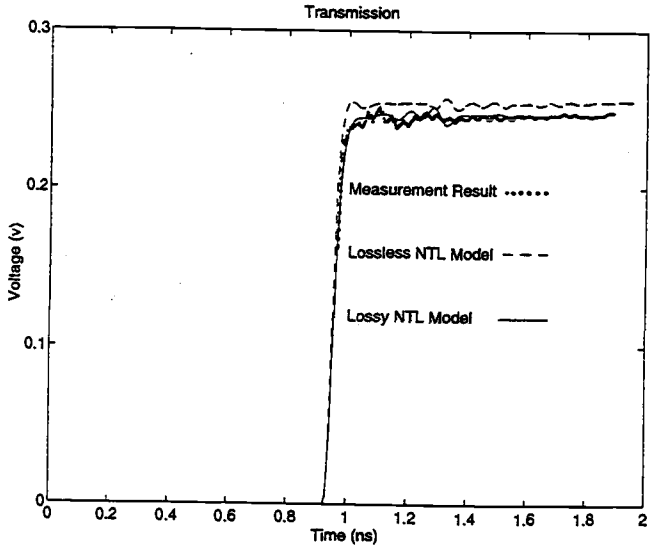


Figure 4.9, continued, (b) The measured transmission data and the simulated transmission data of lossless and lossy nonuniform transmission line models.

As the second example, the schematic interconnection structure is shown in Figure 4.10. A scale of probe pad detail together with test pattern is shown in Figure 4.11–(a) and (b) respectively. The test line is an otherwise uniform microstrip line with 20 right angle bend discontinuities. Again, a Tektronix 11801A TDR/T system with TMP9625 Microwave Probes is used to measured time domain reflection and transmission responses. The measured resistance per unit length from TDT data is 1.4 (Ω/cm) and is readily placed into the resistive transmission line model.

The circuit model of the DUT consists of 50 cascaded resistive transmission line sections. The impedance of each transmission line segment is then extracted from the time domain measured data by using the lossy line peeling algorithm. In Figure 4.12–(a) and (b), the simulated waveforms from the lossy nonuniform transmission line model are compared with the measured data for time domain reflection and transmission responses. The result shows a good agreement and hence assures the validity of the resistive transmission line model.

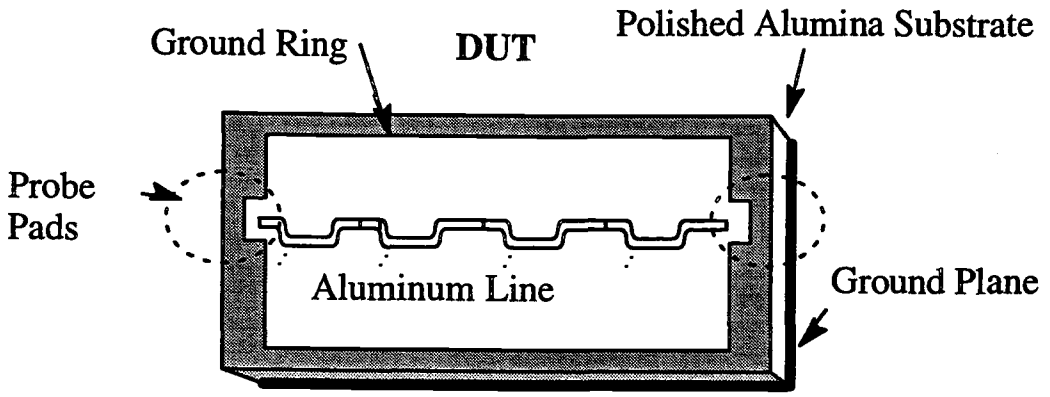
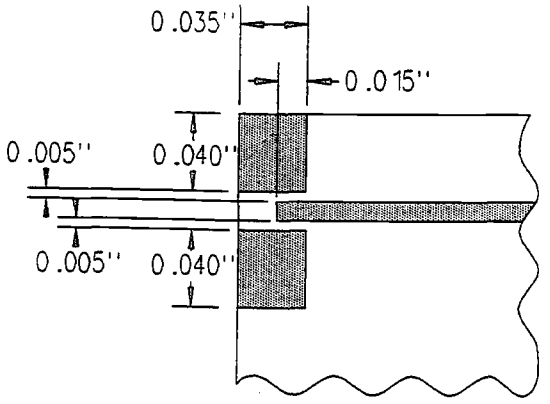
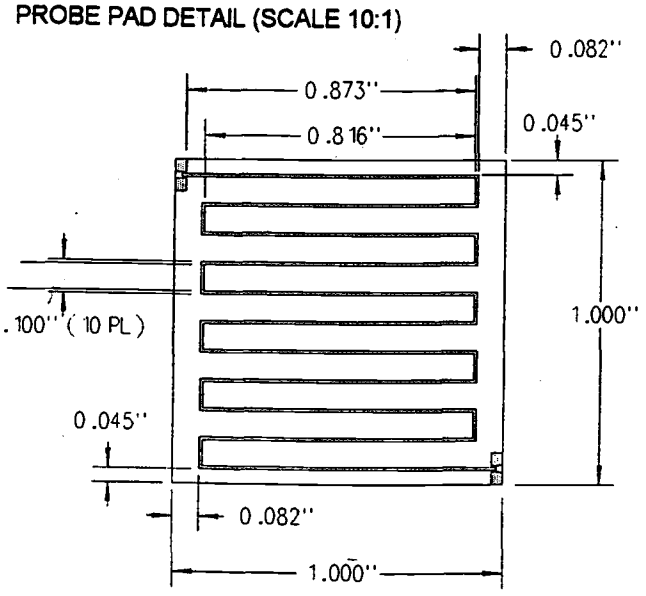


Figure 4.10, A schematic of test fixture.

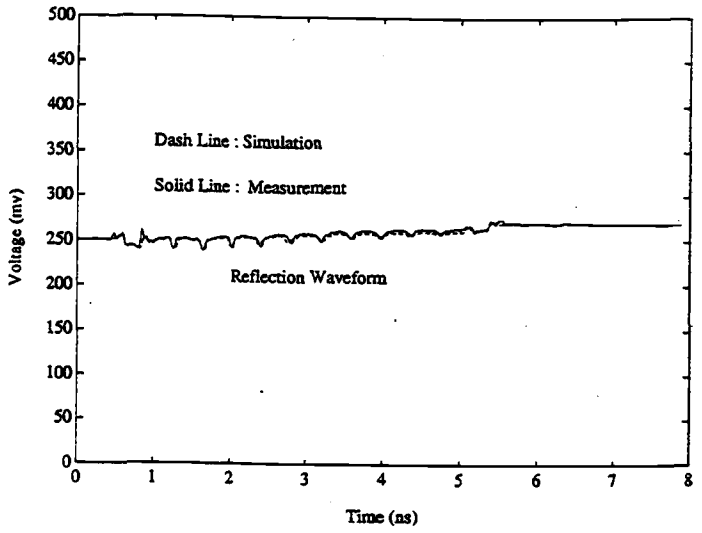


(a)

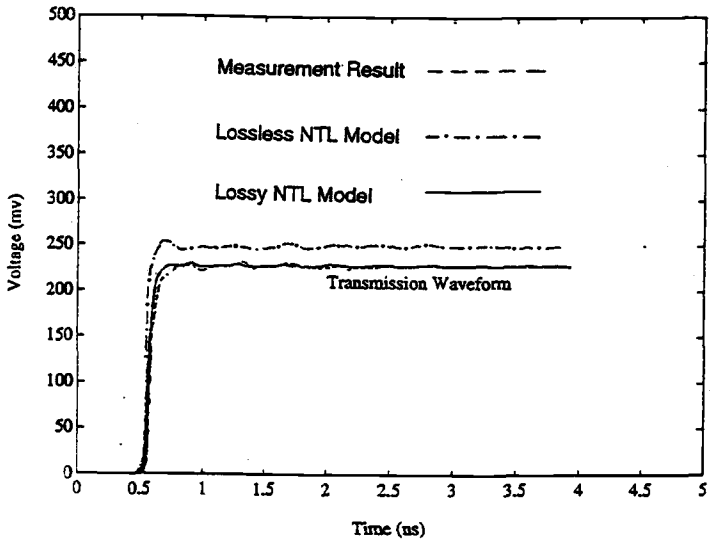


(b)

Figure 4.11, (a) Probe pad detail. (b) Test pattern of microstrip line on thin film package.



(a)



(b)

Figure 4.12, (a) The simulated reflection response of resistive lossy line model and the measured time reflection response for the microstrip test pattern in Figure 4.10. (b) The simulated transmission response together with the measured transmission response.

4.4 Summary

In conclusion, a TDR/T measurement based technique for impedance–loss profiling and characterization of general non uniform lossy interconnections on thin film packages has been presented. The characteristic impedances and resistances associated with resistive transmission line segments are extracted from time domain reflection and transmission responses by using a peeling algorithm formulated for resistive lossy lines. The proposed time domain measurement based technique should be useful in characterizing and modeling general uniform and non uniform resistive lossy interconnections and other quasi–TEM structures in high speed and RF circuits.

It should be noted that the lossy interconnect model described in this paper consists of frequency independent resistance elements and ideal transmission line sections, and hence may not be valid at high frequencies where the skin effect becomes important. However, the technique presented is a general one and can be further extended to extract general lossy line models [39], that include skin effect and dielectric lossless and dispersion, from the time domain measurements.

5. CHARACTERIZATION AND CIRCUIT MODELING OF PARALLEL POWER/GROUND PLANE STRUCTURES IN HIGH SPEED ELECTRONIC PACKAGES

Switching noise caused by the large transient currents flowing into power/ground distribution system has been regarded as a significant problem in high speed analog, digital, and mixed signal integrated circuits. In this chapter, a frequency dependent nonuniform transmission line model is considered for modeling parallel power/ground planes in high performance electronic packages. The model is based on radial transmission line analysis, and is validated by comparing the calculated time domain response with TDR measured data. The transient effects due to transient sources placed at the different locations of parallel power and ground planes are also investigated. Alternate equivalent circuit models consisting of ideal lumped circuit elements for power/ground plane structure in a practical package are also presented. These models are readily incorporated with the driver model for switching noise simulations. In addition, switching noise with the associated packaging resonance for different edge rates and clock rates in typical high speed digital circuits are also examined.

5.1 Introduction

When high speed circuit drivers switch large amounts of current through the power/ground distribution system of the electronic package, the resulting change in the voltage level of the power system and the reference shift of the ground system is known as power/ground switching noise, and ground bounce. This noise voltage, amplitude depends on the power/ground distribution system and the rate of change of the current spike, which creates uncertainty in the reference voltage level of the common power and ground system. This results in a voltage fluctuation in the output of the circuits leading to signal distortion and the reduction of the noise immunity [40–45]. In order to guarantee a successful circuit design, accurate characterization and circuit modeling

of the power/ground interconnect structure is necessary during the design phase of high speed RF, microwave, mixed signal, and digital integrated circuits.

Significant advances in quasi–static and FDTD numerical techniques [50] for the full–wave electromagnetic computational modeling of packages and package components, have been made in recent years. The Partial Element Equivalent Circuits (PEEC) methods [46], enhanced PEEC methods [47,48] and retarded PEEC method [49] which takes into account high frequency retardation effects has formed acceptance in the modeling community as an effective tool for package modeling. This includes the modeling of power and ground planes in integrated circuits and associated packages as shown in Figure 5.1.

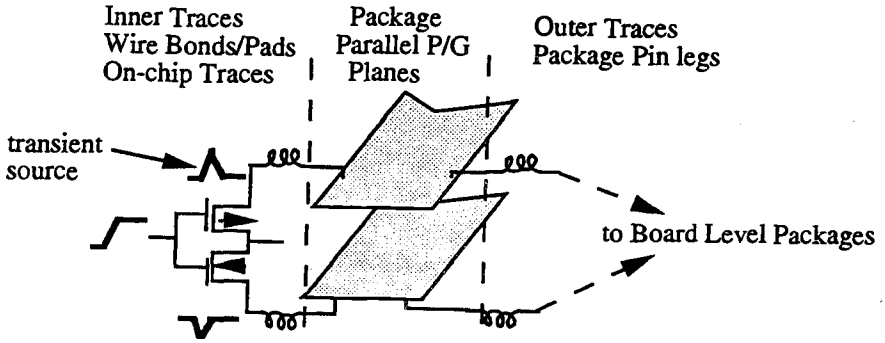


Figure 5.1, A schematic power and ground system associated with IC package.

In addition, as stated earlier general time and frequency domain measurement techniques have been developed to validate these models and develop new measurement based circuit and mathematical models which can be used during the design cycles in standard CAD tools [5,26,27]. In this chapter, a distributed element model for power/ground planes based on classical radial line analysis is presented. The model is verified by time domain reflection (TDR) measurements for different cases on PCB test fixtures. An alternative equivalent lumped element model obtained from the input impedance of the distributed element model is also proposed to model the power and ground system over a certain low frequency region. Power and ground switching noise with the high frequency resonance for a high speed digital circuit is also investigated for a typical MLC package.

5.2 Radial Transmission Line Analysis

5.2.1 Field Representation

The schematic of a typical parallel power/ground planes in an electronic package is shown in Figure 5.2–(a). Whenever a high speed gate is switching from one logic state to another, both the complementary transistors of a gate are on, and current is being sunk into the power and ground planes of the electronic package. The transient current draw by power and ground planes carries high frequency harmonic components that leads to the induced noise on the power and ground planes. To analyze the structure of power and ground planes shown in Figure 5.2–(b), let the direction of energy transmission be chosen along r direction only, such that there is no variation of fields with and z direction in cylindrical coordinate. The fundamental wave that can be guided by this structure is a TEM one with only H_Φ and E_Z [51,52] field components.

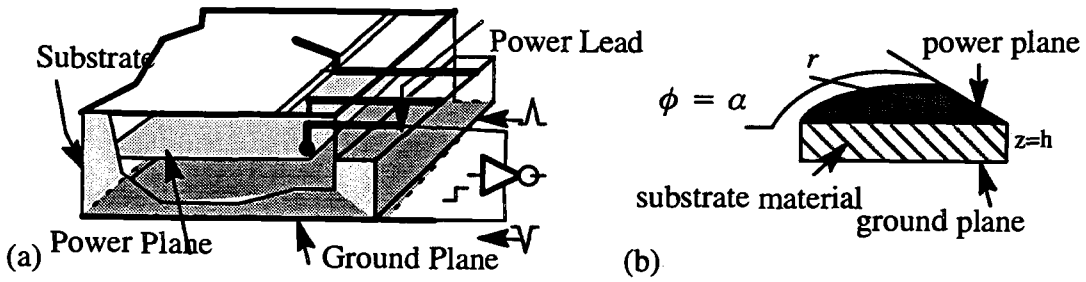


Figure 5.2, (a) Parallel power/ground plane structure in a typical electronic package. (b) The schematic radial line structure for parallel semi–infinite conducting planes.

Thus, E_Z field component is a solution of the Helmholtz equation as given by

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial E_z}{\partial r}\right) + k^2 E_z = 0 \qquad (5.1)$$

leading to the solutions for E_Z and H_Φ as given by

$$E_z = AH_0^{(1)}(kr) + BH_0^{(2)}(kr) \tag{5.2}$$

$$\text{and } H_\Phi = \frac{j}{\eta}\,[AH_1^{(1)}(kr) + BH_1^{(2)}(kr)], \tag{5.3}$$

where $H_n^{(1)}(kr)$ and $H_0^{(2)}(kr)$ are Hankel functions of first and second kinds, $k = \sqrt{\mu\epsilon}$ and $\eta = \sqrt{\frac{\mu}{\epsilon}}$. A and B are constants to be determined by boundary conditions on the fields at r direction and η is the the intrinsic wave impedance of the medium between parallel conducting planes. As $kr \Rightarrow \infty$, the $H_n^{(1)}$ function's behavior approaches that of a radial incoming traveling wave, and the $H_n^{(2)}$ function's behavior approaches that of a radial outgoing traveling wave.

The above equation can be written in terms of the magnitudes and phases of Hankel function as

$$H_\Phi = \frac{G_0(kr)}{Z_0(kr)}[Ae^{j\psi(kr)} - Be^{-j\psi(kr)}] \tag{5.4}$$

$$\text{and } E_z = G_0(kr)[Ae^{j\theta(kr)} + Be^{-j\theta(kr)}], \tag{5.5}$$

where $Z_w(kr) = \eta\frac{G_0(kr)}{G_1(kr)}$ is a frequency dependent characteristic wave impedance, which depends on radial distance r. Eqations (5.4) and (5.5) are readily modified if the given region has an angular aperture α as shown in Figure 5.2–(a). The characteristic impedance of the parallel conducting planes can be obtained, in a conventional manner, in terms of the ratio of voltage to current for a given radial wave as $\frac{E_z h}{H_\Phi \alpha r}$.

5.2.2 Impedance Description

By applying radial transmission line analysis to the structure as shown in Figure 5.2, a parallel power and ground planes is then modeled as a nonuniform transmission line shown in Figure 5.3–(a). Furthermore, the piecewise transmission line sections as shown in Figure Figure 5.3–(b) is used to evaluate the electrical characteristics of the nonuniform transmission line model.

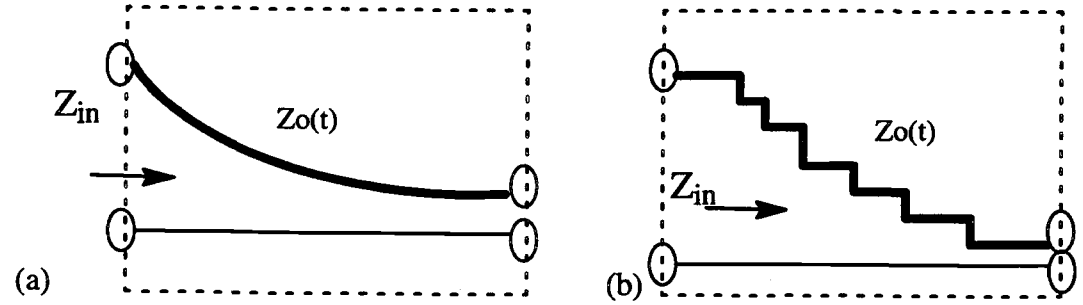


Figure 5.3, (a) Nonuniform transmission line model for parallel power/ground planes. (b) Piecewise impedance line model.

With the outgoing directions for current and voltage in a radial line shown in Figure 5.3, the wave equation is then given by

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial V}{\partial r}\right) + k^2 V = 0 \qquad (5.6)$$

and the propagating voltage and current in a nonuniform transmission line are related by the transmission line equations as

$$\frac{\partial V(r)}{\partial r} = -\,jk\, Z_o(r)\, I(r) \quad , \qquad (5.7)$$

$$\frac{\partial I(r)}{\partial r} = -\,jk\, Y_o(r)\, V(r) \quad , \qquad (5.8)$$

$$Z_o(r) = \sqrt{\frac{L}{C}} \quad , \qquad (5.9)$$

where capacitance and inductance per unit length of the piecewise nonuniform trans-

mission line are $C = \frac{\epsilon \alpha r}{h}$ and $L = \frac{\mu h}{\alpha r}$, respectively, for the case of $kr \gg 1$.

By evaluating the boundary condition along *r* direction at r and r_0, the input and output voltage and current are written in a matrix form as

$$\begin{bmatrix} V(r) \\ I(r) \end{bmatrix} = \frac{\pi k r_0}{2} \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} V_0(r) \\ I_0(r) \end{bmatrix} \quad , \qquad (5.10)$$

where

$$h_{11} = J_1(kr_0)\ N_0(kr) - J_0(kr)\ N_1(kr_0) \quad , \qquad (5.11)$$

$$h_{12} = jZ(r_0)\ [\ J_0(kr)\ N_0(kr_0) - J_0(kr_0)\ N_0(kr)\ ] \quad , \qquad (5.12)$$

$$h_{21} = \frac{-j}{Z(r)}\ [\ J_1(kr_0)\ N_1(kr) - J_1(kr)\ N_1(kr_0)\ ] \quad , \qquad (5.13)$$

$$h_{22} = \frac{Z(r_0)}{Z(r)}\ [\ J_1(kr)\ N_0(kr_0) - J_0(kr_0)\ N_1(kr)\ ] \quad . \qquad (5.14)$$

Note that $J(Kr)$ and $N(Kr)$ are Bessel functions of the first and second kinds.

The input characteristic impedance of the radial transmission line looking in the direction of increasing radius is then obtained from equation (5.10) as

$$Z_c(r) = \frac{Z_o(r)\ H_0^{(2)}(kr)}{j\ H_1^{(2)}(kr)} \qquad (5.15)$$

$$= Z_o(r)\ \frac{G_0(kr)}{G_1(kr)}\ e^{-j[\theta(kr) - \varphi(kr)]} \qquad (5.16)$$

where $\frac{G_0(kr)}{G_1(kr)}$ and $[\theta(kr) - \varphi(kr)]$ vs kr are shown in Figure 5.4–(a) and (b).

If the effect of high frequencies is of interest, i.e., $kr \gg 1$, parallel power and ground planes is then modeled as a frequency dependent nonuniform transmission line [53] as

$$Z_c(r) = \frac{h}{\alpha r}\sqrt{\frac{\mu}{\epsilon}}. \qquad (5.17)$$

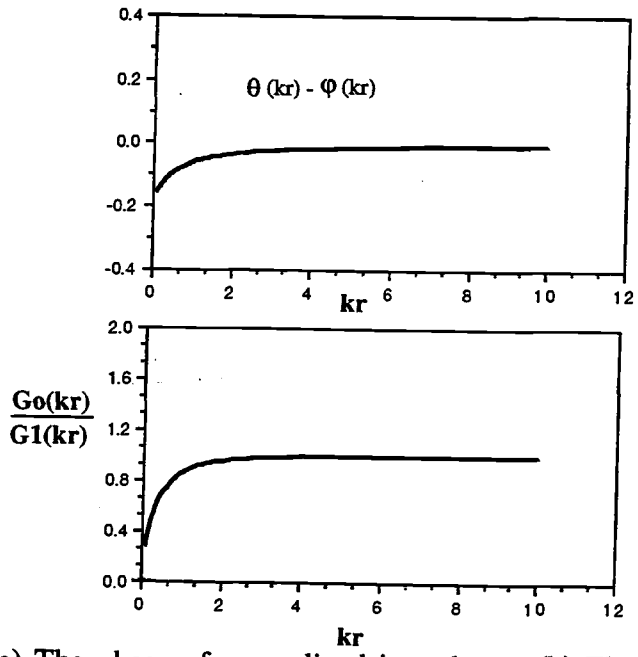
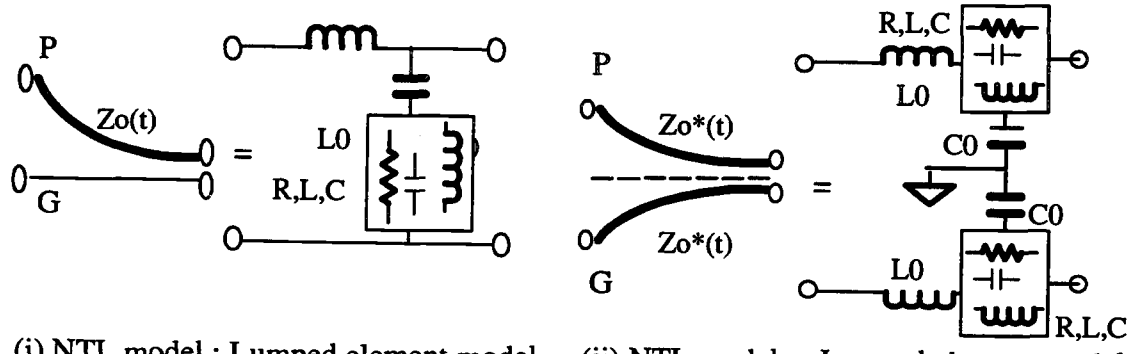


Figure 5.4, (a) The phase of normalized impedance. (b) The amplitude of normalized impedance.

The input impedance of power/ground plane structures can be obtained by truncating the measured nonuniform impedance profile and evaluating the input impedance at a given frequency by using the piecewise impedance model [53]. An alternative equivalent circuit model consisting of R,L,C lumped elements [54] is also shown in Figure 5.5. The circuit parameters of the model are obtained by deriving a lumped element network having the same input impedance as the measured nonuniform transmission line model over a desired frequency range.



(i) NTL model : Lumped element model (ii) NTL model: Lumped element model

Figure 5.5, Nonuniform transmission line models (NTL) of power/ground systems with the corresponding lumped element models.

5.3 Circuit Models of Parallel Power/Ground Plane Structures

5.3.1 Time Domain Measurements

The experimental case study based on time domain measurements is performed to confirm the accuracy of the proposed nonuniform transmission line model for parallel power and ground planes. Time domain measurements are carried out by using Tektronix IPA 310, which consists of an enhanced TDR system and parameter extraction programs. The TDR unit includes Tektronix 11801 main frame, SD–24 high speed sampling head and a step voltage generator that offers a fast step signal with a 28ps rise time. The nonuniform impedance profile is then extracted from the measured time domain reflection response by using layer peeling algorithm (dynamic deconvolution) [5,27]. Multiple reflections due to distributed discontinuities are automatically corrected and the accuracy and resolution of the measurements are enhanced by using the deconvolution algorithm.

A typical single–channel TDR set–up is shown in Figure 5.6–(a) for performing time domain measurements. Figure 5.6–(b) shows a two–port nonuniform transmission line model extracted from the measured time domain reflection response by using the step–up shown in Figure 5.6–(a). In addition to that a single channel TDR measurement, a differential TDR measurement set–up is also shown in Figure 5.7–(a) where two TDR units are side by side connected to the test fixture with one launching a positive–slope step voltage and the other sending out a negative–slope step voltage at the same time. The differential measurement set–up provides an alternative way to handle the test fixtures for obtaining time domain response. Figure 5.7–(b) shows the schematic four–port nonuniform transmission line model corresponding to the differential TDR measured response. The given four–port network having some degree of complexity can be viewed as being constructed from simpler two–port networks, whose reference planes are interconnected and then suppressed while preserving the input and output terminals. It is noted that the characteristic impedances of two–port networks are used

to characterize the individual planes of parallel power and ground planes associated with the pseudo–reference plane between parallel power and ground planes.

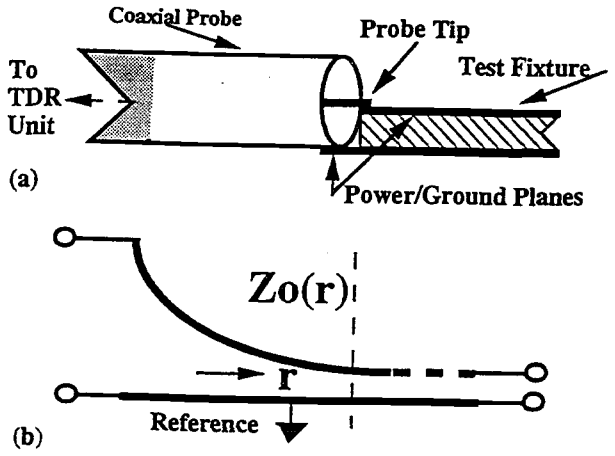


Figure 5.6, (a) Single channel TDR measurement set–up. (b) Two–port nonuniform transmission line model corresponding to the measured response.

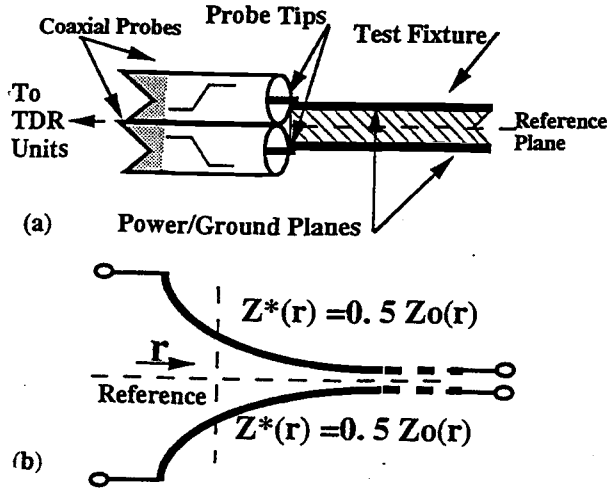


Figure 5.7, (a) Differential TDR measurement set–up. (b) Four–port nonuniform transmission line model corresponding to the measured response.

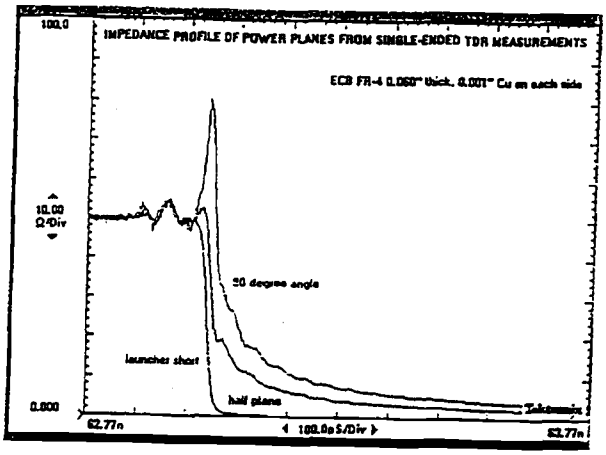
5.3.2 Examples

CASE (I) – PCB Level Packages

The test fixtures are made by bare printed circuit boards (PCB) with FR–4 substrate material. The measured characteristic impedance profiles obtained from

Tektronix IPA 310 for the two cases of 60 mil right angle sector and a half plane are shown in Figure 5.8–(a). It is obvious that the measured characteristic impedances of power and ground planes are nonuniform profiles and depend on the radial angle α. Figure 5.8–(b) shows the measured characteristic impedances as a function of time and distance, together with the calculated characteristic impedance profiles. The agreement is quite good and validates the proposed nonuniform transmission line model. The frequency dependent input impedance of parallel power and ground planes is calculated by truncating the nonuniform transmission line model and evaluating the input impedance by using a stepped transmission line model at given frequencies.

(a)



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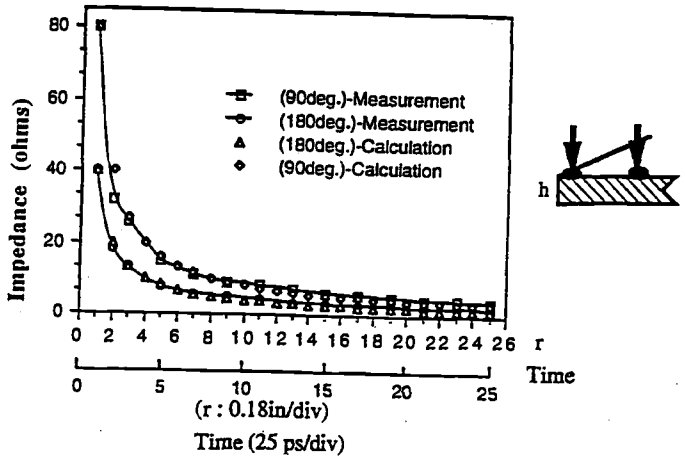


Figure 5.8, (a) The extracted impedance profiles from the TDR measured response. (b) The calculated and the measured impedance profiles for a corner fed right angle and a half plane. (h=60 mil, FR–4 substrate)

The input impedance for typical case of board level parallel power and ground planes with the commonly used 60 mil PCB FR–4 substrate for a half plane is shown in Figure 5.9 for a band of low frequency, e.g., up to 3 GHz. The equivalent inductance $L_{eq} = \frac{Z_{in}(\omega)}{j\omega}$ is of course frequency dependent. The low frequency inductances calculated from Figure 5.9 for half plane and simular figure for 90° section found to be 0.425 nH and 1.02 nH, respectively.

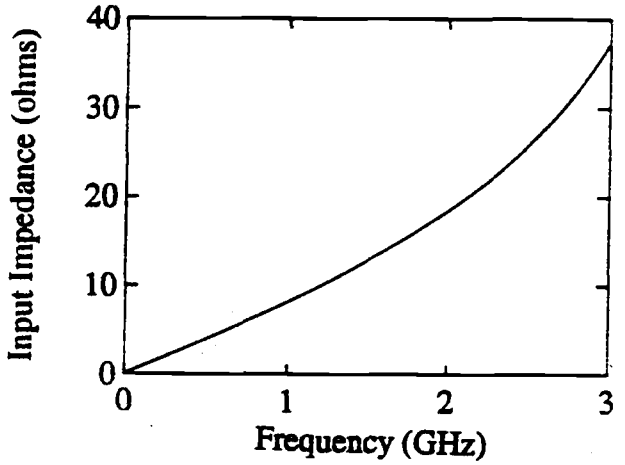


Figure 5.9, Input impedance of parallel half planes. (h=60 mil, FR–4)

CASE (II) – Multilayer Ceramic Package

A second example deals with a parallel power/ground planes in a high speed and high pin count package. A multilayer ceramic package (MLC) with 100 lead counts is shown in Figure 5.10. The power and ground distribution system of the package includes the inner traces which connect on chip power and ground bus to power and ground planes of the package via wire bonds, and the outer traces which provides the interconnection between power and ground planes of the package and the pin leads. The primary reason to perform the measurements on this package is to demonstrate that nonuniform transmission line model is available for modeling power and ground system in a practical package, thus the measured data presented in this section is only focused on that part of the package.

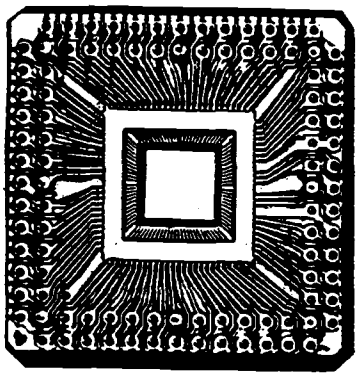


Figure 5.10, A multilayer layer ceramic PGA package.

In order to probe the inner traces of a MLC package, the schematic TDR measurement set–up is shown in Figure 5.11, where TDR unit consists of a high frequency coaxial probe for this typical test fixture. The time domain responses measured from the middle lead of inner traces is shown in the upper half of Figure 5.12, and the extracted nonuniform impedance profile corresponding to the measured data is also shown in the lower half of Figure 5.12. The piecewise nonuniform transmission line model (NTL) is readily obtained from the extracted characteristic impedance profile and then used to model the middle power lead with the associated parallel power/ground planes for this package [5,26]. The simulation result for the nonuniform characteristic impedance profile together with the measured data are also shown in Figure 5.13. The input impedance of the power/ground system can also be obtained by truncating the measured nonuniform impedance profile and evaluating the input impedance at a given frequency by using the stepped impedance model. For the typical case of the power/ground planes in the MLC package with the corresponding measured TDR response shown in Figure 5.12, the input impedance is shown in Figure 5.14. The equivalent inductance is of course frequency dependent.

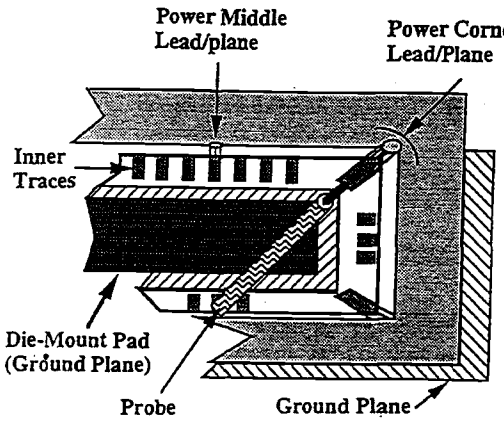


Figure 5.11, The schematic TDR measurement set–up on the inner traces of the MLC package.

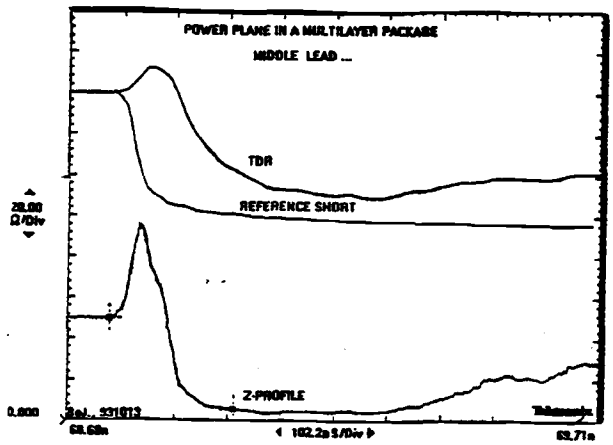


Figure 5.12, The measured time domain response and the extracted nonuniform impedance profile for the middle power lead of the inner traces in the MLC package.

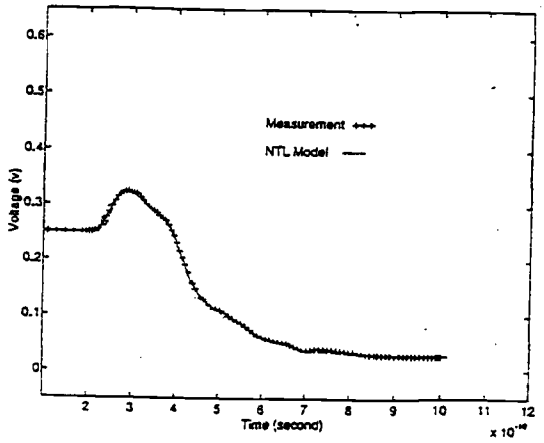


Figure 5.13, The measured TDR waveform and the simulated waveform of nonuniform transmission line model.

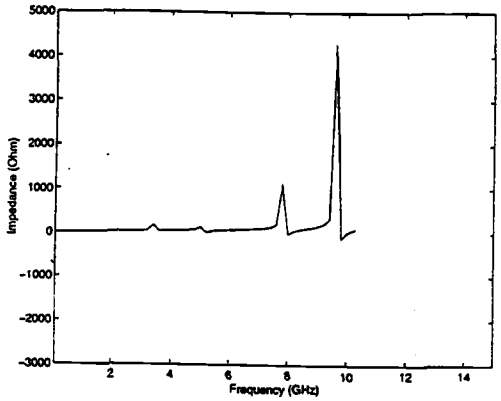


Figure 5.14, The input impedance of power/ground plane structure in Figure 5.12.

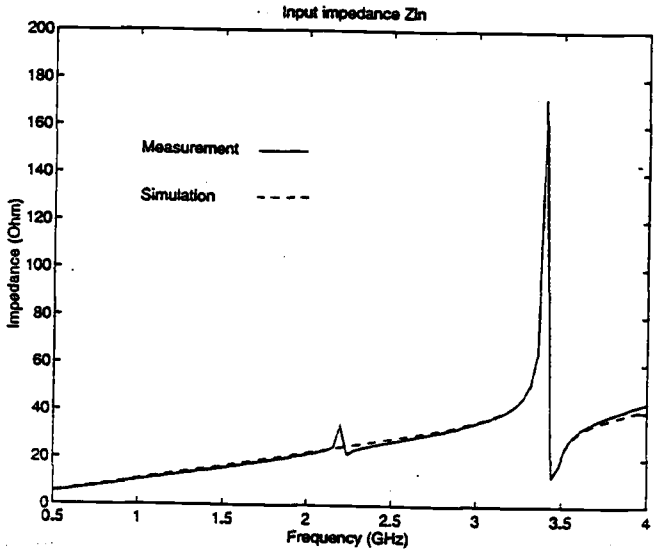
5.3.3 Lumped Element Model

An alternative approach for circuit modeling of the power/ground plane is to derive a lumped element model having the same input impedance over a wide frequency band of interest. The complete circuit model may consist of high order cascaded lumped element network obtained by using the technique given in [39]. However, for a low frequency model up to a certain frequency (e.g., up to 4 GHz) , the input impedance is shown in Figure 5.15–(a) and an associated simple equivalent circuit model consisting of L_o, C_o lumped element model together with a resonant R,L,C lumped section is also shown in Figure 5.15–(b). The L_o, C_o element model is constructed for modeling the power and ground system over the low frequency region, and the augmenting parallel R, L, C section is used to account for the nonlinear frequency dependent impedance and the high frequency resonance. The phenomena of high frequency resonance for the power and ground system is also found by using FDTD methods reported in [50]. The inductance L_{lf} and capacitance C_{lf} are readily calculated from the impedance profiles by using the techniques given in references [26,27] and $\{R_{ro}, L_{ro}, C_{ro}\}$ is determined by minimizing the error function representing the difference between the measured input impedance and the values of the input impedance for the model evaluated over the given frequency band in a least–square sense [54].

$$E\{R_{r0}, L_{r0}, C_{r0}\} = \int_{f1}^{f2} [Zs(f) - Zm(f)]^2 \, df \qquad (5.18)$$

The minimization of the error function was performed by utilizing the conjugate gradient algorithm in an iterative manner [55,56]. The simulated result of the input impedance for the model compared with the measured input impedance in Figure 5.15–(a) shows in a good agreement and validates the accuracy of the lumped model.

(a)



(b)

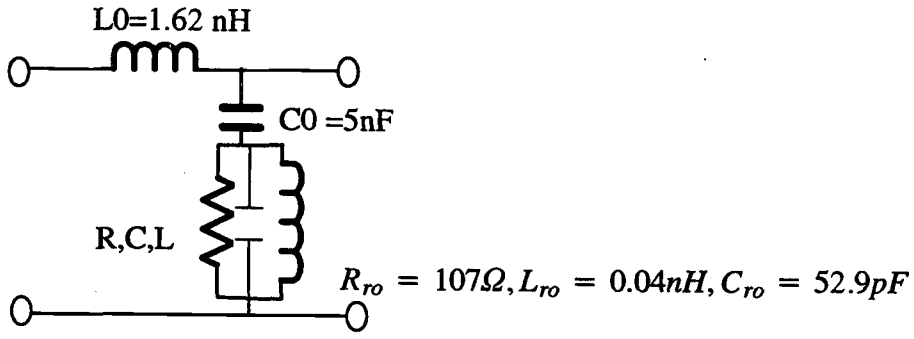


Figure 5.15, (a) The input impedance obtained from the measured TDR data together with the input impedance of the lumped element model in (b). (b) Lumped element model of the power/ground plane structure.

5.4 Modeling and Simulation Of Switching Noise With the Associated Package Resonance FOR High Speed Digital Circuits

Power/ground switching noise is generated by well–synchronized, fast–switching circuits in digital systems such as output drivers for on–chip memories, PLAs, ASICs and dynamic logic circuits. In this section, the investigation of switching noise with the associated package resonance is carried out by incorporating the power/ground model of a MLC package with the driver model in circuit simulations. The effects of the package resonance vs edge rates for the GaAs FL inverter, are also included in this section and in addition, the simulation results of switching noise for a specific digital circuit with various edge rates and clock rates are also examined.

5.4.1 The Switching Current Harmonics

With the advancements in the electronic device process techniques, the switching speed of digital circuits has been increasing and is now in the sub–nano second regime and associated the clock frequency of the digital systems is also increasing and may soon approach the Giga Hertz rank. In such a situation, power/ground switching current may possess higher frequency harmonics, and therefore, switching noise due to power and ground parasitic effects can no longer be ignored. Figure 5.16 shows the schematic circuit diagram of the high speed digital driver/load with the associated power/ground interconnect structure. As an example, a typical GaAs FEL (FL) circuit is used as a vehicle to investigate the effects of switching noise in circuit simulations. A 400 MHz clock signal is used to excite to the input of the inverter and the output waveform of the inverter is shown in Figure 5.17. The waveshape of ground switching currents due to the input clock signal switching from one logic level to another vs edge rates (50ps and 400ps edge rates) of the input signal are shown in Figure 5.18. The resulting frequency harmonics of switching currents are also used to determine the frequency band of interest for the circuit model used fo the power/ground structures.

As shown in Figure 5.18, the switching current observed at this typical digital circuit has two major components. The first component caused by both C–GaAs FETs at the rising and falling edges of the input excitation, is a high frequency spike whose zero–to–peak amplitude is proportional to the switching edge rate of the input clock signal. The second component caused by the charging current of the load, is a clock–like waveform whose frequency depends primarily on the frequency of the excited input signal, e.g., 400 MHz, and the amplitude is independent of edge rate. To examine the frequency harmonics of ground switching currents, the observed switching currents have been processed by using Fast Fourier Transform (FFT). The results of frequency harmonics of switching currents for 100ps and 600ps edge rates are shown in Figure 5.19. It is seen that the switching current with 100ps edge rate possess higher frequency harmonics than that of the switching current with 600ps edge rate. It is worthwhile pointing out that the highest frequency component of concern is dominated by the switching edge rate rather than the fundamental frequency of the excited clock signal for this typical circuit. Therefore, the model of power and ground systems for simulating switching noise should be taken account so that the higher frequency harmonics of switching current due to edge rate of the excited input signal can be modeled in the simula-

tions.

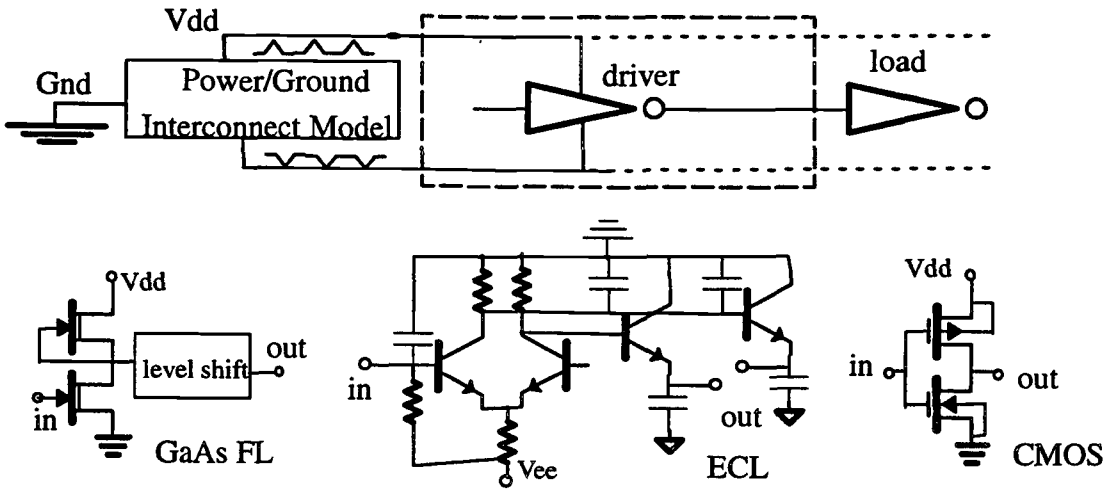


Figure 5.16, Digital circuits with the associated power/ground interconnect model.

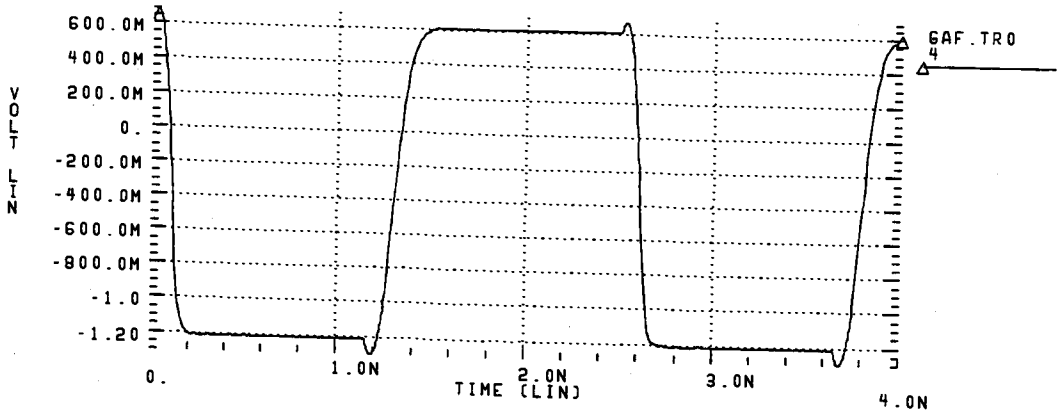


Figure 5.17, The output waveform of a GaAs FL inverter at 400 MHz clock rate.

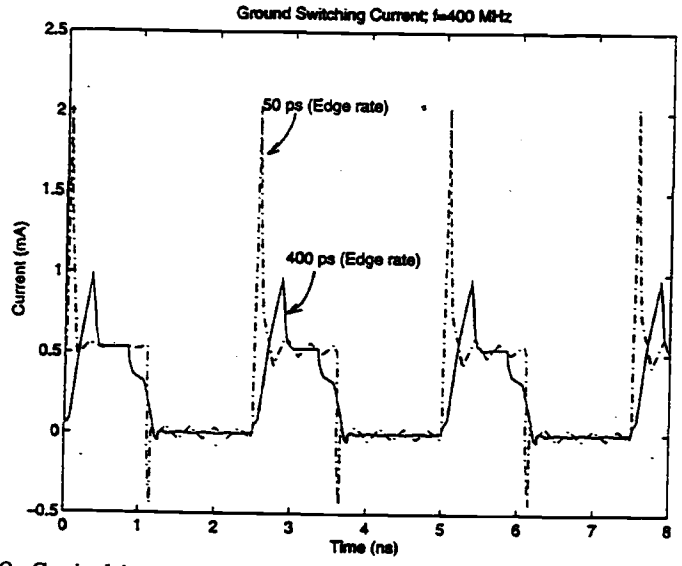


Figure 5.18, Switching currents vs edge rates for a GaAs FL inverter at 400 MHz.

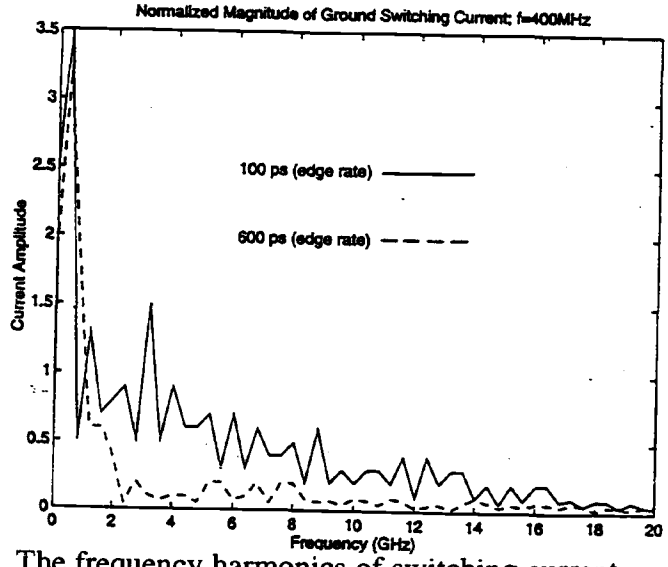


Figure 5.19, The frequency harmonics of switching currents vs edge rates.

5.4.2 Switching Noise: Theory, Modeling and Simulation

An equivalent circuit model used to describe the mechanism of switching noise is shown in Figure 5.20–(a) where Z(s) is the frequency dependent impedance obtained at one of the power/ground systems in a MLC package by using the same procedure demonstrated in the last section R_{on} is the driver's ON resistance and C_L is the capacitive load associated with parasitic capacitance. For the ground switching current possessing low frequency harmonics, a simple equivalent circuit model is considered for theoretically analyzing switching noise as shown in Figure 5.20–(b) where the inductance L_1 is obtained from the the low frequency model of power and ground system as the first order approximation.

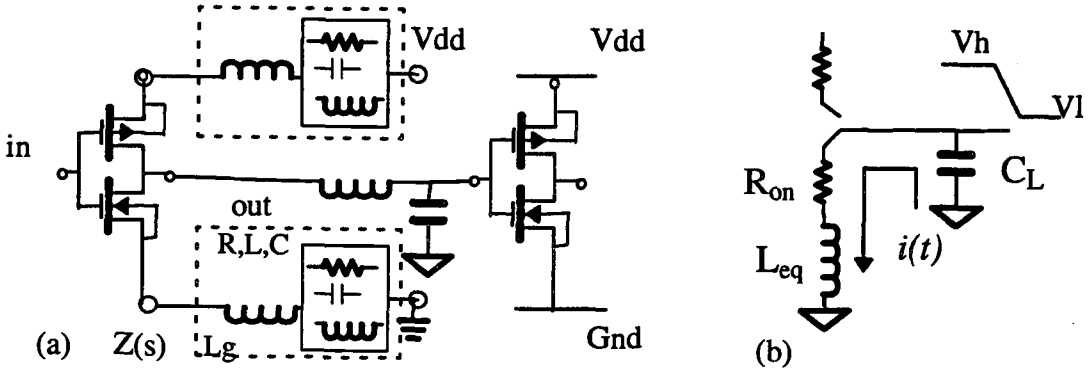


Figure 5.20, (a) Equivalent circuit model for switching current simulation. (b) The circuit model for the first order approximation.

The equation used to describe the transient effect of this circuit and the voltage change induced on the inductance are given by

$$C_L \int i(t)dt + L_{eq}\frac{di(t)}{dt} + R_{on}i(t) = 0 \qquad (5.19)$$

and *i(t)* is the pulse–like waveform of switching current whose amplitude and the frequency harmonics depend on the edge rate of the input clock signal.

By solving the characteristic equation of equation (4.19) as given by

$$L_1C_LS^2 + R_{on}C_LS + 1 = 0, \tag{5.20}$$

the resulting natural frequencies of the switch circuit shown in Figure 5.21 are given by

$$s_{1,2} = -\frac{R_{on}}{2L_1} \pm \sqrt{(\frac{R_{on}}{2L_1})^2 - \frac{1}{L_1C_L}}$$

$$= -\kappa\omega_0 \pm \omega_0\sqrt{\kappa^2 - 1} \tag{5.21}$$

where

$$\kappa = \frac{R_{on}}{2}\sqrt{\frac{C_L}{L_1}} \tag{5.22}$$

and $\omega_0 = \sqrt{\frac{1}{L_1C_L}}$, (5.23)

κ is the damping factor and ω_0 is the undamped resonant frequency. Note that the transient response of the switching circuit is given by the following criterions:

for overdamped mode; $\kappa > 1$,

for critical damping mode; $\kappa = 1$,

for underdamped mode; $\kappa < 1$.

As an example for a GaAsFET inverter, the effective on resistance, R_{on}, is very small and the capacitive load is typically less than 20 fF [57]. If the circuit is packaged by using a MLC package described at the last section, then the low frequency ground inductance obtained from the measurement is 0.775nH which puts this switching circuit in the underdamped mode with the damped frequency

$$\omega_d = \omega_0\sqrt{1 - \kappa^2}. \tag{5.24}$$

The induced voltage on the circuit's ground due to the transient current is then described by the following equation:

$$V_L(t) = L_1 \frac{di(t)}{dt}$$

$$= [A\cos(\omega_d t) + B\sin(\omega_d t)]e^{-\kappa\omega_0 t}, \quad (5.25)$$

where

$$A = L_1(C\omega_d + D\kappa\omega_0), \quad (5.26)$$

and $$B = L_1(D\omega_d - C\kappa\omega_0). \quad (5.27)$$

where C and D depend on the amplitude and frequency harmonics of switching current.

The induced transient voltage then appears as the noise on the common ground of circuits associated with the switching driver resulting in a reduction of noise margin, The waveform of switching noise can be depicted by equation (5.25) and shown in Figure 5.21. When too many drivers simultaneously switch from one logic state to another, the switching current in equation (5.25) is multiplied by the number of outputs switching, then switching noise can become very large for the case of simultaneous switching and become greater than the noise immunity of the ICs as causing false switching.

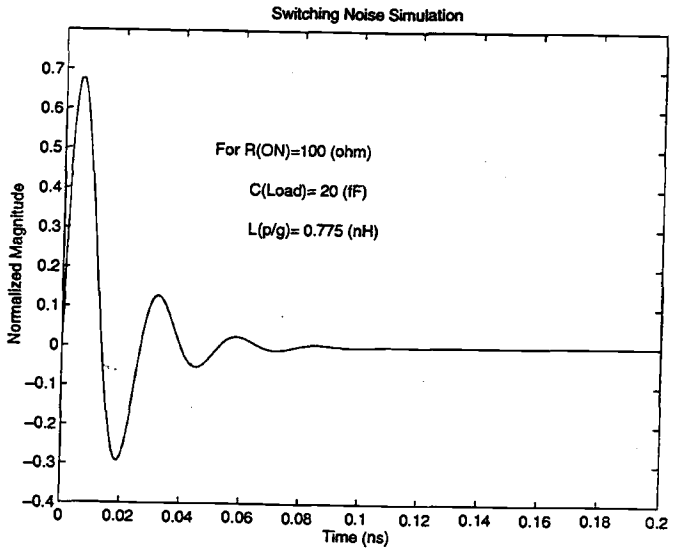


Figure 5.21, Switching noise simulation based on a simple equivalent circuit model.

5.4.3 Switching Noise with the Associated Package Resonance

The circuit model used to simulate switching noise for a FL inveter was shown in Figure 5.20–(a). To observe switching noise due to the high frequency harmonics of switching current, the input node of the FL inverter is excited by a clock signal with variable edge rates. For the case of the first order approximation, the simulated waveforms of switching noise are shown in Figure 5.22 for the input sources having 400 MHz clock rate with 25ps and 50ps edge rates. The simulated data shows that the maximum amplitude of switching noise are 156.5 mv and 75.8 mv for the case of 25ps edge rate and 50ps edge rate, respectively. The waveshape of switching noise also indicates that the switching mechanism of this typical high speed FL inverter operates in the underdamped mode as well as the analytic result based on a simplest circuit model described in the last section.

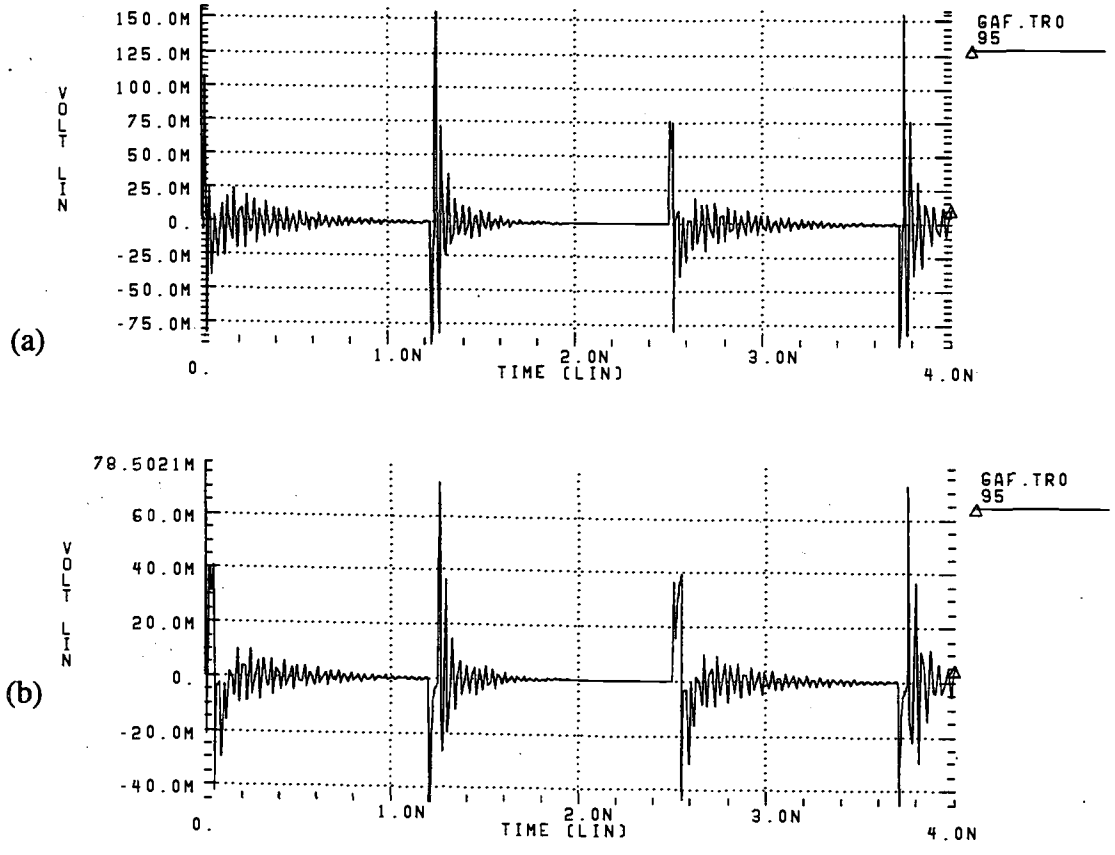


Figure 5.22, Switching noise simulation for a GaAs FL inverter with low frequency power/ground interconnect model. (a) 25 ps edge rate (b) 50 ps edge rate.

In order to accurately predict switching noise in the presence of the high frequency harmonics of switching current, the accuracy of equivalent circuit model for power and ground systems should be confirmed up to a certain high frequency of interest where the resonant effect of power and ground systems may become an important factor to switching noise. By incorporating the high frequency resonant model into the model of power and ground systems, the simulated result of switching noise for a input signal with 400 MHz and 50 ps edge rate is shown in Figure 5.23 together with the simulated result for the model based on the first order approximation. For the case of high frequency model, it is obvious that the simulated switching noise consists of two components, one is spike noise due to the switching circuit operating in the underdamped mode and the other is resonant noise to account for the effect of package resonance. Only the spike noise appeared in the simulated results for the case of the low frequency model based on the first order approximation.

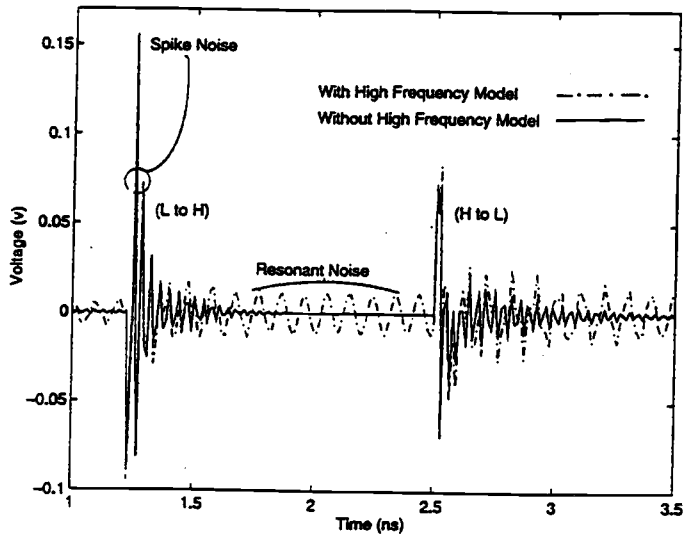
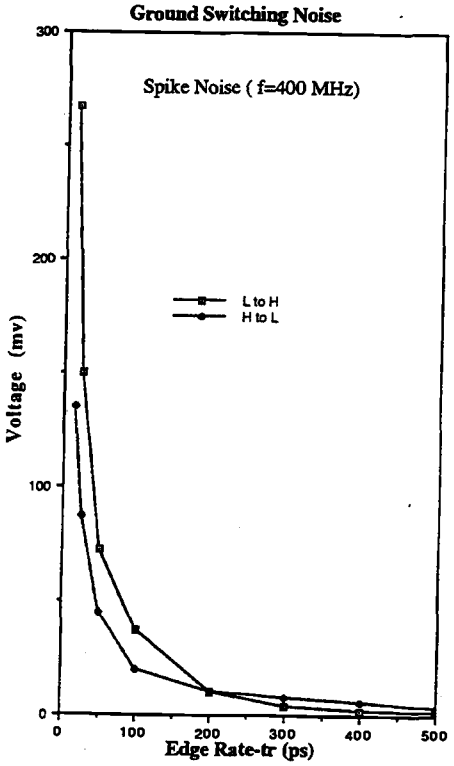


Figure 5.23 The simulation data of switching noise for a GaAs FL with high frequency and low frequency power/ground interconnect models.

The simulations of switching noise based on the high frequency model of power and ground systems were examined for a different edge rates. The simulated spike noise vs edge rates of the input signal are shown in Figure 5.24 with respect to 400

MHz clock rate and 1GHz clock rate. The result indicates that the maximum amplitude of spike noise is dominated by edge rate rather than controlled by the clock rate of input signal. It is also observed that the amplitude of spike noise is decreased with increasing edge rate. The simulated magnitude of resonant noise vs edge rate of the input clock signal is also shown in Figure 5.25. However, as shown in Figure 5.25, the amplitude of resonant noise decays rapidly when the edge rate of the excited input signal is increased. The noise then becomes negligible when the edge rate of the excited input signal is slower than 400ps for this typical GaAsFET FL inverter. Hence the result indicates that the model of power and ground systems based on the first order approximation is available for the simulation of switching noise while the device switches in a slower edge rate such that the higher order effect of switching noise can be ignored.

(a)



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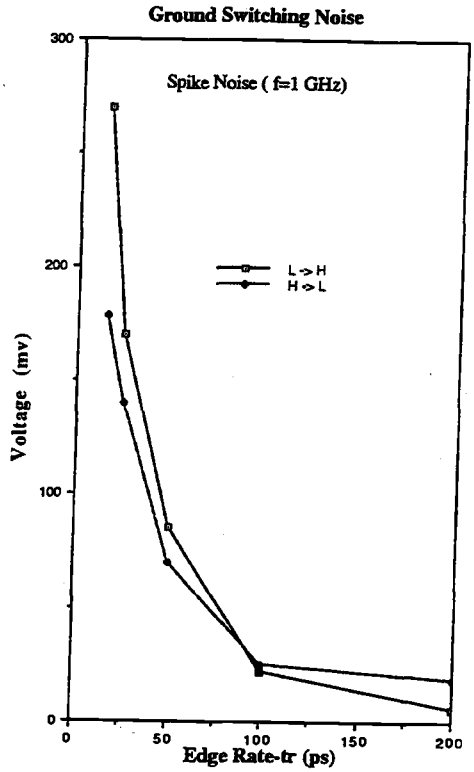


Figure 5.24, Maximum spike noise (a) 400 MHz clock rate (b) 1 GHz clock rate.

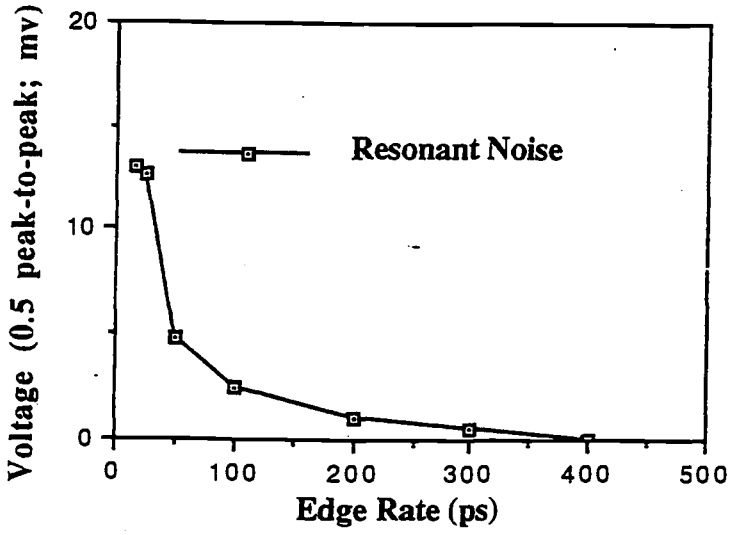


Figure 5.25, Maximum ring noise due to the power/ground resonant effect.

5.5 Summary

In conclusion, a radial line based model for parallel power/ground planes is presented in this chapter. The model is validated by comparing the calculated time domain data with the measured TDR data for different cases in PCB level packages. For a practical case study on a MLC package, the accuracy of the proposed nonuniform transmission line model and the equivalent lumped element model over a limited frequency range for parallel power and ground planes are also confirmed. The model is then used to investigate switching noise for high speed digital circuits. It is shown that the high frequency resonance in the model must be included for the accurate predicting of switching noise.

6. TIME DOMAIN CHARACTERIZATION AND CIRCUIT MODELING OF A MULTILAYER CERAMIC PACKAGE

The dynamic deconvolution algorithms (peeling algorithms) for the characterization of single and coupled interconnects developed in chapters 2 and 3 are used to model a practical high speed electronic package. The multiport measurements performed in time domain are used to evaluate the electrical characteristics and extract equivalent circuit model parameters for interconnect structures associated with a multilayer ceramic (MLC) package.

6.1 Introduction

Multilayer high–pin–count packages are used for high performance integrated circuits and systems. The electrical characteristics of interconnect structures, such as crosstalk in multiconductor structures, signal delay and reflection due to transmission line effects and switching noise in power/ground systems associated with these packages, can degrade the signal quality and limit the overall system performance. Therefore, accurate characterization of interconnect structures are essential to the successful high performance system design. In addition, circuit modeling of interconnect structures can also help to assure the signal fidelity of packaged circuits by incorporating interconnect models into integrated circuit design and simulation in the early design stages.

In recent years, several experimental techniques based on time and frequency domain measurements have been proposed to characterize interconnect structures [5–9,23–27,30–35]. For general interconnect structures, the technique based on peeling algorithm (dynamic deconvolution) has been developed for the electrical characterization and circuit modeling of non uniform single lossless and lossy interconnect, power/ground systems as well as non uniformly coupled interconnects from time domain measurements [5,26,27,31,54,60]. These techniques have been presented in

chapters 2, 3, and 4. The accuracy of peeling algorithm based technique has also been affirmed in these chapters for several interconnect structures made on the test fixtures and printed circuit board (PCB). The work reported in this chapter is focused on a practical multilayer ceramic (MLC) package with 100 lead counts as shown in Figure 6.1.

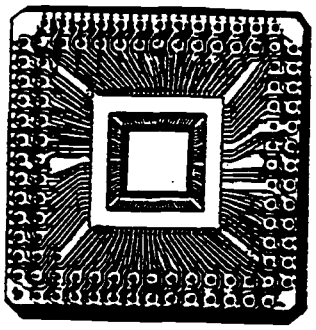


Figure 6.1, Top view of a MLC package

Multiport TDR/T measurements are performed to the package I/O ports, and the measured data is used to evaluate the electrical characteristics and extract equivalent circuit model of interconnect structures associated with the package by using one and multi–dimensional peeling algorithms. The results presented in this chapter will focus on a typical set of coupled signal traces and a power pin with the associated parallel power/ground planes in the MLC package.

6.2 Experimental Technique

6.2.1 Measurement Set–up

In order to interface test equipment to the device under test (DUT), the first task is to find a test configuration which has good flexibility and also satisfies the characterization and possible calibration requirements [20,26]. Figure 6.2–(a) shows the schematic measurement set–up where Tektronix 11801A TDR/T system including

a 250 mv step–like source with 28ps rise time and SD–24 high speed sampling heads, were utilized for performing multiport time domain measurements. Figure 6.2–(b) shows a micro–coaxial probe which was used to measure time domain reflection and transmission response of the device under test. The micro–coaxial probe with the associated TDR/T test system provides a 50 ohm reference impedance to the MLC package where the inner traces and the reference ground plane in the cavity are contacted by the probe.

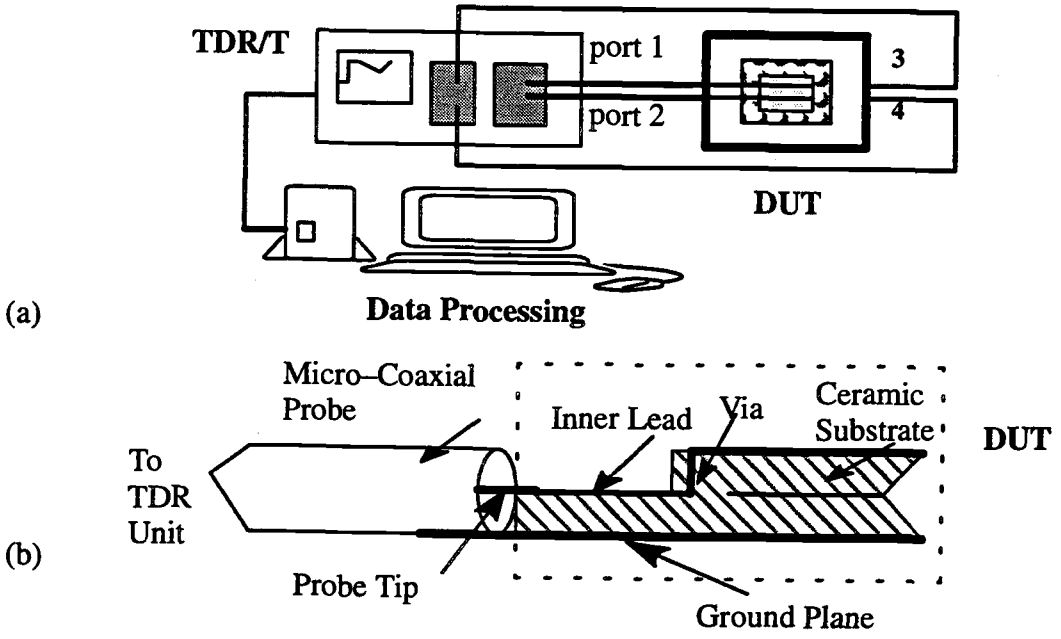


Figure 6.2, (a), The schematic measurement set–up. (b), The device under test with the associated micro–coaxial probe.

6.2.2 Multi–dimensional Peeling Algorithms

For the case of a general interconnect, the resulting waveform obtained from the TDR data is used to characterize the interconnect in terms of a time dependent non uniform impedance profile [5]. The interconnect under test can then be modeled by a non uniform transmission line approximated by cascaded uniform transmission line sections. The impedance of each uniform section is extracted from the measured TDR response by applying one dimensional peeling algorithm [5,27]. This time

domain dynamic deconvolution based peeling algorithm has been formulated in terms of the transfer scattering parameters of the piecewise uniform transmission sections and implemented on general PCs and Work Stations.

For the multiconductor systems, the procedure of one and two dimensional peeling algorithm can be extended to multi–terminal peeling algorithm for the electrical characterization of general coupled interconnect structures from multiport TDR/T measurements. As an example, a general nonuniform coupled interconnects modeled by cascaded uniform coupled line sections is shown in Figure 6.3.

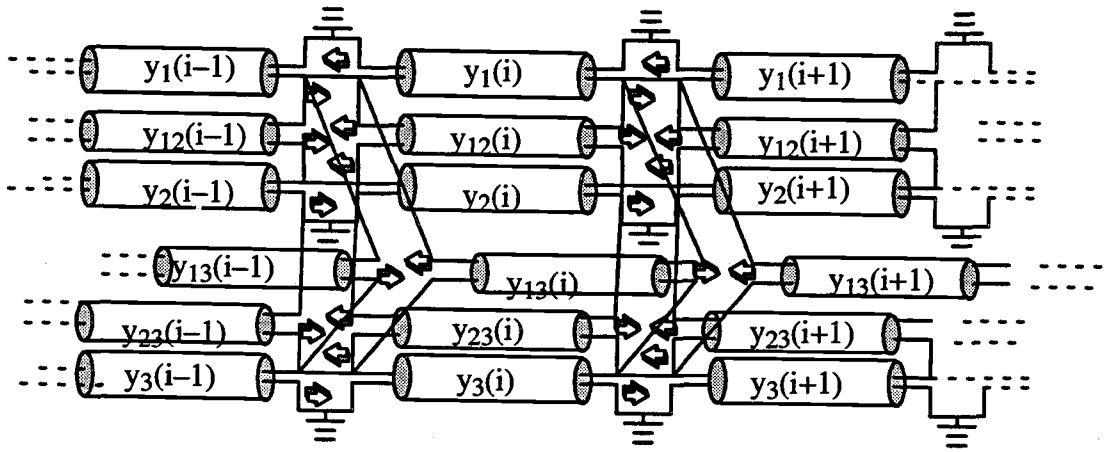


Figure 6.3, A distributed model consisting of cascaded uniform coupled line sections for general three coupled interconnects where y_{ii} is the self characteristic admittance and y_{ij} is the mutual characteristic admittance.

For this three coupled interconnects, three–terminal peeling algorithm is then formulated in terms of the 6×6 transfer scattering transmission matrix of each section.

$$\begin{bmatrix} [b_r(i,t)]_{3x3} \\ [a_r(i,t)]_{3x3} \end{bmatrix}_{6x3} = \begin{bmatrix} [T'_{11}(i)]_{3x3} & [T'_{12}(i)] \\ [T'_{21}(i)]_{3x3} & [T'_{22}(i)] \end{bmatrix} \begin{bmatrix} [b_r(i+1,t)] \\ [a_r(i+1,t)] \end{bmatrix}_{6x3}, \qquad (6,1)$$

where

$$\begin{bmatrix} [T'_{11}(i)] & [T'_{12}(i)] \\ [T'_{21}(i)] & [T'_{22}(i)] \end{bmatrix}_{6x6} = \begin{bmatrix} [T_{11}(i)]_{3x3} & [T_{12}(i)] \\ [T_{21}(i)]_{3x3} & [T_{22}(i)] \end{bmatrix} \begin{bmatrix} [D] & [\emptyset] \\ [\emptyset] & [D^{-1}] \end{bmatrix}. \qquad (6,2)$$

[D] denotes the time shifted matrix consisting of time delay and advance operators and $[T_{ij}]_{3x3}$ is the components of the 6×6 transfer scattering matrix $[T]_{6x6}$ interrelating the input incident and reflected parameter matrices $[a]_{3x3}$ and $[b]_{3x3}$ respectively of any coupled section to that of the adjoining coupled section. The iterative computational procedure is similar to the case of single line leading to the successive identification of each reflection coefficient matrix $[\ \rho_k\ ]_{3x3}$ corresponding to the change in characteristic impedance/admittance values for cascaded coupled line sections. The computational procedure is given by,

$$\begin{bmatrix}[B(k+1,t)]_{3x3}\\ [A(k+1,t)]_{3x3}\end{bmatrix}_{6x3} = [D^{-1}]_{6x6}\,[T^{-1}]_{6x6}\begin{bmatrix}B(k,t)\\ A(k,t)\end{bmatrix}_{6x3}, \tag{6.3}$$

where $[B(0)]_{3x3}$ and $[A(0)]_{3x3}$ denote the initial reflection and incident functions obtained from six–port time domain measurements and $[B(k)]_{3x3}$ and $[A(k)]_{3x3}$ denote the reflection and incident functions obtained from k+1 peeling step.

The 3x3 characteristic admittance matrix elements of coupled piecewise uniform sections represented by $[Y(i+1)]$ for all value of i+1 are extracted in terms of the reflection coefficient matrix defined at each interface by,

$$\left[\rho_{i,i+1}\right]_{3\times3} = \left[[Y(i)] - [Y(i+1)]\right] \times [[Y(i)] + [Y(i+1)]]^{-1}, \tag{6.4}$$

where

$$[Y(i)] = \begin{bmatrix} y_{11}(i)\ y_{12}(i)\ y_{13}(i)\\ y_{21}(i)\ y_{22}(i)\ y_{23}(i)\\ y_{31}(i)\ y_{32}(i)\ y_{33}(i)\end{bmatrix} \tag{6.5}$$

with the initial $[Y(i)]$ being diagonal representing the 50 ohm input terminations. The characteristic impedance matrix elements for each section are

$$[Z(i)] = \begin{bmatrix} y_{11}(i) & y_{12}(i) & y_{13}(i) \\ y_{21}(i) & y_{22}(i) & y_{23}(i) \\ y_{31}(i) & y_{32}(i) & y_{33}(i) \end{bmatrix}^{-1} = \begin{bmatrix} z_{11}(i) & z_{12}(i) & z_{13}(i) \\ z_{21}(i) & z_{22}(i) & z_{23}(i) \\ z_{31}(i) & z_{32}(i) & z_{33}(i) \end{bmatrix}. \quad (6.6)$$

The above description is a procedure used to formulate three–dimensional peeling algorithm for extracting the characteristic impedances and admittances of distributed model shown in Figure 6.3 from multiport time domain measurements. The procedure is also quite general and can be extended to multi–dimensional peeling algorithm for the characterization of multi–conductor structures. A peeling algorithm in terms of 6x6 scattering transmission matrix has also been derived and implemented to characterize a coupled interconnect structure with three signal traces of the MLC package. Many multiconductor interconnects can be decomposed in terms of three coupled interconnects making this algorithm quite useful.

6.3 Lumped and Hybrid Circuit Model

In the last section, the technique used to characterize a general multiconductor structure is based on a distributed element model consisting of cascaded uniform coupled line sections. Lumped element circuit model as well as hybrid circuit model as shown in Figure 6.4, are readily constructed from time domain profiles of the elements of the characteristic impedance and admittance matrices. For the case of hybrid circuit model, a section of coupled elements corresponding to a given time duration are modeled by coupled lumped elements associated with delay elements [59]. The element values in the model are found in the same manner as for general single non uniform interconnections with discontinuities [26,27], i.e., by integrating

the characteristic impedance elements $[Z_{ij}]$ leads to self and mutual inductances, whereas, integrating the characteristic admittance elements $[Y_{ij}]$ gives the the self and mutual capacitances. Moreover, the total inductance and capacitance values of coupled lumped element model are computed by integrating over the entire time period of the corresponding characteristic impedance and admittance profiles. The lumped element models are obviously valid for short interconnects or low frequencies.

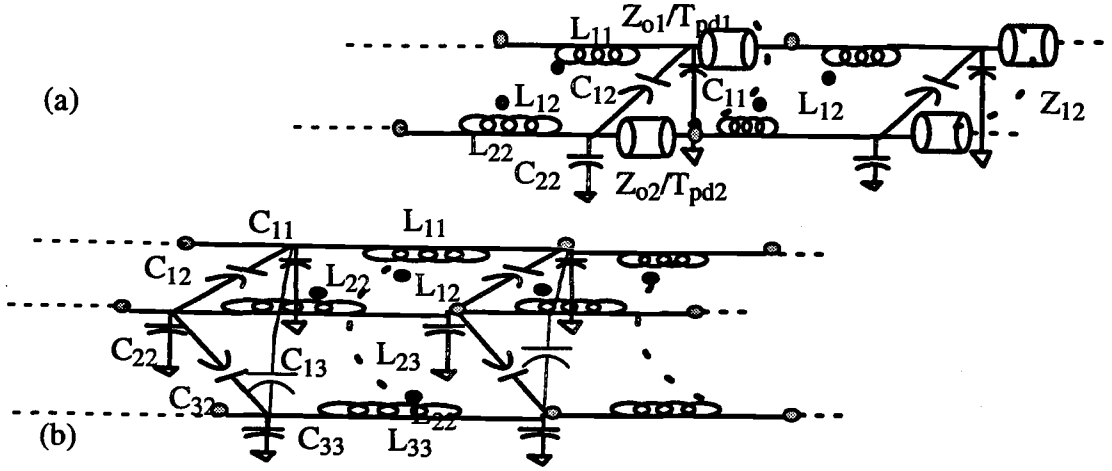


Figure 6.4, (a) Hybrid circuit model of coupled interconnects. (b) Lumped element model of three coupled interconnects.

6.3. Results

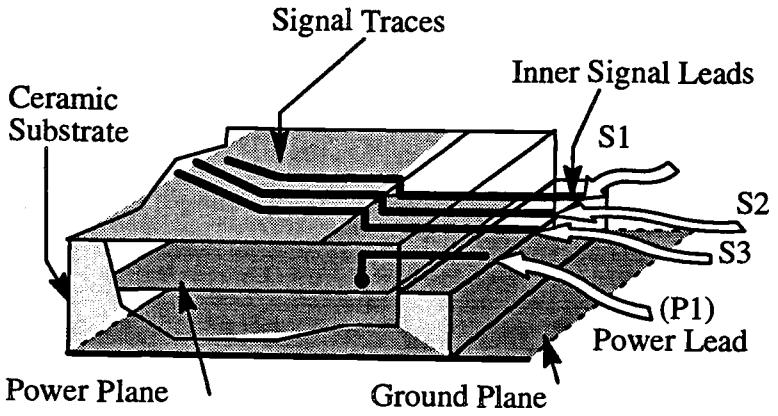


Figure 6.5, The schematic partial interconnect structures in a MLC package.

Figure 6.5 shows the schematic partial interconnect structures of MLC package shown in Figure 1, including three coupled signal lines and a power pin with the associated parallel power/ground planes as a part of power/ground distribution system providing DC power supply and AC reference planes to the integrated circuits. In general, three primary electrical characteristics, e.g., reflection, crosstalk noise and propagation delay, are needed for signal lines. Hence, the self and mutual characteristic impedances and delay time are the most important electrical parameters for the characterization and circuit modeling of the interconnects associated with the MLC package.

By using micro–coaxial probes, TDR/T test points are allowed to reach to the inner signal leads in the cavity of the MLC package. For two coupled interconnects S1 and S2 in Figure 6.5, two–port time domain TDR/T measured waveforms are shown in Figure 6.6–(a) where $V_{ii}(t)$ (i=1,2) are the measured reflection waveforms at port (i) by exciting port (i), and V_{ij} ($i \neq j$) are the measured transmission data at port (j) terminated in 50 ohms. The reflection coefficient matrices are deconvoluted from the measured scattering parameter voltage waveforms by using two–dimensional peeling algorithm. The self and mutual characteristic admittance and impedance profiles of coupled interconnects are then extracted from reflection coefficient matrices and are shown in Figure 6.6–(b). Figure 6.7 shows the extracted self and mutual characteristic admittance and impedance profiles corresponding to the coupled interconnects S2 and S3 in Figure 6.5.

For the case of three coupled interconnects, three–port time domain TDR/T measurements are performed to obtain time domain reflection and transmission response for the coupled interconnects S1, S2 and S3. The mutual characteristic impedance profiles shown in Figure 6.8 is obtained from the measured data by applying multi–dimensional peeling algorithm. The results of total self and mutual inductances and capacitances computed from the extracted characteristic admittance and

impedance profiles are listed in Table 6.1.

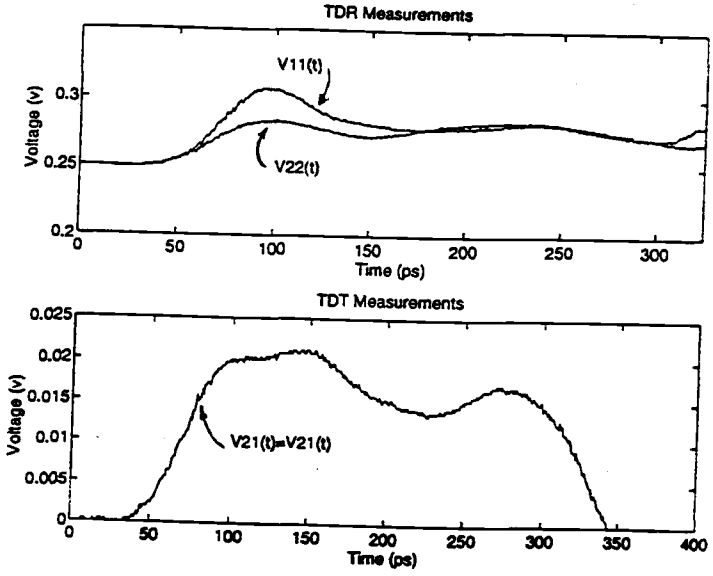


Figure 6.6, (a) The measured TDR/T waveforms of coupled interconnects S1 and S2.

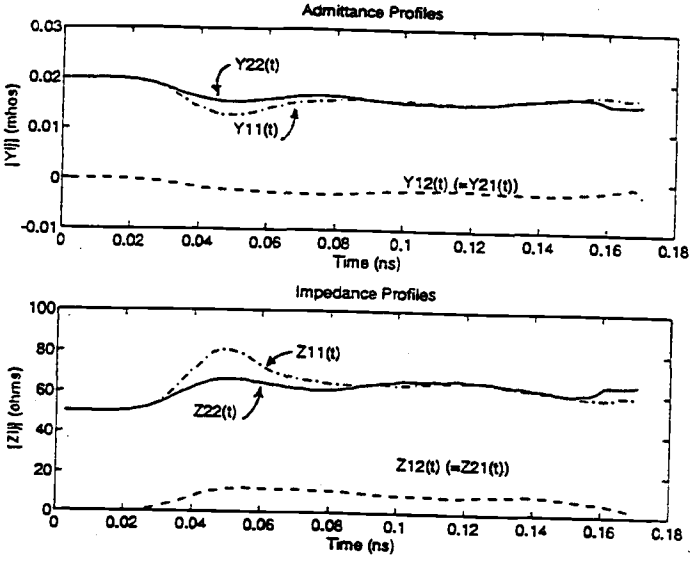


Figure 6.6, (b) The self and mutual characteristic admittance/impedance profiles in (a).

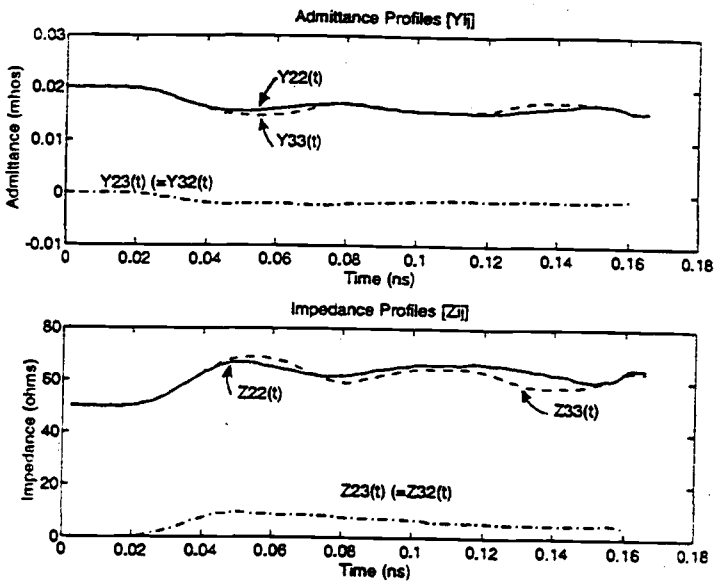


Figure 6.7, The self and mutual characteristic impedance and admittance profiles of coupled lines S2 and S3.

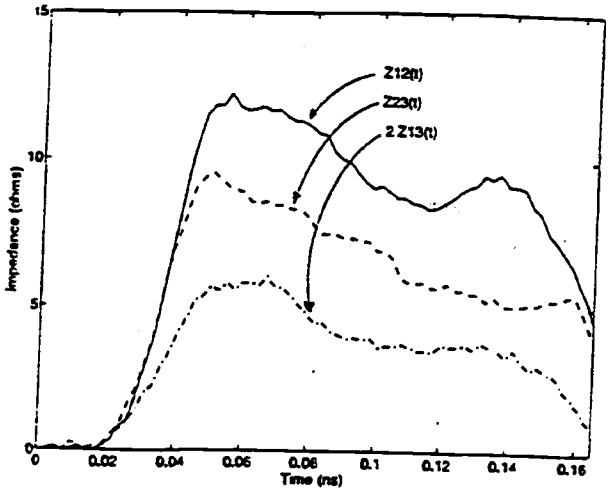


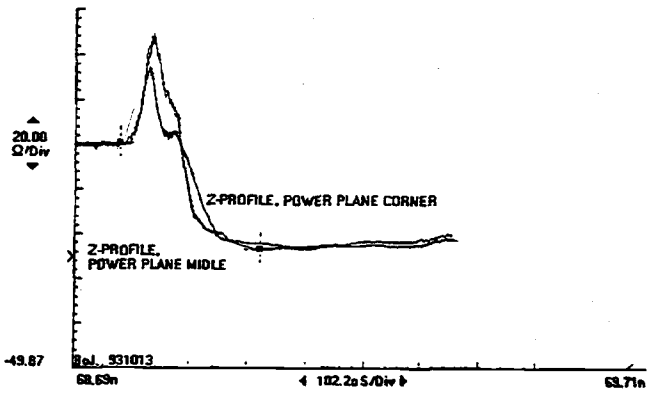
Figure 6.8, The mutual characteristic impedance profiles of three coupled lines S1, S2 and S3.

	Self terms			Mutual terms
#	L (nH)	C (pF)	Tp (ps)	L_{12}= 1.24 nH
S1	9.98	2.51	147.5	L_{23}=0.88 nH
S2	9.73	2.56	144.2	L_{13}=0.27 nH
S3	9.65	2.60	143.0	C_{12}= 0.306 pF
				C_{23}=0.228 pF
				C_{13}=0.078 pF

Table 6.1, Electrical parameters of three coupled lines in atypical MLC package.

Switching noise caused by transient currents injected into power/ground distribution system has been regarded as a significant problem for high pin count packages. So the next task is to deal with the characterization and modeling of power/ground system of the MLC package. In Figure 6.5, a power pin with the associated parallel power/ground planes is examined for the MLC package. By using one–port TDR measurement, a non uniform transmission line model is extracted from time domain reflection response by using one–dimensional peeling algorithm [27]. The measured reflection waveform by exciting TDR source to the inner middle and corner power lead and the corresponding impedance profile are shown in Figure 6.9–(a). The distributed model and hybrid model together with the simulated and measured waveforms for the middle power plane are shown in Figure 6.9–(b). The results are in a very good agreement. Finally, the electrical characteristics of DUT for the partial interconnect structures of the MLC package are summarized in Table 6.2. A partial equivalent circuit models including signal lines and power/ground systems used to model this MLC package are shown Figure 6.10.

(a)



(b)

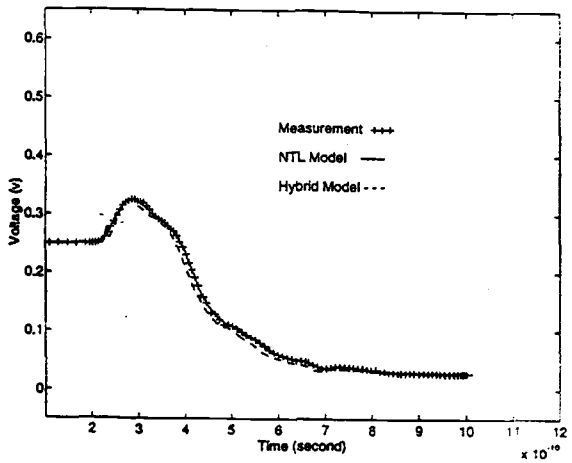


Figure 6.9, (a) The measured time domain response and the extracted nonuniform impedance profile for the power/ground interconnection structure. (b) The simulated and measured waveforms in (a)

Crosstalk (mv)		Reflection (mv) (max. ringing)		Delay Skew (ps)		Switching Noise (mv)
S1/S2	71.3	S1	36	S1/S2	3.3	Spike 157
S2/S3	46.1	S2	20.4	S2/S3	1.2	Ring 21.7
S1/S3	14.	S3	12.8	S1/S3	4.5	

S1, S2 and S3: Signal Leads, P1: Power Lead, $V_{H/L}$=2 v, tr=50ps

Table 6.2, Electrical characteristics of a typical MLC package.

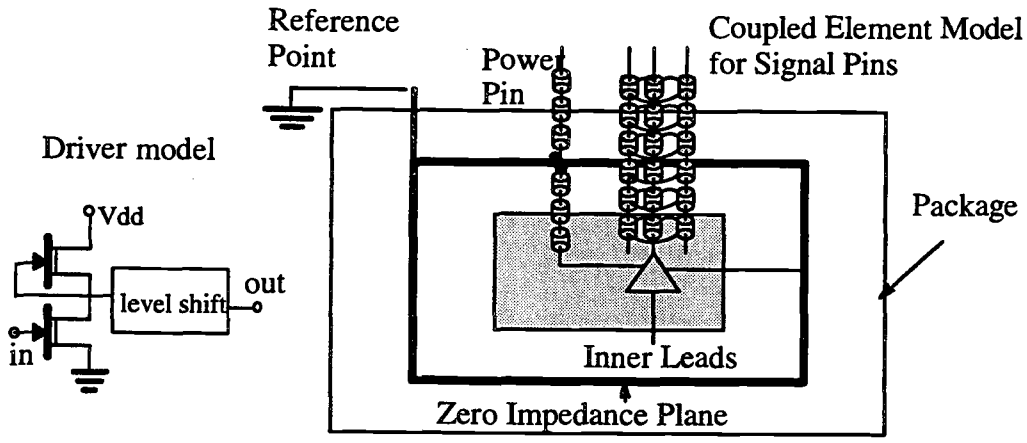


Figure 6.10, Equivalent circuit model of a partial interconnection structures for a MLC package with the digital driver circuit model.

6.5 Summary

In conclusion, one, two and multi–dimensional peeling algorithms for characterizing and modeling general interconnect structures of a typical MLC package from time domain measurements are presented. The applicability of this technique on general interconnects including non symmetrical inhomogeneous coupled interconnect structures with discontinuities and parallel power/ground planes is exemplified by circuit modeling of a multilayer ceramic package.

7. CONCLUSIONS

This dissertation was devoted to the study of time domain measurement techniques based on dynamic deconvolution (peeling algorithms). For general interconnection structures in high speed digital systems, the use of time domain reflection and transmission measurements together with accurate calibration methods makes the technique very reliable. The techniques presented at Chapter 2 and 3 are based on one– and two–dimensional peeling algorithms for characterization and modeling general single (isolated) and coupled interconnection structures from one– and two–port TDR/T measurements. The extended peeling algorithm for characterization of general resistive lossy interconnection structures has been presented at Chapter 4. Chapter 5 presented a hybrid technique based time domain dynamic deconvolution with a frequency domain optimization algorithm which makes the technique very practical. In Chapter 6, multiconductor systems of a multilayer electronic package is used as a vehicle to demonstrate the applicability of multi–dimensional peeling algorithms.

For edge rates of high speed devices in the picosecond regime, the component and system level packaging interconnects introduce transmission line effects that could limit the performance of circuits and systems. Control of electrical characteristics of interconnects is a key factor in ensuring high speed performance. For VLSI high speed applications, modeling the effects of interconnection structures is essential for optimizing the system design through circuit simulations including interconnect parasitic effects. Accurate characterization and modeling of current high speed IC packages must include the modeling of:

. Coupled interconnection structures
. Nonuniform interconnection structures with discontinuities
. Common power/ground distribution systems including parallel plane structures
. DC voltage drop and signal degradation due to transmission loss

For high speed digital circuit and system design, the circuit simulation must be operated in the time domain in order to validate logic level correctly, and hence the input excitation, active and passive device models and outputs are expressed in the time domain. In this dissertation, the approach based on transmission line models for characterization of interconnection structures is compatible with the use of nonlinear circuits such as logic circuits in general integrated circuit simulators such as SPICE. Therefore, for general nondispersive interconnection structures in high speed digital circuits (Appendix D), the proposed time domain modeling technique leads to accurate prediction of signal delay and distortion by incorporating the interconnect model with active circuit models for circuit simulations. However, the models can only be used with signals whose frequencies are limited such that the dispersive effects due to skin effect and dielectric loss are minimal. The dispersive effect of interconnection structures can be taken into account by the proposed hybrid technique with the higher order equivalent circuit models [39].

Finally, future development of electrical characterization and modeling of high speed electronic packages based on this dissertation could be directed towards the development of general dispersive lossy coupled interconnect modeling techniques. In addition, signal integrity issues related with noise budget optimization for high speed circuits need to be investigated by including these models in the design phase of the IC development.

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APPENDIX

Appendix A: Short Pulse TDNA

In recent years, TDR/T measurements have been widely used as a vehicle for characterizing and modeling interconnects. This appendix presents a short–pulse time domain calibration technique based on the developed TDNA [20,61–65]. The accuracy of time domain measurements is enhanced by using time domain transformations to virtually eliminate the FFT associated errors.

Algorithm of Short–Pulse TDNA with Thru–Match–Short Calibration

(i) Short–Pulse Technique

In the past, the technique of short pulse propagation has been used for characterizing the transfer function of microwave antenna, resistive transmission lines, complex dielectrics, the dispersion of microstrip lines from DC up to about 20GHz [32,67,68]. Since the spectrum of short pulse is essentially flat out to the GHz regime, and also the calculated spectrum amplitude and phase are free from the numerical FFT truncation errors, therefore, short pulse propagation has been well recognized as an accurate technique for characterizing interconnects in the microwave bandwidth. In general, the source of impulse is generated by a pulse generator, the differentiated output of a step generator by using a snap–off diode or a passive impulse–forming network [32,67], or an optical pulse from a photo–conductive switch [68]. The method presented here is based on the criterion of causal and linear system constrained to the characteristics of passive interconnect components. A short–pulse with the adjustable pulse–width is then formed by mathematically taking the difference between a step–like waveform and itself with adjustable delay time [69]. Therefore, instead of truly generating a pulse source, short pulse is easily realized by using conventional TDT/R measurements. The usefulness and accuracy of the approach is demonstrated by implementing the algorithm in a production like environment [70].

(ii) TMS Calibration Method

Applying the principle of superposition and the property of time–invariant systems[71,72], the response H(t) of DUT to a pulse is given by

$$V_{IS}(t) * H(t) = V_{OS}(t), \quad V_{IS}(t-T_{pd}) * H(t) = V_{OS}(t-T_{pd}) \tag{a.1}$$

$$[\, V_{IS}(t) - V_{IS}(t-T_{pd})] * H(t) = [V_{OS}(t) - V_{OS}(t-T_{pd})], \tag{a.2}$$

$$\text{and } V_{IP}(t) * H(t) = V_{OP}(t) \tag{a.3}$$

where $*$ is the convolution operator, $V_{IS}(t)$ and $V_{OS}(t)$ are the step–like input source and the corresponding output response, respectively, $V_{IP}(t)$ and $V_{OP}(t)$ are the pulse–like source with pulse width T_{pd} and the corresponding output response, respectively.

By using two–port network analysis, a scattering parameter based signal flow diagram describing the real TDR/T measurements is shown in Figure A.1. The TDR/T measurement non idealities including source impedance, the characteristics of reference cables as well as the transition of SMA–to–trace on the board are grouped in two error box networks. Instead of utilizing a standard sets such as TRL and LRL used for VNA calibration , this calibration method is based on the Thru–Match–Short algorithm (TMS) for the time domain network analysis [20,66]. The corrected two–port S–parameters, S_{ij}^{u} , are obtained from the FFT of the time domain waveforms Vs_{ij}^{x} as given by

$$S_{11}^{U} = \frac{\rho_A - S_{22}^{B} T_1 T_2}{1 - S_{22}^{A} S_{22}^{B} T_1 T_2}, \tag{a.4}$$

$$S_{22}^{U} = \frac{\rho_B - S_{22}^{A} T_1 T_2}{1 - S_{22}^{A} S_{22}^{B} T_1 T_2}, \tag{a.5}$$

$$S_{21}^{U} = (1 - S_{22}^{U} S_{22}^{B}) T_1, \tag{a.6}$$

$$S_{12}^{U} = (1 - S_{11}^{U} S_{22}^{A}) T_2, \tag{a.7}$$

where

$$T_1 = \frac{Vs_{21}^{U} Vs_{12}^{T} (1 - S_{22}^{A} \rho_A)}{Vs_{12}^{T} Vs_{21}^{T} - Vs_{11}^{TM} Vs_{22}^{TM}}, \tag{a.8}$$

$$T_2 = \frac{Vs_{12}^{U} Vs_{21}^{T} (1 - S_{22}^{B} \rho_B)}{Vs_{12}^{T} Vs_{21}^{T} - Vs_{11}^{TM} Vs_{22}^{TM}}, \tag{a.9}$$

$$\rho_A = \frac{M^A \rho_A}{M^A \rho_s S_{22}^{A} + 1 - S_{22}^{A} \rho_s}, \tag{a.10}$$

$$\rho_B = \frac{M^B \rho_A}{M^B \rho_s S_{22}^{B} + 1 - S_{22}^{B} \rho_s}, \tag{a.11}$$

$$S_{22}^{A} = Vs_{22}^{TM} \rho_s \left(1 - \frac{Vs_{11}^{TM}(Vs_{22}^{TM} - Vs_{22}^{SM})}{Vs_{12}^{T} Vs_{21}^{T} Vs_{22}^{SM}}\right), \tag{a.12}$$

$$S_{22}^{B} = Vs_{11}^{TM} \rho_s \left(1 - \frac{Vs_{22}^{TM}(Vs_{11}^{TM} - Vs_{11}^{SM})}{Vs_{12}^{T} Vs_{21}^{T} Vs_{11}^{SM}}\right), \tag{a.13}$$

$$M^A = \frac{Vs_{11}^{UM}}{Vs_{11}^{SM}}, \quad M^B = \frac{Vs_{22}^{UM}}{Vs_{22}^{SM}}, \tag{a.14}$$

$$Vs_{ij}^{xy} = Vs_{ij}^{x} - Vs_{ij}^{y}, \text{ and } Vs_{ij}^{x} = FFT\,[Vs_{ij}^{x}(t)]. \tag{a.15}$$

In the above expression, j is the excitation port, i is the measurement port and x denotes the TMS standard sets or unknown being measured. ρ_A is the short circuit reflection coefficient and $Vs_{ij}^{x}(t)$ are pulse–like waveforms obtained by taking the difference between the measured step–like TDR/T waveforms $V_{ij}^{x}(t)$ with itself delayed in time T_{pd}. High quality match and short circuit terminations are available for many interconnect transmission line structures, the match standard could even be implemented using a reference impedance transmission line of sufficient length. However, TDR/T measurement has the advantage of natural time windowing in the time domain since only a finite duration of response is acquired. The algorithm described above is based on the criterion of causal and linear system constrained on the passive interconnect structures. The accuracy of the results is dependent on the TDR/T system bandwidth and the accuracy of calibration standards.

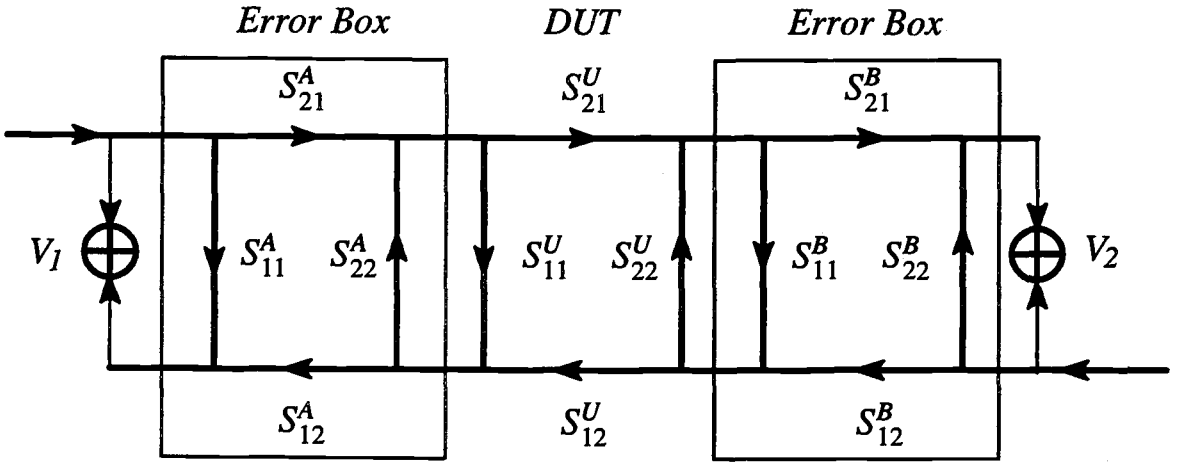

Figure a.1, Flow diagram of the two port time domain network analysis system

Appendix B: Four–Port Network of Coupled Transmission Lines

Consider a general coupled interconnection structure as shown in Figure 3.6, the coupled transmission line equations are given by equations (3.21) and (3.22), such a structure can be characterized by a four–port network. The basic matrix equation of of the four–port network for a single coupled segment is then given by

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{21} & Z_{31} & Z_{41} \\ Z_{21} & Z_{22} & Z_{32} & Z_{31} \\ Z_{31} & Z_{32} & Z_{22} & Z_{21} \\ Z_{41} & Z_{31} & Z_{21} & Z_{11} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix}, \tag{b.1}$$

where

$$Z_{11} = \frac{Z_{c1}\coth(\beta_c l)}{1-\frac{R_c}{R_\pi}} + \frac{Z_{\pi 1}\coth(\beta_\pi l)}{1-\frac{R_\pi}{R_c}} \tag{b.2}$$

$$Z_{12} = \frac{Z_{c1}R_c\coth(\beta_c l)}{1-\frac{R_c}{R_\pi}} + \frac{Z_{\pi 1}R_\pi\coth(\beta_\pi l)}{1-\frac{R_\pi}{R_c}} \tag{b.3}$$

$$Z_{13} = \frac{\frac{Z_{c1}R_c}{\sinh(\beta_c l)}}{1-\frac{R_c}{R_\pi}} + \frac{\frac{Z_{\pi 1}R_\pi}{\sinh(\beta_\pi l)}}{1-\frac{R_\pi}{R_c}} \tag{b.4}$$

$$Z_{14} = \frac{\frac{Z_{c1}}{\sinh(\beta_c l)}}{1-\frac{R_c}{R_\pi}} + \frac{\frac{Z_{\pi 1}}{\sinh(\beta_\pi l)}}{1-\frac{R_\pi}{R_c}} \tag{b.5}$$

$$Z_{22} = \frac{Z_{c1}R_c^{\,2}\coth(\beta_c l)}{1-\frac{R_c}{R_\pi}} + \frac{Z_{\pi 1}R_\pi^{\,2}\coth(\beta_\pi l)}{1-\frac{R_\pi}{R_c}} \tag{b.6}$$

$$Z_{23} = \frac{\frac{Z_{c1}R_c^{\,2}}{\sinh(\beta_c l)}}{1-\frac{R_c}{R_\pi}} + \frac{\frac{Z_{\pi 1}R_\pi^{\,2}}{\sinh(\beta_\pi l)}}{1-\frac{R_\pi}{R_c}} \tag{b.7}$$

and c–mode and pi–mode characteristic impedances are defined by

$$Z_{c1} = \frac{z_1 z_2 - z_m{}^2}{\beta_c (z_2 - z_m R_{c)}} \tag{b.8}$$

$$Z_{\pi 1} = \frac{z_1 z_2 - z_m{}^2}{\beta_\pi (z_2 - z_m R_\pi)} \tag{b.8}$$

where

$z_1 = j\omega L_1$, $z_2 = j\omega L_2$, and $z_m = j\omega L_m$.

and

$$R_c = \frac{1}{2b_1}\left\{(a_1 + a_2) + \sqrt{(a_1 - a_2)^2 + 4b_1 b_2}\right\} \tag{b.9}$$

$$R_\pi = \frac{1}{2b_1}\left\{(a_1 + a_2) - \sqrt{(a_1 - a_2)^2 + 4b_1 b_2}\right\} \tag{b.10}$$

$$a_1 = j\omega(C_1 + C_m)\cdot j\omega L_1 - j\omega C_m \cdot j\omega L_m \tag{b.11}$$

$$a_2 = j\omega(C_2 + C_m)\cdot j\omega L_2 - j\omega C_m \cdot j\omega L_m \tag{b.12}$$

$$b_1 = -j\omega C_m \cdot j\omega L_1 + j\omega(C_2 + C_m)\cdot j\omega L_m \tag{b.13}$$

$$b_2 = -j\omega C_m \cdot j\omega L_2 + j\omega(C_1 + C_m)\cdot j\omega L_m \, . \tag{b.14}$$

The [ABCD] matrix of a coupled line segment is then readily to be obtained from [Z] matrix [80] in equation (b.1) for computing the transmission voltage at port 4 and the coupled voltages at port 2 and port 2 as long as the excitation source is given at port 1.

Appendix C: Scattering Matrix–Based Transmission Line Equations

Consider a lossless nonuniform interconnection structure, such an interconnect can be characterized by the lumped element model or the distributed element model as shown in Figure 2.6. The line voltage and current can the be described by a set of transmission line equations as given by

$$\frac{\partial v(x,t)}{\partial x} = -L(x)\frac{\partial i(x,t)}{\partial t}, \tag{c.1}$$

$$\frac{\partial i(x,t)}{\partial x} = -C(x)\frac{\partial v(x,t)}{\partial t}, \tag{c.2}$$

where $v(x,t)$ is the voltage variable and $i(x,t)$ is the current variable on the line. Let the normalized voltages and currents on the line be defined as

$$V(x,t) = \frac{1}{\sqrt{Z_o(x)}}v(x,t) \tag{c.3}$$

$$I(x,t) = \sqrt{Z_o(x)}\,i(x,t) \tag{c.4}$$

$$\text{where } Z_o(x) = \sqrt{\frac{L(x)}{C(x)}} \text{ and } Y_o(x) = [Z_o(x)]^{-1} \tag{c.5}$$

are the local characteristic impedance and admittance at the position x on the line, then

$$\frac{\partial v(x,t)}{\partial t} = \sqrt{Z_o(x)}\frac{\partial V(x,t)}{\partial t} + V(x,t)\frac{\partial \sqrt{Z_o(x)}}{\partial t}$$

$$= -L(x)\frac{1}{\sqrt{Z_o(x)}}\frac{\partial I(x,t)}{\partial t} \tag{c.6}$$

$$\text{and } \frac{\partial i(x,t)}{\partial t} = \frac{1}{\sqrt{Z_o(x)}}\frac{dI(x,t)}{dx} + I(x,t)\frac{d}{dx}\left[\frac{1}{\sqrt{Z_o(x)}}\right]$$

$$= -C(x)\sqrt{Z_o(x)}\frac{dV(x,t)}{dt} \tag{c.7}$$

Therefore, the transmission line equations can be rewritten as

$$\frac{\partial V(x,t)}{\partial x} + \frac{1}{\partial}\frac{d}{dx}\ln Z(x)V(x,t) = -\sqrt{L(x)C(x)}\frac{\partial I}{\partial t} \tag{c.8}$$

$$\frac{\partial I(x,t)}{\partial x} - \frac{1}{\partial}\frac{d}{dx}\ln Z(x)I(x,t) = -\sqrt{L(x)C(x)}\frac{\partial V}{\partial t}\ . \tag{c.9}$$

Further, the alternative transmission line equations (c.8) and (c.9) are expressed in terms of the forward wave variable

$$a(z,t) = \frac{1}{2}\left[\frac{1}{\sqrt{Z_o(z)}}v(z,t) + \sqrt{Z_o(z)}\,i(x,t)\right] \tag{c.10}$$

and the backward wave variable

$$b(z,t) = \frac{1}{2}\left[\frac{1}{\sqrt{Z_o(z)}}v(z,t) - \sqrt{Z_o(z)}\,i(x,t)\right], \tag{c.11}$$

where $z(x) = \int \frac{1}{v(y)}dy$ is the propagation delay time for a wave transmitting from x=0 to the position x, and $v(x)$ is the local velocity on the line. Then the symmetrical scattering matrix–based transmission line equations are given as

$$\frac{\partial}{\partial z}\begin{bmatrix} a(z,t) \\ b(z,t) \end{bmatrix} = \begin{bmatrix} -\frac{\partial}{\partial t} & -\rho(z) \\ -\rho(z) & \frac{\partial}{\partial t} \end{bmatrix}\begin{bmatrix} a(z,t) \\ b(z,t) \end{bmatrix}. \tag{c.12}$$

where is the local reflectivity function and the corresponding discrete type scattering matrix is described at chapter 1. For example, if the characteristic impedance over a portion of the line is constant, e.g., $Z_o(x) = Z_o$, then $\rho(z) = 0$, the solution of equation (c.12) is given by

$$a(z,t) = a(z - t) \tag{c.13}$$

and $b(z,t) = b(z + t)$, (c.14)

therefore the forward and backward wave variables act as a pure time dely and advanced operators, respectively.

For the resistive lossy interconnection structure, the transmission line equations are

$$\frac{\partial v(x,t)}{\partial x} = -R(x)i(x) - L(x)\frac{\partial i(x,t)}{\partial t}, \tag{c.15}$$

$$\frac{\partial i(x,t)}{\partial x} = -C(x)\frac{\partial v(x,t)}{\partial t}. \tag{c.16}$$

Again, by substituting the normalized voltage and current variables as given by equations (c.3) and (c.4), equations (c.15) and (c.16)

$$\frac{\partial V}{\partial z} + \frac{1}{2}\frac{d}{dz}\ln Z(z)V = -\frac{R}{L}I - \frac{\partial I}{\partial t} \tag{c.17}$$

$$\frac{\partial I}{\partial z} - \frac{1}{2}\frac{d}{dz}\ln Z(z)V = -\frac{\partial V}{\partial t}. \tag{c.18}$$

Now, by introducing the forward and backward wave variables as given by equations (c.10) and (c.11), the resistive lossy transmission line equations is rewritten as

$$\frac{\partial \hat{a}}{\partial z} + \frac{\partial \hat{a}}{\partial t} = -\Lambda\hat{a} - \left(\frac{1}{2}\frac{d}{dx}\ln Z(z) - \Lambda\right)\hat{b}(x) \tag{c.19}$$

$$\frac{\partial \hat{b}}{\partial z} + \frac{\partial \hat{b}}{\partial t} = -\left(\frac{1}{2}\frac{d}{dx}\ln Z(z) + \Lambda\right)\hat{a}(x) + \Lambda\hat{b}. \tag{c.20}$$

where $\frac{R(x)}{L(x)} = \Lambda(x)$.

Therefore, the resistive lossy transmission line equations can be expressed in a form of asymmetrical scattering matrix as given by

$$\frac{\partial}{\partial z}\begin{bmatrix}\hat{a}(z,t)\\ \hat{b}(z,t)\end{bmatrix} = \begin{bmatrix}-\frac{\partial}{\partial t} & -\eta(z)\\ -\rho(z) & \frac{\partial}{\partial t}\end{bmatrix}\begin{bmatrix}\hat{a}(z,t)\\ \hat{b}(z,t)\end{bmatrix} \tag{c.21}$$

where $\eta(z) = \frac{1}{2}\frac{d}{dx}\ln Z_o(z) + \frac{1}{2}\left(\frac{R(x)}{L(x)}\right)\exp\left[-\int_0^z (\Lambda(x))dx\right]$ (c.22)

and $\rho(z) = \left(\frac{1}{2}\frac{d}{dx}\ln Z_o(z) + \frac{1}{2}(\Lambda(z))\right)\exp\left[\int_0^z \Lambda(u)du\right]$. (c.23)

Appendix D: Frequency Domain Characterization of Interconnects and Materials by TDR/T Technique

The purpose of this appendix aims at characterizing uniform interconnects and packaging materials in the frequency domain by using TDT/R measurements. In order to demonstrate this technique, a test fixture of strip line interconnect was made on Printed Circuit Board (PCB). The packaging material was made by epoxy glass which is commonly used on board level electronic packaging systems. In most of practical cases, SMA to strip line transitions are very common in the test board for high speed digital system measurements since strip line must via SMA connectors to connect with reference coaxial lines and measurement systems. As a result, most of the measured waveforms are corrupted in higher frequencies due to the discontinuity of SMA–to–strip line. In order to de–embed the characteristics of a DUT between two transitions, short pulse TDNA with Thru–Match–Short (TMS) calibration procedure (Appendix A) is applied to move the reference plane behind SMA connectors, thus, an undisturbed transfer function of the interconnect is obtained. Furthermore, the electrical characteristics of DUT, such as complex permittivity and dielectric loss of the dielectric material, and complex impedance, conductor loss and attenuation of the interconnect can be extracted from the measured transfer function in the frequency domain, by applying the derived equations based on quasi–TEM field equations.

(i) Electrical Characterization

The theory of this technique is based on a TEM propagation behavior for the lossless transmission line, or a quasi–TEM propagation assumed to be justified for lossy transmission lines. For a transmission line (TL) of length ℓ connected at the sending end with source impedance $Z_s = Z_o$ and terminated in its characteristic impedance Z_o, and with the propagation constant γ, the transfer function of TL can be in terms of the measured input voltage and the measured output voltage as functions of complex frequency, and also related to S–parameter measurements as

$$H(f) = S_{21}(f) = S_{12}(f) = \frac{V_{in}(f)}{V_{out}(f)} = e^{-rl} \tag{d.1}$$

where in general, the characteristic impedance is defined as

$$Z_o(f) = \sqrt{\frac{Z(f)}{Y(f)}} = \sqrt{\frac{R(f) + j\omega L}{G(f) + j\omega C(f)}} \tag{d.2}$$

and the propagation function is denoted as

$$\gamma = \sqrt{[R(f) + j\omega L][G(f) + j\omega C(f)]}$$

$$= \alpha(f) + j\beta(f) + j\omega Tp \tag{d.3}$$

Note that $\alpha(f)$, $\beta(f)$ are attenuation and phase shift introduced by the losses (conductor loss and dielectric loss), while the term ωTp represents the phase shift taken from input to output of the lossless TL of length ℓ . The total impedance per unit length $Z_o(f)$ is given by

$$Z_o(f) = R_{dc} + Z_{sk}(f) + j\omega L_e = R(f) + j\omega L \tag{d.4}$$

where R_{dc} is the DC resistance of TL, $Z_{sk}(f)$ is the skin effect impedance, L_e is the external inductance, $R(f)$ is the effective frequency dependent resistance, L is the effective inductance of TL. The total admittance per unit length $Y(f)$ is also given by

$$Y(f) = G(f) + j\omega C(f) = G(f) + j\omega\left[C_h + C_{ac}(f)\right] \tag{d.5}$$

where $G(f)$ is the dielectric shunt conductance, C_h is the high frequency limit of the capacitance and $C_{ac}(f)$ represents the ac variation of the capacitance due to the real part of the complex dielectric permittivity.

By carefully examining the voltage transfer function of the lossy TL, an alternative definition can be expressed as

$$H(f) = e^{-r(f)l} = H_m(f)e^{-j\omega Tp} \tag{d.6}$$

which means a transfer function of TL is a non minimum–phase network and can be resolved into the cascade of a minimum–phase function $H_m(f)$ and the all pass func-

tion $e^{-j\omega Tp}$ [71,72,75]. The assumption of minimum–phase property has the great importance in dealing with the extraction of attenuation from the measured transfer function, since total attenuation can then be solely obtained from $\alpha(f) = -\ln(H(f))$. Theoretically, $\alpha(f)$ and $\beta(f)$ are uniquely related and can be obtained by using the modified Hilbert Transforms [72].

Next, the equations for extracting the electrical characteristics from the measured transfer function is derived by using the following procedures. First, the transfer function can be measured as $S_{21}(f)$ by using Short Pulse TDNA with TMS calibration, and is mathematically expressed as

$$H(f) = e^{-(\alpha_m(f) + j\beta_m(f))l} \tag{d.7}$$

where the measured attenuation is denoted as $\alpha_m(f)$ and the measured phase function is denoted as $\beta_m(f)$.

For considering most of the applications dealing with interconnects and packages of high speed computer systems, the useful equations for extracting the attenuation and the phase function are written as,

$$\begin{aligned}\alpha_m(f) &\approx \frac{G(f)}{2}\sqrt{\frac{L}{C_h + C_{ac}(f)}} + \frac{R(f)}{2}\sqrt{\frac{C_h + C_{ac}}{L}} \\ &= \frac{G(f)}{2}Z_o(f) + \frac{R(f)}{2Z_o(f)} \\ &= \alpha_d(f) + \alpha_c(f)\end{aligned} \tag{d.8}$$

and

$$\begin{aligned}\beta_m(f) &\approx \omega\sqrt{LC_h} + \omega\sqrt{LC_{ac}} \\ &= \omega T + \omega\sqrt{LC_{ac}} \\ &= \omega Tp + \beta(f)\end{aligned} \tag{d.9}$$

where $\alpha_c(f)$, $\alpha_d(f)$ are denoted as the conductor loss and the dielectric loss, respectively, and $Z_o(f)$ is the frequency dependent complex impedance. Further, the frequency

dependent resistance can be computed for given physical parameters of the interconnect by using the following expression [77]

$$R(f) = R_{dc}\left[\frac{1 + e^{-\zeta t}\eta}{\left(\frac{1-e^{-\zeta t}}{\zeta t}\right) + e^{-2\zeta t}\left(\frac{e^{\zeta t}-1}{\zeta t}\right)}\right] \qquad \text{(d.10)}$$

where

$$R_{dc} = \frac{1}{wt\sigma}, \quad (\sigma : \text{conductivity})$$

$$\zeta = \sqrt{j\omega\mu_0\sigma}, \quad (\mu_0 : \text{vacuum permeability})$$

$$\eta = \frac{\eta_0 - \sqrt{\frac{j\omega\mu_0}{\sigma}}}{\eta_0 + \sqrt{\frac{j\omega\mu_0}{\sigma}}}, \quad (\eta_0 : \text{intrinsic wave impedance})$$

and w, t are the width and the thickness of the conductor corresponding to the interconnect under test.

For computing the electrical characteristics of the dielectric material, the attenuation and the phase function shall be in terms of the dielectric permittivity as given by

$$\beta_m(f) = \omega\sqrt{L\epsilon_h} + \frac{\omega\epsilon_{ac}(f)}{2}\sqrt{\frac{\mu_0}{\epsilon_h}} \qquad \text{(d.11)}$$

and

$$\alpha_m(f) = \alpha_c(f) + \frac{\omega\epsilon''}{2}\sqrt{\frac{\mu_0}{\epsilon_h + \epsilon_{ac}(f)}} \qquad \text{(d.12)}$$

where the conductor loss $\alpha_c(f)$ due to the dc resistance and the skin effects is readily obtained if the complex characteristic impedance of the interconnect can be computed.

In general, most of the dielectric materials for microwave circuits and high speed digital systems are low loss materials, such as epoxy glass, ceramic, polymide,

etc., however, the dielectric loss is much smaller than the total admittance of the interconnect in the frequency range of interest. Thus, the corresponding complex characteristic impedance can be expressed as

$$Z_o(f) = \sqrt{\frac{R(f) + j\omega L}{G(f) + j\omega C(f)}}$$

$$\approx \frac{\beta_m(f) - j\alpha_m(f)}{\omega[\epsilon_h + \epsilon_{ac}(f)]C_0} \qquad \text{(d.13)}$$

Note that ϵ_h and $\epsilon_{ac}(f)$ represent the intrinsic permittivity and the ac permittivity of the real part of the complex permittivity for the dielectric material, and $\epsilon''(f)$ is denoted as the imaginary part of the frequency dependent complex permittivity, and $C0$ is the calculated free space capacitance corresponding to the DUT. In fact, most of the practical cases, the dispersion of the dielectric material resulting in the frequency dependent capacitance $C(f)$ is very small, which means $\epsilon_h \gg \epsilon_{ac}(f)$ and $\epsilon_h \gg \epsilon''(f)$ [26,27]. Thus, the measured low frequency capacitance per unit length of the interconnect by using TDR/T measurements can be used to determined the complex impedance as given by

$$Z_o(f) \approx \frac{Z_m[\beta_m(f) - j\alpha_m(f)]}{\omega Tp} \qquad \text{(d.14)}$$

where Z_m is the measured characteristic impedance of the interconnect by using TDR/T measurements. Here, in order to place the reference point behind the SMA–to–interconnect transitions, time domain layer peeling technique should be applied to extract the characteristic impedance for computing the complex characteristic impedance.

Finally, the complex permittivity of the dielectric materials can then be obtained as

$$\epsilon'(f) = \frac{2\sqrt{\epsilon_h}v_0\beta_m(f)}{\omega l} + \epsilon_h \tag{d.15}$$

$$\epsilon''(f) = \frac{2\sqrt{\epsilon'(f)}[\alpha_m(f) - \alpha_c(f)]}{\eta_0\omega l} \tag{d.16}$$

where v_0 is the speed of light in vacuum.

(ii) Experimental Results

The interconnection structure under test is a strip line made on printed circuit boards with FR–4 substrate material. Tektronix 11801 TDR/T system with a differentiated short pulse (50ps pulse width) is used to obtain reflection and transmission responses as shown in Figure d.1. The schematic of test lines with the associated de–embedding test fixtures is shown in Figure d.2. The frequency domain response of DUT is then extracted from the TDR/T measured data of DUT together with de–embedding test fixtures. Figure d.3 shows attenuation and phase constant of transmission response vs frequencies for the test line. Figure d.4 shows the measured complex characteristic impedance of the interconnect. Finally, the measured dielectric permittivity vs frequencies is shown in Figure d.5 and the nominal value of dielectric permittivity is 4.35 for this typical material.

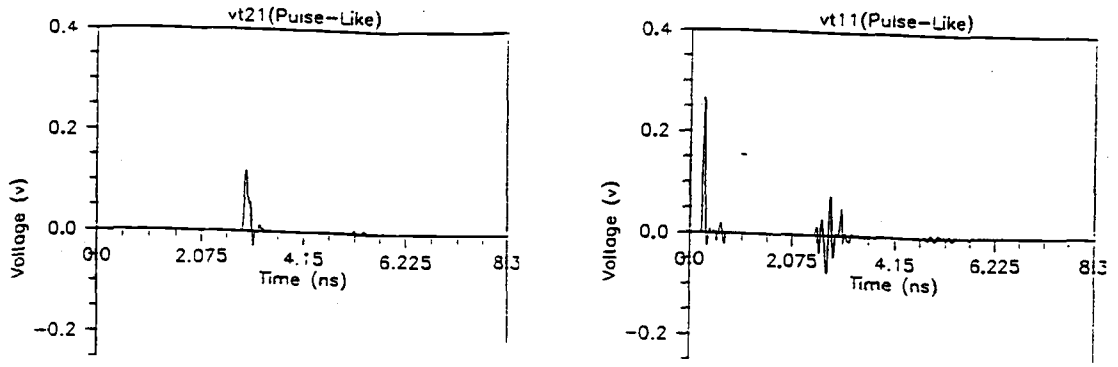

Figure d.1, (a) The measured transmission pulse, (b) Input pulse and reflected waveform.

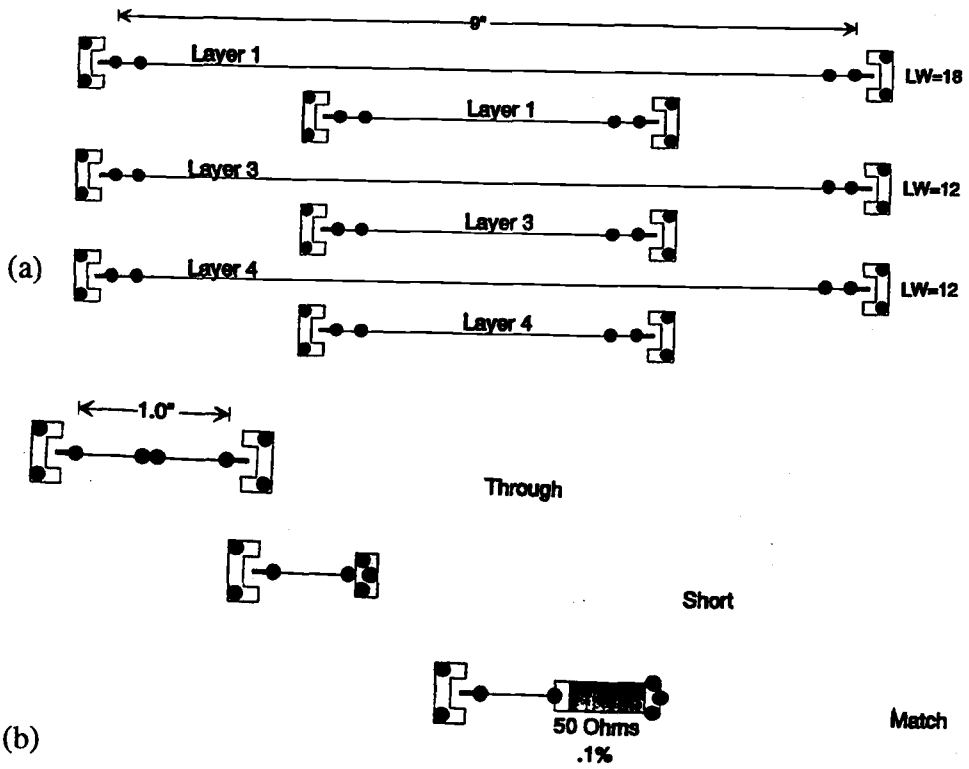

Figure d.2, (a) Test lines. (b) De–embedding test fixtures.

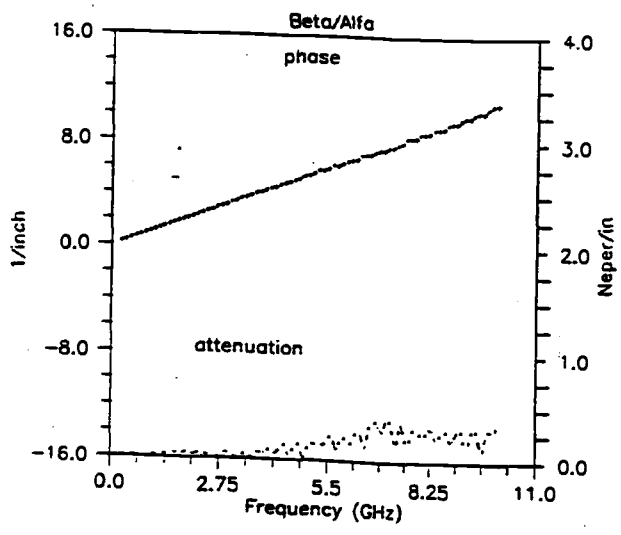

Figure d.3, The measured attenuation and phase constant.

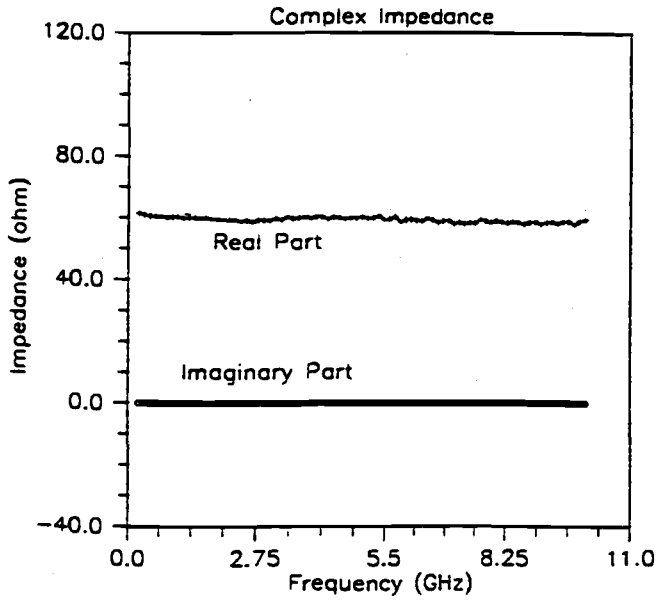

Figure d.4, The measured complex impedance.

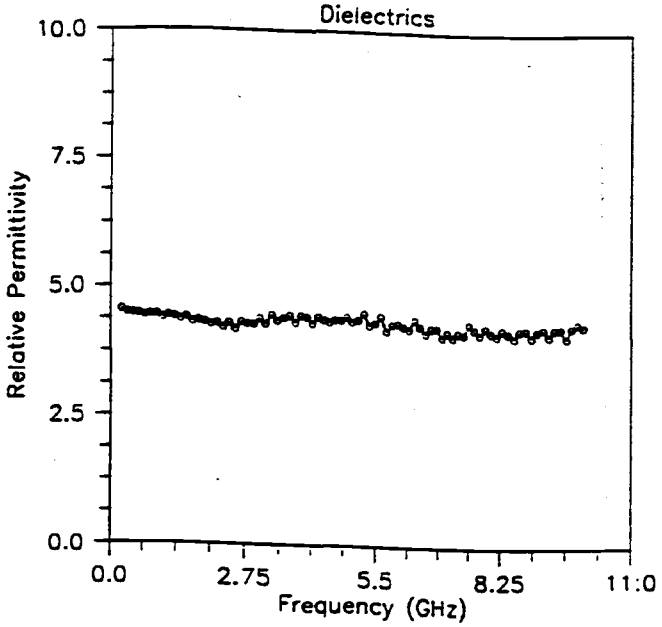

Figure d.5, The measured dielectric permittivity.