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James S. Ayers for the degree of Master of Science in
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Abstract approved:

Redacted for Privacy

Terri S. Fiez

Redacted for Privacy

Kartikeya Mayaram

An analysis of substrate noise coupling in mixed-signal circuits has been performed in the TSMC 0.25 $\mu$m lightly doped and heavily doped CMOS processes. Methods to minimize noise coupling in both the chip design and board design phases are presented along with techniques for accurate circuit simulation of noise coupling. Measurements from test chips validate simulations performed using Silencer!. Suggestions for reducing substrate noise coupling are also provided.

Measurements and simulations show a 15 dB improvement in substrate noise coupling in the lightly doped substrate when compared with the heavily doped substrate with the backplane floating. When no mutual inductance is present and the backplane is grounded through a low impedance, a 17.5 dB improvement in substrate noise coupling is observed in the heavily doped process. Simulations with guard rings show an 8 dB improvement in substrate noise cou-

pling in the heavily doped case and 3.4 dB improvement in the lightly doped case.

# A Comparison of Substrate Noise Coupling in Heavily Doped and Lightly Doped Substrates for Mixed-Signal Circuits

by

James S. Ayers

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APPROVED:

Redacted for Privacy

Co-Major Professor, representing Electrical and Computer Engineering

Redacted for Privacy

Co-Major Professor, representing Electrical and Computer Engineering

Redacted for Privacy

Director of the School of Electrical Engineering and Computer Science

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TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

Page

LIST OF FIGURES

Figure Page

LIST OF TABLES

LIST OF APPENDIX FIGURES

Figure Page

LIST OF APPENDIX FIGURES (Continued)

Figure | Page

# A Comparison of Substrate Noise Coupling in Heavily Doped and Lightly Doped Substrates for Mixed-Signal Circuits

## 1. INTRODUCTION

### 1.1. Motivation

As Moore's law continues to predict integrated circuit (IC) scaling, the industry drive is to make chips faster with higher functionality. The market for dense, highly functional, and custom integrated circuits is soaring due to a constant demand for portable electronics such as cell phones, personal digital assistants (PDA's), and laptop computers. Many circuits that were realized on circuit boards even as recently as a few years ago are now being integrated into a single die referred to as a system on chip (SoC). These systems often require a combination of analog, digital, and radio frequency (RF) functionality to achieve the desired performance, and consequently, circuitry of each of these types must be integrated together on the same silicon substrate [1].

Many challenges arise when integrating analog, digital, and RF electronic building blocks in a single IC. One of these challenges is the noise coupling from the digital circuits to the analog circuits. As the clock speed in digital circuits increases, the noise coupling becomes a very significant factor in the performance of analog circuits [2]. The ability to predict and reduce the noise in mixed-signal chips is essential for designers to continue to follow the trend of faster and more functional chips [3].

## 1.2. Thesis Description and Outline

The choice of the type of substrate (lightly doped or heavily doped) used for IC fabrication is one way of controlling the substrate noise issues in large SoCs. A lightly doped substrate has a higher resistivity and can provide a larger barrier for noise coupling, but it can also cause problems associated with latchup in the digital circuity. Heavily doped substrates, having lower resistivity, provides sensitive analog circuitry little protection against substrate noise coupling while also being more expensive to fabricate due to precise equipment needed to deposit the epitaxial layer.

This thesis examines the substrate noise coupling phenomenon in both heavily doped and lightly doped processes. Chapter 2 provides an overview of the two fabrication processes and an explanation of the substrate coupling model. Chapter 3 details the experimental set up and circuit design. An analysis of the pin parasitics and the efforts taken to eliminate them is also explained. The methodology used for simulation and the inclusion of other parasitics is described in Chapter 4. Chapter 5 contains the simulated results and measurements from test chips. Techniques to reduce substrate noise coupling through the use of guard rings and circuit design are also investigated. Chapter 6 generalizes the results found in Chapter 5 using simple two contact examples. Finally, Chapter 7 provides conclusions and ideas for future work on this subject.

# 2. SUBSTRATE PROFILES AND MODEL

## 2.1. Heavily Doped Substrates

Heavily doped substrates are the most widely used type of substrate for digital circuits today. Although they are primarily employed for large digital designs, they are also used by analog designers for mixed-signal SoCs. The doping profile for a typical heavily doped process is shown in Figure 2.1.

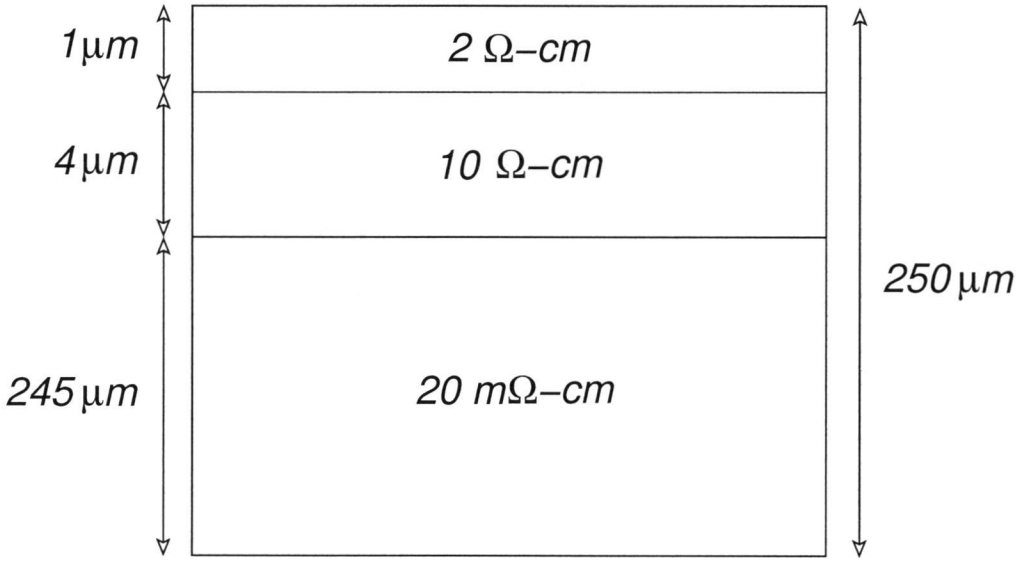



FIGURE 2.1. A cross section of a typical heavily doped CMOS substrate.

The heavily doped substrate has three distinct layers. The bulk of the substrate which is a heavily doped p+ region, the lightly doped epitaxial layer, and the p+ channel stop layer.

One means of isolation in the heavily doped substrate is the lightly doped epitaxial and channel stop layers. These layers provide the main coupling path between contacts spaced at a distance of less than four times the thickness of the epitaxial layer [4]. Beyond this spacing the resistance of the channel stop layer

becomes much greater than the resistance to the heavily doped bulk resulting in most of the noise currents flowing down through the heavily doped bulk and coupling up to the sensitive analog circuitry.

### 2.2. Lightly Doped Substrates

A profile of a typical lightly doped process is shown in Figure 2.2. The lightly doped substrate is made of two layers which include the lightly doped p-type substrate and the more heavily doped p+ channel stop layer.

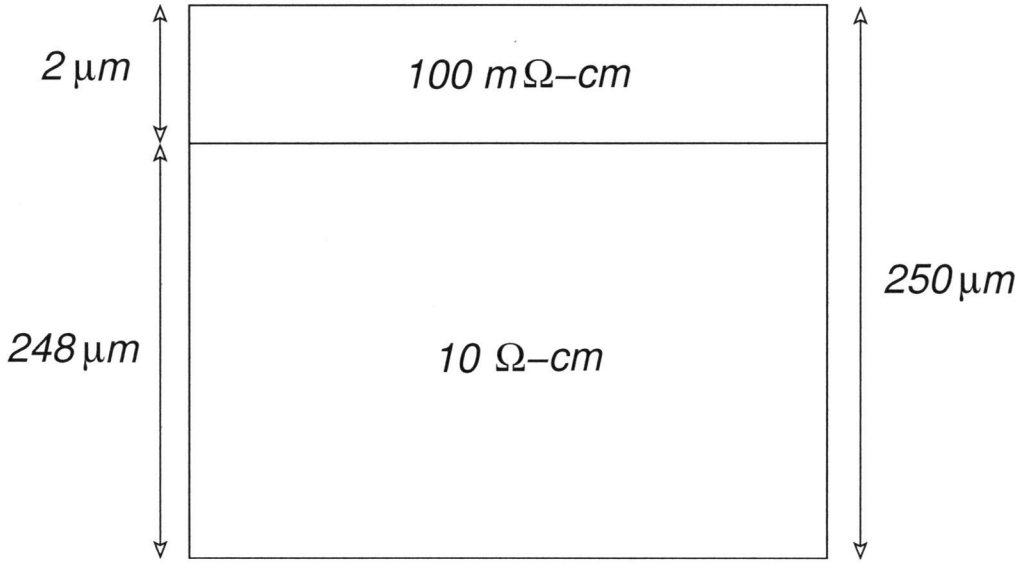



FIGURE 2.2. A cross section of a typical lightly doped CMOS substrate.

The lightly doped substrate is less expensive [5] than the heavily doped substrate while also providing much better isolation between circuits. They are generally less popular for SoC designs because of problems associated with latchup.

## 2.3. Substrate Coupling Model

The model used to simulate the substrate noise coupling is the simple $\pi$ model shown in Figures 2.3 and 2.4. The p+ to p+ model is made up of three resistors. $R_{12}$ represents the path between contacts that is formed in the top p+ channel stop layer (and epitaxial layer in the heavily doped process) while $R_{11}$ and $R_{22}$ represent the path to the backplane.

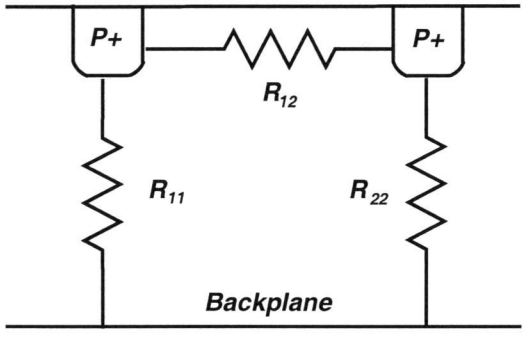



FIGURE 2.3. Substrate coupling model for two p+ contacts.

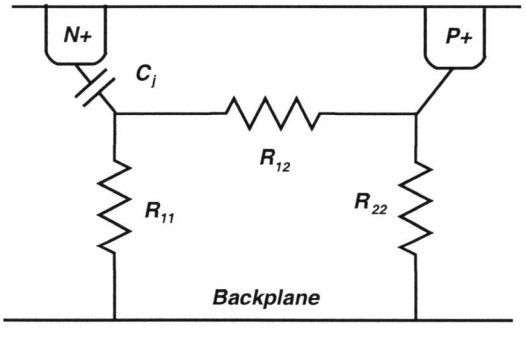



FIGURE 2.4. Substrate coupling model for n+ and p+ contacts.

The n+ to p+ coupling model is the same as the p+ to p+ model with a capacitor added to model the junction capacitance between the n+ and the p-type substrate.

The substrate coupling models used in this thesis have been generated by EPIC [6]. An input file containing geometric data (contact size and spacing) and substrate resistivity data (as in Figures 2.1 and 2.2) is used to calculate the resistive network. EPIC uses the Green's function method to first find the impedance matrix for the contacts in the input file. The impedance matrix is then inverted to get the admittance matrix which is used to calculate the values for $R_{11}$, $R_{22}$, and $R_{12}$ in a two contact case.

In this work the PMOS transistors have been neglected due to the junction capacitance between the n-well and the substrate. This capacitance attenuates most of the low frequency (less than 2GHz) noise whereby this contribution can be neglected [7].

# 3. EXPERIMENTAL SETUP

The main motivation of this work is to compare substrate noise coupling for two identical designs fabricated in heavily and lightly doped substrates. An op-amp and a stepped buffer in close proximity were fabricated in the TSMC 0.25 $\mu$m CMOS process. The op-amp and stepped buffer are within 50 $\mu$m of each other to simulate a situation with severe substrate noise coupling that a designer would face in an actual mixed-signal design. A die perimeter ring has been included at the periphery of the chip to easily ground the chip's substrate in the heavily doped process.

The layout, packaging, test board, and equipment used are the same in both the heavily doped and lightly doped cases. This ensures that the only differences seen between the two cases are those due to the different substrates.

## 3.1. Operational Amplifier Design

An op-amp is a widely used analog building block in most of today's mixed-signal circuit designs. The op-amp chosen for this work is taken from a mixed-signal design where it is used as an analog buffer to drive a low impedance load.

The op-amp is a two stage design that utilizes two sets of input differential pairs in order to achieve a high dynamic range [8]. The two sets of input pairs increase the dynamic range of the amplifier by letting the input signal amplitude be almost as large as the power supply. A schematic of the op-amp is shown in Figure 3.1.

Transistors M1, M2, M3, and M4 compose the two differential pairs. Transistors M5, M6, M7, and M8 allow the amplified signal from the NMOS input pair to be summed with that from the PMOS input pair at the drain of transistors

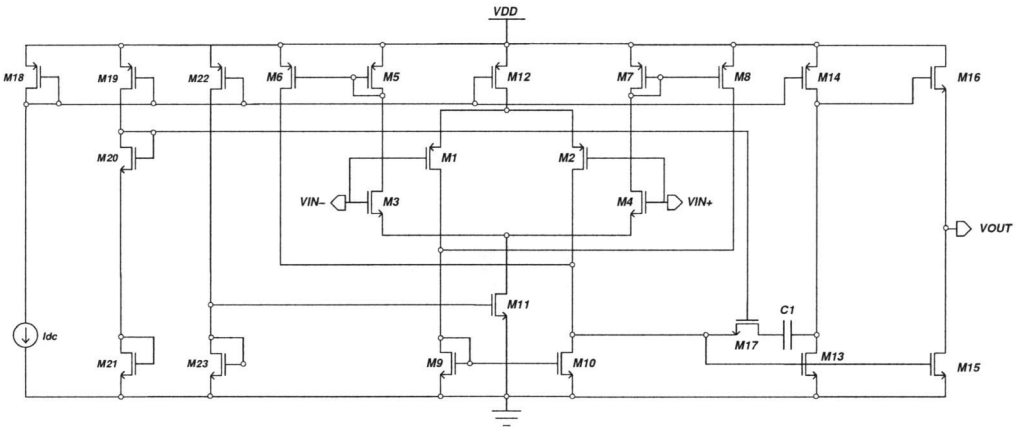



FIGURE 3.1. A high swing two stage op-amp.

M1 and M2. When both of the input pairs are active, the small-signal gain of the first stage is given by:

$$a_{v1} = (g_{m1} + g_{m3})/[g_{ds6} + g_{ds2} + g_{ds10}] \tag{3.1}$$

where M10 carries twice the DC current as M6 and M2. The gain for the entire op-amp (neglecting the output buffer) can easily be found by multiplying the gain from the first stage (3.1) by the gain of the second stage resulting in:

$$a_v = [g_{m13}/(g_{ds13} + g_{ds14})]\{(g_{m1} + g_{m3})/[g_{ds6} + g_{ds2} + g_{ds10}]\}. \tag{3.2}$$

The op-amp is compensated with a transistor biased in the triode region (M17) and a 1 pF capacitor. Transistors M15 and M16 provide a buffer that allows the op-amp to drive a resistive load. The gain of this buffer is:

$$a_{vb} = g_{m16}/[G_L + g_{m16} + g_{mb16} + g_{ds16} + g_{ds15}] \tag{3.3}$$

where $G_L$ is the load admittance and $g_{mb16}$ is the body-effect conductance of M16 [9]. These transistors are sized to minimize the head room voltage required and maximize the total output swing of the amplifier.

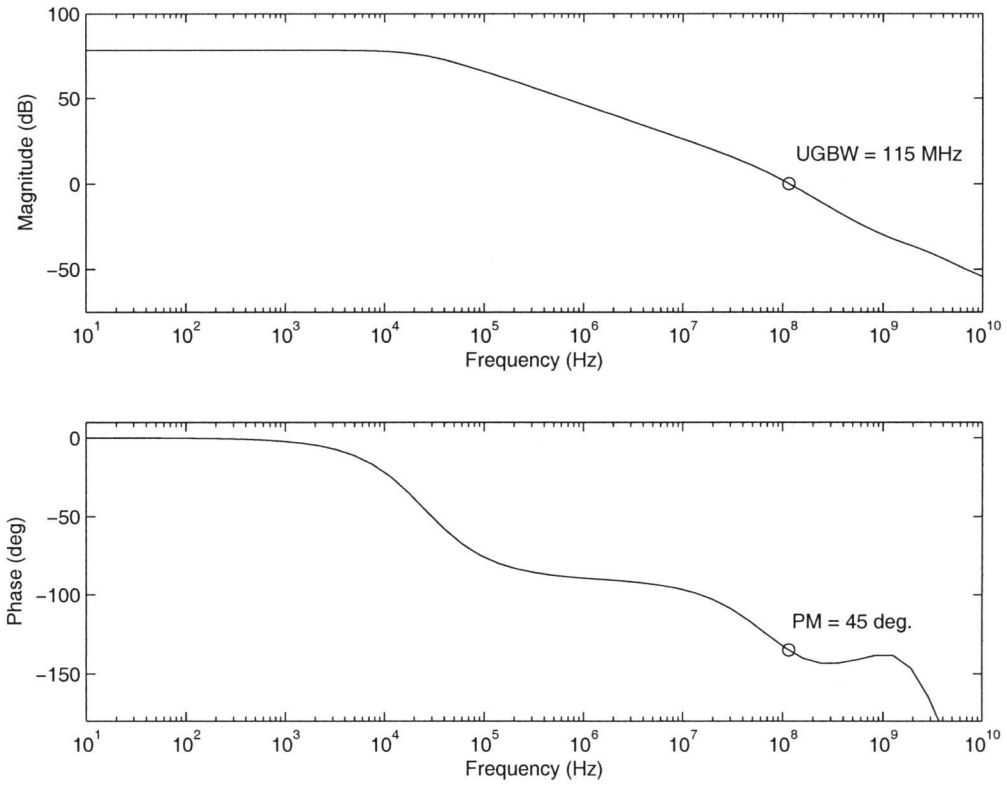



FIGURE 3.2. Simulated frequency response of the high swing two stage op-amp.

The simulated frequency response of the op-amp is shown in Figure 3.2. The DC gain of the op-amp is 78 dB and the unity gain bandwidth is 115 MHz. The op-amp has 45° of phase margin to ensure stable operation when configured in unity gain feedback. The unity gain bandwidth of the amplifier is high enough that the 10 MHz noise coupled to the amplifier will not be filtered before reaching the output.

### 3.2. Stepped Buffer Design

A stepped buffer is a very common block used in most digital designs to allow a weak signal to drive a large capacitive load. This is often needed in clock amplification or when driving a signal off chip.

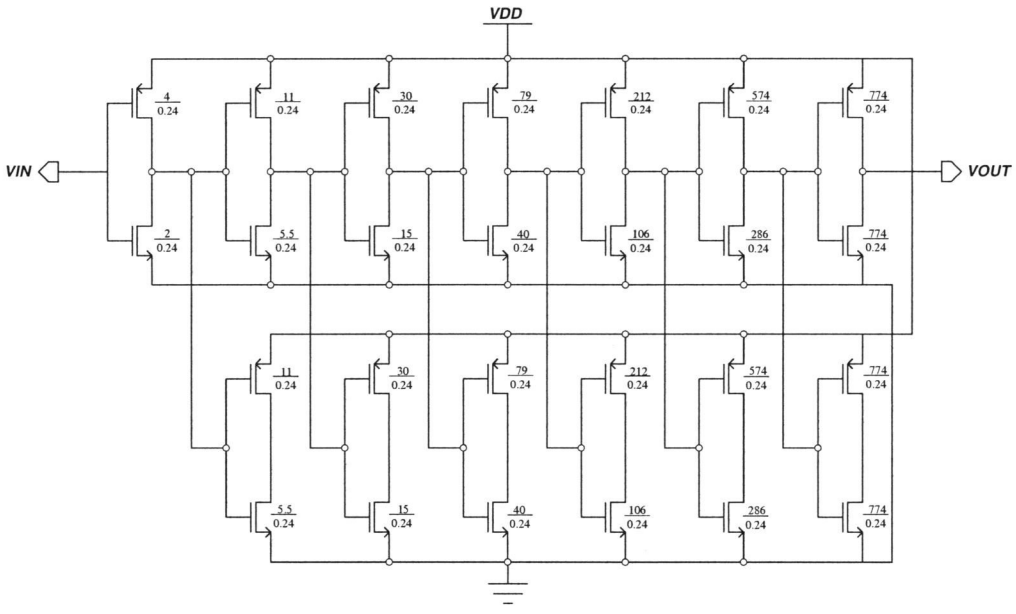



FIGURE 3.3. Digital stepped buffer with transistor sizes ($\frac{w}{l}$) shown in microns.

The stepped buffer is shown in Figure 3.3 [10]. The first stage is made up of a minimum sized inverter that is easily driven by any logic block in the standard logic cell library. Each consecutive inverter stage is a factor of $e$ larger than the previous until the final stage is large enough to drive the specific load. This factor of $e$ dictates the optimal number of buffer stages used when trying to maximize the speed of a buffer driving a given load [11].

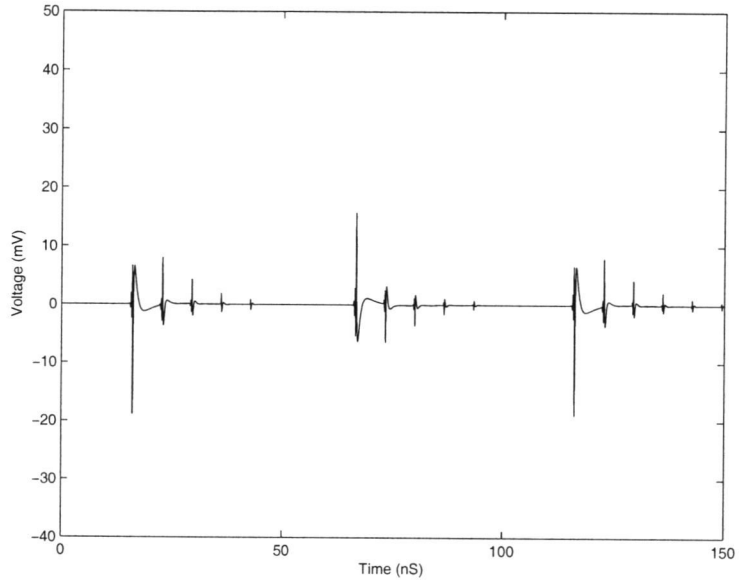
The inverter size ranges from $\frac{2\mu m}{0.24\mu m}$ to the final size which is $\frac{774.8\mu m}{0.24\mu m}$. Each stage also has an inverter that loads it which is sized the same as the next stage.

This forces the buffer to draw twice the amount of current as an unloaded buffer and thus inject approximately twice the amount of noise into the substrate.

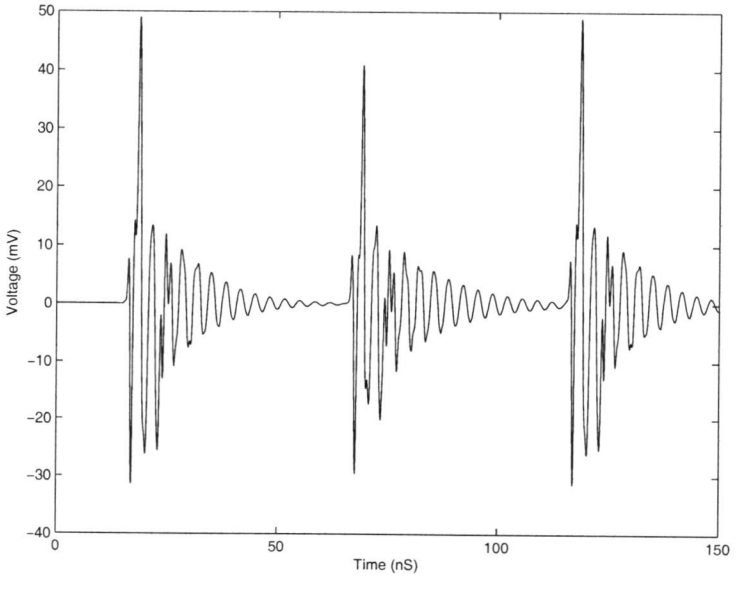
### 3.3. Minimizing Parasitics

When performing substrate noise measurements on ICs, off-chip parasitics must be reduced as much as possible. Bondwire, package, socket, and on board trace impedances can amplify or attenuate the signals making it difficult to obtain meaningful measurements. Figures 3.4 (a) and (b) compare a simulation of the stepped buffer running at 10 MHz and the op-amp in an ideal situation (with no parasitics) with the same op-amp where parasitics for a typical PGA package [15] have been applied. Typical values for the PGA pin model are shown in Figure 3.5.

By comparing (a) and (b) in Figure 3.4 it is obvious that adding pin parasitics to the simulation dramatically changes the output of the op-amp. The pin parasitics create an L-C tank circuit with a resonant frequency of about 220 MHz. This results in components at this frequency in the output that are amplified to a magnitude over twice the size of the signal seen when no parasitics are present. The L-C tank has an extremely small series resistance (19 m$\Omega$), creating a circuit with a high Q value. This high Q circuit produces the ringing seen in Figure 3.4 (b).




(a)




(b)

FIGURE 3.4. Simulated op-amp output (a) with no package parasitics and (b) with package parasitics added.

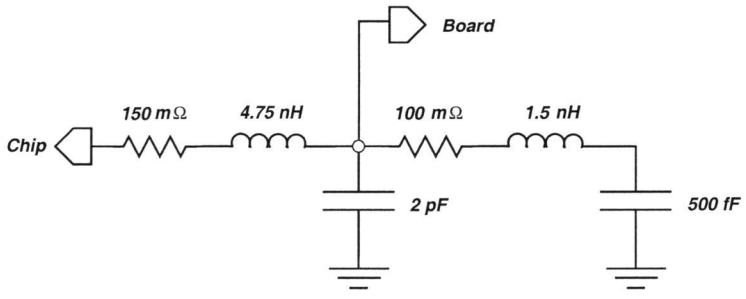



FIGURE 3.5. Pin model with typical values for the PGA 84 pin package.

Package parasitics, mainly pin inductance, can also be detrimental when grounding the backplane through the die perimeter ring in a heavily doped substrate. When inductance is introduced in the path between the die perimeter ring and ground, the grounding of the backplane is not perfect. A backplane that is grounded with a large inductance will present a high impedance to high frequency noise transients in the substrate. In this case, the high frequency noise will find a low impedance path to other contacts resulting in more noise coupling to transistors and other sensitive blocks.

Figure 3.6 shows the schematic used to simulate the effects of inductance introduced into the backplane connection. The two contacts (injector and sensor) sized as 1000 $\mu$m x 1000 $\mu$m for case 1 and 300 $\mu$m x 300 $\mu$m for case 2 are separated by a distance of 200 $\mu$m in the TSMC 0.25 $\mu$m heavily doped CMOS substrate. These contact sizes represent a large digital or analog circuit that would be found in a mixed-signal SoC. In Figure 3.6 the resistor values without parenthesis correspond to the 1000 $\mu$m x 1000 $\mu$m contacts and the values in parenthesis correspond to the 300 $\mu$m x 300 $\mu$m contacts. A noise source with a magnitude of 100 $mV_{p-p}$ is applied to the injector contact while the coupled noise

is measured on the sensor contact. Figure 3.7 shows the noise magnitude on the sensor contact as inductance in the backplane connection is increased.

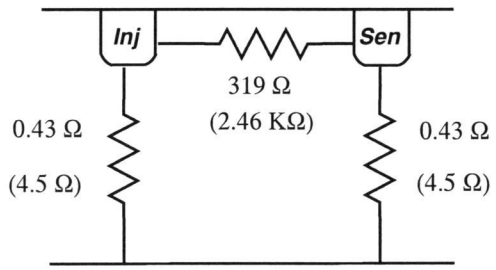



FIGURE 3.6. Substrate noise simulation between two contacts with inductance in the backplane.

The plots show that the amount of parasitic inductance that can be tolerated when grounding the backplane depends on the size of the contact. When the injector contact is 1 $mm^2$, less than 5 % of the injected noise is present on the sensor contact when 20 pH of inductance is present. When the contact size is only 0.09 $mm^2$, the amount of inductance can be as high as 300 pH for a similar value of the peak-to-peak noise. At a value of 300 pH, half of the noise in the 1 $mm^2$ case is seen at the sensor contact. With 300 pH of inductance in the backplane connection, the impedance through the backplane to ground is about j0.2Ω. This creates a voltage divider allowing half of the noise magnitude to be seen on the backplane and the sensor contact in the 1 $mm^2$ contact case.

In this work the parasitics previously described are minimized through the use of a chip-on-board (COB) design. In the COB design, a special footprint was designed on the printed circuit board (PCB) to allow the chip to be directly attached and bonded to the board eliminating the necessity of a package and a socket. Decoupling capacitors and the ground connection for the die perimeter ring are placed as close to the die as possible in order to further reduce any parasitics introduced by the PCB traces.

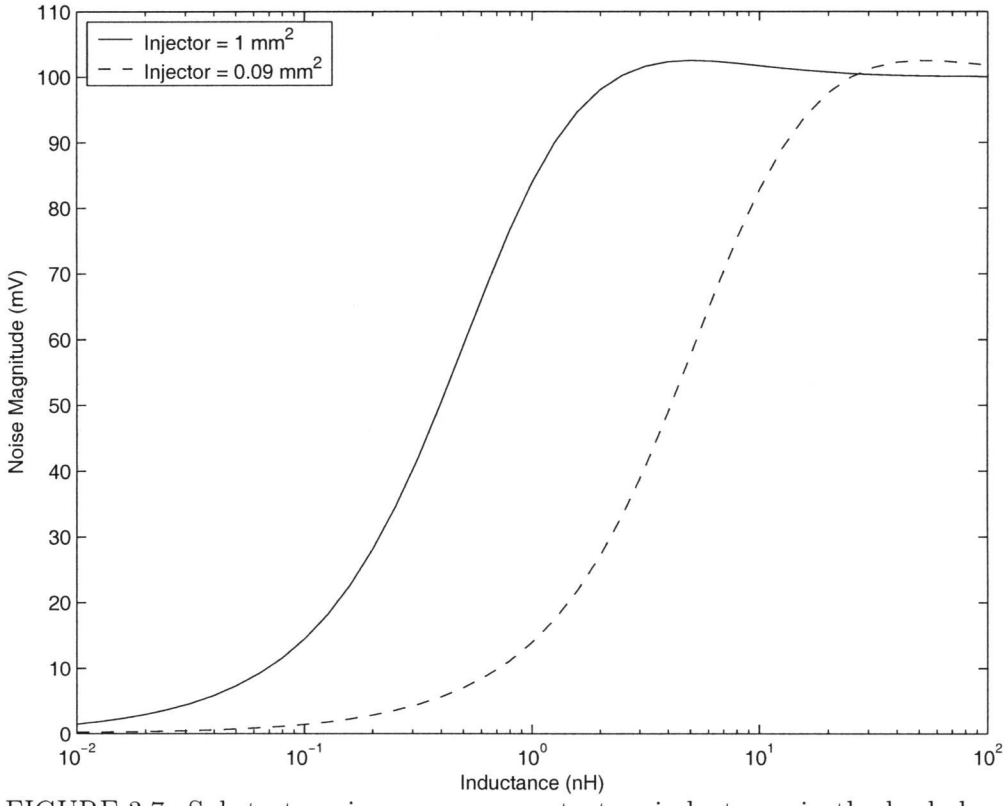



FIGURE 3.7. Substrate noise on sensor contact as inductance in the backplane is increased for 1 $mm^2$ injector and sensor contacts and 0.09 $mm^2$ injector and sensor contacts.

# 4. SIMULATION APPROACH

Post layout substrate noise coupling simulations can be both overwhelming and error prone when performed on circuits with more than just a few transistors. When using the substrate model described in Section 2.3, the number of resistors in the substrate network is $[n \times (n + 1)]/2$ where n is the number of contacts in the circuit. Manually adding the labels, substrate network, and parasitics is extremely inefficient and subject to many errors.

Silencer! [13] provides an easy method for substrate network generation and simulation. By working within the Cadence design tool, Silencer! links the circuit design and layout with the substrate noise coupling simulations through the use of an easy to use graphical interface.

## 4.1. Simulation Method

The simulation method for this work is shown in Figure 4.1. The process begins with the circuit design described in Chapter 3. Once the circuit design and layout are completed, the transistors in the layout are associated with those in the schematic by simply giving each of them a common label. The label is applied to the active region in the layout (areas diffused with n or p dopants) and to the bulk of the transistor in the schematic.

After the labeling is completed, the layout is used to extract the substrate ports that are used when calculating the overall network. Connectivity parasitics (resistance and inductance) of each of the transistor p-taps and the backplane connection are also specified to be included in the schematic for simulation. These parasitic resistances and inductances help to accurately add the effects of power supply noise in the final simulation.

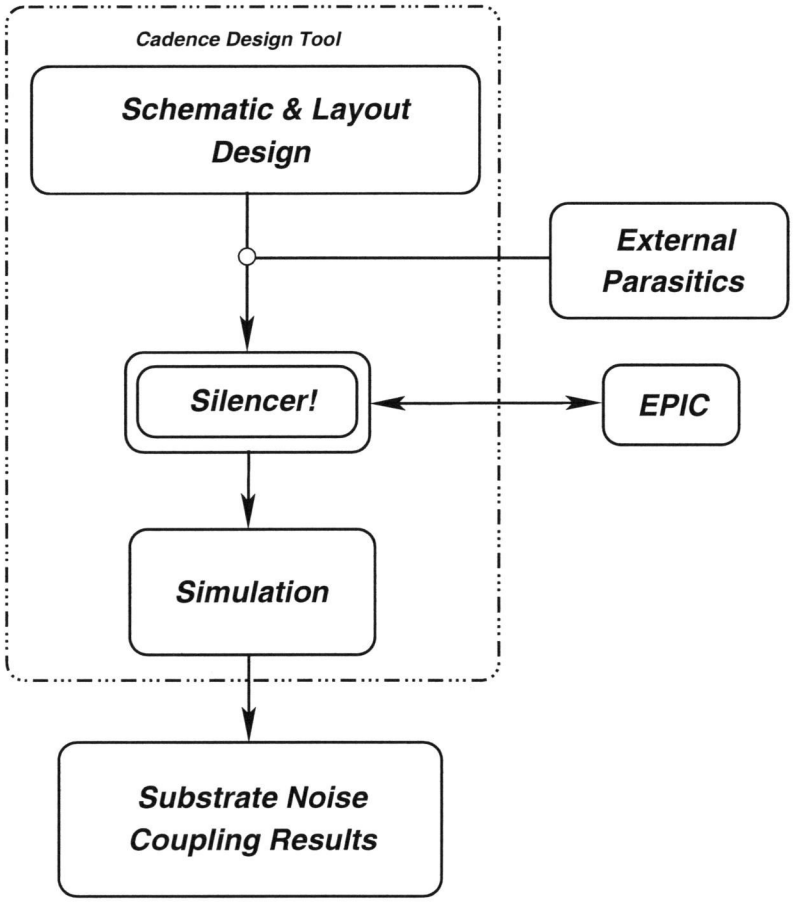



FIGURE 4.1. Flow chart outlining the substrate noise coupling simulations.

Silencer! then activates EPIC to create a netlist that is imported into the schematic for simulation. Figure 4.2 shows an example of a simplified schematic for simulation. The substrate network, backplane connectivity, and p-tap parasitics for each transistor have been added. The analysis is performed by simply running the schematic simulator and viewing the results at the node of interest.

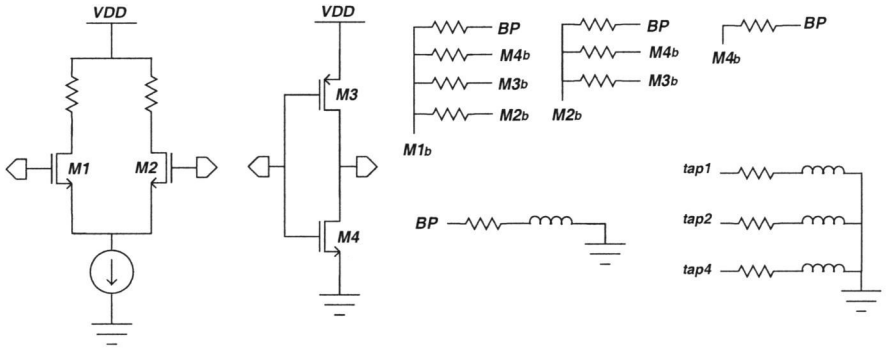



FIGURE 4.2. An example of a schematic after the substrate network and supply parasitics have been added.

## 4.2. External Parasitics

When comparing simulated and measured results, the simulation must take into account all the non-ideal elements present in the measurement setup. Some of these include PCB traces, transmission lines, impedance mismatches, and equipment parasitics. Any one of these elements can contribute to differences between simulation and measurement results.

An example of a simulation with these parasitics included is shown in Figure 4.3. The block labeled "op-amp" represents the schematic of Figure 3.1 and all the other components are included as a result of layout, packaging, board traces, and test equipment.

Each external connection to the circuit has a resistor and inductor to model the bondwire used for the connection. The parasitic resistance from the bondwire is calculated using:

$$R = \frac{\rho l}{A} \tag{4.1}$$

where $\rho$ is the resistivity of the bondwire material, $l$ is the length of the bondwire, and $A$ is the cross sectional area of the bondwire. The bondwire material used here is gold and the average dimensions are a length of about 1.5 mm and a diameter of 1 mil. Using these values along with (4.1), the resistance value used for an average bondwire is 65 m$\Omega$. The parasitic inductance of the bondwire is calculated using:

$$L \approx [\frac{\mu_o l}{2\pi}][ln(\frac{2l}{r}) - 0.75] \tag{4.2}$$

where $\mu_o$ is the permeability of free space and $r$ is the radius of the bondwire [14]. Using (4.2) with the values described above, an average bondwire inductance is found to be about 1.45 nH. Additional resistance was included for the input node due to a long and narrow routing trace used in layout. The value for this resistance was calculated by simply using 70 $m\Omega$/sq [15].

The power supply has three capacitors and an inductor to include the effects of the circuitry on the PCB. The three capacitors represent the decoupling capacitors used on the power supply and the inductor represents the long copper trace connecting the op-amp to the power supply. Three decoupling capacitors are used in the design with values of 10 $\mu$F, 2.2 $\mu$F and 100 nF. The inductance for the copper trace is found using:

$$L \approx \frac{\mu_o l h}{w} \tag{4.3}$$

where $\mu_o$ is the permeability of free space, $h$ is the thickness of the circuit board, $l$ is the length of the trace, and $w$ is the width of the trace [16]. With an average width of 15 mils and a length of 15 mm, the on-board inductance from the power trace is about 75 nH.

The output node has additional elements used to include the effects of the SMA cable and the oscilloscope. The additional resistor in series with the

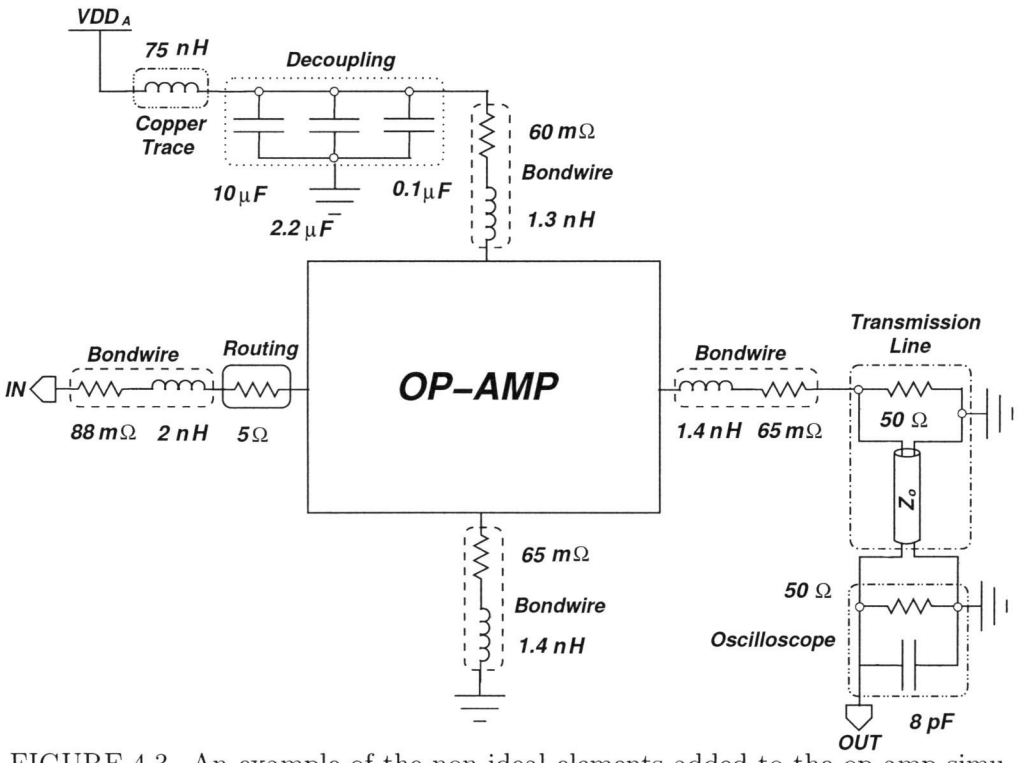



FIGURE 4.3. An example of the non-ideal elements added to the op-amp simulation for comparison with measurements.

bondwire models the impedance for the 50 Ω SMA connector located on the circuit board. The transmission line represents the cable that connects the circuit board to the oscilloscope and the resistor (50 Ω) and capacitor (10 pF) pair represent the termination at the oscilloscope.

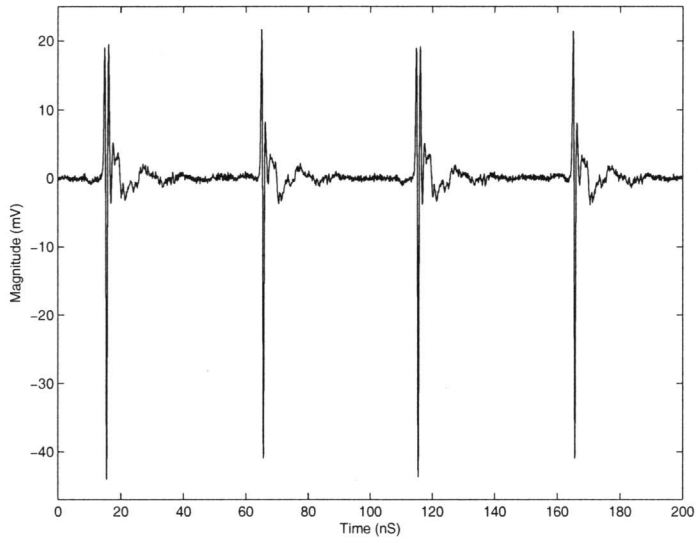
# 5. MEASUREMENT RESULTS AND COMPARISON TO SIMULATIONS

## 5.1. Measurement Results

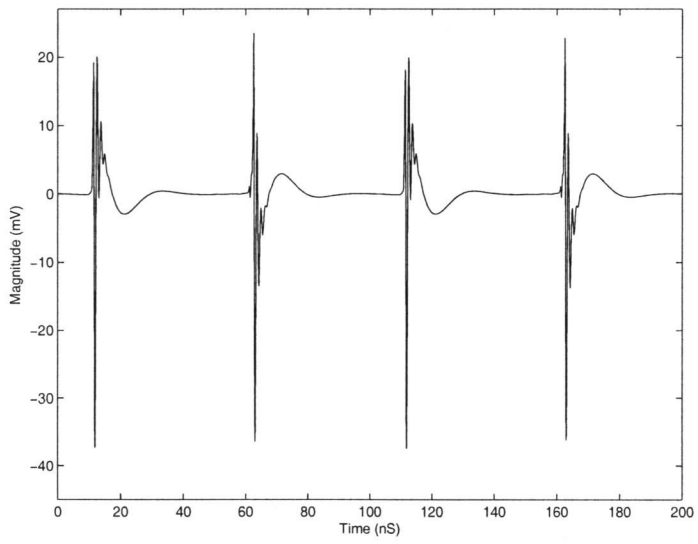
### 5.1.1. Heavily Doped Substrate

The measured and simulated results from the heavily doped substrate are shown in Figures 5.1 (a) and (b). The measurement is taken from the output of the op-amp connected in unity gain when a DC bias is applied to the input and the stepped buffer is running at 10 MHz. The magnitude of the the noise spikes are about 60 $mV_{p-p}$. A very small amount of ringing is present in the measurement due to the absence of a package and the use of small bondwires.

The measurement results with the die perimeter ring grounded are shown in Figure 5.2 (a) and the simulation performed with Silencer! is shown in Figure 5.2 (b). The results show an improvement of 15 $mV_{p-p}$ in the case that the die perimeter ring is grounded when compared to the case where it is left floating. This improvement is a result of noise being shunted away through the grounded backplane.

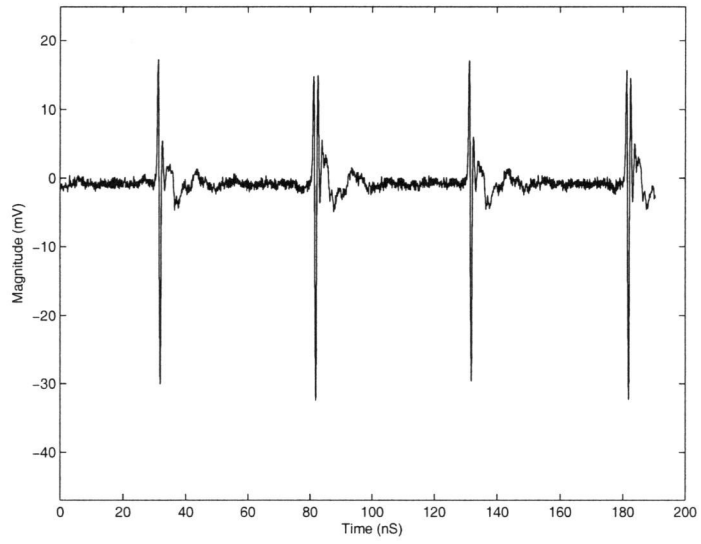



(a)

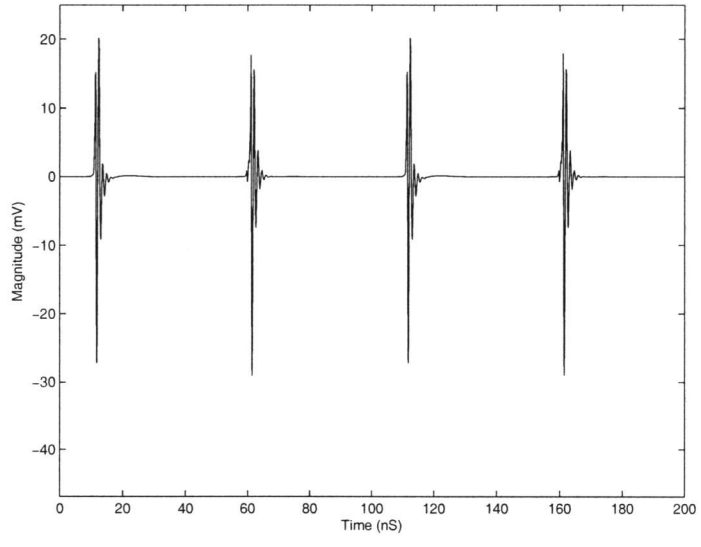



(b)

FIGURE 5.1. (a) Measurement and (b) simulation of the op-amp output in the heavily doped substrate with the stepped buffer running at 10 MHz.




(a)




(b)

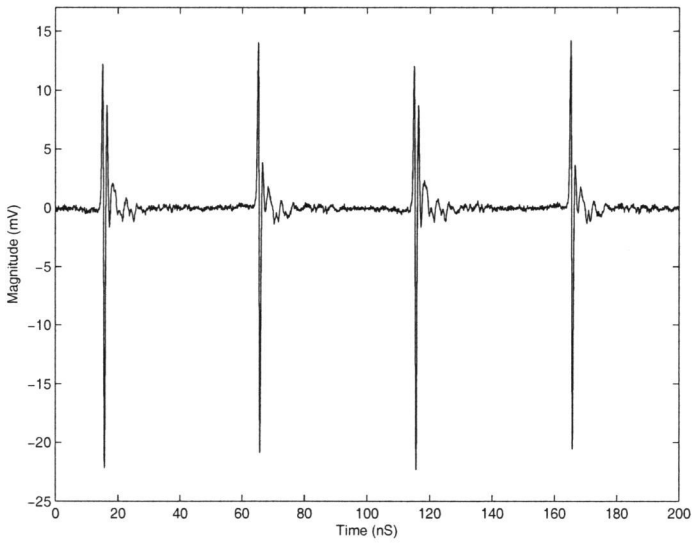
FIGURE 5.2. (a) Measurement and (b) simulation of the op-amp output in the heavily doped substrate with the stepped buffer running at 10 MHz while the die perimeter ring is grounded.

### 5.1.2. Lightly Doped Substrate

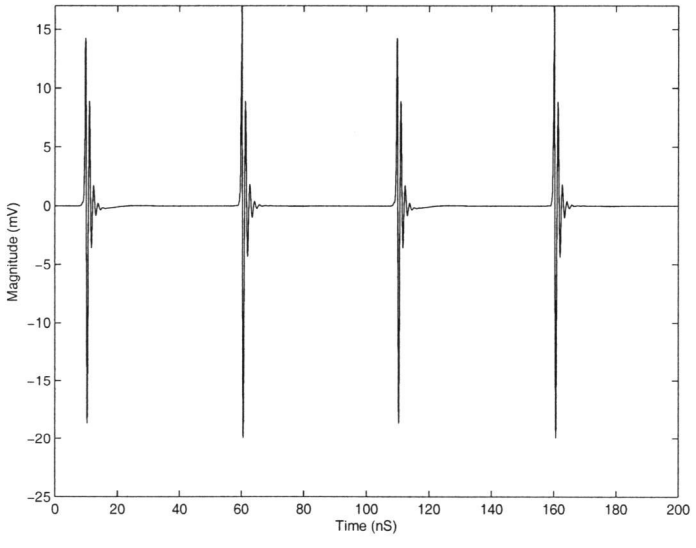
Figure 5.3 shows the measured and simulated results for the test chip fabricated in the lightly doped process. The noise spikes have a magnitude of about 35 $mV_{p-p}$. When compared to the heavily doped case an improvement of about 25 $mV_{p-p}$ is seen. This is due to the high resistivity of the bulk in the lightly doped process.

The high bulk resistance in the lightly doped substrate causes the majority of the noise currents to flow through the channel stop region at the top of the substrate. The coupling path through the channel stop region has a much higher resistivity than the path through the bulk in the heavily doped case. This highly resistive path provides more attenuation of the noise than the low resistivity path in the heavily doped case resulting in lower noise magnitudes.

No difference was seen in measurements when the die perimeter ring was grounded in the lightly doped substrate. This is because of the large amount of noise coupling due to mutual inductance between the bondwires as well as a high inductance in the die perimeter ring connection. Both of these issues are discusses in Section 5.2.1. In Chapter 6 it will be show that improvement can be achieved from grounding the backplane in lightly doped substrates.




(a)




(b)

FIGURE 5.3. (a) Measurement and (b) simulation of the op-amp output in the lightly doped substrate with the stepped buffer running at 10 MHz.

## 5.2. Comparison of Simulation and Measurements

### 5.2.1. Eliminating avoidable parasitics

In the heavily doped case, the die perimeter ring is shorted to ground through a very small trace. The trace extends from the bondwire to a jumper connecting to the ground plane on the daughter board. Even though this trace is very small, a parasitic inductance of 15 nH is present. This inductance blocks a large portion of the noise from shunting through the substrate to ground. This severely limits the effectiveness of the die perimeter ring.

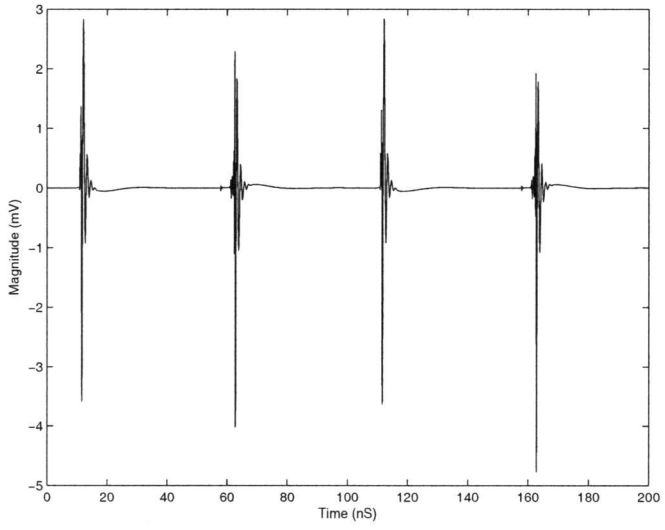



FIGURE 5.4. Simulation of the op-amp output in the heavily doped substrate with the die perimeter connected through a low impedance to ground.

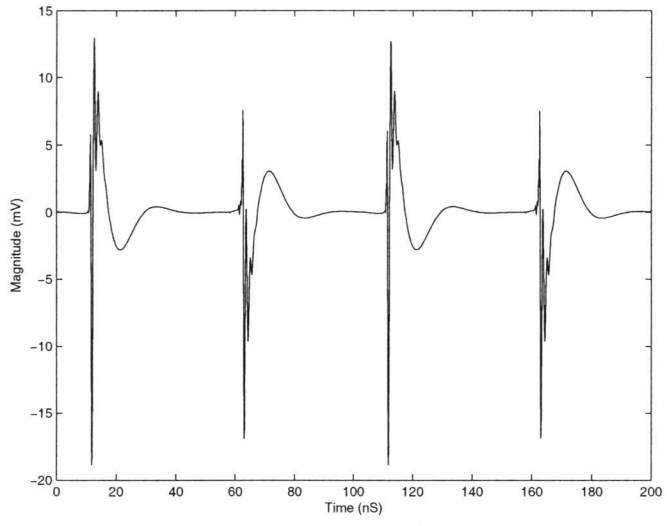
Figure 5.4 shows a simulation of the circuits in the heavily doped process with the die perimeter ring grounded through an interconnect that contains only 1.5 nH of inductance and 100 mΩ of resistance. This illustrates the case where the die perimeter ring is down bonded to the grounded die paddle using a bondwire.

The noise magnitude is reduced by an additional 15 $mV_{p-p}$ (compared to the cases seen in Figure 5.2) and proves to be a very effective method of reducing the substrate noise in heavily doped substrates.

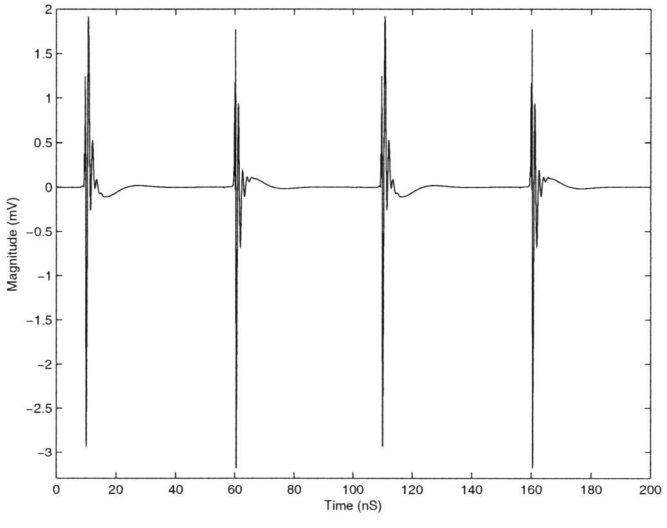
Another one of the parasitics found in measurements is the mutual inductance between the bondwires. In this design the bondwires for the inputs, outputs, and power supplies for the stepped buffer and op-amp are located in close proximity to one another providing a large path for noise coupling. Figure 5.5 shows simulations of the heavily and lightly doped substrates after the mutual inductances have been removed. This simulates the situation where the interconnects from the op-amp and stepped buffer are spaced at a distance large enough that mutual inductance effects are not important.

The simulations show a 30 $mV_{p-p}$ reduction of noise in both the lightly and heavily doped cases when compared to their respective measured cases. This brings the magnitude of the noise in the heavily doped substrate down to 30 m$V_{p-p}$ and the noise in the lightly doped substrate to 5 m$V_{p-p}$.

Figure 5.6 shows a simulation of the op-amp and stepped buffer in the heavily doped process with the mutual inductance excluded and the die perimeter ring grounded with 1.5 nH of inductance. The noise magnitude is reduced to just over 4 $mV_{p-p}$. This illustrates the combined result of no mutual inductance between the stepped buffer and op-amp bondwires and low impedance in the die perimeter ring connection. Under these conditions, the isolation seen in the heavily doped process is slightly better than that seen in the lightly doped process.




(a)




(b)

FIGURE 5.5. Simulation of the op-amp output in the (a) heavily doped and (b) lightly doped substrates with the mutual inductance excluded.

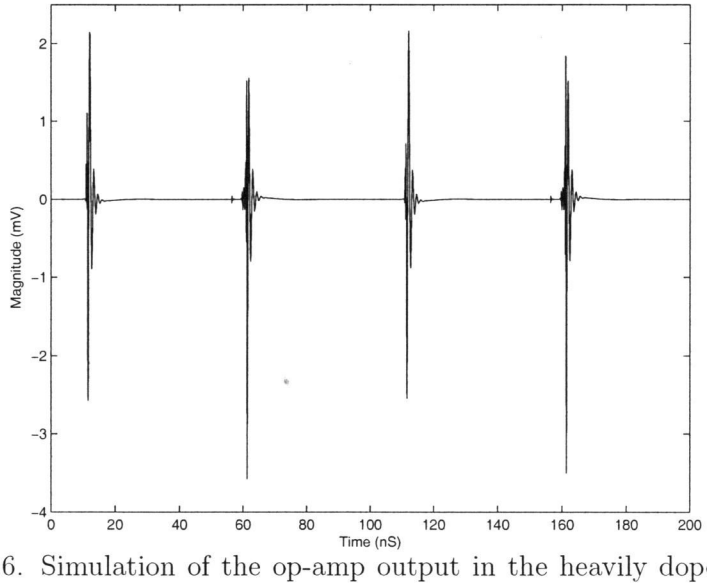



FIGURE 5.6. Simulation of the op-amp output in the heavily doped substrate with the die perimeter ring grounded through 1.5 nH and the mutual inductance excluded.

### 5.2.2. Guard Rings

Another easy and effective method to reduce substrate noise coupling is through the use of guard rings. A guard ring is a ring of p+ material that surrounds either a digital or analog block in mixed-signal designs. The ring is biased at ground potential to allow it to "absorb" as much noise as possible.

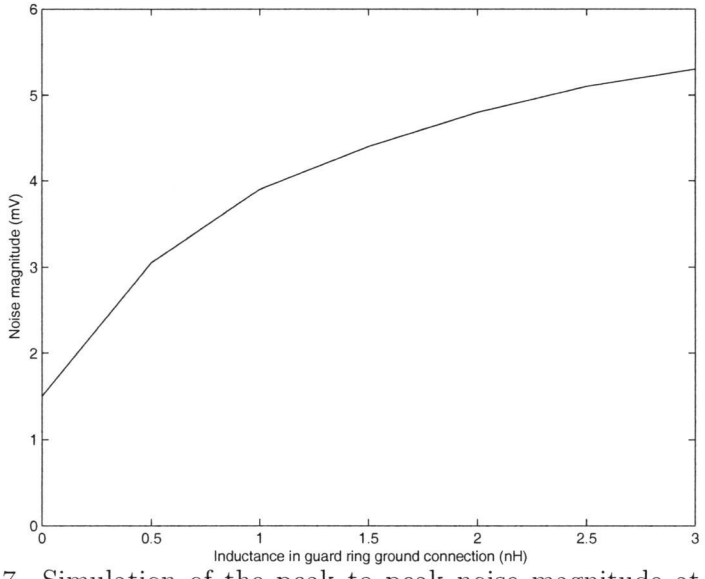


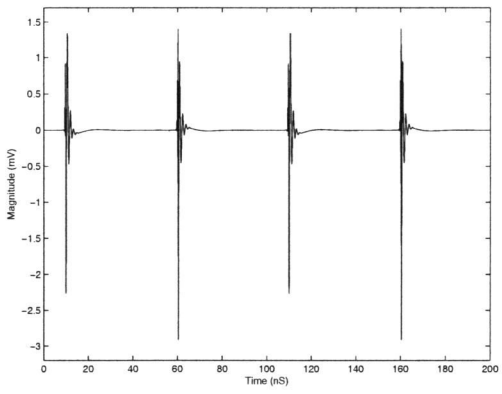

FIGURE 5.7. Simulation of the peak to peak noise magnitude at the op-amp output in the lightly doped substrate for a 2 $\mu$m guard ring around the op-amp. The inductance in the guard ring to ground connection is varied from 0 to 3 nH.

It is crucial that the guard ring ground connection has as little impedance as possible while also having a bondwire and pin that is separated from other noisy signals. A ground connection with a high impedance can generate voltage spikes when noise currents flow through it, making the noise coupling worse than a case with no guard rings. Figure 5.7 shows a simulation of the noise magnitude on the output of the op-amp when the inductance in the ground connection for a 2 $\mu$m guard ring around the op-amp is varied. For an inductance value above

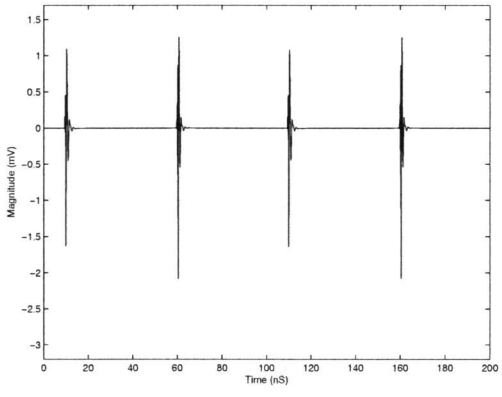
2 nH the noise coupling becomes worse than the case without guard rings. This illustrates the situation where a guard ring can actually worsen the noise coupling if the inductance in it's ground connection is too high.

The op-amp and stepped buffer have been simulated in the TSMC 0.25 $\mu$m lightly doped process with three different guard ring configurations. The first case consists of a guard ring placed around the op-amp, the second case has a guard ring placed around the stepped buffer, and the third case has a guard ring placed around both the op-amp and the stepped buffer. The guard rings are 2 $\mu$m wide and spaced 1 $\mu$m from the closest transistor. In the case with two guard rings, the spacing is 28 $\mu$m between the rings. Each ring is connected to ground through a 100 m$\Omega$ resistor and a 1.5 nH inductor to represent a bondwire connected to the grounded die paddle.

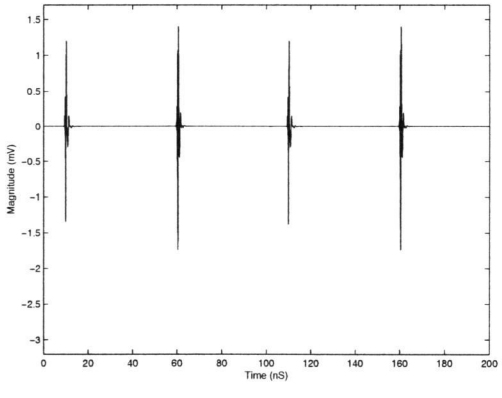
Figure 5.8 shows the simulated results for the cases with the guard ring around the op-amp, the guard ring around the stepped buffer, and guard rings around both the op-amp and stepped buffer. When comparing Figures 5.8 (a) and 5.5 (the case with no guard rings) a 10% improvement is seen. When the guard ring is placed around the stepped buffer rather than the op-amp, the improvement over the case with no guard rings is approximately 30%. Placing guard rings around both the op-amp and stepped buffer offers an improvement of 35%.




(a)




(b)

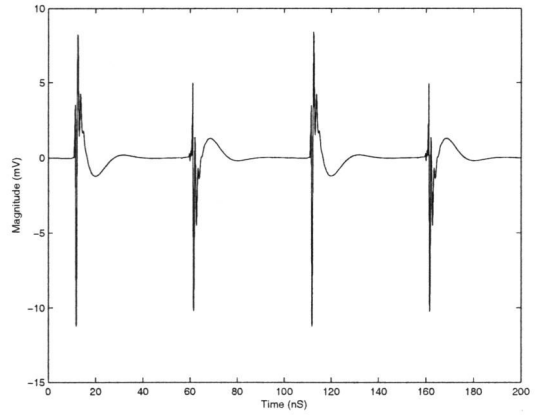



(c)

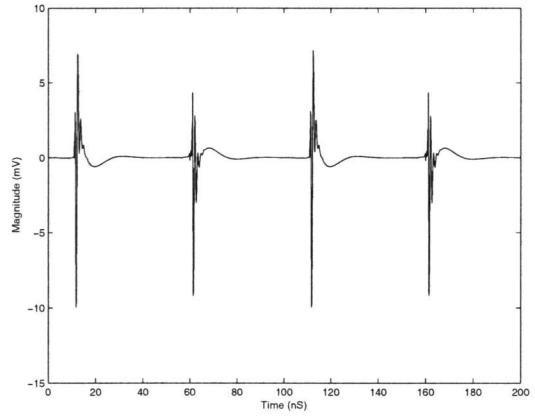
FIGURE 5.8. Simulation of the op-amp and stepped buffer in the lightly doped substrate with a 2 $\mu$m guard ring around the (a) op-amp, (b) stepped buffer, and (c) both the op-amp and the stepped buffer.

In the case where a single guard ring is placed around the op-amp, noise from the buffer continues to couple to all the pads and op-amp inputs and outputs. Though the transistors in the op-amp are shielded, the traces connecting its power, ground, current bias, and input signal are still largely affected by the digital noise. This provides a direct path for the noise to the op-amp. When the guard ring is placed around the buffer a large portion of the digital noise is removed before it reaches other components. Thus, the case with the guard ring around the buffer provides better shielding than the case with the ring around the op-amp. In the case with both guard rings, the noise from the stepped buffer sees the two guard rings in parallel, creating the lowest impedance path to ground of the three cases. This results in the lowest noise magnitude is seen on the output of the op-amp.

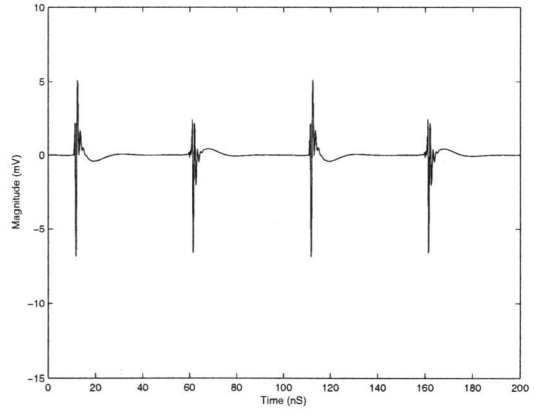
Simulation results from the same setup described above are shown in Figure 5.9 for the heavily doped process . When compared to the simulation of the heavily doped substrate without mutual inductance (Figure 5.5), a large noise reduction is observed. The case with a guard ring around the op-amp offers a 33 % improvement, the case with a guard ring around the stepped buffer offers a 43 % improvement, and the case with guard rings around both the stepped buffer and op-amp offers a 60 % improvement.




(a)




(b)




(c)

FIGURE 5.9. Simulation of the op-amp and stepped buffer in the heavily doped substrate with a 2 $\mu$m guard ring around the (a) op-amp, (b) stepped buffer, and (c) both the op-amp and the stepped buffer.

In the heavily doped process the main noise coupling path is through the low resistivity substrate. Typical $R_{11}$ values for transistors located in the op-amp range from 2 KΩ to 3.5 KΩ. The $R_{11}$ values for the stepped buffer and op-amp guard rings are 90 Ω and 113 Ω, respectively. Thus, noise currents at the backplane will flow through the low resistance paths through the guard rings to ground rather than coupling to the contacts in the op-amp. When both of the guard rings are present, their low impedance paths to ground are seen in parallel resulting in an even greater noise reduction when compared to the single guard ring cases.

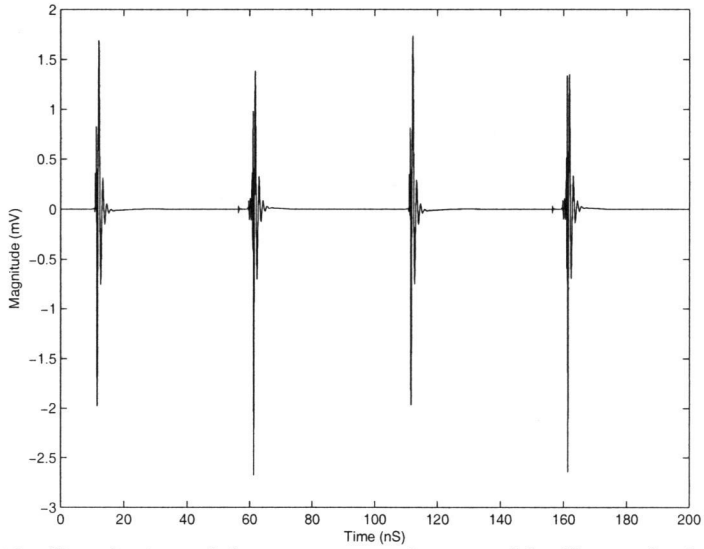



FIGURE 5.10. Simulation of the op-amp and stepped buffer in the heavily doped process with a 2 $\mu$m guard ring around both the op-amp and stepped buffer and the backplane grounded with a 1.5 nH inductor.

When both guard rings are present and the backplane is grounded, shown in Figure 5.10, the noise reduction is not as dramatic. Compared with the case of no guard rings present (Figure 5.6), only a 25 % improvement is observed. This is because the path to ground through the backplane has a much lower impedance

than the paths through the guard rings. Therefore the majority of the noise current flows through the backplane and only a small amount of current flows through the guard rings resulting in only a slight reduction.

The width of the guard ring also plays an important role in the amount of noise reduction seen at the output. Figure 5.11 shows the noise magnitude seen at the output of the op-amp when the width of the guard ring is varied from 2 $\mu$m to to 8 $\mu$m in the heavily doped substrate with the backplane floating.

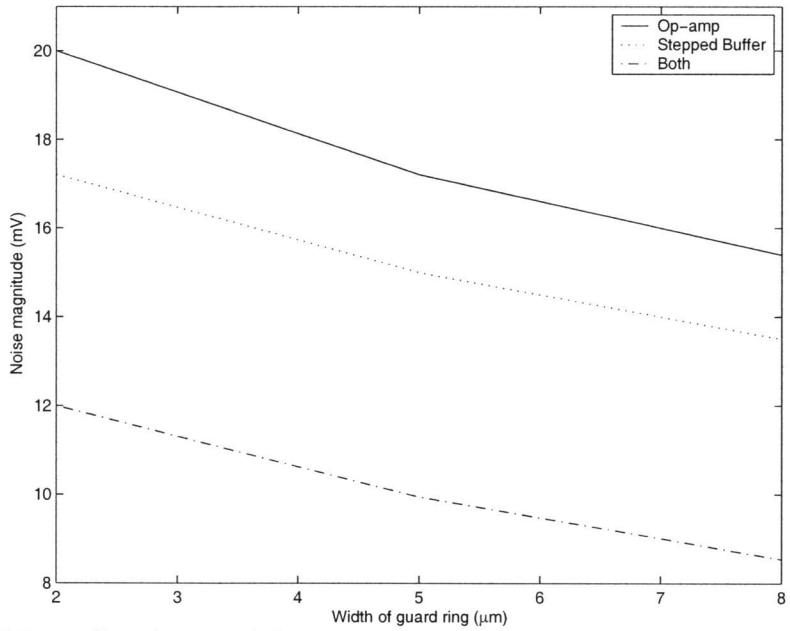



FIGURE 5.11. Simulation of the op-amp output noise magnitude when the guard rings widths around the op-amp and stepped buffer are varied in the heavily doped substrate.

The noise magnitude decreases as the width increases in all three cases. As the contact area is increased, the $R_{11}$ value of the contact decreases [17]. By increasing the guard ring width, the area is also increased which results in lower $R_{11}$ values. These lower values of $R_{11}$ provide lower impedance paths to ground

through the guard rings resulting in a reduction of the substrate noise seen at the op-amp.

The $R_{11}$ values for the op-amp guard ring range from 113 $\Omega$ when the width is 2 $\mu$m to 63 $\Omega$ when the width is 8 $\mu$m. The $R_{11}$ values for the stepped buffer guard ring are 90 $\Omega$ and 53$\Omega$, respectively. The difference in the $R_{11}$ values between the op-amp guard ring and the stepped buffer guard ring is due to the size of the guard rings. The stepped buffer guard ring is about 1.2 times as large as the op-amp guard ring. This accounts for the lower noise magnitude in the case with the stepped buffer guard ring compared to the case with the op-amp guard ring. When both guard rings are present, the two $R_{11}$ values are seen in parallel resulting in the best noise performance.

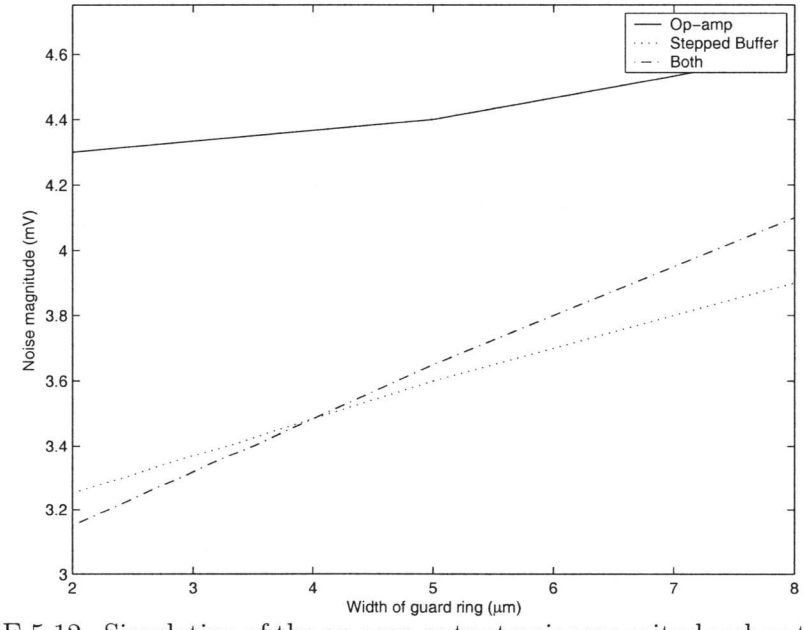



FIGURE 5.12. Simulation of the op-amp output noise magnitude when the guard rings widths around the op-amp and stepped buffer are varied in the lightly doped substrate.

Figure 5.12 shows the same simulation in the lightly doped substrate. Here most of the noise current flows through the p+ channel stop layer on the surface of the substrate which is represented by the $R_{12}$ resistor in the substrate model. In addition to contact size, $R_{12}$ also depends on the distance between contacts.

Consider the case with a guard ring around the op-amp. The distance between the guard ring and the transistors in the op-amp stays constant for all three widths. This results in the $R_{12}$ value between the guard ring and the op-amp transistors to have little change. When the op-amp guard ring width is increased the distance between the transistors in the stepped buffer and the op-amp guard ring decreases. This decrease in distance causes the $R_{12}$ values to decrease from 254 $\Omega$ to 182 $\Omega$. This decrease in $R_{12}$ causes the increase in noise coupling shown in Figure 5.12. The same argument applies for the case with the guard ring around the stepped buffer.

In the case with guard rings around both the op-amp and the stepped buffer, this decrease in the $R_{12}$ values is much larger than in the single guard ring cases. As the width of the guard rings is increased, the distance between them is decreased twice as much as in the case with a single guard ring. Therefore the $R_{12}$ value between the guard rings decreases dramatically (from 988 $\Omega$ to 351 $\Omega$) resulting in the large increase in the noise magnitude shown in Figure 5.12 [18].

A summary of the simulation results for the guard rings in the heavily and lightly doped processes is shown in Tables 5.1 and 5.2. The tables show simulations of the guard rings connected to ground through a 1.5 nH inductance, a 0 nH inductance, and a 0 nH inductance when the die perimeter rings is grounded through a 1.5 nH inductance. Results from each situation are shown when there is no guard ring, a guard ring around the op-amp, a guard ring around the stepped buffer, and guard rings around both the op-amp and stepped buffer.

TABLE 5.1. Summary of simulation results for guard rings in the heavily doped process.

| | **1.5 nH** | **0 nH** | **0 nH/BPG** |
|---|---|---|---|
| **No GR** | 30 mV$mV_{p-p}$ | 30 mV$mV_{p-p}$ | 4.5 mV$mV_{p-p}$ |
| **Op GR** | 20 $mV_{p-p}$ | 19.5 $mV_{p-p}$ | 4.5 $mV_{p-p}$ |
| **SB GR** | 17 $mV_{p-p}$ | 16.5 $mV_{p-p}$ | 4.5 $mV_{p-p}$ |
| **Both GR** | 12 $mV_{p-p}$ | 11.5 $mV_{p-p}$ | 4 $mV_{p-p}$ |

TABLE 5.2. Summary of simulation results for guard rings in the lightly doped process.

| | **1.5 nH** | **0 nH** | **0 nH/BPG** |
|---|---|---|---|
| **No GR** | 5 $mV_{p-p}$ | 5 $mV_{p-p}$ | 3 $mV_{p-p}$ |
| **Op GR** | 4.5 $mV_{p-p}$ | 1.5 $mV_{p-p}$ | 1 $mV_{p-p}$ |
| **SB GR** | 3.5 $mV_{p-p}$ | 0.9 $mV_{p-p}$ | 0.65 $mV_{p-p}$ |
| **Both GR** | 3.25 $mV_{p-p}$ | 0.7 $mV_{p-p}$ | 0.4 $mV_{p-p}$ |

In the heavily doped process, grounding the die perimeter rings provides a much larger improvement than making the guard ring connections ideal. This is because in the heavily doped substrate most of the noise current flows through the backplane. When the die perimeter ring is grounded the impedance to ground from the backplane reduces to less than 1 $\Omega$. The reduction in impedance seen at the backplane when the inductance is excluded from the guard rings is small. This is because the impedance caused by the inductance in the guard ring connection is much lower than the $R_{11}$ value of the guard ring.

In the lightly doped substrate the greatest improvement is seen when the inductance is removed from the guard rings. This is because in the lightly doped substrate most of the noise flows through the channel stop layer. When guard rings are present, most of the substrate noise injected into the op-amp is from ground bounce on the guard rings. When the inductance in the ground connection to the guard rings is excluded, the ground bounce is eliminated. Grounding the backplane provides additional improvement by shunting away most of the noise that flows through the substrate bulk.

Figures 5.13 and 5.14 show a summary of the noise coupling results for the guard ring simulations in the heavily and lightly doped substrates, respectively.

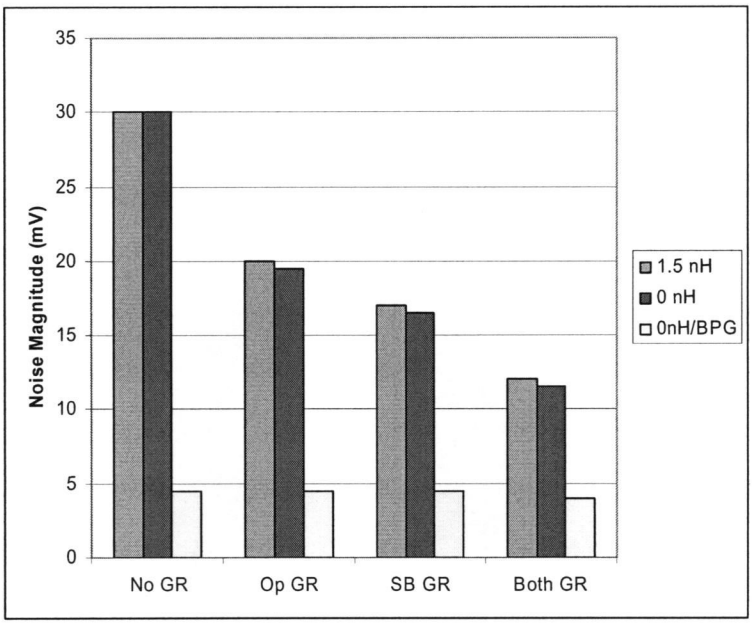



FIGURE 5.13. Summary of the noise coupling results for the guard ring simulations in the heavily doped substrate.

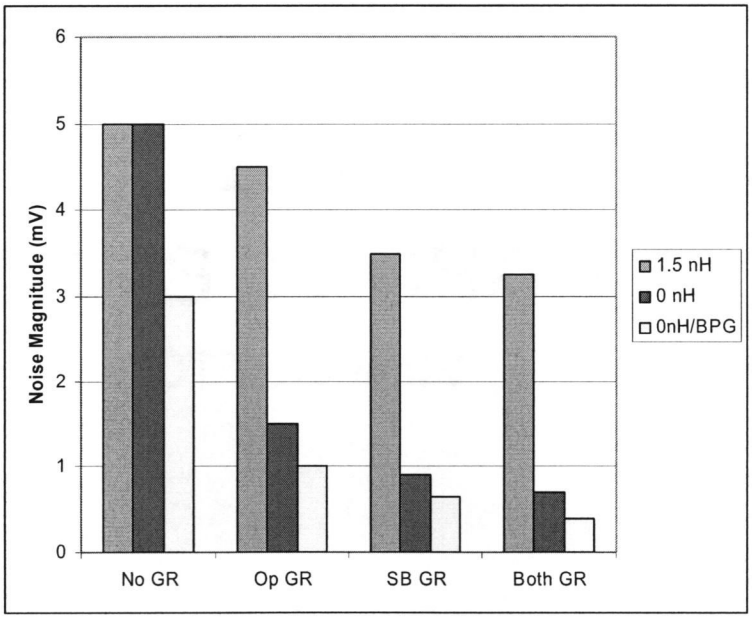



FIGURE 5.14. Summary of the noise coupling results for the guard ring simulations in the lightly doped substrate.

### 5.2.3. Op-amp Design Changes to improve noise performance

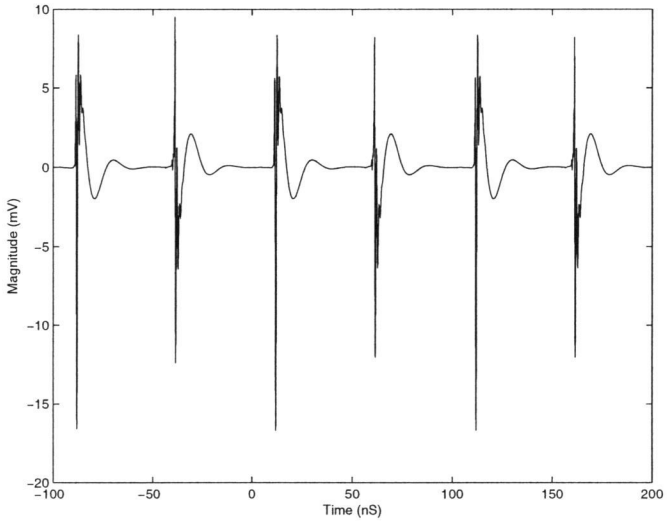
In addition to grounding the backplane of the substrate or adding isolation structures to the layout, schematic level design changes can be made to reduce substrate coupling. Methods such as using PMOS transistors when available or reducing the size of large transistors can provide additional noise reduction.

The two stage op-amp used in this work, shown in Figure 3.1, has a DC gain of over 75 dB. A large portion of this gain comes from the second stage of the amplifier. In the first stage of the amplifier, noise that is coupled to the transistors is seen as a common mode signal and a large portion of it is rejected when the two signals are summed together.

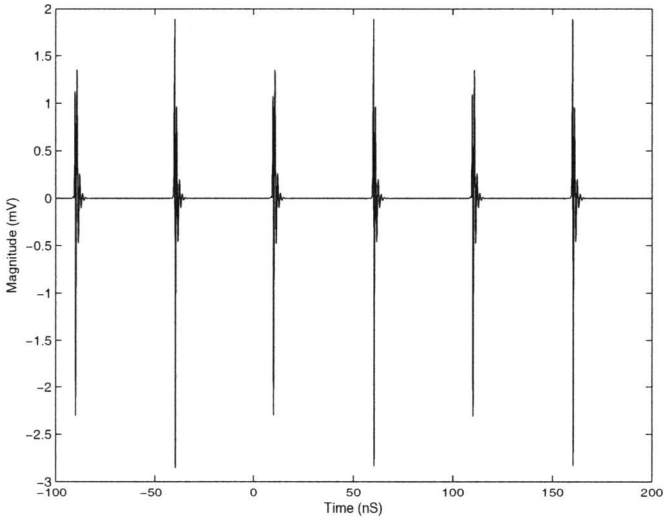
The second stage of the amplifier is single ended, resulting in the noise coupled to the bulk being amplified by the bulk transconductance of the transistor. The bulk transconductance ($g_{mb}$) is given by the equation:

$$g_{mb} = \frac{g_m \gamma}{2\sqrt{V_{SB} + 2\Phi_f}} \tag{5.1}$$

where $\gamma$ is body-effect constant, $g_m$ is the transconductance of the transistor, $V_{SB}$ is the source to bulk voltage, and $\Phi_F$ is the difference between Fermi level in the bulk and the Fermi level of intrinsic silicon [9]. The only two variables available to the designer are the transconductance of the transistor or the source to bulk voltage. Increasing the source to bulk voltage of the transistor is not an option because the source of the transistor is already biased at the lowest potential available (ground). Thus, the only available way to effectively decrease the value for $g_{mb}$ is to decrease the value of $g_m$. In addition to lowering the $g_{mb}$ of the transistor, lowering the $g_m$ will also lower the amount of noise that is amplified from the input of the second stage.




(a)




(b)

FIGURE 5.15. Op-amp output in the (a) heavily doped and (b) lightly doped processes when the gain of the second stage has been reduced.

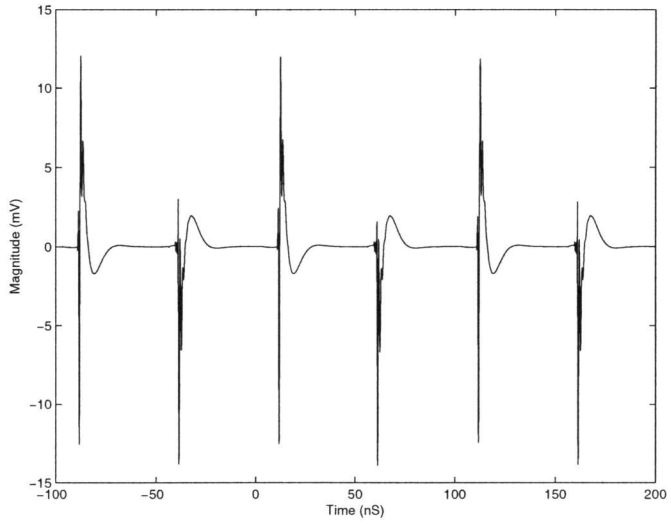
Figure 5.15 shows the output of the op-amp when the gain of the second stage of the op-amp has been decreased. The size of the transistor (M13 in

Figure 3.1) has been reduced by a factor of two which reduces the $g_m$ value of the transistor by 30 %.

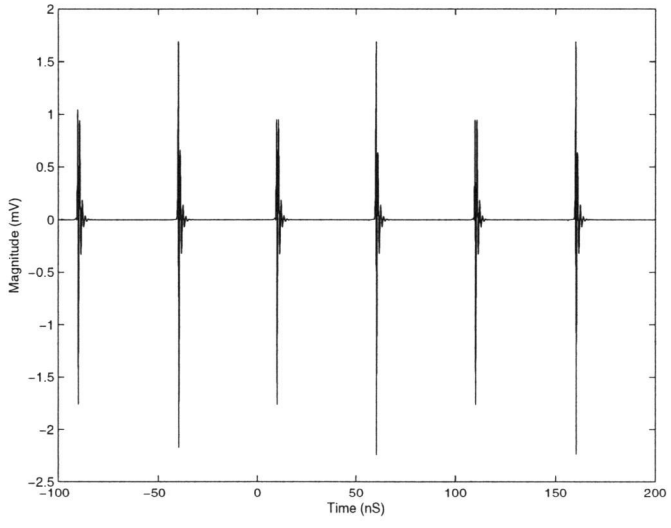
The noise magnitude in the heavily doped process reduced by over 30 % where the noise in the lightly doped process reduced by less than 5 %. This difference in reduction is due to the noise magnitude at the bulk of the transistor. In the heavily doped process the noise at the bulk of the second gain stage transistor has a magnitude of about 180 $mV_{p-p}$ whereas in the lightly doped process the noise magnitude is only about 10 $mV_{p-p}$. This large difference is mainly due to the layout of the op-amp. The majority of the noise in the heavily doped process flows through the low resistivity bulk and is distributed to each transistor through the $R_{11}$ resistors which are dependent on transistor size. In the lightly doped process, the noise flows through the channel stop layer and is distributed based on the $R_{12}$ values which are mainly dependent on spacing. In the op-amp layout the transistor for the second gain stage is much smaller than the output buffer transistors and is located farther away from the stepped buffer than the output buffers. As a result, the noise magnitude seen on the bulk of the second gain stage in the heavily doped case is much larger than in the lightly doped case. (The majority of the noise in the lightly doped case flows to the output buffers.) Therefore the noise reduction from the reduction of the $g_m$ in the heavily doped process is much more drastic that in the lightly doped process.

Another major source of noise coupling into the op-amp is through the output buffer stage. This is made of two NMOS transistors that are size at $\frac{600\mu m}{0.5\mu m}$. This large value was used for two reasons. The first is so the the buffer could drive low impedances. The second reason is to minimize the drain to source voltage drop in order to maximize the output voltage swing. As a result of these transistors

being so large, the amount of noise coupled to them is much higher than the other transistors in the circuit.




(a)




(b)

FIGURE 5.16. Op-amp output in the (a) heavily doped and (b) lightly doped processes when the size of the output buffer has been decreased by two.

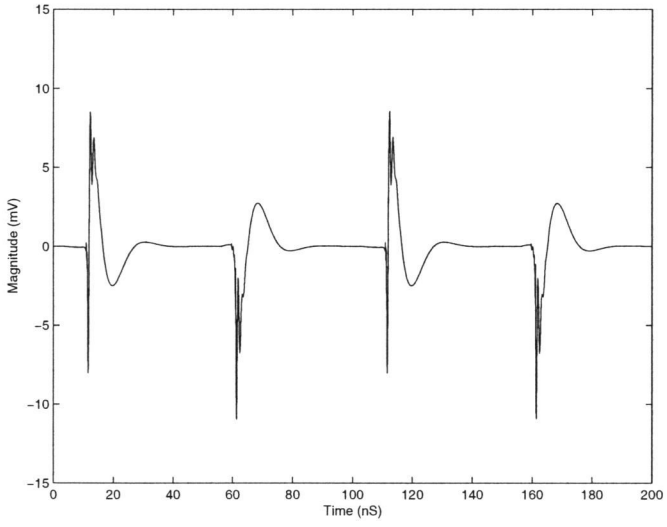
Figure 5.16 shows a simulation of the output of the op-amp in the heavily doped and lightly doped processes when the size of the output buffers have been decreased by a factor of two. A 20 % improvement is seen in the heavily doped

case and a 23 % improvement is seen in the lightly doped case. This implies that a large portion of the coupling in both substrates is from the output buffer and reducing the size of the buffer offers a significant improvement.

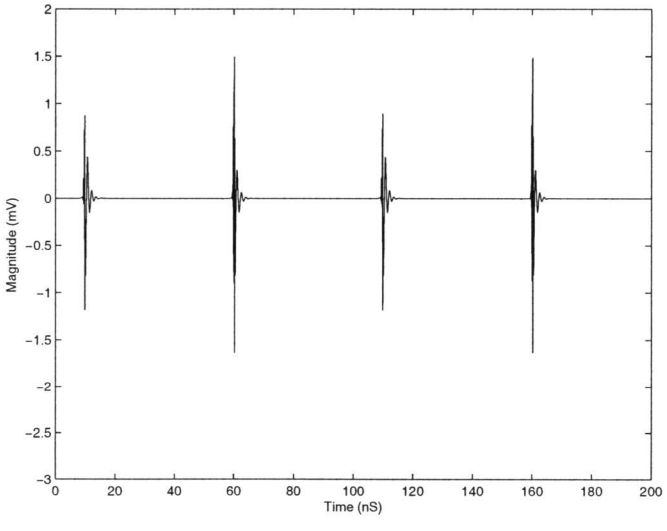
If the coupling to the output buffer could be completely eliminated, the noise magnitude on the output of the op-amp could be further reduced. This can be realized by using PMOS buffers instead of NMOS buffers. As a result of the PMOS transistors being located in an N-well, virtually all of the coupling would be eliminated. Figure 5.17 shows the output of the op-amp when the coupling to the output buffer has been completely removed. This provides a large improvement in both the heavily doped and lightly doped cases. The heavily doped case shows about 45 % improvement and the lightly doped case shows about 40 % improvement. This case shows a larger improvement than the previous circuit design change cases because the majority of the coupling to the op-amp is through the output buffer (because of their physical placement in the layout).

It should be noted that all of the design changes to improve the substrate coupling performance are trade-offs for other design parameters. When reducing the $g_m$ value of the second amplifier stage in the op-amp, the amplifier gain and bandwidth also reduce (30 dB and 20 MHz in this case). By reducing the size of the output buffer, the output swing as well as the load driving capabilities reduce. If the output buffer is replaced by PMOS transistors, the structure of the op-amp will need to be changed. The second stage amplifier will need to be changed to PMOS in order to attain the correct DC operation point for the PMOS output buffers. Changing the second gain stage to PMOS will result in a restructuring of the first stage.

Figure 5.18 shows a summary of the simulation results for the design changes in the heavily and lightly doped processes.




(a)




(b)

FIGURE 5.17. Op-amp output in the (a) heavily doped and (b) lightly doped processes when coupling is eliminated from the output buffer.

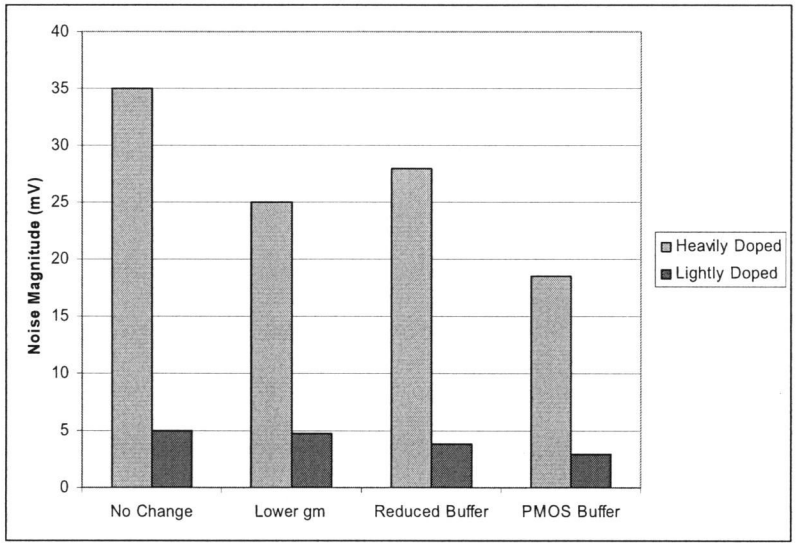



FIGURE 5.18. Summary of the simulation results for the design changes in the heavily and lightly doped substrates.

### 5.2.4. Summary of Results

Various techniques to reduce substrate noise coupling in mixed-signal circuits have been shown. Careful floor planning in the layout stage of a mixed-signal design can lead to a large reduction in noise by avoiding mutual inductance between noisy digital signals and sensitive analog signals. In the heavily doped substrate measurements showed a 25 % reduction in substrate noise magnitude when the backplane was grounded. Measurements taken from the lightly doped substrate showed a reduction of almost 50 % in noise magnitude when compared to the heavily doped substrate. With no mutual inductance between the digital and analog circuits and a low impedance connection to the backplane, a heavily doped substrate can offer an 85 % reduction in substrate noise magnitude. When mutual inductance is excluded from the lightly doped case an improvement of over 80 % is shown when compared to the heavily doped substrate.

It has also been shown that the number of guard rings as well as the width of the guard rings used greatly affect the noise coupling in mixed-signal circuits. In heavily doped substrates, where the majority of the noise current flows through the low resistivity bulk of the substrate, multiple guard rings offer a definite advantage over a single guard ring. As the width of the guard ring was increased to 8 $\mu$m, a noise coupling reduction of over 70 % was shown. Although it has also been shown that guard rings offer little improvement when the backplane is grounded, they do provide a good alternative for substrate noise reduction when providing a low impedance ground connection to the backplane is not available.

In lightly doped substrates guard rings can also be advantageous in reducing substrate noise coupling. Multiple guard rings show an improvement of only about 5 % over a single guard ring and 25 % over the case with no guard

rings. This is largely due to the fact that multiple guard rings can provide a lower impedance coupling path that single guard rings. As the widths of the guard rings increase the coupling between the analog and digital circuitry increases. Therefore when using guard rings in lightly doped substrates the minimum width should be used.

We have seen that modifying the op-amp design can also reduce substrate noise coupling. By reducing the gain, the noise amplification can be reduced by as much as 30 % in the heavily doped process. It should be noted that this reduction in gain is largely dependent on layout and should not be used as a general guideline for reducing substrate noise coupling. Reducing the size of large transistors was also very beneficial in reducing the amount of substrate coupling by reducing the noise magnitudes by 20 % in the heavily doped case and 23 % in the lightly doped case. If PMOS transistors can be used rather than NMOS transistors, coupling is effectively eliminated which greatly increases performance. By replacing the largest NMOS transistors in the circuit with PMOS transistors, the coupling could be reduced by over 45 % and 40 % in the heavily doped and lightly doped processes, respectively.

# 6. GENERALIZATION OF RESULTS

The circuits analyzed in Chapter 5 are hard to generalize due to the large amount of transistors present. The two circuits make up a substrate coupling network that contains close to 100 contacts that have a wide range of shapes and sizes. This chapter will take the results found in Chapter 5 and generalize them to simple cases with a few contacts. Large contact sizes are used to symbolize large digital and analog blocks that would be found in mixed-signal SoCs.

## 6.1. Heavily Doped Substrate

Figure 6.1 shows the substrate coupling model for a set of contacts spaced 200 $\mu m$ apart in the heavily doped substrate. The injector contact is 1 $mm^2$ and the sensor contact is 0.09 $mm^2$. The main noise coupling path between the two contacts is made up by the $R_{11}$ resistors when the backplane is floating. This is because the path through the heavily doped bulk of the substrate ($R_{11}$ resistors) provides a much lower impedance than the channel stop and epi layers ($R_{12}$ resistor).

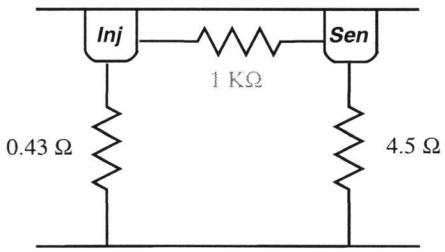



FIGURE 6.1. Substrate coupling model for a 1 $mm^2$ contact and a 0.09 $mm^2$ contact in the heavily doped substrate.

Figure 6.2 shows the same model as shown in Figure 6.1 with the die perimeter ring grounded. The bondwire inductance in the connection to the die

perimeter ring has been excluded for simplicity. In this case the $R_{11}$ value for the die perimeter ring is smaller than the $R_{11}$ value for the sensor contact and larger than the $R_{11}$ value for the injector contact. This illustrates that the effectiveness of the die perimeter ring depends on the size of the contacts in the substrate.

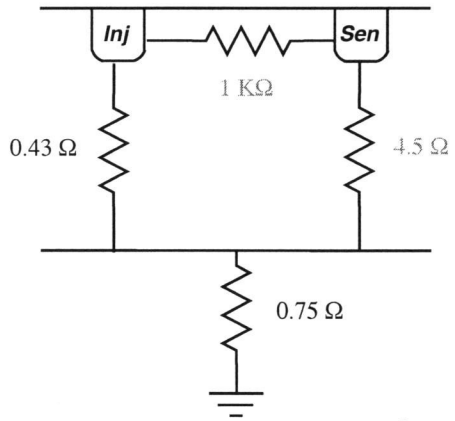



FIGURE 6.2. Substrate coupling model for a 1 $mm^2$ contact and a 0.09 $mm^2$ contact in the heavily doped substrate with the die perimeter ring grounded.

Consider the case where the injector and sensor contacts are both 1 $mm^2$ and the sensor contact is grounded. A large portion of the noise from the injector contact will flow to the sensor contact rather than through the backplane because the impedance through the die perimeter ring would be almost double what is seen through the sensor. The noise coupling to the sensor could be reduced by decreasing the $R_{11}$ value of the die perimeter ring. This is done by increasing it's overall area.

The case with a guard ring around the sensor contact is shown in Figure 6.3. The guard ring is 10 $\mu m$ wide and spaced 20 $\mu m$ from the sensor contact and 200 $\mu m$ from the injector contact. The inductance in the bondwire connected to the guard ring has been excluded for simplicity.

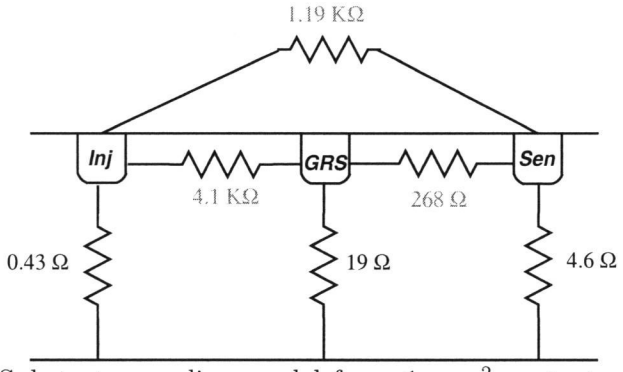



FIGURE 6.3. Substrate coupling model for a 1 $mm^2$ contact and a 0.09 $mm^2$ contact in the heavily doped substrate with a guard ring around the 0.09 $mm^2$ contact.

The $R_{11}$ value for the guard ring is still much larger than the $R_{11}$ value for the sensor when the backplane is floating. As a result, most of the noise from the injector will continue to flow to the sensor. One main difference between what is seen here and what was seen in Chapter 5 is the contact sizes. The contact sizes for the individual transistors in the op-amp are much smaller than the 0.09 $mm^2$ contact used here. These smaller contacts had larger $R_{11}$ values. As a result, a large portion of the noise was shunted to ground through the guard ring rather than coupling to the transistors as seen here. This illustrates that using a very large contact to represent a large circuit will give results with more noise coupling than what would be expected from an actual circuit.

Figure 6.4 shows the case with a guard ring placed around both the sensor and injector contacts. In this case the guard rings are both 10 $\mu m$ wide and separated by 200 $\mu m$. The $R_{11}$ value for the injector guard ring is lower than the $R_{11}$ value for the sensor guard ring because the area of the injector guard ring is larger than the sensor guard ring. In this case the two $R_{11}$ values for the guard

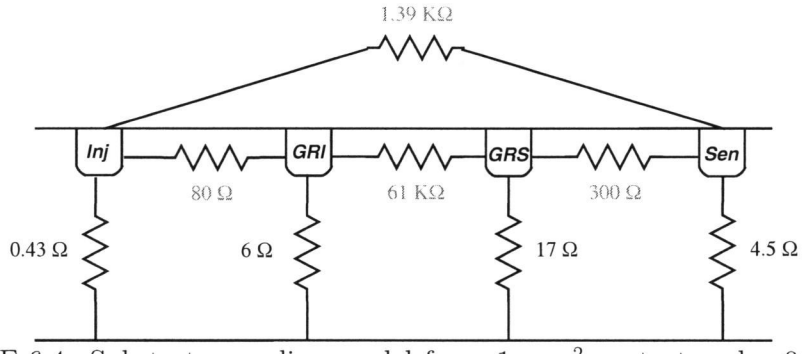



FIGURE 6.4. Substrate coupling model for a 1 $mm^2$ contact and a 0.09 $mm^2$ contact in the heavily doped substrate with guard rings around both contacts separated by 200 $\mu m$.

rings are seen in parallel which reduces the resistance to ground through the guard rings to 4.4 Ω.

Figure 6.5 shows the substrate model for the case where there is only a 50 $\mu m$ space between the guard rings. The only values that change (from the 200 $\mu m$ separation case) are the $R_{12}$ value between the contacts and the $R_{12}$ value between the guard rings. These values are much larger than the other values so the overall noise coupling between the contacts remains the same. When the two guard rings are combined with the grounded die perimeter ring a large improvement will not be seen when compared to the case with just the die perimeter ring grounded. This is because the die perimeter ring impedance to ground is 4 times smaller than the guard rings in parallel.

All of the simple simulated results presented here are consistent with what was found in Chapter 5. In the heavily doped process the majority of the noise coupling takes place through the low resistivity bulk. Since the $R_{11}$ values don't depend on spacing, contact placement doesn't make a very big difference in the

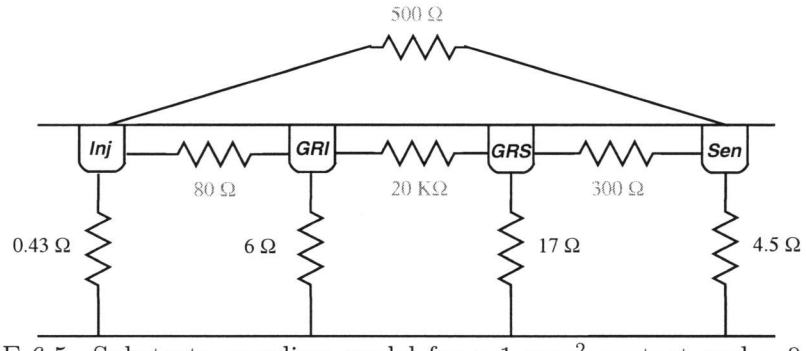



FIGURE 6.5. Substrate coupling model for a 1 $mm^2$ contact and a 0.09 $mm^2$ contact in the heavily doped substrate with guard rings around both contacts separated by 50 $\mu m$.

noise coupling results. As a result of the $R_{11}$ value having a strong dependence on contact size, larger guard rings provide better isolation.

## 6.2. Lightly Doped Substrate

Figure 6.6 shows the substrate coupling model for a 1 $mm^2$ contact and a 0.09 $mm^2$ contact spaced at 200 $\mu m$ in the lightly doped substrate. In this case the resistance in the coupling path through the $R_{12}$ resistor is closer to the resistance made up from the two $R_{11}$ resistors. Thus, a significant amount of the noise seen on the sensor contact will be from noise coupled through the $R_{12}$ resistor. When compared to the heavily doped case the $R_{11}$ values are much higher due to the higher resistivity found in the lightly doped bulk. The $R_{12}$ values are much lower as a result of the channel stop layer having a lower resistivity in the lightly doped process than in the heavily doped process.

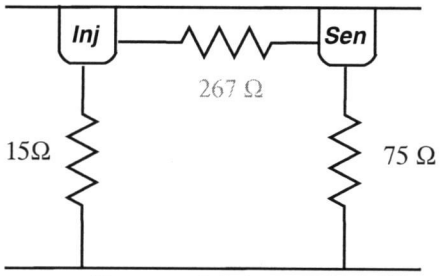



FIGURE 6.6. Substrate coupling model for a 1 $mm^2$ contact and a 0.09 $mm^2$ contact in the lightly doped substrate.

The same two contact substrate model with the die perimeter ring grounded is shown in Figure 6.7. It is obvious that grounding the die perimeter ring will provide a low enough impedance to ground to improve the noise coupling between the two contacts. The path to ground through the die perimeter ring is much smaller than both the $R_{11}$ and $R_{12}$ paths to the sensor contact.

It should be noted that the case simulated in Chapter 5 had much smaller contacts that what is being simulated here. In the case of the op-amp and the stepped buffer, the $R_{11}$ values for the contacts are much higher and a large portion

of the noise coupling takes place through the $R_{12}$ resistors. When measurements were taken no change was seen in the lightly doped case when the die perimeter ring was grounded. This is partially due to high $R_{11}$ values, but also because the mutual inductance from the bondwires was so large that the small change in noise magnitude could not be detected.

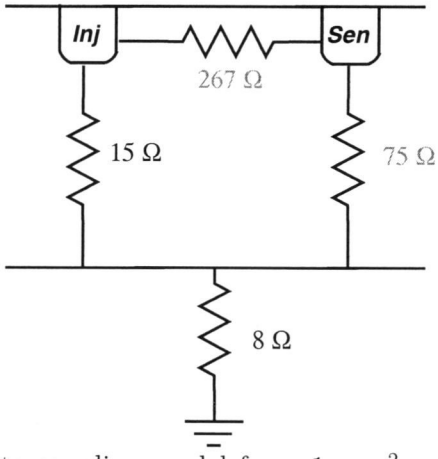



FIGURE 6.7. Substrate coupling model for a 1 $mm^2$ contact and a 0.09 $mm^2$ contact in the lightly doped substrate with the die perimeter ring grounded.

Figure 6.8 shows the case with a 10 $\mu m$ guard ring around the sensor contact. The $R_{12}$ value between the guard ring and the sensor contact is very small and provides a lower impedance coupling path than seen in the case without the guard ring. One must keep in mind that the guard ring is grounded and most of the noise will be shunted away. This shows the importance of having a low inductance in the guard ring connection. If the inductance is too large, more noise will be injected into the sensor than seen in the case with no guard rings.

When both guard rings are added (shown in Figure 6.9) the impedance in the noise coupling path continues to decrease. When the guard ring around the injector contact is added, the noise coupling path through the backplane decreases while the path through the channel stop layer increases. In a case with

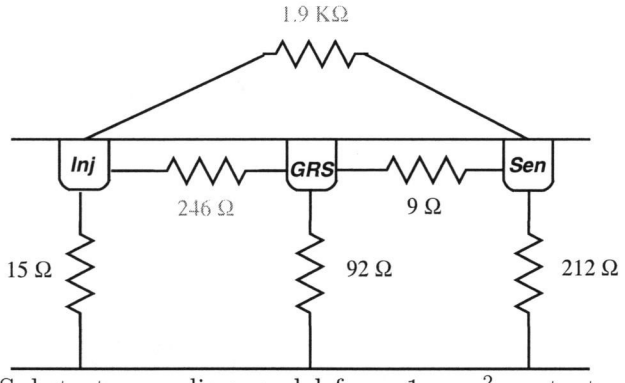



FIGURE 6.8. Substrate coupling model for a 1 $mm^2$ contact and a 0.09 $mm^2$ contact in the lightly doped substrate with a guard ring around the 0.09 $mm^2$ contact.

smaller contacts (and larger $R_{11}$ values) a large improvement is seen as a result of the increasing $R_{12}$ values. Figure 6.10 shows the substrate coupling model for the case when the contacts and guard rings are moved so there is only 50 $\mu m$ between them. As the two contacts and guard rings are moved closer the $R_{12}$ value between the guard rings reduces significantly affecting the substrate noise coupling performance.

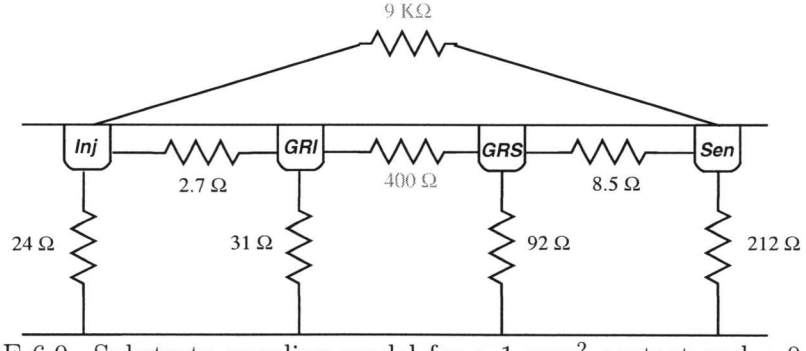



FIGURE 6.9. Substrate coupling model for a 1 $mm^2$ contact and a 0.09 $mm^2$ contact in the lightly doped substrate with guard rings around both contacts separated by 200 $\mu m$.

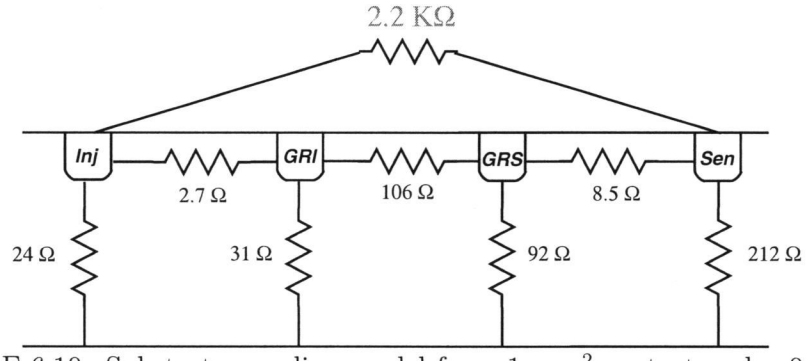



FIGURE 6.10. Substrate coupling model for a 1 $mm^2$ contact and a 0.09 $mm^2$ contact in the lightly doped substrate with guard rings around both contacts separated by 50 $\mu m$.

The generalized results seen here are all consistent with those in Chapter 5. In the lightly doped substrate, the substrate noise coupling is dependent on the size of the contact as well as the spacing. Guard rings can provide improvement, but care must be taken to minimize the amount of noise present on the guard ring and to separate the guard rings as much as possible. The amount of noise on the guard ring can be reduced by reducing the amount of inductance in it's ground connection and the spacing between guard rings can be maximized by making the guard ring widths as small as possible.

Tables 6.1 and 6.2 summarize the generalized data for the heavily and lightly doped processes.

TABLE 6.1. Summary of guard rings in the heavily doped process.

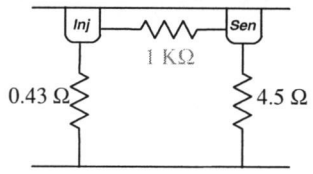
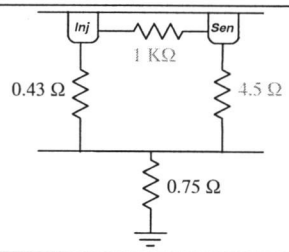
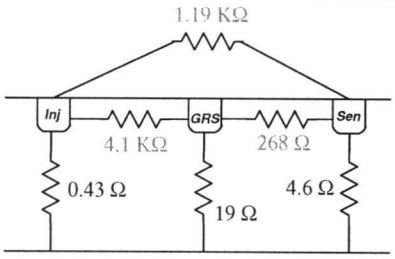
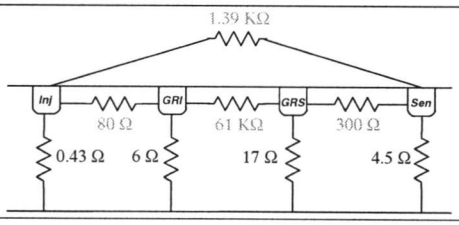
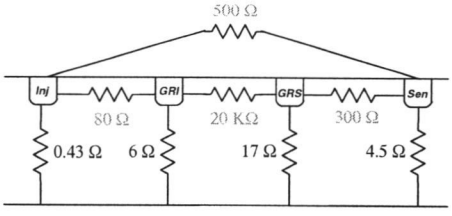
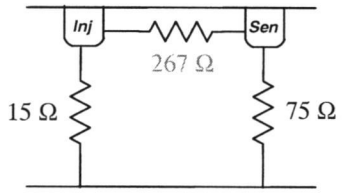
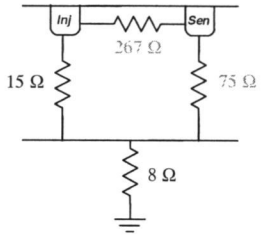
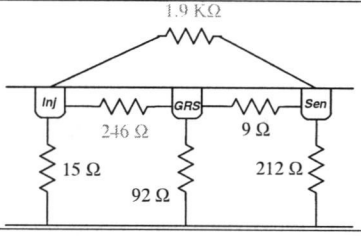
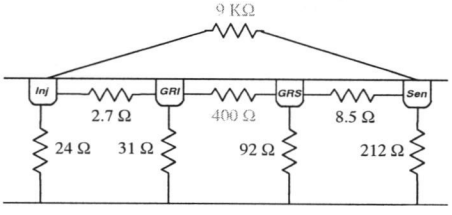
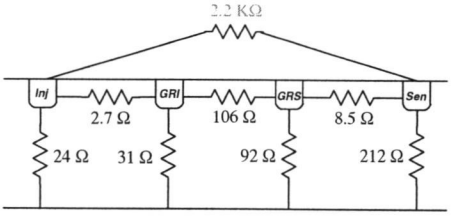
| Design Technique<br>**Performance Rating** | Equivalent Circuit | Dominant coupling path<br>Design Recommendation |
|---|---|---|
| No Guard Ring<br>**Worst Performance** |  | $R_{11}$ values dominate noise coupling<br>Reduce contacts sizes to increase $R_{11}$ values |
| Die Perimeter Ring Grounded<br>**Best Performance** |  | Most of the noise shunted to ground through the die perimeter ring<br>Increase area of the die perimeter ring to decrease it's resistance to ground |
| Single Guard Ring Around Sensor<br>**Medium Performance** |  | Some of the noise is shunted to ground through the guard ring<br>Increase area of the guard ring (by increasing it's width) to reduce the resistance to ground |
| Dual Guard Rings with Large Spacing<br>**Good Performance** |  | Most of the noise shunted to ground through the guard ring<br>Guard ring $R_{11}$ values seen in parallel. |
| Dual Guard Rings with Small Spacing<br>**Good Performance** |  | As spacing is reduced the dominant noise coupling path is unchanged.<br>Keep spacing larger then 4 times the epi thickness to avoid $R_{12}$ coupling. |

TABLE 6.2. Summary of guard rings in the lightly doped process.

| Design Technique<br>**Performance Rating** | Equivalent Circuit | Dominant coupling path<br>Design Recommendation |
|---|---|---|
| No Guard Ring<br>**Worst Performance** |  | Noise coupling takes place through $R_{11}$ and $R_{12}$ resistors<br>Reduce contacts sizes and increase spacing to increase resistor values |
| Die Perimeter Ring Grounded<br>**Best Performance** |  | Most of the noise is shunted to ground through the die perimeter ring<br>Increase area of the die perimeter ring to decrease it's resistance to ground |
| Single Guard Ring Around Sensor<br>**Medium Performance** |  | Most noise coupling takes place through guard ring<br>Reduce guard ring impedance to ground to minimize ground bounce |
| Dual Guard Rings with Large Spacing<br>**Good Performance** |  | Most noise coupling takes place through guard rings<br>Minimize guard ring impedance to ground in order to minimize ground bounce |
| Dual Guard Rings with Small Spacing<br>**Medium Performance** |  | Noise coupling takes place through $R_{12}$ resistor between guard rings<br>Increase spacing between guard rings as much as possible by decreasing guard ring width |

# 7. CONCLUSION AND FUTURE WORK

## 7.1. Conclusions

This thesis has compared substrate noise coupling between analog and digital building blocks in heavily doped and lightly doped processes. The effects of on-chip and off-chip parasitics have been explored along with methods to reduce or eliminate them in different stages of the design. Reducing bondwire and PCB trace lengths along with package parasitics can greatly improve the amount of ringing seen on power supplies and on other sensitive nodes. The modeling of interconnects, bondwires, packaging, and board traces when simulating are essential for accurate results. Techniques to include these elements have also been provided.

Measurements from two test chips fabricated in the TSMC 0.25 $\mu$m heavily doped and lightly doped processes validate simulations performed using Silencer! Measurements and simulations have shown that a lightly doped substrate can offer an improvement of up to 15 dB over heavily doped substrates. Large reductions in noise can also be achieved by carefully placing analog blocks to reduce the effects of mutual inductance. Additional simulations have shown that noise coupling can be further reduced through the use of a die perimeter ring in heavily doped circuits and guard rings in both heavily and lightly doped circuits.

## 7.2. Future Work

Future work in this area could include improving Silencer! to accommodate external parasitics such as bondwire and package parasitics. A system to more accurately account for high frequency coupling from on-chip interconnects

could also be included. For lightly doped substrates, a more complex backplane connectivity model could be implemented to include the effects of non-conductive epoxy to be easily simulated.

Isolation structures including n-wells and deep trenches can be also explored and combined with guard rings to find optimal isolation structures. Methods for grounding the backplane and creating guard structures that do not rely on bondwires would also be very beneficial in reducing substrate noise. Test chips in technologies such as flip-chip packaging should be looked into in order to evaluate the effects of different packaging on noise coupling.

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# APPENDICES

## APPENDIX A. Circuit Layout

A die photo of the lightly doped TSMC 0.25 $\mu$m chip is shown in Figure A-1.

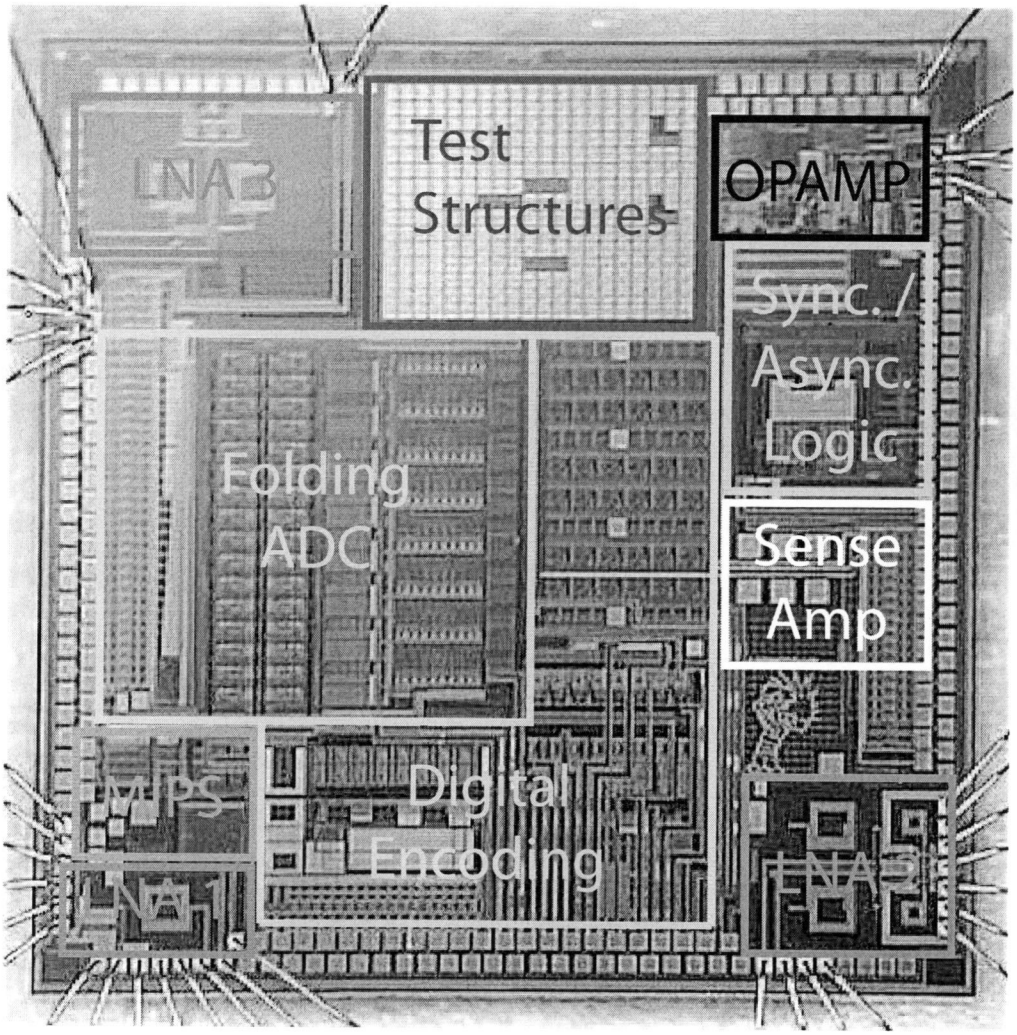


FIGURE A-1. TSMC 0.25 $\mu$m test chip.

The section labeled "OPAMP" in the upper right hand corner of the layout is where the op-amp and stepped buffer used in this work are located. They are

placed as close as possible to the edge of the chip in an effort to minimize routing parasitics.

Figure A-2 shows the layout of the stepped buffer. By observing the layout it can be seen that all of the substrate taps for the transistors are tied to the source. This maximizes substrate noise by allowing any noise created from supply bounce to be injected directly into the substrate via the substrate taps.

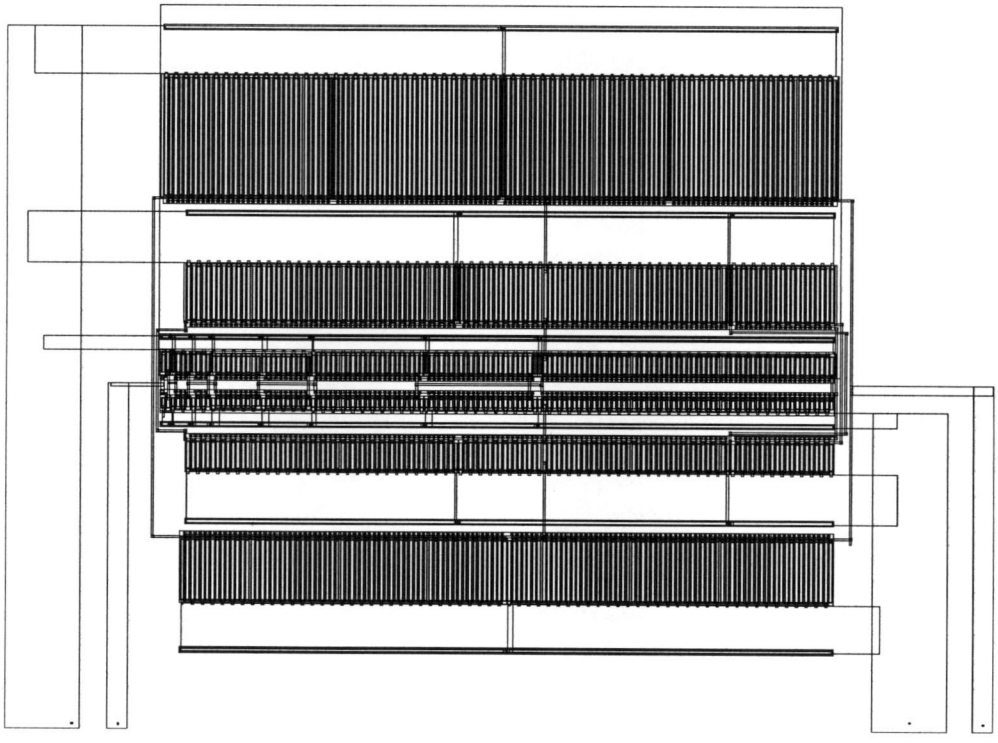

FIGURE A-2. Layout for the stepped buffer with source and bulks connected.

The op-amp layouts for the heavily and lightly doped processes are shown in Figures A-3 and A-4, respectively. The two layouts are identical with the exception of the capacitors. The lightly doped process features an array of 8 very accurate metal to metal capacitors while the heavily doped layout features an array of six MOS caps that are generally only accurate to about 20%. The heavily doped

process uses the MOS capacitors because the technology is primarily for digital circuitry where accurate capacitor sizes are not needed. The noise coupling to the capacitors has been neglected in both cases. The MOS capacitors are made from PMOS transistors which are neglected from the model because of the capacitance between the n-well and the substrate. The metal to metal capacitors have been neglected because they are located between metal layers four and 5 where the capacitance to the substrate is on the order of 1 fF and can be neglected.

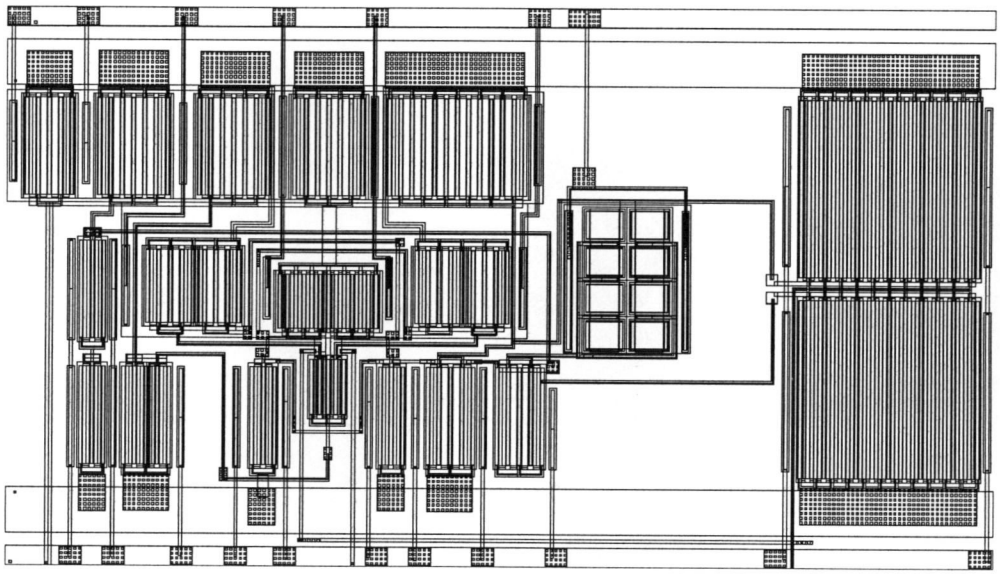

FIGURE A-3. Layout for the op-amp in the heavily doped process.

## APPENDIX B. Board Design

In order to minimize the board parasitics the board design is broken into two separate parts; the mother board and the daughter board. The mother board is designed to supply power, signal I/Os, and a few other logic switches. The smaller daughter board is designed to house the test chip, decoupling caps, and a single output.

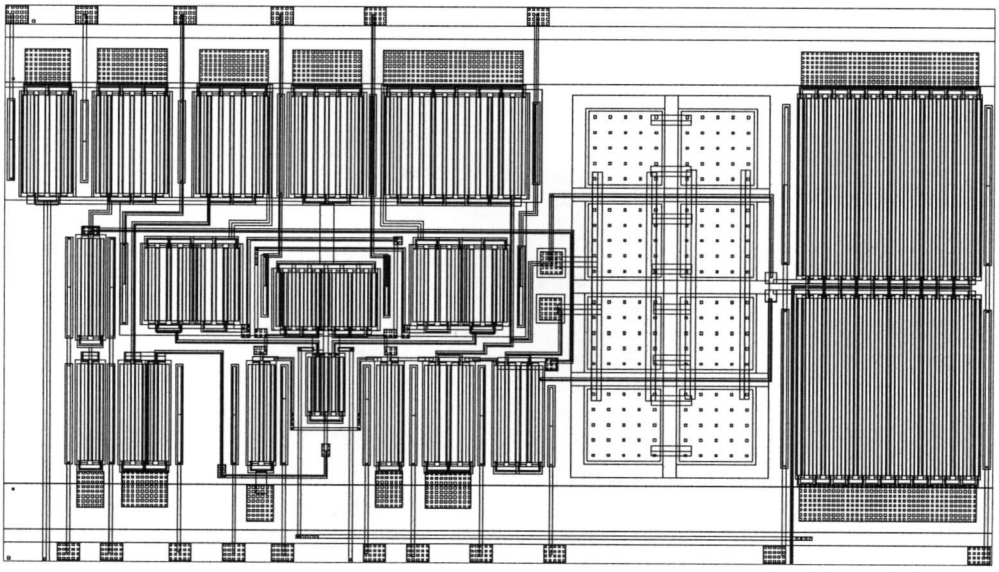

FIGURE A-4. Layout for the op-amp in the lightly doped process.

The schematic for the mother board is shown in Figure B-5. On the left the two different power supplies are shown. Separate power supplies are used for the digital and analog circuitry to eliminate any off-chip digital supply noise coupling to the analog circuitry. Each of the circuits have their own jumpers so that any one of the three digital blocks or two analog blocks can be turned off and on as they are needed. In the center of the schematic the digital and analog I/Os are seen along with the two bias currents needed for the two op-amps. The two connectors that connect the mother board to the daughter board are seen on the right.

The layout of the mother board is shown in Figure B-6. Ground planes (not shown) are filled in on both the top and bottom copper layers in order to minimize the noise seen on the analog bias circuitry and I/Os. Although the ground planes

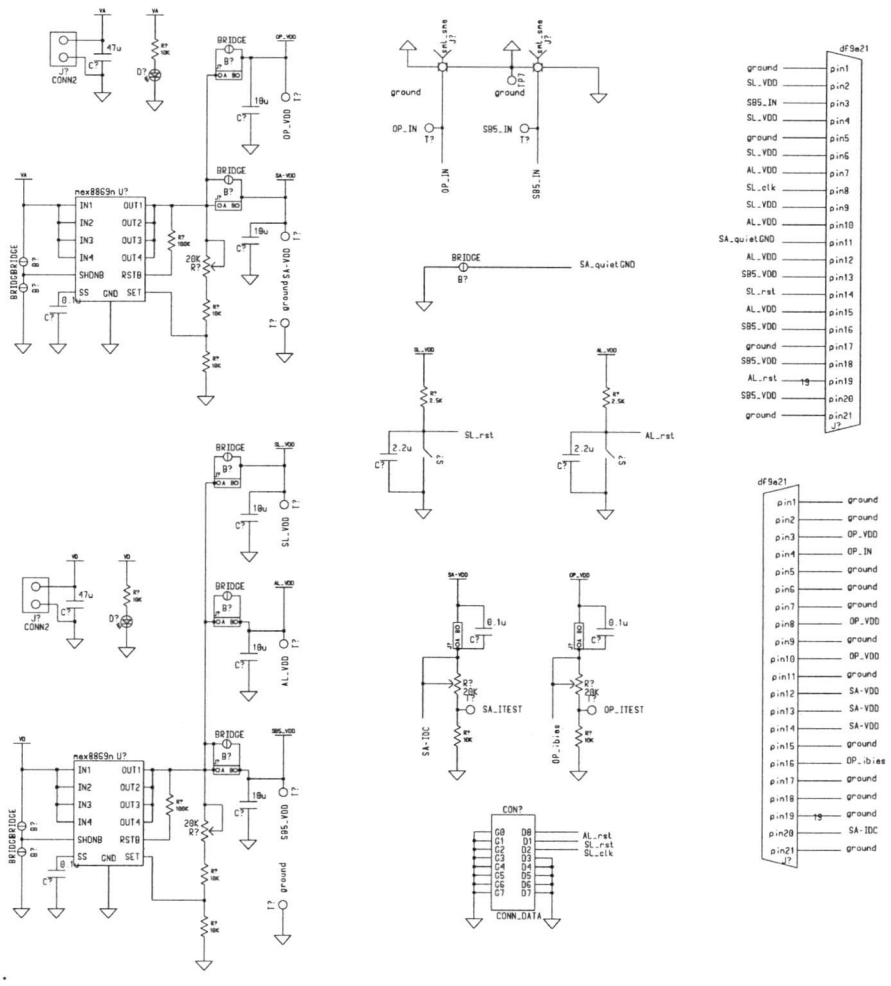


FIGURE B-5. Schematic for the mother board.

are shared by the analog and digital circuitry, the two power sources and their respective circuitry are separated to opposite ends of the board to avoid cross talk.

The daughter board schematic is shown in Figure B-7. It contains the chip footprint, decoupling caps, connectors to the mother board, and a single analog output. The footprint for the daughter board, shown in Figure B-8, was carefully constructed to minimize the length of bondwire needed to connect the chip to the

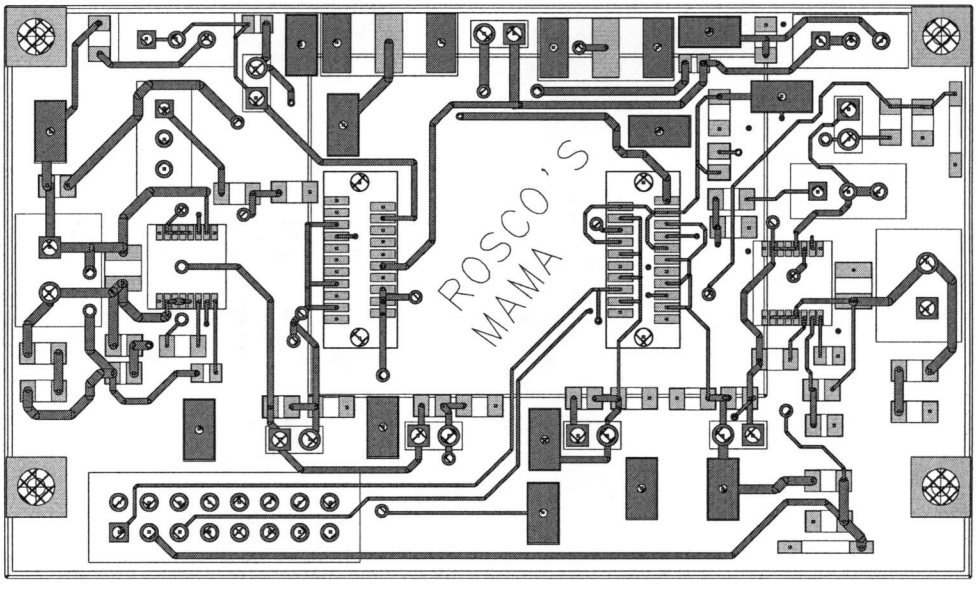


FIGURE B-6. Layout for the mother board.

board. The 6 mil x 6 mil bond pads are spaced 6 mils from the die paddle and have a 14 mil pitch. These are the minimum dimensions that the wire bonding equipment would allow.

The layout for the daughter board, shown in Figure B-9, is constructed as small as possible to minimize trace length. The decoupling capacitors on all of the power supplies are placed within 50 mils of the bond pads and the ground connection for the die parameter ring is within 20 mils. This will reduce the inductance in order to prevent a high impedance path to ground as seen in Section 3.3.

Figures B-10, B-11, B-12 show pictures of the mother board, daughter board, and the two boards connected together, respectively.

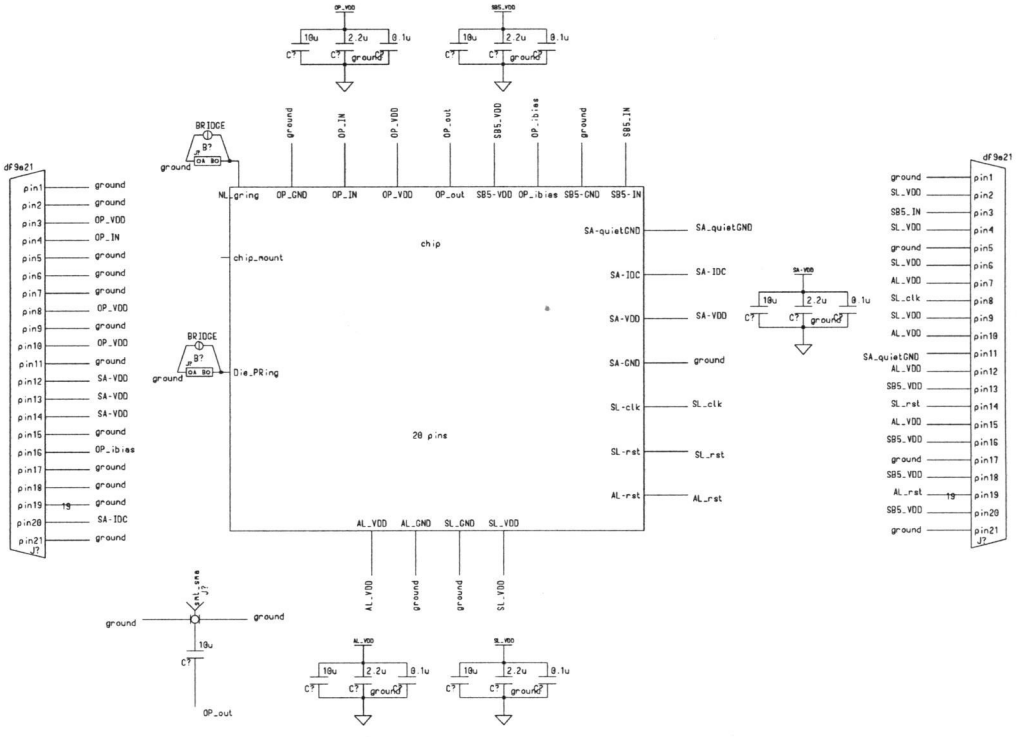


FIGURE B-7. Schematic for the daughter board.

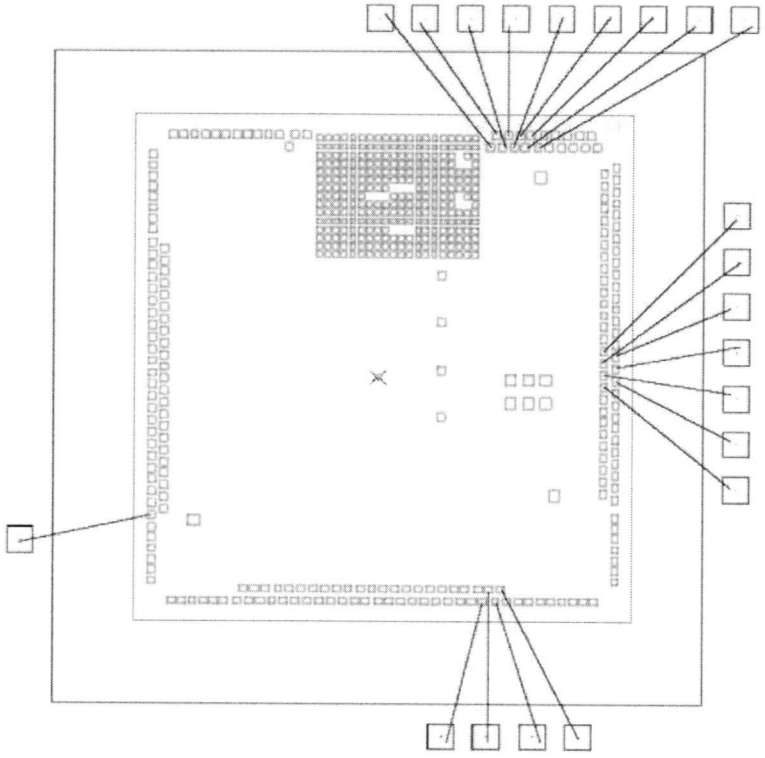

FIGURE B-8. Bonding diagram for the TSMC 0.25 $\mu$m chip.

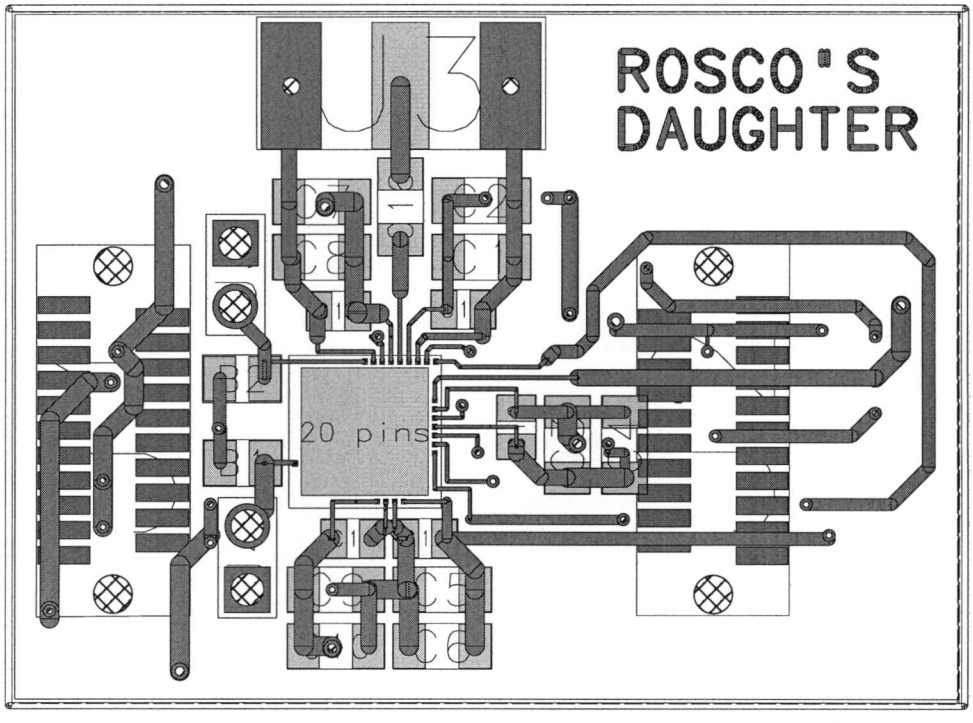


FIGURE B-9. Layout for the daughter board.

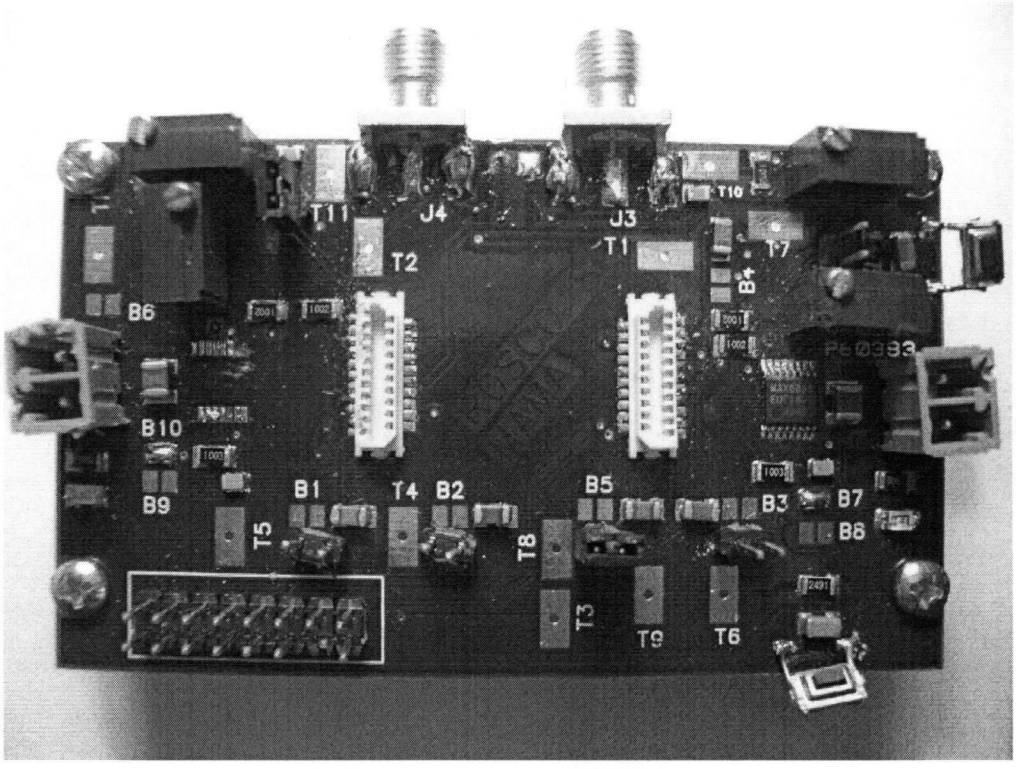


FIGURE B-10. Picture of assembled mother board.

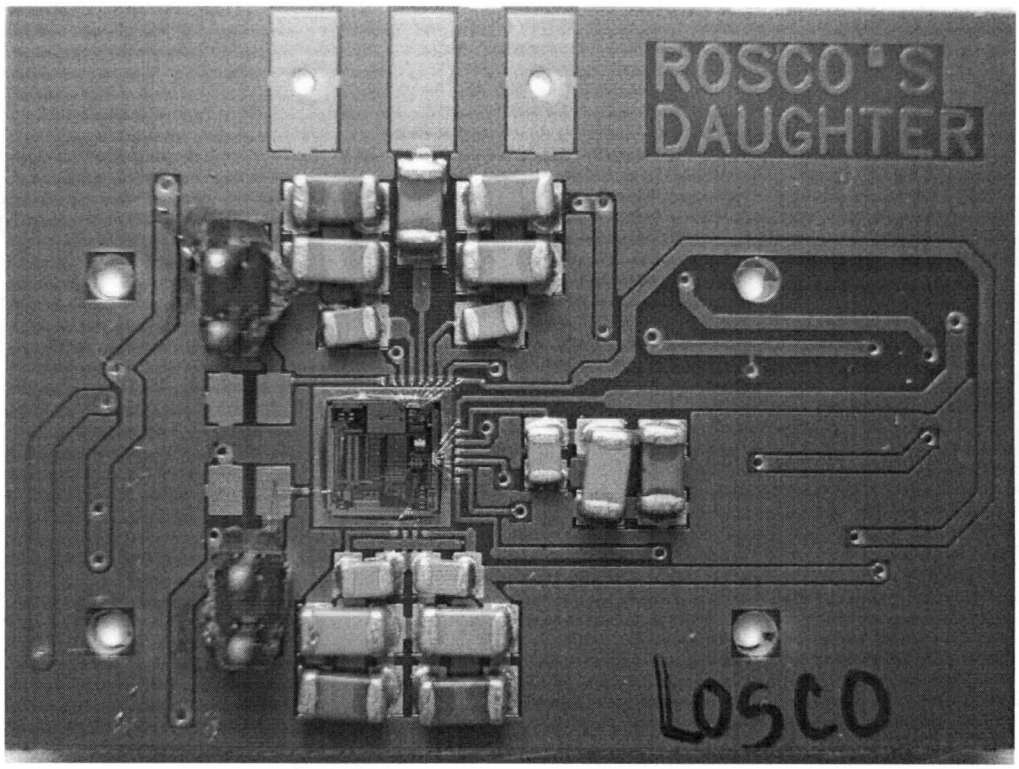


FIGURE B-11. Picture of assembled daughter board.

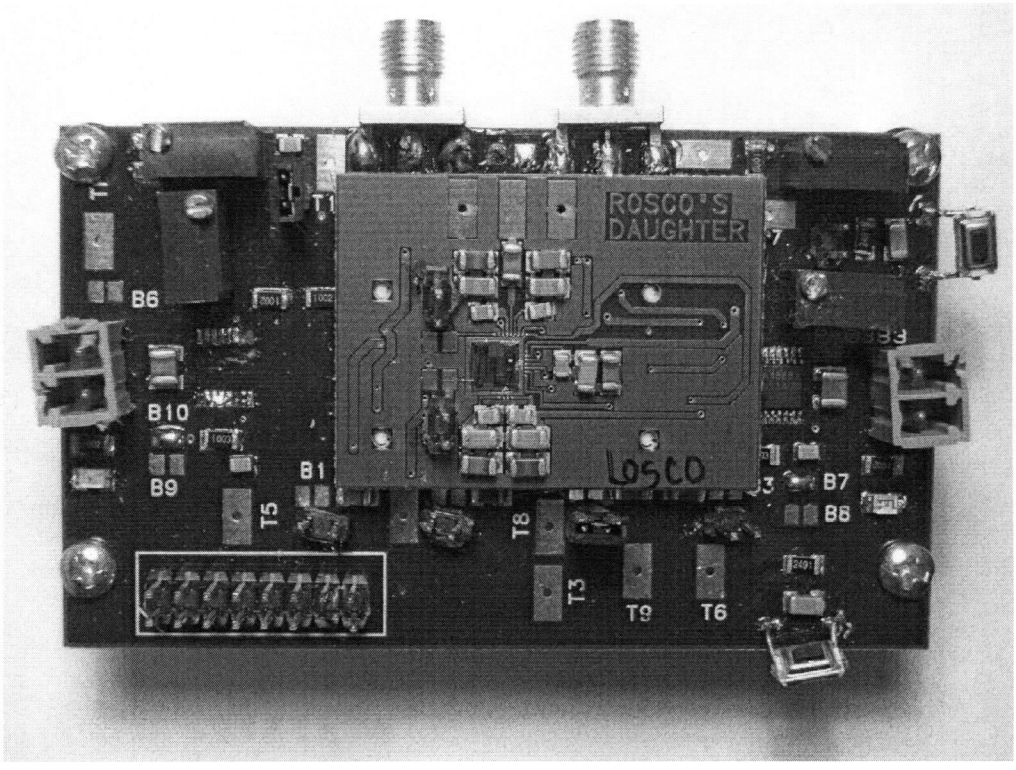


FIGURE B-12. Picture of the two boards connected together.

## APPENDIX C. Op-amp Design

The op-amp used here was originally presented in [8]. The op-amp utilizes two sets of input differential pairs in order to achieve a high dynamic range. A schematic of the first gain stage is shown in Figure C-13.

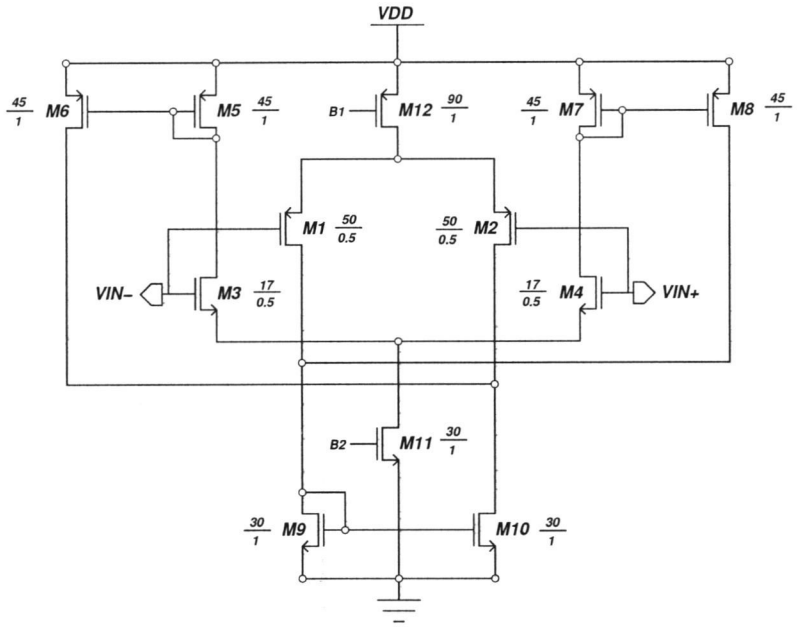


FIGURE C-13. The first gain stage of the two stage high-swing opamp.

In the TSMC 0.25 $\mu$m process the mobility of the NMOS devices is about 3 times as high as the mobility of the PMOS devices. For this reason the current source for the NMOS input pair (M11) is sized three times smaller than the current source for the PMOS input pair (M12). This factor of three assures that equal currents for both the NMOS and PMOS devices will be summed at the drain of transistors M9 and M10.

The NMOS input pair is sized at $\frac{17\mu m}{0.5\mu m}$ and the PMOS input pair is sized at $\frac{50\mu m}{0.5\mu m}$. 0.5 $\mu$m channel lengths are used to increase the $g_m$ value of the transistors in order to boost their gain. The current from the NMOS differential pair is

mirrored through two PMOS current mirrors (M5, M6, M7, and M8). This allows the signal from the NMOS differential pair be summed with the signal from the PMOS differential pair at the drain of transistors M9 and M10. When the current is mirrored an inversion occurs resulting in the current from the positive NMOS device being summed with the current from the negative PMOS device.

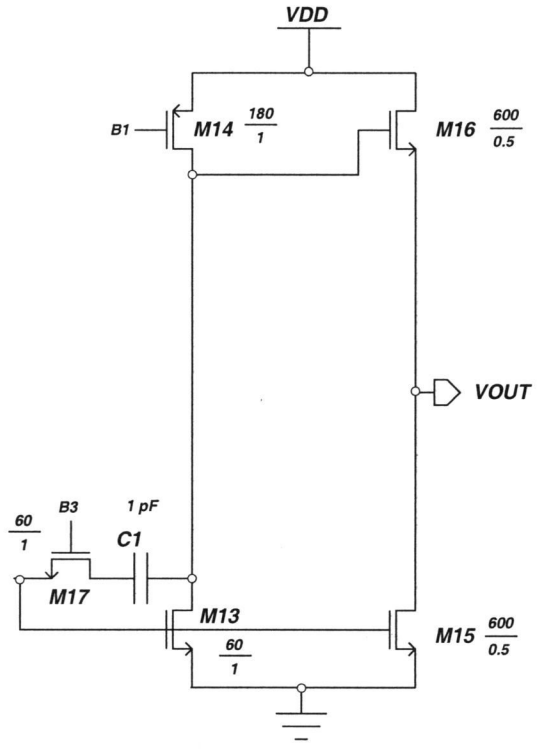


FIGURE C-14. The second gain stage of the two stage high-swing opamp.

The second gain stage is shown in Figure C-14. The amplifying NMOS transistor is sized at $\frac{60\mu m}{1\mu m}$ and is supplied current by a PMOS transistor sized at $\frac{180\mu m}{1\mu m}$. The stage is compensated with a 1 pF capacitor and a transistor operating in triode (M17). This transistor is used as a resistor to cancel the right-half-plane zero created by the compensation capacitor [9]. Transistor M17 is the same size as M13 in order to exactly match the $r_{ds}$ value and cancel the zero.

M15 and M16 make up a buffer to allow the op-amp to drive low impedance loads. The buffer is a source follower with a gain close to 1. Both the transistors in the buffer are of large size very large in order minimize their drain to source voltage drop. This will maximize the amount of output voltage swing.

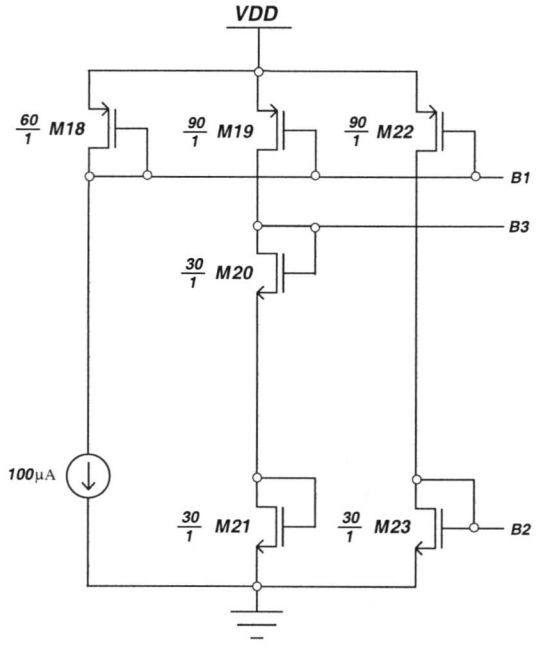


FIGURE C-15. The biasing for the two stage high-swing opamp.

Figure C-15 shows the biasing network used for the two stage op-amp. M18 is sized so that it's $V_{dsat}$ value is about 225 $mV_{p-p}$. This will set the same $V_{dsat}$ voltage for all other transistor biased from it. Bias point B1 is generated for the PMOS current source for the PMOS differential pair in the first stage and PMOS current source is the second stage. B2 is generated for the NMOS current source in the first stage and B3 generates the biasing for the compensation transistor.

## APPENDIX D. Measured Data

In the lab, the stepped buffer and op-amp were operation on separate 2.5 V power supplies. The stepped buffer had a 10 MHz square wave input with rise time of 14 nS and a fall time of 5 nS. The op-amp had a DC bias of 0.5 V on the input. The measured results take for the lightly doped, heavily doped, and heavily doped with die perimeter ring grounded are seen below. The measurements seen in Figures D-16, D-22, and D-19 where taken with higher averaging. This explains why they appear cleaner than the other measurements.

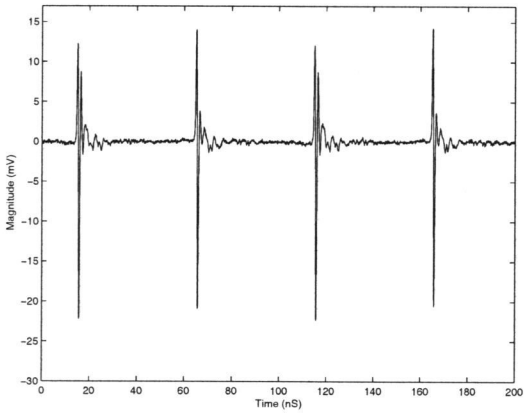


FIGURE D-16. Measurement 1 for the lightly doped substrate.

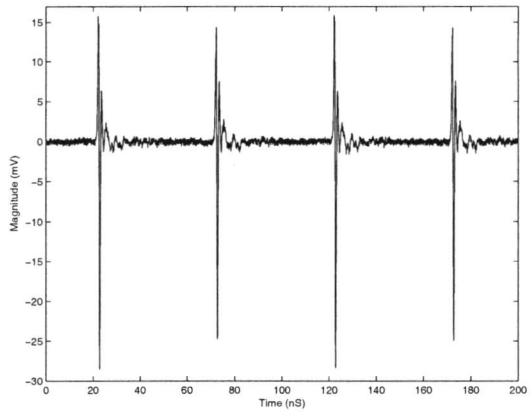


FIGURE D-17. Measurement 2 for the lightly doped substrate.

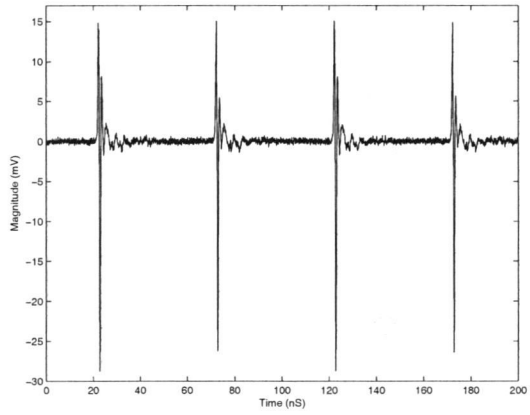


FIGURE D-18. Measurement 3 for the lightly doped substrate.

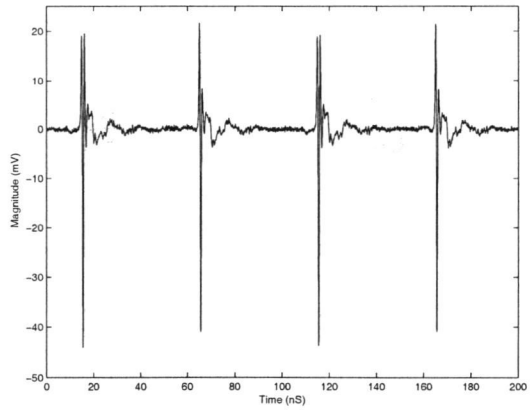


FIGURE D-19. Measurement 1 for the heavily doped substrate.

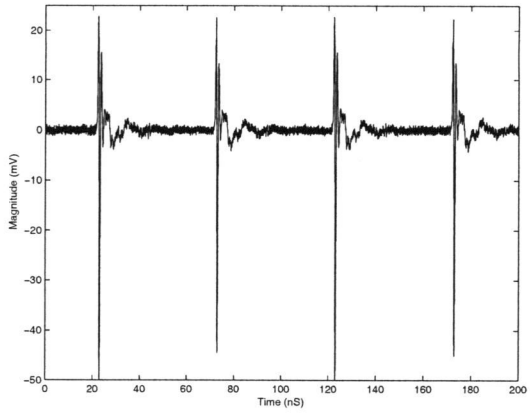


FIGURE D-20. Measurement 2 for the heavily doped substrate.

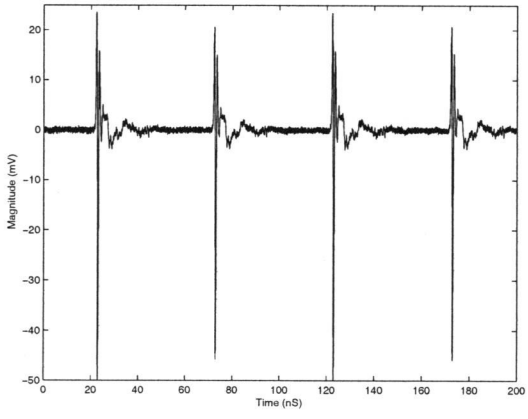


FIGURE D-21. Measurement 3 for the heavily doped substrate.

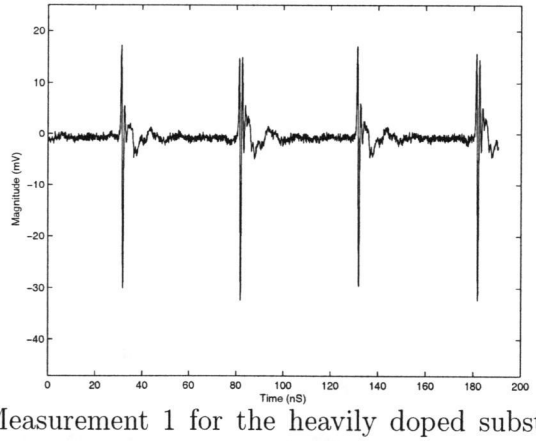


FIGURE D-22. Measurement 1 for the heavily doped substrate when the die perimeter ring is grounded.

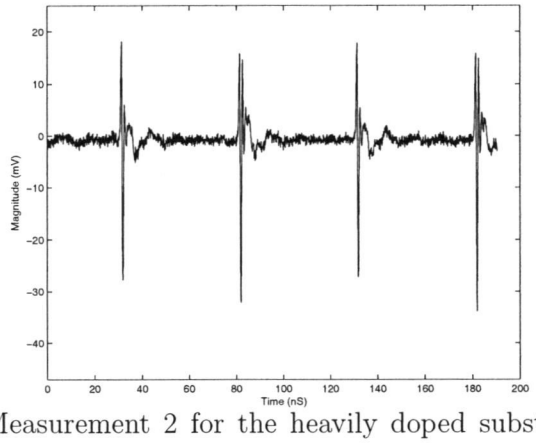


FIGURE D-23. Measurement 2 for the heavily doped substrate when the die perimeter ring is grounded.

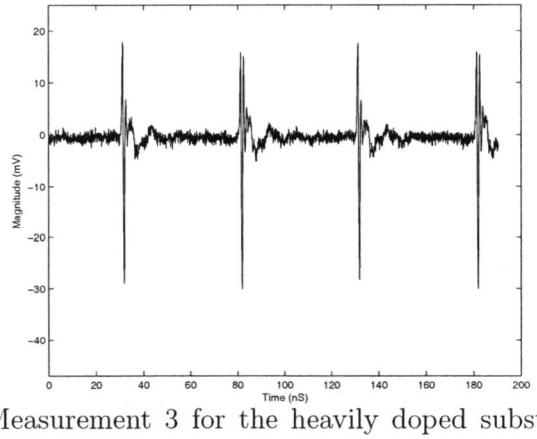


FIGURE D-24. Measurement 3 for the heavily doped substrate when the die perimeter ring is grounded.

## APPENDIX E. Modeling Interconnect and Mutual Inductance

In order to get accurate results from simulations, coupling to interconnects and bondwires have to be accounted for. Metal layers that are close to the surface of the substrate can contribute a non-negligible amount of noise to the inputs, outputs, and power supply lines to sensitive circuits. "Quiet" bondwires (analog signals and power supply lines) that are located in close proximity to digital signals can couple large amounts of noise into the circuits and the substrate. Methods for modeling these effects are discussed below.

The on-chip interconnects are modeled as extra contacts in Silencer! These interconnects include the bondpads and routing that are connected to each of the circuits. A p implant active layer is drawn in the layout in the same shape as the bondpads and metal interconnects. These active regions are then labeled using names that will be easy to associate in the schematic. The substrate coupling network is then calculated and added to the schematic.

In the schematic the contacts created to model the interconnects need to be joined to actual nodes on the schematic. This is done through a capacitance that connects the substrate contacts to the actual nodes in the schematic. These capacitance values depend on the size of the metal interconnect and bondpad and the metal layers that are on. Measured process parameters found on the Mosis website give values for the capacitance to be used.

Consider the ground connection to the stepped buffer. The bondpad and metal routing are both on metal layer 1 and cover an area of about 4000 $\mu m^2$. The measured process parameters on the Mosis website report that the metal 1 to substrate capacitance is 35 af/$\mu m^2$. This results in a capacitance of 150 fF connecting the ground node on the stepped buffer to the substrate contact.

As a result of the op-amp and stepped buffer being placed close to each other mutual inductance between bondwires becomes a large coupling path. The "MIND" component in Cadence is used to model the effects of noise coupling between bondwires. The MIND component requires three parameters: inductor 1, inductor 2, and the coupling coefficient between the two inductors. The coupling parameter is given by:

$$k = \frac{M}{\sqrt{L_1 L_2}} \tag{A.1}$$

where $M$ is the mutual inductance and $L_1$ and $L_2$ are the two bondwire inductors. The mutual inductance is given by:

$$M = \frac{\mu_0 l}{2\pi}[ln(\frac{2l}{D}) - 1 + \frac{D}{l}] \tag{A.2}$$

where $\mu_0$ is the permeability of free space, $l$ is the length of the bondwires, and $D$ is the distance between them.

Consider two bondwires that are each 1.5 mm in length separated by 500 $\mu m$. Using equation 4.2 (assuming the bondwires are 1 mil in diameter) the inductance for each bondwire is 1.4 nH. Plugging this value into equations A.1 and A.2 result in a mutual inductance of 337 pH and a coupling coefficient of 0.24.

Figure E-25 shows the noise contribution from mutual inductance on a sensor contact when the distance between their bondwires are varied. A 100 MHz noise source with a peak-to-peak magnitude of 100 $mV_{p-p}$ is connected to a injector contact and the noise magnitude from mutual inductance is measured on the sensor contact. The injector contact has an area of 1 $mm^2$ and the sensor contact is 0.09 $mm^2$. Each contact has a 1.5 nH bondwire connected to ground.

The noise magnitude decreases exponentially with distance. As the distance between the bondwire increase beyond 1.5 mm, the noise magnitude converges to the value represented by the substrate coupling. Figure E-25 plainly

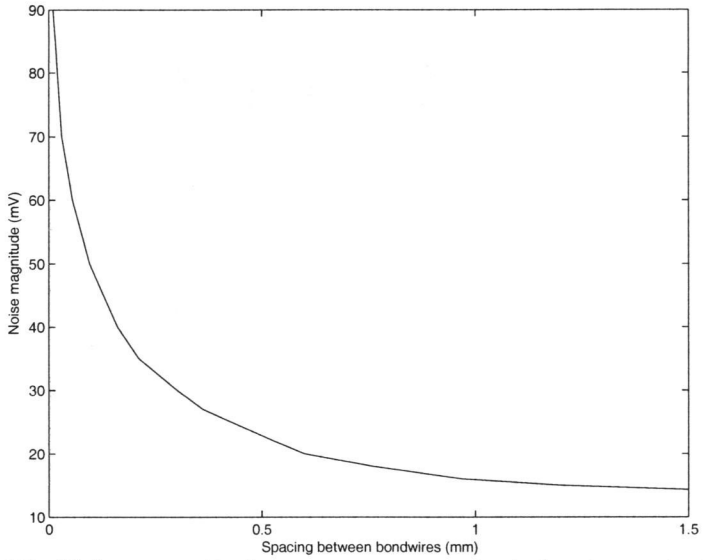


FIGURE E-25. Noise magnitude on a sensor contact due to mutual inductance from a 1.5 nH bondwire.

shows that the contribution to noise coupling due to mutual inductance can far exceed the amount of noise from the substrate if bondwires are spaced too close together.