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Title: Low-Power High-Linearity Digital-to-Analog Converters.

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Gabor C. Temes

In this thesis work, a design of 14-bit, 20MS/s segmented digital-to-analog converter (DAC) is presented. The segmented DAC uses switched-capacitor configuration to implement 8 (LSB) + 6 (MSB) segmented architecture to achieve high performance for minimum area. The implemented LSB DAC is based on quasi-passive pipelined DAC that has been proven to provide low power and high speed operation. Typically, capacitor matching is the best among all integrated circuit components but the mismatch among nominally equal value capacitors will introduce nonlinear distortion. By using dynamic element matching (DEM) technique in the MSB DAC, the nonlinearity caused by capacitor mismatch is greatly reduced. The output buffer employed direct charge transfer (DCT) technique that can minimize *kT/C* noise without increasing the power dissipation. This segmented DAC is designed and simulated in 0.18 μm CMOS technology, and the simulated core DAC block only consumes 403 μW.

Low-Power High-Linearity Digital-to-Analog Converters

by
Ming-Hung Kuo

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APPROVED:

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Ming-Hung Kuo, Author

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Low-Power High-Linearity Digital-to-Analog Converters

CHAPTER 1 INTRODUCTION

1.1 Motivation

Digital-to-analog conversion is essential in many digital systems that need to transfer digital information into analog signals, and many of these systems require high performance digital-to-analog converters (DAC). With CMOS technology shrinking and the evolution in communication systems, the demand for DACs has increased the system on chip (SOC) applications. These applications include the device in consumer electronics, instrumentation, wired and wireless communication and biomedical areas. Many of these applications are in portable devices, hence low power design is crucial for longer battery life.

1.2 System Specification

Most DACs utilized matched components such as resistors, capacitors and MOS switches to perform accurate data conversions. Actual circuit fabrication for nominally equal value components will vary due to unpredictable process variations. These variations or mismatch errors will ultimately diminish the data converter performance. In modern CMOS processes, capacitor matching is typically the best among the integrated circuit components. Thus, switched-capacitor based DAC offers a significant advantage for high resolution applications. In this thesis, a 14-bit, 20 MS/s segmented DAC has been designed in 0.18 μm CMOS technology. The system top block diagram is shown in

Figure 1.1. The segmentation consists of two parts, one is the LSB DAC, and the other is the MSB DAC. The LSB DAC is implemented using binary code as it consumes less chip area. For greater linearity, MSB DAC is implemented using thermometer (unary) code. However, unary coded DAC consumes larger chip-area [1]. The segmented architecture is popular among DAC designs [2], [3], [4] as it offers good balance between performance and chip-area. In this design, the segmentation uses 8-bit binary and 6-bit unary.

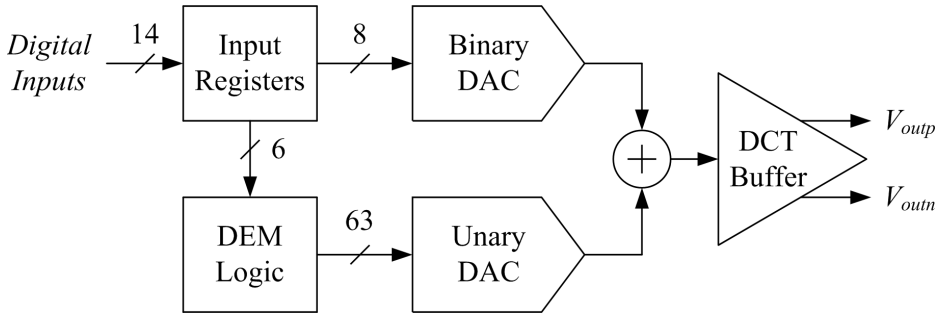


Figure 1.1. Block diagram of 14-bit segmented DAC

1.3 Thesis Organization

This thesis is divided into six chapters. Chapter 1 briefly introduce the design and research motivation of low power, high linearity DAC and the system architecture of the designed DAC. Chapter 2 covers the fundamental and specification of DAC that is used throughout this thesis. Detail theory and circuit implementation will be discussed in Chapter 3. Chapter 4 will focus on the noise analysis in the designed circuit. Chapter 5 will present the simulation results. Finally, chapter 6 will summarize this research, and discuss future work.

CHAPTER 2 D/A CONVERTERS FUNDAMENTAL

The nature of the world is indeed analog. With the ever increasing digital demands, data converters play an important role to bridge these two domains. Nowadays, most computer processing unit performs computation in digital domain, as it is much simpler and more efficient. Figure 2.1 illustrates a modern signal processing system that interface with the real world analog signals [5].

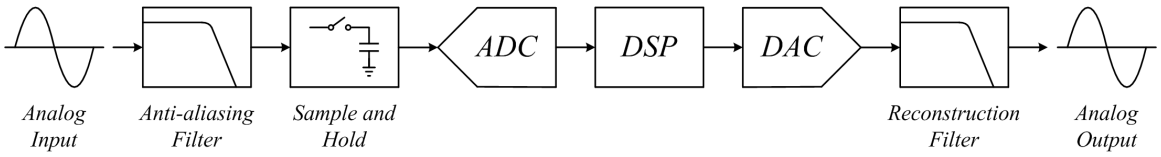


Figure 2.1. Signal processing system

The signal processing chain generally consists of three steps: (1) convert the analog signal to digital form, (2) process the digital signal, and finally (3) convert the processed digital signal back into analog form [6]. The analog input signal is first filtered with a low-pass filter or an anti-aliasing filter to remove any high frequency components that may cause aliasing. Nyquist theorem states that in order to recover the original signal from a sampled signal, the input signal frequency must be less than half of the sampling frequency. Since the amplitude of the input analog signal varies with time, the sampled and hold circuit will provide the following analog-to-digital converter (ADC) with a constant sampled value to allow accurate digital conversion. The ADC further converts the sampled and hold signal to digital data stream, which is discrete in time and

amplitude. Digital data are process through a digital signal processor (DSP), and the resulting digital data are converted back to analog form through a DAC. Normally, the output of the DAC is a sampled and hold signal that is staircase like waveform. To obtain the final analog output that is continuous in time and amplitude, a low-pass filter or a reconstruction filter is used to remove harmonics, images and high frequency components from the sample and hold signal. Due to the scope of this thesis, only the DAC system will be discussed.

2.1 Digital-to-Analog Converter

The DAC input is multi-bit digital signal while its output is an analog signal and normally expressed in either voltage or current quantities. The discussion here will assume the output is a voltage. Consider a *N*-bit DAC as shown in Figure 2.2. The *N*-bit digital input, D_{in}, is express as

$$D_{in} = \frac{b_N}{2^1} + \frac{b_{N-1}}{2^2} + \frac{b_{N-2}}{2^3} + ... + \frac{b_1}{2^N} \tag{2.1}$$

where b_N is defined as the most significant bit (MSB) and b_1 is the least significant bit (LSB). The output quantity, V_{OUT}, can be express as

$$V_{OUT} = V_{REF} \cdot D_{in} \tag{2.2}$$

where V_{REF} is a reference voltage and the number of possible input combinations represented by the input digital word, D_{in}, is equal to 2^N. Each DAC output step is separated by one LSB. The definition of the unit-less quantity, namely, 1 LSB is

$$1 \quad LSB = \frac{1}{2^N} \tag{2.3}$$

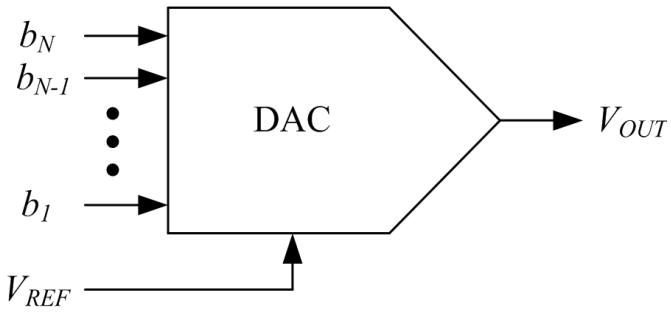


Figure 2.2 Ideal DAC block diagram

The actual voltage change in one LSB step is depending on the reference voltage, and it is defined as

$$V_{LSB} = \frac{V_{REF}}{2^N} \tag{2.4}$$

The input and output transfer characteristic of an ideal 3-bit DAC is showing in Figure 2.3. Note that the maximum output amplitude is not V_{REF}, but rather $V_{REF}\cdot(1-2^{-N})$, which is $V_{REF} - V_{LSB}$ [7].

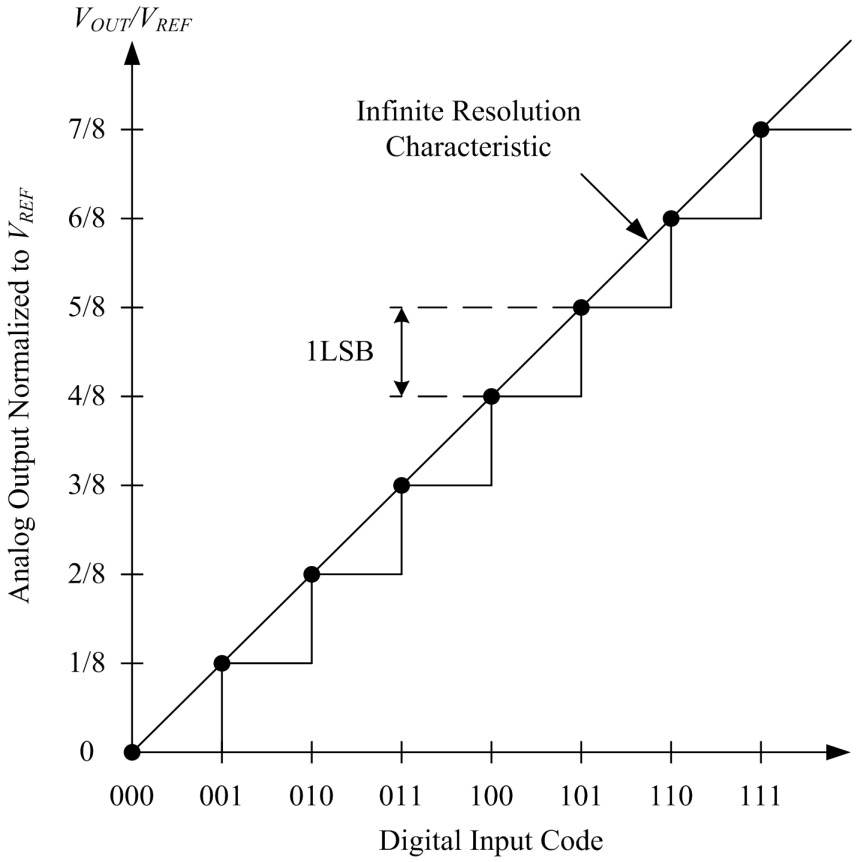


Figure 2.3 Ideal transfer characteristic of a 3-bit DAC

2.2 Quantization Noise

The resolution of the DAC is finite, and one of the most important quantities that limit the maximum achievable SNR is the quantization noise. Quantization noise is the error that introduced during the process of digitizing an analog value; thus, it is the fundamental limit of data converters. To understand this definition, the characteristic of an infinite resolution DAC is plotted on Fig. 2.3. This line represents the limit of the finite resolution DAC characteristic as the number of bits, *N*, approaches infinity. The quantization noise is equal to the analog output of the infinite-bit DAC minus the analog

output of the finite-bit DAC [8]. Fig. 2.4 shows the quantization noise for a 3-bit DAC. The RMS value of the quantization noise can be found by taking the root mean square (RMS) of the quantization noise [7], thus

$$V_{Q(RMS)} = \sqrt{\frac{1}{T}\int_0^T V_Q{}^2 dt} = \frac{V_{LSB}}{\sqrt{12}} \tag{2.5}$$

From equation (2.4) and (2.5), it is clearly shown that the quantization noise will be reduced if the number of bits is increased.

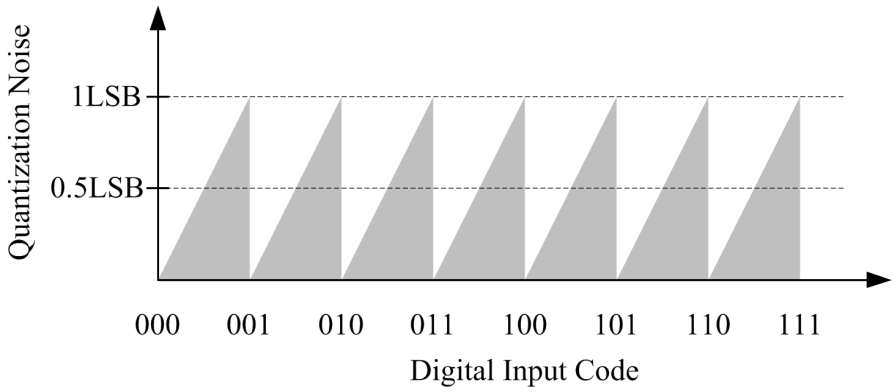


Figure 2.4 Quantization noise of a 3-bit DAC

2.3 Signal to Noise Ratio

The signal to noise ratio (SNR) is probably one of the most important parameters that describes the performance of data converters. The unit of SNR is normally reported in decibel (dB), and it is defined [7] as

$$SNR = 20\log\left(\frac{V_{signal(RMS)}}{V_{noise(RMS)}}\right) \tag{2.6}$$

For a sinusoidal input signal with amplitude from 0 to V_{REF}, its RMS value is

$$V_{input(RMS)} = \frac{V_{REF}}{2\sqrt{2}} \tag{2.7}$$

By substitute equation (2.5) and (2.7) into equation (2.6), the largest possible SNR with a sinusoidal input signal is

$$SNR_{ideal} = 20\log\left(\frac{V_{REF}/(2\sqrt{2})}{V_{LSB}/\sqrt{12}}\right) = 20\log\left(\frac{2^N\sqrt{12}}{2\sqrt{2}}\right) = 6.02N + 1.76 \quad dB \tag{2.8}$$

From equation (2.8), for a 10-bit DAC, the largest achievable SNR is 61.96 dB. Note that the ideal SNR will not only decrease with the number of bit, N, but also with V_{REF} level. For an ADC, V_{REF} is the input signal amplitude where V_{REF} in DAC is the reference voltage. In reality, the measured SNR with a sinusoidal input signal will be less than the ideal SNR. Therefore, the effective number of bits (ENOB) [9] is defined as

$$ENOB = \frac{SNR_{measured} - 1.76}{6.02} \tag{2.9}$$

2.4 Offset

For an ideal DAC, if the input digital code is all zeros, then the corresponding analog output should produce a zero. The offset error is defined to be the output that occurs for the input code that should produce a zero output [7]. The offset will change the transfer characteristic, but typically it remains constant for all input codes. Therefore, it appears as a constant shift in the DAC transfer curve as illustrated in Figure 2.5.

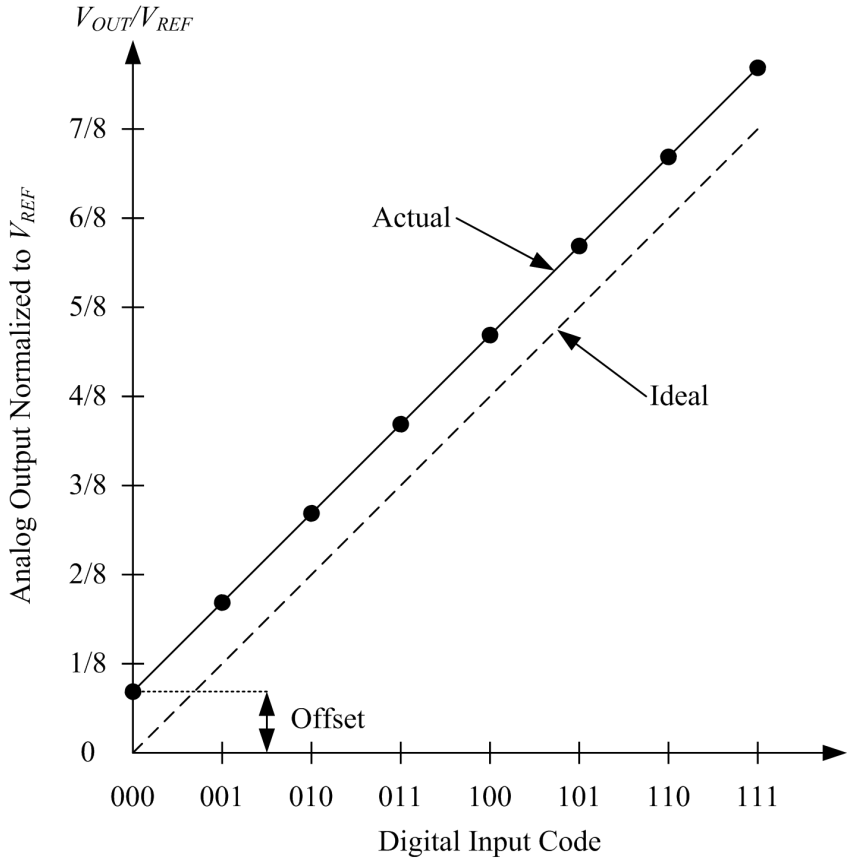


Figure 2.5 Offset error

2.5 Gain Error

The gain error of a D/A converter exists if the slop of the transfer curve is different than the slop of the ideal curve [10]. Normally, the gain error is measured after the offset error has been removed. Unlike offset error, gain error is not constant for all input codes, but rather scaled with a constant ratio. The gain error appears as a change of slope in the DAC transfer curve as shown in Figure 2.6. Neither offset nor gain error will contribute nonlinearity to the system, but if absolute accuracy is required, then the offset and gain error should be made small.

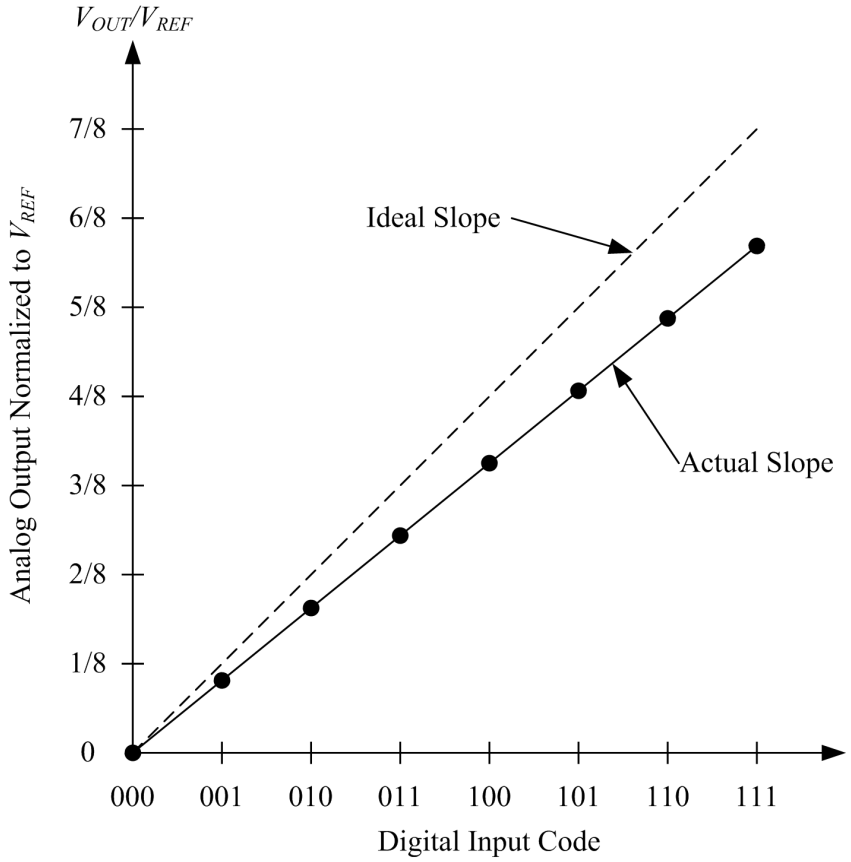


Figure 2.6 Gain error

2.6 Differential Nonlinearity

As seen in Figure 2.3, the ideal DAC output step should be exactly 1LSB between each adjacent output. Non-ideal components can cause the analog increments to differ from its ideal values. The deviation between two adjacent analog outputs from its ideal step values is known as differential nonlinearity (DNL) [10]. Normally, it is after offset and gain errors have been removed. Figure 2.7 illustrates the DNL, note that DNL is only a measure of adjacent step size away from 1 LSB and is independent from the ideal characteristic. This can be seen from code 010 to 011. The maximum DNL occurs from

code 001 to 010 which is +1LSB. Typically, DNL is referred as the maximum magnitude of the DNL values in unit of LSB. Generally, the DAC should have less than ±0.5 LSB of DNL if it is to be N-bit accurate [10].

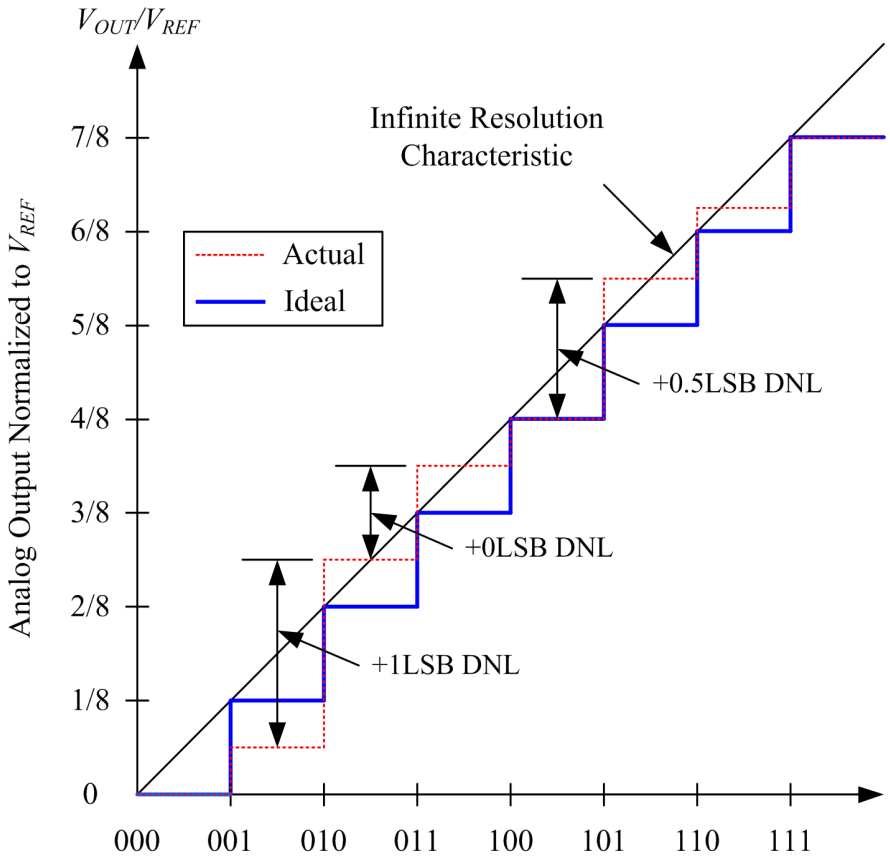


Figure 2.7 DNL illustration of a 3-bit DAC

2.7 Integral Nonlinearity

The integral nonlinearity (INL) is defined as the difference between the data converter transfer curve and the ideal straight line. Another more common definition of INL is the deviation of transfer curve from the endpoint fit line with offset and gain error removed.

This method is illustrated in Figure 2.8. The INL reported is the maximum INL values for all input codes. Normally, INL is a measure in LSB. A large INL means large deviation of transfer curve from the ideal straight line. Therefore, it results in more harmonic distortion [9].

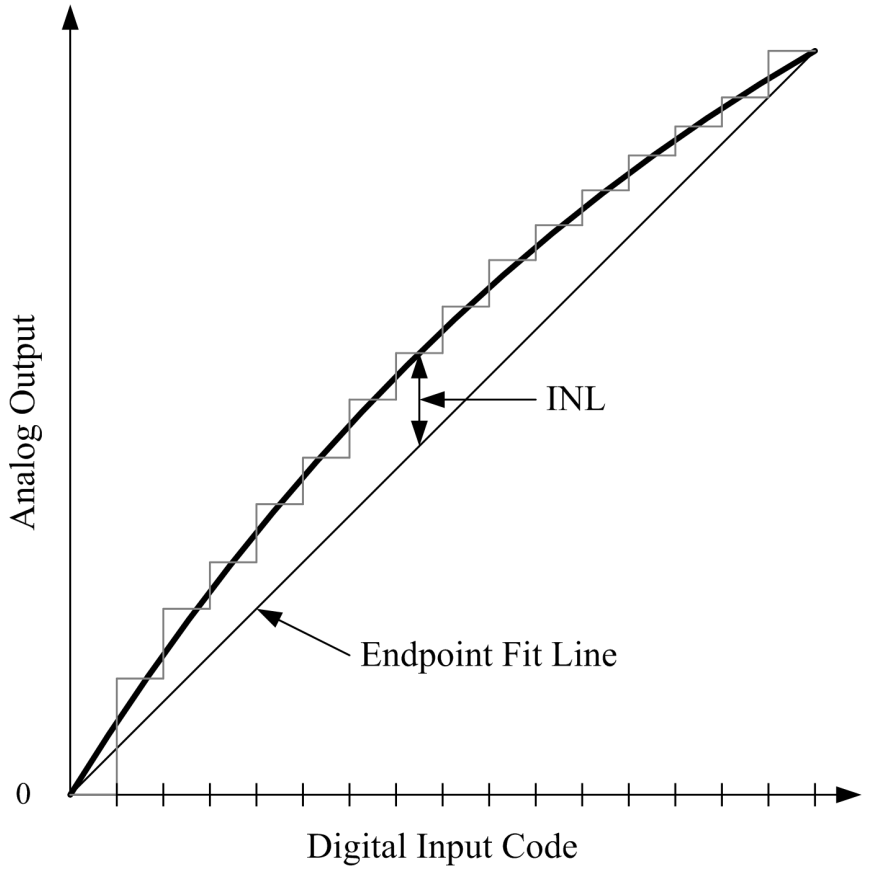


Figure 2.8 Integral nonlinearity using endpoint fit line

2.8 Spurious Free Dynamic Range

A spur is a non-signal spectral component that present in the frequency spectrum as spike like component. It is typically caused by harmonic and intermodulation distortion [11].

Spurious free dynamic range (SFDR) is defined as the difference in dB between the signal amplitude and the largest spur spectral component in the first Nyquist zone. Figure 2.9 illustrated an example of SFDR.

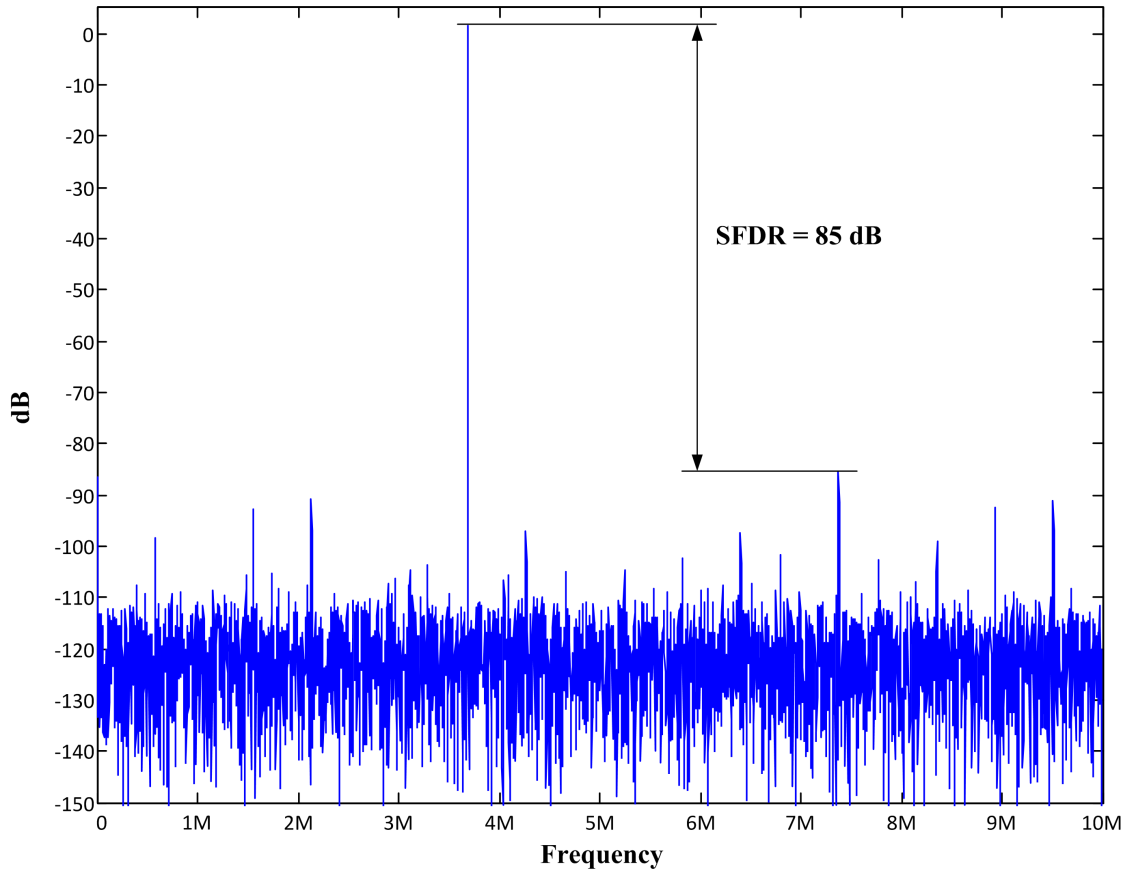


Figure 2.9 Spurious free dynamic range

2.9 Coding Scheme

Digital codes can be represented in many different ways, and certainly the most popular format is binary code. Other common coding schemes include offset binary, gray code and thermometer code. Table 2.1 shows an example of 3-bit binary code representation

with the corresponding thermometer code. Clearly, thermometer code is not the most efficient way to represent a digital code. It takes 2^N-1 digital bits to represent 2^N different digital values, where binary code only requires N digital bits. Despite the inefficiency of representing the digital code, thermometer coding generally offer better linearity [7]. Therefore, it is often used in data converter circuit design.

Table 2.1 Binary vs. Thermometer code representation

Decimal	Binary			Thermometer						
	B_3	B_2	B_1	T_7	T_6	T_5	T_4	T_3	T_2	T_1
0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	1
2	0	1	0	0	0	0	0	0	1	1
3	0	1	1	0	0	0	0	1	1	1
4	1	0	0	0	0	0	1	1	1	1
5	1	0	1	0	0	1	1	1	1	1
6	1	1	0	0	1	1	1	1	1	1
7	1	1	1	1	1	1	1	1	1	1

CHAPTER 3 CIRCUIT DESIGN

Detailed theory and design of the DAC discussed in chapter 1.2 will be presented in this chapter alone with all the supporting circuitries. The 8-bit binary DAC is implemented using stray-insensitive quasi-passive structure and operates in pipelined fashion. This structure is called quasi-passive because of its conversion process does not require any active components. The 6-bit unary DAC is implemented using conventional structure with dynamic element matching technique to suppress nonlinearity caused by capacitor mismatch. The final output voltage is driven by an op-amp utilized direct charge transfer technique to save power dissipation.

3.1 Quasi-Passive Pipelined DAC

The idea of quasi-passive DAC or Q-DAC was originally modified from the serial charge redistribution DAC [12], and later it is first seen in [13], [14]. The Q-DAC consists of MOS switches and all equal value capacitors. A three-phase non-overlapping clock is required to complete the conversion process. The circuit operation is described by using a 4-bit Q-DAC as shown in Figure 3.1. The input of the Q-DAC starts with LSB first and precedes the process toward MSB. Each sampling phase takes 3 clock cycles (Φ_1, Φ_2 and Φ_3), and b^k denotes the input digital word during k^{th} sampling phase. The i^{th} bit of the input digital word during k^{th} sampling phase denotes as b_i^k, and b_1^k is the LSB. Initially during clock phase Φ_1 is high, capacitor C_0 is first discharged to ground, and capacitor C_1 is either charged to V_{REF} if $b_1^k = 1$ or to ground if $b_1^k = 0$. Next during clock phase Φ_2 is

high, the charges in capacitor C_0 and C_1 will redistribute equally and at the same time capacitor C_2 is either charged to V_{REF} if $b_2^k = 1$ or to ground if $b_2^k = 0$. Just at the end of clock phase Φ_2 and before clock phase Φ_3 is high, the voltage across C_0 and C_1 will be $(b_1^k/2)V_{REF}$, and the voltage across C_2 will be $b_2^k V_{REF}$. When clock phase Φ_3 is high, the charges in capacitor C_1 and C_2 will be redistributed while C_3 is charged the same fashion as C_1 and C_2. Next, when clock phase Φ_3 goes low, the voltage across capacitor C_1 and C_2 become $(b_2^k 2^{-1} + b_1^k 2^{-2})V_{REF}$, and capacitor C_3 has voltage of $b_3^k V_{REF}$. Next, at the end of clock phase Φ_1, the voltage across capacitor C_3 and C_4 will be the analog equivalent representation of input digital word, which is $(b_3^k 2^{-1} + b_2^k 2^{-2} + b_1^k 2^{-3})V_{REF}$.

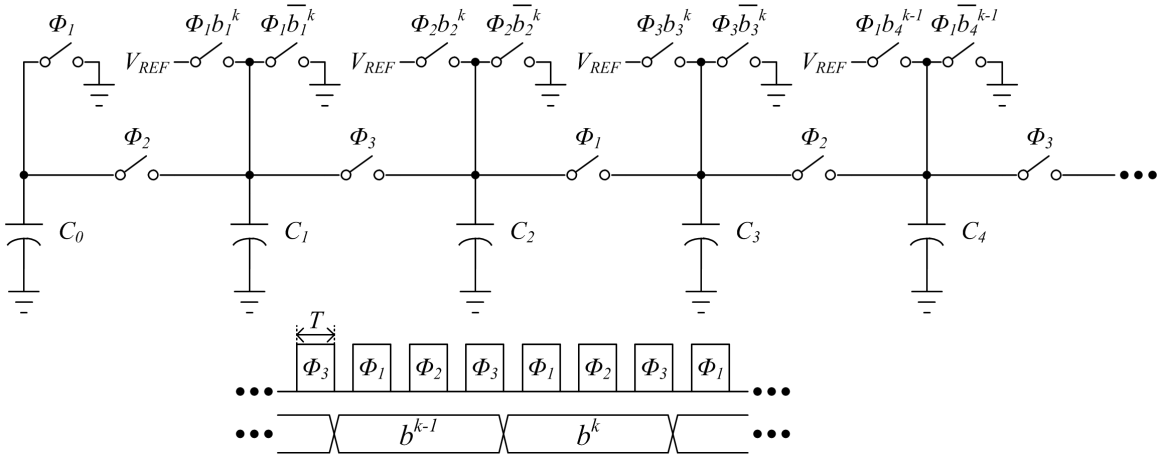


Figure 3.1 4-bit quasi-passive pipelined DAC

The architecture of the Q-DAC is suitable for pipeline operation. Each pipeline stage will process 3-bit segment of a different digital word. Thus, any *N*-bit Q-DAC can be realized by cascading 3-bit Q-DAC sections together followed by either a 2-bit section or a 1-bit section. To provide proper timing for the pipeline operation, shift registers are

used to delay the input digital word. Figure 3.2 shows the block diagram of a 10-bit pipeline Q-DAC by using shift registers. The time between the initial entry of the digital word and the appearance of the corresponding analog output on the last capacitor is equal to (N+2)T delays, where T is the pulse width of the clock phase. The pipeline operation enables the output data to be updated on every sampling cycle. The price paid for the faster operation is the increased digital circuitry and larger capacitor array. Thus, accurate capacitor matching is an important task for achieving higher performance.

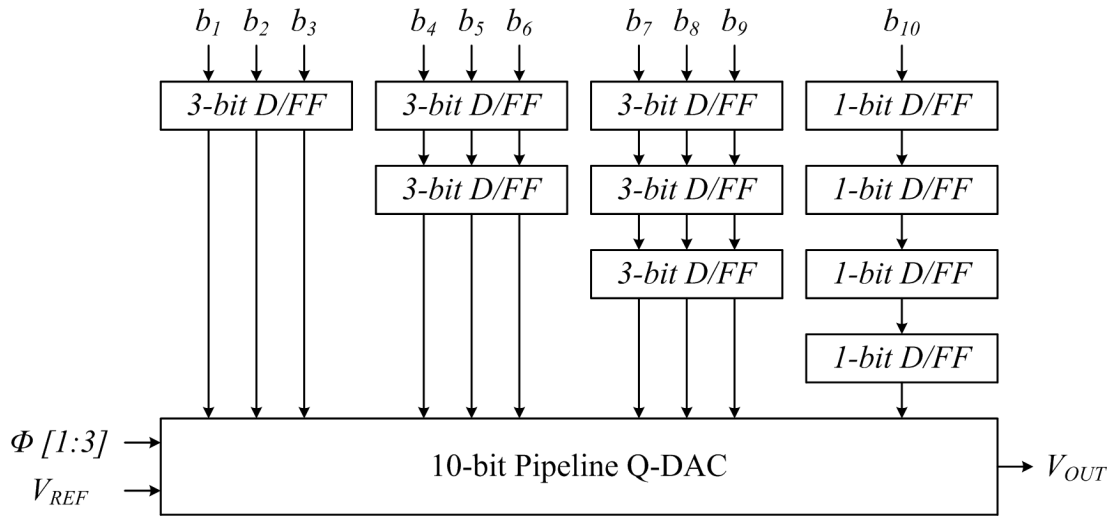


Figure 3.2 Block diagram of 10-bit pipeline Q-DAC

3.1.1 Stray-Insensitive Quasi-Passive Pipelined DAC

The operation of the pipelined Q-DAC is based on the charges stored on the linear capacitors. Thus, the conversion accuracy of the DAC is greatly affected by the presence of any parasitic capacitors. If all the charge redistribution MOS switches in Figure 3.1 are matched, then the gate-to-channel capacitance, C_{gg}, will be the same for every MOS

switches and it only affects the offset and gain error of the transfer characteristic. The junction-to-bulk capacitance, C_j, however is voltage dependent and non-linear. Therefore, it causes nonlinear distortion in the DAC conversion. The parasitic insensitive Q-DAC [15] is achieved by charging the bottom plate of the capacitors during each of the sampling phase, and allows the top plate of the capacitors to participate in the charge redistribution process. The schematic of this converter is shown in Figure 3.3. Its principle operation is similar to original pipelined Q-DAC as discuss in section 3.1.

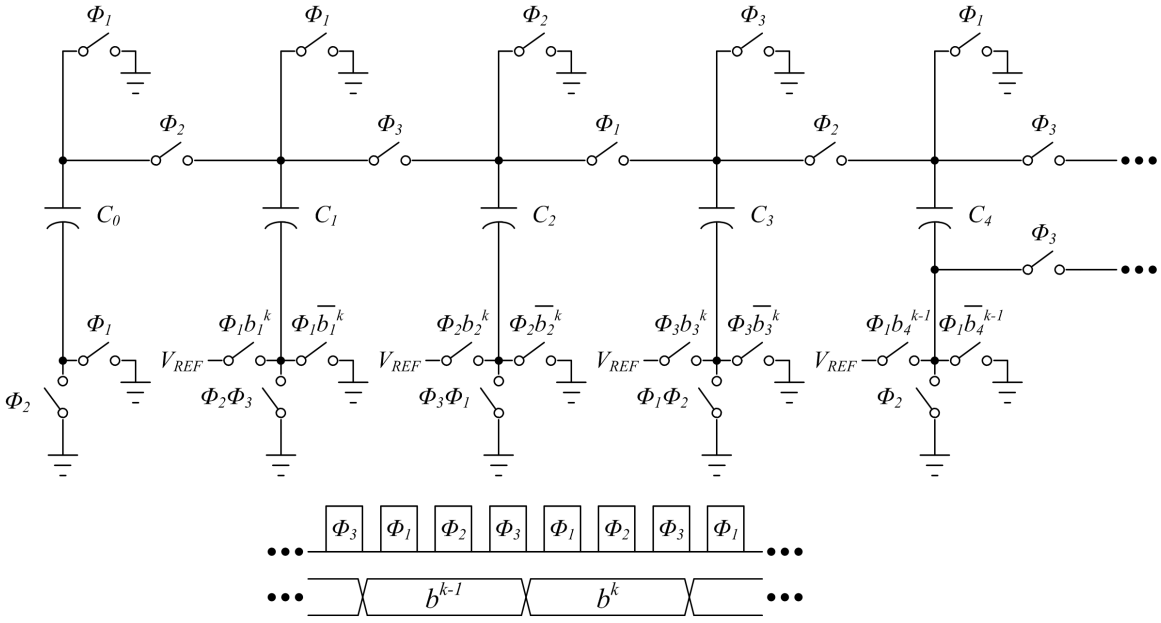


Figure 3.3 Parasitic-insensitive pipelined Q-DAC

Consider a simplest stage of Q-DAC shown in Figure 3.4(a). Sampling capacitors, C_1 and C_2 are sampled during clock phase Φ_1 and Φ_2, where b_1 and b_2 are the input digital code. The charges on the capacitors are redistributed during clock phase Φ_3. To

investigate the behavior of Q-DAC with respect to parasitic capacitance, the parasitic capacitors are labeled with C_{P1} – C_{P4} in Figure 3.4(a). C_{P3} and C_{P4} do not affect the circuit operation as they are always connected to ground. C_{P1} and C_{P2} are the lumped parasitic capacitors at the top plate of C_1 and C_2. They are non-linear as discussed earlier; therefore, it affects the linearity of the DAC. Figure 3.4(b) shows the simplest stage of the parasitic-insensitive Q-DAC. In this case, C_{P1} and C_{P2} are charged to ground during sampling phase, $\boldsymbol{\Phi_1}$ and $\boldsymbol{\Phi_2}$. During $\boldsymbol{\Phi_3}$, the charges on C_{P3} and C_{P4} are discharged to ground while the charges on C_1 and C_2 are shared equally without additional charges from C_{P1} and C_{P2}. Therefore, this configuration can achieve conversion without the effect of parasitic capacitance.

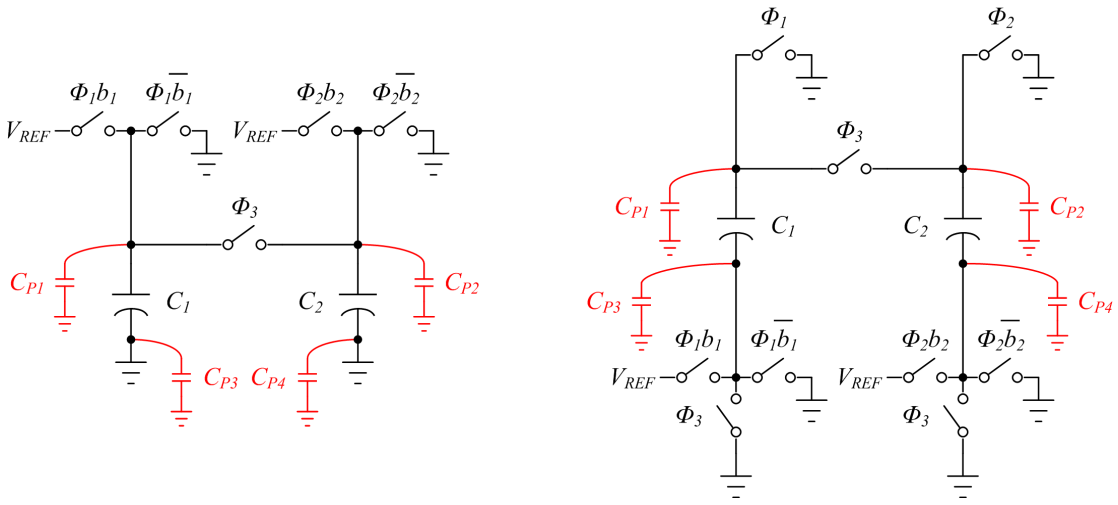


Figure 3.4 Parasitic capacitors in Q-DAC

3.1.2 Design Details

The LSB section of the DAC is binary coded and realized by using stray-insensitive quasi-passive pipelined DAC as discussed in section 3.1.1. Actual circuit implementation is fully differential. The total number of bits for LSB DAC is 8-bit. For simplicity, Figure 3.5 shows the last stage of the fully differential design. During each sampling phase, the sampling switches will either charge or discharge the sampling capacitor to V_{REFP} or V_{REFN}. To reduce the sampling capacitor size, 3.3V supply is chosen for 0.18 μm process, therefore the common mode voltage, V_{COM}, is set to be half of the supply voltage which is 1.65V. The maximum output swing of the DAC is chosen to be $2.4V_{pp}$; thus, V_{REFP} and V_{REFN} are set to be 2.25V and 1.05V.

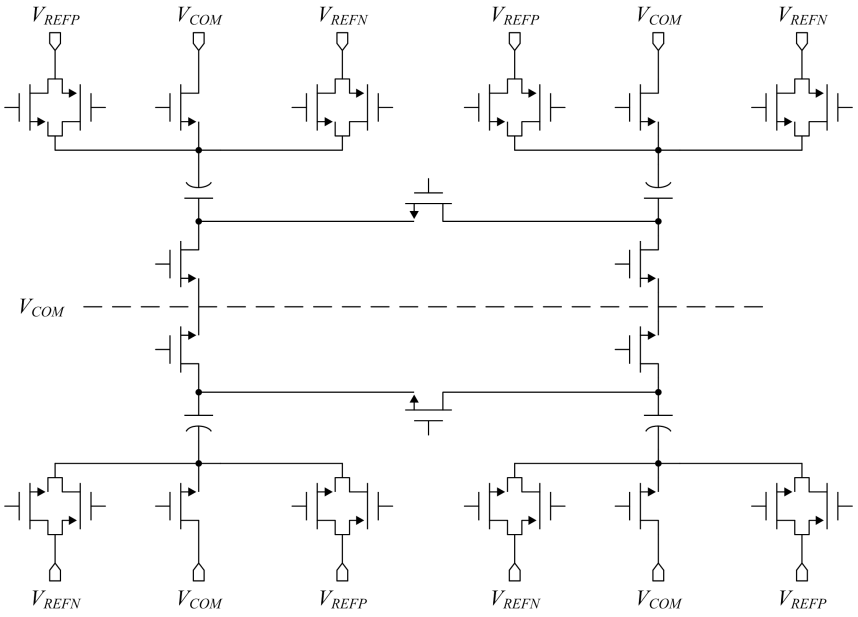


Figure 3.5 One stage of fully differential LSB DAC

The on-resistance of the switches determines the settling behavior of the node voltage. To reduce the switch on-resistance, the sampling switches are realized using transmission gates. The switches connected to V_{COM} are implemented by using single NMOS transistor. To reduce the effect of clock feed through and charge injection, these NMOS transistors connected to V_{COM} are turned off slightly before the sampling clock. This result in a constant charge deposited on the sampling capacitor instead of signal dependent charges. For fully differential circuit, these constant offset will cancel each other out. The charge redistribution switches are also implemented by using single NMOS transistors to reduce the parasitic capacitance on the top plate of the capacitors. The size of sampling capacitor is 200fF, which is selected base on thermal noise estimation. Detailed noise calculation will be discussed in chapter 4. The switch on-resistance requirement can be calculated as

$$R_{on} = \frac{-t}{C \cdot \ln(2^{-N})} \tag{3.1}$$

where t is the allowed sampling time, which is about 15ns, and N is the resolution of settling. In this design, N is set to 16. Therefore, the maximum series resistance of the sampling path should be less than 6.7kΩ.

3.1.3 LSB DAC Layout

The 8-bit differential LSB DAC is laid out symmetrically between positive and negative signal path as shown in Figure 3.6. The sampling switches use inter-digitized layout technique to enhance matching accuracy. Each 200fF sampling capacitor is constructed

using four 50fF poly-poly unit capacitors which are laid out using common-centroid technique. This allows the capacitors to achieve greater matching accuracy and less sensitive to gradient effect.

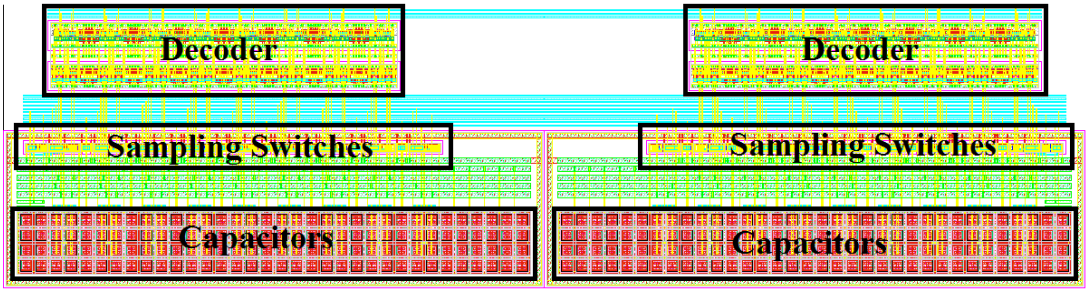


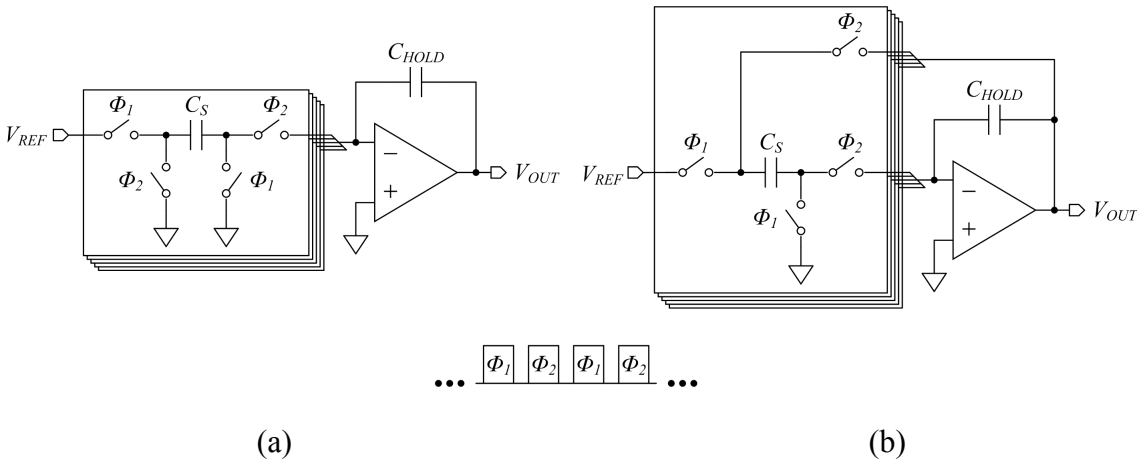
Figure3.6 8-bit LSB DAC layout

3.2 Direct Charge Transfer DAC

The virtual ground enables the charge transferring from capacitor to capacitor possible. Conventional charge transferring DAC is showing in Figure 3.7(a). This circuit operates from charging the sampling capacitor, C_S, to V_{REF} during sampling phase Φ_1, and transfer the charge to the integrating capacitor, C_{HOLD}, during clock phase Φ_2. Note that the op-amp needs to provide charging current during clock phase Φ_2. The capacitor ratio between C_S and C_{HOLD} will determine the gain. The condition $C_S = C_{HOLD}$ results in unity gain. For this scheme, the input and output common mode voltage of the op-amp can have different values; thus, making the design more flexible. Typically, the capacitor size is increased to minimize the kT/C noise and mismatch error, but at the same time, power is increased accordingly [16]. An effective solution to make the power consumption less dependent to capacitor size is to use the direct-charge-transfer (DCT) technique. This

scheme is shown in Figure 3.7(b). For this circuit, the sampling capacitor, C_S, is charged to V_{REF} during clock phase Φ_1, and during clock phase Φ_2, the same sampling capacitor is used as the feedback capacitor. Therefore, the charges are directly deposited to C_{HOLD} without the charging current from the op-amp. The maximum gain for this configuration can only be one, because the same capacitor is used for both input and feedback capacitor. Unlike the charge transfer scheme, the op-amp in DCT stage does not allow different input and output common mode voltages [9]. If parasitic and holding capacitors, C_{HOLD} are neglected, then the feedback factor, β, is one. In the charge transfer scheme, the maximum β will always be less than one. If both C_S and C_{HOLD} are equal, then β = 0.5. Therefore, DCT scheme can achieve lower power dissipation by having lower op-amp unity gain bandwidth requirement. The purpose of capacitor C_{HOLD} in DCT scheme is to prevent the op-amp from running in open loop during sampling phase. However, C_{HOLD} adds a first order low-pass filtering characteristic in addition to the DAC function. The transfer function of DCT stage is

$$H(z) = \frac{C_S}{z(C_S + C_{HOLD}) - C_{HOLD}} \tag{3.2}$$



(a) (b)

Figure 3.7 (a) Charge transferring DAC, (b) Direct-Charge-Transfer DAC

3.2.1 Design Detail

The MSB section of the DAC is thermometer coded and realized by using DCT technique as described in section 3.2. This MSB DAC is controlled by 63 thermometer bits that get decoded from 6-bit binary code. The fully differential implementation is illustrated in Figure 3.8. Since the LSB DAC is 8-bit architecture, the sampling phase will be on clock phase Φ_3. During sampling phase Φ_3, equal valued capacitors C_1 to C_{63} will sample either V_{REFP} or V_{REFN} depending on the input thermometer bits. Next, during charge redistribution phase Φ_1, the sampling capacitor C_1 to C_{63} will be connected in parallel with capacitor C_{HOLD}, and at the same time the charges sampled during Φ_3 will redistribute evenly among these parallel capacitors. As a result, the analog output voltage is generated passively without assistance from the op-amp.

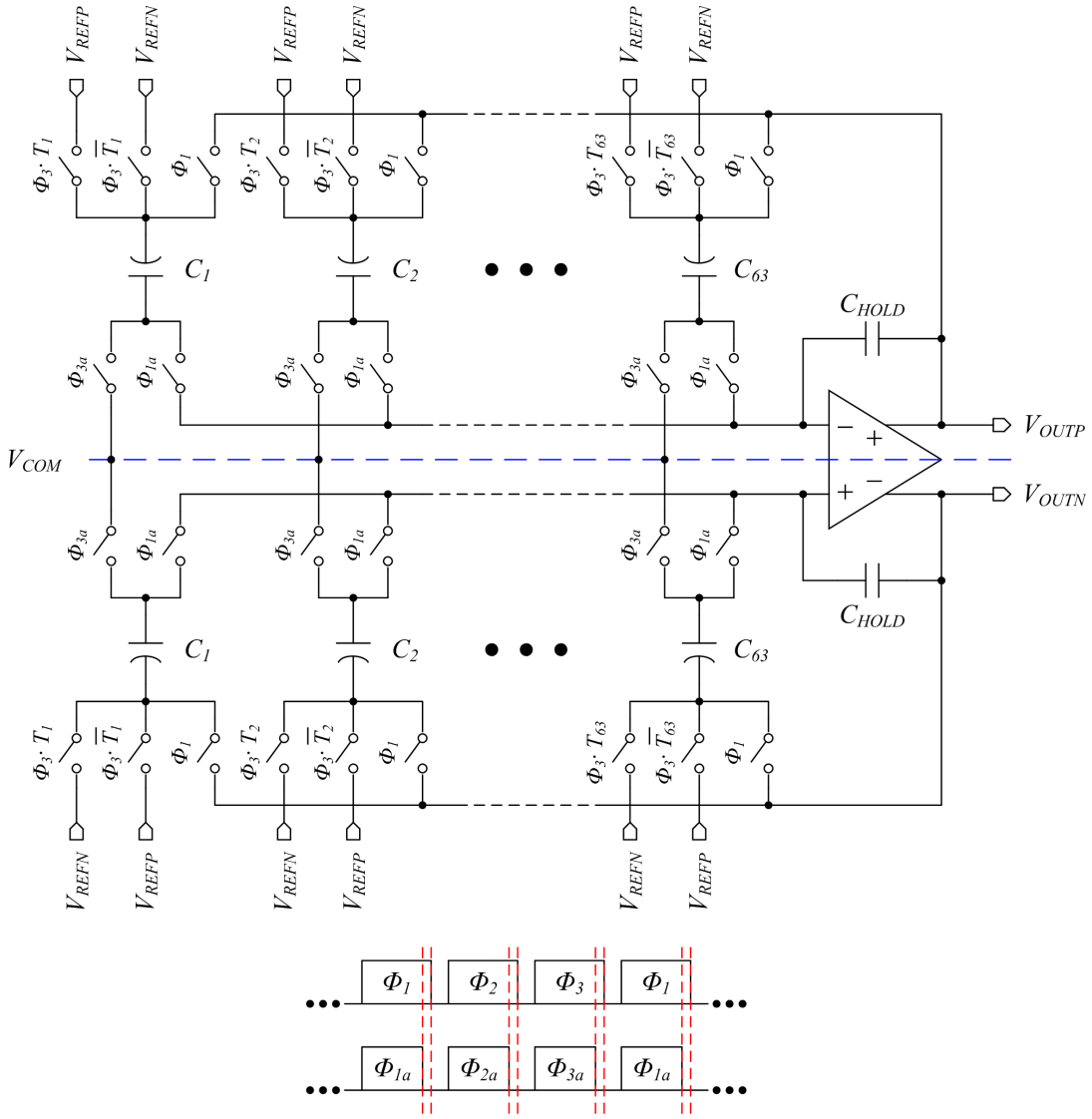


Figure 3.8 Fully differential MSB DAC

The size of each sampling capacitor is 200fF which is the same as the LSB DAC. For simplicity, C_{HOLD} is chosen to be the same as the sampling capacitor. All sampling switches and switches connected to the op-amp outputs are realized by using transmission gates and its on-resistance must satisfy (3.1). The switches connected to the op-amp inputs and the common mode voltage, V_{COM} are realized by using single NMOS transistor

which is controlled by a slightly advanced clock to reduce clock feed through and charge injection effect. In this design, the total sampling capacitor is equal to 12.8pF (64 × 200fF) where the one extra capacitor is coming from the last stage of the LSB DAC. Figure 3.9 plots the frequency response of equation (3.2). Note that because of low-pass filtering effect, signal at higher frequency will experience slightly amplitude reduction.

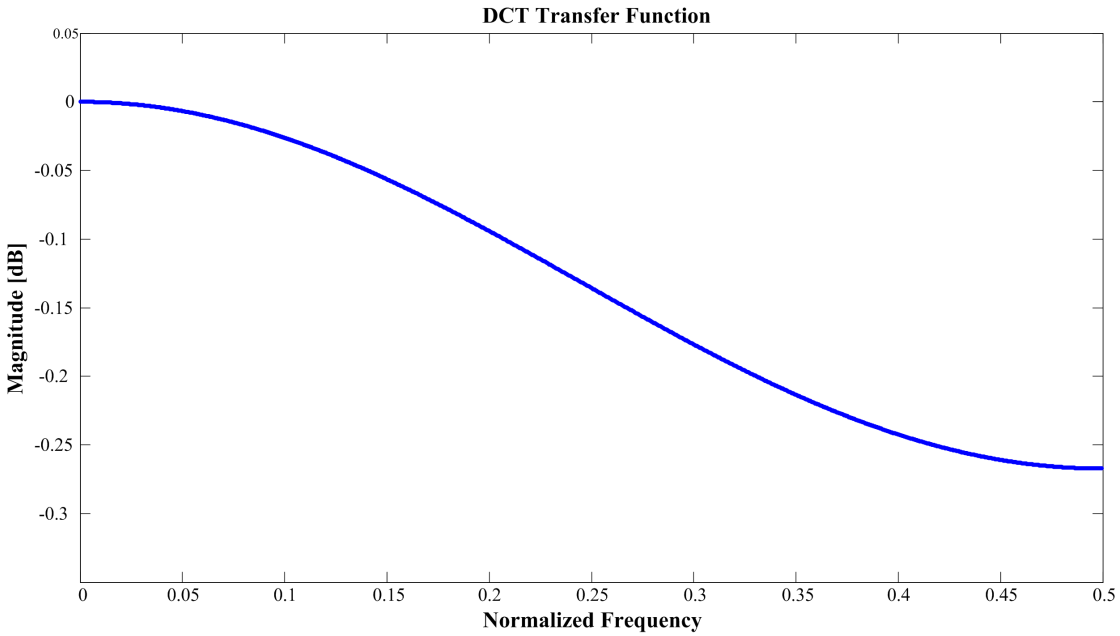


Figure 3.9 DCT frequency response

3.2.2 MSB DAC Layout

The 6-bit MSB DAC is laid out as shown in Figure 3.10. The positive and negative signal paths are each split into two sections to achieve rectangular layout shape. The switches control signals are routed in the middle. Both switches and capacitors are laid out the same way as the LSB DAC.

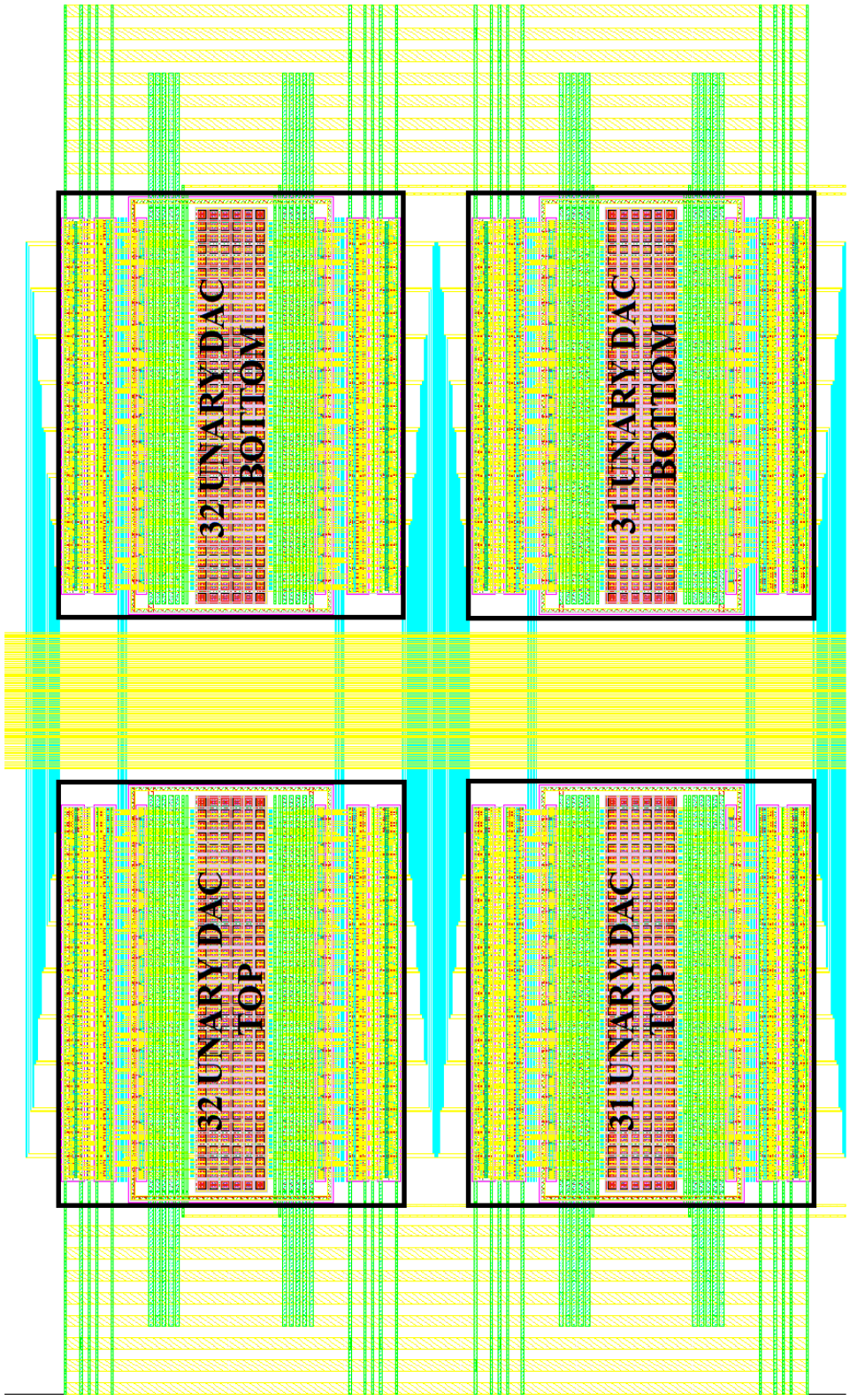


Figure3.10 6-bit MSB DAC layout

3.2.2 Op-amp Design

The fully differential operational amplifier (op-amp) is used as the DCT DAC output driver. Figure 3.11 shows a gain-boosted folded-cascode op-amp that is both capable of supporting large output swing and large DC gain at 3.3V supply. There are several reasons that this architecture was chosen. (1) It accommodates wide input common mode voltages. (2) The op-amp is self-compensated that provides good phase margin for fast close-loop response and (3) class-A output stage deliverers low distortion operation. The PMOS input device is used to minimize the device size of M_5 and M_6. Thus, the op-amp bandwidth can be increased because of the parasitic capacitance at the folding nodes (if NMOS input devices are used) are reduced. The main folded-cascode op-amp can provide adequate gain where the auxiliary amplifier, AUXP and AUXN are added to further boost the DC gain.

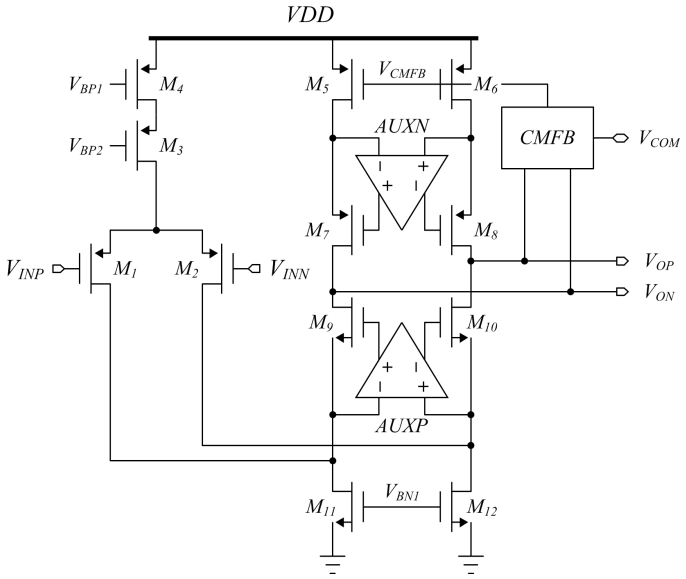
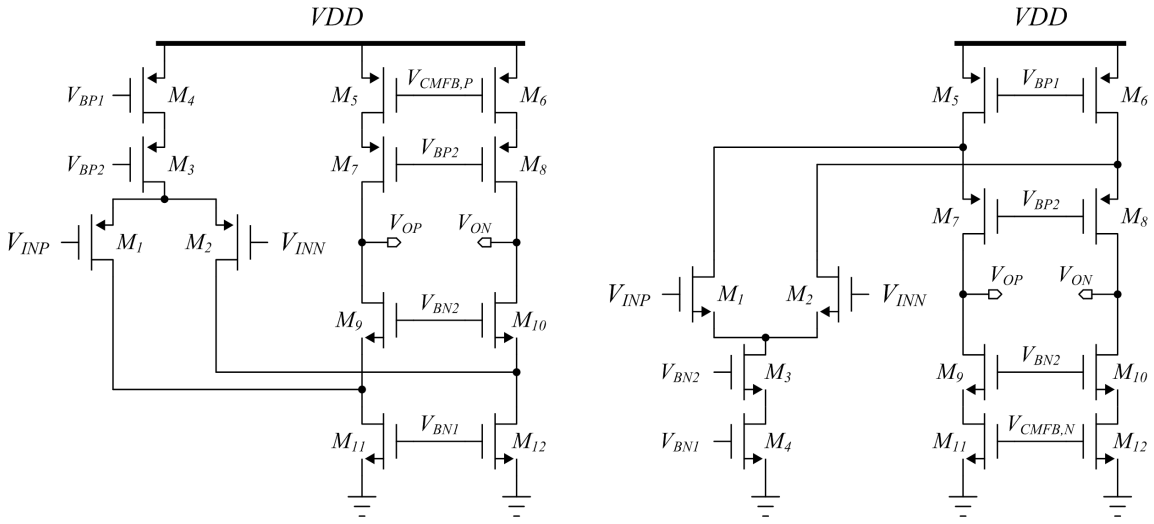


Figure 3.11 Gain-boosted folded-cascode op-amp

Figure 3.12 shows the implementation of the auxiliary amplifiers. To share the bias circuit design, both auxiliary amplifiers are the scaled down version of the main amplifier. Amplifier AUXP uses PMOS input devices to accommodate for lower input common mode voltage, where amplifier AUXN uses NMOS input devices for higher input common mode voltage.



(a) AUXP (b) AUXN

Figure 3.12 Auxiliary amplifiers

All three op-amps in Figure 3.11 are fully differential; hence, common-mode feedback (CMFB) circuit is needed to set all the op-amp output common-mode voltages. Since the Q-DAC implementation is a sampled data system and large output swing is desired, switched-capacitor CMFB is the ideal candidate for all three op-amps. The circuit implementation is shown in Figure 3.13. Capacitor pair C_1 are equal value and formed as voltage divider. A common-mode control bias voltage, V_{CMFB}, is generated

based on the average differential output voltages, V_{OP} and V_{ON}. The DC voltage across C_1 is determined by the switched-capacitor pair C_2, which are charged between the desired common mode voltage, V_{COM}, and a fixed bias voltage, V_{BIAS}, and subsequently put in parallel with capacitor pair C_1. The negative feedback forces the op-amp output common-mode voltage to become the desired common-mode level.

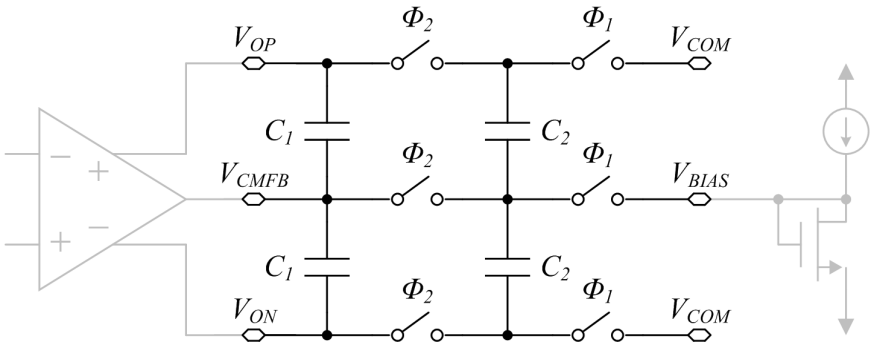


Figure 3.13 Switched-Capacitor common-mode feedback circuit

High swing current mirror bias circuit is shown in Figure 3.14. The referent current is generated by an external resistor, which is not shown in this figure. All NMOS devices are designed to be the same size to improve matching accuracy, and all PMOS devices are designed in the same way.

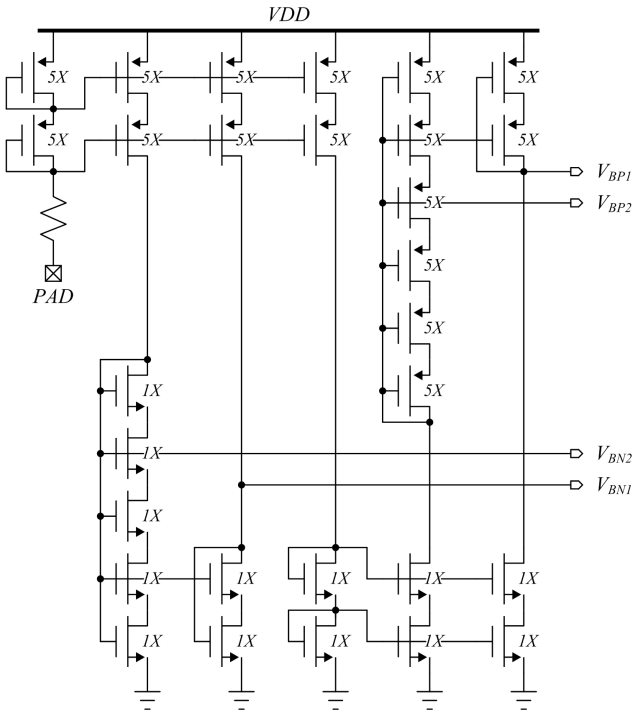


Figure 3.14 Op-amp bias circuit

The op-amp being the last stage of the DAC; therefore, its performance directly affects the conversion accuracy. To determine the op-amp design specification, static (ε_s) and dynamic (ε_d) settling error are set to be less than 0.5 LSB. For design simplicity, static and dynamic settling error each takes 50 percent of the allowable error. The static error is illustrated in Figure 3.15 and it is defined as

$$\varepsilon_s = \frac{V_{step} - V_{out}(\infty)}{V_{step}} \tag{3.1}$$

The op-amp close loop response has transfer function shown in equation (3.2), where β is the op-amp feedback factor, and A_0 is the op-amp DC gain.

$$\frac{V_{out}}{V_{in}} = \frac{A_0}{1 + \beta \cdot A_0} \tag{3.2}$$

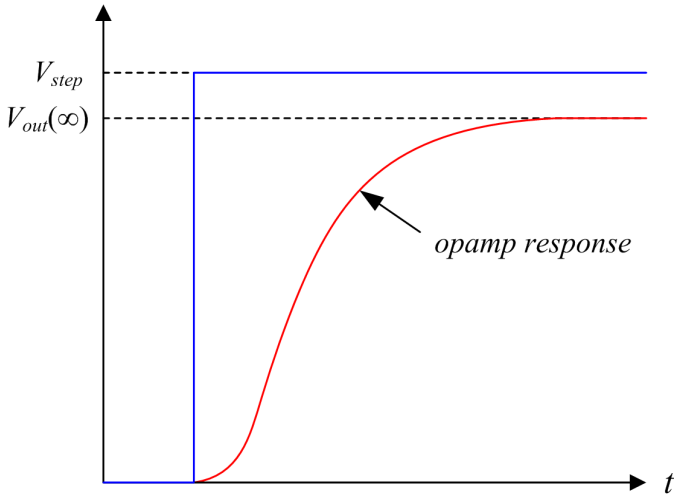


Figure 3.15 Static error illustration

If the DC gain is infinite, then the close loop gain from equation (3.2) will become $1/\beta$, and the static error can be written as a function of β and A_0.

$$\varepsilon_s = \frac{1/\beta - \dfrac{A_0}{1+\beta \cdot A_0}}{1/\beta} = \frac{1}{1+\beta \cdot A_0} \tag{3.3}$$

The DC gain therefore has to satisfy this condition

$$A_0 > \frac{1-\varepsilon_s}{\beta \cdot \varepsilon_s} \tag{3.4}$$

For 14-bit DAC, the static error is $1/2^{16}$, and the feedback factor, $\beta = 1$ for DCT, hence the minimum required DC gain is

$$A_0 > 96.3 \text{ dB} \tag{3.5}$$

The op-amp output is loaded with a capacitive load, and it requires some time before the exponential of the voltage across the output capacitor to reach its final voltage. The deviation from the ideal value to the settled value is defined as dynamic settling error.

$$\varepsilon_d = \frac{V_{out}(\infty) - V_{out}(t = t_s)}{V_{out}(\infty)} \tag{3.6}$$

The close-loop time domain step response is given as

$$V_{out}(t) = \frac{A_0}{1 + \beta \cdot A_0}(1 - e^{\frac{-t_s}{\tau}}) \tag{3.7}$$

where t_s is the maximum time allowed for settling and τ is the time constant. For first order system, the close-loop bandwidth is β multiplied by the unity gain bandwidth (UGB), thus the −3dB time constant is

$$\tau = \frac{1}{2\pi \cdot \beta \cdot UGB} \tag{3.8}$$

The dynamic settling error is the exponential term in equation (3.7) which is

$$\varepsilon_d = e^{\frac{-t_s}{\tau}} \tag{3.9}$$

By substitute the −3dB time constant, τ, from equation (3.8) into (3.9) gives

$$\varepsilon_d = e^{-t_s \cdot 2\pi \cdot \beta \cdot UGB} \tag{3.10}$$

Thus, minimum UGB requirement is

$$UGB > \frac{1}{t_s \cdot 2\pi \cdot \beta} \ln(\frac{1}{\varepsilon_d}) \tag{3.11}$$

During each conversion window, part of the duration is allocated for slewing and the remaining portion is dedicated for small signal settling. Figure 3.16 illustrates a diagram for the op-amp settling time allocation. The total time, T_{total} is equal to T_{slew} + T_{settle}. The op-amp output is assumed to drive 15pF capacitor, C_L, which includes capacitance of bonding pad and off chip components. The output common-mode voltage is set to be at

1.65V with upper and lower reference voltage at 2.25V and 1.05V respectively. The slew current is calculated as

$$I_{slew} = C_L \cdot \frac{dV}{dt} = C_L \cdot \frac{dV}{T_{slew}} = C_L \cdot \frac{dV}{(T_s - T_{settle})} \tag{3.12}$$

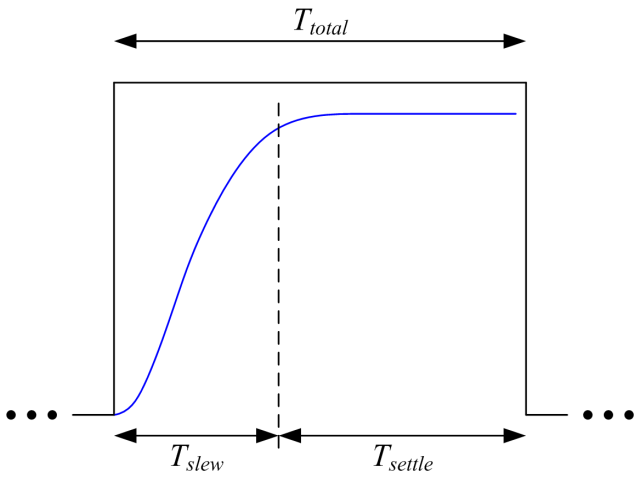


Figure 3.16 Op-amp slewing and settling time allocation

To achieve 0.25LSB or 16-bit small signal settling, T_{settle} is set to be k times time constant, where time constant, τ, is equal to

$$\tau = \frac{T_{settle}}{k} = \frac{1}{\omega_{3dB,closeloop}} \tag{3.13}$$

The UGB for fist order system is g_m/C_L, where g_m is the transconductance of the input device which is

$$g_m = \frac{2 \cdot I_D}{V_{ov}} \tag{3.14}$$

where V_{ov} is the over drive voltage. Therefore, the close-loop bandwidth is

$$\omega_{3dB,closeloop} = \frac{\beta \cdot g_m}{C_L} = \frac{\beta \cdot \frac{I_{settle}}{V_{ov}}}{C_L} \tag{3.15}$$

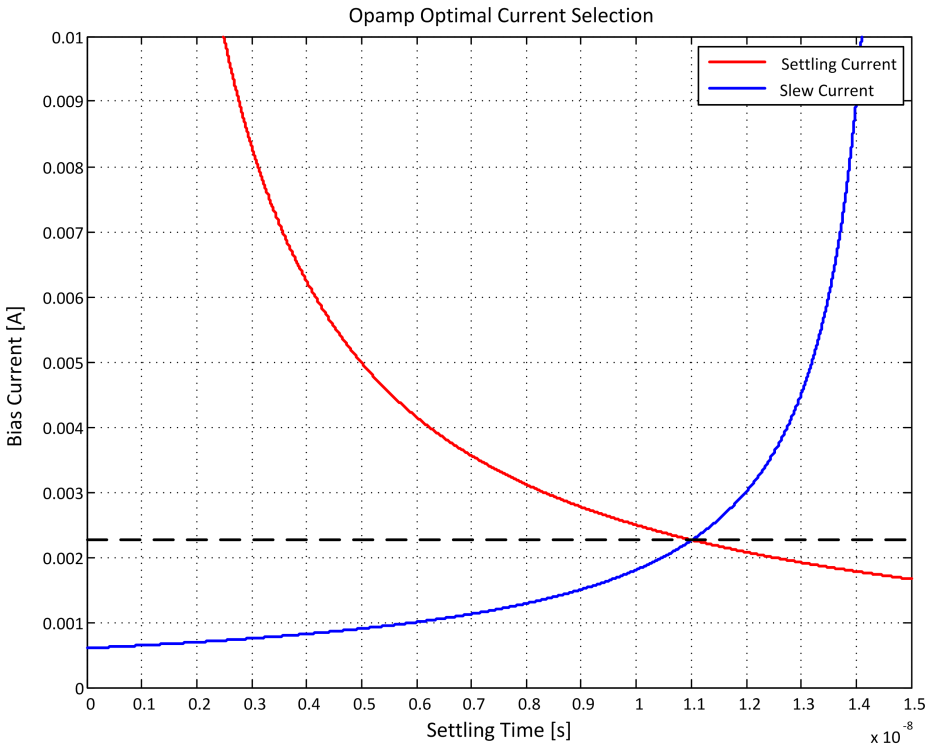


Figure 3.17 Optimal op-amp bias current selection

By substitute equation (3.13) into (3.15), the settling current, I_{settle} is found to be

$$I_{settle} = \frac{k \cdot V_{ov} \cdot C_L}{\beta \cdot T_{settle}} \tag{3.16}$$

Figure 3.17 plots I_{slew} and I_{settle} vs. T_{settle} from equation (3.12) and (3.16) where the optimum bias current is the crossover point. The over drive voltage, V_{ov}, in equation (3.16) is set to 0.15V. To achieve 16-bit settling, $k = \ln(2^{16}) = 11.1$. The maximum voltage step,

dV, in equation (3.12) is ($V_{REF} - V_{COM}$) = 0.6V. To guarantee design, 4mA of bias current is chosen. From this figure, T_{settle} is about 11ns, and the UGB can be calculated from equation (3.11). Therefore, the minimum UGB requirement must be

$$\text{UGB} > 160 \text{ MHz} \tag{3.17}$$

3.2.3 Op-amp Layout

The op-amp layout is shown in Figure 3.18. Each op-amp layout utilized inter-digitized technique to achieve higher matching between transistors. The auxiliary amplifiers, AUXN and AUXP, are placed on top of the main amplifier. The CMFB circuits are placed on the top area to avoid clock signals to interfere with the op-amp signals. The bias circuit is placed on the bottom, and the resulting bias voltages are distributed along the sides.

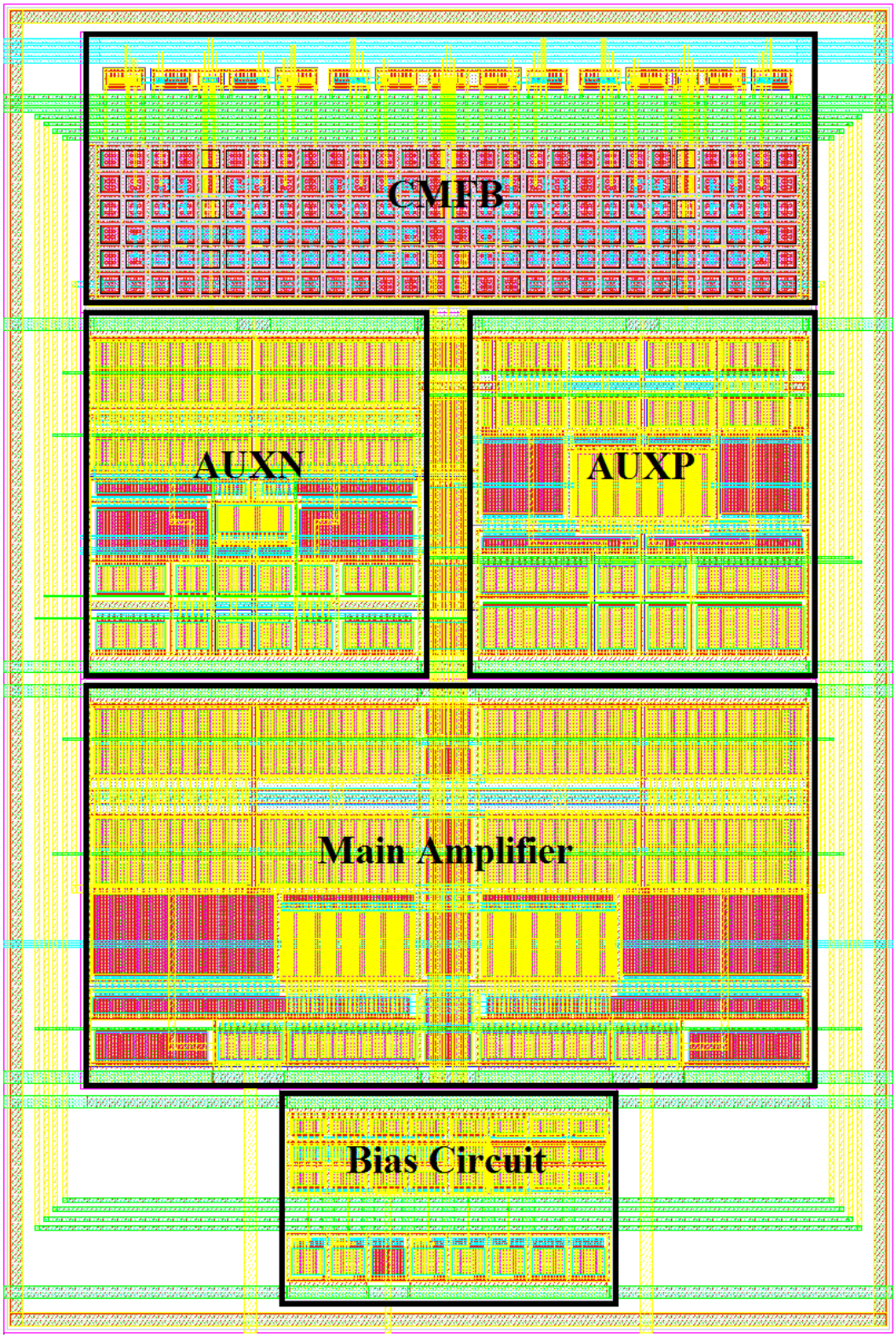


Figure 3.18 Gain-boosted folded-cascode op-amp layout

3.3 Decoding Logic

The DAC core circuit is designed by using 3.3V supply. In order to save power consumption, the digital supporting circuitry is designed to use 1.8V supply. To properly control the 3.3V devices, logic level converters are inserted in between two voltage domains. Figure 3.19 shows the detailed implementation of the sampling switch control logic. Transmission gates are inserted in between NMOS control signal path to duplicate the inverter delay in the PMOS control signal path. The logic level converts are inserted right before the sampling switches.

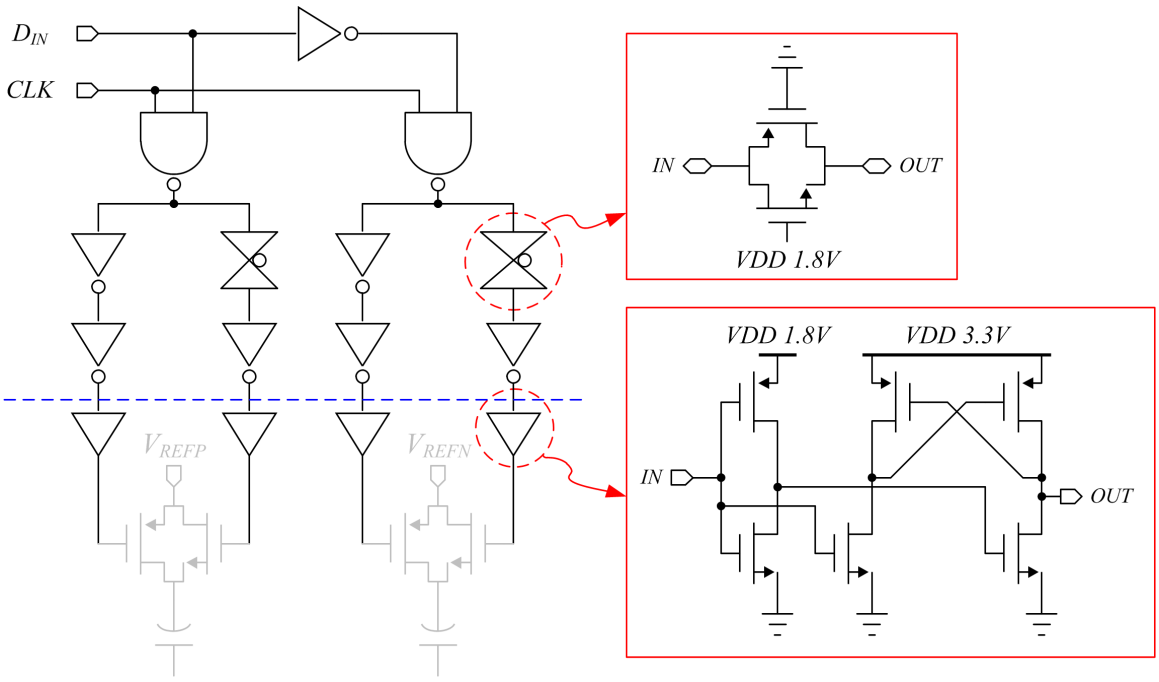


Figure 3.19 Sampling switch control logic

3.4 Clock Generator

The clock generator circuit is designed to provide three-phase non-overlapping clocks. Figure 3.20 shows the three-phase clock generator circuit. An input 60MHz master clock, MCLK, is used to generate three 20MHz clock outputs, P_1, P_2 and P_3. Note that each clock edge is overlapping with its adjacent clock. In order to provide some non-overlapping time between each clock phase, a SR-latch based clock generator shown in Figure 3.21 is used to achieve this. For simplicity only one set of the clock generator is shown here, actual circuit implementation requires 3 sets of figure 3.21. Inverter digital delay cells labeled with D1 are inserted to adjust the advanced clock falling edge, and D2 delay cells are inserted to adjust the non-overlapping time width between each adjacent clock phase. The implementation of the digital delay cell is shown Figure 3.22. The amount of delays is adjusted by using off-chip variable resistor.

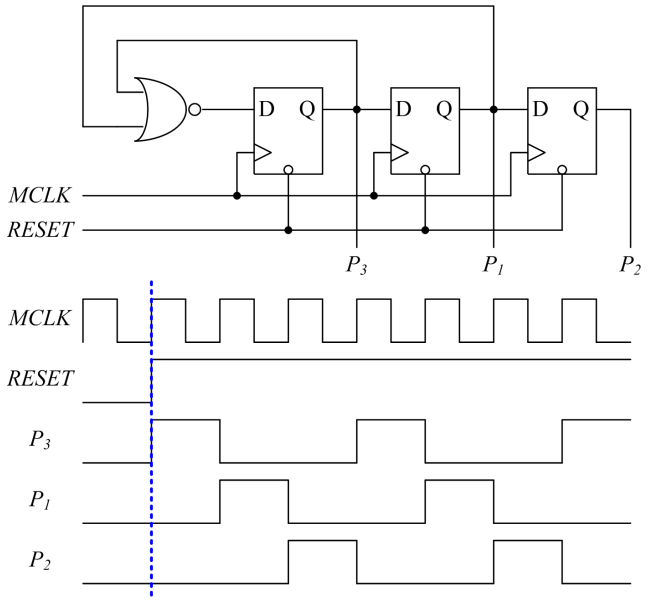


Figure 3.20 Three-phase clock generator

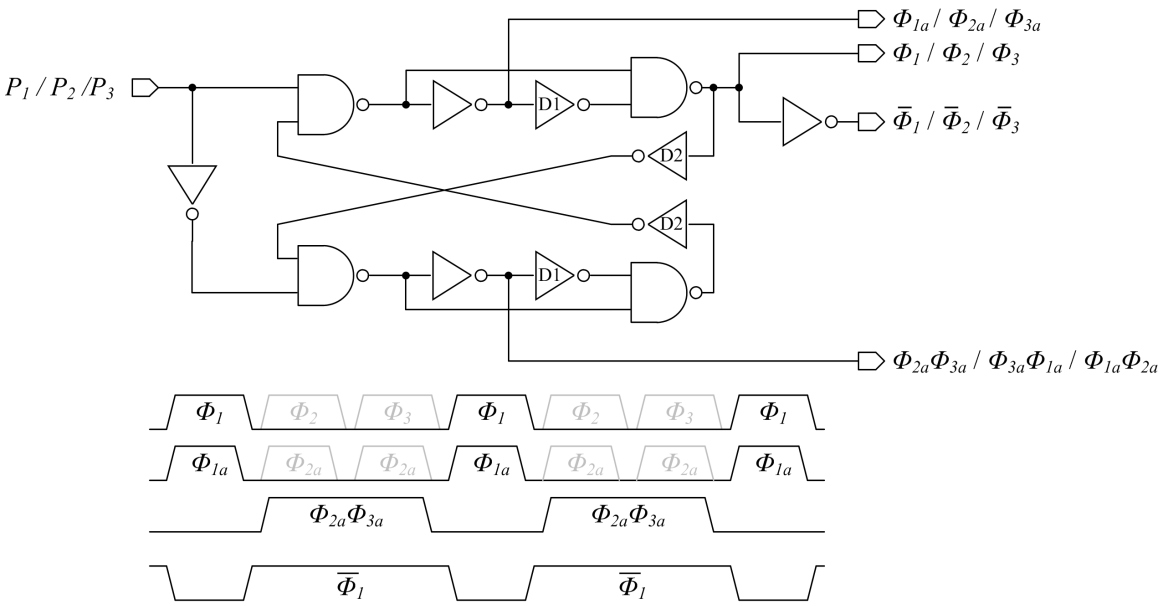


Figure 3.21 Non-overlapping clock generation

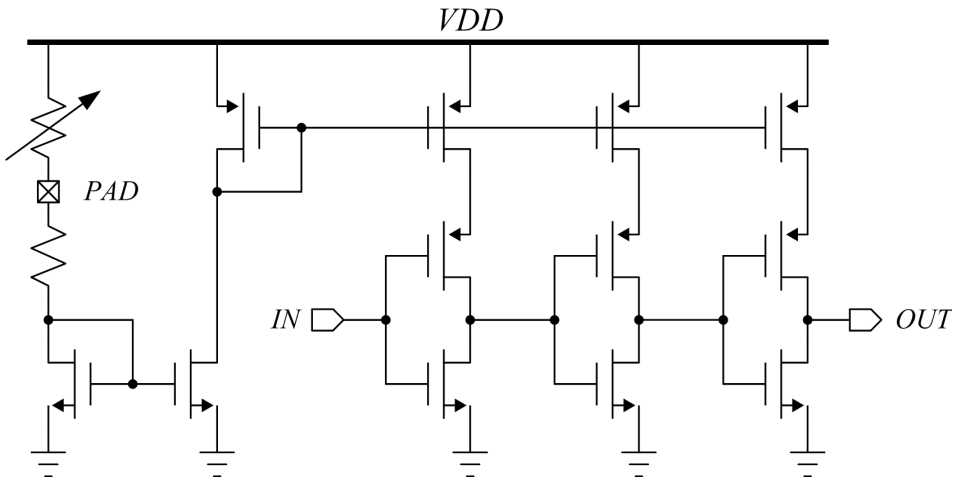


Figure 3.22 Delay cell

3.5 Dynamic Element Matching

In most data converters, the conversion accuracy is limited by the matching accuracy of the nominally equal size elements such as, resistors or capacitors. The mismatches among these nominally identical elements are inevitably created during circuit fabrication, which leads to harmonic distortion. Dynamic element matching (DEM) technique has enabled major performance improvements in high resolution Nyquist-rate and oversampling delta-sigma data converters. By scrambling the usage pattern of the unit elements, DEM causes the mismatch error to be pseudo-random noise that is uncorrelated with the input sequence. Therefore, the noise power is uniformly spread over the entire Nyquist interval [17]. Generally, there are two types of DEM, (1) mismatch-shaping [18], [19], [20] and (2) mismatch-scrambling. In mismatch-shaping, the error generated by the mismatch is moved outside of signal band, thus the in band noise spectral energy is reduced. This technique will only be effective if the signal band occupies a small portion of the Nyquist range, thus it is normally used in oversampling application such as delta-sigma data converters. In mismatch-scrambling, the noise is white; thus, it is more commonly used in Nyquist-rate applications. In this design, the mismatch-scrambling technique will be used. Figure 3.23 shows the block diagram of the implemented DEM. The input binary code is first decoded into thermometer code, and then the logarithmic shifter is used to shift the thermometer bits according to the address selection block.

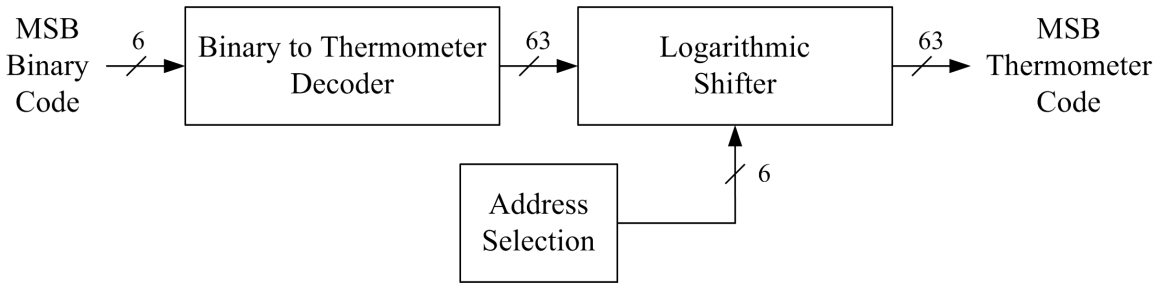


Figure 3.23 DEM block diagram

3.5.1 Binary to Thermometer Decoder

A 6-bit binary to thermometer decoder is used to decode the MSB portion of the segmented DAC. The two-step binary to thermometer decoder [21] is chosen because it is fast and hardware efficient. Figure 3.24 shows the block diagram of the two-step decoder. It consists of a row decoder, a column decoder, and 63 decoding cells. Each decoding cell in the matrix represents one individual thermometer bit. The blue shaded region indicates the thermometer bits are selected. Detail circuit implementation is shown in Figure 3.25.

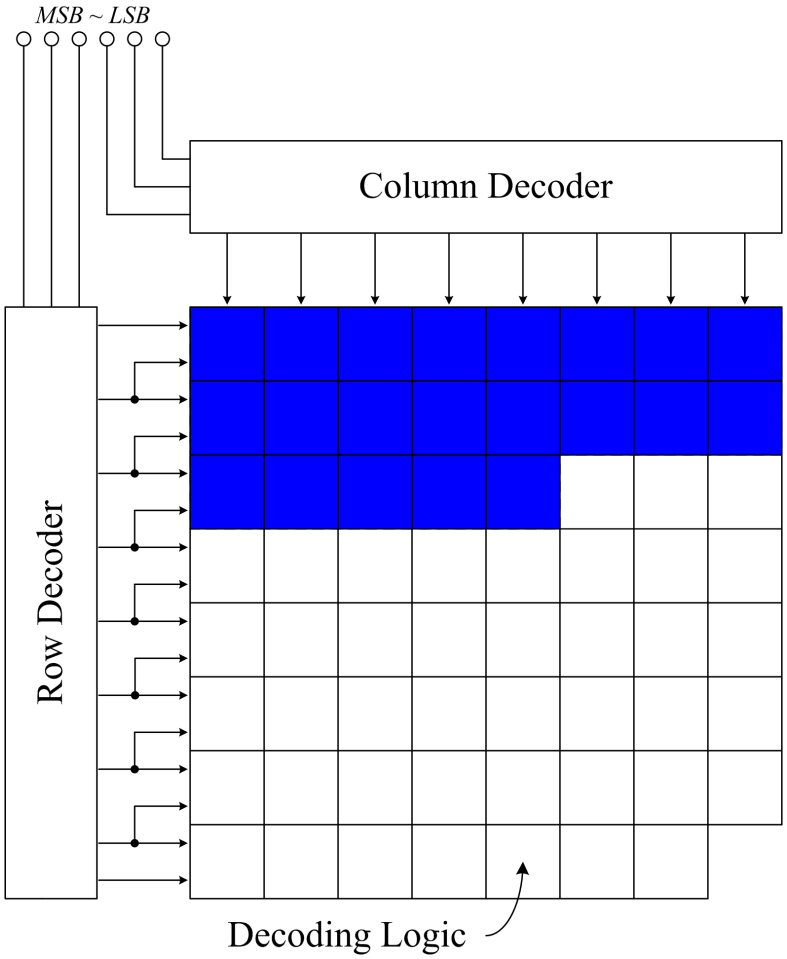


Figure 3.24 Two-step decoder block diagram

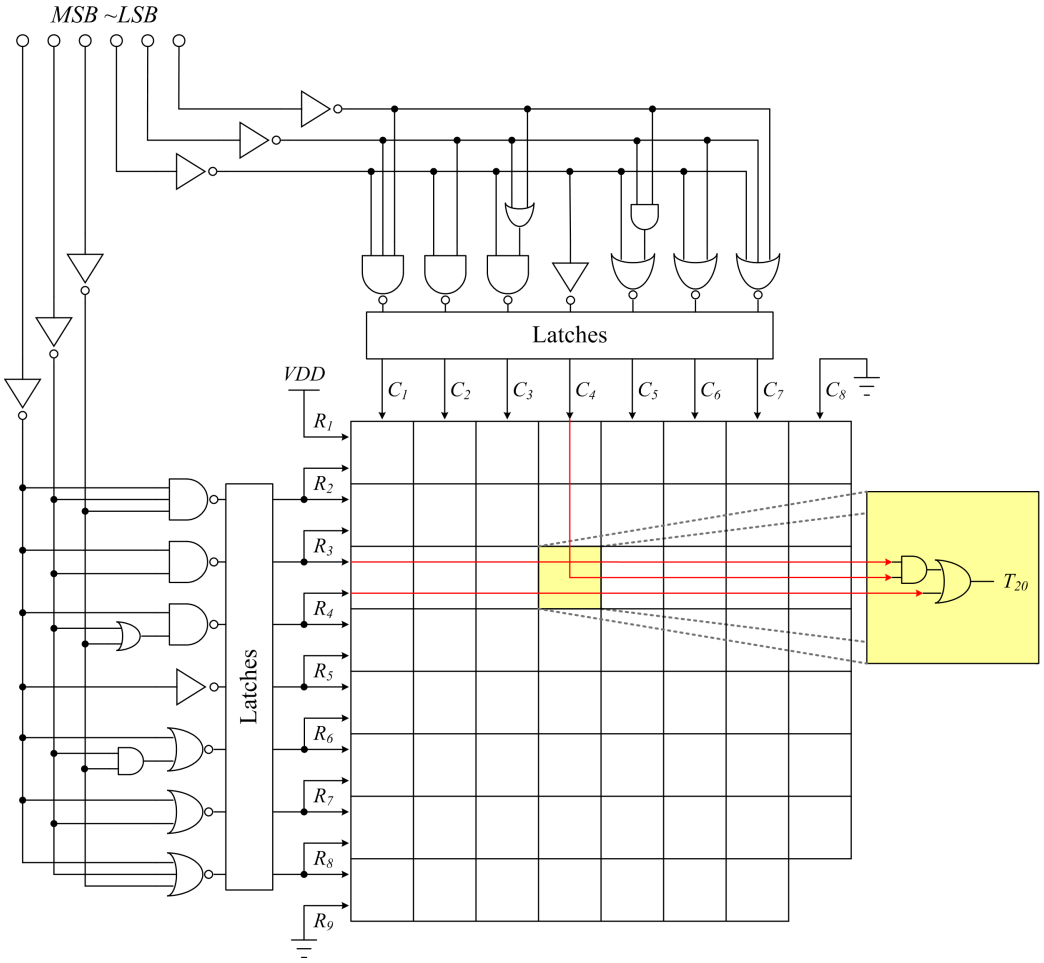


Figure 3.25 Two-step decoder circuits

The operation of the decoder is carried out in 2 steps. First the binary code is split into two sections, and each section is decoded into intermediate thermometer code by the column and row decoder. In the next step, the intermediate thermometer codes are applied to the decoding matrix to generate final thermometer code. Single stage latches are inserted between the intermediate decoder and the decoding matrix to reduce logic switching glitches. Within the matrix in Figure 3.21, three types of rows can be identified. They are: (1) rows in which all cells are turned ON (indicated on the first 2 rows); (2)

rows in which only some cells are turn ON (indicated on the third row); (3) rows in which all cells are turned OFF (indicated from row 4 to 8). From the above description, the decoding cell will turn ON if all the cells on the next row are all ON, or both the intersected signals from row and column decoder produce a one. From the above descriptions, the decoding logic is realized by the following function

$$T_{ij} = (C_i \cdot R_j) + R_{i+1} \tag{3.18}$$

The layout of the 6-bit binary to thermometer decoder is shown in Figure 3.26. Its output, $T_1 - T_{63}$, will be connected to the input of the logarithmic shifter.

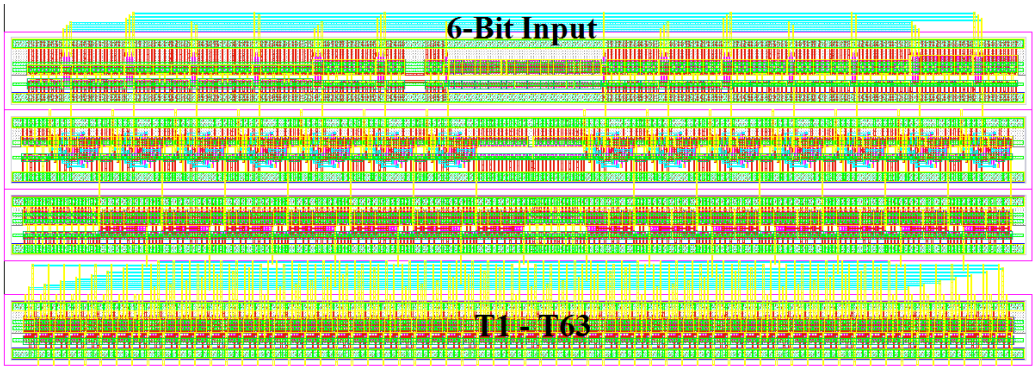


Figure 3.26 6-bit Binary to thermometer decoder layout

3.5.2 Logarithmic Shifter

In order to shift 63 thermometer bits to any locations, a 6-bit logarithmic shifter [22], [23] is implemented to achieve this task. Figure 3.27 shows a 4-bit version of the shifter. The circuit diagram of the actual implementation will take up too much space to illustrate, therefore only 4-bit version is shown here. The individual shifter logic is implemented using a 2 to 1 multiplexer. The layout of this logarithmic shifter is shown in Figure 3.28.

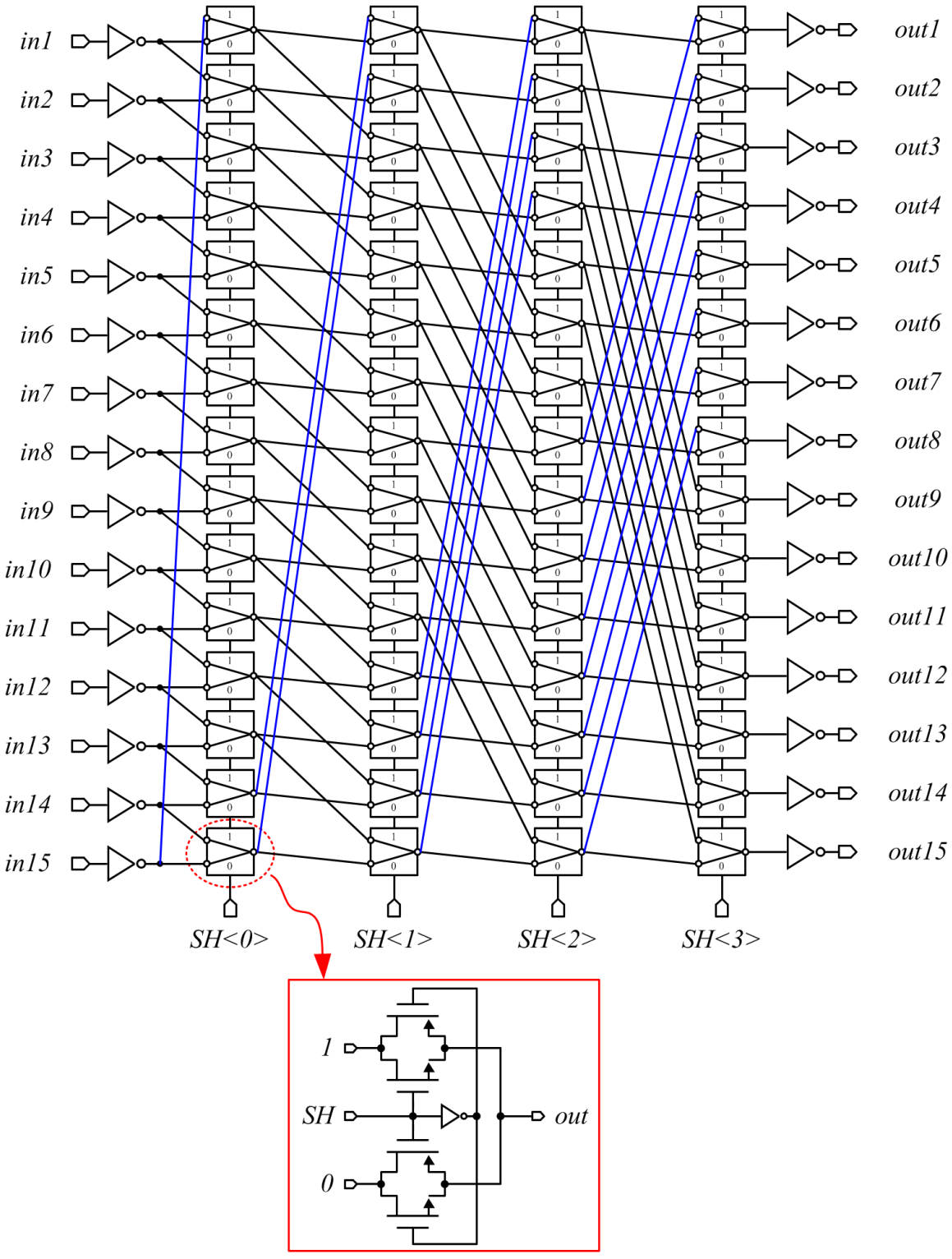


Figure 3.27 4-bit logarithmic shifter

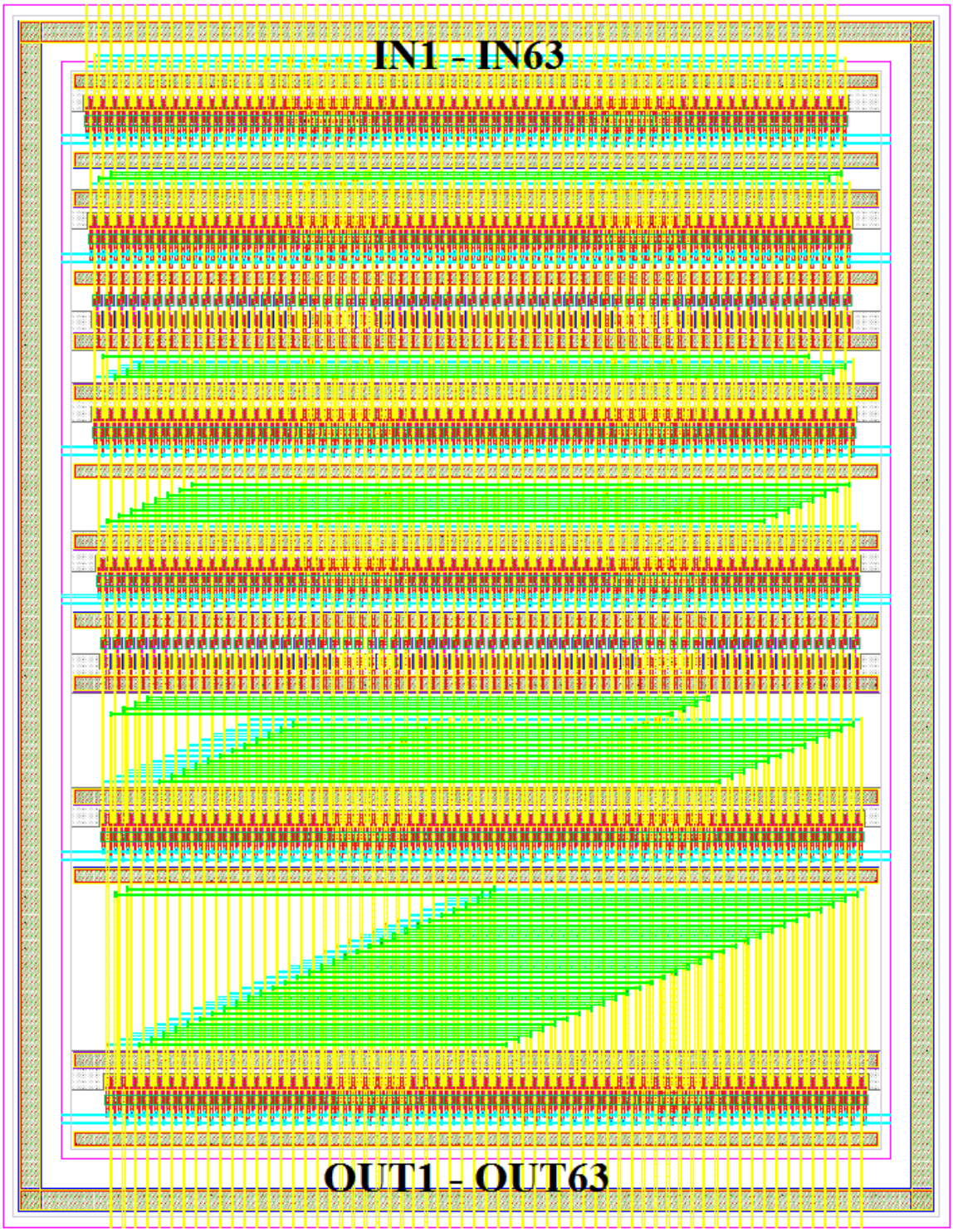


Figure 3.28 6-bit logarithmic shifter layout

3.5.3 DEM Element Selection

The shift address of the logarithmic shifter is provided by a pseudo-random bit generator. Such generator is implemented by using Galois style linear feedback shift register (LFSR) that has feedback polynomial of $x^{16} + x^{14} + x^{13} + x^{11} + 1$. The maximum length of unrepeated sequence is determined by the size of the LFSR, therefore for N registers in LFSR, the maximum sequence is $2^N - 1$. To achieve uncorrelated random bit streams, two LFSRs shown in Figure 3.29 are running in opposite directions, and their outputs are produced by exclusive-or operation [24]. The design implementation uses 16 registers per LFSR to produce the maximum 65535 unrepeated sequence, which is sufficient for the purpose. The output of the LFSR will lock to all zeros if all the register outputs are zero. To prevent this from happening, the additional circuits [25] showing in red are added to initialize the LFSR after reset. The layout of this block is shown in Figure 3.30.

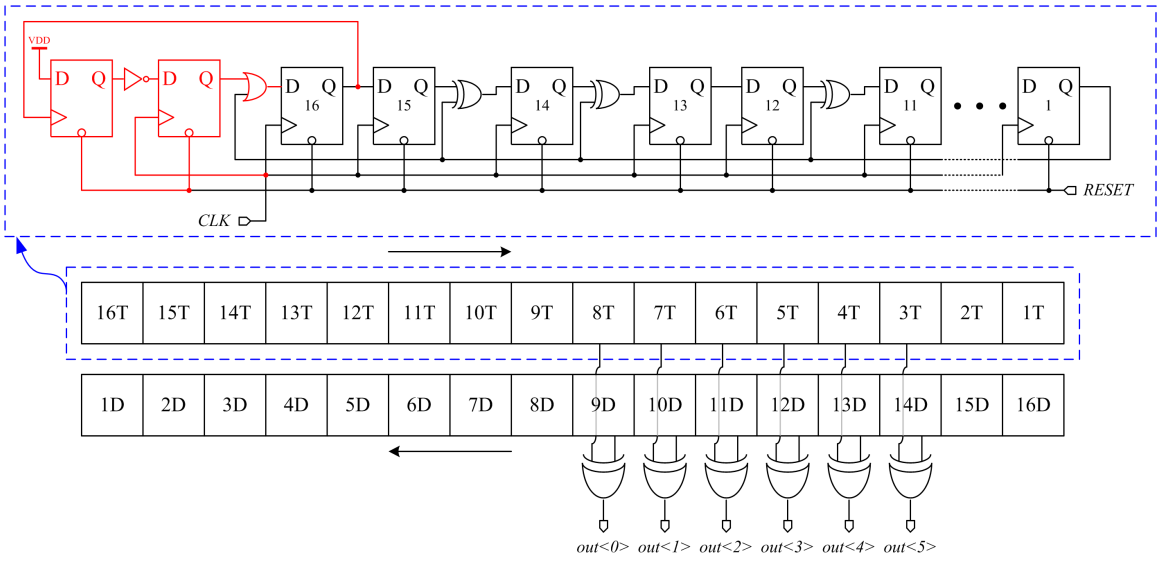


Figure 3.29 Pseudo random bit generator used as address selector

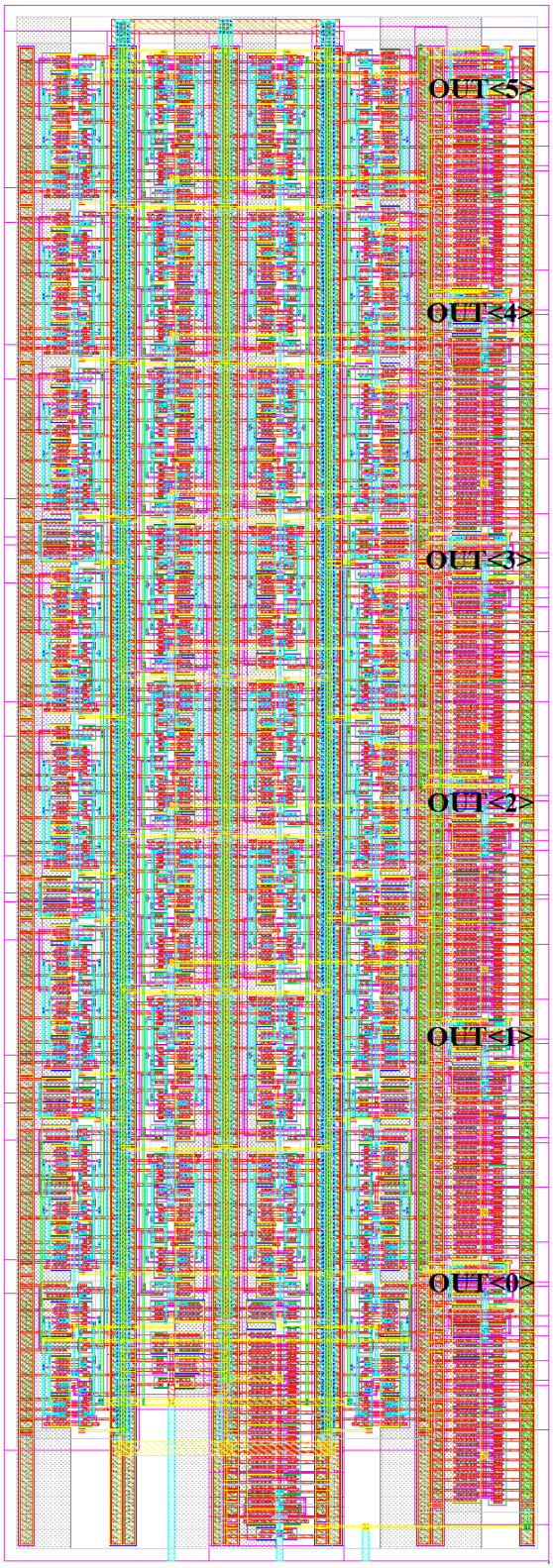


Figure 3.30 Pseudo random bit generator layout

CHAPTER 4 NOISE ANALYSIS

4.1 Thermal Noise

The quantization noise discussed in chapter 2.2 is the fundamental limit of data converters. In any sampled-data system, the thermal noise associated with the sampling switch is unavoidable, and the noise deposited onto the sampling capacitor, C, is known as kT/C noise, where k is the Boltzmann's constant, $k = 1.38 \times 10^{-23}$ J/K and T is the absolute temperature of the device in degree Kelvin. Consider a simple switched-capacitor circuit shown in Figure 4.1. The sampling switch is modeled with its on-resistance, R, and a series thermal noise generator, $V_n^2 = 4kTR$. This RC network formed a low-pass filter, and its transfer function is

$$\frac{V_{out}}{V_n}(s) = \frac{1}{sRC + 1} \tag{4.1}$$

Since low-pass filtering effect, the power spectrum density (PSD) of the noise is 4kTR multiplied by the square of the transfer function [26] of (4.1) which is

$$S_n(f) = 4kTR \frac{1}{4\pi^2 f^2 R^2 C^2 + 1} \tag{4.2}$$

where s in equation (4.1) is $j\omega$, and $\omega = 2\pi f$. The total noise power can be calculated by integrating the shaped PSD from DC to infinite frequency [27].

$$V_{n,out}{}^2 = \int_0^\infty \frac{4kTR}{4\pi f^2 R^2 C^2 + 1} df = \frac{kT}{C} \tag{4.3}$$

From equation (4.3), the kT/C noise will go to zero only if the sampling capacitor is

infinite or the temperature is at zero degree Kelvin. The sampling capacitor size is limited by the *kT/C* noise. Note that the power consumption will increase with the size of the sampling capacitor.

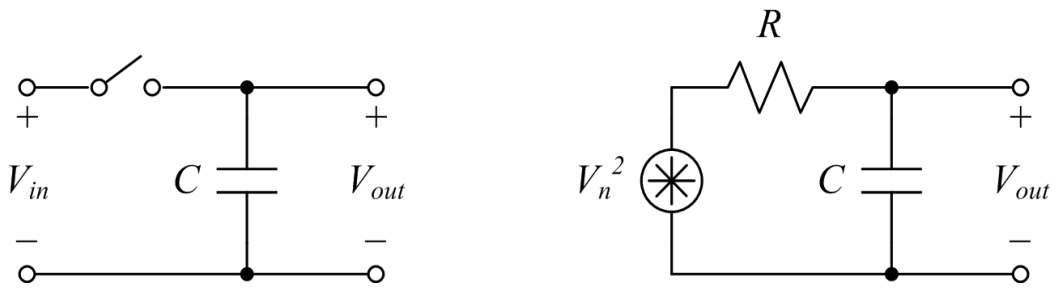


Figure 4.1 Switched-capacitor equivalent noise circuit

4.2 Binary DAC Noise

The stray-insensitive Q-DAC discussed in section 3.1.1 is used here for *kT/C* noise analysis. Figure 4.2 shows the simplest stage of the DAC. At the end of Φ_1, C_1 samples the noise introduced by switch S_1 with noise power equals to kT/C_1. C_2 will also sample the noise introduced by switch S_2 with noise power equals to kT/C_2 at the end of Φ_2. During Φ_3, charges on C_1 and C_2 are redistributed through switch S_3 equally; therefore, the deposited noise power on C_1 and C_2 during Φ_1 and Φ_2 are divided by the gain square where gain is equal to one half. At the end of Φ_3, both C_1 and C_2 sample the noise generated by S_3 with noise power equals to $2kT/C$. The reason coefficient 2 in the numerator is due to C_1 and C_2 are in series during Φ_3. After Φ_3, the noise power generated by switch S_3 will also be divided by the gain square. Since the generated noises are uncorrelated of each other, their noise power adds [26]. The total noise power on capacitor C_2 after sampling and charge redistribution will be

$$V_{n,out}{}^2 = (\frac{kT}{C} + \frac{kT}{C}) / 2^2 + (\frac{2kT}{C}) / 2^2 = \frac{kT}{C} \tag{4.4}$$

From the result shown in equation (4.4), if more stages are added, the total noise power will remain at *kT/C*.

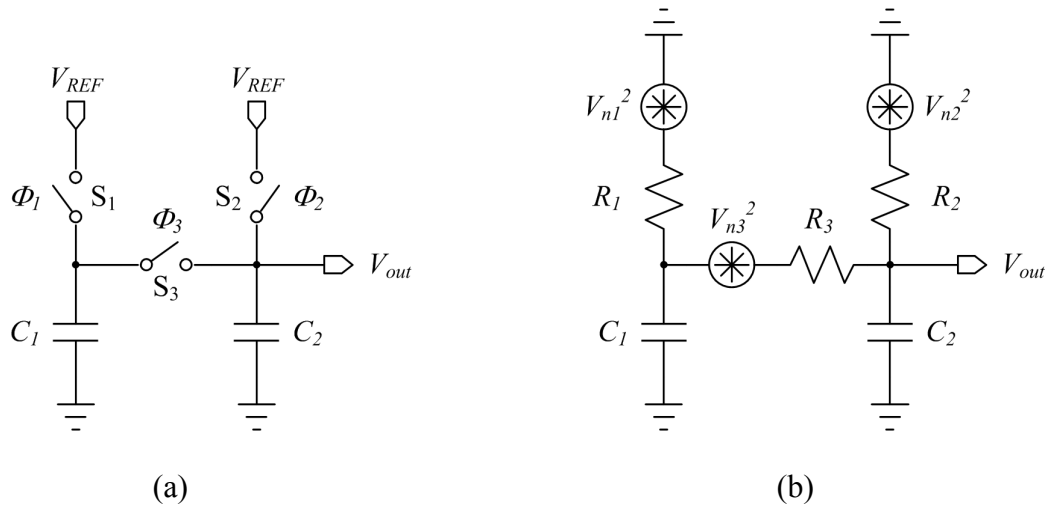


Figure 4.2 LSB DAC noise equivalent circuit

4.3 Op-amp Noise

The op-amp noise is modeled with an input stage of a traditional two-stage op-amp as shown in Figure 4.3. Assume perfect matching between transistor pair M_1, M_2, and pair M_3, M_4. The output noise spectral density (NSD) can be found by adding individual noise contribution from each noise source to the output node. The output noise can be referred back to an equivalent input noise, $V_{n,eq}$ by dividing the output NSD by the gain, $g_{m1}R_o$ [7], which gives

$$V_{n,eq}{}^2(f) = \frac{16kT}{3g_{m1}}\left(1 + \frac{g_{m3}}{g_{m1}}\right) \approx \frac{32kT}{3g_{m1}} \tag{4.5}$$

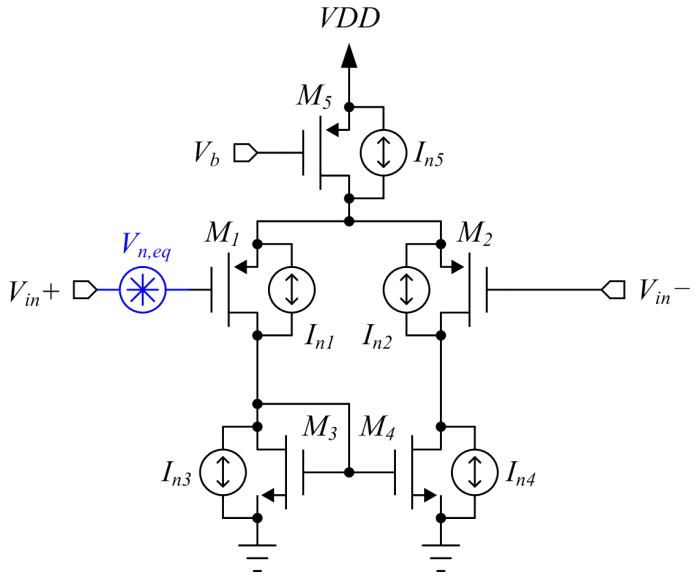


Figure 4.3 Noise equivalent circuit of a CMOS op-amp input stage

The close-loop transfer function of a single pole system is

$$H(s) = \frac{G_0}{1 + s\tau} \tag{4.6}$$

where G_0 is the close-loop DC gain and τ is the settling time constant. The feedback factor, β, in DCT amplifier is about unity. If the op-amp gain is large enough, then the close-loop gain gives

$$G_0 = \frac{1}{\beta + 1/A_0} \approx 1 \tag{4.7}$$

The settling time constant, τ, determines how fast the op-amp can charge the load capacitor, C_{LOAD}. Feedback factor will reduce τ, but since $\beta = 1$, the settling time constant gives

$$\tau = \frac{C_{LOAD}}{\beta g_{m1}} = \frac{C_{LOAD}}{g_{m1}} \tag{4.8}$$

Due to the finite unity gain frequency of the op-amp, its noise will be shaped by the low-pass transfer function given in equation (4.6). The total op-amp noise can be found by integrating the shaped NSD from 0 to infinity which is

$$V_{op}^{\ 2} = \int_0^\infty V_{n,eq}^{\ 2}(f)\left|H(j2\pi f)\right|^2 df = \left(\frac{32kT}{3g_{m1}}\right)\left(\frac{G_0^{\ 2}}{4\tau}\right) = \frac{8kT}{3C_{LOAD}} \tag{4.9}$$

4.4 Unary DAC Noise

The MSB DAC described in section 3.3 is used here to analyze the thermal noise contribution. For simplicity, Figure 4.4 shows the analyzed circuit in signal ended configuration. During sampling phase Φ_3, capacitors C_1 to C_{63} will be charged to either V_{REFP} or V_{REFN} depending on input thermometer code (T_1 – T_{63}). Next, during charge redistribution phase Φ_1, capacitors C_B, C_1 – C_{63} will be connected in parallel through op-amp output and inverting input, where C_B is the last stage capacitor from LSB DAC.

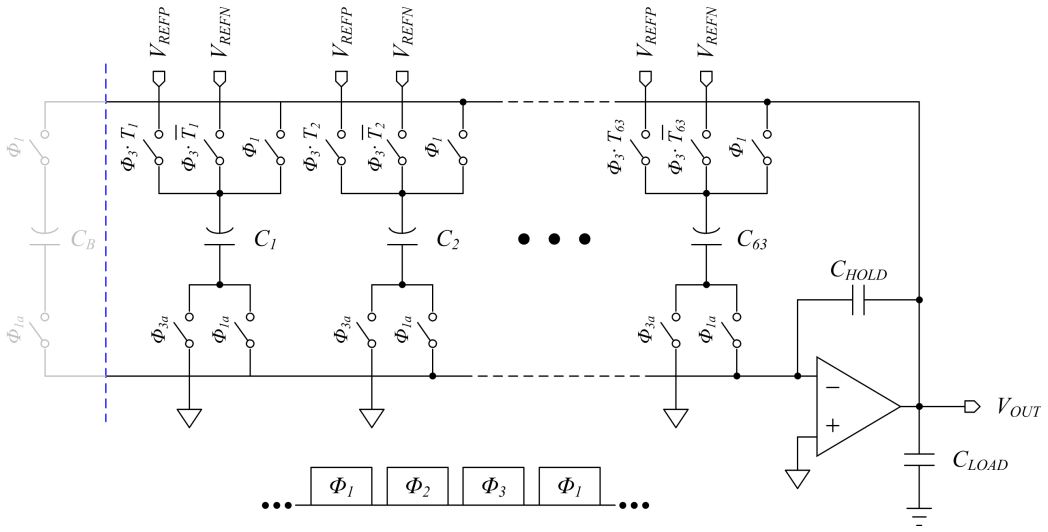


Figure 4.4 Single ended MSB DAC

The noise equivalent circuit of Figure 4.4 during sampling phase is shown in Figure 4.5. At the end of sampling phase, all capacitors C_B, $C_1 - C_{63}$ will individually sample the noise with power equal to kT/C. During charge redistribution phase Φ_1, the sampled noise introduced during Φ_3 will be divided by the gain square, where gain is equal to 1/65 in this case. The noise equivalent circuit is illustrated in Figure 4.6. Since each sampling noise is uncorrelated, the noise contribution at the output will be

$$V_{n,MSB}^{\ 2} = \frac{64kT}{65^2 C} \tag{4.10}$$

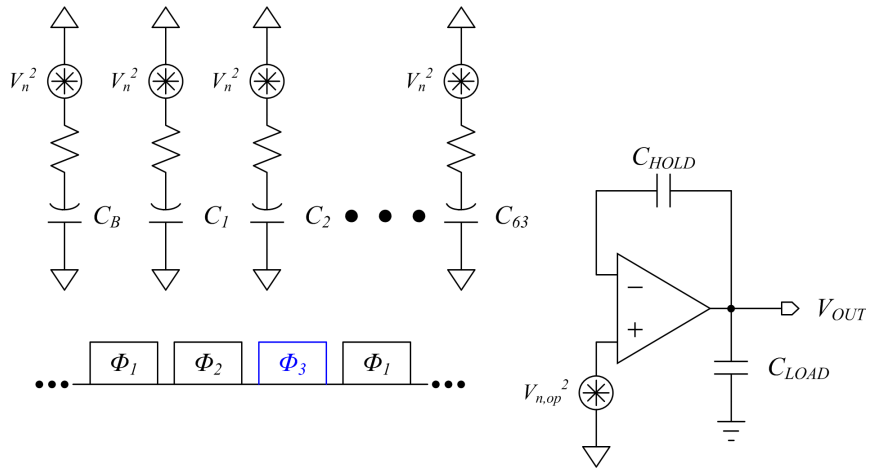


Figure 4.5 Noise equivalent circuit of MSB DAC during sampling phase

The feedback switches connected to the op-amp output will also generate noise. For analysis, consider only one switch is connected to the output. The virtual ground causes the output noise spectrum to be equal to the noise generator $V_n^2 = 4kTR_{on}$ [9]. Thus, the switch introduced noise can be found by integrating the shaped NSD from 0 to infinity which is

$$V_{SW}^{\ 2} = \int_0^{\infty} V_n^{\ 2}(f)\left|H(j2\pi f)\right|^2 df = \left(4kTR_{on}\right)\left(\frac{G_0^{\ 2}}{4\tau}\right) = g_{m1}R_{on}\frac{kT}{C_{LOAD}} \tag{4.11}$$

In reality, there are 64 switches connected to the op-amp output. Each switch will contribute noise that is independent of each other and the gain (65 parallel branches) will reduce the noise power. Therefore, the feedback switch introduced noise is

$$V_{SW}^{\ 2} = \frac{64g_{m1}R_{on}}{65^2}\frac{kT}{C_{LOAD}} \tag{4.12}$$

The total noise power at the op-amp output will include the sampling noise, switch noise and op-amp noise, which is

$$V_{n,total}^{\ 2} = \frac{64kT}{65^2 C} + \frac{64g_{m1}R_{on}}{65^2}\frac{kT}{C_{LOAD}} + \frac{8kT}{3C_{LOAD}} \tag{4.13}$$

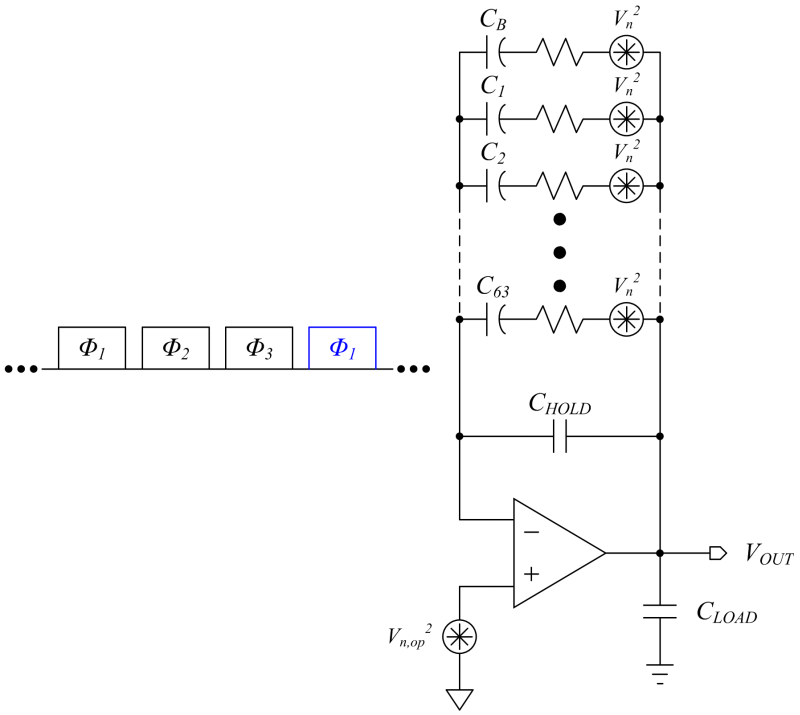


Figure 4.6 Noise equivalent circuit of MSB DAC during charge redistribution phase

4.5 Noise Budget

For 14-bit DAC architecture, it is impossible to achieve 14-bit accuracy in reality. In this design, the target ENOB is 13-bit, thus, it is important to allocate the total allowed noise contribution for each noise source. The amount of quantization noise is fixed by the resolution of the DAC, and it can be used to determine the allowed total noise to achieve 13-bit accuracy. Figure 4.7 shows a graph of quantization noise percentage vs. SNR. The blue curve is the achievable SNR for the corresponding quantization noise percentage and the red dotted line is the target SNR. From this graph, it is clearly shown that if the quantization noise is 100% of the overall noise, then the SNR will be 86 dB. To achieve 13-bit accuracy or 80 dB SNR, the quantization noise has to be 25% of the overall noise.

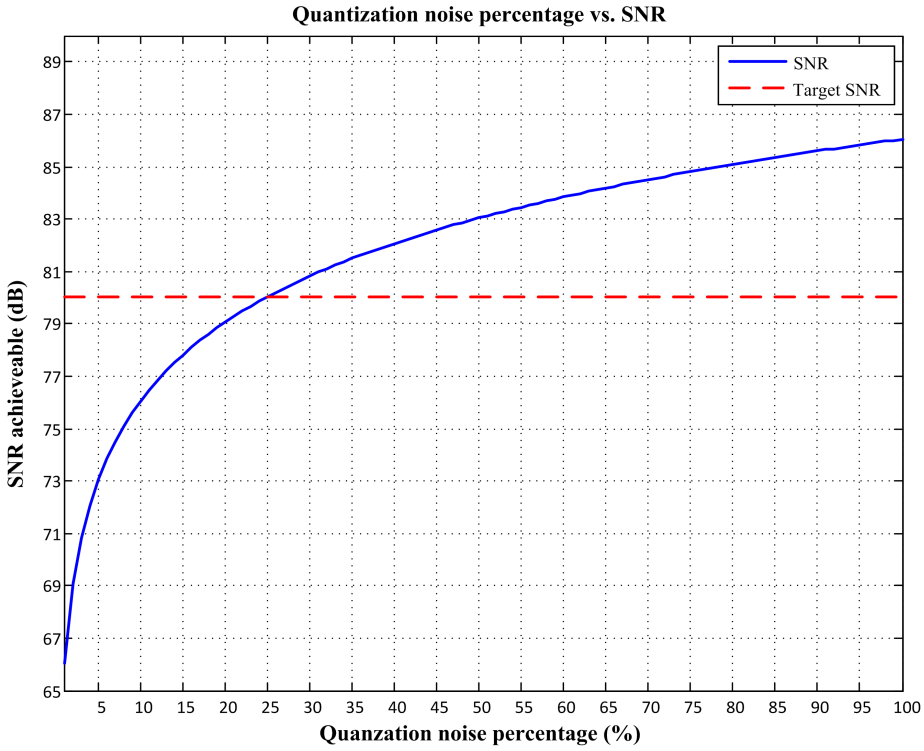


Figure 4.7 Quantization noise percentages vs. SNR

The DAC has common mode voltage at 1.65V, and the reference voltage, V_{REFP} and V_{REFN}, at 2.25V and 1.05V respectively, thus, the differential output swing can reach to $2.4V_{pp}$. From equation (2.4) and (2.5), the RMS value of the quantization noise is

$$V_{Q(RMS)} = \frac{2.4}{2^{14}\sqrt{12}} = 4.229 \times 10^{-5} \quad V \tag{4.14}$$

The quantization noise power is

$$V_{Q(RMS)}{}^2 = 1.788 \times 10^{-9} \quad V^2 \tag{4.15}$$

From the above discussion, the quantization noise is set to 25% of the overall allowed noise, hence the total noise power is

$$V_{n,total}{}^2 = 4 \times V_{Q(RMS)}{}^2 = 7.153 \times 10^{-9} \quad V^2 \tag{4.16}$$

Assume the op-amp loading capacitor, C_L, is 15 pF, input device transconductance, g_{m1}, is 15 mS, and the feedback switch on-resistance, R_{on}, to be 5 kΩ. From equation (4.9) and (4.12), the noise contribution from op-amp and the feedback switch is

$$V_n{}^2 = 2 \times \left(\frac{64 g_{m1} R_{on}}{65^2} \frac{kT}{C_{LOAD}} + \frac{8kT}{3C_{LOAD}} \right) = 2.1 \times 10^{-9} \quad V^2 \tag{4.17}$$

where the coefficient 2 is accounted for the differential configuration. The calculated noise power from equation (4.13) is about 30% of the allowed noise budget. The sampling noise power from equation (4.10) is assigned 20% of the allowed noise budget; therefore, the minimum sampling capacitor is calculated as

$$C = 2 \times \left(\frac{64kT}{65^2 \left(20\% \cdot V_{n,total}{}^2 \right)} \right) = 87.72 \quad fF \tag{4.18}$$

To allow some design margin, the final sampling capacitor is chosen to be 200fF. The

noise budget is summarized in Table 4.1. The remaining 25% of the allowed noise budget is left for other unaccounted noise such as jitter and 1/f noise.

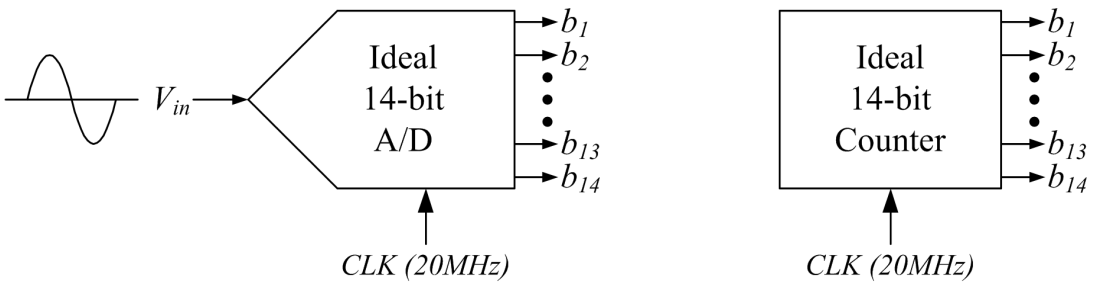
Table 4.1 Noise Budget

Noise Type	Percentage (%)
Quantization Noise	25%
Op-amp Thermal Noise	30%
Sampling Thermal Noise	20%
Other Noise	25%
Total Noise	100%

CHAPTER 5 RESULTS

5.1 Simulation Environment

All circuit simulations are performed using Cadence Spectre, and the resulting data are post-processed through MATLB. All supply and reference voltages use ideal voltage sources. The inputs of the DAC are 14 parallel digital bits. These digital bits are generated through an ideal 14-bit ADC or an ideal 14-bit counter which are modeled using Verilog-A language. Figure 5.1(a) shows how the input digital codes are generated for dynamic performance measurement. For static performance measurement, the ideal 14-bit counter shown in Figure 5.1(b) is used to sweep through all the possible input digital codes. The output digital code in this case will ramp up from code 0 to 2^N. To simulate the effect of capacitor mismatch, capacitor values are assumed to have 0.1% mismatch for 1 standard deviation (σ), and it is calculated using MATLAB for simulation.



(a) (b)

Figure 5.1 Input digital code generation

5.2 Dynamic Performance

The output spectrum is obtained by running fast Fourier transform (FFT) algorithm of the simulated DAC transient output. The number of FFT points will affect the transient simulation time. Using too less points will result in lower spectrum accuracy, but using more points will result in long simulation time; therefore, choosing 2048 FFT points is sufficient enough in this case. Figure 5.2 shows the simulated output spectrum when DEM circuit is disabled. With same simulation setup, but turning on DEM circuit, the output spectrum is plotted in Figure 5.3. Note that the harmonic distortion caused by capacitor mismatch is greatly reduced.

5.3 Static Performance

To determine the static performance, namely DNL and INL, a ramp like digital signal is applied to sweep through all the possible input digital codes. The output nonlinearity errors are calculated after the offset and gain error have been removed. Figure 5.4 and 5.6 shows the DNL and INL when DEM circuit is disabled, and Figure 5.5 and 5.7 shows the DNL and INL when DEM circuit is on. Since the DEM algorithm uses randomization, the DNL and INL seen in Figure 5.5 and 5.7 is random for different input digital code but the average DNL and INL approaches zero. The DNL and INL shown here are represented in unit of LSB.

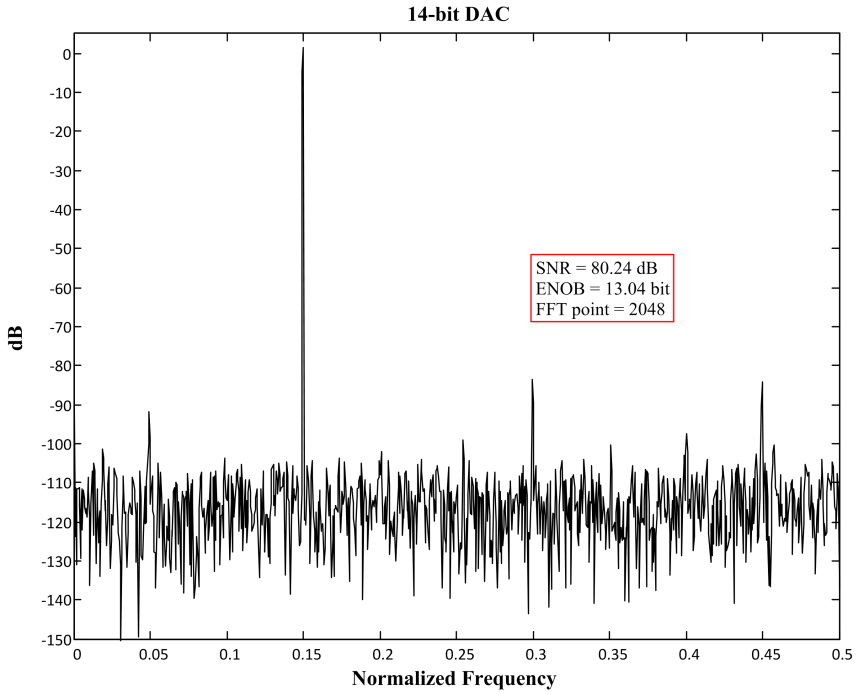


Figure 5.2 Output spectrum with DEM disabled

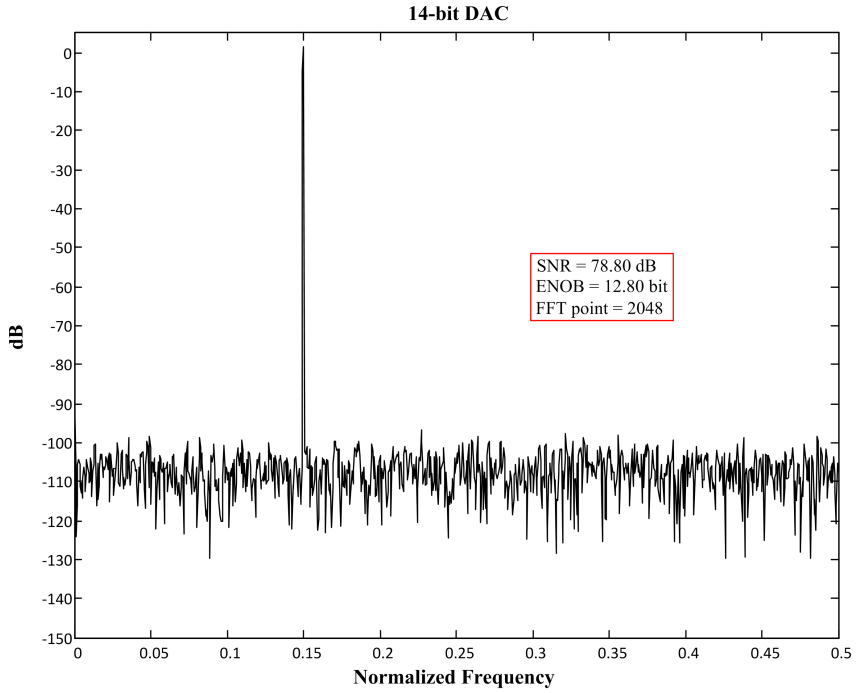


Figure 5.3 Output spectrum with DEM enabled

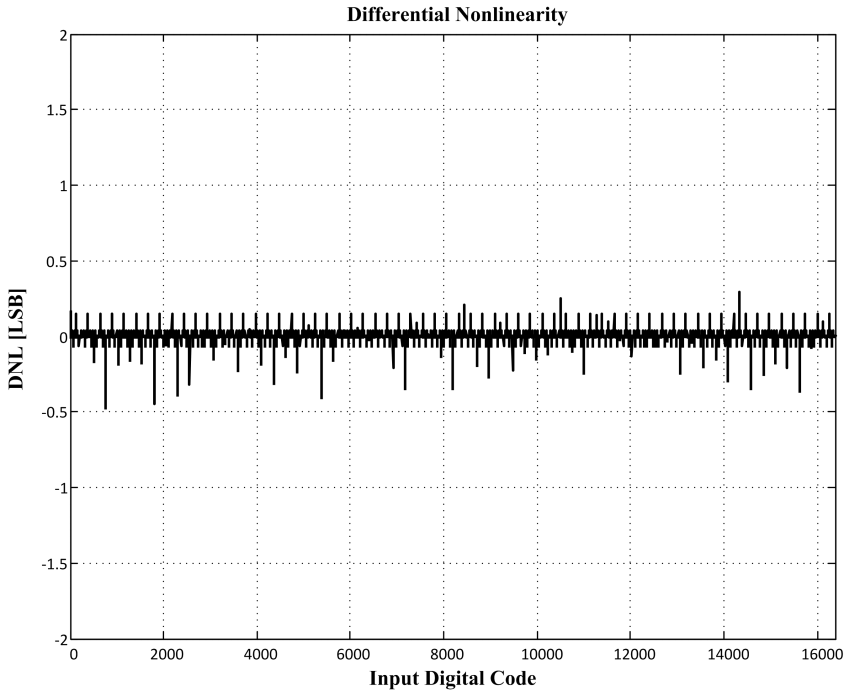


Figure 5.4 Differential Nonlinearity with DEM disabled

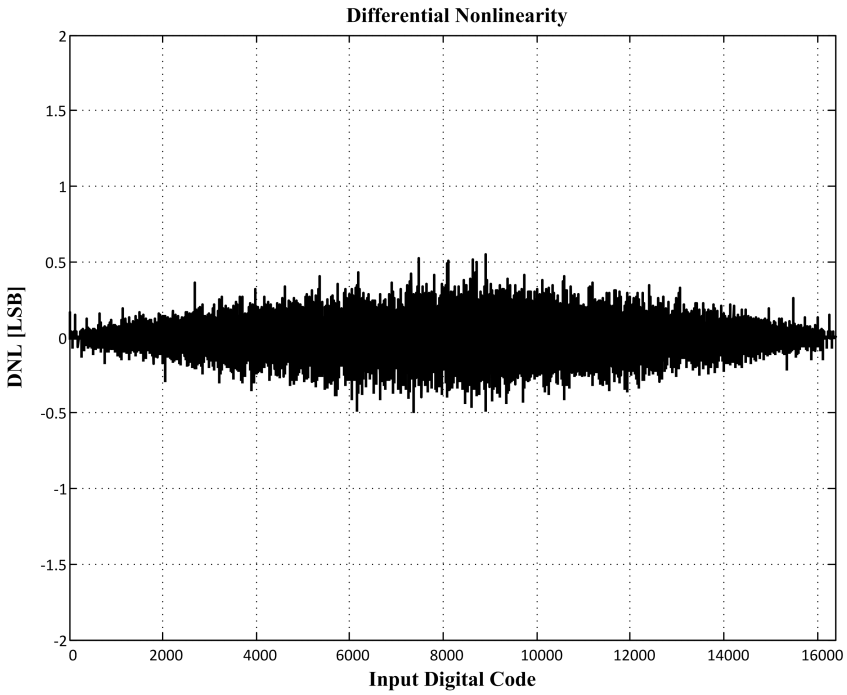


Figure 5.5 Differential nonlinearity with DEM enabled

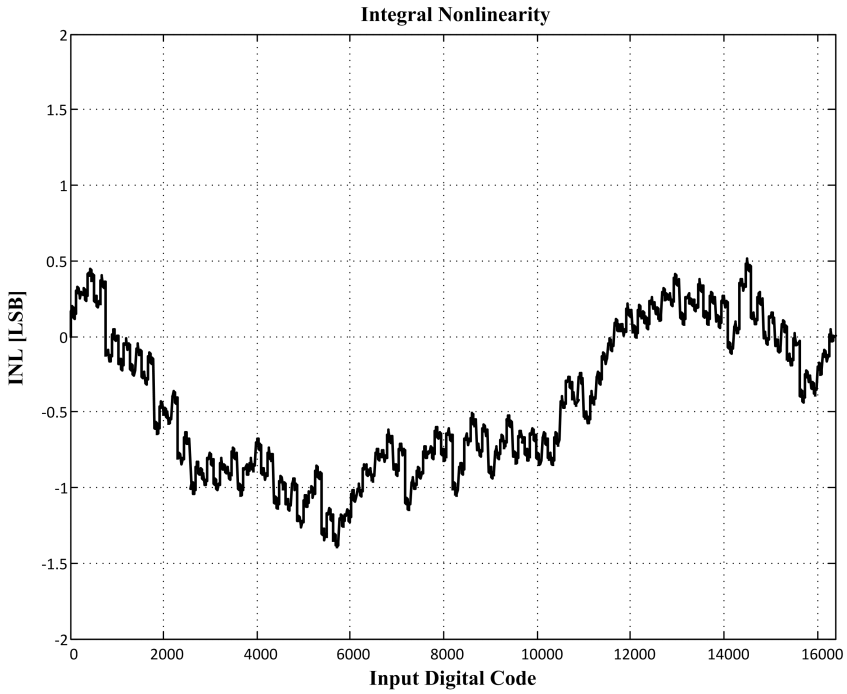


Figure 5.6 Integral Nonlinearity with DEM disabled

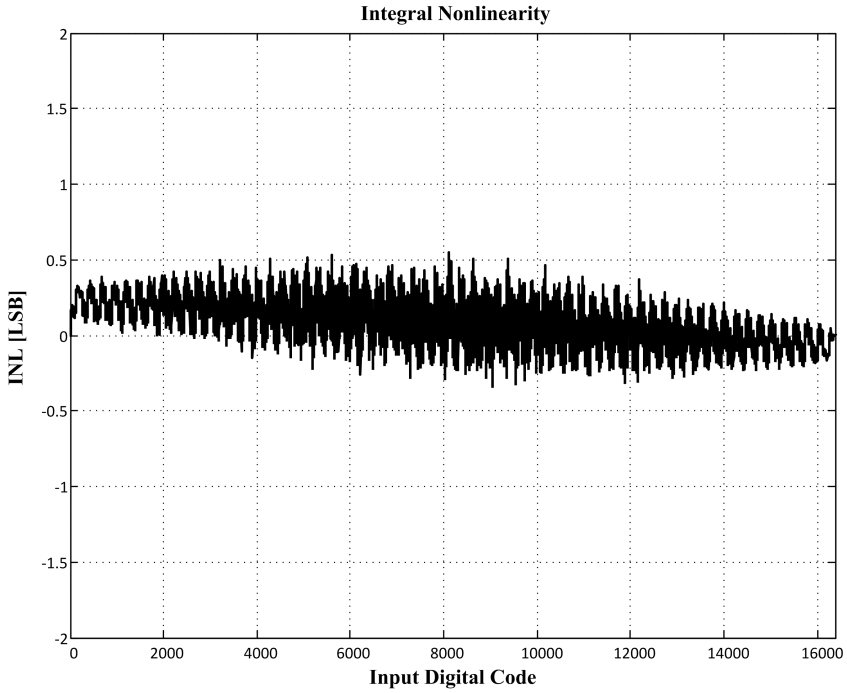


Figure 5.7 Integral nonlinearity with DEM enabled

CHAPTER 6 CONCLUSION

6.1 Summary

In this work, a 14-bit, 20MS/s pipelined segmented DAC has been designed and simulated with 0.18 μm CMOS technology. The designed DAC utilized the segmented architecture to achieve the balance between performance and chip area. Both binary and unary DAC are implemented using switched-capacitor circuits and its operation only consume dynamic power. The output buffer uses DCT technique to lower the *kT/C* noise without sacrifice the power consumption. In some applications such as audio and telecommunication systems, the SFDR requirement is high. From simulation the implemented DEM circuit can effectively improve the SFDR requirement with only little SNR reduction.

6.2 Future Work

The output buffer block consumes a substantial amount of power because it needs to drive large off chip load, thus another low power alternative should be considered. Normally, a continuous time reconstruction filter is followed by a DAC to remove any high frequency components, but this thesis work did not include one. Since the simulated results are post-processed through MATLAB, the higher frequency component can be easily removed. Future work should aim to include the reconstruction filter and actual chip implementation for measurement result.

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