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Title: Electrochemical Etch Characteristics of (100) Silicon in Tetramethyl Ammonium Hydroxide.

Abstract approved _____
Michael E. Kassner

A study of potentiostatic and galvanostatic electrochemical etching of silicon in tetramethylammonium hydroxide (TMAH) has been carried out. In TMAH baths, we find that biased (100) silicon etch rates increase 21% over OCP etch rates. For TMAH baths seasoned with silicon, biased silicon etch rates increase to 63% over those at OCP. Electrochemical etching eliminates the growth of hillocks on etching surfaces regardless of etchant pH, [TMAH] or silicon loading, resulting in highly smooth etching surfaces. Potentiostatic and galvanic etching yield similar etch rates and surface consistency.

Electrochemical Etch Characteristics of (100) Silicon in Tetramethyl Ammonium Hydroxide

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DEDICATION

Dedicated to my wife, who never begrudged my absent hours. Also to my parents whose trust and encouragement were invaluable.

ELECTROCHEMICAL ETCH CHARACTERISTICS OF (100) SILICON IN TETRAMETHYL AMMONIUM HYDROXIDE

INTRODUCTION

Anisotropic, wet chemical etching of silicon is used extensively in the fabrication of many microelectromechanical systems (MEMS) including pressure sensors and microfluidic devices [1,2]. The appropriate choice of etchant is driven primarily by the desire to maximize the etch rate of a particular crystal plane in the

silicon lattice while minimizing the etch rate of others. For example, in anisotropic wet etching of (100) silicon, a higher relative etch rate of the (100) planes in relation to the (110) and (111) results in a well-defined, micromachined trench with final dimensions determined by the etch mask geometry and the angles between the three crystal planes (see Figure 1).

A number of etchants including potassium hydroxide (KOH), ethylenediamine-pyrocatechol-water (EDP), and hydrazine-water have been used to successfully etch silicon in this manner, but each has drawbacks for use in a

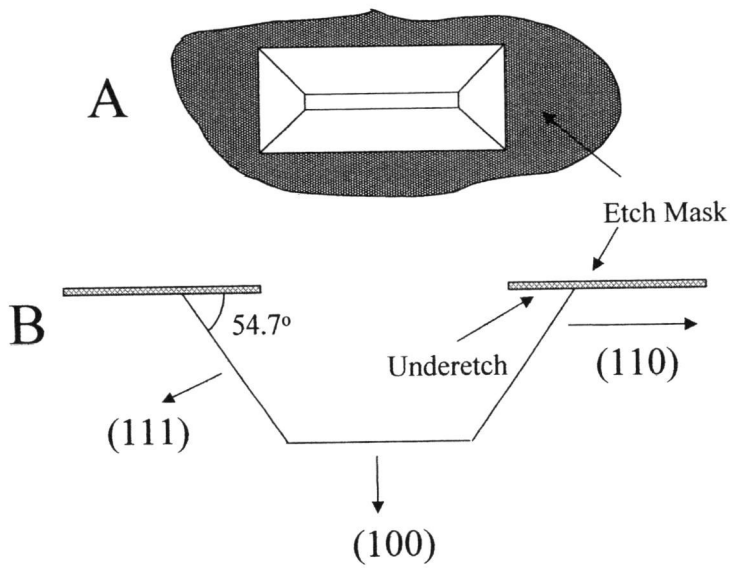

Figure 1: Schematic representation of etch mask and resulting trench A) Plan view and B) Cross section. Note the well defined geometry of the feature dictated by the crystal lattice of the substrate.

manufacturing environment. Aqueous KOH solutions are the most widely used of the three due to high etch rate selectivity and low toxicity, but mobile ion contamination (K^+) precludes compatibility with CMOS processes typically used in fabrication of a working device. Hydrazine-water and EDP also exhibit desirable silicon etch characteristics, but handling of these materials is challenging due to high toxicity and chemical instability.

Recently, the use of non-toxic tetramethyl ammonium hydroxide (TMAH) has received considerable attention as an anisotropic wet chemical etchant which exhibits satisfactory silicon etch rate and (100) vs. (110) and (111) selectivity [3]. A number of researchers have investigated the etching characteristics of TMAH over a range of operating conditions and have successfully fabricated prototype devices based on this technology [4]. The use of TMAH in a manufacturing environment, however, is still under development and requires further optimization. Variability in etch rate (over time or depth) is a concern as well as is the final surface quality of the etched crystal planes. OCP etching results in the formation of hillocks or pyramids on the etch surface, an effect that is minimized by increasing TMAH concentration. This, however, comes at the cost of etch rate. Further, production wafers are commonly etched in silicon loaded baths which lower the etch rate of aluminum, a common conductive layer, as well as the silicon oxide layer for transistor gates. However, this protection results in the growth of additional hillocks and a further lowered etch rate. Inadequate control of surface

morphology and etch rate can result in unacceptable yield loss and delays in production .

An intriguing alternative to conventional TMAH etching that may offer improved control of etch rate, selectivity and surface morphology is etching under an external bias. Conventional wet etching takes place with the electrochemical potential of the silicon floating at open circuit (OCP). While this technique is amenable to batch fabrication, operating at OCP can result in the silicon etch rate being strongly influenced by the presence of other materials on the wafer [5] leading to unpredictable etch behavior and inadequate process control. In contrast, etching with an external bias allows control of etch rate by appropriate choice of operating potential. Through direct biasing of the silicon itself, the influence of other materials on the silicon etch rate is minimized. In addition to rate control, the use of electrochemical etching may lead to increased etch rates as well. Biased etching of (100) silicon in KOH, for example, has been shown to increase the overall etch rate by at least 25% without loss of selectivity [6].

To date, the study of electrochemical etching of silicon in TMAH has been limited primarily to investigations exploring the oxidation reaction mechanisms and product species resulting from silicon corrosion [7]. At this time, however, there exists a need for a systematic study to explore the processing parameter space related to electrochemical etching of silicon in TMAH. In the present study, we attempt to understand and characterize the general electrochemical etch behavior of

silicon in TMAH. Specifically, this study seeks to investigate the effects of applied potential and solution chemistry, pH and temperature on the etch rate, selectivity and surface morphology of (100) p-type silicon.

EXPERIMENTAL

The silicon wafers used in our experiments were commercial grade, p-type, (100) 6" diameter, single side polished wafers with resistivities specified at 12-18 ohm-cm. A 1 *u*m thermal oxide layer was grown on the front polished side of the wafer using standard processing, and served as the etch mask after lithographic patterning. As shown in Figure 2, the mask defined an exposed silicon pattern of trenches, squares and "wagon wheels" which were used for characterizing etch rates and uniformity. The total exposed silicon area of each wafer was approximately 29.25 cm^2. For the purposes of this experiment, four of the 1 mm x 8 mm trenches were considered for etch depth and etch rate calculations. These trenches are marked with a red circle in Figure 2A. These trenches were specifically chosen for their spread across two trench formations and their centralized location, which reduced measuring time. In order to provide uniform

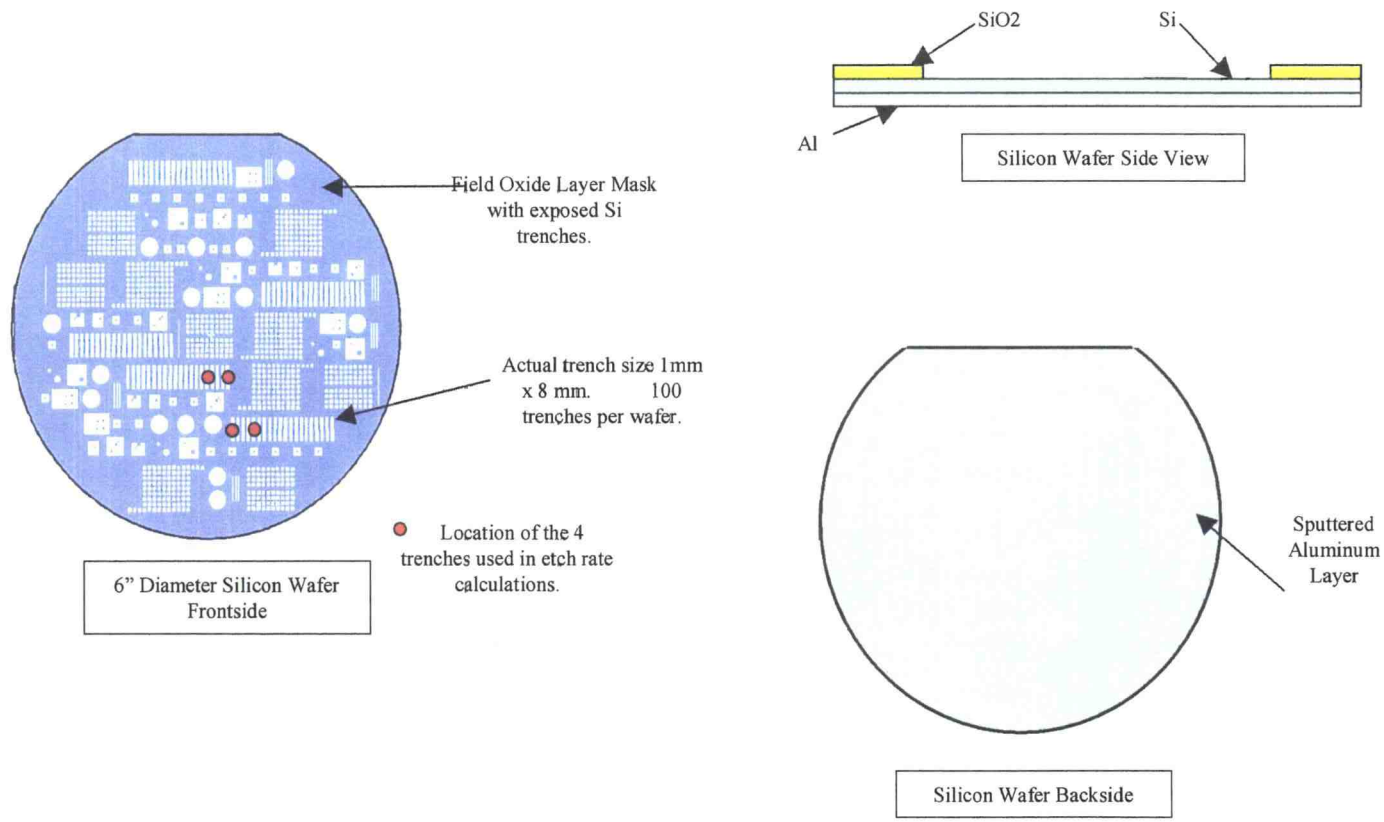

Figure 2: Patterned wafer used in experiments.

electrical contact, the backside of the wafers were sputtered-coated with a 1 *u*m aluminum strapping layer. The aluminum/silicon ohmic resistance was estimated to be 1.5 kΩ[1]. This drop was assumed to be acceptable, as illustrated by the i-V analog scans of these wafers as discussed below. The wafer cross-section (Fig 2C) illustrates the architecture of the sample wafer in cartoon form.

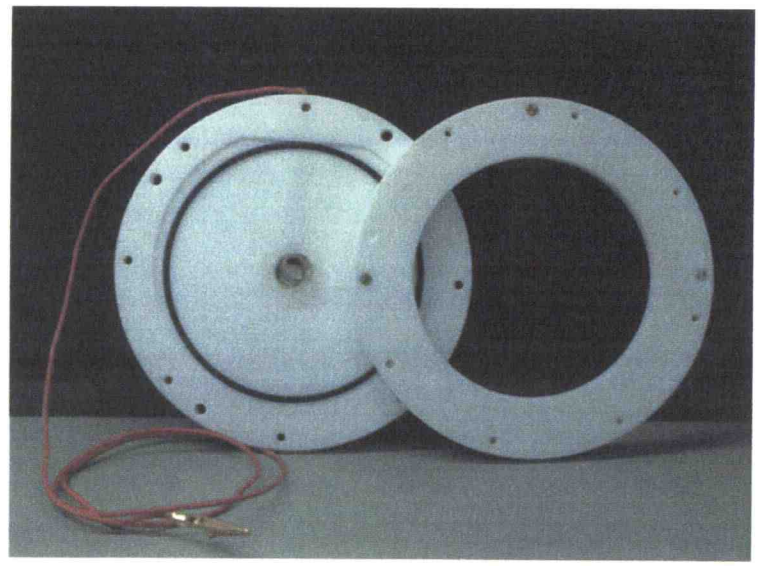

Figure 3: Exploded Digital Image of Wafer Chuck

Etching of the wafers was performed with the use of a polytetrafluoroethylene (PTFE) wafer chuck – see Figure 3. The chuck consisted

[1] Based on ohmic drop measurements between the electrode contact and the front side Si surface

of two pieces that sandwiched the wafer between them, sealing the backside against chemical exposure with two Dupont perfluoroelastomeric 1050LF o-rings. A recessed socket in the center was fitted with a 1" diameter stainless-steel spring that made contact with the aluminum-sputtered backside of the wafer as it was sealed in the chuck. A hole was bored down through the top of the chuck back plate, and an 18 AWG copperwire connected the spring to the power supply. In this way, the chuck could be inserted into the process tank until the entire front surface of the wafer was exposed to the etchant, with the spring acting as a switch, allowing isolated electrical contact to the wafer backside surface.

The complete experimental apparatus is shown in Figure 4. All etching was performed in a rectangular 12 liter Pyrex tank (A). Pyrex was chosen for the tank material due to its acceptable resistance to caustic chemistries[2]. The tank was maintained at 90 +/- 1°C with the use of a Love 1600 Series Temperature Controller (B). The heat loss through the tank walls, however, was high enough that the tank had to be insulated with 1" R13 Styrofoam. A type J thermocouple immersed in the process tank provided feedback to the temperature controller, which used a proportional integral algorithm to maintain temperature. Output of the controller drove a single 500W Vycor heating rod immersed in the process tank. A second heating rod, not connected to the controller, was used to bring the

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[2] While quartz is generally acceptable as a high pH resistant tank, the use of Pyrex is not as widespread. The probable reaction product of Pyrex and TMAH is likely silicose, which should not adversely affect bath chemistry.

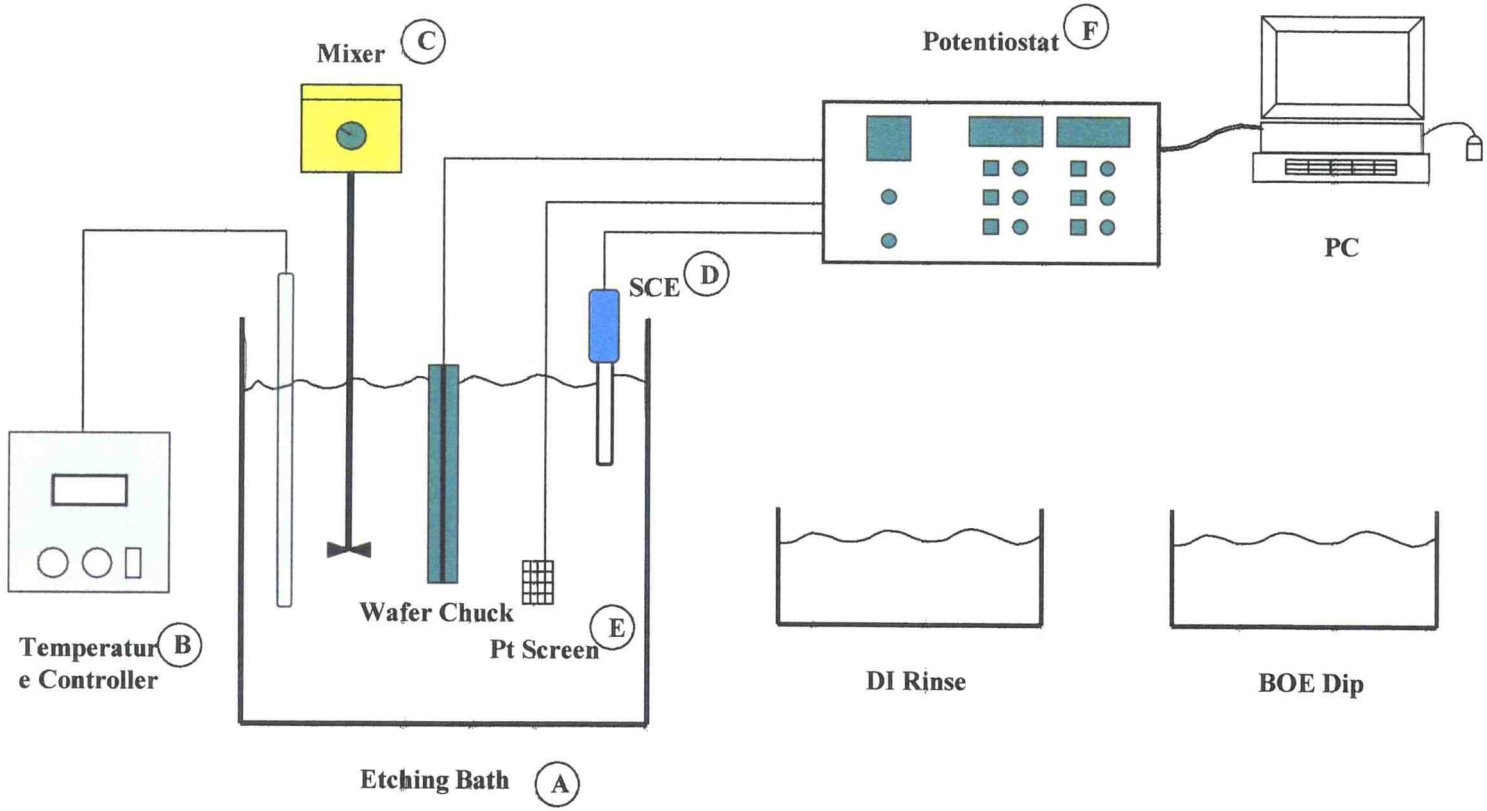


Figure 4: Experimental Apparatus

bath up to the experiment temperature from ambient. The bath temperature was periodically verified with the use of a handheld VWR Scientific Digital Thermometer.

The tank was agitated by an external high-shear Cole-Parmer Laboratory mixer (C). The stainless steel mixer shaft and blades were coated with Teflon to provide additional protection against the caustic bath environment. The motor was mounted above the tank to protect its components from moisture and heat. Low speed, ~100 rpm, agitation of the process bath was found to be necessary for the maintenance of a constant etching temperature and to enhance (albeit in an uncharacterized manner) convective/diffusive mass-transfer to and from the silicon etching surface. The wafer chuck, discussed above, was immersed in the tank and secured with the use of a stainless steel chuck bracket, also coated with Teflon for chemical resistivity. The bracket maintained the wafer chuck at a depth where the entire surface of the wafer was in contact with etchant solution. A Saturated Calomel Electrode (SCE) (D) was used as an electrochemical reference, and a high-surface area platinum mesh (E) was used as the counter electrode. Both were immersed into the tank and held by chemical stand clamps. Supporting tanks were located directly adjacent to the process tank. Both were 8 liter Teflon tanks. The first contained 20:1 Buffered Oxide Etchant (BOE), an aqueous solution of one part 49% hydrofluoric acid and 20 parts 40% ammonium fluoride, purchased premixed from General Chemical (molar concentration at ambient are

approximately [HF] = 1.4M and [NH4F] = 11.4M respectively). BOE was used as a native oxide etch prior to TMAH processing. The second tank was filled with 18 M-Ω deionized water for rinse of wafers after the BOE dip. The pH of the respective TMAH etch chemistries was measured with the use of a Corning pH meter, Model 430.

Monitoring and control of the etching process was made possible with the use of a Pine Bipotentiostat Model AFCBP1 (F) and its accompanying software running on an external PC. Based on vendor specs for SCE and the Pine Bipotentiostat, the accuracy in measuring potential is assume to be +/- 5 mV and +/- 2 mA/cm^2. Connections made to the SCE, platinum net and wafer allowed for complete control of the etching circuit. Bias and current flow between any of the electrodes could be read off an LED display. Potentiodynamic, potentiostatic and galvanostatic electrolysis experiments were driven either from the console or through the software package, which used a straightforward program to monitor and control variables such as electrode potentials, data acquisition intervals and time delays. See Figure 5 for an example of the software control panel. The Pine software also allowed for the graphing of the referenced wafer potential and current.

Etching of the silicon wafers used the following general approach. Wafers were sealed in the wafer chuck, and the circuit from the exposed silicon to the wire

was verified using a Fluke Multimeter Model 75III. The chuck was quickly immersed in BOE and rinsed, followed by immersion in the process bath. Wafer potential was controlled by the Potentiostat, and the software package loaded on the PC recorded current and working electrode potential as a function of time. Following etching, the wafer was rinsed and the depths of the silicon trenches were

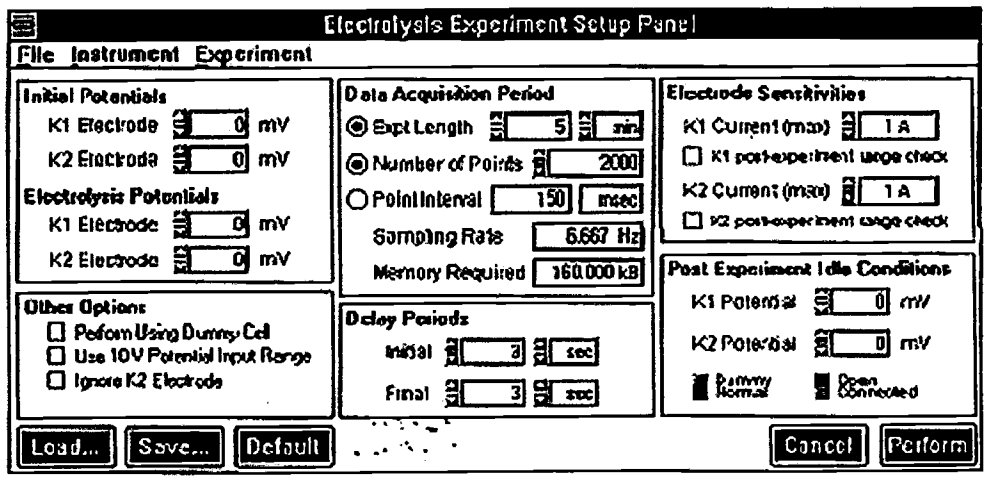


Figure 5: Pine Software Interface Panel

measured. The wafers were also examined using Scanning Electron Microscopy (SEM) to assess quality of the etch surface morphology and to obtain independent depth measurement. This approach allowed for careful and efficient monitoring

of the primary experimental response, i.e. etch rate and surface quality of the etching surface. Details of these different experimental steps follow.

For each experimental trial, a bath chemistry and concentration were first selected. Olin Chemical 25 wt% TMAH was used as the initial bath solution. For baths of lower TMAH concentration, the 25 wt% solution was diluted with DI water. In the present study, Si etching in TMAH concentrations of 2.5, 5, 10, 15 and 25 wt% were explored. Also, experiments were conducted using TMAH solutions containing dissolved silicon. Premixed Moses Lake Industries 5 wt% TMAH with 0.6M silicate were used. For other silicate loading levels, solutions were prepared by first diluting the 25 wt% TMAH to 5 wt%, followed by dissolution of bare Si wafers. Based on known etch rates of silicon in 5 wt% TMAH and fixed bath volume, the desired silicate concentration was obtained after preparation. The chemistry and pH of each bath was confirmed by independent analytical measurements. In independent analyses, bath pH was determined using a Beckman 45 meter calibrated with 4, 7 and 10 pH standards. Conductivity was measured using a Corning Conductivity Meter Model 441 calibrated with 84 uS (40.38 ppm KCl) standard from Oakton. Silicate concentration was determined using UV-VIS spectroscopy in the following way. Five grams of bath solution were analytically weighed to five significant figures, and then each was diluted with 95 grams of de-ionized water. The sample was then titrated with 1.000 N

HCL using an EM Science P200 Auto-Titratator, equipped with potentiometric titration hardware.

After bath preparation, a wafer was selected for etching, and its unique serial number was recorded for tracking purposes. The resistivity of the chuck spring switch was then measured using the Fluke Multimeter. The resistivity between the silicon surface and the wire connector was then measured and recorded. Repeated immersions in the tank and the ensuing exposure to heat and moisture led to degradation of this circuit over the course of our study. Trial and error experimentation revealed that resistance greater than 12 kΩ was consistent with a poor contact between the spring switch and the backside of the wafer, and the switch would be replaced in such a circumstance (over the course of the study, ~700 hours of etching, the spring was replaced 8 times). The wafer was then sealed in the wafer chuck, with the exposed silicon surface facing outward. Throughout the course of the experiment, nitrile gloves (VWR scientific) were worn in order to prevent finger oils from contaminating the wafer surface.

After acceptable contact was achieved, the entire chuck was immersed in the BOE bath for 1.5 minutes to allow the dissolution of the native oxide from the exposed silicon. During this process, the chuck was slowly agitated by hand in the bath to improve the wafer contact to fresh BOE. Next, the chuck was rinsed in the DI bath for 60 seconds, and then immersed in the process tank, secured by the chuck bracket. Connections between the SCE, platinum net, wafer and

Bipotentiostat and the appropriate bias was then applied either through the console or software. All etching was performed for one hour, thus yielding etch depth, as well as etch rate. Implicit in our analysis is the assumption that the etch rate is constant during this time period, as well as being representative of longer etching times. Both of these assumptions are likely only partially true. Implications are discussed in subsequent sections.

Etch trench depths were measured using a UBM Messtechnik gmbH optical profilometer, with associated Microfocus measurement and analysis software. This instrument is specified to be accurate to +/- 0.2 um. Depths were measured from end to end in each of the chosen four trenches on each wafer as shown in Figure 2. Measurements were obtained at 1 mm intervals throughout the trench length (208 data points were collected on each trench for a total of 832 depth measurements per wafer). These depth measurements (in addition to the total etch time) were used to determine the average etch rate for a given wafer. While this data allowed for the quantitative mapping of the trench surface morphology, Scanning Electron Microscopy was used to compliment UBM results. A standard set of four images was taken of each wafer to allow for visual comparison of each trench for a given condition. Each wafer was scribed and then sectioned to produce a sample containing six trenches; with a cross-section across each trench. The samples were mounted on a 45 degree chuck, which enabled SEM images of the trenches in profile, and secured to the mounting plate of a Phillips XL40 SEM. All functions

of the tool were controlled by the associated computer and the Phillips software package including vacuum control, camera focus, mounting plate orientation, and electron beam functionality. The chamber was pumped to high vacuum and the sample brought into focus at a working distance of 10 mm and using an accelerating voltage of 15kV. One of the four trenches on the sample was chosen at random, and four images were taken of that trench. One 100X image was taken of the entire trench in profile, showing the etch depth and etch surface morphology. One 1000X image of the etch surface cross section allowed for close analysis of the surface morphology. The remaining two images, taken at 1000X and 500X respectively, were used to illustrate the corner features of the trench, both at the cross section plane, and a trench corner.

RESULTS AND DISCUSSION

ELECTROCHEMISTRY BASICS AND ELECTROCHEMICAL RESPONSE OF (100) P-TYPE SILICON IN TMAH

Wet etching of silicon is characterized by both thermodynamic and kinetic parameters. Oxidation reactions such as

$$Zn(s) \rightarrow Zn^{2+}(aq) + 2e^{-} \quad E_{ox} = 0.76V \qquad \{1\}$$

involve the loss of electrons from a material and occur, by definition, at the anode. In {1}, E is the electrochemical or equilibrium reduction potential of the Zn/Zn+2 system. In essence, this value is a relative measure of the likelihood that Zinc will be oxidized (or reduced) in a given thermodynamic system. The electrochemical potential of the reaction is measured versus a reference, often SCE or SHE.

Reduction reactions such as

$$Cu^{2+}(aq) + 2e^{-} \rightarrow Cu(s) \quad E_{red} = 0.34V \qquad \{2\}$$

involve the gain of electrons by a material and occur, by definition, at the cathode.

The combination of two half reactions such as those in {1} and {2} is a complete oxidation-reduction or redox reaction.

$$\begin{aligned} &Zn(s) \Leftrightarrow Zn^{2+}(aq) + 2e^{-} \\ &Cu^{2+}(aq) + 2e^{-} \Leftrightarrow Cu(s) \\ &\text{---------------------------------} \\ &Cu^{2+} + Zn \Leftrightarrow Cu + Zn^{2+} \end{aligned} \qquad \{3\}$$

The difference in electric potential between the anode and cathode can be measured by a voltmeter, and is called the cell voltage or cell potential. For Cu/Zn as shown in {3}, the cell potential is the sum of the oxidation and reduction potentials, or 1.10V.

Silicon etching is significantly more complex in terms of redox characteristics. We assume that silicon freely binds hydroxyl groups as in {4}.

$$Si_{(s)} + 2OH^{-}_{(aq)} \rightarrow Si(OH)^{-2}_{2(s)} \qquad \{4\}$$

This initiates the following set of reactions for the oxidation of silicon.

$$\{5\} \quad Si(OH)_{2(aq)}^{-2} + 4OH_{(aq)}^{-} \Leftrightarrow SiO_2(OH)_{2(aq)}^{-2} + 2H_2O + 4e^{-} \qquad [E_{(1)}]$$

$$\{6\} \quad 4H_2O_{(aq)} + 4e^{-} \Leftrightarrow 4OH_{(aq)}^{-} + 2H_{2(g)} \qquad [E_{(2)}]$$

$$\{7\} \quad Si(OH)_{2(aq)}^{-2} + 2H_2O \Leftrightarrow SiO_2(OH)_{2(aq)}^{-2} + 2H_{2(g)} \qquad [E_{(eq)}]$$

Electrolysis occurs when reactions deviate from thermodynamic equilibrium. An applied potential acts as a driving force, shifting a reaction from equilibrium to reduction or oxidation. If the applied potential is more negative than the equilibrium reduction potential, the reduction reaction is favored. Likewise, an applied potential more positive than the equilibrium reduction potential will favor oxidation.

The relationship between cell potential and thermodynamic parameters such as temperature and chemical activity is described by the Nernst Equation.

$$E = E^{o} - \frac{RT}{nF}\ln(Q) \qquad \{8\}$$

where E^{o} is the formal potential at standard state conditions, R is the gas constant (8.314J/K-mol), T is temperature (K), and Q is the reaction quotient ($\Pi a_i^{V_i}$, assuming that a_i can be approximated by concentration, c_i). The Nernst Equation illustrates that changes in temperature as well as species concentrations influence cell potentials. Recall that our experimental setup used a silicon wafer sealed in the etching chuck as the working electrode (anode), and the platinum mesh as the

counter electrode (cathode). To establish a thermodynamic anchor point, we first measured

OCP vs. the SCE using a simple Fluke Multi-meter. This was followed by an i-V analog scan generated by varying the potential of the silicon from negative to positive of equilibrium while measuring the corresponding cell current. The result is generation of a functional relationship between thermodynamic state (E) and reaction rate (j). A representative example of such a scan is illustrated in Figure 6. Following the scan in Figure 6 from –1.75 to –0.50V, a number of features are of interest. First, the point with no net current flow through the circuit

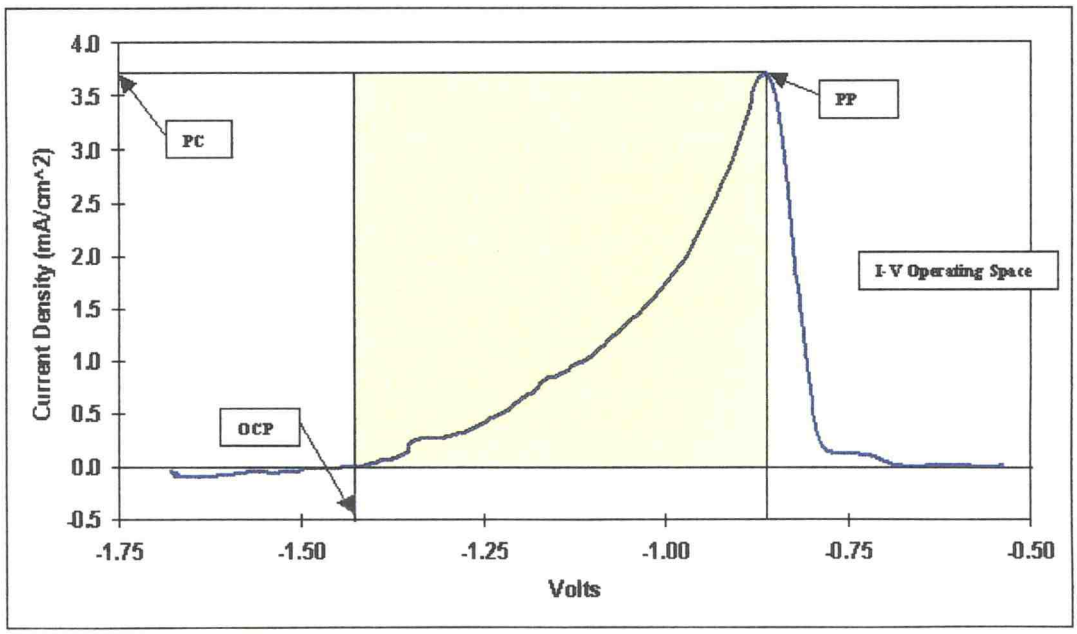


Figure 6: Representative I-V Curve of Silicon wafer in TMAH

is identified as the equilibrium, or Open Circuit Potential (OCP). By definition, the OCP is the potential at which the rates of oxidation and reduction reactions at the wafer surface are equal. The OCP is more commonly referred to as the equilibrium potential of the electrode/electrolyte system, and represents a quantitative measure of the thermodynamic state of the system without application of an external energy source. In Figure 6, for example, the OCP was measured to be -1.37 V vs. SCE. At potentials negative (cathodic) of OCP, reduction reactions predominate and a negative current is measured. At potentials positive (anodic) of OCP, oxidation reactions are thermodynamically favored and positive current is measured. (Note that the convention for current flow varies. Here we stick with oxidation currents > 0 and cathodic currents < 0.) Increasingly positive potentials produce higher anodic current flows until a maximum is reached at the Passivation Potential (PP). This point represents the transition from a silicon dissolution reaction regime to that of silicon passivation. At potentials greater than PP, a passivation reaction occurs in which silicon binds with hydroxyl ions to produce silicon oxide on the wafer surface. At the PP, there is an associated current of the reaction, which we will call the Passivation Current (PC). Increasing anodic cell potentials beyond PP decreases the reaction current as the passivation layer grows and becomes non-conductive.

The i-V response mapped by the analog scan is unique for the thermodynamic state of a given system (e.g. electrode set, temperature and

concentration). For the case of silicon etching, dissolution occurs only in the potential window bounded by the OCP and PP; defined here as the Operating Space (OS) for silicon (and other) etching reactions. In essence, this window defines the range of potentials and currents that correspond to silicon etching.

The information contained in a plot like that shown in Figure 6 can then be used to guide how one might choose to etch silicon by application of an applied potential (potentiostatic etching) or though an applied current (galvanostatic etching). In the case of potentiostatic etching, the application of a specific potential within this space drives a specific reaction (including silicon etching), resulting in the corresponding current flow (proportional to silicon etch rate). In the case of galvanostatic etching, however, the applied current does not necessarily prescribe a set of corresponding reactions; rather the potential at the working electrode floats, resulting in the possibility that a suite of undefined reactions at the silicon surface occur. Clearly, however, one of these reactions includes silicon etching. In either case, the OS defined in Figure 6 provides a bounding space for both potentiostatic and galvanostatic etching of silicon – a range where etch rates were anticipated to be greater than those achieved simply by etching at the OCP.

PROCESS SPACE AND TMAH CONCENTRATION

Figure 7 shows the i-V curves which define the operating space for the five TMAH concentrations investigated. Table 1 summarizes the salient features of each curve. (For reference, OCP of Au in TMAH at 90°C was measured to be 1.2V vs. SCE.) It is observed that both OCP and PP shift cathodically as the TMAH concentration is increased. That is, as TMAH concentration increases, the

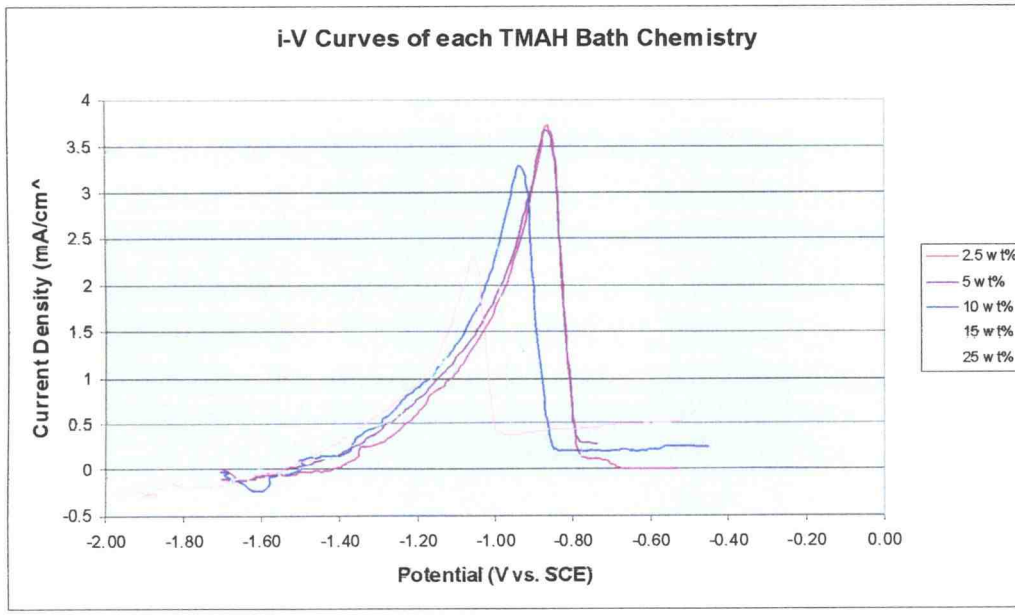


Figure 7: iV Curves of each TMAH Bath Chemistry

Table 1: Bath Chemistry and Associated Electrochemical Characteristics of (100) Si in TMAH (Numerical presentation of data shown in Figure 6)

Concentration (wt% TMAH)	Molar Conc. (M)	Measured pH	OCP (mV vs SCE)	OS (mV)	PP (mV vs SCE)	PC (mA/cm^2)
2.5	0.28	13.51	-1361 +/- 22	511	-850	3.71
5	0.56	13.83	-1443 +/- 17	591	-852	3.66
10	1.11	14	-1481 +/- 11	530	-951	3.28
15	1.67	14	-1533 +/- 19	528	-1005	2.86
25	2.79	14	-1580 +/- 3	526	-1054	2.29

* OCP values given +/- 1 standard deviation.

thermodynamics for oxidation of the silicon surface are less favorable (i.e. more energy is required to start the oxidation reaction). This is consistent with the general behavior of the system as predicted by the Nernst equation. As OH^-/H_2O is in equilibrium per equation {4}, in general, an increase in TMAH (OH^-) leads to a decrease in H_2O concentration. However, as H_2O is a reactant in equation {7}, this will shift OCP cathodically per the Nernst equation.

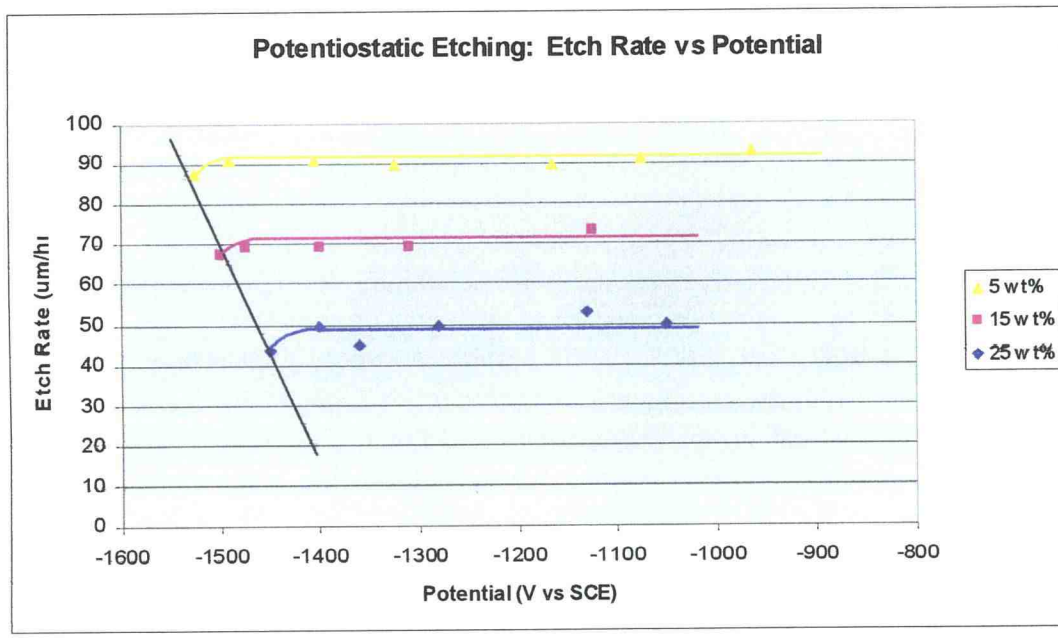


Figure 8: Etch Rates vs Potential

Similarly, PP shifts cathodically with increases in TMAH concentration. This PP shift is consistent across the entire concentration range, becoming more

negative with each increase in concentration. Shifts in PP are influenced both by system thermodynamics and kinetics. Within the OS, the silicon etch reaction is energetically favored over passivation, a balance that is reversed at potentials anodic of the PP. A detailed description of the kinetic factors influencing silicon passivation, however, is beyond the scope of this paper. Briefly, these factors include concentration of reactants and reaction products and associated thermodynamic equilibria, the availability of active reaction sites on the silicon surface (e.g. competitive adoption of silicon by hydroxyl groups and/or blocking of active sites by H_2 molecules), chelation and removal of product groups from the silicon surface (complexation), surface diffusion (both of silicon on wafer surface to active sites, and of electrolyte species to the reaction surface), as well as macroscopic mass-transfer effects.

POTENTIOSTATIC AND GALVANIC ELECTROLYSIS

Figure 8 shows the measured etch rate of wafer trenches in three TMAH concentrations when the reaction is driven by applied potential. For each concentration, the etch rate is lowest at OCP, but then increases moderately at positive deviations from equilibrium. With the application of a small anodic bias, steady state etching was achieved up to PP (e.g. wafers in 15 wt% TMAH achieved

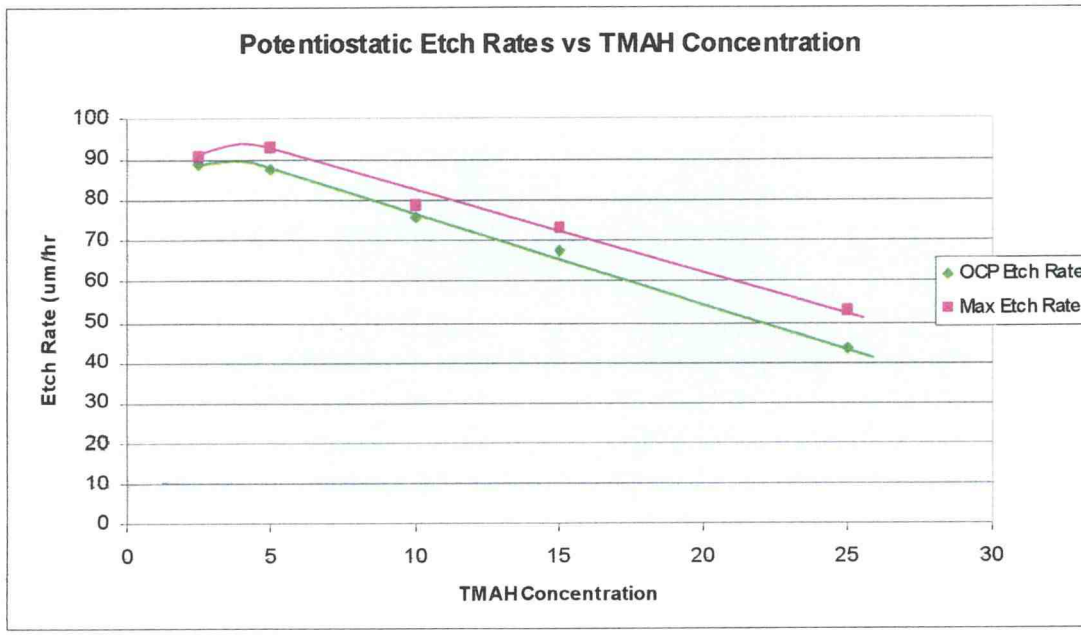


Figure 9: Potentiostatic Etch Rates vs TMAH Concentration

an etch rate of 67.7 um/hr at OCP and a maximum of 73.2 um/hr under bias.) The steady state potentiostatic etch rates and the OCP etch rates for the full range of TMAH concentrations investigated are shown in Figure 9. In general there appears to be a linear relationship between etch rate and concentration, with a maximum in etch rate observed at approximately 5 wt% TMAH (Note, the curves in Figure 9 are added to aid the eye but should not be interpreted as best fit representations; nor are error bars added). There are sources of minor variance in the etch rates, however, due to sample prep, efficiency of removal of native oxide and etch time. Given the difficulty in measuring these processing variances, the true accuracy of the etch

rates cannot be quantified. However, the linearity of the etch rate curves as shown in Figure 8 suggest that the combined variance is small. The maximum OCP etch rate at 5 wt% is consistent with published findings that also explored a range of TMAH concentrations [3, 10, 11, 13 – 15]. However, we were able achieve modest etch rate improvements across all TMAH concentrations with biased etching as an alternative to etching at OCP as shown by the red curve in Figure 9. The maximum etch rate for potentiostatic etching was also recorded with a 5 wt% bath. An applied potential of –965mV resulted in an etch rate of ~ 93 um/hr, approximately a 6.5% increase over the 88.5 um/hr measured at OCP. (This OCP value is comparable to results achieved by Tabata [3], who recorded an etch rate of approximately 84 um/hr at OCP and a 90°C bath temperature.) While maximum etch rate decreased with increasing TMAH concentration, the difference between maximum etch rate and OCP etch rate increased. That is, biased etching offers a larger improvement in etch rate at higher TMAH concentrations. At 25 wt% TMAH, the maximum vs. OCP etch rate is 52.7 um/hr compared to 43.3 um/hr, or a gain of 21.7%.

SEM images were taken of all wafers etched, and Figures 10 and 11 show trench features of wafers etched in 5 wt% TMAH, both at OCP and with potentiostatic and galvanostatic conditions. Undercut of the upper (100) surface is clearly visible and debris remains on several of the (110) surfaces. These images are representative of all the wafers etched, regardless of TMAH concentration, in

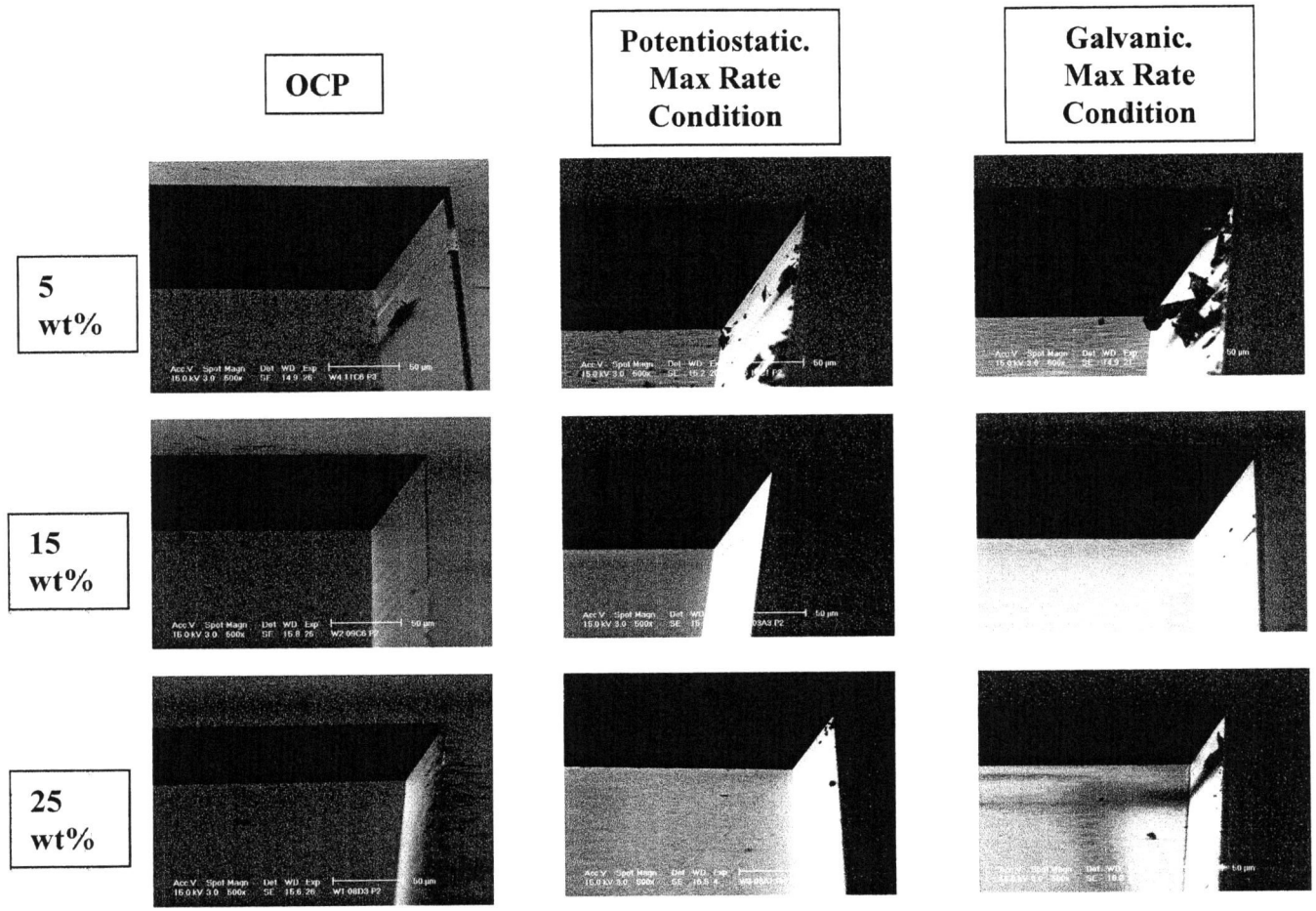


Figure 10: Representative SEM Images. Potentiostatic and Galvanic Etching in 3 TMAH Concentrations.

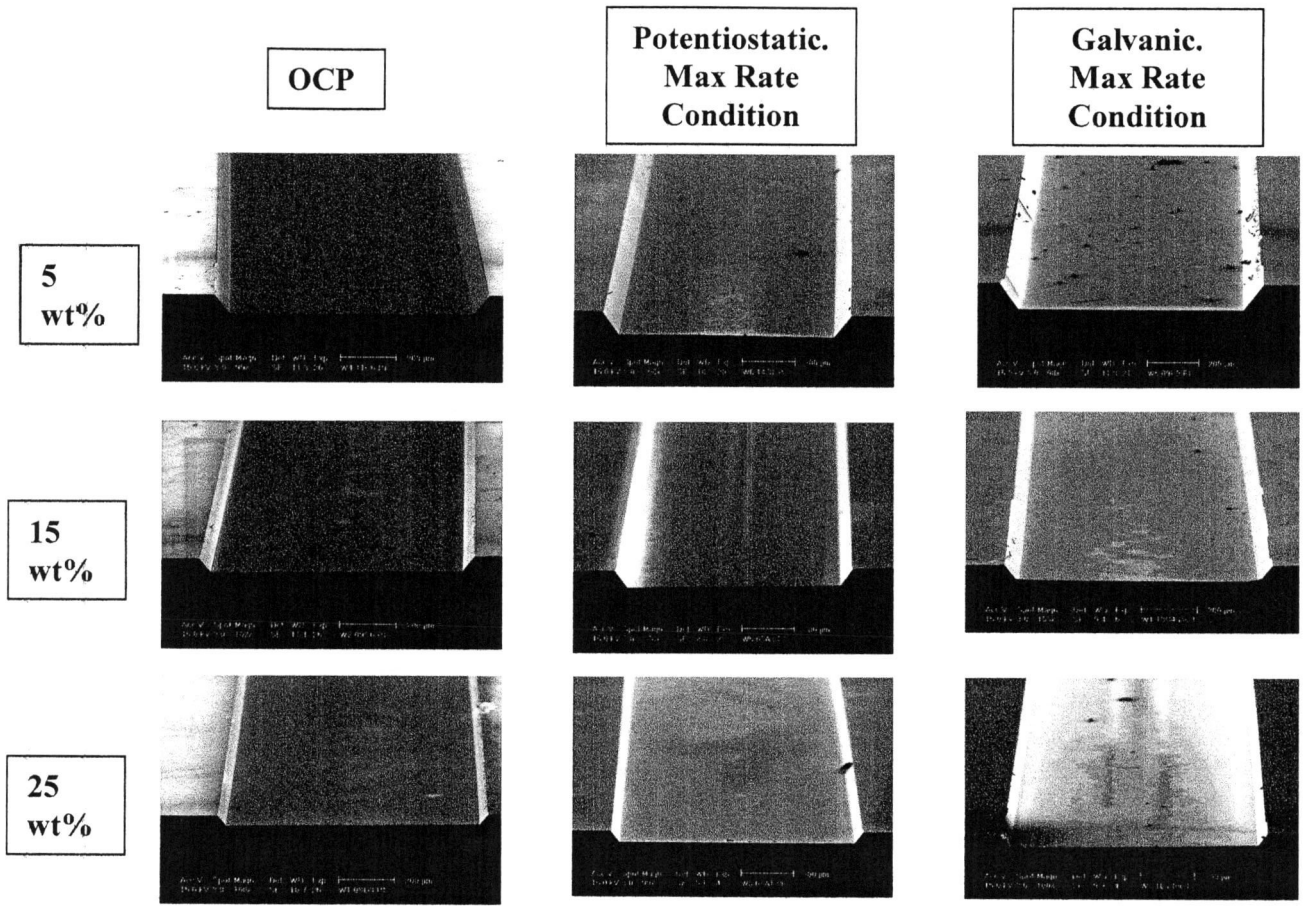


Figure 11: Representative SEM Images. Potentiostatic and Galvanic Etching in 3 TMAH Concentrations.

that the trenches etched at OCP show hillock formations on the etched (100) surfaces, whereas trenches etched with an applied bias lack hillock formations discernable with SEM. The 500X corner images in Figure 10 clearly show the increased etch depths achieved with potentiostatic or galvanostatic etching over etching at OCP. In agreement with published literature [3, 10, 12], we found

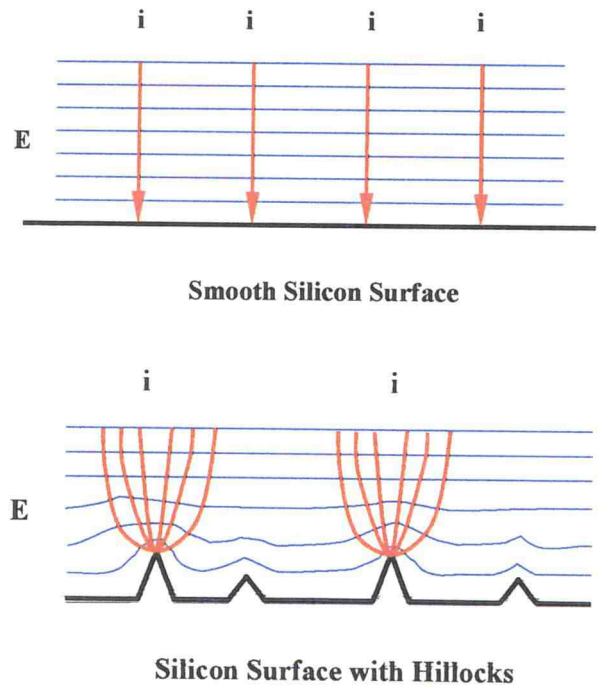


Figure 12: Wafer Surface Topography Exposure to Applied Current

hillock formations on the etched (100) surfaces of wafers etched at OCP, with size and density decreasing with increasing TMAH concentration. A detailed

discussion of hillock formation is beyond the scope of this investigation. However, published literature offers several theories. Schnakenberg [10] noted that wafer pre-treatment affects hillock formation. Wafer surfaces not free of native oxide incurred hillocks of greater size and density. He further proposes that hillocks form when the transfer of etch reaction products away from the solid-liquid interface is less than the rate of production of those products. Choi [12] also found that hillocks form when SiO_2 fails to be dissolved away. In addition, he found wafer defect signals in hillock formation -- annealing wafers prior to etching lowered hillock density. He proposes that this is due to the outdiffusing of interstitial oxygen atoms from the bulk silicon. As shown in Figure 10, wafers etched at 5 wt% TMAH had dense hillocks. Smoother surfaces were achieved by increasing [TMAH], with hillock-free surfaces apparent at concentrations of 25 wt%, albeit at a lower etch rate. Schnakenberg observed similar results and has related hillock formation to pH. The pH of his baths decreased with TMAH concentrations, with hillocks forming when the pH dropped below 13. For his experiments, this corresponded to a [TMAH] of approximately 20%. While we observed the same correlation between [TMAH] and hillock formation, we were unable to confirm Schnakenberg's pH values. Referring back to Table 1, we consistently measured pH values greater than 13.5 regardless of [TMAH]. This was consistent through several repours of the TMAH baths, and verified both by the Beckman 45 pH meter and sample submission for independent lab analysis.

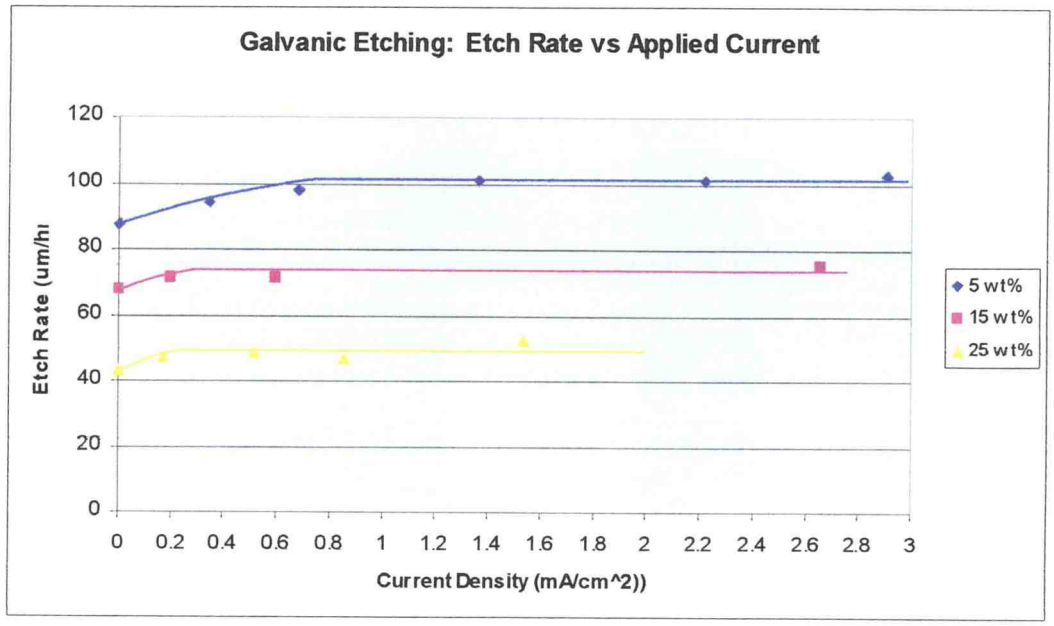


Figure 13: Etch Rates vs Applied Current

Regardless of [TMAH] and bath pH, however, we were able achieve hillock-free etch surfaces with biased etching. This observation is explained by the shape of the potential field and current distribution at the wafer surface, as illustrated in Figure 12. During etching, surface discontinuities, e.g. surface topography, receives more current locally than "low spots". It is favorable, electrochemically, for the hillock formations to minimize this potential, thus driving a faster reaction rate relative to the etch surface at a lower potential. This self-correcting etching enabled remarkably smooth and hillock-free etch surfaces.

Figure 13 shows the measured etch rate of wafer trenches achieved with galvanostatic etching. The abscissa has been converted to current density, with

each wafer having an exposed silicon surface area of ~ 29.25 cm^2. In general, galvanostatic etching results in the same trends as observed with potentiostatic etching. Etch rates greater than those at equilibrium were achieved with decreasing TMAH concentration. Similarly, applied current increased etch rates only moderately above those achieved at equilibrium, even upon continued increases in current. Referring to Figures 10 & 11, hillocks were observed on etched surfaces regardless of TMAH concentration when etched at equilibrium. The application of an applied current eliminated hillock formations and achieved etching rates similar to those achieved with applied potential.

ETCH RATE

Maximum etch rates for galvanostatic, potentiostatic and OCP etching by concentration are illustrated in Figure 14 as well as summarized in Table 2. Given

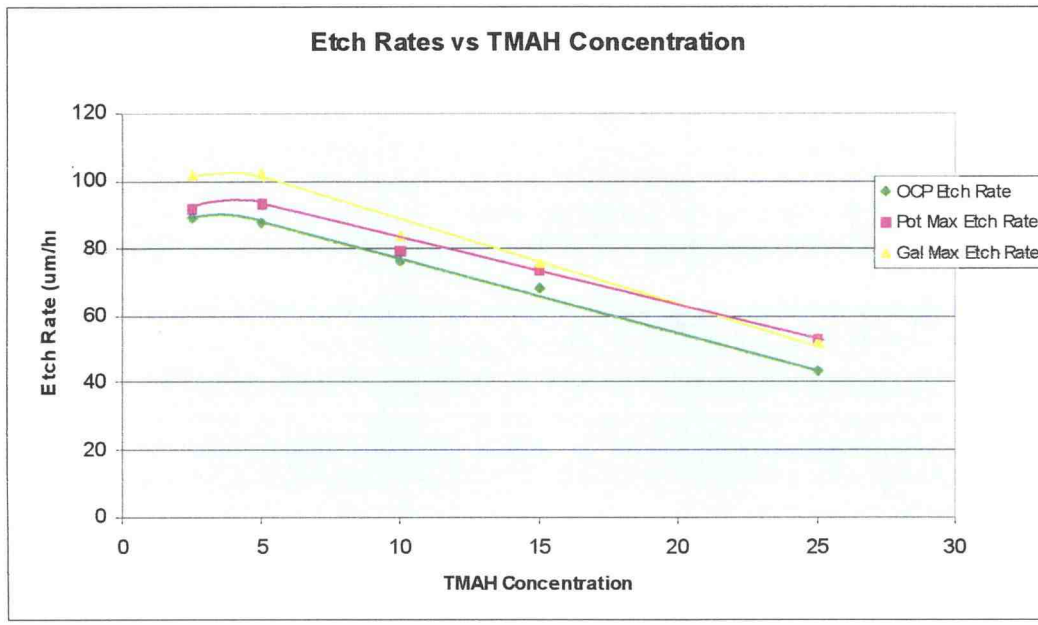


Figure 14: Combined Max Etch Rates vs TMAH Concentration

the variances inherent in etch rate measurements, minor differences between rates achieved with potentiostatic and galvanostatic etching will not be addressed here. Rather, it is observed that both potentiostatic and galvanostatic etching provide a modest increase in etch rate over those achieved etching at OCP at all concentrations. While the greatest percentage increase in etch rate between biased and OCP etching occurs at the 25 wt% TMAH , the maximum etch rate seems to

occur at TMAH concentrations very near 5 wt%. Indeed there is little correlation between the increase in etch rate and [TMAH]. The 5 wt% TMAH bath had the greatest OS (591 mV), yet did not show the etch rate increase achievable at 25 wt% TMAH with applied bias.

Table 2: Summary of Potentiostatic and Galvanic Etch Rates.

TMAH Conc.	OCP Etch Rate (um/hr)	Pot Max Etch Rate (um/hr)	% Difference Pot vs OCP	Gal Max Etch Rate (um/hr)	% Difference Gal vs OCP
2.5	88.7	91.1	2.71%	101.6	14.54%
5	87.5	93.1	6.40%	102.1	16.69%
10	75.8	78.8	3.96%	83.9	10.69%
15	67.7	73.2	8.12%	75.3	11.23%
25	43.3	52.7	21.71%	52.3	20.79%

In fact, the etch rate curves shown in Figures 8 & 13 for both potentiostatic and galvanostatic show evidence that the reactions were limited by additional factors. For example, all curves in Figure 8 increase dramatically from OCP, but then quickly stabilize at a steady state rate despite increases in potential. This behavior is characteristic of mass transfer limited reactions. This limitation was explored with a simple experiment on bath agitation speed. As detailed in the Experimental Section, etching baths were agitated by an external high-shear laboratory mixer at a low speed (~100 rpm). With this agitation speed, the maximum potentiostatic etch rate in 2.5 wt% TMAH of 91 um/hr was achieved, as

detailed in Table 2. As an experiment in wafer-scale mass transfer effects, a new 2.5 wt% TMAH bath was poured and the maximum etch rate at low agitation was remeasured to be 94 um/hr. When the mixer speed was increased to maximum (~1000 rpm), the maximum etch rate increased to 102 um/hr, a gain of 8.5%. However, this modest gain is not sufficient to fully explain the characteristics of the etching rate curves in Figure 8 & 13, and thus the limits on etch rate cannot be explained fully by mass transfer effects.

Table 3: Physical Data of wafers etched in 5 wt% TMAH with increasing [Si].

Wafer	Si Molarity (mol/l)	pH	Conductivity (mS/cm)
1	not detected	13.69	111.9
2	0.0686	13.67	92.3
3	0.6000	12.77	30.0

Limitations on etch rate have been commented on in published literature [10,12], but not explored in great detail. Schnakenberg proposes that etching of silicon occurs through a series of oxidation and chelation reactions in which the silicon surface is first oxidized and then chelated to form a product that can be dissolved away. Schnakenberg further suggests that these reaction combinations allow for a maximum etch rate at a concentration of ~ 5 wt% TMAH. Choi

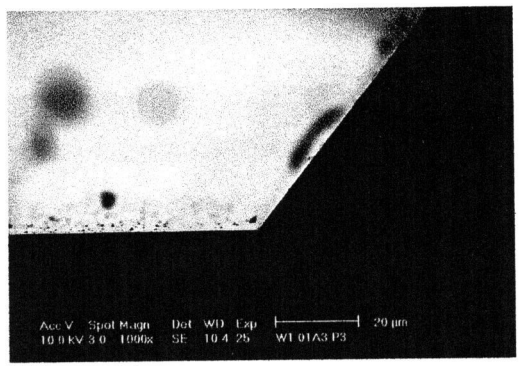
discusses oxidation and chelating reaction effects on hillock growth, which effect overall etch rate. Given these reports and our own observations, it is likely that etch rate is limited by a combination of kinetic, thermodynamic as well as mass transfer effects.

SILICON LOADING OF TMAH

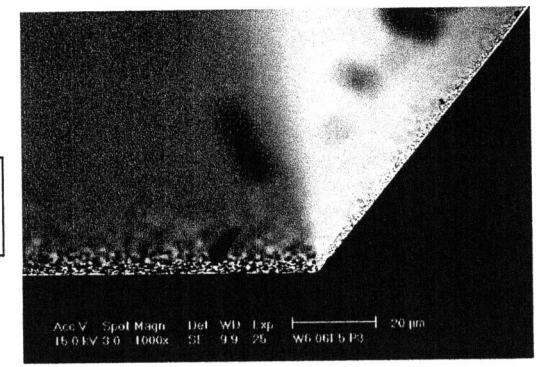
Etch rates of TMAH solutions with loaded silicon increase dramatically with the use of biased etching. Three wafers were etched at OCP in baths of different silicon loading levels as shown in Table 3. As the silicon molarity increased from 0.0 to 0.6 mol/liter, there is a drop in pH and Conductivity. A series of 1000x SEM images in Figure 15 show that the wafer etched in the bath with no silicon loading results in a (100) topography with scattered small hillocks. However, hillock size and density increase with silicon loading – indeed the (100) plane etched in 0.6M Si bath is dominated by hillocks.

Yet the growth of hillocks in silicon seasoned baths can be overcome with biased etching. Figure 16 shows SEM images of two (100) wafers from a uniform wafer lot etched in a 5 wt% TMAH solution with 0.6M silicon loading. Bath pH was measured at 12.43. The first wafer was etched at OCP and the resulting surface is heavily populated with hillocks. The bath conditions match all those as

0.000 M Si



0.0686 M Si



0.600 M Si

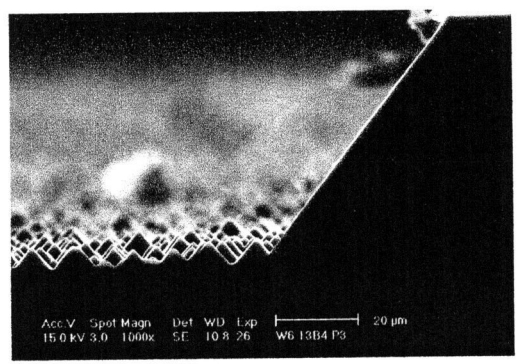


Figure 15: Trenches etched at OCP, 5 wt% TMAH. Evolution of Hillocks with increasing Silicon Concentration

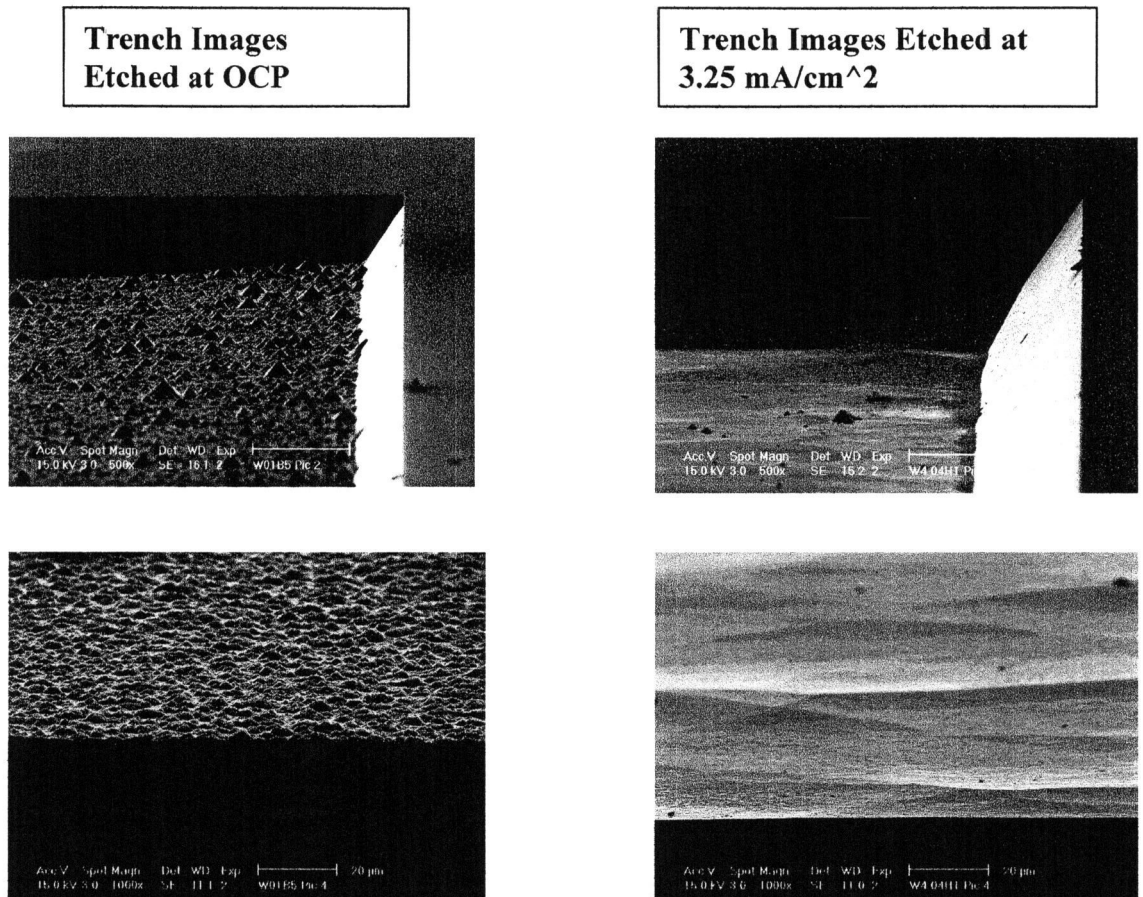


Figure 16: SEM Images from 5 wt% TMAH, 0.6M Si.

described by Schnakenberg, Tabata and Choi for promoting hillock growth (i.e. TMAH concentration is low and pH is below 13). However, when a second wafer was etched with an applied galvanic current in the same bath, the hillocks were eliminated. In addition, the etch rate increased from 58 um/hr at OCP to 95 um/hr

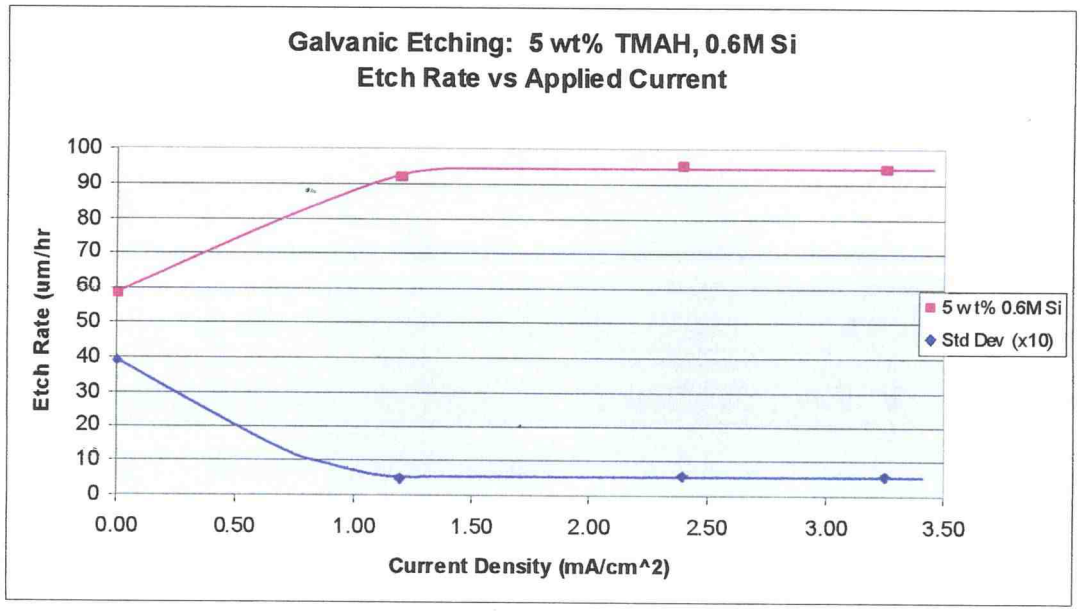


Figure 17: Etch Rates in Si Seasoned TMAH

with an applied current density of 2.25 mA/cm^2. Figure 17 shows this increase in etch rate across the full OS, with steady state etching a 63.8% increase in rate over those at OCP. The elimination of hillocks is shown graphically by the reduction in standard deviation of the etch surface measurements.

CONCLUSIONS

We have shown that potentiostatic and galvanostatic biased etching of silicon wafers in TMAH yields a moderate increase in etch rate over those rates achieved at equilibrium (OCP). Maximum etch rates appeared to be limited by mass transfer effects as well as kinetic factors. Further, biased etching eliminates the growth of hillocks on etching surfaces regardless of etchant pH, [TMAH] or silicon loading, resulting in highly smooth etching surfaces.

Increased etch rate and the elimination of hillocks through potentiostatic and galvanostatic etching has substantial micromachining, microfluidics and electronics implications. MEMS processing often relies on bulk wet-etching of silicon to form precise features and structures such as piezoresistive membranes, pressure transducers, and thermal inkjet printheads. The performance of micro-fluic devices often requires smooth sidewall and trench floors for precision. Improved etch surface morphology, etch rate, and rate process control will improve yield and quality. While silicon etching at OCP requires trading etch surface morphology and etch depth precision for etch rate, potentiostatic and galvanostatic etching allows for both increased etch rate and the elimination of hillocks regardless of [TMAH] or bath silicon concentration.

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