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Title: Design of Current-mode Track and Hold Circuits

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Terri S. Fiez

A differential current-mode track-and-hold (T/H) amplifier is used to sample an analog input signal. A new closed-loop current-mode architecture has been developed that overcomes the stability problems associated with closed-loop architectures. The T/H circuit has been fabricated in a 0.35-μm quad-metal, double-poly CMOS process. The measured total harmonic distortion (THD) is -81dB and -65dB with an input signal frequency of 100KHz and 10MHz, respectively. This is the best performance reported to date for a CMOS implementation.

Design of Current-mode Track and Hold Circuits

by

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Madhusudhan Chennam, Author

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DESIGN OF CURRENT-MODE TRACK AND HOLD CIRCUITS

1. INTRODUCTION

1.1. Sample and Hold Circuits

Processing of signals in the digital domain is easier and more efficient than processing analog signals; hence, it is desirable to convert analog signals into digital signals as early as possible. For many communication applications, this means both high speed and high resolution analog-to-digital conversion is required and this performance can not be achieved without the use of high linearity and high speed front end blocks. The sample-and-hold (S/H), the front end of analog-to-digital conversion, is a critical analog building block in many applications. The function of the S/H circuit is to sample the analog input value and hold it for a certain amount of time for subsequent signal processing. Figure 1.1 shows a simple S/H circuit.A S/H circuit consists of an input buffer, an electronic switch, a storage capacitor and an

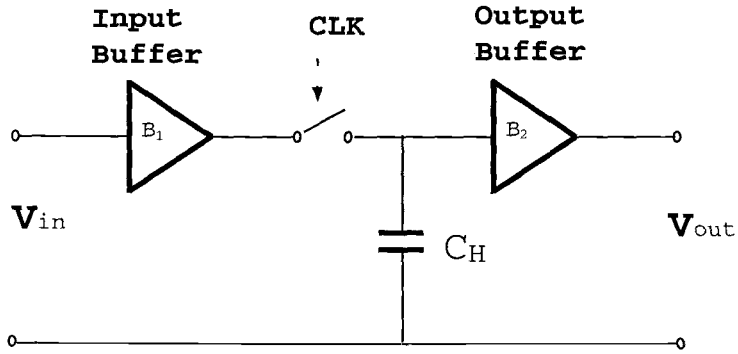

Figure 1.1. Simple sample and hold circuit.

output buffer. In the sample or acquisition mode, the switch is closed, allowing V_{out} to track the input voltage. In the hold mode, the switch is opened, isolating the storage capacitor from the input and V_{out} remains constant until the next sampling phase. The switching operation and transient currents drawn by C_H introduce noise at the input, often mandating the use of a front-end buffer. The output buffer is used to isolate the holding capacitor from the load. In practice, the nonidealities associated with the buffer and the sampling switch in Fig. 1.1 necessitate substantial added complexity to achieve a given set of performance specifications.

1.2. Drawbacks of CMOS S/H Circuits

Switches are usually implemented using either MOS devices or diodes. Since they are nonlinear devices, practical switches suffer from many nonidealities. MOS switch nonidealities are shown in Fig. 1.2 and include: charge injection (Q_{CH}), clock feedthrough, signal dependent charge injection ($\propto V_{DS}$), signal dependent switch on-resistance (R_{CH}) and switch noise [15]. Signal dependent charge injection and switch on-resistance increase harmonic distortion of the circuit. The clock feedthrough problem can be decreased by using a differential configuration. The charge injection, Q_{CH}, and the swith on-resistance, R_{CH}, respectively, are expressed by:

$$Q_{CH} = WLC_{ox}(V_{GS} - V_{TH}) \tag{1.1}$$

$$R_{CH} = \frac{1}{\mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})} \tag{1.2}$$

where W is the width of the device, L is the length of the device, μ is the mobility of the carriers (electrons or holes), C_{ox} is the gate capacitance per unit area, V_{GS} is

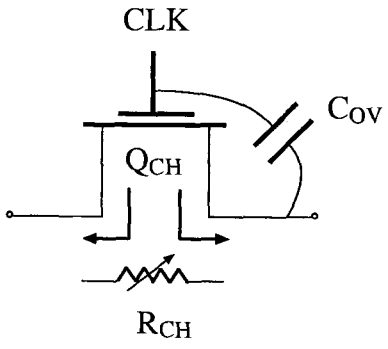

Figure 1.2. MOS switch with parasitics illustrating nonidealities.

the voltage between the gate and the source of the device and V_{TH} is the threshold voltage.

Traditionally, S/H circuits are designed in voltage-mode because most of the physical quantities measured are available in the form of voltage. In voltage-mode, the input voltage is sampled at discrete times and held constant until the next sampling instant. These circuits are relatively simple to design, dissipate low power and give highly linear outputs at low to medium speeds [4], [6], [8], [14], [13]. At high speeds, large W/L ratios for the switch increases signal dependent charge injection and degrades linearity of the circuit. Thus, accuracy of open-loop circuits reduces at high speeds. Closed-loop techniques are often employed when distortion is limiting overall perfomance. However, often closed-loop approaches require special considerations to obtain stability especially at high speed applications [1], [2]. To achieve high performance even when low voltage, submicron processes are deployed, alternative approaches of designing S/H circuits are needed. One such alternative is to use a current-mode architecture where the input current is sampled instead of

input voltage. The current-mode approach offers several advantages like minimized switch-induced distortion and reduced sesitivity to parasitic capacitance [5], [6], and can achieve high speed and resolution. The rest of the thesis is arranged as follows. Chapter 2 describes various current-mode T/H architectures and a new approach to achieve high speed and resolution. Chapter 3 presents the implementation and design issues. The experimental results are given in chapter 4 and finally chapter 5 concludes the thesis.

2. CURRENT-MODE ARCHITECTURES

2.1. Open Loop Architecture

Current-mode signal processing has been proposed as an alternative to the more conventional voltage-mode techniques [6], [8], [14]. Current-mode data conversion systems require current input signals and current output sampling circuits. However, even in the case of current-mode circuits, the signal is stored as a voltage rather than a current because capacitors are far easier to fabricate than inductors and require less chip area. Thus, in these architectures, the input current must first be converted to a voltage so that it can be stored, and the stored voltage must be subsequently converted to an output current. Figure 2.1 shows an open-loop architecture of a current-mode S/H circuit.

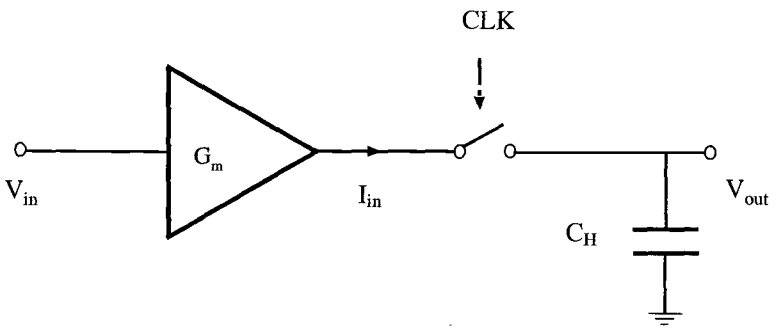

Figure 2.1. Open-loop current-mode S/H architecture.

The input voltage, V_{in}, is converted into a current using a transconductor (G_m). The transconductor output current is used to charge a holding capacitor

(C_H) when the switch is closed. The holding capacitor voltage is held constant when the switch is closed and thus further processing can take place. The input transconductor is a very important block in any current-mode architecture. The linearity of the input transconductor and the switch determine the linearity of the S/H circuit.

Open-loop current-mode circuits are very simple and they are unconditionally stable because they do not use global feedback. They can therefore be designed for high-speed operation. This architecture has the advantage of having only one switch which decreases the nonideal effects like charge injection, clock feedthrough and switch on-resistance. However, since there is no global feedback, these circuits are sensitive to switch on-resistances. The expression for V_{out} is given by:

$$V_{out}[nT] = \frac{-1}{C_H} \int_{nT-\tau}^{nT} G_{min} v_{in} \sin(\omega_{in} t) dt \tag{2.1}$$

where τ is the integration time and ω_{in} is the input radian frequency and G_{min} is the input transconductance.

V_{out} can be expressed in closed form as:

$$V_{out}[nT] = \frac{2G_{min}V_{in}}{C_H\omega_{in}} \sin(\frac{\omega_{in}\tau}{2}) \sin[\omega_{in}(nT - \frac{\tau}{2})] \tag{2.2}$$

The integration time, τ, causes a gain term, which is given by $\sin(\frac{\omega_{in}\tau}{2})$, and a phase term, $\frac{\omega_{in}\tau}{2}$. The voltage gain, V_{out}/V_{in}, is frequency dependent and varies as one over the frequency.

The shortcoming of this architecture is that it is very sensitive to the aperture jitter of the clock because the amount of charge accumulated on the holding capacitor

is directly proportional to the length of time the switch is on. Jitter, in turn increases the noise floor of the output signal. If σ_τ is the *rms* value of the jitter, then $V_{out}[n]$ is obtained by substituting $\tau + \sigma_\tau$ for τ in (2.2), this results in:

$$V_{jitter}[nT] = \frac{2G_{min}V_{in}}{C_H\omega_{in}} \sin(\frac{\omega_{in}(\sigma_\tau + \tau)}{2}) \sin[\omega_{in}(nT - \frac{\sigma_\tau + \tau}{2})] \tag{2.3}$$

The error in V_{out} is the difference between the ideal output voltage and the output voltage with jitter, i.e.,

$$V_{err}[nT] = V_{out}[nT] - V_{jitter}[nT] \tag{2.4}$$

Substituting (2.3) into (2.4), we obtain:

$$V_{err}[nT] = \frac{2G_{min}V_{in}\sigma_\tau}{C_H\omega_{in}} \sin[\omega_{in}(nT - \tau)] \tag{2.5}$$

From (2.5), we can see that the error or noise floor of the output spectrum is proportional to the *rms value* of the jitter. Consequently, the signal-to-noise-plus-distortion ratio (SNDR) of V_{out} is limited by the noise rather than by harmonic distortion at high clock frequencies. The total noise power can be expressed in terms of the input and clock frequencies and it is:

$$P_{err} \propto 4\sigma_\tau^2 f_{clk}^2 (1 + \frac{f_{in}^2}{4f_{clk}^2}) \tag{2.6}$$

where f_{clk} is the clock frequency and f_{in} is the input frequency.

The noise power, P_{err}, is composed of a signal frequency dependent term and a signal frequency independent (DC) term. Unlike voltage-mode cases, jitter degrades the SNR even at low input signal frequencies. Hence, this architecture requires very high precision clocks to obtain reasonable values of SNR. To reduce

sensitivity to aperture jitter, alternative architectures must be considered. Closed-loop current-mode S/H architectures are one way of achieving low sensitivity to jitter and at the same time high linearity.

2.2. Closed-Loop Architecture

Using a closed-loop architecture improves the performance of current-mode S/H circuits because of reduced sensitivity to jitter and suppression of the non-idealities by the loop gain of the circuit [5] [6]. A block diagram of a closed loop architecture is shown in Fig. 2.2. The major difference between the open loop and

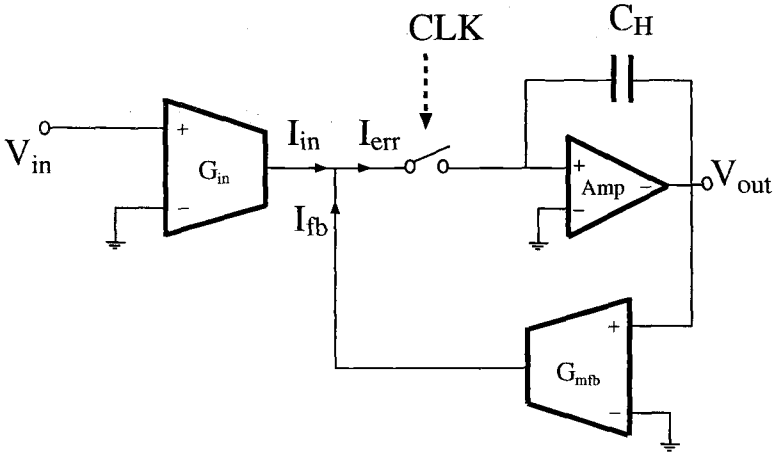

Figure 2.2. Closed -oop current-mode architecture.

closed loop architectures is the feedback transconductor which senses the output voltage and generates a feedback current. The input transconductor, G_{min}, generates a current, I_{in}, proportional to the input voltage. The feedback transconductor,

G_{mfb}, generates a current, I_{fb}, proportinal to output voltage. I_{in} and I_{fb} sum together to produce an error current, I_{err}. This error current charges the holding capacitor when the switch is on. When the output settles, I_{err} is zero and the voltage across the drain and source of the switch (V_{ds}) is zero. This removes the signal dependent charge injection and increases the total harmonic distortion of the circuit. I_{err} and the settling time (τ_c) of the output are given by:

$$settling\ time = \tau_c = \frac{C_H}{G_{mfb}} \tag{2.7}$$

$$I_{err} \propto I_{in} e^{\frac{-t}{\tau_c}} \tag{2.8}$$

The error current exponentially decreases to zero and if the switch turns off when the error current is zero, the errors introduced by the switch are negligible.

The time domain expression for V_{out} is given by :

$$V_{out}[nT] = \frac{-1}{C_H} \int_{nT-\tau}^{nT} G_{min} v_{in} e^{\frac{-t}{\tau_c}} \sin(\omega_{in} t) dt \tag{2.9}$$

and the closed form expression for V_{out} is:

$$V_{out}[nT] = \frac{G_{min} V_{in}}{C_H \sqrt{\frac{1}{\tau_c^2} + \omega_{in}^2}} [\sin(\omega_{in} nT - \theta)] - e^{-\frac{\tau}{\tau_c}} \sin(\omega_{in}(nT - \tau) - \theta)] \tag{2.10}$$

where θ is given by

$$\tan(\theta) = \omega_{in} \tau_c \tag{2.11}$$

To achieve better settling, a very small value of τ_c is required, necessitating either a smaller holding capacitor (C_H) or a higher feedback transconductance, G_{mfb},

value. However, increasing the feedback transconductance will increase the current consumption and thus the overall power dissipation. Additionally, the value of C_H is set by the thermal noise and linearity requirements of the circuit. Stringent linearity requirements force the value of C_H to be quite high and a very high value of G_{mfb} is needed for high closed-loop bandwidth.

DC gain of the configuration is G_{min}/G_{mfb} and it has a single pole roll-off characterstic with a pole located at G_{mfb}/C_H. The frequency dependent output is expressed as:

$$\frac{V_{out}}{V_{in}} = \frac{\frac{G_{min}}{G_{mfb}}}{(1 + \frac{sC_H}{G_{mfb}})} \tag{2.12}$$

The main challenge in the design is achieving a very high bandwidth closed-loop S/H circuit to reduce the effect of aperture jitter and signal dependent charge injection of the switch. For high bandwidth circuits, the sensitivity to jitter approaches that of voltage-mode circuits. Closed-loop architectures have less charge injection because fewer switches are used in the design, and the non-linear effects of switch on-resistance are reduced by loop gain. Using a differential configuration further reduces clock feedthrough. Thus, highly linear S/H circuits can be obtained, provided very linear input transconductors are designed. Another advantage of this architecture is that only two clock phases are needed. Reducing the number of clock phases removes many problems associated with routing clock signals. The closed-loop configuration retains the good qualities of the open-loop architecture and removes many of its disadvantages at the expense of extra power dissipation. One challenge in designing the closed-loop current-mode architecture is obtaining stable operation. The parasitic poles of the amplifier and the feedback transconductor between the input,

I_{in}, and feedback, I_{fb}, signals cause a phase shift of I_{fb} from I_{in}. Reducing these parasitic poles for high speed and stable operation is critical.

2.3. Improved Closed-Loop Architecture

To create a wideband architecture, phase correction techniques can be employed. The architecture proposed to correct stability problems faced by the closed-loop wideband T/H circuits is shown in Fig. 2.3. This circuit contains the additional elements: a transconductor (G_{mff}) and a phase shifter.

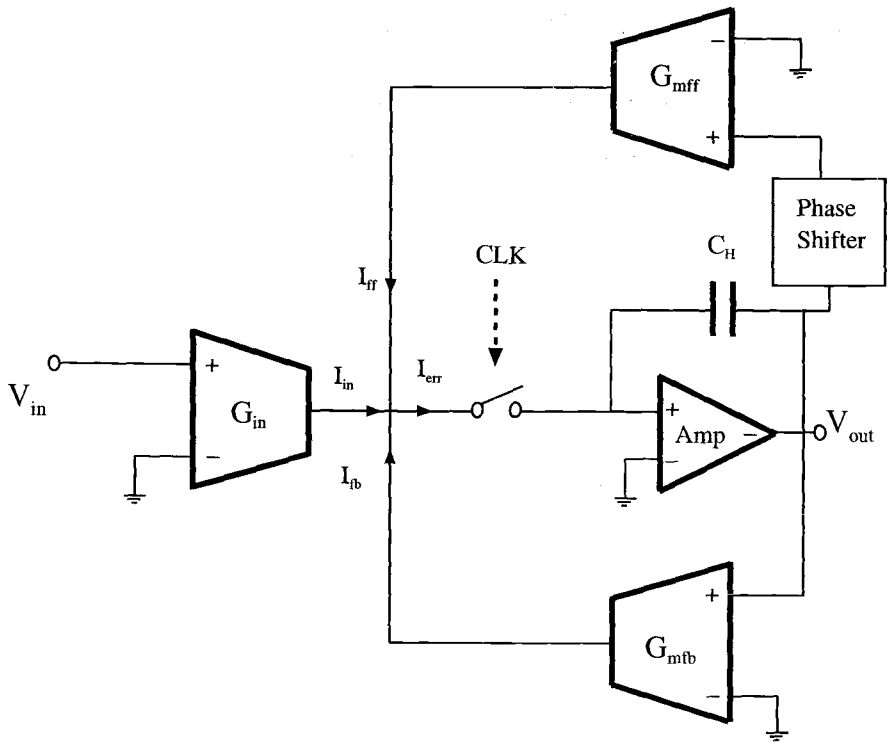

Figure 2.3. Improved closed-loop current-mode architecture.

The phase shifter senses V_{out} and generates a delayed version of the same. The transconductor G_{mff} senses the output of the phase shifter and generates a feedforward current (I_{ff}) which is used to increase the phase margin of the feedback signal. I_{in}, I_{fb} and I_{ff} sum together to produce I_{err}. I_{err} then charges the holding capacitor when the switch is on. In this modified architecture, the effective transconductance, G_{meff}, of the feedback path is given by the vector sum of G_{mfb} and G_{mff}:

$$G_{meff} = \sqrt{G_{mfb}^2 + G_{mfb}^2 + 2G_{mfb}G_{mff}\cos\phi} \tag{2.13}$$

where ϕ is the phase difference between them.

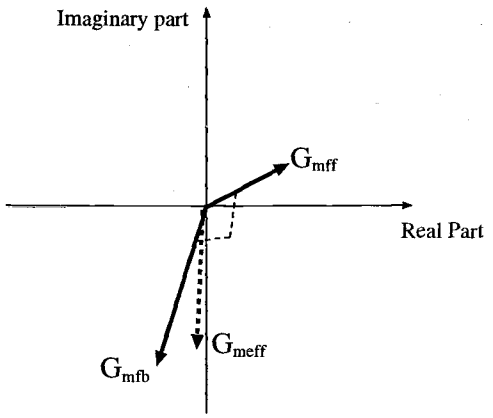

Figure 2.4. Graphical view of effective transconductance.

The phasor diagram is shown in Fig. 2.4. The phase shift of G_{meff} from G_{min}, is smaller than that of G_{mfb}. Thus, this architecture is more stable than the standard closed-loop architecture. However, the magnitude of G_{meff} is smaller than the magnitude of G_{mfb}, and so the current into the feeback transconductor must be

increased to obtain higher values of G_{meff}. The voltage gain is now a function of G_{meff} rather than G_{mfb}:

$$\frac{V_{out}}{V_{in}} = \frac{\frac{G_{min}}{G_{meff}}}{(1 + \frac{sC_H}{G_{meff}})} \tag{2.14}$$

Expressions for the settling time, τ_c, is also determined by G_{meff} and it is:

$$settling\ time = \tau_c = \frac{C_H}{G_{meff}} \tag{2.15}$$

The time domain expression for V_{out} is given by:

$$V_{out}[nT] = \frac{-1}{C_H} \int_{nT-\tau}^{nT} G_{min} v_{in} e^{\frac{-t}{\tau_c}} \sin(\omega_{in} t) dt \tag{2.16}$$

where τ is the integration time and ω_{in} is the radian input frequency. The closed form equation for V_{out} is given by:

$$V_{out}[nT] = \frac{G_{min} V_{in}}{C_H \sqrt{\frac{1}{\tau_c^2} + \omega_{in}^2}} [\sin(\omega_{in} nT - \theta)] - e^{-\frac{\tau}{\tau_c}} \sin(\omega_{in}(nT - \tau) - \theta)] \tag{2.17}$$

where θ is given by

$$\tan(\theta) = \omega_{in} \tau_c \tag{2.18}$$

To determine the effect of the clock jitter on V_{out}, we substitute $\sigma_\tau + \tau$ for τ and obtain:

$$V_{jitter}[nT] = \frac{G_{min} V_{in}}{C_H \sqrt{\frac{1}{\tau_c^2} + \omega_{in}^2}} [\sin(\omega_{in} nT - \theta)] - e^{-\frac{\tau + \sigma_\tau}{\tau_c}} \sin(\omega_{in}(nT - (\tau + \sigma_\tau) - \theta))] \tag{2.19}$$

The error in the output voltage due to jitter is given by:

$$V_{error}[nT] = \frac{G_{min}V_{in}}{C_H}\frac{1}{\sqrt{\frac{1}{\tau_c^2}+\omega_{in}^2}}e^{-\frac{\tau}{\tau_c}}[e^{-\frac{\sigma_\tau}{\tau_c}}\sin(\omega_{in}(nT-\tau-\sigma_\tau)-\theta)) - \sin(\omega_{in}(nT-\tau)-\theta)] \quad (2.20)$$

Since $e^{\frac{-\sigma_\tau}{\tau_c}}$ is nearly equal to 1 for practical values of τ_c and σ_τ, (2.20) can be rewritten as:

$$V_{error}[nT] = \frac{G_{min}V_{in}\omega_{in}\sigma_\tau}{2C_H}\frac{1}{\sqrt{\frac{1}{\tau_c^2}+\omega_{in}^2}}e^{-\frac{\tau}{\tau_c}}\cos[\omega_{in}(nT-\tau-\frac{\sigma_\tau}{2})-\theta] \quad (2.21)$$

Small values of τ_c will significantly reduce the effect of jitter. The power of the error signal is:

$$P_{err} \propto 4\sigma_\tau^2 f_{clk}^2(e^{-\frac{2\tau}{\tau_c}}+\frac{f_{in}^2}{4f_{clk}^2}) \quad (2.22)$$

where f_{clk} is clock frequency and f_{in} is input frequency. From (2.22), we see that the effect of signal independent jitter is reduced by an exponential factor compared to open-loop case. For lower clock frequencies, f_{clk}, the effect of jitter is small. For small values of τ_c, the noise power, P_{err}, proportional to $\sigma_\tau^2\omega_{in}^2$. Thus, high linearity and a low noise floor can be achieved if the circuit is designed for high closed-loop bandwidth. The linearity of this architecture is limited by the linearity of input transconductor, G_{min}, the feedback transconductor, G_{mfb}, the feedforward transconductor, G_{mff}, and the phase shifter. Because of the feedforward path, linearity at high frequencies is increased at the expense of reduced linearity at low frequencies and increased power dissipation.

3. DESIGN AND IMPLEMENTATION OF THE TRACK AND HOLD STAGE

3.1. Transconductor Design

The transconductor is a critical building block of any current-mode circuit. The linearity of the output depends heavily on the transconductor linearity. Thus, designing the transconductor is a critical part of designing the current-mode T/H circuits. Resistors, which are used to convert voltages into currents, are important elements of transconductors [3], [12], [11]. Figure 3.1 shows the block diagram of the input transconductor. Input resistors R_{ip} and R_{in} are used to convert the input voltage, V_i, into a current. Negative current feedback is provided by a high bandwidth amplifier. The input terminals of the amplifier are maintained at virtual ground, provided the loop gain is sufficiently high. This provides highly linear transconductances which are proportional to $\frac{1}{R_i}$.

Figure 3.2 shows the schematic of the transconductor. R_{in} and R_{ip} are input resistors and are choosen to have a value of 2kΩs each. This value reduces the thermal noise of the resistance and increases the transconductance, G_m, value. The source degeneration resistor, R_S, increases the linearity of the output current by providing local current feedback. R_s also decreases the effect of mismatches in the input resistors and the mismatch in the theshold voltages of the input transistors by increasing impedance seen at the source of M_1 from $\frac{1}{g_{m2}}$ to approximately $R_s+\frac{1}{g_{m2}}$, where g_{m2} is the transconductance of M_2. The capacitor C_{ff} provides a feedforward path and increases the phase margin of the feedback signal by introducing a zero in the frequency response. The threshold voltage mismatches for simulation are described in [7].

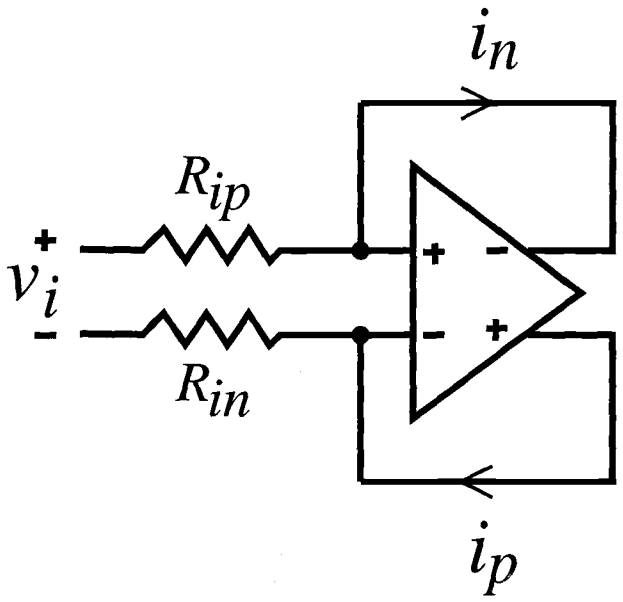

Figure 3.1. Block diagram of transconductor.

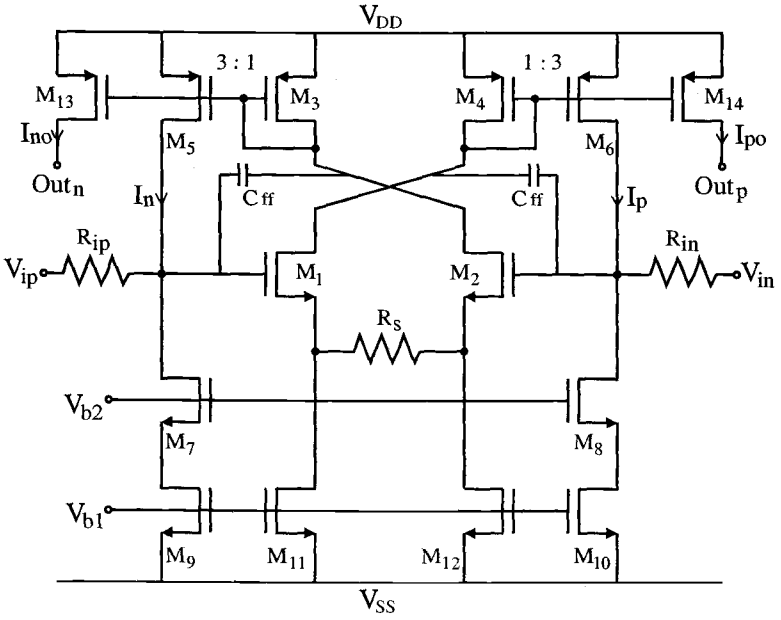

Figure 3.2. Schematic of input transconductor.

Transistors M_{13} and M_{14} source the output current. The minimum channel length for the diode-connected PMOS transistors (M_3 and M_4 in the schematic) is avoided for better current matching at the expense of decreased f_T. Using this configuration, high bandwidth and high linearity are achieved in the output current. Figure 3.3 shows simulated spectrum of the output current when a 20MHz input voltage signal is applied.

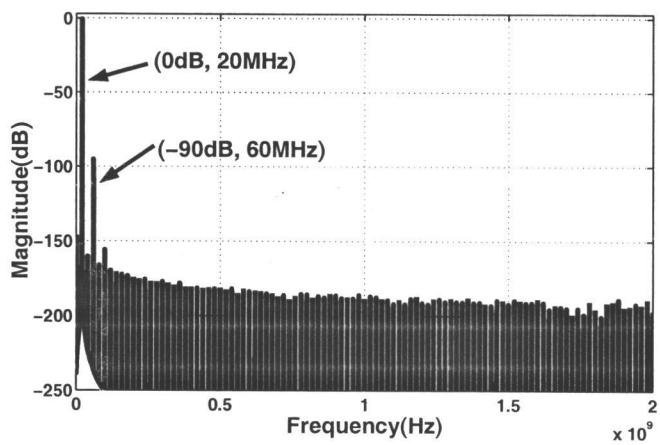

Figure 3.3. Spectrum of the output current of the transconductor with a 20MHz input signal.

Since the linearity of the T/H circuit depends both on the linearity of the input signal and that of the feedback signal, wideband and very linear feedback and feedforward transconductors are required. PMOS input transistors (M_1 and M_2) are used for the feedback and feedforward transconductors instead of NMOS input transistors so that the output stage DC currents can be shared. The schematic is shown in Fig. 3.4. Diode connected NMOS transistors (M_3 and M_4) are used

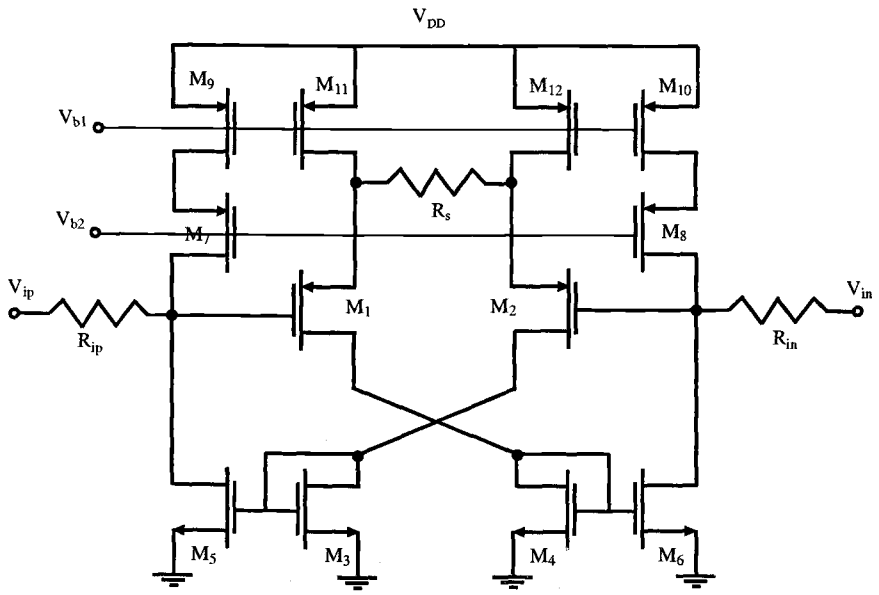

Figure 3.4. Schematic of feedback and feedforward transconductors.

to generate the feedback current. Since the NMOS transistors have f_T values 4 or 5 times greater than PMOS transistors, achieving stability is not difficult when compared to the input transconductor. Hence, a feedforward capacitor, C_{ff}, is not required for achieving stability.

3.2. Phase and Level Shifter

Another important block in the improved current-mode architecture is the phase shifter. A very linear phase shifter is needed since it is in the main signal path. Phase shifting is achieved using poly resistors and poly-poly capacitors. MOS resistors are avoided because they are not linear and the resistance value depends on the voltage across the drain-source terminals. Figure 3.5 shows the schematic of

the phase shifter. This serves the dual purpose of phase and DC level shifting. V_{outn}

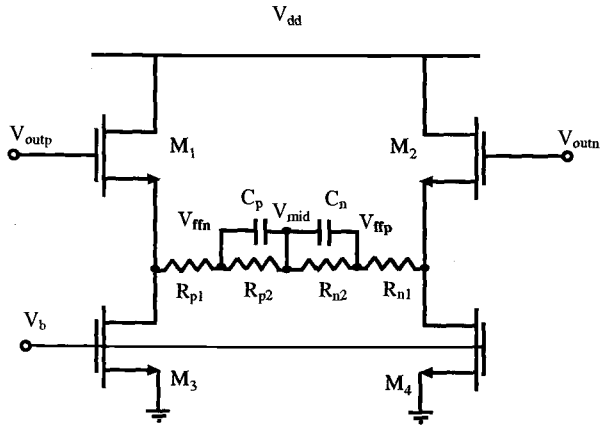

Figure 3.5. Schematic of phase and level shifter.

and V_{outp} are the actual outputs of the T/H circuit. V_{ffp} and V_{ffn} are the inputs to the feedforward transconductor. R_{p1}, R_{p2}, R_{n1}, R_{n2}, C_p and C_n are used for phase shifting V_{out}. If the resistors and capacitors are matched, then V_{mid} acts as a virtual ground and there is no DC power dissipation in the resistors. The linearity of V_{fb} and V_{ff} determines the linearity of the feedback current. To obtain highly linear V_{fb} and V_{ff}, either a high value of M_1 and M_2 transconductances or high value resistors are needed. For 4kΩs resistors and a 6mA current, low distortion output signals are obtained.

3.3. Main Amplifier and CMFB

Figure 3.6 shows the schematic of the amplifier. Simulations show that this current-mode architecture requires high bandwidth and is more sensitive to the unity

gain bandwidth of the amplifier than its DC gain. A simple op amp architecture is therefore choosen to achieve high bandwidth. The gain and phase response of the amplifier are shown in Figs. 3.7 and 3.8. A DC gain of 42dB and unity gain

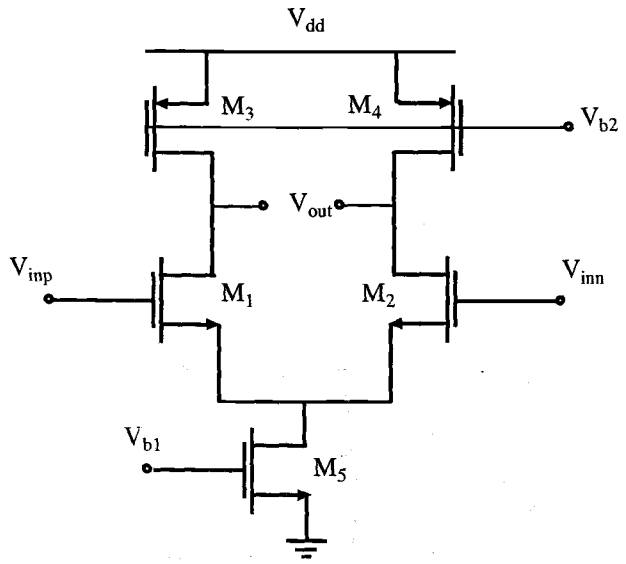

Figure 3.6. Schematic of main amplifier.

bandwidth of 1.1GHz with 90^o phase margin are obtained. The amplifier requires a common-mode feedback network (CMFB) to set the DC output voltage. Continuous-time CMFB is used so that there are no charge injection problems.

The CMFB circuit used here is shown in Fig. 3.9. This circuit amplifies the difference between the average value of the differential outputs (V_{outp} and V_{outn}) and the reference voltage (V_{cm}). The amplified voltage is fed into the main amplifier. The first stage of this circuit is designed to operate over a wide input voltage swing and has a bandwidth of order of f_T. The gain of the first stage is kept low to avoid

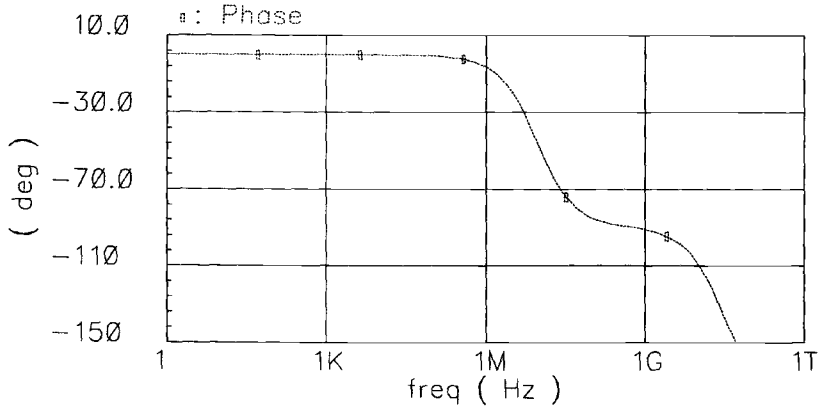

Figure 3.7. Phase response of op amp.

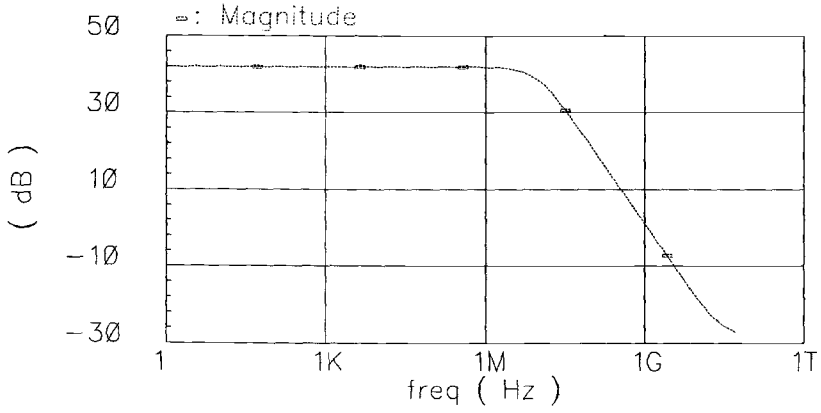

Figure 3.8. Gain responses of op amp.

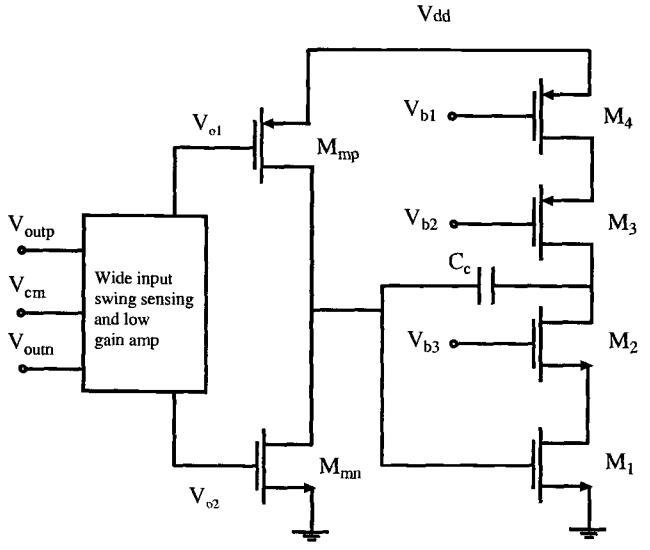

Figure 3.9. Schematic of CMFB circuit.

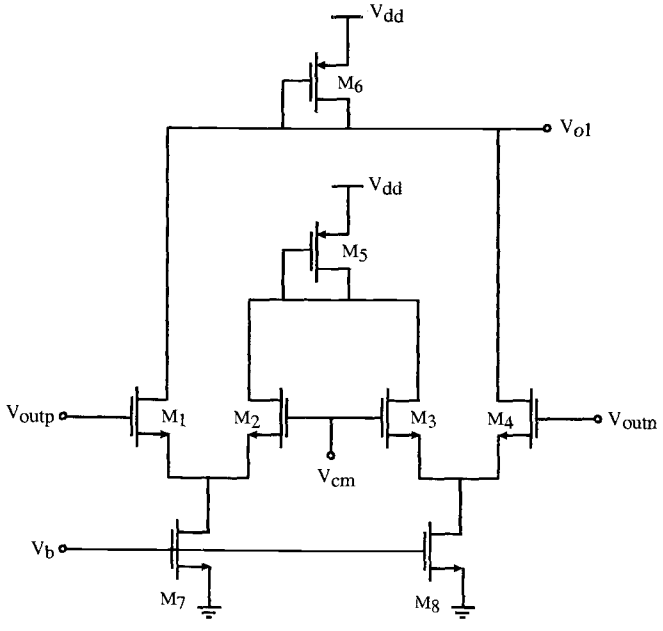

Figure 3.10. Schematic of the first stage of the CMFB circuit.

saturation of the output. The schematic of the first stage is shown in Fig. 3.10. The differential output voltage of the amplifier is applied to the differential pairs so that the common-mode voltage is generated. Figure 3.9 generates the voltage V_{o1} and a circuit with the same configuration but with all NMOS devices replaced with PMOS devices and vice versa is used to generate V_{o2}. These two circuits produce DC output voltages that allow for maximum voltage swing. By applying the common-mode voltage to both M_{mn} and M_{mp} in Fig. 3.9, the effective g_m of this amplifier is increased by approximately a factor of 2 since g_{meff} is equal to $g_{mnp}+g_{mmn}$. As a result of an increased transconductance, the bandwidth of the overall CMFB circuit is also increased. This circuit uses a Miller capacitor (C_c) for compensation and has a DC gain of 64dB with 200MHz unity-gain bandwidth and 60 degrees phase margin. The value of C_c is small compared to the value of the load capacitance. Thus, loading due to C_c is negligible.

3.4. Current steering circuit

The circuit in Fig. 3.11 steers the current into the holding capacitor when the clock is high and then sinks it when the clock is low. The bottom half of the circuit (M_1 and M_2) is the same as the output stage of the feedback transconductor and generates I_{fb}. I_{in} is the current generated by the input transconductor. Since the output stage of the input transconductor is a PMOS transistor, the DC current of the output stages of the input and feedback transconductors can be shared. The output stages are connected to a low impedance node, in this case the source of the NMOS trasistor. The node that is connected to the switches is a high impedance node which means a common-mode feedback circuit is needed to set the DC voltages.

The common-mode feedback circuit is shown in Fig. 3.12. Transistors M_2 and M_3 generate the common-mode error signal which is mirrored to the output nodes (S_n and S_p) by the PMOS current mirror M_7. Since the nodes S_1 and S_2 are in the main signal path, this circuit should operate at high speeds. The power dissipation of the circuit is 20mW.

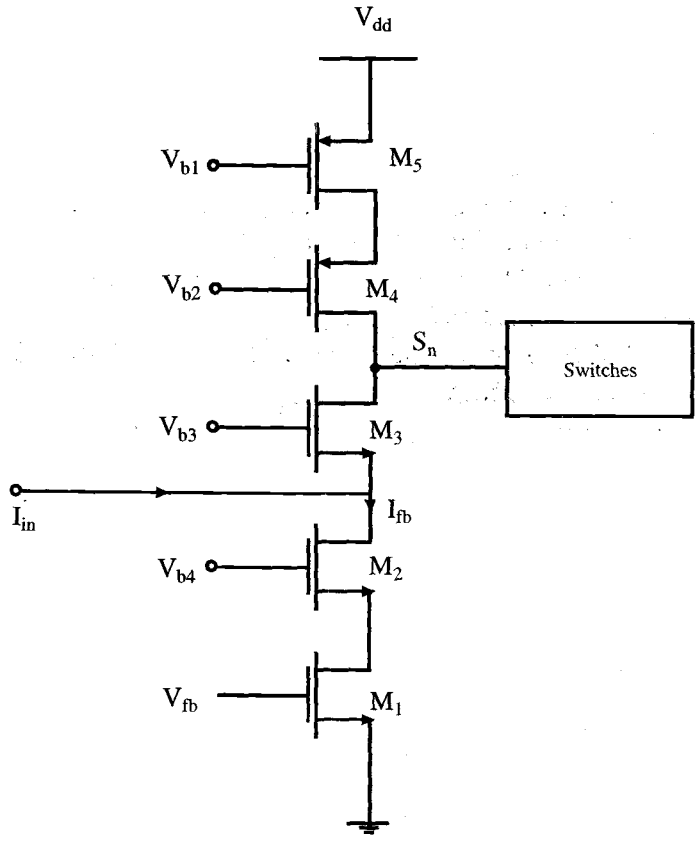

Figure 3.11. Current steering circuit.

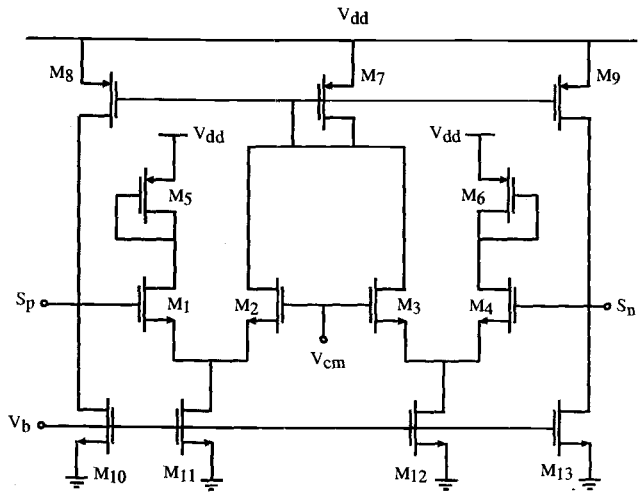

Figure 3.12. Common-mode feedback circuit

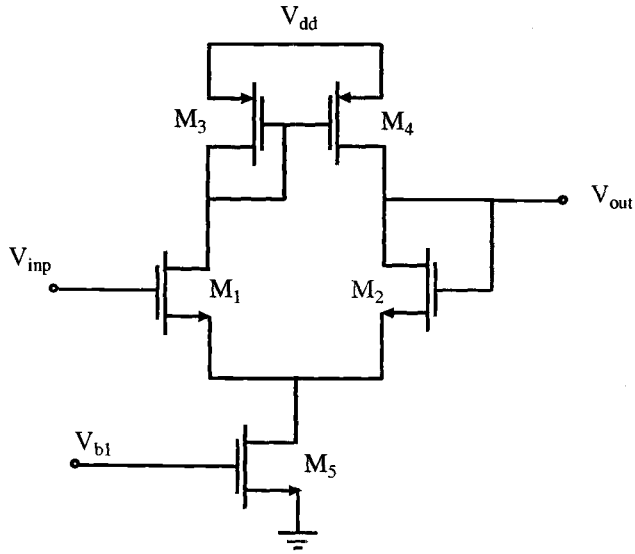

Figure 3.13. Unity Gain Buffer

3.5. Output Buffers

The output of the main amplifier is a high impedance node. In order to drive a low off-chip impedance, the outputs of the two channels of the T/H circuit are buffered. A unity-gain buffer is used to do this. Simulations show that the buffer has a THD of -90dB at 10MHz with a 0.7Vpp input signal and 3.3V power supply. It can drive a load as small as 300Ωs load. The schematic of unity gain buffer is shown in Fig. 3.13.

4. MEASUREMENTS

The differential closed-loop current-mode T/H was fabricated in a 0.35μm quad-metal double-poly CMOS process. The layout of the T/H is shown in Fig. 4.1. The active area measures 2.6mm X 2.6mm, and the power dissipation is 320mW with a 3.3V power supply. It is laid out using a common-centroid techniques. Resistors, switches and capacitors are inter-digitated and laid out using dummy elements at the ends to avoid nonuniform etching problems and achieve better matching. Critical sections of the circuit are laid out in low stress and temperature gradient regions. Sectioned resistors are preferred over the serpentine resistors for better matching and small sections are avoided to neglect the effect of contact resistance. High sheet resistance resistors are very sensitive to charge spreading and so they should be avoided when laying two matched resistors.

The capacitors are laid out away from active regions and diffusion regions to avoid surface discontinuities and a square geometry is used for the capacitor cells. The high impedance nodes of the circuit are connected to the upper electrode of the capacitor to reduce the parasitic capacitance and substrate noise coupling. A N-well, which is connected to the most positive voltage, is used beneath the resistor and capacitor layouts to reduce substrate noise coupling. All the matched resistors and capacitors are placed away from the transistors with high bias current for better matching. Small finger sizes for the MOS trasistors will increase the perimeter capacitance of the drain and source and considerably effect the speed of operation of the circuit. The clock signals routing should be done very carefully and separate it as far as possible from the critical analog signals. It is necessary to put an electrostatic shielding plate when analog and digital signals cross.

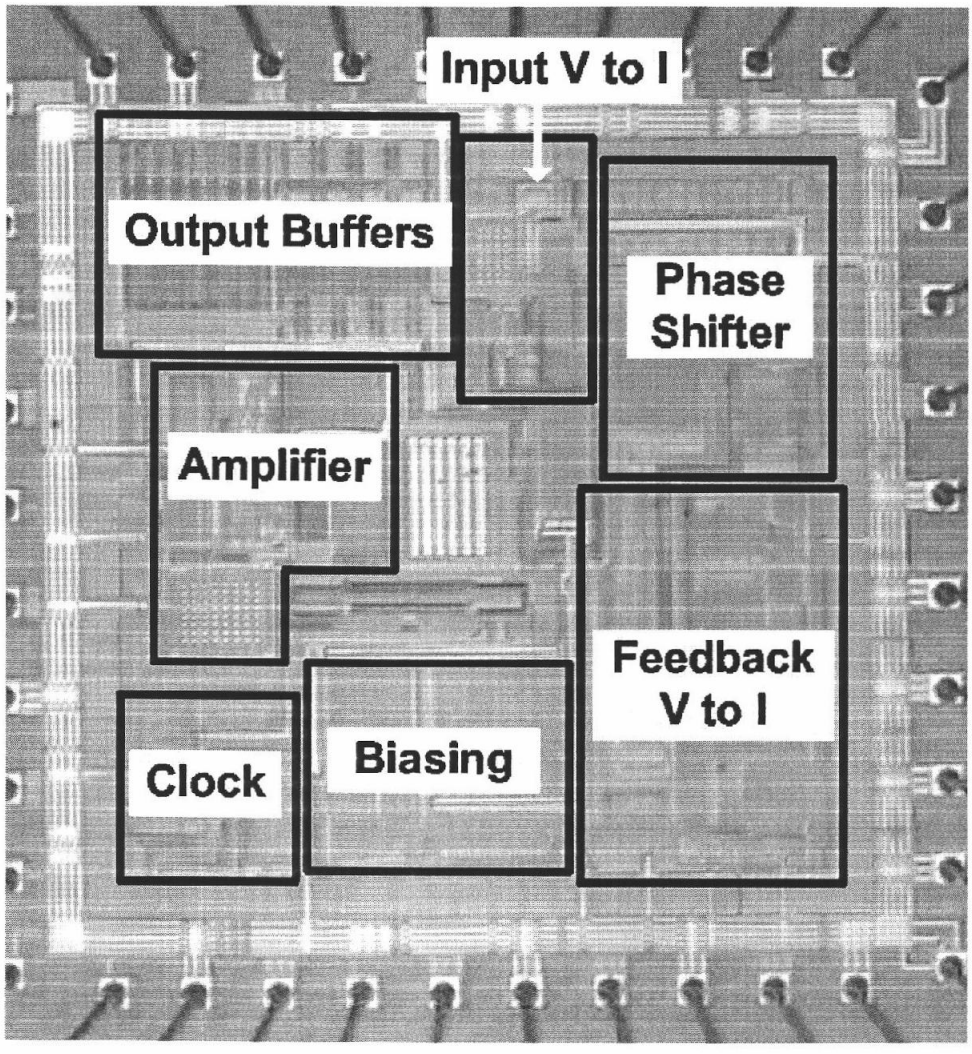

Figure 4.1. Layout of current-mode T/H.

Large numbers of substrate contacts are placed around important analog blocks to reduce the effect of signals coupling through the substrate. To remove the effects of coupling between two adjacent pins, pins adjacent to critical pins are connected to analog ground. The chip is packaged using a DIP40 ceramic package. The packaged T/H chip is mounted on a four-layer printed circuit board. The photo

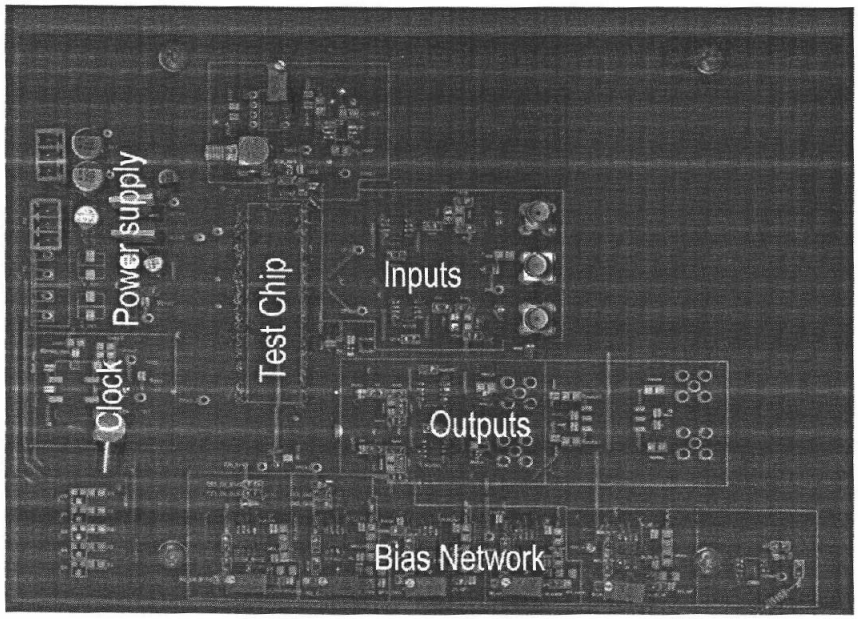

Figure 4.2. Schematic of test board

of the printed circuit board is shown in Fig. 4.2. The differential inputs to the chip are taken either from the audio precision source (good for low frequencies) or generated using high bandwidth and low distortion amplifiers on the board. A center tapped RF transformer with a 1:1 winding ratio is used to generate the differential inputs at high frequencies. Transformer is terminated with 50Ωs resistance. The

input signals to the transformer are generated using very sharp cut-off filters which attenuate all harmonics of the filter input. The bias voltages are generated using low bandwidth and low noise amplifiers. The power supplies to the chip are generated using voltage regulators. An external clock is generated using an arbitrary waveform generator for the input clock of the test chip. The layout of the board should be done very carefully with digital signals and analog signals widely separated as far as possible. The analog and digital blocks should have different power supplies to avoid any digital noise coupling into the sensitive analog section. Special care should be taken while laying out high bandwidth amplifier circuits since the parasitic capacitances can make them unstable.

Two phase clocks are generated inside the chip from an externally supplied clock. Differential to single ended conversion is done on the board. The output of the Differential to single ended converter is fed into a spectrum analyzer to measure the frequency response of the output voltage. Figure 4.3 shows the measured harmonic distortion as a function of frequency with $0.8V_{pp}$ differential inputs and a 40MHz clock frequency. The THD is approximately -82dB at 100KHz input frequency and falls to a value of -65dB at 10MHz. Figure. 4.4 shows the output spectrum when 10KHz input signal is applied with 40MHz input clock measured using audio precision. The noise floor of the spectrum is quite high because of the jitter of the clock.

This work illustrates the design of a wideband and highly linear T/H stage in current-mode even in standard CMOS processes. Since current-mode circuits deal with currents, high transconductance devices are preferable in the design of the current-mode circuits. Bipolar transistor, which have transconductance values 4 or 5 times higher than the CMOS devices because of their exponential current-voltage

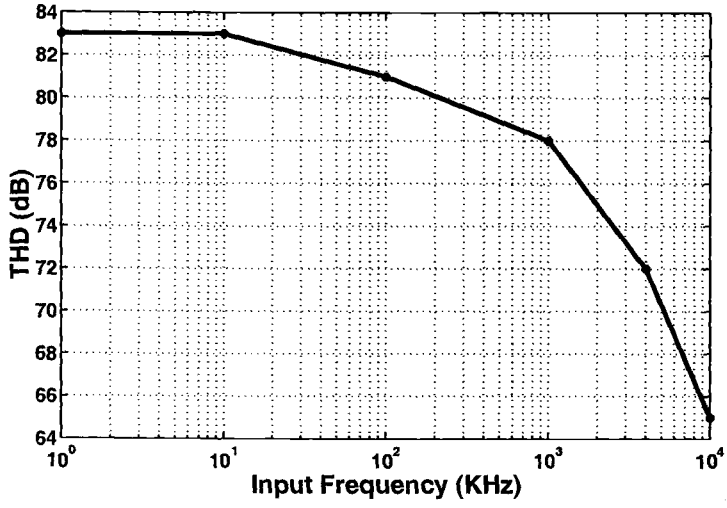

Figure 4.3. Measured THD plot vs frequency.

characterstics, are more suitable for the current-mode circuit design than CMOS devices. The performance of the T/H stage has been summarized in Table 4.1. A comparison with recently published T/H circuits has also been provided. It can be seen that all other implementations were designed either in bipolar or BiCMOS technologies which have much greater transconductance and f_T values. Since f_T is equal to the frequency where the current gain of the device is equal to unity, higher f_T values imply that a loop-gain greater than unity can be achieved over wide bandwidth for closed-loop current-mode architectures. Higher loop-gain circuits give highly linear outputs because any non-idealities inside the closed-loop get suppressed by a factor equal to the loop-gain. Thus, we can design wideband and highly linear current-mode circuits with much less power dissipation in higher f_T processes.

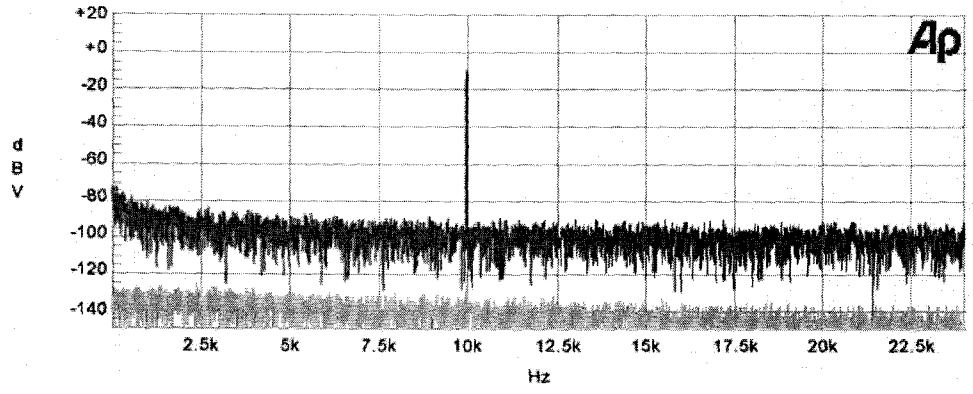

Figure 4.4. Frequency spectrum of the output with 10k input signal and 40MHz clock

Table 4.1. Performance comparison of recently published T/H stages.

Reference	Razavi [9]	Schillaci [10]	Razavi [8]	Real [5]	This work
THD (dB)	-65dB	-52dB	-60dB	-54dB	-65dB
Frequency of Measurement	10MHz	10MHz	10MHz	10MHz	10MHz
Opearation Mode	Voltage	Voltage	Voltage	Current	Current
Power Supply	3V	3V	3V	+/- 5V	3.3V
Technology	BiCMOS	BiCMOS	Bipolar	BiCMOS	CMOS
Clock Frequency	200MHz	150MHz	100MHz	20MHz	40MHz

5. CONCLUSIONS

A new current-mode closed-loop T/H architecture is developed to design high speed and high resolution circuits. The sensitivity of the current-mode circuits to jitter has been analysed. High bandwidth and high linearity transconductors are designed using phase correction techniques for the feedback signal. It is shown that high speed and high linearity current-mode T/H circuits can be designed even in standard CMOS process. This illustrates that the non-ideal effects of the CMOS switch are considerably suppressed in closed-loop current-mode architectures.

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