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Analysis and Modeling of Microstrip On-Chip Interconnects on Silicon Substrate.

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Andreas Weisshaar

The electrical performance of on-chip interconnects has become a limiting factor to the performance of modern integrated circuits including RFICs, mixed-signal circuits, as well as high-speed VLSI circuits due to increasing operating frequencies, chip areas, and integration densities. It is advantageous to have fast and accurate closed-form expressions for the characteristics of on-chip interconnects to facilitate fast simulation and computer-aided design (CAD) of integrated circuits. This thesis work is mainly concerned with the analysis and the methodology of developing closed-form expressions for the frequency-dependent line parameters $R(\omega)$, $L(\omega)$, $G(\omega)$, and $C(\omega)$ for microstrip-type on-chip interconnects on silicon substrate.

The complete solutions of the frequency-dependent line parameters are formulated in terms of corresponding lossless/static configurations for both single and coupled microstrip-type on-chip interconnects. The series impedance parameters are developed using a complex image approach, which represents the complicated loss effects in the semiconducting silicon substrate. The shunt admittance parameters are developed using low- and high-frequency asymptotic solutions based on the shunt equivalent circuit models. The closed-form expressions are shown to be

in good agreement with full-wave and quasi-static electromagnetic solutions. Based on the proposed closed-form solutions, a new on-chip interconnect extractor tool, CELERITY, is implemented. It is shown that the new tool can significantly reduce the simulation time compared with a quasi-static EM-based tool. The proposed extraction technique should be very useful in the design of silicon-based integrated circuits.

Analysis and Modeling of Microstrip On-Chip Interconnects on Silicon Substrate

by

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Redacted for Privacy

Major Professor, representing Electrical and Computer Engineering

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Chair of the Department of Electrical and Computer Engineering

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1. INTRODUCTION

1.1. Background and Motivation

Silicon semiconductor integrated circuit technology has played a critical role for decades since the 1960's in most of very large scale integrated circuit (VLSI), mixed-signal integrated circuit, and radio-frequency integrated circuit (RFIC) systems. Driven by the highly demanding market of wireless communications, high-speed communication backbones, optical networks, and the trend of system-on-a-chip (SoC), current integrated circuit design is aimed at increasing operating frequencies, chip areas, and integration densities. For example, at the time of writing this thesis, the world's fastest desktop CPU chip was just released, which operates at 2GHz with integration of about 42 million transistors in $0.18\mu m$ technology [1]. The electrical performance of on-chip interconnects has become a limiting factor in the performance of many such modern applications including RFICs, mixed-signal circuits as well as high-speed VLSI circuits.

On-chip interconnects are the wires that are used to interconnect the circuit cells, components, and blocks, etc., in integrated circuit chips. Figure 1.1 shows the typical configuration of on-chip interconnects. While the ideal wire does not affect circuit performance at all, a real wire exhibits significant transmission line effects that may have a dominant influence on the integrated circuit operation.

These interconnect effects increase as device dimensions are reduced and thus can dominate in today's deep submicron technologies. This situation is even aggravated by the fact that rapid improvement in technology is making the volume production of larger and larger die sizes economically feasible, which results in increases in average length of interconnect wires and in the associated transmission line effects. In general, interconnects can lead to significant signal delay, cross-talk, and power dissipation in the metallization and the lossy silicon substrate [2]. Consequently, efficient and accurate simulation taking into account the important interconnect effects is becoming an essential stage and has become a major bottleneck in the whole IC design cycle.

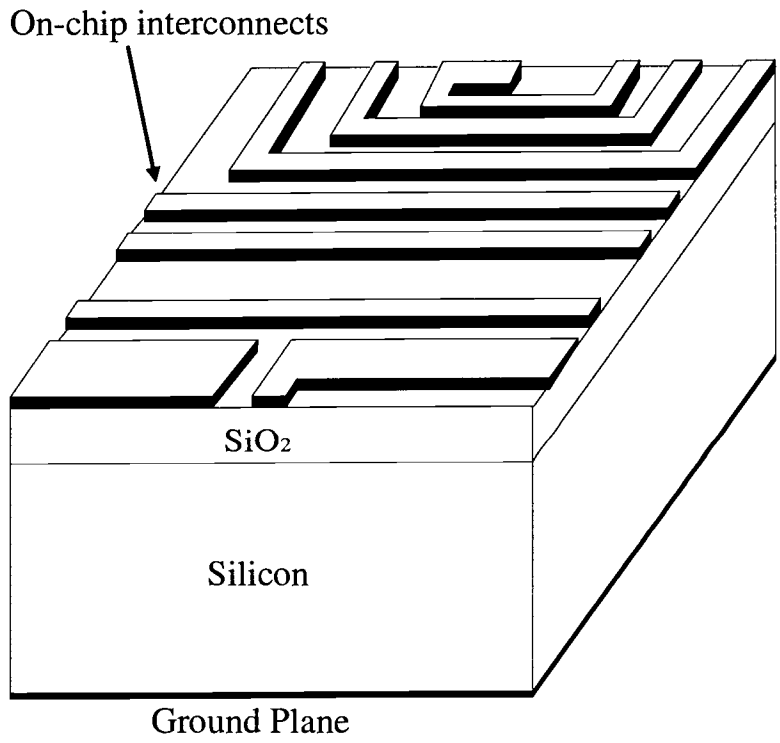


FIGURE 1.1. Typical on-chip interconnects

On-chip interconnects are fabricated in various shapes of planar transmission line configurations. Further more, many important on-chip-wiring-based passive components, such as spiral inductors, are also constructed by planar transmission line structures. As shown in Figure 1.1, all these planar transmission lines are realized in inhomogeneous media and with silicon substrates of conductivities varying from lightly doping levels to heavily doping levels. Due to the semiconducting nature of the silicon substrate as well as the complicated inhomogeneous media structure, it is generally difficult to accurately characterize these planar transmission lines on silicon substrate, i.e., on-chip interconnects. The inhomogeneous media structure make it difficult to develop closed-form equations, and the lossy silicon substrate layer leads to significant frequency-dependent and conductivity-dependent effects particularly at high operating frequencies, which makes the characterization even more complicated.

Transmission lines on silicon substrate have been extensively studied by full wave electromagnetic (EM) analysis [3], [4], [5] and more recently by quasi-static EM approaches [6], [7]. Generally speaking, all these numerical EM techniques are based on analyzing the electric and magnetic field distributions by solving applicable multi-dimensional wave equations subject to a certain type of given boundary conditions. Typical techniques include the Method of Moments (MoM), the Finite Difference Time Domain Method (FDTD), and the Finite Element Method (FEM), etc. In the case that the solution to the Laplace equation can adequately approximate the properties of the structures in the frequency range of interest, the quasi-static EM methods can significantly reduce the cost of simulation. A quasi-static Spectral Domain Approach (SDA) has been successfully applied in solving for planar transmission line structures including on-chip interconnects on silicon substrate [8]. Particularly, it is recommended to use these rigorous EM techniques when very accurate frequency-dependent characterization of on-chip interconnects

on lossy silicon substrate is needed. However, EM analysis, in general, takes a considerable amount of time, which severely lowers the efficiency of analysis for on-chip interconnect effects. For example, at the early stage in the IC design cycle, it is quite common in practice that a very fast yet considerably accurate estimation of on-chip interconnect effects is needed to provide the designer a first insight on the interconnect performance. Using rigorous full-wave or quasi-static EM techniques is not suitable for fast simulation purposes, where the bottleneck of the entire process in determining the characteristics of on-chip interconnects is the time consuming EM simulation.

Hence, it is highly desirable to have fast yet adequately accurate solution to the on-chip interconnect issue. It is one of the major goals of this thesis work to develop a very fast extraction methodology and modeling approach to capture the frequency-dependent characteristics of on-chip interconnects on lossy silicon substrate. Frequency-dependent transmission line parameters, $R(\omega)$, $L(\omega)$, $G(\omega)$, $C(\omega)$, are usually used to fully characterize the on-chip interconnect properties. This thesis focuses on the derivations of closed-form expressions for $R(\omega)$, $L(\omega)$, $G(\omega)$, $C(\omega)$ that are suitable for computer-aided design (CAD). The goal is to significantly speed up the on-chip interconnect simulation and CAD modeling by replacing the time-consuming EM analysis by a fast closed-form-expressions-based extraction technique.

1.2. Organization of the Study

This thesis presents the analysis and fast extraction methodology for line parameters of a class of on-chip interconnects. The main focus is on typical microstrip-type planar transmission line structures on a silicon substrate. An overview of the research work and the organization of the study is given below.

Chapter 2 presents the basic theory of planar microstrip transmission lines on silicon substrate. Rigorous electromagnetic field analysis of conventional microstrip lines is reviewed as a background. Previous studies on Metal-Insulator-Semiconductor (MIS) structures are briefly introduced, with emphasis on the understanding of the physical behavior of the different operating modes as well as the corresponding equivalent circuit models. Currently available EM based extraction approaches are summarized, showing the disadvantage in computation time. The new methodology of developing closed-form expressions, which includes the significant frequency- and conductivity-dependent lossy silicon substrate effects, is therefore very worthwhile to be developed.

Chapter 3 starts with the single microstrip line on silicon substrate. The investigation on the simplest configuration can clearly capture the different mechanisms that cause the overall complexity in extracting the line parameters of on-chip interconnects and thus eases the derivation of complete closed-form expressions. A complex image approach is introduced and extended to MIS structures. The series impedance line parameters $R(\omega)$ and $L(\omega)$ are developed using the extended image approach, that represents the complicated lossy effects of silicon substrate. The shunt admittance line parameters $G(\omega)$ and $C(\omega)$ are developed using asymptotic solutions in the low- and high- frequency limits based on the broadband equivalent circuit model and the physical behavior at the upper and lower frequency limits. The accuracy of the new modeling approach is illustrated by comparison with full-wave and quasi-static EM solutions.

Chapter 4 addresses the coupled microstrip on-chip interconnects on silicon substrate. The calculation of static partial self and mutual inductances is reviewed as a background. The complex image approach is extended to the coupled line case to calculate the complex inductance matrix, from which the series impedance parameters $[R(\omega)]$ and $[L(\omega)]$ can be extracted. The shunt admittance parameters

$[G(\omega)]$ and $[C(\omega)]$ are obtained using high- and low-frequency asymptotic solutions, but involve a more complicated extraction procedure. A simple yet efficient approach based on $\triangle$ -Y transforms is used to extract the two-port capacitance network. The validations are done with EM simulations for various dimensions and process parameters.

Chapter 5 presents applications of the developed new modeling approach and fast extraction technique for on-chip interconnects on lossy silicon substrate. The developed closed-form expressions for on-chip interconnects are implemented into the on-chip interconnect modeling tool, CELERITY. By replacing the time consuming EM extraction part with the fast, compact, yet adequately accurate closed-form expressions, very fast on-chip interconnect parameters extraction can be obtained to speed up the entire process of on-chip interconnect CAD modeling. The improvement in simulation time, including frequency-dependent line parameters extraction and equivalent lumped subcircuit model extraction, is shown to be a factor of tens to several hundred, as compared with an EM-based tool.

Chapter 6 concludes the study and suggests further research.

2. BASIC THEORY OF MICROSTRIP ON-CHIP INTERCONNECTS

2.1. Introduction

Due to dense, large chips with higher operating frequencies, the electrical performance of on-chip interconnects has become a limiting factor in the performance of integrated circuits. The interconnection effects such as loss, dispersion, delay, and crosstalk may degrade the performance of integrated circuits. Therefore, a thorough understanding and accurate simulation of on-chip interconnects are required in order to confidently predict the circuit performance.

Microstrip transmission lines are one of the most elementary components in form of interconnects in modern silicon-based integrated circuits. As the most common interconnect in conventional RF/microwave circuits, microstrip transmission lines on lossless or very low loss substrate have been thoroughly studied over years. With the increasing interest in silicon based integrated circuit and more recently system-on-a-chip (SoC), microstrip lines on insulator-semiconductor have attracted various research effort from different angles. Hasegawa [3] studied the interactions between the electromagnetic fields and the lossy substrate and introduced his categorization of three major operating modes as well as the corresponding equivalent circuits. Various numerical electromagnetic techniques have been successfully applied to deal with microstrip lines on silicon substrate. Different lumped circuit modeling approaches aiming at efficient simulation at the circuit level have been developed.

This chapter introduces the basic theory of microstrip on-chip interconnects. Maxwell's's equations are first reviewed as a background, followed by the field analysis of microstrip transmission lines. The conventional way of characterizing trans-

mission lines in terms of line parameters is thereafter introduced. MIS structure is explained with focus on the physical origins of each operating mode and the effects of silicon substrate loss. An overview of the related research work on MIS interconnects is given and the motivation for this research is then elucidated.

2.2. Field Analysis of Planar Transmission Lines

Maxwell's equations are the fundamental laws governing the behavior of electromagnetic fields. In general, Maxwell's equations take the following form

$$\nabla \times \mathbf{E}(\mathbf{r},t) = -\frac{\partial \mathbf{B}(\mathbf{r},t)}{\partial t} \tag{2.1}$$

$$\nabla \times \mathbf{H}(\mathbf{r},t) = -\frac{\partial \mathbf{D}(\mathbf{r},t)}{\partial t} + \mathbf{J}(\mathbf{r},t) \tag{2.2}$$

$$\nabla \cdot \mathbf{D}(\mathbf{r},t) = \rho(\mathbf{r},t) \tag{2.3}$$

$$\nabla \cdot \mathbf{B}(\mathbf{r},t) = 0 \tag{2.4}$$

where $\mathbf{E}$ and $\mathbf{H}$ are, respectively, the electric and magnetic field intensities, $\mathbf{D}$ and $\mathbf{B}$ are, respectively, the electric and magnetic flux densities, $\mathbf{J}$ is the conduction current density, and ρ is the electric charge density.

The relationships of $\mathbf{D}$ to $\mathbf{E}$ and $\mathbf{B}$ to $\mathbf{H}$ are known as constitutive relations

$$\mathbf{D} = \epsilon \mathbf{E} \tag{2.5}$$

$$\mathbf{B} = \mu \mathbf{H} \tag{2.6}$$

where ϵ and μ are, respectively, the permittivity and permeability of the medium.

Maxwell's equations describe essentially how the electromagnetic fields are generated from sources ρ and $\mathbf{J}$. In order to solve Maxwell's equations, one also needs

the constitutive relations, which macroscopically characterize a material medium and how it responds to electromagnetic fields.

In general, for transmission line structures, the electric and magnetic fields are the solutions of homogeneous vector Helmholtz equations, i.e.,

$$\nabla^2\mathbf{E} + k^2\mathbf{E} = 0 \tag{2.7}$$

$$\nabla^2\mathbf{H} + k^2\mathbf{H} = 0 \tag{2.8}$$

where k is the wave number. Under the assumption of axial uniformity, the type of solution sought of (2.7) and (2.8) is that corresponding to a wave that propagates along the axis, here assumed to be the z-axis. The general solutions can be separated into transverse and axial components as [10]

$$\begin{aligned}\mathbf{E}(x,y,z) &= \mathbf{E}_t(x,y,z) + \mathbf{E}_z(x,y,z) \\ &= \mathbf{e}(x,y)e^{-j\beta z} + \mathbf{e}_z(x,y)e^{-j\beta z}\end{aligned} \tag{2.9}$$

$$\begin{aligned}\mathbf{H}(x,y,z) &= \mathbf{H}_t(x,y,z) + \mathbf{H}_z(x,y,z) \\ &= \mathbf{h}(x,y)e^{-j\beta z} + \mathbf{h}_z(x,y)e^{-j\beta z}\end{aligned} \tag{2.10}$$

where $\mathbf{E}_t$, $\mathbf{H}_t$ are the transverse components, and $\mathbf{E}_z$, $\mathbf{H}_z$ are the axial components. Also note that $\mathbf{e}$ and $\mathbf{h}$ are transverse vector functions, and $\mathbf{e}_z$ and $\mathbf{h}_z$ are axial vector functions.

It is of particular interest to study three types of solutions: transverse electromagnetic (TEM) waves, where $\mathbf{E}_z = \mathbf{H}_z = 0$, transverse electric modes (TE), where $\mathbf{E}_z = 0$ but $\mathbf{H}_z \neq 0$, and transverse magnetic modes (TM), where $\mathbf{H}_z = 0$ but $\mathbf{E}_z \neq 0$.

The microstrip line does not support pure TEM waves because of the inhomogeneity of the surrounding medium. However, when the transverse dimensions

are much smaller than the wavelength, a quasi-TEM assumption may be applicable [9], [11]. It was reported that the quasi-TEM assumption may be valid up to switching speeds of 7ps [11]. Under the quasi-TEM assumption, the original vector field problem is reduced to a problem of finding a scalar potential Φ which is a solution of two dimensional Laplace equation

$$\nabla_t^2 \Phi(x,y) = 0 \tag{2.11}$$

and satisfies the proper boundary conditions. Thus the fields are given by

$$\mathbf{E} = \mathbf{E}_t = \mathbf{e} e^{\pm jkz} = -\nabla_t \Phi e^{\pm jkz} \tag{2.12}$$

$$\mathbf{H} = \mathbf{H}_t = \mp \mathbf{h} e^{\pm jkz} = \mp Y_0 \mathbf{a}_z \times \mathbf{e} e^{\pm jkz} \tag{2.13}$$

where Y_0 is the wave admittance.

More rigorous EM analysis of the microstrip transmission line shows that the actual propagating waves are the hybrid of TM and TE modes. Since TM0 is the lowest wave mode that the microstrip transmission line can support, it is of fundamental importance to have EM solution of TM waves. Separating (2.7) into axial and transverse parts and replacing ∇^2 by $\nabla_t^2 - \beta^2$ yields [10]

$$\nabla_t^2 e_z(x,y) + k_c^2 e_z(x,y) = 0 \tag{2.14}$$

$$\nabla_t^2 \mathbf{e} + k_c^2 \mathbf{e} = 0 \tag{2.15}$$

where $k_c^2 = k^2 - \beta^2$. Once a solution of e_z satisfying (2.14) subject to the boundary conditions is obtained, the transverse fields are then given by

$$\mathbf{E}_t = \mathbf{e} e^{\mp j\beta z} = -\frac{j\beta}{k_c^2} \nabla_t e_z e^{\mp j\beta z} \tag{2.16}$$

$$\mathbf{H}_t = \pm \mathbf{h} e^{\mp j\beta z} = \pm Y_e \mathbf{a}_z \times \mathbf{e} e^{\mp j\beta z} \tag{2.17}$$

where Y_e is the wave admittance for TM waves. Therefore the complete expressions for the waves propagating in the $+z$ are given by

$$\mathbf{E} = (\mathbf{e} + \mathbf{e}_z)e^{-j\beta z} \tag{2.18}$$

$$\mathbf{H} = (\mathbf{h} + \mathbf{h}_z)e^{-j\beta z} \tag{2.19}$$

Specifically, for a microstrip line on a lossless substrate with thickness H, the unknown charges and current densities on the conducting microstrip, ρ and $\mathbf{J}$, can be expressed as

$$\rho(x, y, z) = \rho_s(x, z)\delta(y - H) \tag{2.20}$$

$$\mathbf{J}(x, y, z) = \mathbf{J}_s(x, z)\delta(y - H) \tag{2.21}$$

and the substrate material is characterized by a dielectric constant ϵ_y in the y direction and ϵ_r in the x and z directions. With the aid of vector magnetic potential $\mathbf{A}$, which is an auxiliary variable defined as

$$\mathbf{B} = \nabla \times \mathbf{A} \tag{2.22}$$

solving the original equations becomes seeking for solutions to the following homogeneous equations, subject to the specified boundary conditions, in the substrate region [10]

$$(\nabla^2 + \epsilon_r k_0^2)A_x = 0 \tag{2.23}$$

$$(\nabla^2 + \epsilon_r k_0^2)A_z = 0 \tag{2.24}$$

$$\nabla^2 A_y + \epsilon_y k_0^2 A_y = j\omega\mu_0\epsilon_0(\epsilon_y - \epsilon_r)\frac{\partial \Phi}{\partial y} \tag{2.25}$$

$$\frac{\partial^2 \Phi}{\partial x^2} + \frac{\partial^2 \Phi}{\partial z^2} + \frac{\epsilon_y}{\epsilon_r}\frac{\partial^2 \Phi}{\partial y^2} + \epsilon_r k_0^2 \Phi = -j\omega(\epsilon_y - \epsilon_r)\frac{\partial A_y}{\partial y} \tag{2.26}$$

Therefore, the corresponding electric and magnetic fields in microstrip transmission line can be solved with the solution of $\mathbf{A}$ available, which can be obtained by solving the above homogeneous equations.

2.3. Transmission Line Parameters

Although the field analysis can give complete characterization of the transmission line property, it is advantageous to use the circuit parameters to describe the transmission line. A general form of the transmission line model consists of a per unit length (p.u.l.) series impedance $Z(\omega)$ and a p.u.l. shunt admittance $Y(\omega)$, as shown in Fig. 2.1.

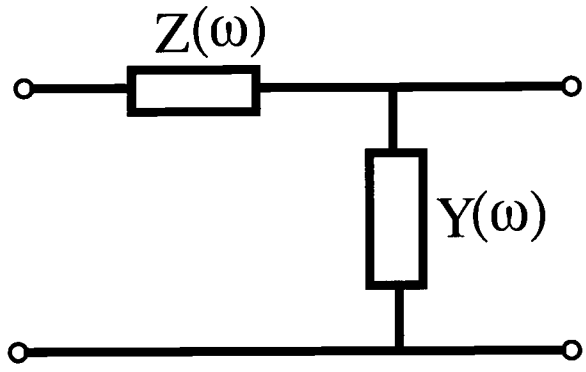


FIGURE 2.1. P.u.l. general form of transmission line model

$$Z(\omega) = R(\omega) + j\omega L(\omega) \tag{2.27}$$

$$Y(\omega) = G(\omega) + j\omega C(\omega) \tag{2.28}$$

Moreover, it is common to use distributed circuit parameters R, L, G, and C to fully capture the transmission line characteristics. It should be noted that, in general, these parameters are frequency-dependent. Figure 2.2 shows the frequency dependent p.u.l. distributed circuit model of the transmission line. It is important to understand the physical meaning of R, L, G, and C parameters and relate them

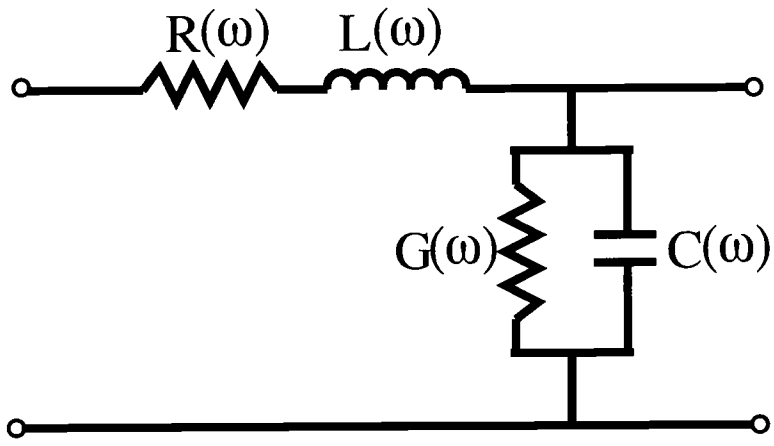


FIGURE 2.2. Transmission Line Parameters: p.u.l. $R(\omega)$, $L(\omega)$, $G(\omega)$, and $C(\omega)$

to the electrical and magnetic fields. These parameters can be determined from the evaluation of the stored electric and magnetic energy and power disspation (loss) in the transmission line structure. L measures the energy stored in the magnetic fields. C measures the energy stored in the electric fields. The power loss in the conductor as well as the eddy current loss in the lossy substrate, e.g., silicon substrate, is accounted by R. The power loss due to the dielectric or lossy substrate is accounted for by G. For TEM or quasi-TEM waves, suitable definitions for the p.u.l. parameters R, L, G, and C based on the above energy concept can be expressed in the form of line or surface contour integrals [10]

$$R = \frac{R_m}{I_0 I_0^*} \oint_{S_1+S_2} \mathbf{H} \cdot \mathbf{H}^* dl \tag{2.29}$$

$$L = \frac{\mu}{I_0 I_0^*} \int_S \mathbf{H} \cdot \mathbf{H}^* dS \tag{2.30}$$

$$G = \frac{\omega \epsilon''}{V_0 V_0^*} \int_S \mathbf{E} \cdot \mathbf{E}^* dS \tag{2.31}$$

$$C = \frac{\epsilon'}{V_0 V_0^*} \int_S \mathbf{E} \cdot \mathbf{E}^* dS \tag{2.32}$$

Here I_0 is the total current on the line and V_0 is the potential difference. $R_m = 1/\sigma\delta$ and δ is the skin depth. The dielectric has a complex permittivity $\epsilon = \epsilon' - j\epsilon''$. In (2.29), (2.30),(2.31) and (2.32), integrals of electromagnetic fields over the appropriate contours are used as convenient definitions for voltage and current. These definitions of voltage and current are valid, however, only for TEM and quasi-TEM, as stated earlier.

For TM waves, the contour integral definitions of voltage and current are no longer applicable due to the presence of longitude electric field, which implies that the transverse components do not satisfy the static situation. A more rigorous energy-based method has been applied to obtain the corresponding R, L, G, and C parameters [13]. However, in the content of this thesis, TEM or quasi-TEM assumption is always satisfied.

It is also conventional to use propagation constant γ and characteristics impedance Z_0 to describe the transmission line characteristics. The R, L, G, and C transmission line parameters are related to them as

$$\gamma = \alpha + j\beta = \sqrt{[R(\omega) + j\omega L(\omega)][G(\omega) + j\omega C(\omega)]} \tag{2.33}$$

$$Z_0 = \sqrt{\frac{R(\omega) + j\omega L(\omega)}{G(\omega) + j\omega C(\omega)}} \tag{2.34}$$

where α is the attenuation constant and β is the phase constant.

2.4. Metal-Insulator-Semiconductor Interconnects

Metal-insulator-semiconductor (MIS) interconnects, being one of the most elementary components in modern integrated circuits, have been of fundamental interest. The MIS structure, as illustrated in Figure 2.3, may exhibit complicated behavior due to the semiconducting property of the doped silicon substrate. The

slow-wave propagation, which will be clarified later in this section, of such interconnects can be employed to reduce the size and cost of distributed elements to realize delay lines, phase shifters, voltage-tunable filters, etc. Moreover, the energy loss effects resulting from both semiconductor substrate and conductor strip may have significant impacts on the overall performance of MIS interconnects. In order to analyze and model the on-chip interconnects accurately, it is very important to understand the MIS structure clearly. In the following text, basic aspects of the MIS structure are reviewed.

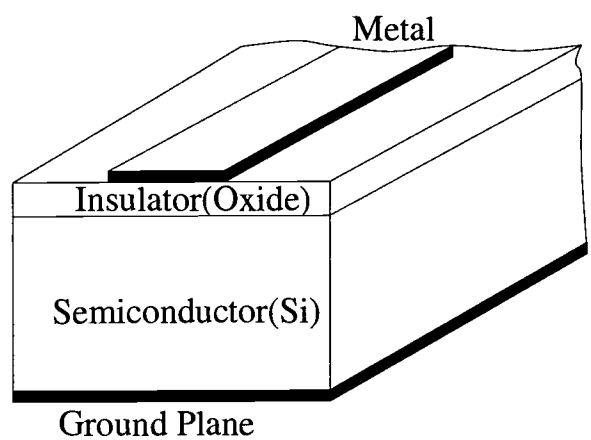


FIGURE 2.3. Metal-Insulator-Semiconductor (MIS) structure

In 1971, Hasegawa thoroughly studied the influence of the semiconducting substrate in a microstrip line on silicon and silicon-dioxide ($Si-SiO_2$) system on the transmission line characteristics over a wide range of silicon substrate conductivities, using a parallel-plate waveguide model as well as experimental data [3]. For the first time the concept of three major operating modes was introduced. According to his studies, depending on different operating frequencies and doped silicon conductivities, there may exist three fundamental operating modes in an MIS system,

i.e., dielectric quasi-TEM mode, skin-effect mode, and slow-wave mode, as qualitatively illustrated in Figure 2.4. Since each mode has a complicated wave propagation mechanism resulting from the interactions of the electromagnetic fields and the lossy substrate, it is helpful to first understand the physical origin of each mode and then model each of them in terms of frequency- and conductivity-dependent distributed series and shunt transmission line parameters.

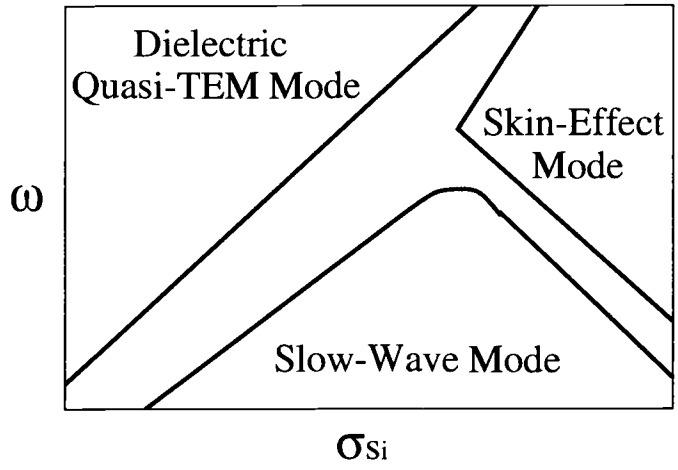


FIGURE 2.4. Three major operating modes in frequency-conductivity domain chart

When the frequency-conductivity ($\omega\sigma_{Si}$) product is low enough to produce a small dielectric loss angle, the silicon substrate can be treated as a dielectric and the corresponding MIS system can be treated as a microstrip line fabricated on a two-layer dielectric consisting of silicon and silicon-dioxide. The fundamental mode would resemble the TEM mode very closely since the wavelength is much larger than the physical height of the substrate media. Moreover, since the physical height of the silicon layer is greater than that of the oxide layer for practical cases, most of the electromagnetic field is concentrated in the silicon layer. In this mode, the

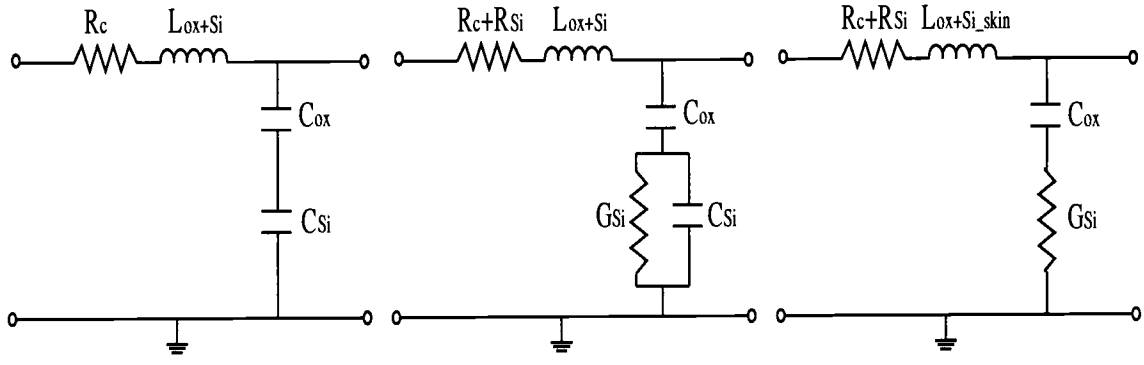
knowledge of electrostatic analysis of quasi-TEM mode can be employed, which assumes no longitudinal variation in field distribution.

On the contrary, when the frequency-conductivity ($\omega\sigma_{Si}$) becomes large enough to yield a small field penetration into the silicon substrate, the silicon layer acts just as an imperfect (i.e., lossy) ground plane. In this mode, only a small portion of field exists in the silicon layer due the wave reflection at the interface between oxide and silicon. Hence the wave propagation mechanism is mainly determined by the interactions between the conducting strip and the skin depth in the silicon layer. This mode is named skin-effect mode.

In addition to the above two limiting cases of lossless dielectric and lossy metallic, there exists a third mode when the $\omega\sigma_{Si}$ stays in the intermediate range, for example, when the frequency is not very high and the silicon conductivity is moderate. In this mode, the silicon substrate exhibits the semiconducting behavior. The slow-wave mode was described by Guckel in [14]. The propagating velocity slows down owing to the energy transfer across the interface associated with the dielectric dispersion and strong interfacial polarization at the silicon substrate.

Based on the above qualitative explanation of the physical origin of each mode, equivalent circuits were proposed, as shown in Figure 2.5. In the quasi-TEM mode, the conduction current in the silicon layer is negligible compared to the displacement current since the relaxation frequency $\sigma_{Si}/\epsilon_{Si}$ is much less than the operating frequency. Hence the shunt part consists of two series connected capacitances. Note that R_c represents the conductor loss and L_{ox+Si} corresponds to the flux linkage between the conductor strip and the ground plane through the double-layer dielectric consisting of oxide and silicon. On the contrary, in the skin-effect mode, the shunt displacement current is negligible compared to the conduction current because the magnetic field penetration into the silicon substrate is just the substrate skin depth. Moreover, this leads to a reduced inductance value because the

flux linkage is only in the oxide layer and the skin depth into the silicon layer. The series resistance also increases by an additional term of R_{Si} since additional energy is dissipated by the longitudinal substrate currents (eddy currents). In between these two modes, i.e., in the slow-wave mode, both shunt capacitance and conductance should be included in the silicon substrate since neither displacement current nor conductance current dominates over the other one.



(a)Quasi-TEM mode (b)Slow-wave mode (C)Skin-effect mode

FIGURE 2.5. Equivalent circuits for three operating modes of MIS structure

The equivalent circuits not only qualitatively explain and represent the different mechanisms in the three different modes but also suggest that one may study the circuit elements separately. For example, in the slow-wave mode, which is of particular interest because it appears to be within the frequency and conductivity range suited for on-chip interconnects, both conductor loss and substrate loss contribute to the overall resistance, and it has been shown that they are approximately additive [16]. The analytical expression for conductor loss appears well known while the loss due to the semiconducting silicon substrate is more complicated. One may

concentrate on the analytical expression for the latter one by assuming a perfect conductor.

2.5. Overview of Analysis and Modeling Techniques for MIS Interconnects

There has been much research done to analyze and model MIS interconnects. Various techniques can be roughly categorized into numerical electromagnetics (EM) based analysis and physical models based analysis, although the classification criteria are not unique.

Numerical EM analysis refers to those various numerical algorithms of solving for rigorous electric and magnetic field solutions of the corresponding Maxwell's equations with proper boundary conditions and constitute relations. Different approaches for this type of analysis can be roughly classified into three categories, quasi-TEM (quasi-static) analysis, frequency-domain full-wave analysis, and time-domain full-wave analysis.

As stated earlier, MIS structures can not support a pure TEM wave mode due to the inhomogeneous dielectric medium and energy disspation in the lossy substrate. However, under certain conditions when the transverse dimensions are much smaller than the wavelength, the longitudinal variation in field distribution can be ignored with acceptable accuracy and thus a quasi-TEM assumption may be applied. The original Maxwell's equations can be solved more easily by virtue of quasi-TEM assumption. The commonly used approach to solve the quasi-TEM problem is based on potential theory, which basically simplifies the original vector field problem to a potential problem by introducing an auxiliary variable, i.e., an electric scalar potential. This can significantly reduce the complexity as well as the computation time while preserving adequate accuracy.

When the quasi-TEM assumption is not satisfied or a very accurate solution is required, full-wave analysis should be used. The frequency-domain full-wave analysis solves the problem of interest at each interesting frequency point. Consequently, it can easily incorporate various frequency-related effects, such as skin effect, dispersion, losses, reflections at discontinuities, etc. Generally it solves one of three equivalent sets of equations, time-harmonic Maxwell's equations, Helmholtz wave equations, and Green's functions-based integral equations. The first two are in nature differential equations while the latter one is in nature an integral equation. Commonly used algorithms include, but are not limited to, finite difference method (FDM, [17]), finite element method (FEM, [18]), spectral domain approach (SDA, [19]), frequency-domain transmission line matrix method (FDTLM, [20]), etc. For transient analysis, time-domain full-wave analysis is more powerful and efficient than frequency-domain analysis. The most widely used algorithms include the finite-difference time-domain (FDTD, [21]) method and the time-domain transmission line matrix (TDTLM, [22]).

Physical models refer to those modeling approaches based on physical concepts. This type of techniques includes, but is not limited to, parallel-plate waveguide model [3], CAD-oriented ideal lumped equivalent circuit model [12], analytical or empirical circuit model [17], multi-conductor transmission line model [19], partial-element equivalent circuit (PEEC) based model [15], and combined electromagnetic and device simulation model [13], etc.

Although MIS interconnect structures have been studied from various points of view, there still exists a bottleneck in the simulation process or design cycle for on-chip interconnect analysis. Various numerical EM techniques generally provide accurate characterization of the interconnects at the cost of computation complexity in terms of memory size, simulation time, and calculation stability, etc. There have been great efforts working on the improvement of numerical EM analysis, for

example, a new magnetic-potential based quasi-static spectral domain approach [7], [8] which overcomes the invalidity of the conventional quasi-static SDA for typical interconnects in CMOS technology with increasing frequency-range of operation. Fast simulation is a concern in practice. For example, one may be interested in very fast estimation of on-chip interconnect impacts, at the early stage of the design cycle as a first insight into interconnects issue. At the post layout stage, one may pursue very fast yet adequately accurate parasitics extraction given interconnect dimensions and process parameters. The current available parasitics extraction tools, most of which are based on EM analysis, are not very efficient in terms of simulation time although accurate. This difficulty in nature is due to the fact that large sized computations of numerical integral and/or differential operations are needed to solve field problems.

In a word, the bottleneck in the entire process in determining the characteristics of on-chip interconnects is still the time consuming EM simulation. Current EM based approaches are not viable for fast simulation. It is then highly desirable to have closed-form expressions for the frequency-dependent line parameters of on-chip interconnects that are suitable for CAD and thus can significantly speed up the simulation. It is one of the major goals in this thesis to develop a new methodology for deriving closed-form expressions for the line parameters $R(\omega)$, $L(\omega)$, $G(\omega)$, and $C(\omega)$ of microstrip on-chip interconnects. The closed-form expressions should be very efficient in computation, adequately accurate in accuracy, and should, of course, take into account the important silicon substrate loss effects. The complete closed-form solution of frequency-dependent characteristics can be combined with CAD-oriented equivalent circuit extraction techniques [12] to facilitate on-chip interconnect analysis as well as synthesis. It should be very useful for the design of silicon-based integrated circuits.

2.6. Conclusion

Microstrip on-chip interconnects have been studied by rigorous field analysis, many numerical full-wave or quasi-TEM EM computation techniques, and various modeling approaches. However, the time consuming part of extraction for line parameters is still the bottleneck in the entire process of on-chip interconnects simulation. It is the purpose of this research to develop closed-form expressions for the frequency-dependent line parameters. The development of closed-from expressions is especially difficult due to the presence of lossy silicon substrate, which leads to the excitation of frequency-dependent horizontal currents (eddy currents). In the following chapters, the conductors are first chosen to have zero thickness and infinite conductivity in order to focus on the substrate loss effects. For conductors with finite thickness and conductivity, the contribution of the conducting strips will later be discussed separately.

3. ANALYSIS AND MODELING OF SINGLE ON-CHIP INTERCONNECTS

3.1. Introduction

The single microstrip line may be the simplest on-chip interconnect configuration but has fundamental importance. By examining the single line case, different mechanisms that contribute to the frequency-dependent line parameters can be carefully studied, and, accordingly the methodology for developing closed-form expressions can be formulated. The development of closed-form expressions is especially difficult for semiconducting silicon substrate, such as in typical CMOS and BiCMOS processes, due to the excitation of frequency-dependent horizontal currents (eddy currents) in the lossy substrate. A new modeling approach for developing closed-form expressions for the frequency-dependent line parameters of a single microstrip line is in our recent research [23].

In this chapter accurate closed-form expressions for the series impedance and shunt admittance line parameters are presented separately. The series impedance parameters $L(\omega)$ and $R(\omega)$ are developed using an extended complex image method, which can represent the silicon loss effects with sufficient accuracy. The shunt admittance parameters $C(\omega)$ and $G(\omega)$ are obtained using low- and high-frequency asymptotic static solutions based on the physical understanding of the corresponding equivalent circuit model.

3.2. Extraction of Series Impedance Line Parameters

Theoretically, the calculation of series impedance parameters $R(\omega)$ and $L(\omega)$ should take into account not only the effects due to semiconducting substrate but

also the effects of finite thicknesses and finite conductivities of the conducting strips. However, the latter effects have been extensively studied and the closed-form expressions for conductor loss and conductor skin effect are available. On the other hand, the frequency-dependent effects due to the silicon substrate are difficult to describe in terms of closed-form expressions. The contributions to the overall characteristics of microstrip interconnects due to the lossy silicon substrate and non-ideal conductor have shown to be approximately additive [16]. This allows us to concentrate on the more complicated silicon substrate loss effects. In the following sections, ideal conductors are assumed first in order to focus on the study of substrate loss effects.

Silicon substrates with varying doping levels or varying resistivities are used in modern ICs. Particularly, for substrates with low resistivity, the time-varying magnetic fields in the substrate give rise to frequency-dependent horizontal currents (eddy currents) in the substrate. At higher frequencies the presence of these substrate currents can lead to a significant reduction in series inductance and substantial increase in series resistance or loss. The evaluation of p.u.l. series impedance can be obtained by considering the complex equivalent inductance

$$L_e = L(\omega) + R(\omega)/j\omega = \Psi/I = \oint \vec{A} \cdot d\vec{l}/I \tag{3.1}$$

where I is the total current on the conductor, Ψ is the magnetic flux linkage associated with the interconnects, and $\vec{A}$ is the vector magnetic potential. For a z-directed current on the conducting strip, only the z-component of the vector magnetic potential $\vec{A}$ is non-zero. Therefore, L_e can be determined by solving for the current distribution given the vector magnetic potential on the conductor. A_z satisfies the quasi-static magnetic potential equation [12]

$$\nabla^2 A_z(x,y) - j\omega\mu_0\sigma_i A_z(x,y) = 0 \tag{3.2}$$

with the appropriate boundary conditions at the interface between the i-th and the $(i+1)$-th layer, i.e.,

$$\frac{\partial A_{i+1}(x,y)}{\partial y} - \frac{\partial A_i(x,y)}{\partial y} = \begin{cases} \mu_0 J_z & \text{if on strip} \\ 0 & \text{otherwise} \end{cases} \tag{3.3}$$

and

$$\frac{\partial A_{i+1}(x,y)}{\partial x} - \frac{\partial A_i(x,y)}{\partial x} = 0 \tag{3.4}$$

The equations above can be efficiently solved by a modified spectral domain approach [7].

Alternatively, this problem can be solved by applying a complex image theory [23], [24]. The motivation of using an image approach is that the complicated lossy substrate behavior can be approximately represented in terms of an image plane located at a complex distance from the oxide/silicon interface. With the use of the complex image approach, the static inductance formulas for the conventional microstrip line can be employed to calculate the frequency-dependent series impedance parameters.

3.2.1. Complex Image Approach

The image principle has been used for a long time in optics and electrostatics. The use of a conducting image plane with the source is an evident translation of the electromagnetic equations. However, there is no direct corresponding principle for the dielectric half-space problem. Initially motivated by the study of the effects of power lines above the conducting earth [27], [28] and in geophysics by the study of magnetic variations associated with ionospheric or magnetospheric currents [24], [29], complex image techniques have been developed to obtain approximate solutions that accurately describe the effects caused by the horizontal currents in the conducting earth. The beauty of the complex image concept is in its simple geometrical property in replacing the half-space by a certain image as a mirror to its

original source. This section will review the complex image theory and extend the equations originally for the open boundary medium case to the MIS structure case.

3.2.1.1. Basic Theory of Complex Image Approach

Conceptually, the essence of the complex image approach is to replace the finitely conducting medium by a perfectly conducting ground plane located at a complex depth h_{cplx}. The location of this complex image depth can be derived by several methods, one of which is to equate the z-directed wave impedances for normal incidence at the surface. The derivation of this method is illustrated in Figure 3.1. Figure 3.1(a) shows the configuration with air and a finitely conducting medium in the lower half space. Figure 3.1(b) shows its equivalent air-filled configuration but bounded by a perfectly conducting ground plane at the complex depth of h_{cplx}.

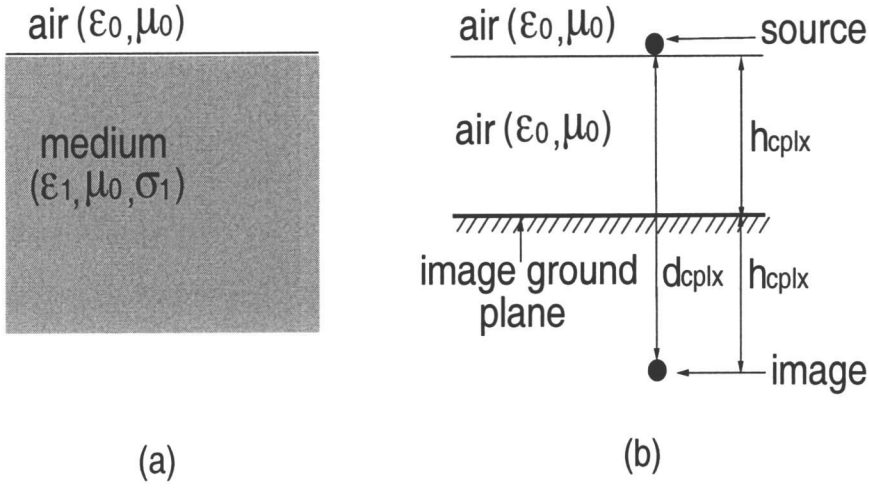


FIGURE 3.1. Illustration of complex image approach for structure with unbounded half space medium.

For case (a), the wave impedance for TE mode is [24]

$$Z_a = \frac{\eta_1}{(1 - \gamma_0^2/\gamma_1^2)^{1/2}} \tag{3.5}$$

where

$$\gamma_0^2 = -\omega^2 \mu_0 \epsilon_0 \tag{3.6}$$

$$\gamma_0^2 = -\omega^2 \mu_0 (\epsilon_1 - \frac{j\sigma_1}{\omega}) \tag{3.7}$$

and

$$\eta_1 = \sqrt{\frac{\mu_0}{\epsilon_1 - \frac{j\sigma_1}{\omega}}} \tag{3.8}$$

From transmission line theory it is known that a transmission line of length l with characteristic impedance Z_c transforms a load impedance Z_L into an input impedance as

$$Z_{in} = Z_c \frac{Z_L + Z_c \tanh(\gamma l)}{Z_c + Z_L \tanh(\gamma l)} \tag{3.9}$$

For case (b), since the perfect ground plane exists at distance h_{cplx}, the wave impedance for TE mode can be determined with (3.9) as

$$Z_b = \eta_0 \tanh(\gamma_0 h_{cplx}) \tag{3.10}$$

where $\eta_0 = \sqrt{\mu_0/\epsilon_0} = 120\pi$. When $|\gamma_0 h_{cplx}|$ is much smaller than 1, (3.10) can be simplified as

$$Z_b \approx \eta_0 \gamma_0 h_{cplx} \tag{3.11}$$

Equating (3.5) and (3.11) results in

$$\begin{aligned} h_{cplx} &= \frac{\eta_1}{\eta_0 \gamma_0 (1 - \eta_0^2/\eta_1^2)^{1/2}} \\ &= \frac{1}{\gamma_1 (1 - \eta_0^2/\eta_1^2)^{1/2}} \\ &= \frac{1}{(\gamma_1^2 - \gamma_0^2)^{1/2}} \\ &= \frac{1}{\sqrt{j\omega\mu_0\sigma_1}} \end{aligned} \tag{3.12}$$

Noting that the skin depth is defined as $\delta = 1/\sqrt{\pi f \mu_0 \sigma_1}$ and $\sqrt{j} = (1+j)/\sqrt{2}$, (3.12) can be rewritten as $h_{cplx} = \delta(1-j)/2$. Accordingly, the image depth is

$$d_{cplx,TE} = 2h_{cplx} = (1-j)\delta \tag{3.13}$$

The wave impedance for TM mode in case (a) is

$$Z_a = \eta_1(1 - \gamma_0^2/\gamma_1^2)^{1/2} \tag{3.14}$$

Then, the image depth for TM mode can be obtained as

$$d_{cplx,TM} = \frac{2}{\gamma_1}(1 - \gamma_0^2/\gamma_1^2)^{1/2} \tag{3.15}$$

For normal incidence, or if $|\gamma_1^2/\gamma_0^2| > 15$ [24], (3.13) and (3.15) are shown to be the same as

$$d_{cplx,TE} = d_{cplx,TM} = d_{cplx} = 2/\gamma_1 \tag{3.16}$$

When $\sigma_1 \gg \omega\epsilon_0\epsilon_{r,1}$, which is always satisfied in our case, $\gamma_1 \approx \sqrt{j\omega\mu_0\sigma_1}$. Therefore, in terms of skin depth defined earlier, d_{cplx} in (3.16) can be rewritten as

$$d_{cplx} = (1-j)\delta \tag{3.17}$$

This result shows the complex image depth for both TE and TM modes are identical.

3.2.1.2. Extension of Complex Image Approach to MIS Structure

In the following, the complex image approach is extended to MIS structures having an oxide-silicon substrate with ground plane.

First, a single layer substrate is considered bounded by a perfect ground plane. Figure 3.2 shows this configuration in (a) and an equivalent configuration in (b). In the following, TE mode propagation is considered. The derivation for TM mode is similar. For case (a), the wave impedance can be determined with (3.9) as

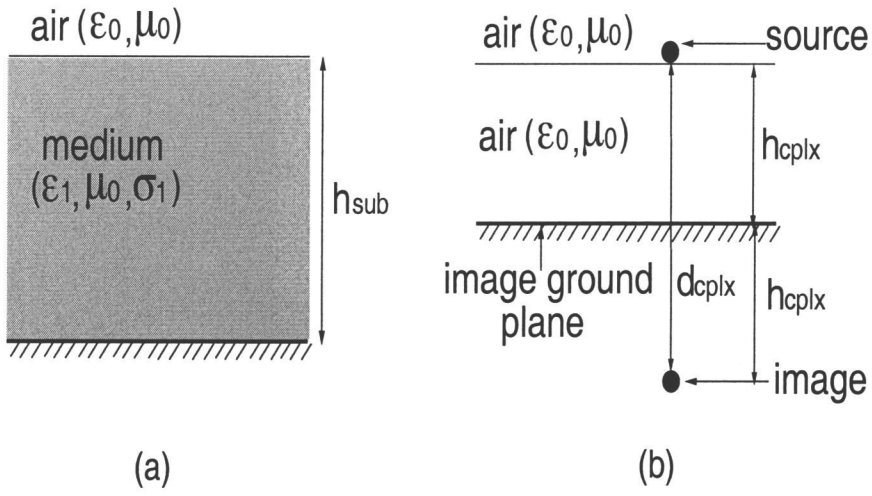


FIGURE 3.2. Extension of complex image approach for structure with bounded half plane medium.

$$Z_a = \frac{\eta_1}{(1-\gamma_0^2/\gamma_1^2)^{1/2}} \tanh(\gamma_1 h_{sub}) \tag{3.18}$$

For case (b), the wave impedance is the same as (3.10) and is repeated here

$$Z_b = \eta_0 \tanh(\gamma_0 h_{cplx}) \approx \eta_0 \gamma_0 h_{cplx} \tag{3.19}$$

Equating (3.18) and (3.19) results in

$$h_{cplx} = \frac{1-j}{2}\delta \tanh(\gamma_1 h_{sub}) \tag{3.20}$$

where $\gamma_1 \approx \sqrt{j\omega\mu_0\sigma_1}$ when $\sigma_1 \gg \omega\epsilon_0\epsilon_{r,1}$. Thus, (3.20) reduces to

$$\begin{aligned} h_{cplx} &= \frac{1-j}{2}\delta \tanh(\sqrt{j\omega\mu_0\sigma_1}h_{sub}) \\ &= \frac{1-j}{2}\delta \tanh(\frac{1+j}{\sqrt{2}}\frac{\sqrt{2}}{\sigma}h_{sub}) \\ &= \frac{1-j}{2}\delta \tanh[(1+j)h_{sub}/\sigma] \end{aligned} \tag{3.21}$$

Next, by adding an insulating layer, e.g., oxide layer, the effective complex distance at which an image ground plane is located is expressed as

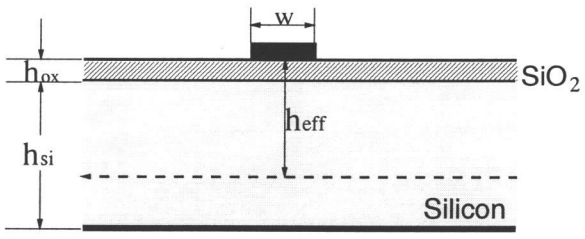


FIGURE 3.3. Illustration of the image ground plane for a single line MIS structure.

$$h_{eff} = h_{insulator} + \frac{1-j}{2}\delta \tanh[(1+j)h_{sub}/\delta] \tag{3.22}$$

h_{eff} is a function of frequency, silicon conductivity, as well as oxide/silicon geometrical parameters.

3.2.2. Extraction of R and L Line Parameters

As a result of applying the extended complex image approach to represent the silicon substrate loss effect, the physical oxide-silicon substrate can be replaced by an air medium but with a virtual image ground located at a complex distance h_{eff} from the oxide-silicon interface, as shown in Figure 3.3. In general, h_{eff} is expressed as (3.22). More specifically, for oxide-silicon substrate it is given by

$$h_{eff} = h_{ox} + \frac{1-j}{2}\delta \cdot \tanh[(1+j)h_{si}/\delta] \tag{3.23}$$

where h_{ox} is the oxide thickness, h_{si} is the thickness of the bulk silicon, and $\delta = 1/\sqrt{\pi f \mu_0 \sigma_{si}}$ is the skin depth of the bulk silicon. To illustrate the frequency-dependence of the effective height, Figure 3.4 shows the real part of h_{eff} for a microstrip line with different substrate conductivities. It can be seen that the image ground plane coincides with the real ground plane at very low frequencies and approaches to the oxide-silicon interface in the high frequency limit. It also shows that

for heavily doped (high conductivity) silicon substrates, the frequency-dependence of the effective height is more significant, as expected.

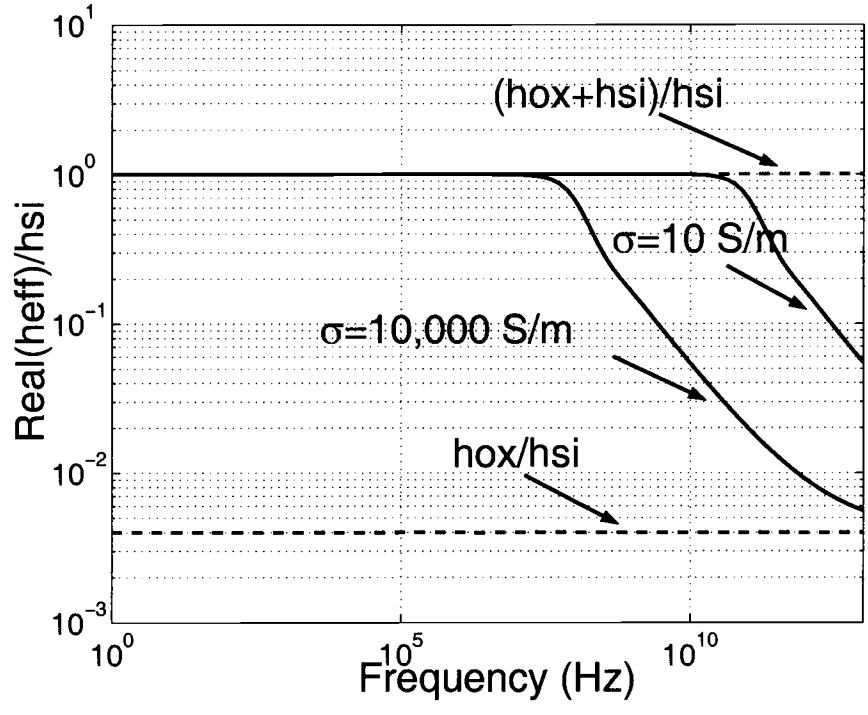


FIGURE 3.4. Illustration of the variation in effective height as a function of frequency

Figure 3.3 illustrates that a single microstrip line on oxide-silicon substrate can be approximately represented by a single microstrip at a distance h_{eff} above the image ground plane with oxide-silicon substrate removed. Therefore, the configuration becomes similar to a conventional microstrip line on single layer lossless dielectric (air), except for having a complex distance between the conductor strip and the ground plane. There are various well developed formulas for static inductance of the conventional single microstrip line. They can be directly used with the

complex effective height h_{eff} to calculate the complex equivalent inductance. (3.1) suggests that the complex equivalent inductance is in the form of

$$L_e = L(\omega) - j\frac{R(\omega)}{\omega} \tag{3.24}$$

Therefore, the series impedance line parameters $L(\omega)$ and $R(\omega)$ are determined as

$$L(\omega) = Re\{L_{cf}(w/h_{eff})\} \tag{3.25}$$

and

$$R(\omega) = -\omega Im\{L_{cf}(w/h_{eff})\} \tag{3.26}$$

where L_{cf} can be any suitable closed-form expression for the static inductance of the conventional single microstrip line on single layer lossless dielectric substrate.

3.2.3. Static Inductance Formulas

The conventional microstrip line configuration can be directly employed in the calculation of the MIS on-chip interconnect series impedance parameters with the lossy substrate effect being approximately represented by an effective complex image height, as stated earlier. Therefore, it is valuable to give a review of static inductance formulas for conventional microstrip line structures with lossless substrate. Figure 3.5 shows the configuration of a conventional microstrip with zero conductor thickness and lossless single layer substrate. It should be noted that this configuration is different from the on-chip interconnect structure, as shown in Figure 3.3.

Two viable means can be employed to calculate the static inductance. One is based on the characteristics of the conventional microstrip line. The alternative one is to use self and mutual partial inductance formulas.

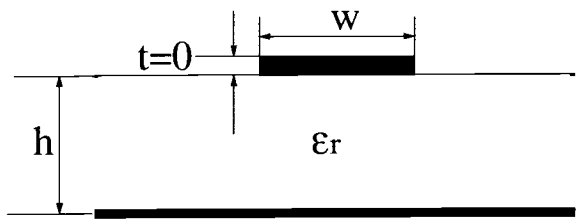


FIGURE 3.5. Conventional microstrip with lossless substrate and zero conductor thickness

For the conventional microstrip line, the formulas for calculating the characteristic impedance Z_c and the effective dielectric constant $\epsilon_{r,eff}$ have been well developed. Many of these types of formulas can be found in Appendix A. The static inductance can be calculated by directly using the following relationship

$$L = Z_c^{air}/c \tag{3.27}$$

where Z_c^{air} is the characteristic impedance of the transmission line with substrate medium removed and c is the light velocity in free space. Z_c is used to denote the characteristic impedance of the transmission line with dielectric substrate.

It should be noted that the various equations given in Appendix A are for the characteristic impedance of conventional microstrip lines on a lossless dielectric substrate. When they are used to calculate static inductance, the substrate medium needs to be assumed to be air. Therefore, various formulas for microstrip with dielectric substrate given in literature can be used to obtain Z_c^{air} by setting the dielectric constant of the substrate $\epsilon_r = 1$. The corresponding static inductance can then be calculated with (3.27). For example, using (A11) results in the static inductance formula as

$$L_0 = \frac{\mu_0}{4\pi} \ln \left\{ 1 + 32 \left(\frac{h}{w} \right)^2 \left[1 + \sqrt{1 + \left(\frac{\pi}{8} \frac{w}{h} \right)^2} \right] \right\} \tag{3.28}$$

where μ_0 is the permeability in free space ($4\pi \times 10^{-7} H/m$).

An alternative way is to use the partial self and mutual inductance formulas. An overview of partial inductance is in Appendix B. Figure 3.6 shows the configuration consisting of the source conductor and the image conductor. The static inductance formula can be formulated by the corresponding partial self and mutual inductance formulas

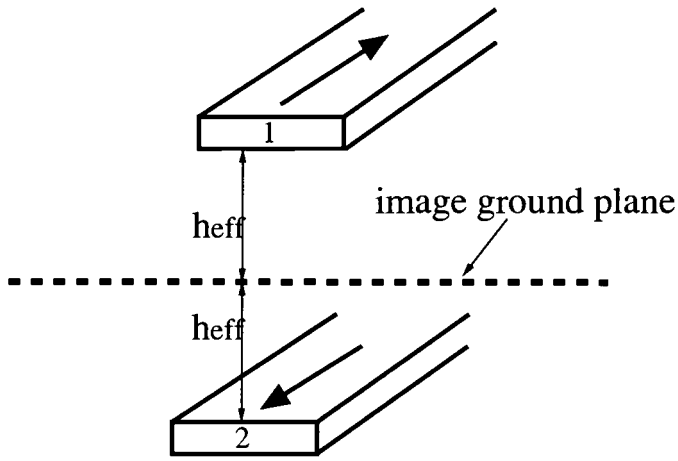


FIGURE 3.6. Static Inductance Calculation using partial self and mutual inductances.

$$L_0 = L_{11} - L_{12} \tag{3.29}$$

where L_{11} is the self partial inductance of the source conductor itself and L_{12} is the mutual partial inductance between the source conductor and the image conductor.

3.3. Modeling and Extraction of Shunt Admittance Line Parameters

The shunt admittance line parameters are formulated using corresponding lossless/static configurations with the aid of a physics-based equivalent circuit model

for shunt admittance. The lumped elements in the equivalent circuit can be calculated using various well developed static characteristic impedance formulas for a lossless microstrip line. The equivalent circuit exhibits the frequency-dependent behavior of the p.u.l. shunt admittance.

3.3.1. Equivalent Circuit Model for Shunt Admittance

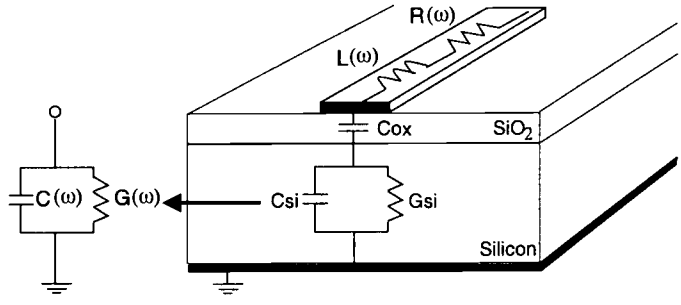


FIGURE 3.7. Equivalent circuit topology for the shunt admittance of single microstrip line on silicon.

Figure 3.7 shows an equivalent circuit model for the p.u.l. shunt admittance of a microstrip on-chip interconnect. The frequency-dependent behavior of the shunt admittance can be adequately represented in terms of an equivalent circuit consisting of three ideal lumped elements [12]. The physical origins of the circuit elements can be explained as follows: C_{ox} represents the capacitance due to the lossless oxide dielectric. C_{si} and G_{si} together can describe the semiconducting property of the silicon substrate, representing partly capacitive and partly conductive characteristics. This equivalent circuit not only provides an efficient CAD-oriented modeling approach but also suggests a way of calculating each element by using low- and high-frequency asymptotic solutions, as described in the following sections.

3.3.2. Extraction of G and C Line Parameters

To determine the frequency-dependent p.u.l. shunt admittance components $C(\omega)$ and $G(\omega)$, the electric behavior of the substrate in the low and high frequency limits is considered. At sufficiently low frequencies for which the relaxation frequency $\sigma_{si}/\epsilon_{si}$ of the silicon substrate is much higher than the operating frequency, the substrate behaves almost like a perfect ground plane. The resulting shunt capacitance $C(\omega) = C_{ox}$ is that of a microstrip of height h_{ox} and with SiO_2 only as dielectric medium. The oxide capacitance can be determined using readily available closed-form expressions. In the high frequency limit, the shunt conduction current in the lossy substrate can be neglected compared to the shunt displacement current. The resulting problem then reduces to solving the capacitance C_∞ of a lossless two-layer microstrip.

Knowing C_{ox} and C_∞ and using the equivalent circuit shown in Figure 3.7, the silicon capacitance is then obtained as

$$C_{si} = \frac{C_{ox}C_\infty}{C_{ox} - C_\infty} \tag{3.30}$$

The corresponding silicon shunt conductance G_{si} is determined using the relaxation time constant $\epsilon_{si}/\sigma_{si}$ as

$$G_{si} = \frac{\sigma_{si}}{\epsilon_{si}} C_{si} \tag{3.31}$$

By examining the equivalence of the equivalent circuit topology and the distributed shunt admittance parameters, one may readily calculate the shunt admittance components in form of closed-form expressions as

$$G(\omega) = \frac{\omega^2 G_{si} C_{ox}^2}{G_{si}^2 + \omega^2 (C_{si} + C_{ox})^2} \tag{3.32}$$

and

$$C(\omega) = \frac{\omega^2 C_{si} C_{ox}(C_{si} + C_{ox}) + C_{ox} G_{si}^2}{G_{si}^2 + \omega^2 (C_{si} + C_{ox})^2} \tag{3.33}$$

where C_{ox}, C_{si}, and G_{si} are available in terms of closed-form expressions.

3.3.3. Static Capacitance Formulas

For single microstrip on-chip interconnects, the static capacitance formulas are employed at both low- and high-frequency limits to determine the asymptotic solutions. Although the exact solution for the capacitance between a conductor strip of width W and a distance H above a ground plane can be obtained from rigorous EM analysis [10], it is desirable to have much less complicated yet adequately accurate formulas. A number of investigators have proposed such formulas to calculate the single microstrip line static capacitance. Basically, these formulas are based on the characteristics of the conventional microstrip line structure, as listed in Appendix A. In general, the static capacitance of a microstrip line can be calculated by

$$C^{air} = \frac{\sqrt{\epsilon_{r,eff}}}{Z_c c} \tag{3.34}$$

where C^{air} denotes the static capacitance for the microstrip line with substrate, $\epsilon_{r,eff}$ is the effective dielectric constant, and c is the speed of light in free space.

3.3.4. Multilayer Dielectrics

The prior section has dealt with static capacitance calculation for conventional microstrip where only one dielectric layer exists. Those formulas can be directly used to determine the low-frequency asymptotic solution. However, they are not directly applicable for high-frequency asymptotic configuration, where a multilayer dielectric microstrip structure needs to be considered. Therefore, a way

of determining the effective dielectric constant in multilayer dielectrics should be developed. The effective dielectric constant, $\epsilon_{r,eff}$, may be evaluated by EM analysis. However, it is desirable to obtain a compact expression to calculate $\epsilon_{r,eff}$. A simple yet accurate formula for effective dielectric constant for two-layer substrate microstrip structure was developed in [40] based on the quasi-TEM assumption and superposition of partial capacitance. It is adopted by this thesis work to obtain the high-frequency asymptotic capacitance solution, and thus it is reviewed here.

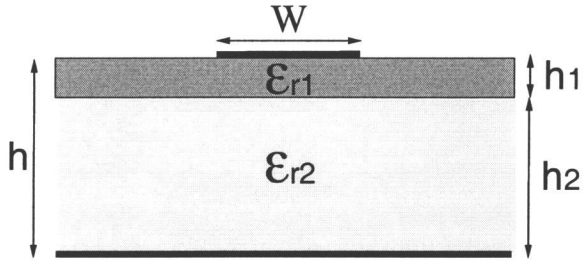


FIGURE 3.8. Microstrip line on double layer dielectric

In the microstrip with a two-layer dielectric substrate shown in Figure 3.8, the dielectric/dielectric boundary may be regarded as an electric wall under the quasi-TEM assumption. Hence, the capacitance of each layer is in series connection, which results in the equivalent dielectric constant for two dielectric layers as

$$\epsilon_{eq} = \frac{d_1 + d_2}{d_1/\epsilon_{r1} + d_2/\epsilon_{r2}} \tag{3.35}$$

where ϵ_{r1} and ϵ_{r2} are the relative dielectric constants for the two layers, respectively. d_1 and d_2 are the mapped distances in the conformal mapping plane corresponding to the thickness of the two layers in the real plane. They can be expressed as

$$d_1 = \frac{K(k_1)}{K'(k_1)} \tag{3.36}$$

$$d_2 = \frac{K(k)}{K'(k)} - \frac{K(k_1)}{K'(k_1)} \tag{3.37}$$

where, $k_1 = 1/\cosh\left(\frac{\pi w}{4h_1}\right)$, $k = 1/\cosh\left(\frac{\pi w}{4h}\right)$, and $K(k)$ is the complete elliptical integral of the first kind introduced by the conformal mapping. Hence, the formula for effective dielectric constant of two dielectric layers can be written as

$$\epsilon_{r,eff} = 1 + 2(\epsilon_{eq} - 1)K_{air}\frac{K'(k)}{K(k)}, \tag{3.38}$$

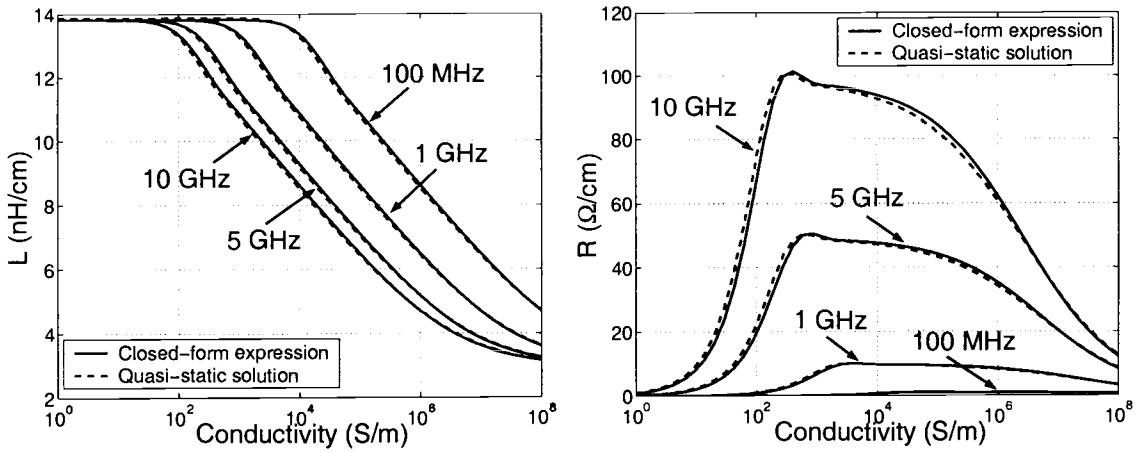
where $K_{air} = \epsilon_0 c Z_c^{air}$ and Z_c^{air} stands for the impedance of an air-filled microstrip line, and can be accurately evaluated by the formula proposed in [30].

These static capacitance formulas, developed for one layer substrate, can be applied with the equations above to calculate the double dielectric layer capacitance. Consequently, the high-frequency asymptotic capacitance can be determined in terms of closed-form expressions.

3.4. Simulation Results

The proposed closed-form expressions have been applied to various cases. To illustrate the accuracy of the closed-form expressions, the frequency-dependent $R(\omega)$, $L(\omega)$, $G(\omega)$ and $C(\omega)$ line parameters of a microstrip line on silicon substrate have been calculated and compared with the solution obtained by electromagnetic simulation.

Figure 3.9 and Figure 3.10 show the simulation results for the frequency-dependent line parameters of a microstrip line on oxide-silicon substrate with $w = 4\mu m$, $h_{ox} = 2\mu m$, $\epsilon_{ox} = 3.9$, $h_{si} = 500\mu m$, and $\epsilon_{si} = 11.8$. The conductor here is assumed to be ideal and to have zero thickness and infinite conductivity. To elucidate the applicability of the proposed closed-form expressions for wide range silicon conductivities, Figure 3.9 and Figure 3.10 show the distributed line parameters as functions of silicon conductivity at 100MHz, 1GHz, 5GHz, and 10GHz.

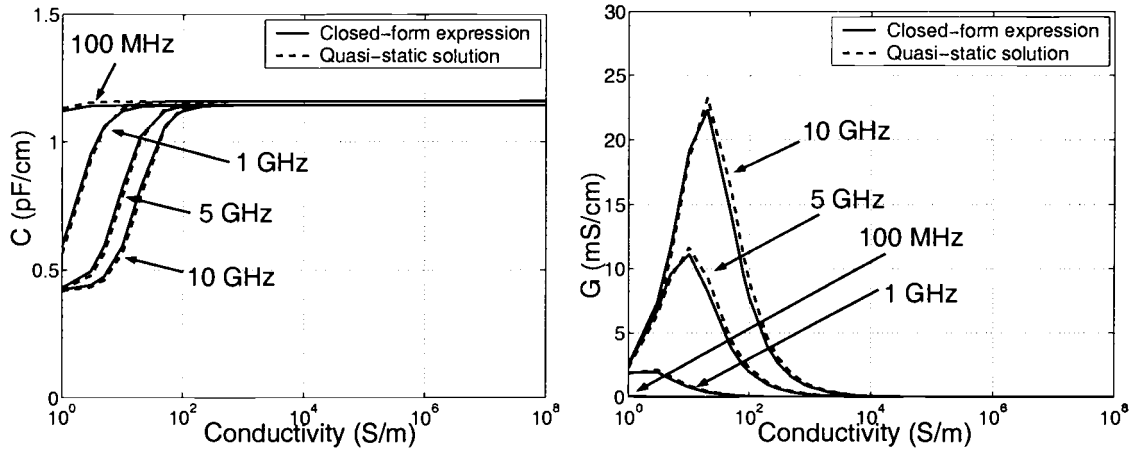


(a) (b)

FIGURE 3.9. Series impedance parameters of a microstrip line on silicon substrate with $w = 4\mu m$, $h_{ox} = 2\mu m$, $\epsilon_{ox} = 3.9$, $h_{si} = 500\mu m$, and $\epsilon_{si} = 11.8$ (a)distributed series inductance L and (b)distributed series resistance R as functions of silicon substrate conductivity

The closed-form expressions are compared with quasi-static EM solutions, which are obtained by solving (3.2) with a spectral domain approach [8].

Figures 3.9(a) and (b) show respectively the p.u.l. L and R as functions of silicon conductivity. It can been seen that the proposed closed-form expressions agree well with the quasi-static EM solutions. The difference between the two results is found to be less than three percent over a wide range of substrate conductivities as well as frequencies. It is worth noticing that the inductance parameter decreases as silicon conductivity increases or frequency increases. This is expected because the silicon substrate skin effect has a significant impact on the overall characteristics particularly when the operating frequency is high and/or the silicon is moderately or highly doped. The lossy silicon substrate can give rise to eddy currents in the substrate and therefore can lead to a reduction in inductance and increase in resistance. It should be pointed out here that the resistance shown in the figure is



(a) (b)

FIGURE 3.10. Shunt admittance parameters of a microstrip line on silicon substrate with $w = 4\mu m$, $h_{ox} = 2\mu m$, $\epsilon_{ox} = 3.9$, $h_{si} = 500\mu m$, and $\epsilon_{si} = 11.8$ (a)distributed shunt capacitance C and (b)distributed shunt conductance G as functions of silicon substrate conductivity

obtained from the imaginary part of the complex inductance and thus it only represents the resistance due to substrate skin effect. For practical conductors with finite conductivity and finite thickness, the contribution of the conducting strip including the metallic ohmic loss and conductor skin effect to the overall R can be calculated separately and added to the R shown here. It is also interesting to see that, unlike L varying monotonically, for a given frequency, R reaches a maximum at a certain silicon doping level.

Figures 3.10(a) and (b) show respectively the p.u.l. C and G for the same microstrip configuration. Good agreement can be seen over the entire simulation range. The closed-form solutions are found to be within about five percent when compared with the quasi-static EM solutions. It should be noted that, in general, the accuracy of C and G directly depends on the accuracy of the available closed-

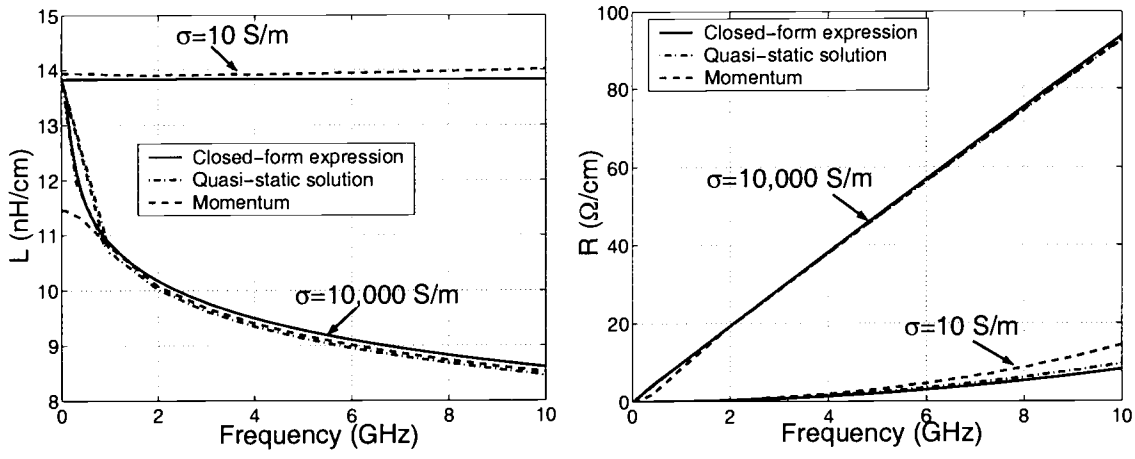
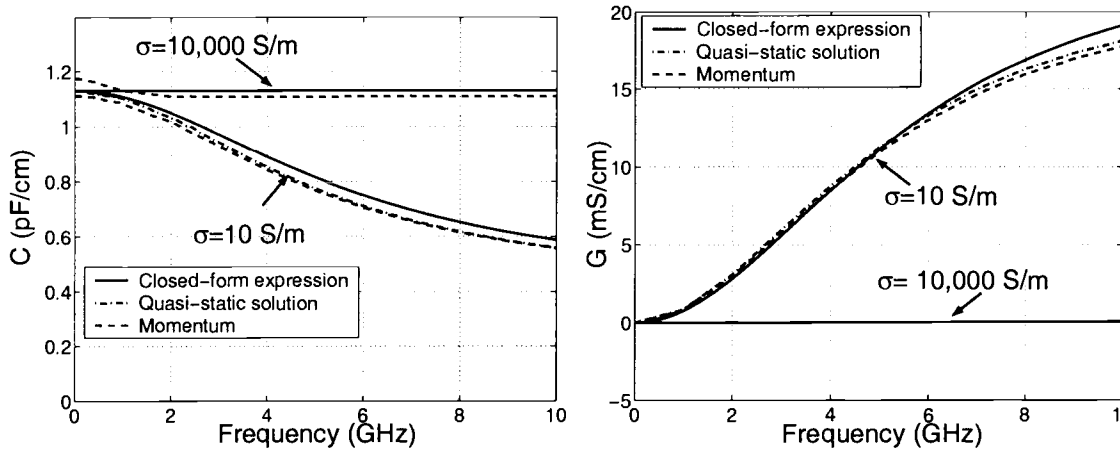


FIGURE 3.11. Frequency-dependent series impedance parameters of a microstrip line on low-conductivity and high-conductivity silicon substrate with $w = 4\mu m$, $h_{ox} = 2\mu m$, $\epsilon_{ox} = 3.9$, $h_{si} = 500\mu m$, and $\epsilon_{si} = 11.8$ (a)$L(\omega)$ and (b)$R(\omega)$.

form expressions for the p.u.l. capacitance of the lossless single and double-layer microstrip lines. C is seen to be almost a constant when the silicon conductivity is high enough. This can be explained by looking at the equivalent circuit for shunt admittance shown in Figure 3.7. For high conductivities, the silicon substrate works virtually as a ground and thus the oxide capacitance dominates over the silicon capacitance. Similar to R, G does not vary monotonically. G may be significant only when operating frequency is high and the silicon conductivity is moderate to low.

To further validate the developed closed-from expressions, $R(\omega)$, $L(\omega)$, $G(\omega)$ and $C(\omega)$ are calculated as functions of frequencies and compared with both quasi-static EM solutions and the results obtained by the rigorous full-wave EM field solver Agilent Momentum [41]. The validations of series impedance parameters and shunt admittance parameters are shown in Figure 3.11 and Figure 3.12, respectively. The



(a) (b)

FIGURE 3.12. Frequency-dependent shunt admittance parameters of a microstrip line on low-conductivity and high-conductivity silicon substrate with $w = 4\mu m$, $h_{ox} = 2\mu m$, $\epsilon_{ox} = 3.9$, $h_{si} = 500\mu m$, and $\epsilon_{si} = 11.8$ (a)$C(\omega)$ and (b)$G(\omega)$.

proposed models, generally speaking, are in considerably good agreement with both quasi-static EM solutions and full-wave Momentum results. Moreover, these figures explicitly demonstrate the significant frequency dependence in $R(\omega)$ and $L(\omega)$ for large substrate conductivities and in $G(\omega)$ and $C(\omega)$ for low substrate conductivities.

4. ANALYSIS AND MODELING OF COUPLED ON-CHIP INTERCONNECTS

4.1. Introduction

Figure 4.1 shows the typical configuration of coupled on-chip interconnects on silicon substrate. With the presence of oxide-silicon double-layer substrate, the field distribution in a MIS coupled on-chip interconnect system is complicated [3]. Extensive studies have been done to obtain the even and odd mode characteristics of conventional symmetric coupled microstrip line with only one lossless substrate layer, for example, [30], [43]. However, there have not been complete closed-form expressions reported for MIS coupled on-chip structure. For substrates with low resistivity, the time-varying magnetic fields in the substrate give rise to frequency-dependent eddy currents, which are non-uniform and functions of operating frequency and substrate conductivity. The eddy currents become more significant as frequency goes to GHz range, and thus can result in significant reduction in inductance and substantial increase in series resistance.

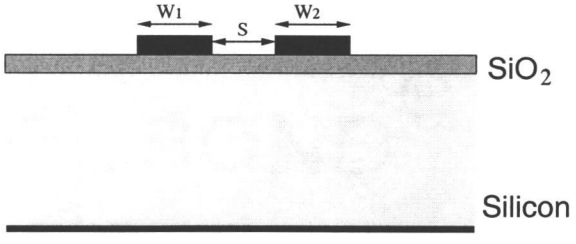


FIGURE 4.1. Coupled on-chip interconnects on silicon substrate.

This chapter presents the development of closed-form expressions for the frequency-dependent line parameter matrices $[R(\omega)]$, $[L(\omega)]$, $[G(\omega)]$, and $[C(\omega)]$ of coupled microstrip on-chip interconects. The complex image approach is extended to apply for the coupled line case. Two-port static inductance formulas are used with effective complex height to calculate the complex inductance matrix, from which $[R(\omega)]$ and $[L(\omega)]$ can be extracted. The shunt admittance matrices $[G(\omega)]$ and $[C(\omega)]$ are developed using the high- and low-frequency asymptotic solutions with the aid of an equivalent lumped circuit model for shunt admittance parameters. A simple yet efficient approach using $\triangle$-Y transforms is applied to extract the capacitance network.

4.2. Extraction of Series Impedance Matrices

4.2.1. Closed-form Expressions for [R] and [L]

The frequency-dependent series impedance parameters can be formulated in terms of the corresponding static configurations with the aid of the extended complex image approach. In general, the static inductance formulas are used with the effective complex height h_{eff} to compute the complex equivalent inductance matrix. Similar to what has been done in the single line case, the frequency-dependent p.u.l. complex inductance matrix $[L(\omega)]+[R(\omega)]/(j\omega)$ can be calculated using any suitable two-port static inductance formulas. The series inductance matrix and resistance matrix can be determined respectively as

$$[L(\omega)] = Re\{[L_{cf}]\} \tag{4.1}$$

and

$$[R(\omega)] = -\omega Im\{[L_{cf}]\} \tag{4.2}$$

where $[L_{cf}]$ can be any appropriate two-port static/lossless closed-form inductance formula.

4.2.2. Two-port Static Inductance Formulas

There are various ways to calculate the two-port static inductance matrix for the coupled line case.

One approach is to use the partial inductance formulas, which results in good extraction results of the frequency-dependent series impedance and is valid for general asymmetric coupled lines. Figure 4.2 illustrates the configuration of coupled on-chip interconnects with the lossy substrate being replaced by an image ground located at a complex distance h_{eff} from the oxide-silicon interface. This is a four conductor system, and the two-port inductance matrix can be determined as

$$[L_{cf}] = \begin{bmatrix} L_{11} - L_{13} & L_{12} - L_{14} \\ L_{12} - L_{23} & L_{22} - L_{24} \end{bmatrix} \tag{4.3}$$

where L_{11} and L_{22} are the partial self inductances, L_{13}, L_{12}, L_{14}, L_{23} and L_{24} are the partial mutual inductances. All these partial self and mutual inductances can be readily calculated using closed-form static inductance formulas, as given, for example, [44] and [45], but with the effective complex distances between conductors.

Alternatively, the closed-form expressions for the characteristics of the conventional microstrip line can be used. There have been years of intensive work on the static and frequency-dependent characteristics of conventional parallel coupled microstrip lines. The first reliable numerical static solution on coupled microstrip transmission line characteristics was proposed in 1968 by Bryant and Weiss [47]. After that, the most accurate and generally valid static model of coupled microstrips was given by Hammerstad and Jensen in 1984 [30]. As part of the efforts in proposing wide-range design equations for frequency-dependent characteristics of coupled

microstrip lines, Kirschning later remodeled the static odd mode parameters of Hammerstad's formulas for an improved accuracy of 0.5 percentage over the range of validity [43]. For example, Kirschning [43] proposed a set of equations to calculate the odd and even mode characteristics of symmetric coupled microstrip line. A full description of Kirschning's formulas is given in [43]. The range of validity to which the claimed accuracies apply is

$$0.1 \leq u \leq 10, \quad 0.1 \leq g \leq 10, \quad 1 \leq \epsilon_r \leq 18 \tag{4.4}$$

where $u = w/h$ denotes normalized strip width and $g = s/h$ denotes normalized spacing, h is the substrate thickness and ϵ_r is the dielectric constant of the substrate. Kirschning's formulas calculate four parameters, Zc^{air}_{even}, Zc^{air}_{odd}, $\epsilon_{eff,even}$ and $\epsilon_{eff,odd}$ in closed-form equations. The claimed accuracies, when in range of applicability (4.4), are 0.6%, 0.6%, 0.7% and 0.5% for the above four parameters, respectively. In terms of the two-port inductance matrix

$$[L] = \begin{bmatrix} L_{11} & L_{12} \\ L_{12} & L_{11} \end{bmatrix} \tag{4.5}$$

the characteristic impedances and effective dielectric constants can expressed as,

$$Zc^{air}_{even} = \sqrt{\frac{L_{11} + L_{12}}{C_{11} + C_{12}}} \tag{4.6}$$

$$v^{-1}_{even} = \frac{\sqrt{\epsilon_{eff,even}}}{c} = \sqrt{(L_{11} + L_{12})(C_{11} + C_{12})} \tag{4.7}$$

for the even mode and

$$Zc^{air}_{odd} = \sqrt{\frac{L_{11} - L_{12}}{C_{11} - C_{12}}} \tag{4.8}$$

$$v^{-1}_{even} = \frac{\sqrt{\epsilon_{eff,odd}}}{c} = \sqrt{(L_{11} - L_{12})(C_{11} - C_{12})} \tag{4.9}$$

for the odd mode, where c is the speed of light in free space. Hence, the mutual and self inductance elements in the inductance matrix can be determined from the even and odd mode characteristics as

$$L_{11} = \frac{Zc_{even}^{air} \cdot v_{even}^{-1} + Zc_{odd}^{air} \cdot v_{odd}^{-1}}{2} \tag{4.10}$$

$$L_{12} = \frac{Zc_{even}^{air} \cdot v_{even}^{-1} - Zc_{odd}^{air} \cdot v_{odd}^{-1}}{2} \tag{4.11}$$

However, this type of static solution is only given for the symmetric coupled line case and its applicability is limited by 4.4. The partial inductance method does not have this limitation.

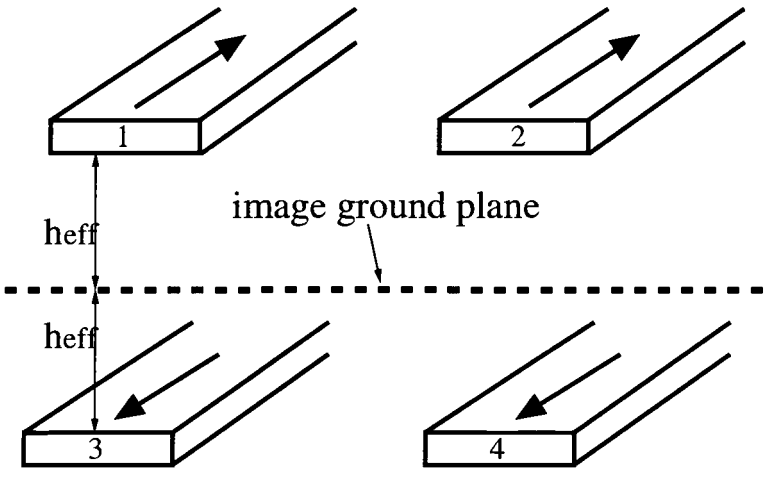


FIGURE 4.2. Complex inductance calculation using image method.

4.3. Modeling and Extraction of Shunt Admittance Matrices

Similar to the single line case, for the coupled microstrip line the shunt admittance parameters can also be formulated in terms of corresponding lossless/static

configurations in the low- and high-frequency limits, for which closed-form formulas are available. It should be noted that the overall accuracy of the p.u.l. shunt admittance directly depends on the accuracy of the static formulas.

4.3.1. Broadband Equivalent Circuit Model for Shunt Admittance

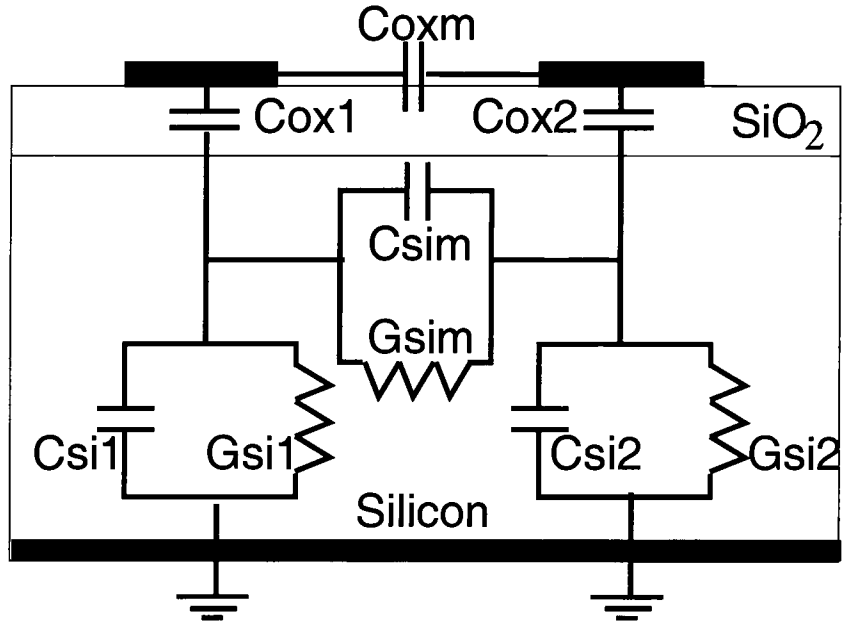


FIGURE 4.3. Equivalent circuit for p.u.l. shunt admittance of coupled microstrip on-chip interconnects

Figure 4.3 shows the equivalent circuit topology for the shunt admittance network of coupled on-chip interconnects. This model was proposed [12] based upon the physical substrate structure shown in Figure 4.1. In this model, C_{ox1} and

C_{ox2} represent the oxide capacitances between the conductor strips and the bulk substrate, and C_{oxm} represents the capacitive coupling through the oxide layer as well as air. The part in the silicon substrate has the same two-port π-like topology as that in the oxide layer except that each capacitance is replaced by a parallel connection of a capacitance and a conductance to account for the lossy nature of the silicon substrate. This equivalent circuit model was proposed with original intention to extract the lumped circuit elements from the frequency-dependent line parameters obtained by EM analysis. It was found to be a good broadband model, which can fit the EM data fairly well up to around 20 GHz. Meanwhile, this model provides a way to develop closed-form expressions for the frequency-dependent line parameters for the two-port shunt admittance network.

4.3.2. Calculation of [C] and [G]

At sufficiently low frequencies, the displacement currents are negligible compared with the conduction currents and, thus, the lossy substrate behaves nearly as a ground plane. The resulting shunt capacitance network is that of a coupled-line microstrip with oxide only. Therefore the circuit topology reduces to a capacitance network due to oxide only, $[C_{ox}]$. In the high frequency limit, the conduction currents are negligible compared with the displacement currents in the lossy substrate. The resulting problem reduces to solving for an overall capacitance matrix $[C_{\infty}]$ of a two-layer lossless coupled microstrip line.

Having both $[C_{ox}]$ and $[C_{\infty}]$ available, the remaining capacitance elements C_{si1}, C_{sim} and C_{si2} can be readily extracted by using $\triangle$-Y transforms. The corresponding conductance elements in the silicon substrate can then be obtained using the relaxation time constant as

$$G_{si_{1,2,m}} = \frac{\sigma_{si}}{\epsilon_{si}} C_{si_{1,2,m}} \tag{4.12}$$

With all lumped circuit elements known in the equivalent circuit topology, the overall two-port shunt admittance matrix $[Y(\omega)]$ is given by

$$[Y(\omega)] = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \tag{4.13}$$

with matrix elements given by

$$Y_{11} = \frac{1}{Z_2} + \frac{1}{(Z_3//Z_6 + Z_5)//Z_4 + Z_1} \tag{4.14}$$

$$Y_{12} = -\frac{1}{Z_2} - \frac{Z_4 Z_6}{[Z_3 + Z_6//(Z_5 + Z_1//Z_4)](Z_5 + Z_6 + Z_1//Z_4)(Z_1 + Z4)} \tag{4.15}$$

$$Y_{21} = -\frac{1}{Z_2} - \frac{Z_4 Z_6}{[Z_1 + Z_4//(Z_5 + Z_3//Z_6)](Z_5 + Z_4 + Z_3//Z_6)(Z_3 + Z6)} \tag{4.16}$$

$$Y_{22} = \frac{1}{Z_2} + \frac{1}{(Z_1//Z_4 + Z_5)//Z_6 + Z_3} \tag{4.17}$$

where $Z_1 = 1/(j\omega C_{ox1})$, $Z_2 = 1/(j\omega C_{oxm})$, $Z_3 = 1/(j\omega C_{ox2})$, $Z_4 = 1/(G_{si1} + j\omega C_{si1})$, $Z_5 = 1/(G_{sim} + j\omega C_{sim})$, and $Z_6 = 1/(G_{si2} + j\omega C_{si2})$. The notation // stands for a parallel connection of two impedances. Hence, the shunt conductance matrix and capacitance matrix can be determined respectively as

$$[G(\omega)] = Re\{[Y]\} \tag{4.18}$$

and

$$[C(\omega)] = Im\{[Y]\}/\omega \tag{4.19}$$

4.3.3. Two-Port Static Capacitance in the Frequency Limits

Since the closed-form expressions for the shunt admittance parameters are developed using low- and high-frequency asymptotic solutions, it becomes important to have appropriate approaches to calculate the two-port static capacitance networks, i.e., $[C_{ox}]$ in the low-frequency limit and $[C_{\infty}]$ in the high-frequency limit.

4.3.3.1. Low-frequency Asymptotic Solutions

The calculation of the static capacitance network can be derived from the solutions of static characteristics of microstrip coupled lines, which calculate the characteristic impedance and effective dielectric constant for even and odd modes. In this thesis work, Kirschning's closed-form expressions [43] for static characteristics of coupled microstrip lines have been adopted to calculate the two-port static capacitance network in the low frequency limit.

For symmetric coupled lines, the two-port capacitance can be written as

$$[C] = \begin{bmatrix} C_{11} & C_{12} \\ C_{12} & C_{11} \end{bmatrix} \tag{4.20}$$

It should be noted that by definitions, C_{11} is a positive value and C_{12} is a negative value. Knowing the equations (4.6), (4.7), (4.8) and (4.9), the matrix elements in the two-port capacitance matrix can be determined from the even and odd mode characteristics as can be determined from the even and odd mode characteristics as

$$C_{11} = \frac{[Zc_{even} \cdot v_{even}]^{-1} + [(Zc_{odd} \cdot v_{odd}]^{-1}}{2} \tag{4.21}$$

$$C_{12} = \frac{[Zc_{even} \cdot v_{even}]^{-1} - [(Zc_{odd} \cdot v_{odd}]^{-1}}{2} \tag{4.22}$$

4.3.3.2. High-frequency Asymptotic Solutions

In order to obtain high-frequency asymptotic solutions, coupled lines on multilayer dielectrics needs to be considered. $[C_\infty]$, in general, is difficult to calculate. Typically the silicon substrate has a thickness of several hundred μm, which leads to a very small ratio of W/H and is beyond the validity range of most applicable formulas. Although a compact closed-form expression has been successfully applied for a single line on multilayer dielectrics in section 3.3.4, it may not be suitable for coupled line case, where very small ratio of W/H with typical values of 0.01-0.05. For

example, Kirschning's formulas were proposed for a single layer configuration and has a certain range of validity in dimensions. They are suitable for low-frequency asymptotic solution while they are not applicable for high-frequency asymptotic solution. One of the possible approaches to accurately determine the high-frequency asymptotic solution is to use a quasi-static spectral domain approach (SDA) as described in Appendix C. It should be emphasized here that if applicable static compact closed-form expressions are available and found to be accurate to deal with small ratio of W/H, the quasi-static SDA may be replaced.

4.3.4. Two-Port Capacitive Network Extraction using △-Y Transforms

In the high-frequency limit, the capacitance network can be determined as $[C_\infty]$. Meanwhile, $[C_\infty]$ is also equivalent to a purely capacitive network consisting of C_{ox1}, C_{oxm}, C_{ox2}, C_{si1}, C_{sim} and C_{si2}, as shown in Figure 4.3. The task here is to extract C_{si1}, C_{sim} and C_{si2}, given $[C_{ox}]$ and $[C_\infty]$. This problem may be addressed by directly solving an 8-th order equation or using optimization techniques. However, computational difficulties may occur, such as algorithm stability and convergence. Alternatively, a simple yet fast and efficient way of extracting all the capacitance elements is developed employing a basic circuit theory, △-Y transform.

In terms of the lumped circuit elements in Figure 4.3, the low-frequency asymptotic solution $[C_{ox}]$ can be written as

$$[C_{ox}] = \begin{bmatrix} C_{ox1} + C_{oxm} & -C_{oxm} \\ -C_{oxm} & C_{ox2} + C_{oxm} \end{bmatrix} \tag{4.23}$$

The high-frequency asymptotic solution $[C_\infty]$ is

$$[C_\infty] = \begin{bmatrix} C_a + C_c & -C_c \\ -C_c & C_b + C_c \end{bmatrix} \tag{4.24}$$

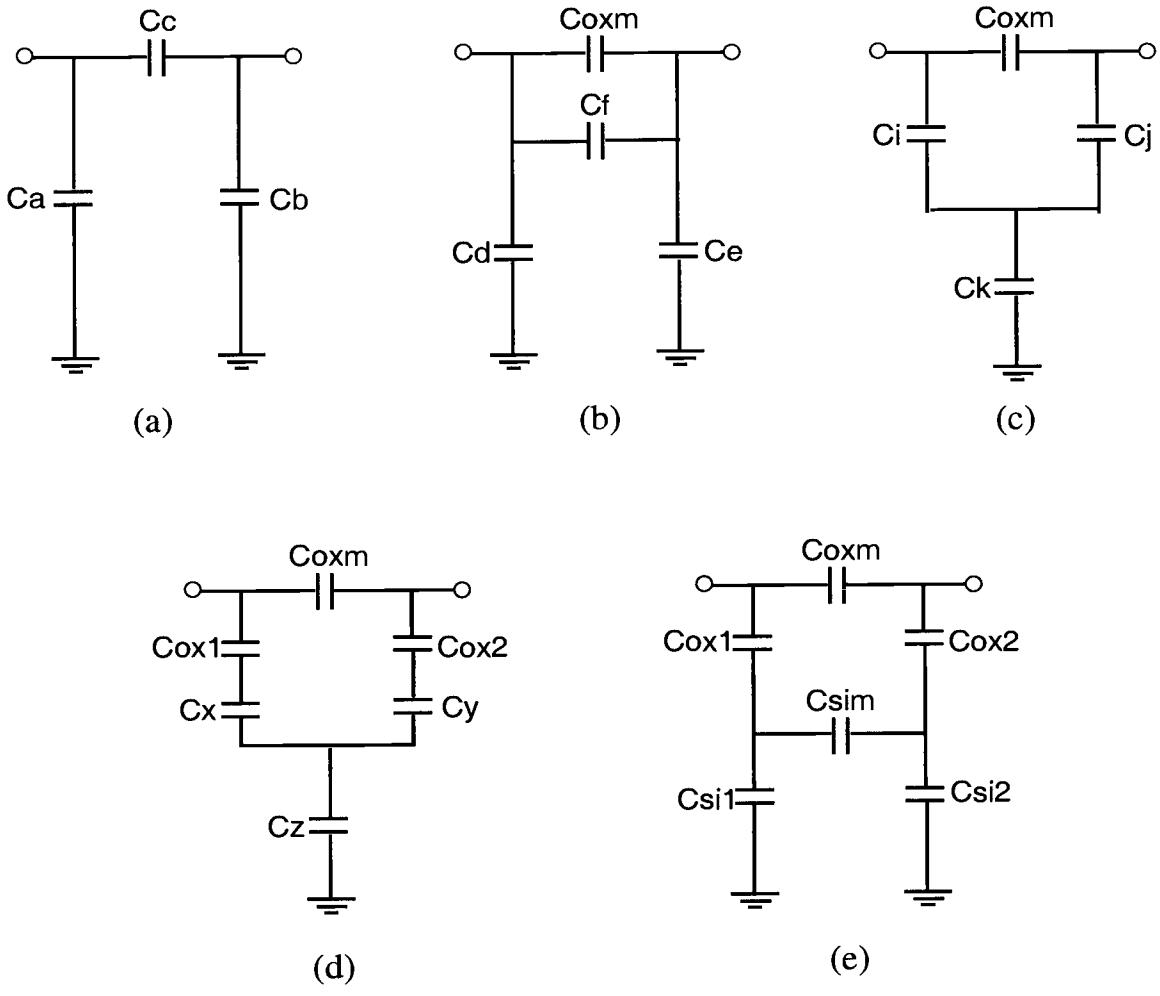


FIGURE 4.4. Capacitance network extraction using Δ-Y transform

Knowing $[C_{ox}]$ and $[C_{\infty}]$, the remaining unknown circuit elements, namely, C_{si1}, C_{sim} and C_{si2}, can be derived in a compact way by applying multiple Δ-Y transforms. The procedure is illustrated in Figure 4.4.

First, since the capacitance network shown in Figure 4.4 (a) is known from the high-frequency asymptotic static solution, C_c can be split into two parallel connected capacitances C_{oxm} and C_f, as shown in (a) and (b). C_d, C_e and C_f can be simply written as

$$\begin{cases} C_f = C_c - C_m \\ C_d = C_a \\ C_e = C_b \end{cases} \tag{4.25}$$

Second, transform the $\triangle$ network consisting of C_d, C_e and C_f into an equivalent Y network consisting of C_i, C_j and C_k, as shown in (b) and (c). The transform equations are

$$\begin{cases} C_i = (C_d C_e + C_d C_f + C_e C_f)/C_e \\ C_j = (C_d C_e + C_d C_f + C_e C_f)/C_d \\ C_k = (C_d C_e + C_d C_f + C_e C_f)/C_f \end{cases} \tag{4.26}$$

Next, splitting C_i and C_j into two series connections of C_x and C_{ox1}, C_y and C_{ox2} respectively results in the topology shown in (d). The corresponding equations are

$$\begin{cases} C_x = C_i C_{ox1}/(C_{ox1} - C_i) \\ C_y = C_j C_{ox2}/(C_{ox2} - C_j) \\ C_z = C_k \end{cases} \tag{4.27}$$

Finally, by applying $\triangle$-Y transform again, all unknown capacitances C_{si1}, C_{sim} and C_{si2} can be determined as

$$\begin{cases} C_{sim} = C_x C_y/(C_x + C_y + C_z) \\ C_{si1} = C_x C_z/(C_x + C_y + C_z) \\ C_{si2} = C_y C_z/(C_x + C_y + C_z) \end{cases} \tag{4.28}$$

4.4. Simulation Results

To demonstrate the validity of the proposed modeling approach for coupled microstrip on-chip interconnects, four cases of symmetric coupled interconnects with different combinations of conductor dimensions and substrate conductivities are considered here. The simulation results are shown in Figures 4.5-4.8. The two-port

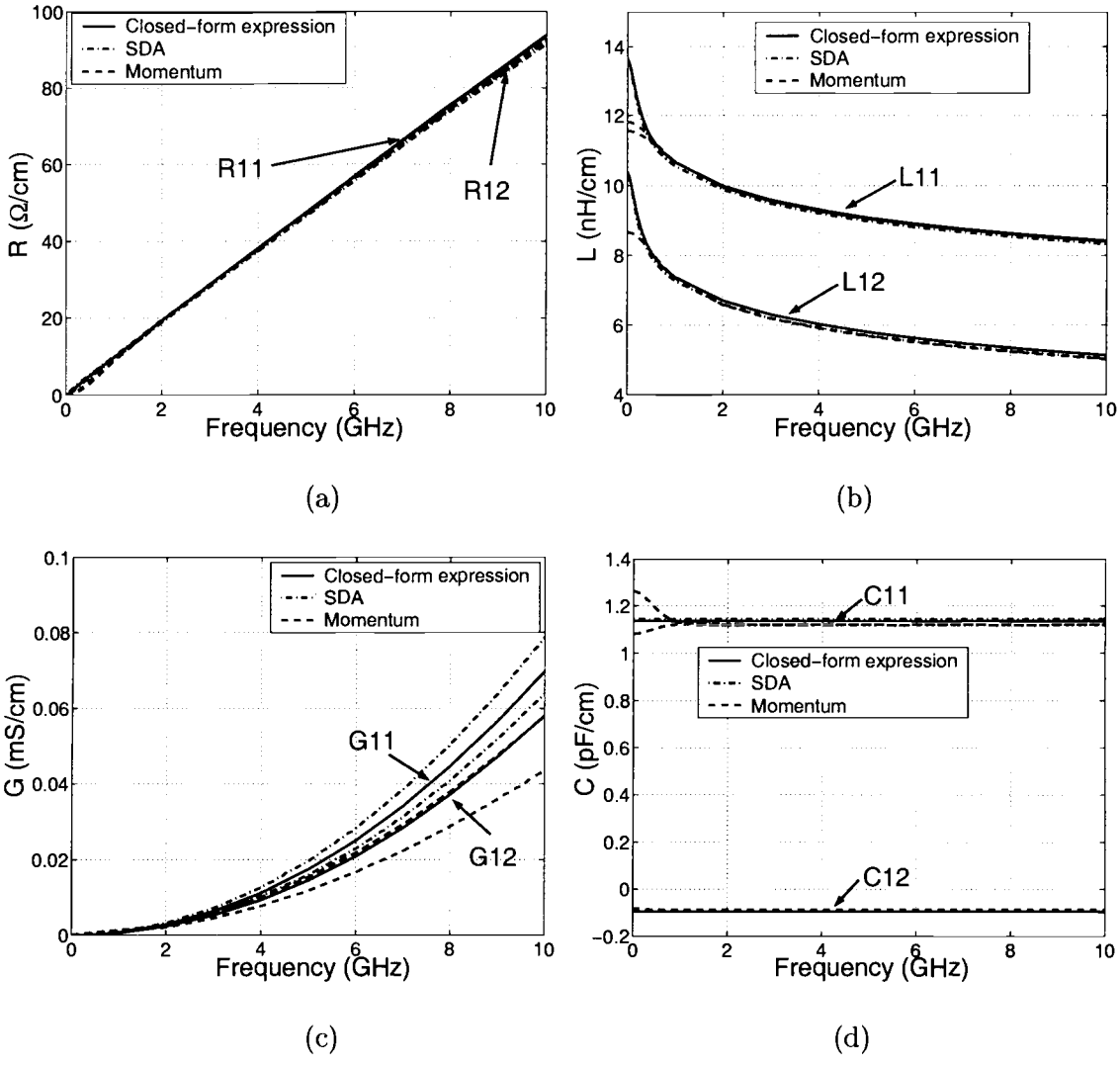


FIGURE 4.5. Frequency-dependent line parameters of a coupled microstrip line on silicon substrate with $w_1 = w_2 = 4\mu m$, $s = 2\mu m$, $h_{ox} = 2\mu m$, $\epsilon_{ox} = 3.9$, $h_{si} = 500\mu m$, $\epsilon_{si} = 11.8$ and $\sigma_{si} = 10,000 S/m$ (a)$[R(\omega)]$, (b)$[L(\omega)]$, (c)$[G(\omega)]$, and (d)$[C(\omega)]$

frequency-dependent line parameters are computed by the closed-form expressions and compared with both the quasi-static EM solutions based on spectral domain approach (SDA) [8] and the more rigorous results generated by the full-wave EM simulator Agilent Momentum [41].

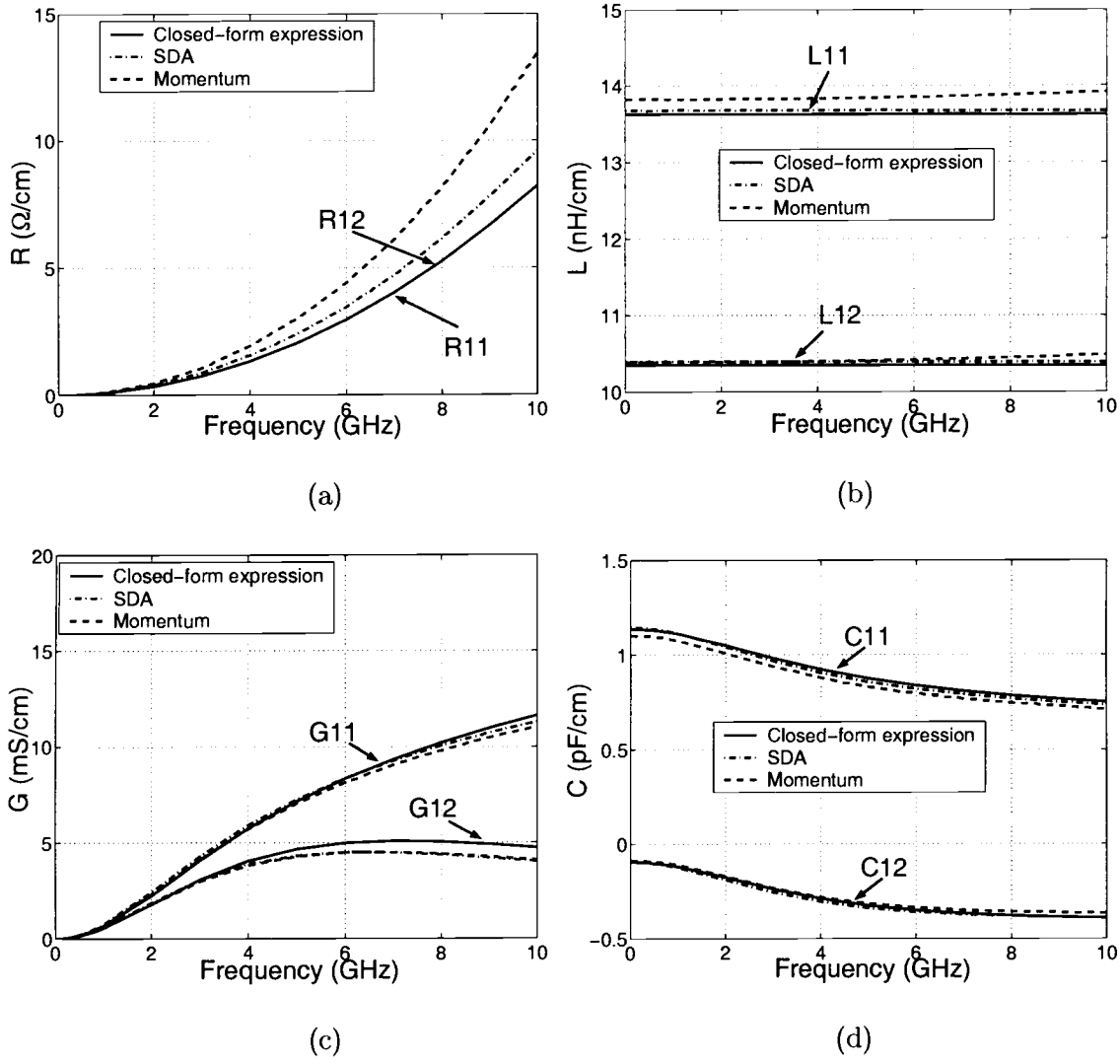


FIGURE 4.6. Frequency-dependent line parameters of a coupled microstrip line on silicon substrate with $w_1 = w_2 = 4\mu m$, $s = 2\mu m$, $h_{ox} = 2\mu m$, $\epsilon_{ox} = 3.9$, $h_{si} = 500\mu m$, $\epsilon_{si} = 11.8$ and $\sigma_{si} = 10S/m$ (a)$[R(\omega)]$, (b)$[L(\omega)]$, (c)$[G(\omega)]$, and (d)$[C(\omega)]$

As a first example, a symmetric coupled microstrip on-chip interconnect on a heavily doped silicon substrate is considered. The width of the two conductor strips is chosen to be $w_1 = w_2 = 4\mu m$ and the spacing between the conductors is $s = 2\mu m$. To emphasize the series resistance due to the skin effect in the silicon

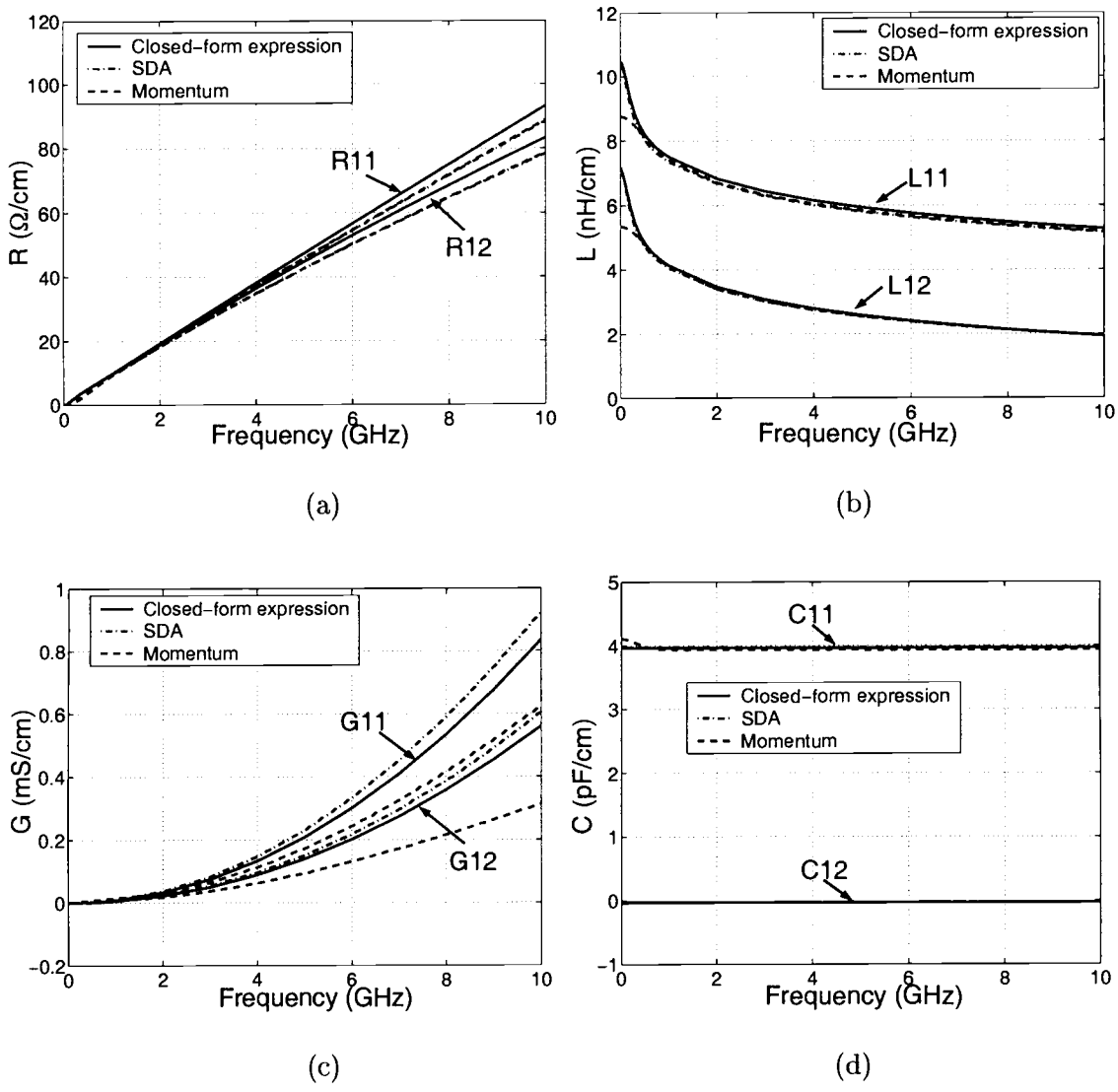


FIGURE 4.7. Frequency-dependent line parameters of a coupled microstrip line on silicon substrate with $w_1 = w_2 = 20\mu m$, $s = 10\mu m$, $h_{ox} = 2\mu m$, $\epsilon_{ox} = 3.9$, $h_{si} = 500\mu m$, $\epsilon_{si} = 11.8$ and $\sigma_{si} = 10,000 S/m$ (a)$[R(\omega)]$, (b)$[L(\omega)]$, (c)$[G(\omega)]$, and (d)$[C(\omega)]$

substrate, the conductors are chosen to have zero thickness and resistivity. The double-layer substrate is chosen to be an oxide layer with thickness $h_{ox} = 2\mu m$ and dielectric constant $\epsilon_{ox} = 3.9$, and a bulk silicon layer with thickness $h_{si} = 500\mu m$,

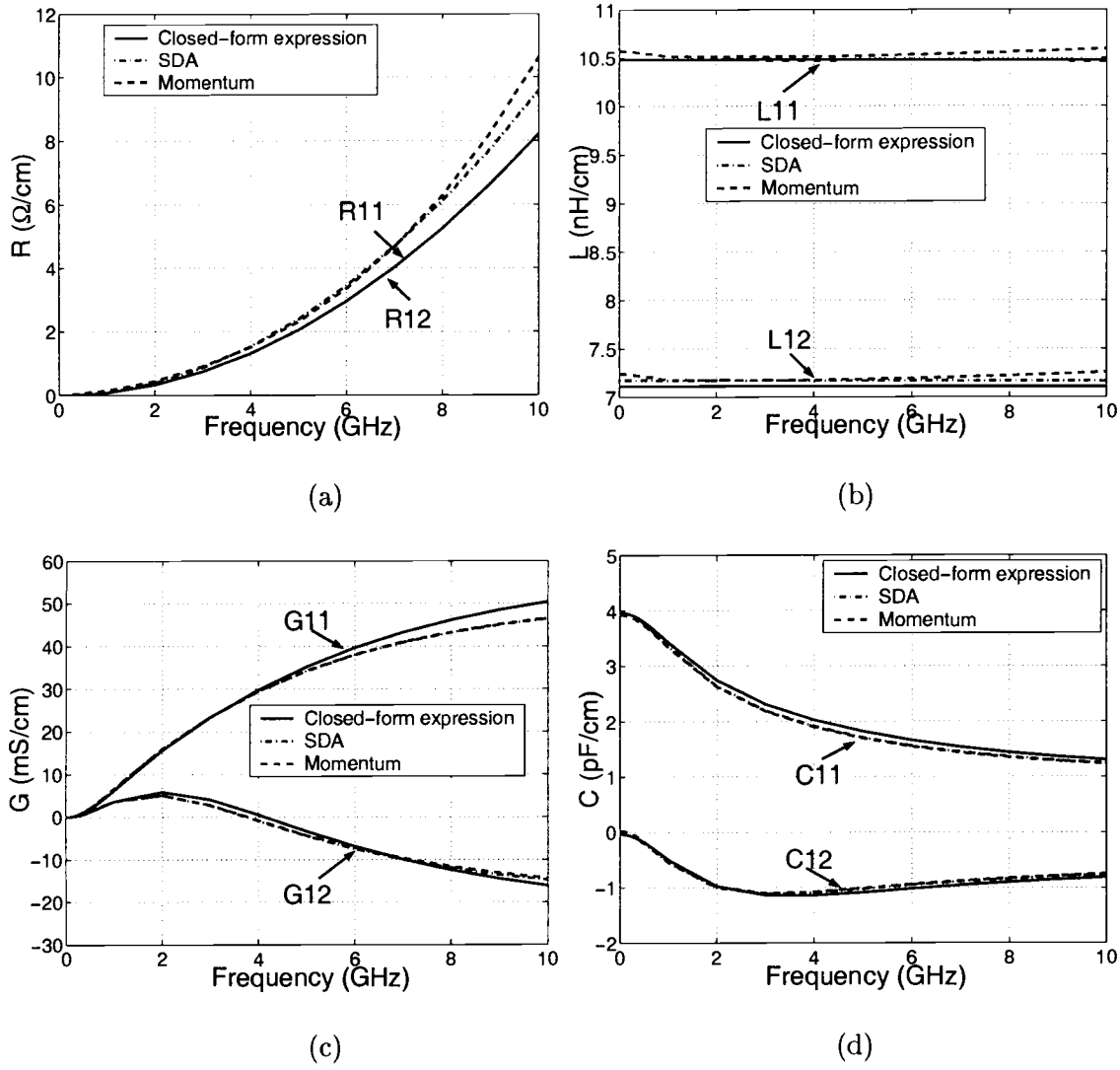


FIGURE 4.8. Frequency-dependent line parameters of a coupled microstrip line on silicon substrate with $w_1 = w_2 = 20\mu m$, $s = 10\mu m$, $h_{ox} = 2\mu m$, $\epsilon_{ox} = 3.9$, $h_{si} = 500\mu m$, $\epsilon_{si} = 11.8$ and $\sigma_{si} = 10S/m$ (a)$[R(\omega)]$, (b)$[L(\omega)]$, (c)$[G(\omega)]$, and (d)$[C(\omega)]$

dielectric constant $\epsilon_{si} = 11.8$, and silicon conductivity $\sigma_{si} = 10,000S/m$. The two-port line parameters of this coupled line are shown in Figure 4.5 as functions of frequency up to 10GHz.

Figures 4.5(a) and (b) show the frequency-dependent series parameters, including both self and mutual parameters. As seen from the comparisons with both SDA and Momentum, the results of p.u.l. $[R(\omega)]$ and $[L(\omega)]$ computed by the proposed closed-form expressions are in very good agreement with the EM solutions. The relative difference between the results of the closed-from solutions and the EM solutions was found to be, in general, less than 3% over a wide frequency range. Moreover, this good agreement exhibits the capability of the proposed image method to adequately capture the frequency dependence in the series impedance.

Figures 4.5(c) and (d) show the frequency-dependent shunt admittance parameters, including both self and mutual parameters. The p.u.l. capacitance matrix $[C(\omega)]$ computed by the proposed method agrees fairly well with that generated by SDA or Momentum EM solutions, as illustrated in Figure 4.5(d). Moreover, $[C(\omega)]$ is found to be nearly a constant over the entire simulation frequency range. This behavior is expected because for a highly doped substrate like this case of $\sigma_{si} = 10,000 S/m$, $[C(\omega)]$ is virtually solely determined by the oxide capacitance only and thus remains nearly constant. The comparison in $[G(\omega)]$, as shown in Figure 4.5(c), can be described as very reasonable, although not as excellent as in $[C(\omega)]$. It is also of interest to note that there is a noticeable difference even between the quasi-static and full-wave EM analysis. However, the difference is acceptable because for highly doped silicon bulk like this case, $[G(\omega)]$ itself is small and thus is believed to be unimportant in determining the overall frequency-dependent characteristics.

Figure 4.6 shows the frequency-dependent series impedance and shunt admittance parameters, including both self and mutual terms, for the same coupled interconnect configuration as mentioned above, except that the silicon substrate is changed into being lightly doped with $\sigma_{si} = 10 S/m$. It is observed again that, in

general, the line parameters computed by the proposed method are in good agreement with those determined by SDA and Momentum. For lightly doped substrates like this case, where $\sigma_{si} = 10S/m$, $[G(\omega)]$ and $[C(\omega)]$ show significant frequency dependence while $[R(\omega)]$ (due to silicon loss only) is small and $[L(\omega)]$ remains nearly constant over the entire interested frequency range. Again, the comparison shown in Figure 4.6 can further demonstrate the capability of the proposed low- and high-frequency asymptotic approach to capture the frequency dependence in the p.u.l. shunt admittance parameters.

Two more examples are next examined, where wider conductor strips are used on the same oxide and silicon substrate structure. Figure 4.7 shows the simulation results for a coupled line structure with $w_1 = w_2 = 20\mu m$ and $s = 10\mu m$ on a heavily doped silicon substrate with $\sigma_{si} = 10,000S/m$. Figure 4.8 shows the results for the same configuration except for a lightly doped substrate with $\sigma_{si} = 10S/m$. Due to the increased width of conductor as well as spacing in between them, some expectable changes can be found in these results, for example, the decrease in inductance and increase in capacitance. Once again, the results obtained with the proposed method agree very well with those by SDA and Momentum.

4.5. Interconnects with Finite Thickness

In the previous sections, the conductors are assumed to be ideal, i.e., with zero thickness and infinite conductivity, in both single and coupled interconnects. The major purpose of this assumption is to focus on the study of the complicated silicon substrate loss contribution to the line parameters. However, all interconnects in reality have finite thickness and finite conductivity. When the thickness-to-width ratio becomes big, which is especially widely used in VLSI circuits, the effects of

finite thickness as well as finite conductivity have to be considered to accurately model the line parameters.

In general, a thick conductor with finite conductivity itself leads to conductor loss including conductor skin effect, proximity effect, and apparently, DC resistance loss. However, DC resistance is not the focus here since it can be readily evaluated. In fact, some manufacturers are using high-conductivity material such as copper to reduce such loss. At low frequencies (towards the DC end), the current is nearly uniformly distributed over the cross section of each conductor. As frequency increases, the current distribution is no longer uniform due to the induced electric field. The current tends to concentrate more at the sharp edges of a conductor. This effect is more pronounced in the signal conductor than in the ground plane. The interaction of induced fields between neighboring conductors also affects the current distribution, i.e., proximity effects. Actually the proximity effects may be even more pronounced in the ground plane since the current in the ground plane tends to concentrate more at the area below the signal conductor. As frequency gets to high enough, the conductor skin effect becomes pronounced because the current becomes concentrated in a thin layer under the conductor surface, which is on the order of the skin depth δ. All these effects make the p.u.l. resistance larger. As an adequately accurate approximation, frequency dependent p.u.l. $R(\omega)$ can be expressed in terms of three additive terms

$$R(\omega) \approx R_{dc} + R_{con}(\omega) + R_{sub}(\omega) \tag{4.29}$$

where R_{dc} is DC resistance, $R_{sub}(\omega)$ is the resistance due to silicon substrate loss only and $R_{con}(\omega)$ is the resistance due to conductor skin effect and proximity effect. R_{dc} can be readily calculated. $R_{sub}(\omega)$ can be calculated by closed-form expressions proposed in previous sections. $R_{con}(\omega)$ has been extensively studied over years and

various numerical and analytical solutions are available, .e.g., by [10], [33], and [34]. The formulas in [10] are given by

$$R_{con} = \frac{R_m}{w} \cdot k \left[\frac{1}{\pi} + \frac{1}{\pi^2} \ln \left(\frac{4\pi w}{t} \right) \right] \tag{4.30}$$

where R_m is given by $(\omega\mu/\sigma)^{1/2}$. The coefficient k is given by

$$k = \begin{cases} 1 & w/h \leq 0.5 \\ 0.94 + 0.132(w/h) - 0.0062(w/h)^2 & 0.5 < w/h \leq 10 \end{cases} \tag{4.31}$$

Meanwhile, the change in current distribution also modifies the magnetic field distribution in the space between conductors as well as with conductors. As a result, both external inductance and internal inductance get reduced. If finite thickness needs to be considered, we may refer to those well developed closed-form expressions for evaluating characteristic impedance of transmission line with finite thickness. A common strategy of taking finite thickness into account is to substitute the actual strip with by an effective strip width. Such formulas can be found in many places in the literature, such as [30], [10], [34], and [35], etc. As an example, an expression for strip thickness correction for homogeneous media is given by [30]

$$w_e = w + \frac{t}{\pi} \ln \left(1 + \frac{4exp(1)}{t \coth^2 \sqrt{6.517(w/h)}} \right) \tag{4.32}$$

A similar strategy is used for static capacitance calculation. The effect of finite strip thickness is taken into account by using the concept of effective width, as enunciated by Wheeler. Such formulas can be readily obtained in many literatures, e.g., [10], [33], etc.

In treating interconnects with finite thickness, in addition to the above closed-form formulas, more rigorous analytical EM approaches can also be applied to obtain more accurate results. Many studies have been done in dealing with conductor loss by various full-wave or quasi-static techniques [36], [37]. Kollipara and Tripathi [38] introduced a modeling technique using a stacked conductor model, which was

later implemented with a great reduction in computation size [8] to accurately and efficiently evaluate the finite thickness effect in C and L.

In conclusion, the finite thickness effects to p.u.l. line parameters can be separately evaluated, in most cases, in terms of the modified closed-form expressions and can be added to the contributions resulting from silicon substrate skin effect. Therefore, complete solutions for calculating p.u.l. frequency-dependent line parameters of practical microstrip-type on-chip interconnects are available now.

4.6. Conclusion

As a conclusion, accurate and complete closed-form expressions for frequency-dependent line parameters can be nicely formulated in terms of corresponding lossless configurations for which closed-form solutions are widely available. The series impedance parameters are obtained using an image method and the shunt admittance parameters are obtained using low- and high-frequency asymptotic solutions. The results by this method have been examined by various coupled microstrip on-chip interconnects cases in comparison with quasi-static SDA [8] and full-wave field solver Momentum [41]. It was shown in this chapter that the results computed by the proposed method are in good agreement with those by EM analysis.

5. APPLICATION TO ON-CHIP INTERCONNECTS SIMULATION AND MODEL EXTRACTION

5.1. CAD-Oriented Modeling of On-Chip Interconnects on Silicon Substrate

Once the distributed line parameters are obtained, on-chip interconnects can be simulated to facilitate circuit level design and/or synthesis of silicon based integrated circuits. Due to the frequency-dependent nature of line parameters, direct implementation of the distributed model in general purpose circuit simulators such as SPICE is difficult and even impossible. Different techniques have been applied to perform the simulation of transmission line effects of interconnects, for example, a method based on moment matching [48] and an inverse Laplace transform approach [49]. However, not all of these methods are fully compatible with circuit level simulators. Therefore, it is advantageous to represent the broadband characteristics of interconnects by modeling the frequency-dependent distributed line parameters in terms of ideal lumped equivalent circuit elements. A comprehensive CAD-oriented modeling methodology for single and coupled on-chip interconnects has been developed in [12]. An overview of this CAD-oriented modeling approach is given in this section since in the next section it will be applied to implement the fast extractor for on-chip interconnects.

Figure 5.1 shows the equivalent circuit with only ideal lumped elements for a single on-chip interconnect on silicon substrate. It should be noted that this model is for a basic interconnect cell. For longer interconnects the basic cells can be readily cascaded. In the following, the circuit elements extraction procedure is described separately for the series impedance part and the shunt admittance part.

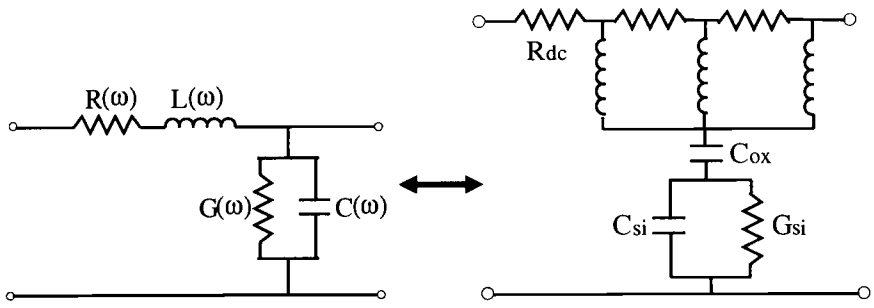


FIGURE 5.1. Distributed frequency-dependent circuit and an equivalent circuit with only ideal lumped elements for a single on-chip interconnect on silicon substrate [12]

As stated previously, the equivalent circuit model for the p.u.l. shunt admittance is proposed based on the physical understanding of the oxide-silicon substrate. The capacitance C_{ox} represents the oxide layer and it is in series with the parallel connection of capacitance C_{si} and conductance G_{si} representing the semiconducting silicon bulk. In [12], these three circuit elements are extracted from the frequency-dependent shunt admittance $G(\omega) + j\omega C(\omega)$ at one frequency point with help of the additional relationship $G_{si}/C_{si} = \sigma_{si}/\epsilon_{si}$. However, this extraction procedure may not be necessary if using the new closed-form expressions. Instead of extracting circuit elements from the $G(\omega) + j\omega C(\omega)$ obtained from quasi-static SDA [12], the new approach directly calculates the circuit elements C_{ox}, C_{si} and G_{si}. As a result, when one uses new closed-form expressions to obtain the frequency-dependent shunt admittance parameters, the equivalent circuit model becomes automatically available without any further extraction procedure.

The equivalent circuit model for the series impedance parameters shown in Figure 5.1 is derived by constructing a rational polynomial approximation of the general form

$$F(j\omega) = \frac{A_0 + A_1(j\omega) + A_2(j\omega)^2 + \cdots + A_m(j\omega)^m}{1 + B_1(j\omega) + B_2(j\omega)^2 + \cdots + B_n(j\omega)^n} \tag{5.1}$$

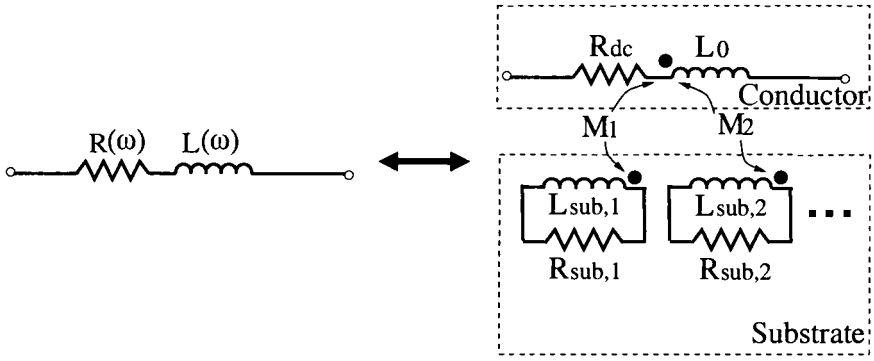


FIGURE 5.2. An alternative equivalent circuit model for series impedance based on effective substrate current loops [12]

The rational polynomial function is synthesized in terms of ideal R and L elements in a ladder-type canonical topology as shown in Figure 5.1. In [12] the authors presented an alternative equivalent circuit for the p.u.l. series impedance providing more physical insight. This model is shown in Figure 5.2. In the main branch, L_0 and R_{dc} represent the inductance and resistance at low frequency where the silicon skin effect is negligible. In the substrate, the inductance $L_{sub,i}$ and resistance $R_{sub,i}$ together represent the i-th effective substrate current loop. The mutual inductance M_i represents the inductive coupling between the conductor and semiconducting silicon substrate. According to this circuit topology, the overall series impedance can be written as

$$Z(j\omega) = R_{dc} + j\omega L_0 - \frac{M_1(j\omega)^2}{j\omega L_{sub,1} + R_{sub,1}} - \frac{M_2(j\omega)^2}{j\omega L_{sub,2} + R_{sub,2}} - \cdots \tag{5.2}$$

The lumped circuit elements can be extracted from the rational polynomial function. The order of the rational polynomial is mainly determined by the substrate

conductivity and thickness. It has been shown that for typical medium and heavily doped silicon substrate, up to three effective substrate current loops should be sufficient to model the broadband characteristics of on-chip interconnects.

The CAD-oriented modeling technique for single on-chip interconnects described above can be extended to the equivalent circuit model for coupled on-chip interconnects. Since the modeling methodology is the same as that of single interconnect, it will not be repeated here. The readers are referred to [12] and [15] for detailed discussion.

5.2. Implementation of Fast On-Chip Interconnect Extractor: CELERITY

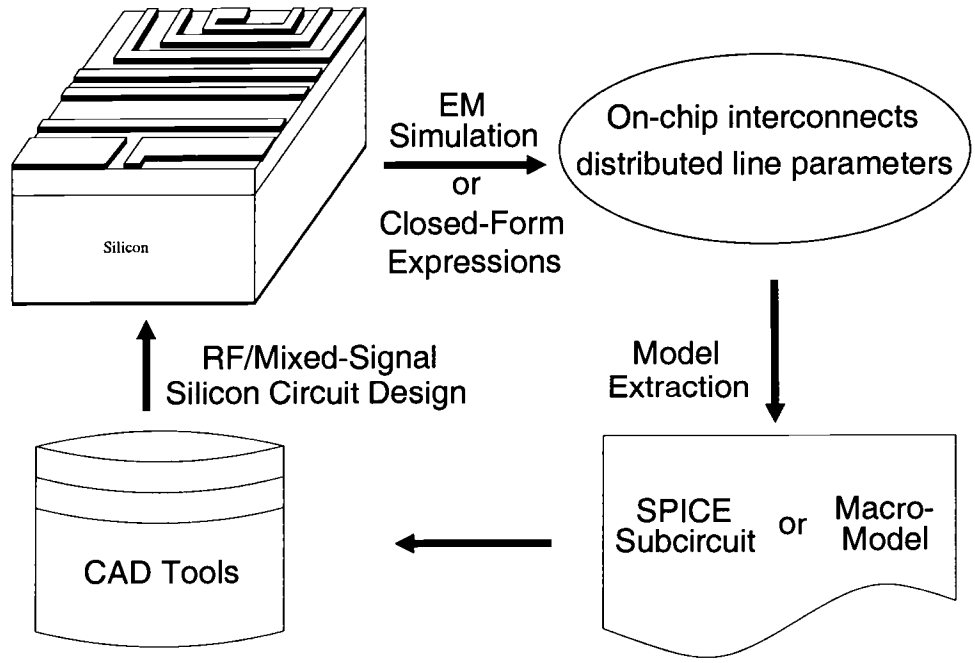


FIGURE 5.3. CAD modeling methodology for On-chip interconnects

A general CAD modeling methodology for on-chip interconnects is illustrated in Figure 5.3. The characteristics of transmission lines on silicon substrate can be obtained by full-wave electromagnetic (EM) analysis and by quasi-static EM approach. Once the interconnect parameters, typically in terms of frequency-dependent distributed line parameters, are obtained by EM simulation, they can be used to extract SPICE compatible subcircuit and/or macro-model. The extracted model can then be directly or indirectly employed in the commercial CAD tools, such as Agilent EEsof ADS [41] and HSPICE [50], to facilitate the silicon-based integrated circuit design and/or synthesis.

However, EM simulations generally are too time-consuming to be a viable solution for practical computer-aided design (CAD). Alternatively, closed-form expressions for the characteristics of on-chip interconnects are very desirable for fast simulation and CAD. This thesis work has focused on one of the most important interconnects configurations, i.e., microstrip-type on-chip interconnects, and as a result complete and fast closed-form expressions for single and coupled microstrip-type on-chip interconnects have been developed and validated.

A fast on-chip interconnect modeling tool was developed and named CELERITY. The software CELERITY inherently performs two functions. The first is to calculate the frequency-dependent line parameters of on-chip interconnects using the closed-form expressions. The second part is to extract equivalent circuit models consisting of ideal lumped circuit elements only, which can be given in form of fully SPICE compatible subcircuit netlists. Figure 5.4 illustrates the flowchart of the implementation of CELERITY. The software tool takes, as inputs, the geometrical parameters, substrate material parameters, and interested frequency range, etc. The current version can deal with microstrip-type single and symmetric coupled on-chip interconnects only. The tool calculates the series impedance and shunt admittance parameters as functions of layout geometrical parameters, process parameters, and

operating frequency. The process of calculating line parameters is based on the proposed closed-form expressions and, thus, the simulation speed is much faster than that of the previously developed tool, OSU-SMILES [51], which is based on quasi-static EM analysis. The calculated RLGC parameters are saved and used for post processing, such as, plotting. Meanwhile, the interconnect parameters are fed to an equivalent circuit extractor to generate the equivalent circuit model, which is compatible with the commonly used SPICE subcircuit format. It is worth noticing that since the most time-consuming part, i.e., the EM simulation, is replaced by our fast closed-form expressions, significant improvement in simulation speed should be expected. The speed-up will be exemplified in the following section by speed comparison between the new tool CELERITY and the previous quasi-static EM based on-chip interconnect extractor, OSU-SMILES.

5.3. Speed Comparison between CELERITY and OSU-SMILES

Two on-chip interconnect extractors are compared here. OSU-SMILES is a quasi-static spectral domain approach (SDA) based on-chip interconnect extractor while CELERITY is a new closed-form-expressions-based extractor. Both of them can perform frequency-dependent line parameters extraction from single or coupled interconnect layouts for a given process, and can extract equivalent circuit models with fixed lumped circuit elements. Two test examples are simulated by CELERITY and OSU-SMILES on three different computer platforms and CPU times in seconds are recorded, as shown in Table 5.1.

Test case 1 is a single line on-chip interconnect with $w = 6\mu m$, $h_{ox} = 2\mu m$, $\epsilon_{ox} = 3.9$, $h_{si} = 500\mu m$, and $\epsilon_{si} = 11.8$, $\sigma_{si} = 10,000 S/m$. Test case 2 is a coupled on-chip interconnect structure with $w_1 = w_2 = 10\mu m$, $s = 4\mu m$, $h_{ox} = 2\mu m$, $\epsilon_{ox} =$

3.9, $h_{si} = 500\mu m$, $\epsilon_{si} = 11.8$ and $\sigma_{si} = 10,000 S/m$. Both cases are simulated from 0-20GHz with 25 frequency points on an AMD-K6 2/235 PC with 64M RAM, a SUN Ultra10/440 workstation with 256M RAM, and an HP Visualize C3600 workstation with 128M RAM. All simulations performed include both RLGC line parameters extraction and equivalent circuit model extraction. Table 5.1 shows the simulation times for the two test cases on the three different computer platforms.

CPU times of CELERITY v.s. OSU-SMILES (in seconds)

Platform	PC	SUN	HP
Case1	0.28/41.58	0.08/21.36	0.06/10.56
Case2	2.75/137.7	1.43/72.89	0.67/35.2

TABLE 5.1. CPU times (in seconds) of CELERITY/OSU-SMILES. Case 1: single line (25 frequency points, 0-20 GHz). Case 2: coupled line (25 frequency points, 0-20 GHz). The three computer platforms are: PC AMD-K6 2/235 64M RAM, SUN Ultra10/440 workstation 256M RAM, and HP Visualize C3600 workstation 128M RAM

As shown in Table 5.1, CELERITY significantly reduces the CPU time in performing the same simulation task. In case 1, where a single line structure is analyzed, CELERITY is faster than OSU-SMILES approximately by a factor of 148 on the PC, 267 on the SUN workstation, and 176 on the HP workstation. In case 2, where a coupled line structure is analyzed, CELERITY is faster than OSU-SMILES approximately by a factor of 36 on the PC, 51 on the SUN workstation, and 52 on the HP workstation. In general, CELERITY runs tens to several hundred times faster than OSU-SMILES. In conclusion, it is observed that approximately 0.5-3% of the computation time is achieved in CELERITY compared with the quasi-

static SDA-based OSU-SMILES. This result not only verifies that the most time-consuming part is the EM simulation in on-chip interconnects modeling but also demonstrates the high efficiency of the proposed closed-form expressions. As an additional comment, since OSU-SMILES is a quasi-static SDA based extraction tool, it already has significantly improved the simulation speed compared to that of full-wave EM analysis.

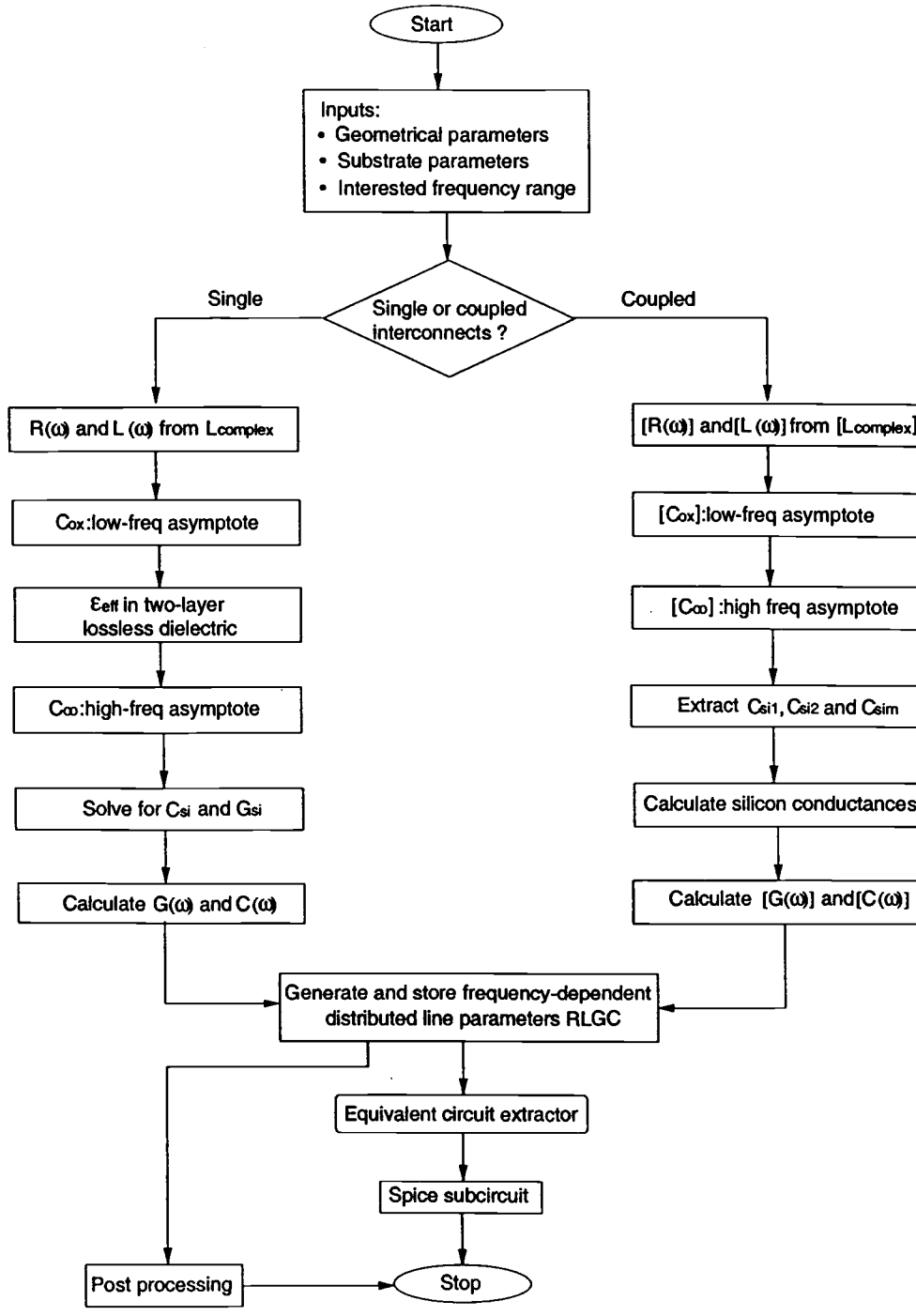


FIGURE 5.4. Flowchart of CELERITY

6. CONCLUSION AND FURTHER RESEARCH

6.1. Conclusion

This thesis has presented a new, fast extraction technique for the line parameters of microstrip-type on-chip interconnects on silicon substrate. After a review of the basic theory and previous research on conventional and MIS microstrip line in chapter 2, the motivation of obtaining accurate closed-form expressions for the frequency-dependent line parameters of on-chip interconnects on lossy silicon substrate was highlighted. A complex image theory was employed and extended to the MIS structure. The resulting effective complex height was used to approximate the complicated silicon substrate loss effects. With the aid of effective complex height, appropriate static inductance formulas were then used to calculate complex inductances, from which the p.u.l. series impedance line parameters were extracted. Based on the equivalent circuit model, p.u.l. shunt admittance parameters expressions were developed using low- and high-frequency asymptotic static solutions. Chapter 4 followed with coupled line on-chip interconnects on silicon substrate. The image method was extended to the coupled line configuration and partial self and mutual inductance formulas were applied to calculate p.u.l. series impedance matrices. P.u.l. shunt admittance matrices were determined by low- and high-frequency asymptotic solutions. This thesis showed that the complete solution of the frequency-dependent characteristics of on-chip interconnects can be formulated in terms of corresponding lossless/static configurations for which closed-from solutions are readily available. The accuracy of the presented extraction technique for the line parameters was illustrated by extensive comparison with corresponding full-wave and quasi-static EM simulations for both single and coupled microstrip

on-chip interconnects. It was shown the that the proposed closed-form expressions are in good agreement with the EM solutions.

The technique presented in this thesis is applicable to CAD modeling of on-chip interconnects. In chapter 5, a fast on-chip interconnect extractor tool, CELERITY, was developed based on the proposed closed-form expressions for the frequency-dependent p.u.l. line parameters. By comparison with a previous quasi-static-EM-based on-chip interconnect modeling tool, CELERITY was shown to be able to improve the simulation speed significantly by an order of ten to several hundred.

6.2. Further Research

Further work in developing fast closed-form expressions of on-chip interconnects should include, but is not limited to, interconnects without ground plane, e.g., coplanar transmission line. A modified or new complex image solution as well as asymptotic static solution should be derived to handle interconnect configurations where no ground plane exists. Moreover, for multilevel interconnects, where conducting strips may lie in different levels in parallel or are crossing, the methodology presented in this work is not directly applicable. However, it may lend itself well to being extended to such cases.

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APPENDICES

APPENDIX A. Formulas for the Characteristics of Microstrip Line

The microstrip line is conventionally characterized by the characteristic impedance Z_c and the effective dielectric constant $\epsilon_{r,eff}$. Exact compact equations for Z_c and $\epsilon_{r,eff}$ are difficult to obtain due to the inhomogeneous dielectric. However, approximate formulas have been developed by various methods, such as the method of modified conformal images and the functional approximation of numerical results. These types of formulas give acceptable accuracy, which is more than sufficient in practice.

In the following, the single microstrip line is assumed to have conductor width w, lossless dielectric substrate thickness h, and dielectric constant ϵ_r. The conductor thickness is assumed to be zero unless otherwise specified.

An equation obtained by the method of modified conformal images by Wheeler [26] is given as

$$Z_c = \frac{120}{\sqrt{2(\epsilon_r+1)}}\left\{\ln\left[\frac{4h}{w}+\sqrt{16\left(\frac{h}{w}\right)^2+2}\right]-\frac{\epsilon_r-1}{2(\epsilon_r+1)}\left[\ln\left(\frac{\pi}{2}\right)+\frac{\ln(4/\pi)}{\epsilon_r}\right]\right\} \tag{A1}$$

for narrow conductors with $w/h \leq 3.3$. For wide conductors with $w/h \geq 3.3$,

$$Z_c = \frac{60\pi}{\sqrt{\epsilon_r}}\left\{\frac{w}{2h}+\frac{\ln 4}{\pi}+\frac{\epsilon_r+1}{2\pi\epsilon_r}\left[\ln\left(\frac{\pi e}{2}\right)+\ln\left(\frac{w}{2h}+0.94\right)\right]+\frac{(\epsilon_r-1)\ln(e\pi^2/16)}{2\pi\epsilon_r^2}\right\}^{-1} \tag{A2}$$

An improved Wheeler's equation, for $0 < w/h < \infty$ and $1 \leq \epsilon_r < \infty$, is given as

$$Z_c = \frac{42.4}{\sqrt{\epsilon_r+1}}\ln\left\{1+\frac{4h}{w}\left[\left(\frac{14+8/\epsilon_r}{11}\right)\frac{4h}{w}+\sqrt{\left(\frac{14+8/\epsilon_r}{11}\right)^2\left(\frac{4h}{w}\right)^2+\frac{\pi^2}{2}\left(1+\frac{1}{\epsilon_r}\right)}\right]\right\} \tag{A3}$$

Hammerstad presented equations in [30] by functional approximation of the exact conformal image value. The equations are

$$Z_c^{air} = \frac{\eta_0}{2\pi\sqrt{\epsilon_{r,eff}}} \ln\left[\frac{F_1 \cdot h}{w} + \sqrt{1 + (2h/w)^2}\right] \tag{A4}$$

with

$$F_1 = 6 + (2\pi - 6)exp\{-(30.666h/w)^{0.7528}\} \tag{A5}$$

where η_0 is the wave impedance in free space and $\epsilon_{r,eff}$ is the effective permittivity, which can be derived by functional approximation of the numerically calculated values from the static Green's function method and is given as

$$\epsilon_{r,eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2}\left(1 + \frac{10h}{w}\right) - a \cdot b \tag{A6}$$

with

$$a = 1 + \frac{1}{49}\ln\left\{\frac{(w/h)^4 + [w/(52h)]^2}{(w/h)^4 + 0.432}\right\} + \frac{1}{18.7}\ln\left[1 + \left(\frac{w}{18.1h}\right)^3\right] \tag{A7}$$

and

$$b = 0.564\left(\frac{\epsilon_r - 0.9}{\epsilon_r + 3}\right)^{0.053} \tag{A8}$$

For a microstrip line without substrate (air-filled), Schneider gave functional-approximation-based equations for the characteristic impedance. For $0 < w/h \leq 1$,

$$Z_c^{air} = 60\ln\left(\frac{8h}{w} + \frac{w}{4h}\right) \tag{A9}$$

and for $w/h \geq 1$,

$$Z_c^{air} = \frac{120\pi}{(w/h) + 2.42 - (0.44h/w) + [1 - (h/w)]^6} \tag{A10}$$

In [26], Wheeler also gave an equation for the characteristic impedance of a microstrip without substrate (that is, $\epsilon_r = 1$), which is also a functional approximation of exact solutions obtained by means of the method of conformal images. The equation for the entire range $0 < w/h < \infty$ with an error of less than 1% is given as

$$Z_c^{air} = 30 \ln \left\{ 1 + 32 \left(\frac{h}{w} \right)^2 \left[1 + \sqrt{1 + \left(\frac{\pi}{8} \frac{w}{h} \right)^2} \right] \right\} \tag{A11}$$

The formulas above have been compared with accurate values determined by the static variant of the method of lines [32]. The comparisons show that Z_c calculated by equations from Wheeler's modified conformal images differs by a maximum of 0.4%, when calculated by the equations from Schneider's functional approximation differs by a maximum of 1.5%, when calculated by the functional approximation from Wheeler's differs by a maximum of 0.9%, when calculated by Hammerstad's equations differs by a maximum of 0.2%, and when calculated by Wheeler's formula for microstrip without substrate differs by a maximum of 1%. Therefore, these equations seem to be accurate enough to calculate the characteristic impedance as well as static inductance and/or static capacitance.

APPENDIX B. Overview of Partial Inductance

For any two conductors of uniform cross sections a_i and a_j, around loops i and j, the mutual inductance between loops i and j is formulated as

$$L_{ij} = \frac{1}{a_i a_j} \frac{\mu}{4\pi} \oint_i \int_{a_i} \oint_j \int_{a_j} \frac{d\mathbf{l}_i \cdot d\mathbf{l}_j}{r_{ij}} da_i da_j \tag{B1}$$

where $r_{ij} = |\mathbf{r}_i - \mathbf{r}_j|$ and $d\mathbf{l}_i$ is the element length taken along the axis direction of the conductor. This formula shows that the mutual inductance is fully dependent on the geometrical property of the conductor loops. It is seen that averages are taken over the conductor cross sections for both conductors. Actually this formula reduces to the well-known Neumann formula when both conductors are infinitely thin, i.e., filaments, and is given by

$$L_{f_{ij}} = \frac{\mu}{4\pi} \oint_i \oint_j \frac{d\mathbf{l}_i \cdot d\mathbf{l}_j}{r_{ij}} \tag{B2}$$

The above definitions of inductances are suitable for a set of loops since the flux linkage induced in a closed loop where the area is bounded by the loop is clearly defined. However, it seems that no unique flux is associated with an open loop or a segment of loop. Nevertheless, the concept of partial inductance can be introduced to deal with this type of inductance calculation. A partial inductance is defined as

$$L_{p_{mk}} = \frac{1}{a_k a_m} \frac{\mu}{4\pi} \int_{a_k} \int_{a_m} \int_{b_k}^{c_k} \int_{b_m}^{c_m} \frac{d\mathbf{l}_k \cdot d\mathbf{l}_m}{r_{km}} da_k da_m \tag{B3}$$

where b_k, b_m are the starting points and c_k and c_m are the ending points on the segments considered. (B3) can also be seen as the result of replacing all loop integrals in (B1) by line integrals.

Based on the definition of partial inductance, exact inductance solutions may be obtained in terms of numerical integrals or summations, such as in [45] and [46]. For fast computation purpose, various formulas have been developed dealing with different geometries, e.g., in [45].

Grover [44] provides a more extensive treatment of inductance calculation and supplies a thorough list of references. Grover's formulas are used in this thesis work to calculate both self and mutual inductances. Grover's formulas are essentially the results of deriving inductance expressions based on geometric mean distance (g.m.d.) calculations. In most cases, only partial inductances, i.e., with finite length, are calculated using the working formulas and thus are length dependent. The p.u.l. self and mutual inductances, which are of our interest, can be obtained by extrapolating the corresponding partial inductance value $L(l)$ for finite length conductors, as given by

$$L_{p.u.l} = \lim_{l \to \infty} \frac{L(l)}{l} \tag{B4}$$

In the presence of a ground plane, e.g., for microtrip-type on-chip interconnects, the p.u.l. self and mutual inductance can be efficiently obtained from the closed-form expressions in [44] with the aid of image conductors. The calculation is convergent when the length l is large enough. Numerical results [15] show a length of 10^4 times the cross sectional dimensions will be sufficient to assure the convergence.

APPENDIX C. Brief Overview of the Quasi-Static Spectral Domain Approach

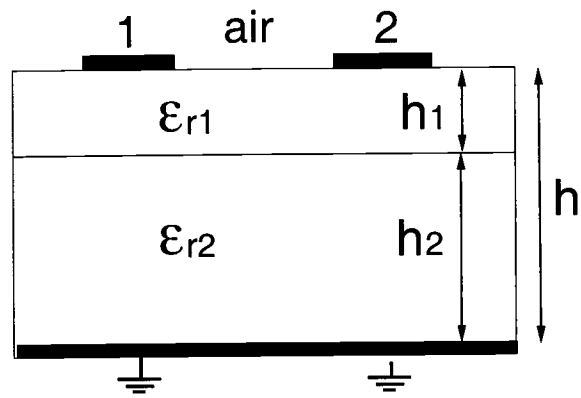

FIGURE C.1. Single level coupled microstrip line with a two-layer dielectric substrate

Figure C.1 illustrates a single level, coupled microstrip line with a two-layer lossless dielectric substrate. Under the quasi-TEM assumption, the problem of coupled lines with a two-layer lossless substrate can be formulated as a 2D Poisson's equation

$$\nabla_t^2 \Phi_i(x,y) = -\frac{\rho(x)}{\epsilon_i}\delta(y-h) \tag{C1}$$

In the transformed (spectral) domain, Poisson's equation becomes

$$\frac{d^2}{dy^2}\tilde{\Phi}(\alpha,y) = \alpha^2\tilde{\Phi}(\alpha,y) \tag{C2}$$

This equation together with appropriate boundary conditions can be manipulated and results in the corresponding algebraic form in the spectral domain given by

$$\tilde{\Phi}(\alpha, y = h_1 + h_2) = \sum_{m=1}^{2} \tilde{g}(\alpha)\tilde{\rho}_m(\alpha) \tag{C3}$$

where $\tilde{\rho}_m$ is the spectral domain representation of charge density $\rho_s(x)$ on the m-th conductor, and $\tilde{g}(\alpha)$ is boundary Green's function in the spectral domain. For the two-layer case shown in Figure C.1, $\tilde{g}(\alpha)$ is determined as [8]

$$\tilde{g}(\alpha, y = h_1 + h_2) = \frac{\epsilon_{r1}\coth(|\alpha|h_1) + \epsilon_{r2}\coth(|\alpha|h_2)}{|\alpha|\epsilon_0\{\epsilon_{r1}[\epsilon_{r1} + \coth(|\alpha|h_1)] + \epsilon_{r2}\coth(|\alpha|h_2)[1 + \epsilon_{r1}\coth(|\alpha|h_1)]\}} \tag{C4}$$

The unknown charge density $\rho_m(x)$ is expanded in terms of Chebyshev basis functions as

$$\rho_m(x) = \sum_{n=0}^{N} C_{nm} \frac{T_n(\frac{2(x-x_m)}{w_m})}{\sqrt{1 - (\frac{2(x-x_m)}{w_m})^2}} \tag{C5}$$

where T_n stands for Chebyshev polynomial. Correspondingly, in the spectral domain, $\tilde{\rho}_s(\alpha)$ is expanded in terms of the first kind Bessel functions,

$$\tilde{\rho}_m(\alpha) = \sum_{n=0}^{N} C_{nm}\pi\frac{w}{2}(-1)^n J_n(\frac{|\alpha|w_m}{2})e^{-j\alpha x_m} \tag{C6}$$

where J_n is the n-th order Bessel function of the first kind. A set of algebraic equations can be obtained by taking inner product of basis functions and test function. As a result, the coefficients of the basis function for the unknown charge density are obtained and, thus, the capacitance matrix can be readily calculated.