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Title:

Development, Fabrication, and Characterization of Transparent Electronic Devices.

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John F. Wager

The objective of this thesis is to provide an initial demonstration of the feasibility of constructing highly transparent active electronic devices. Such a demonstration is successfully achieved in the fabrication of ZnO-based thin film transistors (TFTs) exhibiting transparency greater than ~90% in the visible portion of the electromagnetic spectrum and prototypical n-channel, enhancement mode TFT characteristics. Electrical characterization studies of these ZnO-based transparent TFTs and of $CuYO_2$ / ZnO / ITO p-i-n heterojunction diodes serve to elucidate the mechanisms responsible for the behavior of these devices in particular, and of transparent electronic devices in general. Energy band analysis of the degenerate semiconductor / insulator heterojunction yields insight into the phenomenon of charge injection into an insulator, with important implications for the analysis of devices containing heterojunctions of this nature. Finally, a novel technique for simultaneously characterizing carrier injection into an insulator and interface channel formation, the capacitance-(voltage, frequency) [C-(V,f)] technique, is proposed and employed in the characterization of ZnO-based TFT structures.

Development, Fabrication, and Characterization of Transparent Electronic Devices

by

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Randy L. Hoffman, Author

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DEVELOPMENT, FABRICATION, AND CHARACTERIZATION OF TRANSPARENT ELECTRONIC DEVICES

1. INTRODUCTION

The existence of materials simultaneously exhibiting optical transparency and electrical conductivity has been known for many years; the first report of such a material (CdO) appears to have been made by Badeker in 1907 [1]. A number of additional transparent conducting oxides (TCOs), such as ZnO, In_2O_3, and SnO_2, have been known to exist for many years. However, the use of transparent conductors has been limited to passive applications. This is a consequence of the fact that, until quite recently, the only known transparent conductors were n-type. The recent discovery of a number of p-type transparent conductors, however, has opened the door to the development of active electronic devices based entirely upon transparent materials.

Since the field of transparent electronics is in an early stage of development, an understanding of the electrical behavior of transparent conductors must be developed prior to their integration into active electronic devices. Such an understanding is essential, as transparent conductors exhibit a number of properties that are quite different than those considered optimal within the framework of conventional electronics. Preconceived notions based upon established device theory are, in general, more harmful than beneficial; an unbiased methodology must be employed both in developing novel transparent electronic devices and in understanding their electrical characteristics.

The goal of this thesis is the fabrication and characterization of transparent active electronic devices; both experimental and theoretical achievements are presented herein. Although recent research devoted to novel p-type transparent conductors has been accompanied by several reports of transparent diodes, electrical characterization

of these devices has been essentially nonexistent; this thesis contains the first detailed electrical characterization study of a transparent diode, a $CuYO_2$ / ZnO / ITO p-i-n heterojunction. Perhaps the most significant achievement contained herein is the fabrication and characterization of highly transparent ZnO-based thin film transistors (TFTs), with an average transparency above ~90% in the visible portion of the electromagnetic spectrum; this is, in fact, the first report of a highly transparent transistor. A novel characterization technique, the capacitance-(voltage, frequency) [C-(V,f)] method, is proposed and employed in the characterization of charge injection and interface channel formation for ZnO-based TFT structures. The energy band structure of the degenerately doped semiconductor / insulator heterojunction is examined, yielding insight into the mechanism underlying charge injection into an insulator.

The structure of this thesis is as follows. Chapter 2 contains a review of the pertinent literature and provides the technical background necessary to establish a context within which experimental results can be discussed. Chapter 3 provides a description of important fabrication tools and techniques, followed by a discussion of relevant optical and electrical thin film and device characterization methodology. Chapter 4 presents an electrical characterization study of transparent $CuYO_2$ / ZnO / ITO p-i-n heterojunction diodes. Chapter 5 presents the fabrication and characterization of highly transparent ZnO-based TFTs. Finally, Chapter 6 contains conclusions and recommendations for future work.

2. LITERATURE REVIEW AND TECHNICAL BACKGROUND

This chapter presents a review of the existing literature and fundamental concepts pertaining to the development of transparent electronic devices. A brief introduction to transparent conducting and semiconducting materials is provided. The properties of zinc oxide (ZnO) are explored in some detail, in anticipation of results presented in Chapters 4 and 5. Relevant materials and device issues are examined, including self-compensation, space-charge-limited current, the injection of charge into an insulator, and consequences of the low mobilities typically possessed by transparent semiconductors. The chapter concludes with a review of transparent active electronic devices reported in the literature; characterization and interpretation concerns are noted as they arise throughout this section.

2.1 Transparent conductors

The simultaneous existence of optical transparency and electrical conductivity requires a wide bandgap ($\gtrsim$3 eV) material, doped (intentionally or unintentionally) so as to modulate the Fermi level close enough to the conduction (valence) band to induce mobile electrons (holes). Due to the relatively low mobilities exhibited by this class of materials, typical transparent conductors used in passive applications are degenerately doped in order to maximize their conductivity.

Until recently, all known transparent conductors were n-type. The first report of p-type conductivity in a transparent material ($CuAlO_2$) came in 1997. [2] Since this report, a number of new p-type as well as n-type transparent conducting materials have been discovered. Tables 2.1 and 2.2 list known n- and p-type conductors along with typical values of important thin film electrical and optical properties (optical bandgap, average transmission in the visible region, Hall mobility, conductivity, and carrier concentration) as available. Further details regarding individual material

characteristics relevant to results presented in this thesis are included in the sections where such results are presented.

Note that the division of transparent conducting materials by conductivity type is quite reasonable, in that bipolar conductivity in this class of materials is exceedingly rare. To date only two transparent semiconductors, GaN [3] and $CuInO_2$ [4], have been reported to exhibit bipolar conductivity.

2.2 Zinc oxide

Zinc oxide (ZnO) is a well-known wide bandgap semiconductor. As results reported in this thesis rely strongly upon the use of ZnO films, a fairly detailed discussion of their important properties is given here. ZnO exhibits a set of properties that allow its use in a number of applications. It is one of the common transparent conductor materials. [38] ZnO varistors (polycrystalline ceramic electronic devices with non-linear current-voltage characteristics) are used to limit large voltage transients. [39] ZnO can also function as a phosphor (cathodoluminescent [40], photoluminescent [41, 42], electroluminescent [43]); as a thin film chemical sensor [44]; and as a piezoelectric material. [45] ZnO exhibits a large degree of photoconductivity as well as persistent photoconductivity, as discussed in Section 2.2.2.

ZnO thin films have been deposited using a number of methods, including reactive sputtering (DC [46], RF [46], ion beam [47]), activated reactive evaporation (ARE) [48], spray pyrolysis [49], solgel [50], laser ablation [51], pyrosol [52], metalorganic chemical vapor deposition (MOCVD) [53], and electrochemical reaction. [54] The substrate is often unheated during deposition; as-deposited films are nearly always polycrystalline.

Table 2.1: Thin film electrical and optical properties of n-type transparent conductors. E_G^{opt} denotes optical bandgap, T^{typ} denotes typical optical transmission in the visible region, μ_H^{typ} denotes typical Hall mobility, σ^{typ} denotes typical conductivity, n^{typ} denotes typical carrier concentration.

Material	E_G^{opt} (eV)	T^{typ} (%)	μ_H^{typ} ($cm^2/V\ s$)	σ^{typ} ($\Omega^{-1}\ cm^{-1}$)	n^{typ} (cm^{-3})
$AgInO_2$ [5, 6]	4.1-4.4	80	1	50	10^{20}
CdO [7, 8]	2.2-2.6		1-30	≤ 20	$\leq 10^{20}$
Cd_2SnO_4 [9, 10]	2.9-3.1	80	30-50	$\leq 10^4$	$\leq 10^{21}$
$CdSb_2O_6$ [11]	3.8-4.4	90	2	40	10^{20}
$CuInO_2$ [4]	3.9	50-80		3.8×10^{-3}	
$GaInO_3$ [12]	3.3	90	10	3×10^2	10^{20}
$(Ga,In)_2O_3$ [13]				2×10^3	
GaN [3, 14, 15]	3.4		100	$\leq 10^4$	$\leq 10^{20}$
In_2O_3 [9]	3.55-3.75	80-90	10-50	$\leq 10^4$	$\leq 10^{21}$
$In_4Sn_3O_{12}$ [16]	3.5	80	20	2.5×10^{-3}	10^{21}
$MgIn_2O_4$ [17]	3.4	80	5	10^2	10^{20}
SnO_2 [9]	3.9-4.3	80-90	5-30	$\leq 10^3$	$\leq 10^{20}$
$SrTiO_3$ [18]	3.2	85-95	6.4	0.6	5.8×10^{17}
ZnO [9, 13, 19]	3.2-3.3	80-90	5-50	$\leq 10^4$	$\leq 10^{21}$
$Zn_2In_2O_5$ [20]	2.9	80	12	2.5×10^3	$5x10^{20}$
Zn_2SnO_4 [13]				50	
$ZnSnO_3$ [21]	$\sim$3.5	80	10	10^2	10^{20}

Table 2.2: Thin film electrical and optical properties of p-type transparent conductors. E_G^{opt} denotes optical bandgap, T^{typ} denotes typical optical transmission in the visible region, μ_H^{typ} denotes typical Hall mobility, σ^{typ} denotes typical conductivity, p^{typ} denotes typical carrier concentration.

Material	E_G^{opt} (eV)	T^{typ} (%)	μ_H^{typ} ($cm^2/V\ s$)	σ^{typ} ($\Omega^{-1}\ cm^{-1}$)	p^{typ} (cm^{-3})
$AgCoO_2$ [22]	4.15	40-60		0.2	
$BaCu_2S_2$ [23]	2.3	60-80	3.5	17	10^{19}
$CuAlO_2$ [2, 24]	3.5	70-80	0.13	0.3	3×10^{19}
$CuCrO_2$ [25]	3.1	30		220	
$CuFeO_2$ [26]	3.35				
$CuGaO_2$ [22, 27]	3.6-4.3	70-85	0.23	6×10^{-2}	1.7×10^{18}
$CuGa_{1-x}Fe_xO_2$ [22]	3.4	50-70		1	
$CuInO_2$ [4]	3.9	50-80		2.8×10^{-3}	
$CuNi_{2/3}Sb_{1/3}O_2$ [22]	3.4	60		5×10^{-2}	
$CuScO_2$ [28]	3.3	40		30	
$CuYO_2$ [29]	3.5	40-50		1	
diamond [30, 31, 32]	5.5		10	1-10	10^{17}
GaN [3, 15]	3.4		5	≤ 10	$\leq 10^{18}$
LaCuOS [33]	3.1	70		0.26	
NiO [34, 35]	3.6-4	40-80	1	≤ 10	$\leq 10^{19}$
$SrCu_2O_2$ [36]	3.3	70-80	0.46	4.8×10^{-2}	6×10^{17}
$Sr_2Cu_2ZnO_2S_2$ [37]	2.7				

2.2.1 Electrical properties

The work function (difference between the vacuum level and the Fermi level) of ZnO, from UV photoelectron spectroscopy measurements, varies from 5.3 eV (undoped) to 4.5 eV (heavily Al-doped). [55] Assuming that the Al-doped ZnO is degenerately doped, with the Fermi level located at or slightly above the conduction band minimum, it is reasonable to conclude that the electron affinity (difference between the vacuum level and the conduction band minimum) of ZnO is approximately 4.5 to 5 eV. Photoemission measurements of single-crystal ZnO, consistent with this conclusion, yield a work function of 4.57 eV. [56]

ZnO is a direct bandgap material. [57] There is some discrepancy in the literature regarding its bandgap energy; Srikant and Clarke claim that the true room temperature bandgap of ZnO is 3.3 eV, while a valence band to donor level transition at 3.15 eV accounts for the fact that a smaller value (typically 3.2 eV) is often reported. [58] Thus, the room temperature bandgap of ZnO can be confidently placed in the range 3.2 to 3.3 eV.

A high degree of n-type conductivity ($> 5000\ \Omega^{-1}\ cm^{-1}$) is attainable in ZnO, due to intrinsic defects, intentional donor doping (Al, In, Ga, B, F) or a combination thereof. [59] Reported thin film electron mobilities are typically ~20 to 30 $cm^2/V\ s$ [19, 48, 49]; the maximum mobility obtainable in ZnO single crystals is ~200 $cm^2/V\ s$. [57, 60] There is not a consensus in the literature as to which intrinsic defect (O vacancy or Zn interstitial) is responsible for intrinsic n-type conductivity. [60] P-type conductivity has not been convincingly or reproducibly demonstrated, although compensation of n-type doping through the introduction of acceptor impurities is possible. [61, 62] This difficulty in obtaining p-type ZnO is attributed to the phenomenon of self-compensation, as discussed in Section 2.3.1.

2.2.2 Photoconductivity

ZnO has long been known to exhibit an anomalously large and persistent photoconductivity. A change in conductivity by as much as seven orders of magnitude can be observed under UV illumination; the time constant of this photoresponse is typically extremely large, often taking days to return to equilibrium after illumination has been removed. [63, 64] Verification of this behavior was qualitatively observed in ZnO films fabricated during research leading to this thesis.

The observed ZnO photoresponse is generally made up of two components. The first is a fairly typical, rapid, and reproducible photoconductive response, while the second is a much slower response that is highly dependent on the gas ambient and pressure during the photoresponse measurement, on processing conditions, and on film history. The first process is typical photoconductivity, where UV radiation generates electron-hole pairs, thus increasing the free carrier density. The second process is nearly always attributed to chemisorption and photodesorption of oxygen at the film surface and/or grain boundaries, causing modulation of surface and/or grain boundary depletion regions and a corresponding modulation of the trapped charge to free charge ratio in the film. [61, 62, 63, 64]

The oxygen chemisorption/photodesorption process proceeds as follows. Adsorbed oxygen molecules or atoms at the surface or at grain boundaries within the film trap electrons (majority carriers), thus becoming chemisorbed; the resulting negative space charge induces a positive space-charge depletion region in the adjacent bulk, thus reducing the total free carrier density and the conductivity of the film. When UV illumination creates electron-hole pairs, holes (minority carriers) are drawn by the depletion region field to the surface and to grain boundaries where they are trapped by the chemisorbed negatively-charged oxygen. Thus, the chemisorbed oxygen returns to an adsorbed state, and may desorb (photodesorption) from the surface if the gas ambient is such as to make this favorable (e.g. low oxygen partial pressure). Upon removal of UV radiation, free holes recombine with free electrons, leaving an

equilibrium concentration of free electrons in the bulk. Adsorbed oxygen begins to trap electrons, space charge regions reform, and the conductivity decreases to its equilibrium (dark) value. Clearly this process is strongly dependent on gas ambient, as the oxygen partial pressure directly influences the adsorbed oxygen density.

The persistent nature of this photoconductivity is due to two slow processes that must occur to return the film to the equilibrium (dark) conductivity state: the adsorption/desorption of oxygen at the surface and at grain boundaries, and the diffusion of electrons from the bulk across surface and grain boundary depletion regions to complete chemisorption of adsorbed oxygen. At the film surface, oxygen that has trapped a hole under UV illumination may quickly desorb (depending on the oxygen partial pressure), thus requiring replacement by adsorption in returning to the equilibrium (dark) conductivity state (adsorbed oxygen at grain boundaries within the film may be less likely to desorb upon trapping a hole, due to physical constraints). Secondly, as the density of chemisorbed oxygen increases, the depletion region field hindering electron diffusion to surfaces and grain boundaries is increased, thus yielding a slow and decreasing rate of chemisorption regardless of the rate of oxygen adsorption.

2.3 Relevant materials and device theory

In the effort to develop electronic devices using transparent materials, it must be understood that this class of materials demonstrates a number of properties that differ significantly from those of traditional semiconductors. Since these materials must first satisfy the condition of optical transparency, it is reasonable to expect that optimal electrical and device-related properties will not be simultaneously realized; this is indeed the case. However, although such properties may be less than optimal, based upon classical electronic device expectations, they appear to constitute the relevant constraining attributes of these materials. In fact, a successful approach

to the development of this new technology will likely involve a creative approach to exploitation of these properties so as to yield novel devices and systems.

2.3.1 Self-compensation

Self-compensation is a phenomenon that arises as a consequence of the general tendency toward minimization of system energy. In typical semiconductor materials (e.g. Si), both n-type and p-type conductivity are easily attained by intentionally doping the host lattice with an appropriate impurity. Once incorporated into the lattice, these impurities introduce discrete energy levels in the bandgap near the valence or conduction band edge, thus modulating the Fermi level toward the relevant band edge and inducing free carriers in the band. [57]

However, as the bandgap of the semiconductor host lattice increases, this straightforward approach becomes less likely to yield the expected results. For nearly all materials with bandgaps larger than ~2.5 eV, at least one of the two conductivity types is essentially impossible to attain; in many cases appreciable conductivity cannot be attained for either carrier type. Without exception, in all of the well-known transparent conductors (e.g. In_2O_3, SnO_2, ZnO), conductivity is realized due to degenerate n-type doping (extrinsic and/or intrinsic) [13]; p-type doping of these materials, on the other hand, has not been reproducibly or convincingly demonstrated.

Self-compensation occurs when the overall system energy can be reduced by the creation of an intrinsic defect and the subsequent redistribution of electronic state occupancy. While the compensating intrinsic defect may in theory be either a vacancy or a self-interstitial, self-compensation seems to be more often attributed to vacancy formation. The remainder of this section assumes that self-compensation is mediated by vacancy formation; however, the same line of reasoning applies if the compensating defect is a self-interstitial. The essence of the following discussion is based upon that given by Van Vechten [65]; equivalent results are obtained elsewhere. [66, 67, 68]

In order to provide a simple framework within which to explain the mechanism of self-compensation, consider an n-type semiconductor self-compensated by the spontaneous formation of single-acceptor vacancies. In the absence of self-compensation, donor doping modulates the Fermi level toward the conduction band. The introduction of an acceptor into the n-type semiconductor lattice creates an empty energy level below the Fermi level, generally near the valence band. The system subsequently returns to electronic equilibrium by dropping an electron from a filled state near the Fermi level into the newly created acceptor level, with a concomitant decrease in electronic energy. This electron may come from the conduction band or from a midgap state (e.g. a donor level). This redistribution of electronic state occupancy moves the Fermi level downward; the average electronic energy gained with the introduction of each acceptor is equal to the difference between the Fermi level and the acceptor level. [65]

The introduction of such an acceptor level may be accomplished by the spontaneous creation of a vacancy at an appropriate lattice site. Clearly, however, energy is required to remove an atom from the lattice; thus the electronic energy gained due to the introduction of an acceptor state must be weighed against the energy required to create a neutral vacancy. As stated above, the average electronic energy gain is equal to the difference in energy between the Fermi level and the compensating acceptor level; the energy required to create a neutral vacancy, although not as easily determined, is certainly some constant value (i.e. not a function of Fermi level position), and may be quantitatively estimated using the macroscopic cavity model (MCM). [65] Thus, the Fermi level can be moved toward the conduction band by the introduction of donor impurities until the difference between the Fermi level and the energy level of the compensating acceptor is precisely equal to the energy required to form the neutral compensating vacancy, establishing an effective maximum equilibrium Fermi level position,

$$E_F^{max} = E_V + [\Delta H_f(V_{comp}^0) + E_A], \tag{2.1}$$

where E_V is the valence band maximum, $\Delta H_f(V^0_{comp})$ is the enthalpy of formation of the neutral compensating vacancy, and E_A is the difference in energy between the compensating acceptor level and the valence band maximum. From this point on, it is energetically favorable to form compensating defects rather than to modulate the Fermi level further toward the conduction band; the introduction of each additional donor is accompanied by the spontaneous formation of a compensating acceptor vacancy.

A parallel argument in the case of a p-type semiconductor self-compensated by the spontaneous formation of single-donor vacancies establishes a minimum Fermi level position,

$$E_F^{min} = E_C - [\Delta H_f(V^0_{comp}) + E_D], \tag{2.2}$$

where E_C is the conduction band minimum, $\Delta H_f(V^0_{comp})$ is the enthalpy of formation of the neutral compensating vacancy, and E_D is the difference in energy between the conduction band minimum and the compensating vacancy donor level.

Thus, for an arbitrary material, the equilibrium Fermi level is restricted to the range between some E_F^{min} and E_F^{max}. Typical values of $\Delta H_f(V^0_{comp})$, estimated using the MCM, are 2 to 4 eV [65]; the compensating donor (acceptor) level is generally less than 0.5 eV from the conduction (valence) band edge. On the basis of this model, self-compensation becomes possible in materials with bandgap larger than $\sim$2 eV, becomes increasingly likely as the bandgap moves toward larger values, and is essentially guaranteed to occur for both conductivity types in materials with bandgap larger than $\sim$4.5 eV.

Due to the nearly universal occurrence of strong self-compensation in materials with bandgaps sufficient to provide transparency in the visible region ($\gtrsim$3 eV), it is highly probable that transparent electronic devices will rely on p-n heterojunctions. Although the realization of bipolar doping and a p-n homojunction is certainly attractive from a performance standpoint, the inherent challenges in attaining this situation are significant. Thus, although from a materials-development perspective

the search for bipolar conductivity in transparent materials should and will continue, the development of transparent electronic devices at the present time must rely on the use of heterojunction-based devices.

2.3.2 Space-charge-limited current

In certain circumstances, currents far larger than those expected from Ohm's law can flow through an insulator. This is known as space-charge-limited current (SCLC). Although the phenomenon of SCLC was first studied and explained many years ago [69, 70, 71], it is not in general a well-understood topic. Brief mention, at most, is typically made of SCLC in material and device textbooks, as it is not often witnessed in conventional electronic devices. However, the wide bandgap materials appropriate for use in transparent electronic devices are more likely to exhibit SCLC than are those used in conventional electronics; a well-developed understanding of SCLC is an important tool in the development and characterization of transparent electronic devices. The following is based on the standard SCLC theory presented in a number of sources. [72, 73, 74]

Typically, if a bulk region is expected to influence device behavior, it is assumed that current flow in this region obeys Ohm's law. Ohmic current flow requires the existence of a non-negligible equilibrium concentration of carriers, n, in the relevant bulk region. An applied potential, V, across this region induces an electric field, ξ; carriers drift through the bulk, due to the applied field, with a constant velocity

$$v = \mu\xi, \tag{2.3}$$

where μ is the drift mobility. The resulting current density is

$$J_{ohmic} = qnv = qn\mu\xi, \tag{2.4}$$

where q is the electron charge.

Note that in ohmic conduction the equilibrium carrier concentration in the bulk is not disturbed; just enough carriers are supplied/extracted at the ends of the bulk

region to maintain the equilibrium carrier concentration. Thus, a change in ohmic current is due solely to a change in the drift velocity of the carriers, or equivalently to a decrease in the bulk transit time. SCLC, on the other hand, occurs when the bulk carrier concentration is enhanced above its equilibrium level; an increase in current is due not only to an increase in average drift velocity, but also to an increase in the number of carriers moving through the bulk.

The basis for SCLC behavior can be most easily understood in the context of a perfect insulator with ideal contacts. A perfect insulator, within the context of simple SCLC theory, is a wide bandgap crystalline material without bulk traps or other defects, and with no free carriers in equilibrium; an ideal contact supplies or removes carriers in excess of the number needed for bulk conduction while dropping a negligible voltage. Simple SCLC theory assumes the existence of an electron-injecting contact that supplies an infinite reservoir of carriers to the bulk, with a negligible injection barrier. This does not, however, imply that an infinite diffusion current flows from the contact into the bulk; for this reason, diffusion current is neglected in the simple SCLC model. Essentially, simple SCLC theory assumes that contacts do not limit overall current flow; contacts are neglected entirely.

Within this context, let a potential be applied across the bulk region. In the absence of an injecting contact, this would yield a constant electric field through the insulator (i.e. a parallel plate capacitor); this field is set up by equal quantities of positive and negative charge at the anodic and cathodic interface, respectively. Clearly, however, with ideal contacts in place, the electrons constituting the negative charge at the cathodic interface are partially drawn into the insulator by the field. The resulting negative space charge in the bulk, near the cathode, acts to inhibit an unrestrained rush of electrons into the bulk, so that an equilibrium bulk space charge distribution is reached; electrons move through the bulk, thus yielding SCLC.

The distribution of injected space charge can be precisely calculated [72, 73, 74], however more insight may be provided by a qualitative explanation. The field acts to

draw electrons toward the anode. However, it is clear that there must be some field remaining near the cathode in order to draw a continuous supply of electrons into the bulk. Current continuity requires a balance throughout the bulk between carrier density and electric field. Neglecting diffusion, the drift current,

$$J_{drift} = q\mu n(x)\xi(x), \tag{2.5}$$

must be constant throughout. With mobility a constant bulk parameter (assuming low field operation), the product of carrier concentration and electric field must therefore be constant. Since the electric field reaches a maximum at the anodic interface (i.e. all electric field flux lines pass through this plane), the carrier concentration must reach a minimum at this point. Similarly, since the field decreases monotonically from anode to cathode, the carrier concentration must simultaneously increase. Finally, since the cathode provides carriers with a negligible injection barrier, the electric field must be essentially zero at the cathode; thus, nearly all of the negative charge involved in setting up the electric field is located within the bulk (no flux lines pass through the cathodic interface).

A derivation of the SCLC current-voltage relationship is presented in a straightforward manner in a number of references [72, 73, 74]; such a derivation is not repeated here. The resulting expression for a trap-free insulator is

$$J_{SCLC} = \frac{9}{8}\epsilon\mu\frac{V^2}{L^3}, \tag{2.6}$$

where ϵ is the dielectric permittivity of the insulator, μ is the carrier mobility, V is the applied voltage, and L is the physical length of the insulator.

If the insulator contains bulk traps, the SCLC is reduced in proportion to the fraction, θ, of the total bulk space charge that is free to participate in conduction (not immobilized in traps); the ideal current-voltage relationship is directly multiplied by this fraction, yielding

$$J_{SCLC} = \theta(V)\frac{9}{8}\epsilon\mu\frac{V^2}{L^3}, \tag{2.7}$$

where, as indicated, θ is in general voltage-dependent. As the applied voltage and the current increase, the amount of space charge in the bulk also increases; this causes the electron quasi-Fermi level to move toward the conduction band. As the electron quasi-Fermi level moves through the band gap, θ varies according to the trap distribution.

For a discrete level of shallow traps (here the term shallow implies that the trap level, E_T, is above the electron quasi-Fermi level by kT or more), θ is independent of voltage. [72] The spatial variation of electric field, charge concentration, and potential remain the same as in the ideal case; the current is simply reduced due to the fact that trapped charge does not contribute to current flow. Further modifications to the ideal model can be made for multiple discrete trap levels, a uniform (in energy) trap distribution, and an exponential distribution. [72]

If the insulator contains a non-negligible concentration of equilibrium carriers (still assuming ideal contacts), SCLC is not immediately seen. For small voltages, the excess carrier concentration arising from injected space charge is much smaller than the equilibrium carrier concentration, so that conduction is approximately ohmic. As the voltage is increased, additional space charge is injected into the bulk by the increasing field at the cathode. When the injected space charge becomes comparable to the equilibrium carrier concentration, SCLC begins to dominate the current-voltage characteristics.

In order for injected space charge to make a non-negligible contribution to the net current density, injected carriers must be able to transit a significant portion of the bulk before the space charge perturbation is relaxed by majority carrier action. This occurs when the average transit time of an injected carrier,

$$\tau_B = \frac{L^2}{\theta \mu V}, \tag{2.8}$$

becomes smaller than the dielectric relaxation time

$$\tau_r = \rho \epsilon, \tag{2.9}$$

where ρ is the intrinsic resistivity of the bulk region. The transition from ohmic conduction to SCLC occurs when $\tau_B = \tau_r$. The voltage at this transition is

$$V_x = \frac{L^2}{\theta\mu\rho\epsilon} = \frac{qnL^2}{\theta\epsilon}, \tag{2.10}$$

where q is the electron charge and n is the intrinsic carrier concentration. The same result can be obtained, perhaps in a more intuitive manner, by equating the expression for ohmic current (Eq. 2.4) with the expression for SCLC (Eq. 2.7) and solving for voltage; the result is identical to Eq. 2.10 except for an additional multiplicative factor of 8/9 arising from Eq. 2.7. In practice, the expressions for ohmic and SCLC can be combined additively, with the net result that ohmic conduction dominates below V_x and SCLC dominates above V_x. [72, 73, 74]

2.3.3 Basic heterojunction energy band structure

Figure 2.1 serves to facilitate a discussion of the process used in constructing a basic pn heterojunction energy band diagram; this example provides a foundational procedure that is used to examine several variations on the degenerately doped n-type semiconductor / insulator heterojunction in Section 2.3.4. Further detail and analysis of pn heterojunctions can be found in the text by Wolfe *et al.* [75]

Figure 2.1a portrays energy band diagrams for the isolated p- and n-type regions, with the vacuum level (E_{vac}) serving as an energy reference. The conduction band and valence band discontinuities, ΔE_C and ΔE_V, are established as indicated in Fig. 2.1a; this procedure for establishing interfacial band discontinuities is referred to as the electron affinity rule (EAR). [75, 76] The EAR is based upon the assumption that, for an ideal heterojunction (i.e. in which there is no interfacial dipole), the local vacuum level (E^{ℓ}_{vac}) is continuous across the interface.

With the interfacial band discontinuities thus established, construction of the heterojunction energy band diagram begins by drawing the Fermi level (E_F); in equilibrium (zero applied voltage), E_F is constant across the heterojunction, as illustrated in Fig. 2.1b. Next, the bulk (i.e. beyond the junction space charge region) bands (E_C

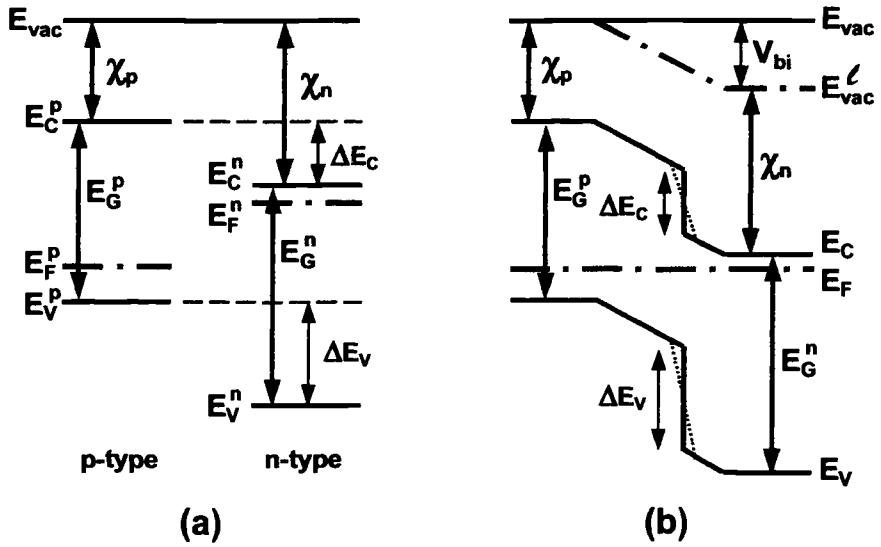

Figure 2.1: Energy band diagrams for isolated n-type and p-type semiconductors (a) and the corresponding pn heterojunction band structure (b) for an ideal interface (i.e. no interfacial dipole or fixed charge). The dotted portions of E_C and E_V at the interface in (b) indicate compositional grading resulting from chemical interdiffusion.

and E_V) and the local vacuum levels (E_{vac}^{ℓ}) for the p- and n-type regions are added; the Fermi level serves as an energy reference in locating the energy positions of the bulk bands, since the p- and n-type regions are in equilibrium beyond the junction space charge region (i.e. E_F returns to its equilibrium value with respect to E_C and E_V so that charge neutrality holds beyond the junction space charge region). Note that the bulk region local vacuum levels are established by adding the relevant electron affinity to the conduction band minimum. Moreover, the junction built-in potential, V_{bi}, defined as the change in the local vacuum level across the interface, is determined by the difference in the local vacuum levels of the bulk regions in Fig. 2.1b.

The next step is to establish the nature of the local vacuum level in the intermediate region between the p- and n-type bulk regions. The local vacuum level is continuous across the interface (based upon invocation of the EAR), with curva-

ture established by the junction space charge profile. The sign of the space charge on either side of the interface is determined by the relative positions of the bulk local vacuum levels, so as to yield the correct junction electric field polarity; negative (positive) space charge is required on the side of the junction where the local vacuum level is higher (lower). Alternatively, the sign of the space charge can be determined by comparing the relative Fermi level positions for the isolated materials, as depicted in Fig. 2.1a, and recognizing that, when these materials are brought into contact, electrons (holes) will flow from the material with a relatively higher (lower) Fermi level, thus giving rise to a positive (negative) space charge region in the material whose Fermi level (for the isolated materials, as shown in Fig. 2.1a) is relatively higher (lower); the driving force responsible for this charge exchange is a reduction in the net system energy.

For an arbitrary heterojunction, the required space charge regions may in general be established in one (or more) of several ways. In addition to the familiar pn junction depletion region, space charge may also arise as an interfacial accumulation region or due to a change in the equilibrium occupancy of deep levels. The specific form of the local vacuum level transition across the interface, therefore, may vary greatly depending upon the nature of the junction space charge, and in general warrants careful consideration. Recall that the junction electric field is related to the space charge profile according to Poisson's equation (given here in one dimension), [57]

$$\frac{d\xi(x)}{dx} = \frac{\rho(x)}{\epsilon}, \tag{2.11}$$

where ξ(x) is the electric field, ρ(x) is the space charge density, and ϵ is the dielectric constant. The voltage across the junction (which corresponds to the shape of the local vacuum level) is given by [57]

$$\frac{dV(x)}{dx} = -\xi(x). \tag{2.12}$$

Returning to Fig. 2.1b, note that the necessary space charge in this particular situation arises from the formation of typical pn junction depletion regions. The local vacuum level is connected across the junction according to the electric field typically resulting from such a space charge profile (a linear approximation is depicted for simplicity). The conduction and valence bands on either side of the interface follow the local vacuum level curvature to the interface, where they meet with discontinuities ΔE_C and ΔE_V as determined using the EAR in Fig. 2.1a.

The spatial dimensions of the space charge region on either side of the junction depend upon the space charge density. For a one-sided pn junction, the space charge region width is given by [57]

$$W = \sqrt{\frac{2\epsilon V_{bi}}{qN_B}}, \tag{2.13}$$

where ϵ and N_B are the dielectric constant and dopant concentration on the lightly doped side of the junction, q is the electron charge, and V_{bi} is the built-in potential (the difference in local vacuum level across the junction). This expression can be used to approximate the width of a space charge region segment for which the space charge magnitude can reasonably be represented as constant across the relevant segment of the space charge region; the value of V_{bi} is equal to the voltage dropped across the relevant space charge region segment.

This concludes construction of the pn heterojunction shown in Fig. 2.1b. However, several additional factors must be considered in a real heterojunction. First, the analysis presented thus far assumes a perfectly abrupt transition from one material to the other at the interface; in reality, some degree of chemical interdiffusion is quite likely to occur, particularly if high temperature processing is employed following junction formation. The effect of such interdiffusion is to form a "graded" interface, in which there is some transitional distance over which material properties such as bandgap and electron affinity make a smooth transition from one material to the other. The result is that abrupt interfacial conduction and valence band features (e.g. spikes, notches, and other discontinuities) are smoothed out to some degree

(depending on the extent of interdiffusion). The distance across which such compositional grading occurs is not related to the space charge region widths; rather it is established by physical diffusion and chemical reaction processes. The dotted portions of E_C and E_V at the interface in Fig. 2.1(b) indicate a moderate degree of such compositional grading.

Secondly, the space charge profile may be modified by the existence of interface charge (either fixed charge or interface states whose charge state depends upon Fermi level position) or an interfacial dipole. An interfacial dipole adds to or subtracts from the conduction band and valence band discontinuities established by the EAR; with this modification, junction band bending is determined in the manner discussed above. Interface charge (including the phenomenon of Fermi level pinning [57]) does not modify the conduction band and valence band discontinuities resulting from the EAR; rather, it constitutes an additional space charge contribution to be considered in establishing charge balance. Further discussion of such interfacial nonidealities may be found in the text by Wolfe *et al.* [75]

2.3.4 Degenerate semiconductor / insulator heterojunction energy band structure

Injection of charge into an insulator, as discussed in Section 2.3.2 for space-charge-limited current, in general requires an interface between an injecting contact (a metal or degenerately doped semiconductor) and an insulator. In anticipation of energy band diagrams presented in Sections 4.2.1 and 5.2.1, where n^+-ITO / i-ZnO heterojunctions play an essential role in establishing overall device performance, the discussion here examines several variations on the degenerately doped n-type semiconductor / insulator heterojunction. Of particular interest is the situation in which interface band alignment is such that charge can be efficiently injected into the insulator.

Little attention has been given in the literature to heterojunctions of this nature. Although the development of space-charge-limited current theory (Section 2.3.2) relies upon the existence of a low voltage injecting contact to an insulator layer, the early SCLC literature generally provides at best a cursory discussion of the nature of such a contact. [70, 77] The analysis performed by Mott and Gurney (solving Poisson's equation and equating drift and diffusion current throughout the insulator space charge region) yields an exact solution for the equilibrium (i.e. zero applied voltage) energy band profile and charge distribution in the insulator at an injector / ideal insulator interface. [69] Simmons performs a similar analysis, although his results differ from those obtained by Mott and Gurney due to the choice of bulk boundary conditions. [78] The reason for this ambiguity as to choice of bulk boundary condition arises due to the fact that both analyses consider only the charge contribution arising from conduction band electrons (and neglect the equilibrium conduction band electron concentration). This assumption is indeed valid near the metal / insulator interface (for an injecting contact); however, as the insulator relaxes toward equilibrium (in moving into the insulator, away from the interface) the excess conduction band electron concentration decreases until the net space charge is no longer reasonably approximated by the conduction band electron concentration. Thus, these "one-band" models provide insight into the behavior of injector / insulator contacts, and are in reasonable quantitative agreement with the true situation near the interface where the insulator space charge is indeed dominated by excess conduction band electrons; however, a smooth transition to insulator bulk equilibrium is not attained, since all space charge contributions are not considered.

Van Ostenburg and Montgomery employ a "two-band" model, in which both conduction band electrons and valence band holes are considered, to perform detailed analyses of metal / metal, metal / insulator, and insulator / insulator contacts; since all charge contributions are considered, a smooth transition to bulk insulator equilibrium is attained. [79] Similar results are given by Many *et al.*, within the context

of an arbitrary accumulation region. [80] Murgatroyd provides a survey comparing existing "one-band" and "two-band" models. [81]

The discussion presented within this section is meant to provide an intuitive understanding of these analyses, within the framework of heterojunction energy band analysis, and to elucidate the nature of charge injection into an insulator.

With the basic heterojunction band diagram construction process (presented in Section 2.3.3) in mind, consider the degenerate n-type semiconductor / insulator heterojunction illustrated in Fig. 2.2. The insulator is assumed to be an ideal, intrinsic insulator, free from midgap states; although such a defect-free material is impossible to obtain in practice, this example provides valuable insight into more realistic scenarios.

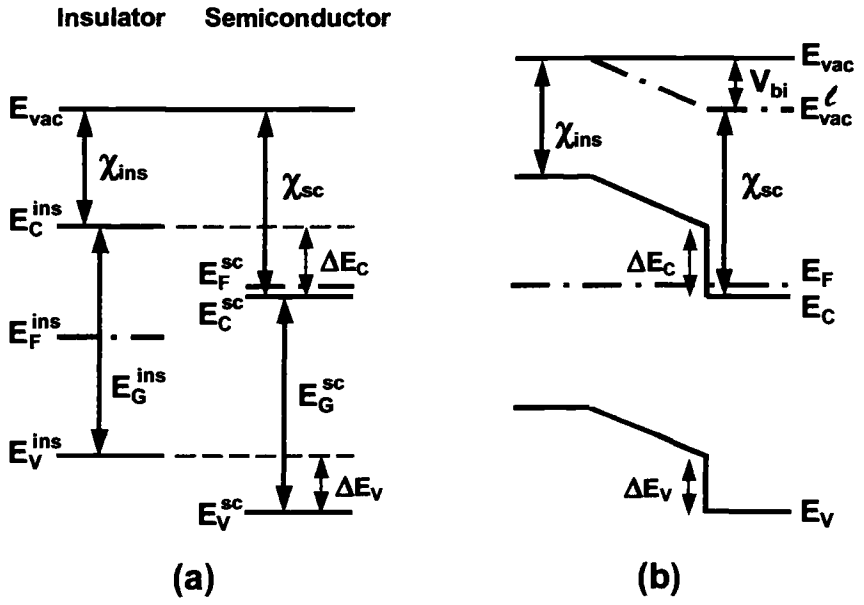

Figure 2.2: Energy band diagrams for (a) an isolated degenerate n-type semiconductor and a perfect insulator with $\chi_{sc} > \chi_{ins}$ and (b) the corresponding heterojunction band structure for an ideal interface (i.e. no interfacial dipole or interface charge). Spatial truncation of the insulator region for realistic insulator dimensions would result in elimination of much of the space charge region shown here and a concomitant reduction in V_{bi} (see Fig. 2.3 and accompanying discussion).

The energy band diagram depicted in Fig. 2.2b is obtained using the basic process described in Section 2.3.3 to obtain Fig. 2.1b, and is qualitatively similar to Fig. 2.1b in terms of interfacial band discontinuities and general band bending trends; however, the nature of the space charge region is significantly different. As is the case for the situation depicted in Fig. 2.1, the n-type semiconductor positive space charge region is that of a typical depletion region (although quite narrow, due to the degenerate doping level). The required negative space charge in the insulator, however, cannot originate from a depletion region, since the insulator is assumed to be ideal, and hence undoped; rather, negative space charge in the insulator arises due to the existence of conduction band electrons in excess of their equilibrium concentration (since the band bending in the insulator space charge region is such as to reduce the value of (E_C^{ins} - E_F) below its bulk equilibrium value, thus yielding negative charge associated with excess conduction band electrons).

For the situation depicted in Fig. 2.2, where $\chi_{sc} > \chi_{ins}$, the excess conduction band electron concentration at the interface and extending through the insulator space charge region is extremely small, so that the insulator space charge region width is concomitantly large. Table 2.3 lists the free conduction band electron volume concentration as a function of (E_C^{ins} - E_F) for an insulator with an effective conduction band density of states, N_C, equal to 3.5×10^{18} cm^{-3} and a dielectric constant $\epsilon = 9.0$ ϵ_0 (representative of ZnO, as discussed in Section 4.2.2). Table 2.3 also estimates the insulator space charge region width (W_{SCR}^{ins}) corresponding to the situation shown in Fig. 2.2b (using Eq. 2.13), with the space charge density estimated using the value of (E_C^{ins} - E_F) at the interface (this is the maximum space charge density in the insulator space charge region, thus yielding a gross underestimate of the true space charge region width). Assuming the insulator bandgap to be 3 eV, and the Fermi level to be located at midgap, V_{bi} (the total local vacuum level bending across the interface) is approximately equal to [$E_G^{ins}/2$ - (E_C^{ins} - E_F)] (see Fig. 2.2b).

Table 2.3: Free electron concentration, n, as a function of (E_C - E_F), and approximate space charge region width, W_{SCR}^{ins}, for a one-sided step junction with space charge density equal to n; $N_C = 3.5 \times 10^{18}$, $\epsilon = 9.0\ \epsilon_0$ (e.g. ZnO). V_{bi} is approximated as [$E_G^{ins}/2$ - (E_C^{ins} - E_F)], with $E_G^{ins} = 3$ eV.

E_C - E_F (eV)	n (cm^{-3})	$\sim V_{bi}$ (V)	W_{SCR}^{ins} (Eq. 2.13) (μm)
0.1	7.5×10^{16}	1.4	1.4×10^{-1}
0.2	1.6×10^{15}	1.3	9×10^{-1}
0.3	3.4×10^{13}	1.2	5.9×10^{0}
0.4	7.3×10^{11}	1.1	3.9×10^{1}
0.6	3.3×10^{8}	0.9	1.6×10^{3}
0.8	1.5×10^{5}	0.7	6.8×10^{4}
1.0	6.9×10^{1}	0.5	2.7×10^{6}

Clearly, if the value of (E_C^{ins} - E_F) at the interface is ~0.4 eV or larger, the space charge region width (as approximated in Table 2.3) becomes essentially infinite with respect to reasonable device dimensions; therefore, when the corresponding energy band diagram is plotted using a realistic distance scale, the slope of the insulator bands becomes negligibly small. Thus, from a practical perspective, for any application in which the insulator width is constrained to be on the order of a micron or less, the insulator space charge region depicted in Fig. 2.2b is truncated at an energy very close to the top of the interfacial conduction band discontinuity, before any significant band bending occurs, resulting in insulator bands that are essentially flat at an energy defined by the top of the interfacial conduction band discontinuity.

Figure 2.3 illustrates this spatial truncation of the energy band diagram as witnessed in practical devices. Identical degenerate n-type semiconductor contacts

are placed at each end of the insulator region (the heterojunctions are identical to that depicted in Fig. 2.2b). Figure 2.3a portrays the situation in which the insulator width is semi-infinite, so that the insulator is able to return to bulk equilibrium in the central portion. However, this energy band diagram is not appropriate for a practical situation in which a reasonable insulator thickness (e.g. $\lesssim$1 μm) is employed. The band diagram appropriate for practical insulator dimensions, as shown in Fig. 2.3b, may be intuitively understood by considering a process in which the semi-infinite insulator width in Fig. 2.3a is gradually decreased. When the space charge regions at either end of the insulator begin to overlap, further reduction in insulator width yields an incremental reduction in the net insulator negative space charge (as the widths of the depletion regions are incrementally reduced). If the insulator width is reduced until it is significantly smaller than the width of the space charge regions depicted in Fig. 2.3a for a semi-infinite insulator region, the residual band bending through the insulator region due to the remaining space charge is negligible so that the insulator bands are essentially flat, as indicated in Fig. 2.3b. Since the net insulator space charge is zero, no semiconductor depletion regions are required to satisfy charge balance; the space charge profile in Fig. 2.3b is essentially zero throughout.

As evident from Fig. 2.3b, the energy barrier to electron injection from the semiconductor into the insulator is essentially the conduction band discontinuity, ΔE_C (assuming ΔE_C to be $\sim$0.3 to 0.4 eV or larger); also, this barrier arises from the interfacial band discontinuity, rather than as a result of a junction electric field, yielding a built-in potential of zero. Electron injection at such an interface may be modeled by thermionic emission over a fixed energy barrier [57]; forward bias voltage (negative voltage to the semiconductor) is dropped entirely across the insulator, with a small and essentially voltage-independent current established by the conduction band discontinuity barrier height (until barrier lowering begins to occur at a high insulator field). Forward bias (negative voltage to the semiconductor) is initially established by a reduction of the semiconductor depletion layer charge. However, if the insulator

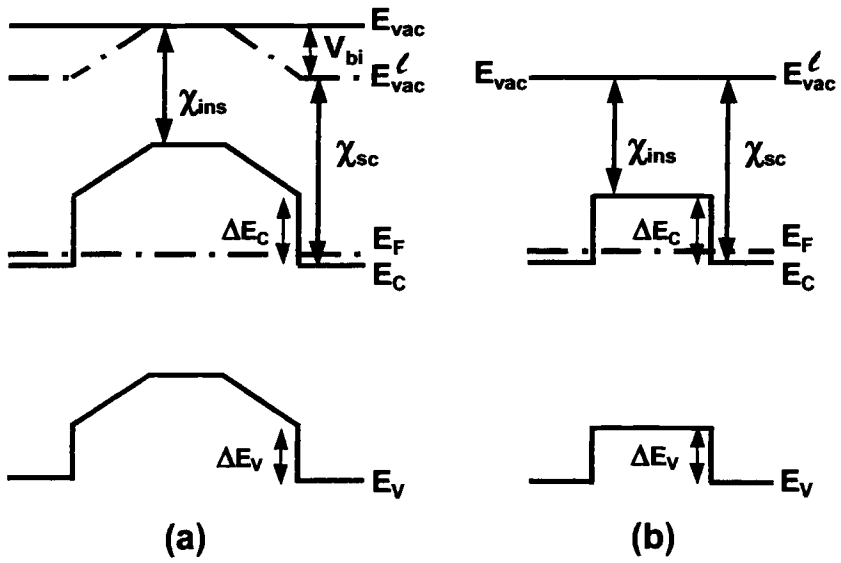

Figure 2.3: Energy band diagram corresponding to the degenerate n-type semiconductor / perfect insulator heterojunction depicted in Fig. 2.2, with an identical degenerate n-type semiconductor placed at each end of the insulator region, where the insulator width is (a) semi-infinite so that the insulator returns to bulk equilibrium at the central region, or (b) spatially truncated so as to reflect a realistic insulator width (e.g. $\sim$1 μm), thereby yielding insulator bands that are essentially flat due to the negligible space charge concentration.

charge is negligibly small, the equally small semiconductor depletion layer is nullified by the application of a small forward bias, after which additional forward bias is mediated by the formation of an electron accumulation layer in the semiconductor at the semiconductor / insulator interface, which is balanced by positive space charge (arising from the formation of a depletion region) at the opposite interface such that a constant electric field is established throughout the insulator region.

Note that the energy band diagram illustrated in Fig. 2.3b is identical to that expected for an ideal MIM capacitor with identical metal contacts. Such an energy band diagram is typically constructed by simple alignment of the metal Fermi levels, ignoring the Fermi level in the insulator (since equilibrium is not expected to exist in a wide bandgap insulator region of finite length with boundary conditions fixed by

contacts), and assuming that the insulator region contains no space charge. Therefore, although the energy band diagram result shown in Fig. 2.3b may seem rather peculiar when it is derived via conventional heterojunction analysis procedures (as established in Section 2.3.3), this analysis yields novel insight into the heterojunction device physics of moderate bandgap (e.g. ~3 to 4 eV) insulators or semi-insulators. Furthermore, since Fig. 2.3b corresponds to a well-known and relatively simple result (the MIM capacitor), confidence is gained with respect to the viability of the assessment procedure employed.

Figure 2.4 depicts a degenerate n-type semiconductor / insulator heterojunction where the electron affinity relationship, $\chi_{sc} < \chi_{ins}$, is opposite to that shown in Fig. 2.2. As in Fig. 2.2, the insulator is assumed to be an ideal, intrinsic material. This energy band diagram is again obtained using the basic procedure described in Section 2.3.3. However, the nature of the space charge region shown in Fig. 2.4b is even more complex than that witnessed in Fig. 2.2b. Although a quantitative analysis is not performed, it is clear that the interfacial band alignment is such that, at the interface, the insulator conduction band is quite near (and perhaps even below) the Fermi level. As such, the negative insulator space charge due to free conduction band electrons is quite large near the interface; an accumulation layer is formed. This accounts for the large field (reflected by the large slope of the local vacuum level) near the interface. However, this accumulation layer can only act to pull the insulator bands abruptly upward while the conduction band is below or near the Fermi level (since a large negative space charge density due to free conduction band electrons requires that E_F be quite near to E_C); in moving into the insulator (away from the interface), the insulator space charge density (conduction band electron concentration) decreases rapidly, as does the electric field and the slope of the local vacuum level, as indicated in Fig. 2.4b. When the insulator conduction band has been pulled to ~0.4 eV above the Fermi level, the space charge profile is approximately that discussed previously for Fig. 2.2b; although the insulator does indeed return to equi-

librium at some finite distance from the junction, the space charge density (composed of conduction band electrons) is so small that, as indicated in Table 2.3, this space charge region width is essentially infinite with respect to reasonable insulator region dimensions.

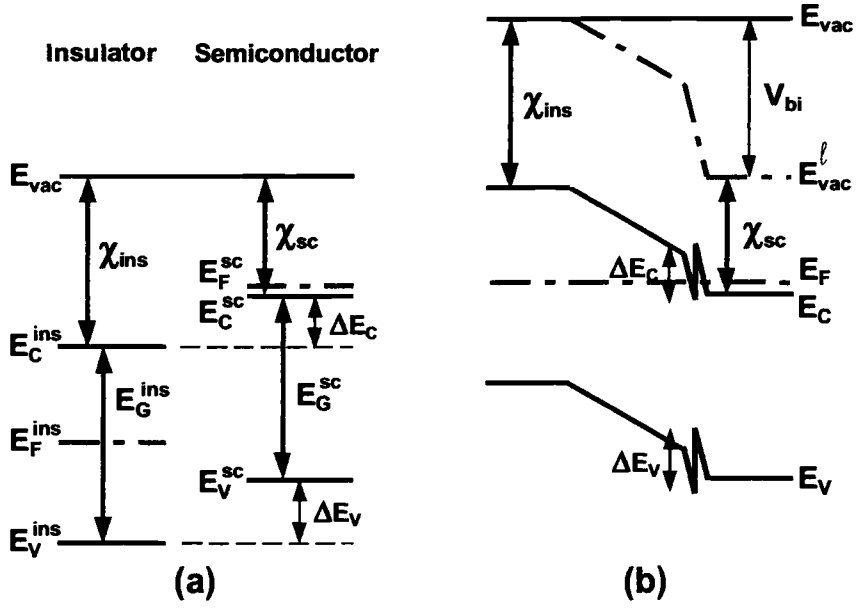

Figure 2.4: Energy band diagrams for (a) an isolated degenerate n-type semiconductor and a perfect insulator with $\chi_{sc} < \chi_{ins}$ and (b) the corresponding heterojunction band structure for an ideal interface (i.e. no interfacial dipole or interface charge). Note that the insulator region in (b) is assumed to be semi-infinite. Spatial truncation of the insulator region for realistic insulator dimensions would result in elimination of much of the space charge region shown here and a concomitant reduction in V_{bi} (see Fig. 2.5 and accompanying discussion).

Practically, for any application where the insulator width is constrained to be on the order of a micron or less, the insulator bands are essentially flat beyond the initial region of rapid change due to the interfacial accumulation layer; the semi-infinite space charge region is effectively truncated, in a similar fashion as discussed previously for Fig. 2.3. Figure 2.5 illustrates this spatial truncation for a structure

in which identical degenerate n-type semiconductor contacts are placed at each end of the insulator region (i.e. the same structure employed in Fig. 2.3). In Fig. 2.5a, the insulator width is semi-infinite; Fig. 2.5b illustrates the energy band diagram for more realistic insulator dimensions (e.g. $\lesssim 1$ μm), for which case the insulator bands are essentially flat (beyond the electron accumulation layer in the insulator at the interface) as a result of the negligible space charge concentration.

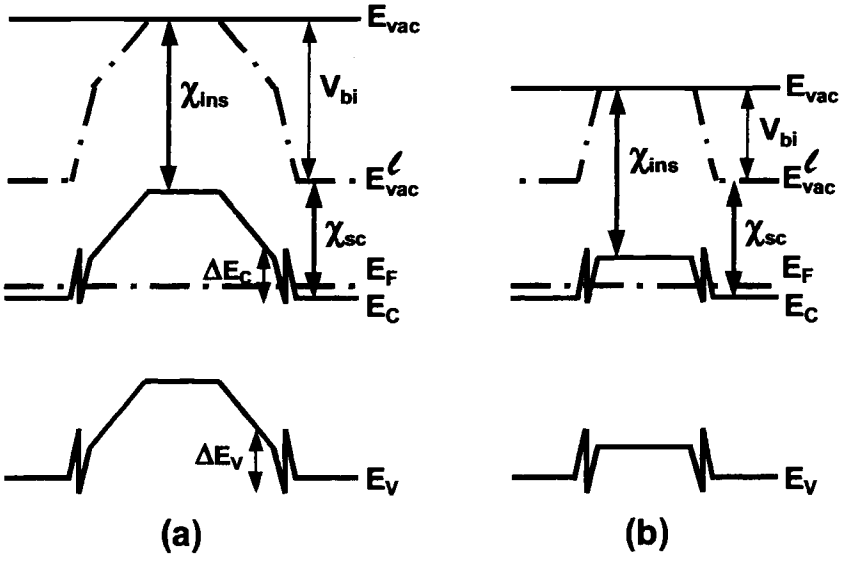

Figure 2.5: Energy band diagram corresponding to the degenerate n-type semiconductor / perfect insulator heterojunction depicted in Fig. 2.4, with an identical degenerate n-type semiconductor placed at each end of the insulator region, where the insulator width is (a) semi-infinite so that the insulator returns to bulk equilibrium at the central region, or (b) spatially truncated so as to reflect a realistic insulator width (e.g. ~ 1 μm), thereby yielding insulator bands that are essentially flat (beyond the electron accumulation layer in the insulator at the interface) due to the negligible space charge concentration.

Unlike the situation portrayed in Fig. 2.3b, the electron injection barrier in Fig. 2.5b arises as a result of a space charge induced junction field, yielding a non-zero

built-in potential. In equilibrium (i.e. zero applied bias), the negative space charge of the insulator accumulation layer is balanced by positive charge in a narrow depletion region in the degenerately doped semiconductor. This heterojunction embodies the ideal injecting contact assumed in the simplified space-charge-limited current model (Section 2.3.2). Although an electron injection barrier exists at the interface, the interface is capable of dropping at most $\sim$0.2 to 0.4 V in forward bias (negative voltage applied to the semiconductor) and can supply large current densities. Forward bias of the junction is established by a reduction in the semiconductor space charge region width; the concomitant reduction of the junction electric field strength causes the injected current magnitude to increase rapidly with junction forward bias. The forward bias current magnitude is effectively established by space-charge-limited current flow in the insulator, while the injector / insulator interface drops a negligible voltage ($\lesssim$0.2 to 0.4 V) for any finite current density; efficient electron injection into an insulator is thus attained.

Figure 2.6 illustrates a degenerate n-type semiconductor / insulator heterojunction similar to that depicted in Fig. 2.4; however, this situation is representative of a more realistic scenario in which the insulating nature arises due to self-compensation (as discussed in Section 2.3.1) rather than by the invocation of an ideal, defect free insulator material. Self-compensation of shallow donors (acceptors) is generally mediated by the formation of an equal concentration of fairly deep (e.g. $\lesssim$0.5 eV) acceptor-like (donor-like) defects near the valence (conduction) band. Although both donor-like and acceptor-like self-compensating defect levels are shown in Fig. 2.6, only the donor-like centers are active in establishing the heterojunction characteristics in Fig. 2.6b.

The heterojunction portrayed in Fig. 2.6b is similar to that depicted in Fig. 2.4b. However, in Fig. 2.6b the insulator space charge region contains an additional charge contribution arising from filled donor-like levels below the Fermi level, near the interface. This change in donor-like level occupancy establishes an additional negative

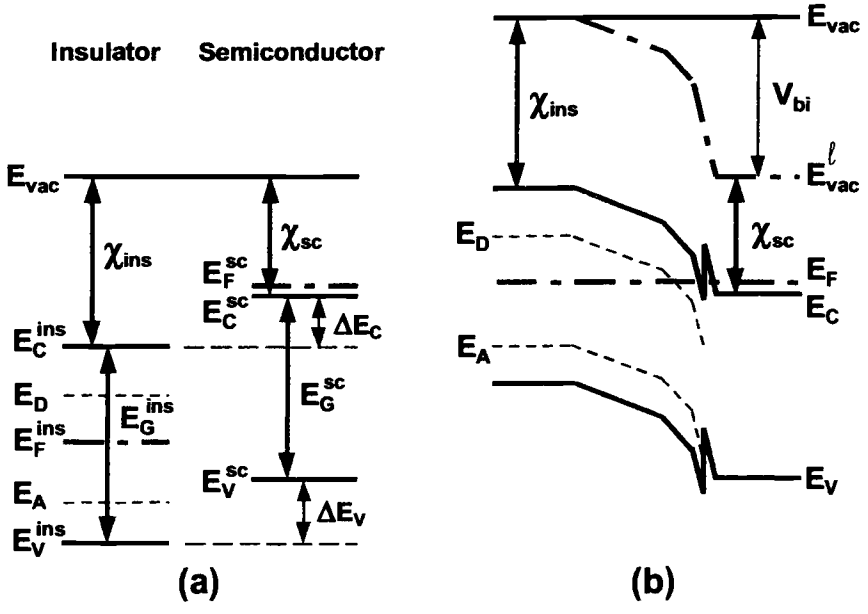

Figure 2.6: Energy band diagrams for an isolated degenerate n-type semiconductor and a self-compensated insulator with $\chi_{sc} < \chi_{ins}$ (a) and the corresponding heterojunction band structure (b) for an ideal interface (i.e. no interfacial dipole or fixed charge). Note that the insulator region in (b) is assumed to be semi-infinite. Spatial truncation of the insulator region for realistic insulator dimensions would result in elimination of much of the space charge region shown here and a concomitant reduction in V_{bi}.

space charge contribution to the insulator space charge region. To a first approximation, as indicated in Fig. 2.6b, there are three effective regions of distinctly different electric field (as witnessed by the three differing regions of local vacuum level slope in the insulator space charge region). As previously considered in Fig. 2.4b, the high field region closest to the interface is established by a conduction band electron accumulation layer, with the insulator conduction band below or slightly above the Fermi level. Further from the interface, the conduction band electron concentration decreases and the negative space charge due to filled donor-like levels constitutes the majority of the space charge. This region continues until the insulator bands have been pulled upward so that E_D is above the Fermi level; beyond this point, the donor-like levels return to their equilibrium occupancy (empty) and no longer make

a significant space charge contribution. Beyond this point, the space charge region is composed of residual conduction band electrons and residual filled donor levels (both concentrations are exceedingly small, since the Fermi level is well below both E_C and E_D); this constitutes the region of smallest insulator space charge region slope, and extends over an essentially infinite distance (as established by numerical calculations in Table 2.3). As discussed for Fig. 2.4, therefore, for reasonable device dimensions, the energy band diagram shown in Fig. 2.6b should be spatially truncated near the beginning of the final (furthest from the interface) space charge region segment in the insulator (as discussed previously for Figs. 2.3 and 2.5).

The essence of this discussion regarding Fig. 2.6 is that, even when the ideal insulator invoked in Figs. 2.2 and 2.4 is modified to reflect a more realistic scenario, the general characteristics of the heterojunction are retained. Thus, an understanding established upon the idealized situations depicted in Figs. 2.2 and 2.4, employing the general procedure discussed in Section 2.3.3, can be extended in a straightforward manner to the analysis of an arbitrarily complex scenario.

The analysis performed by Mott and Gurney, as discussed at the beginning of this section, yields an analytical solution for the injector / insulator heterojunction when the insulator carrier concentration is nondegenerate (i.e. for E_C - $E_F \lesssim 3kT$); this requirement is satisfied for a positive interfacial discontinuity injection barrier of 3kT or larger (ϕ_{inj} - $\chi_{ins} \gtrsim 3kT$). The voltage, V, and electron concentration, n, as a function of distance from the interface into the insulator, x, are given by [69]

$$V(x) = 2kT \ln\left(\frac{x}{x_0} + 1\right) \tag{2.14}$$

and

$$n(x) = n_0 \left(\frac{x_0}{x_0 + x}\right)^2, \tag{2.15}$$

where k is the Boltzmann constant and T is the temperature. x_0 is a characteristic length given by [69]

$$x_0 = \left(\frac{n_0 q^2}{2\epsilon kT}\right)^{-\frac{1}{2}}, \tag{2.16}$$

where q is the electron charge and ϵ is the insulator dielectric constant. n_0 is the insulator electron density at the interface; n_0 can be calculated using the standard expression for conduction band electron concentration in a nondegenerate material [57]

$$n = N_C \exp\left[\frac{-(E_C - E_F)}{kT}\right], \tag{2.17}$$

with E_C - E_F equal to the interfacial discontinuity injection barrier (ϕ_{inj} - χ_{ins}); the result is strictly valid only for ϕ_{inj} - $\chi_{ins} \gtrsim$ 3kT, so that the use of nondegenerate statistics is appropriate (N_C is the conduction band effective density of states).

Figure 2.7 portrays the insulator conduction band curvature at a metal / perfect insulator interface (assuming an ideal interface) calculated using Eq. 2.14 for several positive interfacial discontinuity injection barrier heights (ϕ_{inj} - χ_{ins} = 0, 0.1, 0.2, 0.3, and 0.4 eV). Since nondegenerate statistics (i.e. Eq. 2.17) are employed in obtaining Fig. 2.7, the ϕ_{inj} - χ_{ins} = 0 eV curve is not strictly accurate near the interface (i.e. where E_C - $E_F \lesssim$ 3kT); however this region accounts for a very short segment of the calculated curve, and the general characteristics of the curve are retained.

Several features of Fig. 2.7 are of interest in light of the preceding discussion. First, for an interfacial discontinuity injection barrier height smaller than ~0.2 eV, the shape of the insulator bands exhibits little dependence on barrier height, beyond a relatively narrow interfacial region where strong accumulation and the accompanying charge density act to bend the insulator bands rapidly upward. This observation serves to validate the discussion of injecting contacts accompanying Figs. 2.4, 2.5, and 2.6. For an interfacial discontinuity injection barrier height larger than ~0.3 eV, on the other hand, there is no appreciable insulator band bending (since the injected space charge density is exceedingly small), and the insulator bands are effectively constant at a level defined by the interfacial discontinuity injection barrier. This observation validates the discussion of non-injecting contacts accompanying Figs. 2.2 and 2.3.

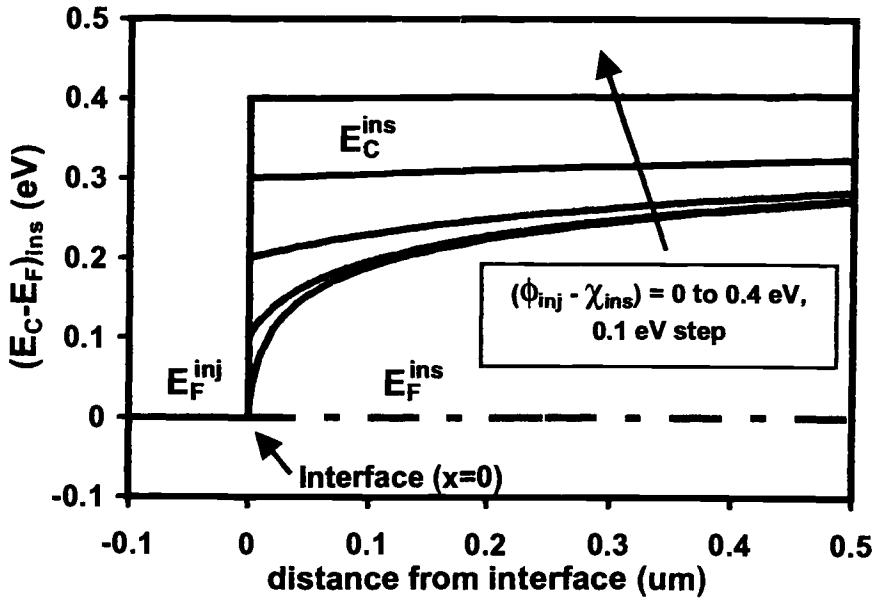

Figure 2.7: Energy band diagram (insulator valence band not shown) for a metal / perfect insulator heterojunction (assuming an ideal interface), calculated using Eq. 2.14 with $\epsilon = 9.0\ \epsilon_0$ and $N_C = 3.5 \times 10^{18}$ cm^{-3} (e.g. ZnO), for ϕ_{inj} - χ_{ins} (the interfacial discontinuity injection barrier) equal to 0, 0.1, 0.2, 0.3, and 0.4 eV. Note that nondegenerate statistics are employed to calculate $(E_C - E_F)_{ins}$, so that the ϕ_{inj} - $\chi_{ins} = 0$ eV curve is not strictly accurate near the interface (i.e. where $E_C - E_F \lesssim 3kT$).

2.3.5 Implications of low mobility and conductivity

As mentioned previously, the necessity of choosing from materials that exhibit optical transparency necessitates acceptance of less than optimal electrical properties. Perhaps the best example of this tradeoff is demonstrated with respect to carrier mobility. Whereas traditional semiconductor materials (e.g. Si, Ge, GaAs) exhibit mobilities in the range of ~400 to 8000 cm^2/V s, typical transparent semiconductor thin film mobilities are rarely higher than ~30 cm^2/V s, and are often small enough so as to be essentially unmeasurable ($\lesssim$1 cm^2/V s) using conventional Hall analysis.

An obvious consequence of such low mobility is that higher carrier concentrations are required to obtain a degree of conductivity that might be considered reasonable in the context of traditional semiconductor materials. However, this does not

provide a simple solution, as heavily doped materials are not necessarily conducive to the fabrication of active electronic devices. In a pn junction, for example, the doping of one or both of the p and n-type materials must be low enough that tunneling does not occur across the junction; traditional transparent conductors rely on degenerate doping that is far too large for even this basic application. Thus, it is clear that in applying these materials to device development, reasonable doping limits enforce a maximum level of useful conductivity for a given mobility. The range of practical conductivity values is far lower than that appropriate to traditional semiconductor materials, and it must be kept in mind that simply increasing the conductivity of a given material may not be beneficial from a device perspective.

2.4 Transparent electronic devices in the literature

Although n-type transparent conductors have been used in passive applications for many years, the realization of transparent active electronic devices has only become possible with the recent effort to develop p-type transparent conductor and semiconductors. The following discussion constitutes a review of transparent and semi-transparent active electronic devices (diodes and transistors) that have been reported in the literature, interspersed with brief comments concerning relevant characterization and fabrication issues and concerns.

It should be mentioned here that the fabrication of transparent passive electrical devices (resistors and capacitors) is of little relevance to the development of transparent active electronic devices, and is therefore absent from the following literature review. Transparent thin-film resistors rely only upon the ability to control doping and geometry of an arbitrary transparent semiconductor film. Likewise, a transparent capacitor is realized simply by stacking a wide bandgap insulating film (e.g. Al_2O_3, SiO_2, Si_3N_4) between transparent conducting electrodes.

2.4.1 Transparent diodes

A number of transparent or semi-transparent diodes have been reported in the literature, particularly as research into new transparent conductors has recently intensified. In several cases, these results arise as a consequence of research on new p-type transparent conductor materials; often electrical characterization of the reported transparent diode is neglected in part or entirely. The observation of rectification is typically presented as evidence for the p-type nature of the new material, accompanied perhaps by a current-voltage measurement. Thus, such reports of transparent diodes should be taken in context; although they are generally reported as being pn junctions, this claim is often based only upon the fact that some degree of rectification is observed. The existence of a rectifying current-voltage curve is not, in general, conclusive evidence that a true pn junction has been formed.

Apparently, the earliest reports of semi-transparent rectifying devices rely on the use of NiO as the p-type material. NiO has a bandgap of ~3.6 to 4 eV and can be doped (intentionally with Li, or due to intrinsic defects such as Ni vacancies or O interstitials) to obtain a p-type conductivity of ~0.1 to 1 Ω^{-1} cm^{-1} with mobility as high as 0.1 to 1 cm^2/V s and hole concentration ~10^{18} to 10^{19} cm^{-3}. [34]

In 1993, Sato *et al.* reported the fabrication of Al / p$^+$-NiO / i-NiO / i-ZnO/n$^+$-ZnO:Al / Al diodes with ~1 order of magnitude rectification and ~20% transparency in the visible region [34]; both NiO and ZnO were deposited by RF sputtering. This structure is not technically transparent, as Al is used to contact the p$^+$-NiO layer; however, if the p$^+$-NiO layer is indeed degenerately doped, this contact could probably be made using any degenerate transparent conductor. Attempts to form Al / p$^+$-NiO / n$^+$-ZnO:Al / Al diodes resulted in ohmic current-voltage characteristics, attributed to tunneling through the narrow depletion region arising due to the heavy doping of both the n- and p-type regions. This illustrates the important point that the typical degenerately-doped transparent conductor materials cannot be used exclusively to form rectifying junctions; rather a lightly-doped ($\lesssim 10^{17}$ to 10^{18} cm^{-3}) region must be

interposed between heavily-doped p and n regions. Due to the typically low mobilities of this class of materials, the conductivity of this lightly-doped region will probably be quite low; however this is unimportant as this material functions similarly to the depletion region of a simple pn junction diode, thus making no contribution to parasitic series resistance.

Ohya *et al.* used a liquid phase deposition method (dip coating) to form NiO and ZnO layers for Au / ZnO:Al / NiO(:Li) / Au and ITO / ZnO:Al / NiO:Li / Au diodes. [82] The degree of transparency is not given, however it is stated that the NiO and ZnO films are transparent; the ZnO/NiO stack probably exhibits transparency similar to that of Sato *et al.* [34] Significant differences in electrical characteristics (strong rectification vs. essentially symmetric current-voltage curves) are observed between the two structures; although the physical structures are different, the fact that two different ZnO contact materials are employed constitutes a strong indication that the contacts play an important role in determining the overall measured device characteristics. Ideal pn junction capacitance-voltage characterization techniques are applied directly to these structures; although the data appears to fit the expected relationship, the results are essentially nonsensical (for example, a negative built-in potential is obtained in one case). This indicates the futility of applying ideal pn junction theory to an arbitrary structure simply because it contains an interface between p- and n-type materials. In this case, it is unclear whether the ZnO / NiO junction is responsible for the measured electrical characteristics. It may just as well be that an unidentified contact or bulk effect is being measured; the current-voltage characteristics clearly do not represent those of an ideal pn junction. It is unlikely that invocation of ideal pn junction theory will in general provide any real insight into devices of this nature.

The third NiO-based device was reported by Lee *et al.*, using sputter deposition and patterning through lithography. [83] Although the focus of this report is not transparency, the use of transparent materials for the active region is of interest

here. Two to three orders of magnitude rectification is obtained, and current-voltage measurements are reasonably close to those expected from ideal pn junction theory. The contribution of contacts is questionable, as the ITO in particular is lightly doped ($\sim 10^{16}$ to 10^{17} cm^{-3}); confirmation that the contacts are ohmic is not explicitly given. Regardless of questions of interpretation, however, these three reports [34, 82, 83] indicate that NiO may be of practical interest as a transparent p-type material for use in the development of transparent electronics.

Kudo *et al.* gave the first report of a highly transparent diode (p-$SrCu_2O_2$ / n-ZnO) in 1999 [84], followed by the observation of forward-bias UV emission from the same heterojunction. [85, 86] These diodes, fabricated from all transparent materials (including contacts), exhibit an average transparency of ~70% in the visible region and UV forward-bias emission centered at ~3.2 eV; the forward-to-reverse current ratio is ~80 between -1.5 and 1.5 V. UV emission is attributed to radiative recombination of electrons in the n-ZnO layer with holes injected from the p-$SrCu_2O_2$ layer. Although little electrical characterization is presented, current-voltage characteristics resemble those expected for such a p-n heterojunction. It appears that the use of photolithography may have been an important factor in obtaining devices of sufficient quality to exhibit UV emission.

The first detailed electrical characterization of a transparent diode was given by Hoffman *et al.* [87] The p-$CuYO_2$:Ca / i-ZnO / n-ITO diodes [88] exhibit a forward-to-reverse current ratio of ~60 between -4 and 4 V, and average transparency in the visible region of ~35 to 65%. Characterization details are given in Chapter 4.

The realization of bipolar conductivity in $CuInO_2$ [4] led to the report of the first transparent pn homojunction diode. [89] This fully transparent structure (using ITO contacts) exhibits ~60 to 80% transparency in the visible region and a forward-to-reverse current ratio of ~10 between -4 and 4 V. Electrical characterization consists of a current-voltage measurement; the relatively large reverse leakage current is in-

consistent with that expected for an ideal p-n homojunction, leaving some question as to the true mechanism behind the observed rectification.

Although there have been several recent reports of ZnO pn junctions [90, 91, 92], there is significant doubt as to the validity and reproducibility of these results. [60, 93] Aoki *et al.* reported rectification and weak forward bias white-violet emission from a Au / "p-ZnO"(50 nm) / n-ZnO(substrate) structure. Direct experimental evidence for a p-type ZnO layer is apparently not obtained; rather, the observation of rectification and forward bias emission is taken as evidence that a pn junction has indeed been formed. The Au / "p-ZnO" contact is characterized by passing a lateral current between two such contacts; a linear current-voltage curve is taken as evidence that the contacts are ohmic. However the currents observed in this measurement are four orders of magnitude smaller than seen in the diode structure at similar voltages. The contacts are not characterized in the relevant current range, and the linear current-voltage curve is almost certainly due to the fact that the applied voltage is dropped across the horizontal current path through the bulk rather than at the contacts. Light emission appears to be witnessed only for relatively large voltages ($\gtrsim$10 V). It seems probable that the true structure is Au / i-ZnO / n-ZnO, that rectification occurs due to asymmetrical electron injection into the i-ZnO layer (efficient injection from n-ZnO, poor injection from Au), and that the observed light emission is a high-field effect (10 V applied across a 50 nm i-ZnO film yields a field of 2 MV/cm).

The report given by Ryu *et al.* [91] is similarly lacking in electrical characterization and interpretation of results to fortify the claim of pn junction formation. Extremely weak rectification is observed, with a forward-to-reverse current ratio of $\sim$3 between -2 and 2 V; light emission is not observed. No attempt is made to explain the observed current-voltage characteristics in terms of the expected behavior of a pn homojunction. The conclusion that a pn junction has been formed does not seem to be justified in light of the little corroborating experimental evidence that is presented.

Finally, Guo *et al.* report a transparent ZnO light-emitting diode (LED). [92] Although the interpretation of results is more thorough and careful than in the preceding cases, similar issues remain. The observed rectification is again quite weak, with a forward-to-reverse current ratio of ~3 between -2 and 2 V. Light emission is reported to begin at 5 to 10 V, however the included electroluminescent (EL) spectra appear to have been measured at much higher voltages (EL spectra are denoted by diode current rather than by voltage). The authors do note that, due to the relatively low doping level of the supposed "p-ZnO" layer, the device might alternatively be considered a metal / insulator / semiconductor (MIS) LED. This seems to be a more likely explanation in light of the observed electrical characteristics, and again points to high-field light emission rather than minority carrier injection and radiative recombination due to adjacent p- and n-type ZnO regions. However, the authors appear to be quite convinced that they have indeed obtained injection luminescence.

2.4.2 Transparent transistors

The literature appears to contain only one report of a semi-transparent transistor. In 1997 Prins *et al.* reported the fabrication of a transparent ferroelectric thin film transistor (TFT). [94, 95] SnO_2:Sb is used for the channel material, $SrRuO_3$ for the gate electrode, and $PbZr_{0.2}Ti_{0.8}O_3$ (PZT) for the gate insulator. PZT, a well-known ferroelectric material, is polarized by the application of a voltage to the gate electrode, thus allowing the transistor to be used as a memory element. The focus of this report is on the ferroelectric nature of the device; little electrical characterization is presented. The claim to transparency is backed up only by the statement that optical absorption is some tens of percents; thus it might be reasonable to assume that the transparency is ~50 to 60% or less. Optical absorption is attributed to the $SrRuO_3$ gate electrode; $SrRuO_3$ is not transparent, however the film is made thin enough that optical transmission is not completely suppressed. [96, 97] It is mentioned in passing that an alternate structure using heavily-doped SnO_2 for the gate

electrode was fabricated to verify that higher transparency can be achieved. There is, however, no further discussion of this device.

A GaN-based TFT was reported by Kobayashi *et al.* in 1997 [98]; although their realization of the device utilized opaque gate (c-Si) and source/drain (Al) electrodes, the possibility of using transparent electrodes to form a fully transparent device is mentioned. It is curious that this was not (apparently) done, as it should have been a fairly simple extension of the process used to fabricate the reported device. Again, a detailed electrical characterization of the transistor is not presented.

European Patent Application No. 99972374.5 [99] includes a set of I_D-V_{DS} measurements for an n-channel, depletion mode TFT using ZnO as the channel material. No other material or fabrication details are given. This patent application essentially claims every possible realization of a transparent transistor (MOSFET, JFET, and BJT), using any possible combination of transparent materials.

United States Patent No. 5,744,864 [96] and the corresponding international patent application [97] claim a number of variations on the transparent TFT concept; electrical characteristics presented in this patent are based on the semi-transparent ferroelectric TFT reported by Prins *et al.* The channel layer is specified to be a degenerately-doped semiconductor with mobility greater than 10 cm^2/V s; thus the envisioned device operates in depletion mode, and the scope of the claim does not appear to encompass enhancement mode devices.

2.5 Conclusions

This chapter provides a summary of important issues relevant to the development of transparent electronic devices. A brief introduction to transparent conducting and semiconducting materials is given; the simultaneous existence of optical transparency and electrical conductivity is explained. Known n- and p-type transparent conductor materials are tabulated, along with important thin film electrical and optical properties as available in the literature. Particular attention is given to ZnO, due

to its importance in achieving results presented in this thesis; the anomalous persistent photoconductivity that can be exhibited by ZnO is explored and, in agreement with the bulk of the literature, is attributed to oxygen chemisorption/photodesorption at surfaces and grain boundaries.

Several materials and device issues of particular interest in the development of transparent electronics are discussed. Self-compensation, the compensation of intentional dopants by the spontaneous creation of intrinsic defects, places an upper limit on maximum doping for a given material and prohibits bipolar conductivity in nearly all wide bandgap materials. Space-charge-limited current, a non-ohmic bulk conductivity mechanism, is much more likely occur in wide bandgap materials than in conventional semiconductors. The phenomenon of carrier injection into an insulator is explored through application of conventional heterojunction energy band diagram analysis. Transparent semiconductor materials exhibit much smaller mobilities than do conventional semiconductors; acceptable conductivities for device applications must be reduced accordingly.

The chapter concludes with a review of transparent active electronic devices reported in the literature. Since the number of such reports is small, an individual assessment of each is possible. In many cases, little electrical characterization is presented; interpretation of results is often questionable. Common characterization pitfalls such as the inappropriate application of ideal pn junction theory and insufficient characterization of contact contributions to measured electrical characteristics are noted and discussed.

3. EXPERIMENTAL TOOLS AND TECHNIQUES

This chapter describes experimental tools and techniques utilized in the research leading to this thesis. Thin film deposition and processing tools and methodology are first discussed. Several important thin film optical and electrical characterization techniques are noted; the theoretical basis for each technique is examined. The chapter concludes with a discussion of the optical and electrical characterization of transparent electronic devices.

3.1 Thin film deposition and processing

This section examines thin film deposition and processing tools. The evaporation and sputter deposition processes are discussed, followed by a look at post-deposition rapid thermal processing (RTP).

3.1.1 Evaporation

Evaporation is perhaps the simplest and most intuitive thin film deposition method. [100] A solid phase evaporation source is heated, under high vacuum ($\lesssim 10^{-6}$ Torr), until its vapor pressure is sufficiently high that atoms sublime (evaporate) from the solid (liquid) phase and travel through the gas phase to condense on the substrate. Low pressure ensures that evaporated atoms can travel the source to substrate distance uninterrupted by gas phase collisions, as well as minimizing the incorporation of gas phase impurities into the growing film.

Thermal evaporation is accomplished by passing a large current through a refractory metal (e.g. W, Mo, Ta) boat or wire basket containing the evaporation source material. Alternatively, the source material may be contained in a ceramic (e.g. Al_2O_3) crucible which is then placed within a refractory wire coil. Electron beam evaporation employs a high energy electron beam to heat the evaporation source material (typically a pressed ceramic pellet). The electron beam is focused onto a small

area of the pellet, providing intense localized heating. For this reason, electron beam evaporation can be used to deposit materials that require much higher temperatures than are attainable using thermal evaporation; however, the material must be a poor thermal conductor so that intense localized heating is possible.

Deposition of binary and higher order compound films through evaporation generally requires the use of multiple evaporation sources; direct evaporation of a multi-component source material often results in a different stoichiometry in the film than in the source material, as each atomic component has a different vapor pressure and sticking coefficient at the substrate. Electron beam evaporation tends to yield a more stoichiometric evaporation rate at the source, due to the intensity of the heat provided, however unmatched sticking coefficients may still present a problem. The use of multiple evaporation sources allows independent control of the evaporation rates of each atomic component, although with a concomitant increase in processing complexity.

While evaporation is typically done at the lowest possible pressure, reactive evaporation utilizes a controlled flow of a reactive gas that is incorporated into the growing film. The reactive gas may serve as the sole source of the relevant atomic component, or may be included to improve an otherwise deficient stoichiometry. Since the pressure must be low enough that evaporated atoms can transit the source to substrate distance with few gas phase collisions, there is an effective upper limit on the amount of reactive gas that may be introduced; thus incorporation of the reactive gas component into the growing film cannot be further increased by simply increasing pressure beyond this limit. Further improvement can be attained, however, by employing activated reactive evaporation (ARE). ARE uses a low pressure plasma source to break reactive gas molecules (e.g. O_2) into highly reactive radicals (e.g. O). Thus incorporation of the reactive gas component into the film is enhanced while maintaining the low pressure necessary for evaporation.

3.1.2 Sputtering

Thin film deposition via sputtering involves the physical removal of atoms from a metallic or pressed ceramic target through bombardment with high energy ions. [100] Sputtered atoms are ejected from the target with sufficient energy to cross the target to substrate distance and condense on the substrate. In the more common RF and DC sputtering methods, a voltage is applied between the target and the substrate to generate ions and accelerate them toward the target; RF sputtering applies an AC voltage (typically 13.56 MHz), while DC sputtering applies a DC voltage. In an ion beam sputtering system, an ion source and extraction assembly (ion gun) are used to direct a beam of high energy ions at the sputter target. The ion beam sputtering process is discussed in some detail here, as it has been extensively used in this thesis research. Specific details of system operation refer to the modified Veeco ion beam sputtering system in the OSU ECE solid state processing lab.

Ion beam sputtering employs a collimated beam of energetic positive ions directed at the surface of the sputter target by the ion gun. As ions strike the target surface, a portion of their energy is transferred as kinetic energy to atoms in the sputter target, ejecting them from the target surface. The process is carried out under a sufficiently high vacuum so that ejected sputter target atoms are able to transit the target-to-substrate distance with a minimal number of gas phase collisions. Impinging sputtered atoms condense onto the substrate, forming a thin film. An inert gas such as Ar is typically used as the sputter gas; if a reactive gas (e.g. O_2) is combined with the inert sputter gas, film growth may further rely on reaction of the reactive gas phase component with sputter target atoms as they arrive at the film surface; this is known as reactive sputtering.

The ion source is a low-pressure DC discharge, contained in a cylinder mounted on the process chamber. An electron emitting filament (e.g. W), the cathode, supplies electrons to the discharge; these electrons are accelerated toward the metal cylinder, the anode, by an applied potential ($\sim$40 V). An electromagnet mounted outside the

ion source chamber (magnet coils wrapped around the cylinder) produces a magnetic field parallel to the axis of the cylinder. This magnetic field deflects the electrons into cycloidal trajectories due to the Lorentz force,

$$\vec{F_L} = q\vec{v}\times\vec{B}, \tag{3.1}$$

where q is the electron charge, $\vec{v}$ is the electron velocity, $\vec{B}$ is the magnetic field, and $\times$ denotes the vector cross product. This serves to increase the distance traveled by each electron between emission from the cathode and collection by the anode; each emitted electron is able to participate in a greater number of collisions. A controlled flow of sputter gas is introduced into the discharge chamber through a precision leak valve or mass flow controller (MFC); high energy electrons generate ions (and free radicals, if a reactive gas such as O_2 is used) through collisions with neutral gas atoms/molecules.

Ion extraction and acceleration is accomplished by the application of a large positive DC potential ($\sim$600 to 1000 V) to the ion source assembly (relative to the grounded deposition chamber). Collimation of the ion beam is accomplished by a set of three parallel grids between the ion source and the deposition chamber. The top grid (nearest the ion source) is kept at the anode potential, electrically screening the ion source from the large accelerating field. The middle grid is negatively biased ($\sim$250 V) in order to suppress the backflow of electrons from the processing chamber into the ion source. The grid assembly also serves to restrict gas flow into the deposition chamber, thus maintaining a pressure differential between the ion source and the deposition chamber. Such a pressure differential allows the coexistence of a high enough pressure in the ion source chamber to maintain a stable plasma discharge, and a low enough pressure in the target chamber to keep the mean free path for the ion beam and sputtered particles sufficiently large.

The collimated ion beam is directed to the sputter target surface. The positive space charge of the ion beam can result in spatial dispersion of the beam due to like-

charge repulsion. Charging of the target surface can also result in a reduced and time-varying sputter rate. In order to minimize such adverse effects, an electron emitting filament (neutralizer) is placed within the ion beam path, allowing neutralization of the positive ion beam space charge. Since the ion beam and target surface charge can be neutralized in this way, it is theoretically possible to sputter insulating targets without excessive charging and heating. Practically, however, ion beam sputtering is probably not suited to the deposition of high quality insulator films.

3.1.3 Post-deposition annealing

Post-deposition annealing of thin films is an important step in the fabrication of transparent electronic devices. [100] Perhaps most important is the enhancement of crystallinity beyond that of the as-deposited film; also important is the modification of film stoichiometry by annealing in an appropriate gas ambient. Stoichiometry is important in determining the degree of conductivity in many transparent semiconductor materials, since intrinsic defects are often directly responsible for conductivity (e.g. oxygen vacancies in ZnO and ITO). Electronic transport is strongly influenced by crystallinity and stoichiometry; a crystalline material has a much higher mobility than that of the same material in amorphous or polycrystalline form, and the degree of stoichiometry is directly related to defect concentration, also strongly influencing mobility.

Rapid thermal processing (RTP) is the post-deposition annealing method used throughout this thesis research. RTP uses an array of halogen lamps and a cooling mechanism to facilitate rapid heating and cooling of the sample; temperature ramp times are typically on the order of 30 seconds or less. In addition to the simple benefit of consuming less time than traditional furnace annealing, RTP offers the ability to anneal devices fabricated on glass substrates at significantly higher temperatures than would be otherwise possible. Since heating and cooling can be done rapidly, a glass

substrate can be annealed at temperatures ~200°C higher than would be possible in a traditional furnace, without damage due to excessive substrate warping or strain.

3.2 Thin film characterization

The development and fabrication of transparent electronic devices requires a thorough understanding of the optical and electrical properties of potentially useful materials; such an understanding is developed through the application of appropriate characterization tools and techniques. A careful and consistent approach to thin film characterization provides a solid basis for selecting the appropriate material combinations and processing conditions to yield desired device characteristics, and permits a more sophisticated approach to analysis and interpretation of experimental device characteristics. This section outlines a number of useful optical and electrical thin film characterization techniques.

3.2.1 Optical transmission and bandgap

Optical measurements can, in principle, be used to determine both the bandgap energy and transition type (allowed direct, forbidden direct, allowed indirect, forbidden indirect), as well as the degree of transparency of a thin film. Practically, characterization of the bandgap requires fitting of experimental data to one of several ideal models, and making a judgement as to which model provides the best fit to the data. Although this analysis may provide fairly conclusive results, a large degree of uncertainty often exists. The degree of transparency, as a directly-measured quantity, does not exhibit such ambiguity.

Optical bandgap characterization is accomplished by first measuring the optical absorption of the film and calculating the optical absorption coefficient

$$\alpha = \frac{1}{t} \ln \left[\frac{1}{1-A} \right], \tag{3.2}$$

as a function of photon energy

$$E_{ph} = h\nu, \tag{3.3}$$

where t is the film thickness, A is the optical absorption ($0 \leq A \leq 1$), h is the Planck constant, and ν is the photon frequency. The variation of α with photon energy near the bandgap energy is determined by the bandgap transition type. Note that Eq. 3.2 neglects reflection from film surfaces; however if reflection is independent of E_{ph} (as is often the case), no error is introduced into the bandgap analysis (although the calculated α values are not strictly accurate).

When the valence band maximum and conduction band minimum occur at the same location in k-space, the bandgap is said to be direct; if this is not the case, the bandgap is said to be indirect. In a direct bandgap material, the dominant mechanism responsible for photon absorption is the direct electronic transition, in which the energy of an absorbed photon excites an electron from the valence band into the conduction band with no change in crystal momentum ($\Delta k = 0$). Quantum mechanical selection rules determine the relative probability (as a function of k) that photon absorption mediated by an electronic transition from the valence band to the conduction band will take place. When the transition between valence band and conduction band is quantum mechanically allowed, this probability is not strongly dependent on k, and the electronic transition is said to be allowed. [101, 102] When the transition between valence band and conduction band is quantum mechanically forbidden, the probability of a direct transition is zero at the valence band maximum (conduction band minimum) and increases with k^2 moving away from this point; in this case, the electronic transition is said to be forbidden. [101, 102]

For an allowed transition between direct, parabolic bands the variation of α with photon energy for $h\nu > E_G$ is given by [101, 102, 103, 104]

$$\alpha \propto (h\nu - E_G)^{1/2}, \tag{3.4}$$

where E_G is the bandgap energy. This expression can be reorganized to yield the linear relationship

$$\alpha^2 \propto h\nu - E_G. \tag{3.5}$$

The analogous relationship corresponding to a forbidden transition between direct, parabolic bands is [101, 102, 103]

$$\alpha \propto (h\nu - E_G)^{3/2} \tag{3.6}$$

which can be reorganized to yield

$$\alpha^{2/3} \propto h\nu - E_G. \tag{3.7}$$

When the bandgap is indirect, optical absorption requires a change in crystal momentum accompanying the excitation of an electron from the valence band into the conduction band; a phonon (lattice vibration) must be absorbed or emitted simultaneously with photon absorption in order to satisfy momentum conservation. For an allowed transition between indirect, parabolic bands the variation of α with photon energy is given by [101, 102]

$$\alpha \propto \frac{(h\nu - (E_G - E_p))^2}{e^{\frac{E_p}{kT}} - 1} + \frac{(h\nu - (E_G + E_p))^2}{1 - e^{-\frac{E_p}{kT}}}, \tag{3.8}$$

where E_p is the energy of a phonon with momentum equal to the separation in k-space between the valence band maximum and the conduction band minimum and k is the Boltzmann constant (not the crystal momentum). The first term in Eq. 3.8 corresponds to phonon absorption, and is nonzero for $h\nu > E_G - E_p$; the second term corresponds to phonon emission, and is nonzero for $h\nu > E_G + E_p$. For low temperatures ($E_p \gg kT$) the denominator of the first term is large, so that the second term dominates the net absorption coefficient; in this case, the expression can be reorganized to yield

$$\alpha^{1/2} \propto h\nu - (E_G + E_p). \tag{3.9}$$

As the temperature increases, the contribution of the first term (phonon absorption) is no longer negligible. For high temperatures ($E_p \ll kT$) this term dominates the net absorption coefficient, and the overall expression can be reorganized to yield

$$\alpha^{1/2} \propto h\nu - (E_G - E_p). \tag{3.10}$$

The contribution of E_p in this analysis is often neglected, with the implicit assumption that $E_p \ll E_G$ (or, equivalently, with the acceptance of a $\pm E_p$ error window in the estimated value of E_G).

For a forbidden transition between indirect, parabolic bands the variation of α with photon energy is given by [101]

$$\alpha \propto \frac{(h\nu - (E_G - E_p))^3}{e^{\frac{E_p}{kT}} - 1} + \frac{(h\nu - (E_G + E_p))^3}{1 - e^{-\frac{E_p}{kT}}}, \tag{3.11}$$

where k is the Boltzmann constant (not the crystal momentum). Manipulation of this expression yields results analogous to those obtained in Eqs. 3.9 and 3.10,

$$\alpha^{1/3} \propto h\nu - (E_G + E_p) \tag{3.12}$$

for low temperatures such that phonon emission dominates, and

$$\alpha^{1/3} \propto h\nu - (E_G - E_p) \tag{3.13}$$

for high temperatures such that phonon absorption dominates.

The characterization of bandgap energy and transition type is accomplished by constructing plots of α^m as a function of photon energy, with m taking the values 2 (allowed direct transition), 2/3 (forbidden direct transition), 1/2 (allowed indirect transition), and 1/3 (forbidden indirect transition). The value of m producing a linear plot in the vicinity of the bandgap energy indicates the transition type, and the photon energy axis-intercept of this linear fit yields an estimate of the bandgap energy. In practice, however, there is often a large degree of ambiguity in the interpretation of such results.

Finally, note that optical absorption in materials where the bandgap is either forbidden direct, allowed indirect, or forbidden indirect may be quite small for energies below that of the smallest allowed direct transition. This is due to a combination of the energy dependence of the absorption coefficient and the relative values of the proportionality constants in Eqs. 3.4, 3.6, 3.8, and 3.11; the proportionality constant is significantly smaller for indirect and/or quantum mechanically forbidden transitions

than for allowed, direct transitions. Thus, as long as the smallest allowed direct transition is ~3 eV or larger, a material may exhibit sufficient transparency for use in transparent electronic device applications, even if the minimum bandgap (establishing electrical behavior) falls well within the visible region.

3.2.2 Conductivity, mobility, and carrier concentration

Basic electrical characterization of a semiconducting thin film consists of determining the conductivity, majority carrier type, mobility and carrier concentration. Conductivity is related to carrier mobility and concentration according to

$$\sigma = q(\mu_n n + \mu_p p), \tag{3.14}$$

where q is the electron charge, μ_n (μ_p) is the electron (hole) mobility and n (p) is the electron (hole) concentration per unit volume. In an n-type (p-type) semiconductor, the term corresponding to holes (electrons) is negligible, yielding the more familiar simplified form of the equation.

There are several methods commonly used to measure the conductivity of a thin film; these include the two-point and four-point probe methods [105] and the van der Pauw method. [105, 106, 107] The conductivity of a thin film is perhaps most easily measured by applying full width metal contacts at each end of a rectangular sample and directly measuring the resistance using an ohmmeter. The conductivity is then given by

$$\sigma = \frac{\ell}{Rtw}, \tag{3.15}$$

where R is the measured resistance, t is the film thickness, w is the film width, and ℓ is the film length (between the metal contacts). This measurement provides an accurate assessment of conductivity only if the contact resistance is negligible as compared to the sample resistance; this is often the case, as the contact area is many times larger than the film cross-sectional area, so that the contact resistance per unit area may be relatively large without interfering with measurement accuracy. The contacts can

be easily evaluated by preparing two identical samples with different length-to-width ratios; if the measured resistance is proportional to the length-to-width ratio, the contact resistance is indeed negligible.

Majority carrier type can be determined using the thermoelectric probe method. [105] Adjacent hot and cold probes are placed in direct contact to the sample with a voltmeter (or ammeter) connected between the probes. The hot probe may be as simple as a soldering iron, with an unheated probe serving as the cold probe. Thermal energy supplied by the hot probe locally enhances majority carrier diffusion, yielding a net majority carrier diffusion current away from the vicinity of the hot probe. Space charge accumulates until the resulting electric field is sufficient to balance the thermally activated diffusion current. This produces a potential between the probes that is measured by the voltmeter. In the case of an n-type (p-type) sample, a deficit of electrons (holes) near the hot probe leaves a net positive (negative) space charge so that the hot probe is at a positive (negative) potential relative to the cold probe.

The most commonly used method for determining mobility, carrier concentration, and majority carrier type is the Hall method. As this measurement is described in detail in a number of references [104, 105], a brief description only will be given here. The Hall effect arises as a consequence of the Lorentz force exerted by a magnetic field on a moving charged particle,

$$\vec{F_L} = q\vec{v}\times\vec{B}, \tag{3.16}$$

where q is the charge on the particle, $\vec{v}$ is the particle velocity, $\vec{B}$ is the magnetic field, and $\times$ denotes the vector cross product. The basic Hall measurement is accomplished by passing a current between two contacts on a sample; a magnetic field perpendicular to the sample plane deflects charge carriers (electrons or holes) toward the sample edges. The resulting space charge generates a voltage across the sample, perpendicular to the direction of current flow; this is referred to as the Hall voltage.

The sign and magnitude of the Hall voltage are used to calculate the majority carrier type, mobility, and concentration.

The Hall mobility, μ_H, resulting from the simple Hall theory is not in general equal to the conductivity mobility, μ; this error can be accounted for by two multiplicative factors [104, 105], yielding the expression

$$\mu_H = KM\mu, \tag{3.17}$$

where

$$K = \frac{\langle \tau^2 \rangle}{\langle \tau \rangle^2} \tag{3.18}$$

is a correction for the assumption of energy-independent carrier scattering (τ is the mean time between carrier collisions) and M is a correction for the assumption of isotropic effective mass. K is typically between one and two; M is typically slightly less than one.

The van der Pauw Hall method is a particularly useful technique, as it can be used to measure the Hall effect in a sample of arbitrary geometry. [105, 106, 107] Sample preparation consists of placing four contacts at arbitrary locations along the sample edge. Contacts are assumed to be infinitely small and located exactly at the sample edge; corrections can be made to the van der Pauw equations if these conditions are not met. [106, 107, 108] Although the van der Pauw method can theoretically be used to characterize a film of arbitrary geometry, in practice a high degree of symmetry is necessary to characterize low mobility materials. The Hall voltage is given by [105, 106, 107]

$$V_H = \frac{\mu_H B I \rho}{t} = \frac{BI}{qtn}, \tag{3.19}$$

where μ_H is the Hall mobility, B is the magnetic field strength, I is the measurement current, ρ is the film resistivity, t is the film thickness, q is the electron charge, and n is the majority carrier concentration. In an asymmetric sample the Hall voltage is superimposed upon a large offset voltage resulting from sample asymmetry, thus requiring the evaluation of a slight change (the Hall voltage) in a large voltage signal

(the asymmetry offset voltage). Since the Hall voltage is proportional to mobility, this problem becomes worse as mobility decreases. Sample preparation is, therefore, critical in obtaining Hall mobility for low mobility films. The use of shadow masks to pattern Hall sample films with a cloverleaf or cross pattern [105] is a practical method for improving the minimum measurable Hall mobility; such an approach is used to measure a mobility of ~3.5 cm^2/V s in $BaCu_2S_2$. [23] The practical minimum mobility measurable with the Hall technique is ~1 cm^2/V s.

3.2.3 Kelvin probe measurement of work function

The Kelvin probe technique can be used to evaluate the work function (ϕ = E_{vac} - E_F) of a metal or semiconductor. [109] The measurement setup consists of a metal probe electrode (e.g. Pt, Au) in close physical proximity to the test surface. The reference electrode is attached to a mechanical or piezoelectric assembly in order to allow periodic oscillation (normal to the test surface) of the reference electrode/test surface separation distance, d_{gap}. Since the reference electrode/test surface capacitance is inversely proportional to the separation distance (d_{gap}), this oscillation yields a corresponding time-varying capacitance. The reference electrode and the test surface are electrically connected through a DC bias source (V_{bias}) and a current amplifier, as shown in Fig. 3.1. The time-varying capacitance c(t) induces a current

$$i(t) = V_C^{eff} \frac{d}{dt} c(t), \tag{3.20}$$

where V_C^{eff} is the effective capacitor voltage, given by

$$V_C^{eff} = (V_{probe} - V_{sample})^{eff} = V_{bias} - V_{CPD}, \tag{3.21}$$

and V_{CPD}, the contact potential difference, is defined as

$$qV_{CPD} = \phi_{probe} - \phi_{sample}, \tag{3.22}$$

where q is the electron charge.

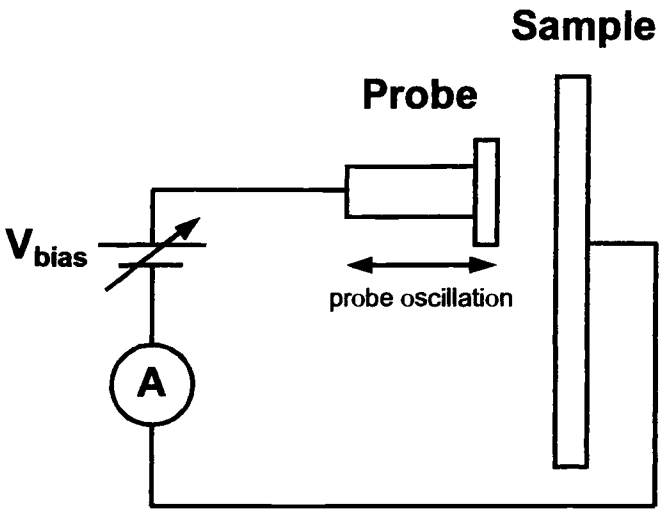

Figure 3.1: Kelvin probe measurement setup.

In the simplest analysis of the Kelvin probe measurement, both the probe electrode and the sample are metals with ideal (chemically pure, clean, and charge free) surfaces. With zero bias applied between the reference electrode and test surface, DC equilibrium prevails and the Fermi levels are aligned. However, since the sample work function is not in general the same as that of the probe, an electric field is induced in the gap with concomitant formation of space charge layers at the probe and sample surfaces. The surface charge density is modulated by the oscillating electrode separation, producing a current, i(t), that is measured in the external circuit. Figure 3.2 portrays an energy band diagram corresponding to this situation.

V_{CPD} is evaluated by varying V_{bias} until the measured current, i(t), is equal to zero. This occurs when V_{bias} is exactly equal to V_{CPD}, so that the local vacuum level E^{ℓ}_{vac} is constant across the gap and the gap field and probe/sample surface charge is identically zero. Variation in the probe/sample separation does not require modulation of surface charge density, so that no current flows in the external circuit.

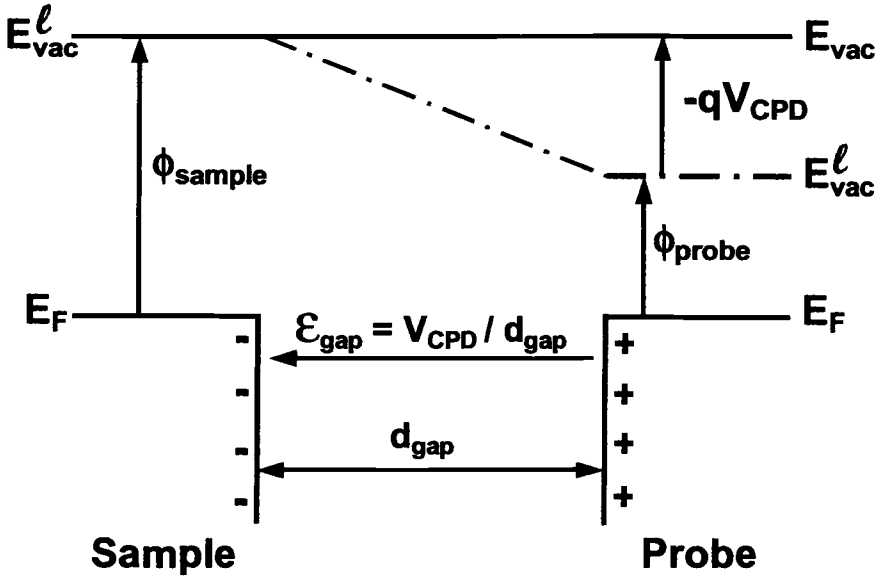

Figure 3.2: Kelvin probe measurement energy band diagram with metal probe and sample, ideal surfaces, and zero external bias. E^{ℓ}_{vac} and q denote the local vacuum level and the electron charge, respectively.

Using this value for V_{CPD} and the known value of ϕ_{probe}, Eq. 3.22 directly yields the work function of the sample material, ϕ_{sample}.

The ideal analysis presented above does not, in general, provide an accurate evaluation of the work function of a metal sample. This is a result of deviation from the assumption of ideal surfaces; such deviations generally take the form of a charged surface insulating layer and/or a surface dipole. Unless sample preparation and the subsequent Kelvin probe measurement are performed under vacuum, avoiding exposure to atmosphere and other potential contaminants, some degree of surface modification is essentially unavoidable.

The error introduced by a charged surface insulating layer is most easily evaluated by inspecting the energy band diagram when V_{bias} has been adjusted so as to nullify the measured current, i(t), requiring that the electric field in the gap be

exactly zero. This is depicted in Fig. 3.3, where both the sample surface and the probe surface are covered by insulating layers with charged surfaces.

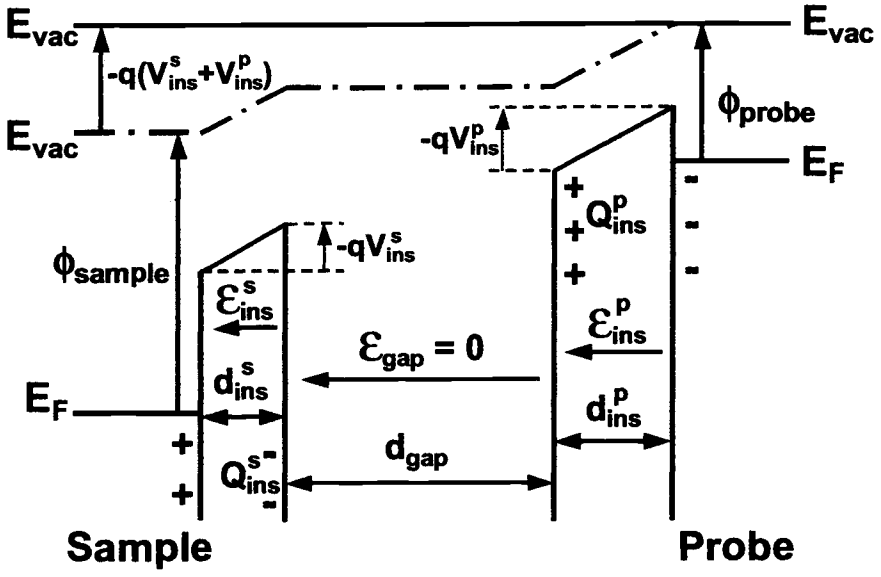

Figure 3.3: Kelvin probe measurement energy band diagram with metal probe and sample, charged surface insulating layers, and external bias adjusted so as to nullify i(t). E^{ℓ}_{vac} and q denote the local vacuum level and the electron charge, respectively.

When the gap field is zero, the probe (sample) insulator surface charge is exactly matched by charge at the probe (sample) metal / insulator interface. The voltage dropped across the probe insulator layer is

$$V^p_{ins} = -\frac{Q^p_{ins} d^p_{ins}}{\epsilon^p_{ins}}, \tag{3.23}$$

and the voltage dropped across the sample insulator layer is

$$V^s_{ins} = \frac{Q^s_{ins} d^s_{ins}}{\epsilon^s_{ins}}, \tag{3.24}$$

where Q^p_{ins} (Q^s_{ins}) is the probe (sample) insulator surface charge, d^p_{ins} (d^s_{ins}) is the probe (sample) insulator thickness, and ϵ^p_{ins} (ϵ^s_{ins}) is the dielectric constant of the

probe (sample) insulator (note that the voltage polarity convention used here assigns a positive voltage to the node nearest the probe and a negative voltage to the node nearest the sample). The external bias (when i(t) has been nullified) is now given by

$$qV_{bias} = (\phi_{probe} - \phi_{sample}) + q(V^p_{ins} + V^s_{ins}), \tag{3.25}$$

and the apparent sample work function, ϕ^{app}_{sample}, is related to the true sample work function, ϕ_{sample}, as

$$\phi^{app}_{sample} = \phi_{sample} - q(V^p_{ins} + V^s_{ins}). \tag{3.26}$$

An electronic dipole at either the sample or the probe surface (or at the surface of a sample or probe insulating layer) has an effect similar to that of a charged surface insulating layer. If the situation depicted in Fig. 3.3 is extended to include a dipole at both the probe and sample surfaces, the apparent sample work function is given by

$$\phi^{app}_{sample} = \phi_{sample} - q(V^p_{ins} + V^s_{ins}) - q(V^p_{dipole} + V^s_{dipole}), \tag{3.27}$$

where V^p_{dipole} and V^s_{dipole} are the probe and sample surface dipoles, respectively (a positive V_{dipole} is such that the voltage decreases in moving across the dipole from the probe toward the sample).

Kelvin probe analysis of a semiconducting test surface proceeds similarly to that appropriate for a metal test surface, with a few notable differences. First, an exposed semiconductor surface is typically depleted, so that the surface work function is not the same as that of the bulk. Second, if a charged surface insulating layer is present, charge compensation in the semiconductor requires modulation of the semiconductor space charge region width; the resulting voltage is divided between the insulator and the semiconductor depletion region, so that the resulting offset error is dependent on semiconductor doping and dielectric constant (whereas in a metal the offset error is determined solely by the characteristics of the insulator).

The error resulting from a semiconductor surface depletion region can be greatly reduced by illumination with light of sufficient energy to create electron-hole pairs

in the semiconductor. If the illumination intensity is sufficiently large, surface band bending is eliminated so that the Kelvin probe analysis is similar to that appropriate for a metal test surface.

Table 3.1 lists the calculated voltage error magnitude introduced by a charged insulator on either the probe or sample surface (Eqs. 3.23 and 3.24), with a dielectric constant $\epsilon = 10\ \epsilon_0$. Clearly, the error introduced by insulator charging can be significant. However, it would appear that the Kelvin probe measurement of work function is not necessarily rendered impractical by such effects, particularly if care is taken to minimize contamination of the sample surface.

Table 3.1: Kelvin probe measurement calculated offset voltage error due to a charged insulating layer with thickness d_{ins} and surface charge Q_S on the probe or sample surface. A typical dielectric constant $\epsilon = 10\ \epsilon_0$ is assumed.

Q_S (cm^{-2})	d_{ins} (nm)	V_{error} (V)
10^{11}	1	0.0018
10^{11}	10	0.018
10^{12}	1	0.018
10^{12}	10	0.18
10^{13}	1	0.18
10^{13}	10	1.8

Kelvin probe measurements were performed at Mitsubishi Silicon America, Salem, OR (using a FAaST 330 Epi-τ AC SPV system) in order to evaluate the work functions of several p-type transparent conductive oxides ($CuYO_2$:Ca, $CuScO_2$:Mg, and $CuCrO_2$). The $CuYO_2$:Ca, $CuScO_2$:Mg, and $CuCrO_2$ layers are deposited on a

p^+-Si wafer; Au, Cu, Al, and ZnO:Al are deposited on an n^+-Si wafer as reference materials for calibration of the measurement. The probe electrode is Pt ($\phi_{Pt} \approx 5.7$ eV [57]). Table 3.2 lists experimental results. Only V_{CPD}^{light} (the measured contact potential difference with illumination) is tabulated, as the light sensitivity is quite small (i.e. $\lesssim$0.05 eV for all materials but n-Si). The rather large uncertainties in the measured values of V_{CPD}^{light} are due to the data output format (data output is available only in the form of color-coded surface contour plots; the raw numerical data is not available).

The results listed in Table 3.2 may appear somewhat ambiguous. However, note that these films were exposed to atmosphere for an extended period of time between deposition and Kelvin probe measurement, so that some degree of surface oxidation and contamination certainly occurred. The last column (ϕ_{meas} - 0.5 eV) in Table 3.2 lists work function values corrected for an apparent systematic offset error, presumably due to contamination of the Pt probe surface. Although this correction is somewhat arbitrary, note that it yields the expected work functions for Au and ZnO:Al; both Au and ZnO should be fairly insensitive to surface modification due to exposure to atmosphere, whereas the Si, Al, and Cu surfaces are more prone to oxidation. Even the corrected values for Si, Al, and Cu are fairly reasonable (within ~0.5 eV of the expected values). Thus the work function estimates given in the final column of Table 3.2 for $CuYO_2$:Ca, $CuScO_2$:Mg, and $CuCrO_2$ appear to be reasonable. Also note that, as oxides, these materials should be relatively insensitive to surface modification due to atmospheric exposure. The result for $CuYO_2$ (5.3 eV $< \phi <$ 5.8 eV) can be compared to that obtained by Benko and Koffyberg, who used photoelectrochemical measurements to estimate the $CuYO_2$ valence band location to be 5.3 $\pm$ 0.2 eV below the vacuum level. [110]

Table 3.2: Results of Kelvin probe work function measurements at Mitsubishi Silicon America. The measured work function ϕ_{meas} is given by ϕ_{Pt} - qV_{CPD}. Values with uncertainty greater than 0.1 eV are represented as min / max. The (ϕ_{meas} - 0.5 eV) column entry is an estimate of the true work function, corrected for an apparent Pt probe contamination offset.

Material	V_{CPD}^{light} (V)	ϕ_{meas} (eV)	$\phi_{expected}$ (eV)	ϕ_{meas} - 0.5 eV (eV)
Au	0 / 0.1	5.6 / 5.7	5.2 [57]	5.1 / 5.2
Cu	0.1 / 0.3	5.4 / 5.6	4.7 [57]	4.9 / 5.1
Al	1.3 / 1.7	4 / 4.4	4.3 [57]	3.5 / 3.9
ZnO:Al	0.1 / 0.3	5.4 / 5.6	4.5 / 5.2 (Section 2.2.1)	4.9 / 5.1
n^+-Si	0.3 / 0.8	4.9 / 5.4	4.0 [57]	4.4 / 4.9
p^+-Si	-0.1 / 0.3	5.4 / 5.8	5.1 [57]	4.9 / 5.3
$CuYO_2$:Ca (sputtered)	-0.4 / -0.1	5.8 / 6.2		5.3 / 5.8
$CuYO_2$:Ca (evaporated)	-0.4 / -0.1	5.8 / 6.2		5.3 / 5.8
$CuScO_2$:Mg	-0.1 / 0.3	5.4 / 5.8		4.9 / 5.3
$CuCrO_2$	-0.1 / 0.3	5.4 / 5.8		4.9 / 5.3

3.3 Device characterization

The basic electrical characterization process for a transparent electronic device proceeds in a manner similar to that appropriate for the analogous non-transparent device. Optical characterization at the device level typically consists of a transparency measurement as described in Section 3.2.1 for individual thin films.

3.3.1 DC current-voltage and AC impedance measurements

Electrical characterization of an arbitrary two-terminal electronic device consists of a DC current-voltage measurement and a set of AC impedance-(voltage, frequency) measurements. DC characterization of a three-terminal device requires a set of current-voltage measurements; the AC characteristics of a three-terminal device are often most easily determined by characterizing an appropriate two-terminal test structure (for example, characterization of a MOS capacitor yields information regarding the corresponding MOSFET).

DC current-voltage measurement results given in this thesis are obtained using an HP 4140B picoammeter with two integrated voltage sources (-100 V $\leq V_{source} \leq$ 100 V, $|I_{source}| <$ 10 mA). AC impedance measurements employ an HP 4192A LF impedance analyzer (5 Hz $\leq$ f $\leq$ 13 MHz, -35 V $\leq V_{bias} \leq$ 35 V). Visual Basic is used to automate data collection.

3.3.2 Thin film transistor mobility and threshold voltage extraction

A thin film transistor (TFT) is essentially a thin film version of a MOSFET, the primary difference being that the TFT is fabricated on an insulating substrate and employs a thin film as the channel region while the MOSFET is fabricated on a single crystal semiconducting substrate that also serves as the channel. [57, 111] The ideal TFT drain current characteristics are identical to those of the MOSFET, with

the drain current given by [111]

$$I_D = \mu C_{ins} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{{V_{DS}}^2}{2} \right], \; V_{DS} \leq V_{GS} - V_T \tag{3.28}$$

and

$$I_D = \frac{1}{2} \mu C_{ins} \frac{W}{L} (V_{GS} - V_T)^2, \; V_{DS} \geq V_{GS} - V_T, \tag{3.29}$$

where μ is the channel mobility, C_{ins} is the gate insulator capacitance, W is the gate width, L is the gate length, V_{GS} is the gate-to-source voltage, V_T is the threshold voltage, and V_{DS} is the drain-to-source voltage. The channel mobility is the average mobility of carriers in the channel layer when the TFT is turned on through the application of an appropriate gate voltage. Since carriers drawn into the channel layer by the gate voltage are localized in a narrow accumulation region in the channel layer at the channel layer / gate insulator interface, the TFT channel mobility is generally lower than the channel layer bulk mobility due to additional scattering mechanisms at the interface (e.g. interface defect scattering and surface roughness scattering).

In order to characterize a TFT according to the ideal model, estimates of the channel mobility and threshold voltage must be extracted from experimental drain current measurements. There are three ways in which this can be accomplished. [105]

The first two methods rely upon measurement of I_D as a function of V_{GS} for a fixed V_{DS} such that the device operates in the linear region ($V_{DS} \ll V_{GS}$ - V_T), so that the drain current can be approximated as

$$I_D \approx \mu C_{ins} \frac{W}{L} (V_{GS} - V_T) V_{DS}. \tag{3.30}$$

The mobility and threshold voltage can be estimated from this expression using either the linear region drain conductance

$$g_d \equiv \frac{dI_D}{dV_{DS}}\Big|_{V_{GS}=constant} = \mu C_{ins} \frac{W}{L} (V_{GS} - V_T) \tag{3.31}$$

or the linear region transconductance

$$g_m \equiv \frac{dI_D}{dV_{GS}}\Big|_{V_{DS}=constant} = \mu C_{ins} \frac{W}{L} V_{DS}. \tag{3.32}$$

The mobility estimated from the linear region drain conductance is referred to as the effective mobility, μ_{eff}. [105] The effective mobility and the threshold voltage may be estimated graphically by plotting the linear region drain conductance as a function of V_{GS}. For V_{GS} - $V_T \gg V_{DS}$ this plot should become linear; the slope yields the effective mobility

$$\mu_{eff} = \frac{slope}{C_{ins}\frac{W}{L}}, \tag{3.33}$$

and the x-intercept approximates the threshold voltage V_T. Equivalently, μ_{eff} and V_T can be calculated numerically from the linear region drain conductance as

$$\mu_{eff} = \frac{\frac{dg_d}{dV_{GS}}}{C_{ins}\frac{W}{L}} \tag{3.34}$$

and

$$V_T = V_{GS} - \frac{I_D}{\mu_{eff}C_{ins}\frac{W}{L}V_{DS}}. \tag{3.35}$$

The resulting estimates are valid for gate voltages V_{GS} - $V_T \gg V_{DS}$ such that the assumption of linear region operation is satisfied.

The mobility estimated from the linear region transconductance is referred to as the field-effect mobility, μ_{FE}. [105] The field-effect mobility and threshold voltage are calculated numerically from the linear region transconductance as

$$\mu_{FE} = \frac{g_m}{C_{ins}\frac{W}{L}V_{DS}} \tag{3.36}$$

and

$$V_T = V_{GS} - \frac{I_D}{\mu_{eff}C_{ins}\frac{W}{L}V_{DS}}, \tag{3.37}$$

with results valid for V_{GS} - $V_T \gg V_{DS}$ such that the assumption of linear region operation is satisfied.

The third method for estimating mobility and threshold voltage relies on measurement of I_D as a function of V_{GS} with $V_{DS} > V_{GS}$ - V_T; the resulting mobility is referred to as the saturation mobility, μ_{sat}. [105] The device operates in the saturation region, with the saturation drain current $I_{D,sat}$ given by Eq. 3.29. The saturation

mobility and the threshold voltage may be estimated graphically by plotting $\sqrt{I_{D,sat}}$ as a function of V_{GS}. For $V_{GS} > V_T$ this plot should become linear; the slope yields the saturation mobility

$$\mu_{sat} = \frac{slope^2}{\frac{1}{2}C_{ins}\frac{W}{L}}, \tag{3.38}$$

and the x-intercept approximates the threshold voltage V_T. Equivalently, μ_{sat} and V_T can be calculated numerically from $I_{D,sat}$ as

$$\mu_{sat} = \frac{\left(\frac{d\sqrt{I_{D,sat}}}{dV_{GS}}\right)^2}{\frac{1}{2}C_{ins}\frac{W}{L}} \tag{3.39}$$

and

$$V_T = V_{GS} - \sqrt{\frac{I_{D,sat}}{\frac{1}{2}C_{ins}\frac{W}{L}}}, \tag{3.40}$$

with results valid for $V_{GS} > V_T$ such that the assumption of saturation region operation is satisfied.

Figure 3.4 shows the experimentally extracted effective mobility (μ_{eff}) and saturation mobility (μ_{sat}) along with the corresponding threshold voltage (V_T) estimates for a transparent ZnO-based TFT described in Chapter 5 (with current-voltage characteristics portrayed in Figs. 5.5 and 5.6).

As expected [105], the estimated saturation mobility, μ_{sat}, is smaller than the estimated effective mobility, μ_{eff} (this discrepancy arises due to the fact that the gate voltage dependence of the mobility is neglected in estimating μ_{sat} using Eqs. 3.38 and 3.39). Although μ_{eff} generally yields a better estimate of the true channel mobility [105], μ_{sat} gives an estimate of the channel mobility based on an independent data set and a different set of assumptions; a reasonable degree of agreement between the two estimates (μ_{eff} and μ_{sat}), as seen in Fig. 3.4, provides support for the validity of this analysis. Although the mobility and threshold voltage estimates do not become independent of V_{GS} as expected for a TFT following the ideal model (Eqs. 3.28 and 3.29), they appear to be leveling off near the maximum applied gate voltage of 40 V. Although the mobility and threshold voltage cannot be precisely estimated from this

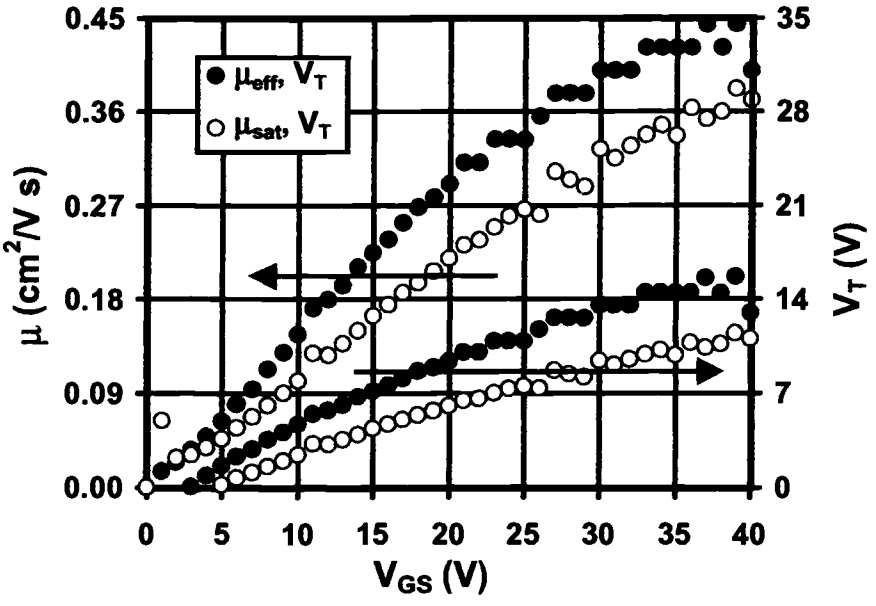

Figure 3.4: Experimentally extracted effective mobility, μ_{eff} ($I_D(V_{GS})$ measured with V_{DS} = 1 V), and saturation mobility, μ_{sat} ($I_D(V_{GS})$ measured with $V_{DS} = V_{GS}$), along with the corresponding threshold voltage estimates, V_T, for a transparent TFT (Chapter 5). A 10 second settling delay is allowed at each point before taking a current measurement.

analysis, they can be confidently placed within some reasonable range; the results depicted in Fig. 3.4 indicate a mobility and threshold voltage of 0.35 to 0.45 cm^2/V s and 10 to 15 V, respectively.

3.3.3 C-(V,f) characterization of carrier injection and interface channel formation

This subsection describes a novel technique, the capacitance-(voltage, frequency) [C-(V,f)] method, for simultaneously characterizing carrier injection into an insulator (i.e. an insulating wide bandgap semiconductor) and mobile carrier accumulation (i.e. interface channel formation) at an insulating semiconductor (e.g. TFT channel) / wide bandgap insulator (e.g. TFT gate insulator) interface. C-(V,f) characterization relies upon acquiring AC capacitance measurements over a wide range of DC

bias voltages and measurement frequencies. As this method was conceived late in the process of completing this thesis research, its capabilities and limitations as a characterization technique for an arbitrary material system have not yet been thoroughly evaluated. However, C-(V,f) analysis of the transparent TFT structure presented in Section 5.2.3 indicates that this technique can indeed provide a great deal of information. Since TFT C-(V,f) characterization results are presented in Section 5.2.3, the discussion here is limited to a general description of the test structure, the characterization process, and analysis and interpretation of results. Before proceeding it should be pointed out that, although the discussion presented here assumes that the layer into which injection occurs is substantially insulating, this is not meant to imply that the measurement cannot provide valuable information if this assumption is not satisfied.

Figure 3.5 illustrates the C-(V,f) technique test structure. The injecting top contact layer (hereafter referred to as the injector) is selectively deposited upon isolated regions of the insulating semiconductor layer (hereafter referred to as the semiconductor); the area of the injector region, A_{inj}, is smaller than the area of the insulating semiconductor region, A_{sc}, by a factor of $\sim$2 or more. The substrate is coated with a conducting layer (hereafter referred to as the substrate conductor) and a wide bandgap insulator (hereafter referred to as the insulator).

The C-(V,f) test structure portrayed in Fig. 3.5 exhibits a maximum of three distinct measured capacitance plateaus as the DC bias and the AC measurement frequency are varied. These capacitance plateaus are denoted C_{ins}^{sc}, C_{ins}^{inj}, and $C_{sc,ins}^{inj}$. Figure 3.6 shows a C-(V,f) contour plot where these three capacitance plateaus are clearly visible at $\sim$7.8, 3.5, and 2.3 nF for C_{ins}^{sc}, C_{ins}^{inj}, and $C_{sc,ins}^{inj}$, respectively. Fabrication details and further discussion of Fig. 3.6 are provided in Section 5.2.3.

The maximum capacitance plateau that may be observed in a C-(V,f) measurement is denoted C_{ins}^{sc} and is observed in Fig. 3.6 under forward bias at low AC measurement frequency. Examination of the energy band diagram depicted in Fig.

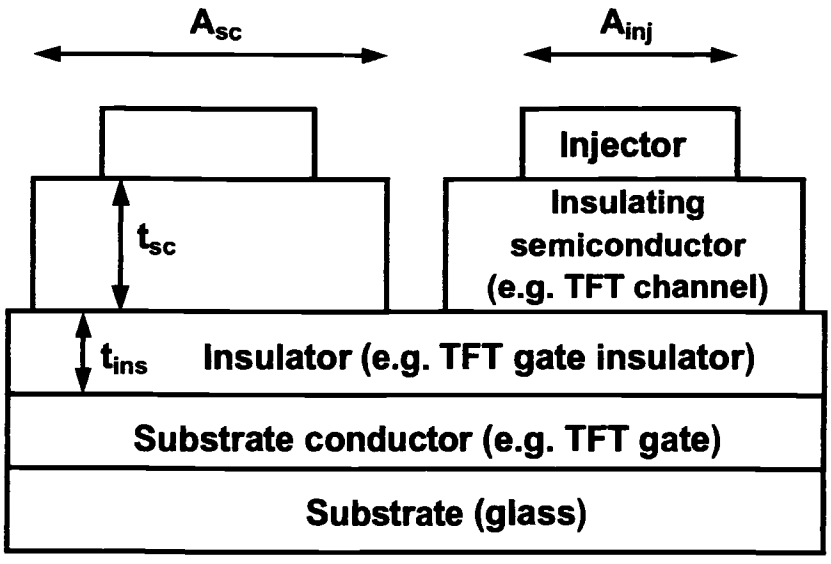

Figure 3.5: C-(V,f) characterization technique test structure. A_{sc} and A_{inj} refer to the areas of the semiconductor and injector regions, respectively.

3.7 facilitates an understanding of the origin of C_{ins}^{sc}. As indicated in Fig. 3.7, if the injector / semiconductor interface provides efficient electron injection into the insulating semiconductor layer (as discussed in Section 2.3.4), the applied DC forward bias voltage (negative voltage to the electron injector) is dropped entirely across the insulator layer, supported by negative (positive) space charge at the semiconductor / insulator (substrate conductor / insulator) interface. Efficient electron injection, within this context, implies that a non-negligible electron flux flows from the injector into the semiconductor under forward bias; the band alignment, interface dipole, and/or interface charge combine to yield a relatively small energy barrier to electron injection. Thus, under forward bias and for a sufficiently low AC measurement signal frequency, the semiconductor / insulator interface charge is able to respond to the measurement signal, and the measured capacitance is that of the insulator layer with

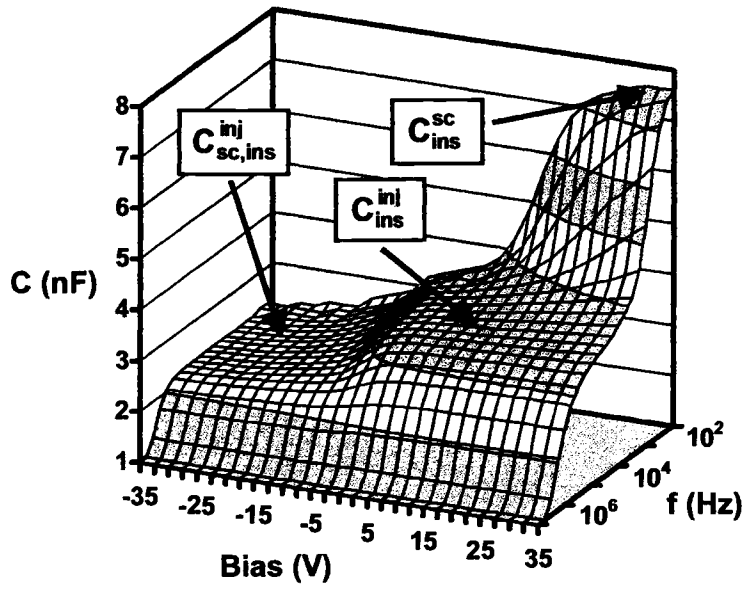

Figure 3.6: C-(V,f) contour plot of capacitance as a function of bias voltage (-35 to 35 V) and measurement frequency (100 Hz to 10 MHz), using the C-(V,f) test structure depicted in Fig. 3.5. The injector, semiconductor, insulator, and bottom conductor layers are ITO (300 nm, 0.08 cm^2), ZnO (100 nm, 0.18 cm^2), ATO (220 nm), and ITO (200 nm), respectively.

an area equal to that of the semiconductor region,

$$C^{sc}_{ins} = \frac{\epsilon_{ins} A_{sc}}{t_{ins}}, \tag{3.41}$$

where ϵ_{ins} and t_{ins} are the insulator layer dielectric constant and thickness, respectively. Figure 3.8a illustrates the physical location at which AC charge modulation corresponding to C^{sc}_{ins} occurs.

The intermediate capacitance plateau that may be observed in a C-(V,f) measurement is denoted C^{inj}_{ins} and is evident in Fig. 3.6 throughout the forward bias portion of the C-(V,f) plot, except for the portion occupied by the C^{sc}_{ins} plateau and the sloped face defining the transition between C^{inj}_{ins} and C^{sc}_{ins}. Figure 3.8b illustrates the physical location at which AC charge modulation corresponding to C^{inj}_{ins} occurs. The mechanism responsible for the transition from C^{sc}_{ins} to C^{inj}_{ins} will be elaborated

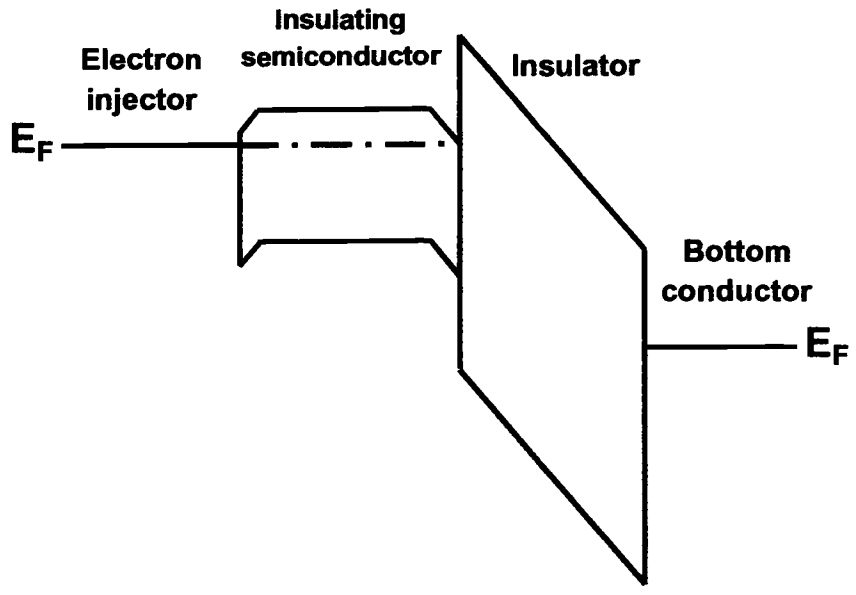

Figure 3.7: Forward bias energy band diagram through the injector / semiconductor / insulator / substrate conductor region of the C-(V,f) test structure, where the injector is an electron injector so that forward bias implies a negative voltage to the injector.

momentarily. The magnitude of C_{ins}^{inj},

$$C_{ins}^{inj} = \frac{\epsilon_{ins} A_{inj}}{t_{ins}}, \tag{3.42}$$

is related to the value of C_{ins}^{sc} precisely by the ratio of their effective areas, A_{sc} and A_{inj}.

The minimum capacitance plateau that may be observed in a C-(V,f) measurement is denoted $C_{sc,ins}^{inj}$ and is observed throughout the majority of the reverse bias portion of the C-(V,f) plot in Fig. 3.6, as shown. Figure 3.8c illustrates the physical location at which AC charge modulation corresponding to $C_{sc,ins}^{inj}$ occurs. The value of $C_{sc,ins}^{inj}$,

$$C_{sc,ins}^{inj} = [(C_{sc}^{inj})^{-1} + (C_{ins}^{inj})^{-1}]^{-1} = \frac{\epsilon_{sc}\epsilon_{ins} A_{inj}}{\epsilon_{ins} t_{sc} + \epsilon_{sc} t_{ins}}. \tag{3.43}$$

is a series combination of the insulator layer and the semiconductor layer with an area defined by the injector region.

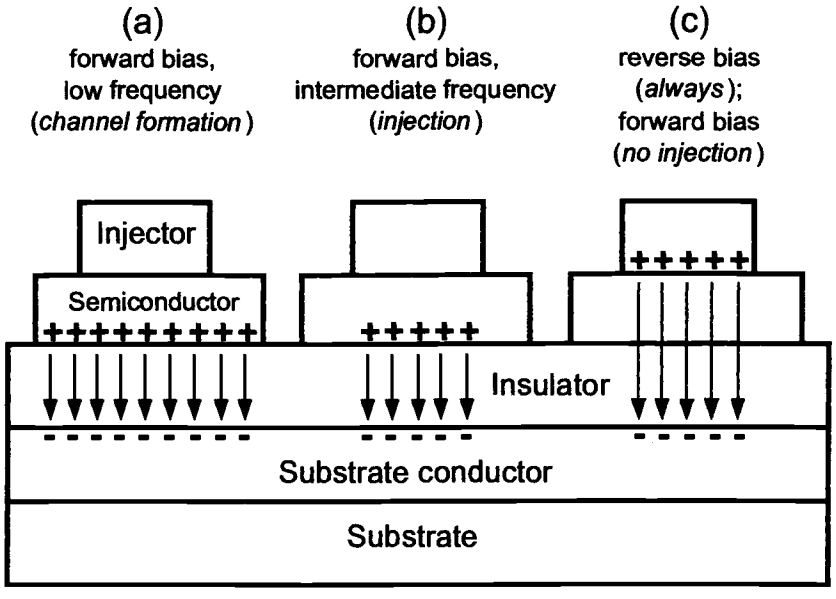

Figure 3.8: The physical location at which AC charge modulation occurs for each capacitance level observed in the C-(V,f) measurement (Note: The AC modulated charge distribution is not in general the same as that of the corresponding DC space charge).

Figure 3.9 depicts the relevant small-signal circuit elements associated with each of the three possible C-(V,f) capacitance plateaus. For each capacitance plateau, one (or more) parasitic resistance acts to establish an effective RC time constant, with the result that, above a frequency equal to the inverse of the RC time constant, the parasitic resistance inhibits charging and discharging of the capacitor by the AC measurement signal and the capacitance is no longer detected.

Before proceeding further, several comments regarding notation employed in Fig. 3.9 are in order. First, broken capacitor plates in Figs. 3.9a and 3.9c indicate portions of the effective capacitance that are charged and discharged through different current paths, as indicated, so that one physical segment of the capacitor may experience frequency-induced roll off sooner than another. Second, although R_{sc}^{lat} (Fig. 3.9a), R_{chan} (Fig. 3.9a), and R_{inj}^{lat} (Fig. 3.9c) are portrayed as discrete resis-

tors for simplicity, a more accurate model would replace these discrete elements with distributed RC networks.

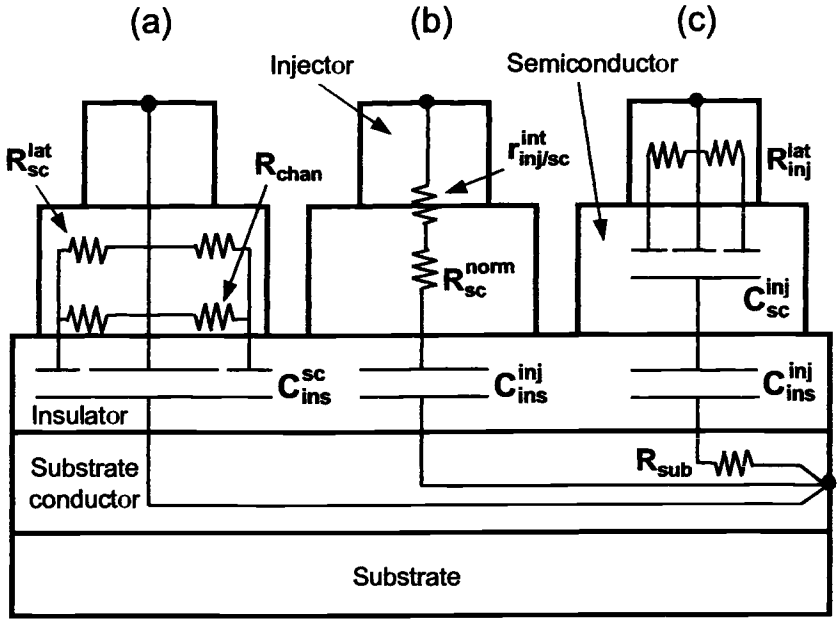

Figure 3.9: Parasitic resistances responsible for roll off in measured capacitance at each capacitance plateau observed in the C-(V,f) measurement. Broken capacitor plates in (a) and (c) indicate portions of the effective capacitance that are charged and discharged through different current paths, as indicated, so that one physical segment of the capacitor may experience frequency-induced roll off sooner than another.

At the maximum capacitance plateau, C_{ins}^{sc}, as portrayed in Fig. 3.9a, the relevant parasitic resistance is that which effects lateral current flow through the semiconductor layer from the region covered by the injector layer to the peripheral (exposed) region. This resistance is a parallel combination of the bulk semiconductor layer lateral resistance, R_{sc}^{lat}, and the resistance of the accumulated negative charge (the channel) at the semiconductor / insulator interface, R_{chan}. If the semiconductor is sufficiently insulating (so that R_{sc}^{lat} is large enough to be neglected), the interface channel resistance determines the effective resistance of this current path. Above some

measurement signal frequency (for a given forward bias) lateral AC current flow is suppressed by this resistance, so that AC charge modulation at the semiconductor / insulator interface occurs only in the area defined by the injector region, as shown in Fig. 3.8b; hence, the measured capacitance decreases to C_{ins}^{inj}.

At the intermediate capacitance plateau, C_{ins}^{inj}, as portrayed in Fig. 3.9b, the relevant parasitic resistance is a series combination of the injector / semiconductor interface small-signal resistance, $r_{inj/sc}^{int}$, and the semiconductor layer resistance normal to the plane of the structure, R_{sc}^{norm}. Above a frequency established by the applicable RC time constant (i.e. $R = r_{inj/sc}^{int} + R_{sc}^{norm}$ and $C = C_{ins}^{inj}$), the parasitic resistance inhibits AC current flow to and from the semiconductor / insulator interface, so that AC charge modulation occurs at the injector / semiconductor interface, as shown in Fig. 3.8c; thus, the measured capacitance decreases to $C_{sc,ins}^{inj}$. This minimum capacitance plateau at $C_{sc,ins}^{inj}$ extends throughout the reverse bias portion of the C-(V,f) plot. Note that the bias-induced transition from C_{ins}^{inj} to $C_{sc,ins}^{inj}$ corresponds to depletion of the semiconductor layer.

At the minimum capacitance plateau, $C_{sc,ins}^{inj}$, as portrayed in Fig. 3.9c, two independent parasitic resistances act to induce the final high frequency roll off in measured capacitance. The first, R_{inj}^{lat}, is the resistance seen by lateral current flow through the injector layer from the physical contact (which can typically be treated as a point contact) throughout the injector region. The second, R_{sub}, is the resistance of the substrate conductor. R_{sub} combines with $C_{sc,ins}^{inj}$ to yield a straightforward RC time constant, defining a frequency above which typical RC roll off occurs. On the other hand, since R_{inj}^{lat} is inherently a distributed resistance, its inhibition of lateral current flow acts to incrementally reduce the effective area of the capacitor above a certain frequency. In either case, however, this effective time constant establishes the maximum useful frequency for an arbitrary device structure (as witnessed by the high frequency roll off seen in Fig. 3.6).

Thus, carrier injection into the semiconductor is verified by the existence of a forward bias capacitance plateau with a measured capacitance equal to C_{ins}^{inj} (Eq. 3.42). If injection is attained, the formation of a conducting channel at the semiconductor / insulator interface is verified by the existence of a low frequency, forward bias capacitance plateau with a measured capacitance equal to C_{ins}^{sc} (Eq. 3.41). A reverse bias capacitance equal to $C_{sc,ins}^{inj}$ (Eq. 3.43) verifies that the semiconductor layer is fully depleted.

Care must be taken, however, to verify that the semiconductor layer is sufficiently insulating, as a similar maximum capacitance plateau can occur due to lateral current flow through the semiconductor layer bulk, R_{sc}^{lat}). Figure 3.10 shows a C-(V,f) contour plot for a structure identical to that yielding the C-(V,f) contour plot shown in Fig. 3.6, except that the semiconductor layer is processed so as to exhibit a higher (although still relatively small) degree of conductivity. Although all three capacitance levels are apparent, the maximum capacitance plateau, C_{ins}^{sc}, extends well into the reverse bias region for low measurement frequency, without a clear threshold voltage for interface channel formation as witnessed in Fig. 3.6; the analysis of such results is somewhat ambiguous.

The change in bias voltage required to reduce the capacitance from C_{ins}^{inj} to $C_{sc,ins}^{inj}$, ΔV_{depl}, can be used to estimate the semiconductor layer carrier concentration when it is realized that this transition corresponds to depletion of the semiconductor layer. A rough approximation is obtained by neglecting the semiconductor layer thickness, yielding a carrier concentration

$$n_{sc} \approx \frac{\epsilon_{ins} \Delta V_{depl}}{q t_{ins} t_{sc}}, \tag{3.44}$$

where q is the electron charge. ΔV_{depl} is readily assessed from a capacitance-voltage (C-V) curve such as that shown in Fig. 5.10. Note that this estimate applies only to the portion of the semiconductor layer directly beneath the injector region; the result is not affected by the carrier concentration of the exposed portion of the semiconductor

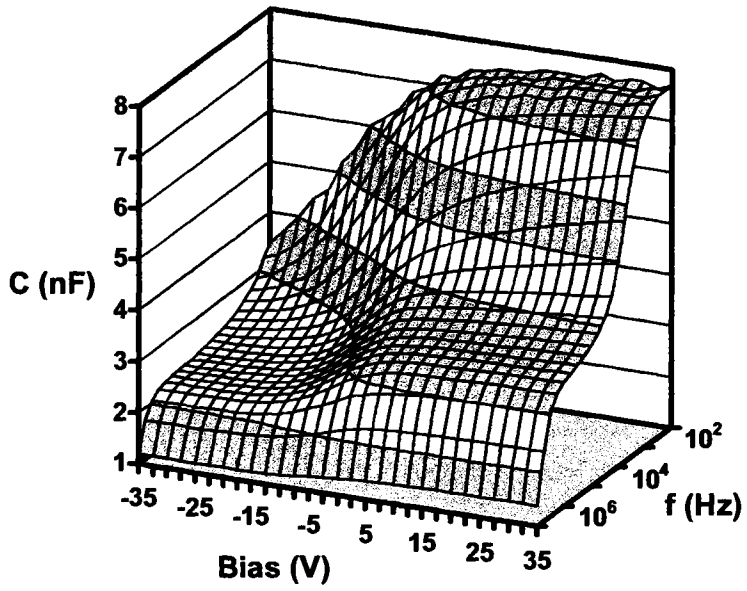

Figure 3.10: C-(V,f) contour plot of capacitance as a function of bias voltage (-35 to 35 V) and measurement frequency (100 Hz to 10 MHz), using the C-(V,f) test structure depicted in Fig. 3.5. The structure is identical to that yielding Fig. 3.6, except that the semiconductor layer here exhibits a higher degree of conductivity so that measurement results are somewhat obscured.

layer, and the existence of a non-negligible difference between the two regions is certainly possible.

In conclusion, a C-(V,f) contour plot of measured capacitance as a function of bias and frequency yields a great deal of information regarding injection and interface channel formation. There is undoubtedly much additional information available from this characterization method, however time constraints have not allowed a thorough investigation of these possibilities.

Finally, it should be noted that although DC characterization of an injecting interface might yield results in a more straightforward manner, the structure employed for the C-(V,f) characterization technique (Fig. 3.5) circumvents fabrication challenges confronted in an attempt to realize a test structure for DC interface characterization. In such a DC test structure, fabrication and processing steps required

to obtain an insulating semiconductor region and a high quality carrier injecting interface must be such as to maintain the conductivity of the bottom conductor layer, and the bottom conductor / semiconductor interface must be able to extract injected carriers efficiently (i.e. with a minimal voltage drop) so that the measured characteristics are predominately those of the injector / insulator interface. In the C-(V,f) structure, the insulator layer serves to protect the bottom conductor layer from degradation during processing. The choice of material for the bottom conductor layer is relatively unrestricted, as long as compatibility with the insulator layer is maintained; the bottom conductor layer functions strictly as a conductor, since carrier extraction from the semiconductor layer does not need to be considered.

3.4 Conclusions

This chapter describes experimental tools and techniques relevant to the research and results presented in this thesis. Thin film deposition via evaporation and sputtering is first discussed, followed by a look at post-deposition annealing using rapid thermal processing (RTP). Ion beam sputtering is given particular consideration, as it is heavily used in fabricating transparent thin film transistors to be described in Chapter 5.

Optical and electrical characterization of thin films is next explored. The theory behind optical characterization of bandgap energy and transition type is examined, as a useful interpretation of experimental results requires a thorough understanding of the complexities of this analysis. Simple conductivity measurement methods are noted; the physical mechanism behind the thermoelectric probe method for determination of majority carrier type is explained. The Hall method is perhaps the most commonly-used method for characterization of mobility and carrier concentration. The physical basis underlying the Hall effect is first considered, followed by a look at practical considerations and limitations in applying the van der Pauw Hall method. Evaluation of work function using the Kelvin probe technique is described; experi-

mental results are given for several p-type transparent conducting oxides ($CuYO_2$:Ca, $CuScO_2$:Mg, and $CuCrO_2$).

The final topic considered in this chapter is device characterization. Basic optical characterization of a transparent electronic device consists of a simple measurement to determine the degree of transparency. Electrical characterization in general merits brief mention only, as it is carried out in essentially the same manner as would be appropriate for the analogous conventional electronic device. The extraction of thin film transistor (TFT) mobility and threshold voltage from drain current measurements is considered in some detail, in anticipation of results given in Chapter 5. Finally, a novel technique, the capacitance-(voltage, frequency) [C-(V,f)] method, is proposed for simultaneously characterizing carrier injection into an insulating semiconductor and mobile carrier accumulation (interface channel formation) at an insulating semiconductor / wide bandgap insulator interface. The C-(V,f) method employs AC capacitance measurements over a range of DC bias voltages and AC measurement signal frequencies; the test structure requires a relatively simple fabrication process and circumvents potential material and process compatibility issues.

4. ELECTRICAL CHARACTERIZATION OF $CuYO_2$ / ZnO / ITO p-i-n HETEROJUNCTION DIODES

This chapter presents the results of an electrical characterization study of transparent $CuYO_2$ / ZnO / ITO p-i-n heterojunction diodes. [88] As discussed in Section 2.4.1, electrical characterization of previously reported transparent diodes has been inadequate at best; rectification is typically interpreted within the framework of the ideal pn junction model, despite the lack of evidence that such an analysis is appropriate. The devices characterized in this chapter exhibit electrical characteristics that are quite similar to those of many previously reported transparent diodes, however the conclusions reached here are distinctly different.

The transparent p-i-n heterojunction diodes are fabricated using heavily doped, p-type $CuYO_2$:Ca and semi-insulating ZnO thin films deposited onto a glass substrate coated with degenerately doped, n-type indium-tin oxide (ITO). The diode structure has a total thickness of 0.75 μm and an optical transmission of $\sim$20% to 70% in the visible region of the electromagnetic spectrum. Rectification is observed, with a forward-to-reverse current ratio as high as 60 in the range -4 to 4 V. DC current-voltage and AC capacitance measurements bear little resemblance to those expected from ideal pn junction theory. The forward bias current-voltage characteristics are dominated by the flow of space-charge-limited current (SCLC) in the i-ZnO layer, with electron injection from the n-ITO / i-ZnO interface; forward bias hole injection is suppressed by the large hole injection energy barrier at the p-$CuYO_2$:Ca / i-ZnO interface. Capacitance measurements are dominated by the effects of bulk electron traps in the i-ZnO layer. SCLC theory is used to estimate the ZnO bulk trap depth and concentration from the current-voltage characteristics; analysis of capacitance measurements yields a similar estimate for bulk trap depth.

4.1 Device fabrication and materials characterization

Figure 4.1 shows the structure used to fabricate the diodes. [88] The 1 inch square glass substrate, coated with a 200 nm sputtered ITO film, is supplied by Planar Systems, Beaverton, OR. The ITO is highly transparent and has a conductivity of $\sim 10^3$ to $10^4\ \Omega^{-1}\ cm^{-1}$. ZnO is deposited onto the ITO-coated glass by RF magnetron sputtering at a substrate temperature of 150°C, in 10 mTorr of Ar, with a target-to-substrate distance of 2.5 cm and an RF power of 100 W; the film thickness is ~250 nm. Two doping procedures are employed to vary the carrier concentration in the as-deposited ZnO films; intentionally doped ZnO:Al is sputtered from a ZnO target doped with 2% Al, and intrinsically doped oxygen-deficient ZnO_{1-y} from a pure ZnO target. P-type $CuYO_2$:Ca dots are deposited through a shadow mask at a substrate temperature of 100°C by reactive co-evaporation; Cu, Y, and Ca are thermally evaporated from refractory boats in oxygen at 150 μTorr. The thickness of the $CuYO_2$:Ca layer is ~300 nm. The completed structure is subjected to a rapid thermal anneal (RTA) for three minutes at 600°C in oxygen. This RTA process is necessary to improve the conductivity of the p-type $CuYO_2$:Ca via oxygen intercalation, but simultaneously renders the ZnO layer semi-insulating to insulating ($\sigma \lesssim 0.1\ \Omega^{-1}\ cm^{-1}$); the post-RTA conductivity of the ZnO cannot be directly determined, as the relevant ZnO regions are those covered by the $CuYO_2$ dots and the conductive ITO underlayer shunts current flow in the film plane. As discussed in Section 2.2.1, the conductivity of ZnO is enhanced by an oxygen-deficient stoichiometry; thus annealing in an oxidizing ambient acts to reduce the conductivity of the ZnO films. Finally, a small amount of In is applied to make reliable electrical contact to the ITO and $CuYO_2$ layers

Hall mobility and conductivity measurements are performed using the van der Pauw Hall method (Section 3.2.2). For ZnO:Al, the Hall mobility $\mu = 11.9\ cm^2/V\ s$ and conductivity $\sigma = 1800\ \Omega^{-1}\ cm^{-1}$ give a carrier concentration $n = 9.6 \times 10^{20}\ cm^{-3}$. For an undoped, nonstoichiometric ZnO film, the Hall mobility $\mu = 6.2\ cm^2/V$

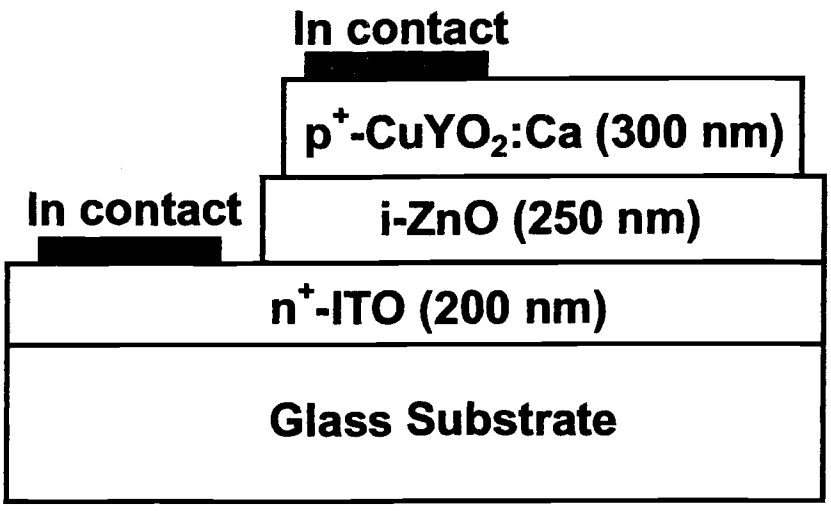

Figure 4.1: Device structure of a $CuYO_2$:Ca / ZnO / ITO p-i-n heterojunction diode.

s and conductivity $\sigma = 50\ \Omega^{-1}\ cm^{-1}$ give a carrier concentration $n = 5 \times 10^{19}\ cm^{-3}$. These measurements are for ZnO films sputtered on glass, with no post-deposition annealing; both types of ZnO are strongly affected by the high-temperature oxygen anneal required for the $CuYO_2$:Ca layer.

The $CuYO_2$:Ca films show p-type conductivity by thermoelectric probe measurements, with a Seebeck coefficient of 280 μV/K. Hall measurements cannot determine the mobility of holes in the $CuYO_2$ films, thus placing an approximate upper limit on mobility of $\sim$1 cm^2/V s. Using this mobility value and a conductivity of $\sim 1\ \Omega^{-1}\ cm^{-1}$ yields a minimum carrier concentration of $p \sim 10^{19}\ cm^{-3}$ for p-type $CuYO_2$:Ca. $CuYO_2$:Ca thin films typically exhibit $\sim$40% to 50% transparency in the visible region of the electromagnetic spectrum.

4.2 Electrical characterization

4.2.1 Energy band considerations

An approximate equilibrium energy band diagram for the transparent $CuYO_2$:Ca / ZnO / ITO p-i-n heterojunction diode is shown in Fig. 4.2. ITO has a bandgap of ~3.6 eV [55] and is degenerately doped n-type, so that its Fermi level, E_F, is positioned slightly above the conduction band minimum, E_C. The ZnO bandgap is ~3.3 eV. [58] The electron affinities (χ) of ZnO and ITO are ~4.5 to 5 eV (Section 2.2.1) and ~4.7 to 4.8 eV [55], respectively. The ITO / ZnO interface portion of the energy band diagram is established as discussed in Sections 2.3.3 and 2.3.4.

As mentioned previously, the ZnO layer becomes semi-insulating ($\sigma \lesssim 0.1\ \Omega^{-1}$ cm^{-1}) after the 600°C RTA treatment in oxygen, corresponding to an electron concentration, $n \lesssim 10^{17}\ cm^{-3}$, which is at least two orders of magnitude smaller than the carrier concentration of the $CuYO_2$:Ca or the ITO layers.

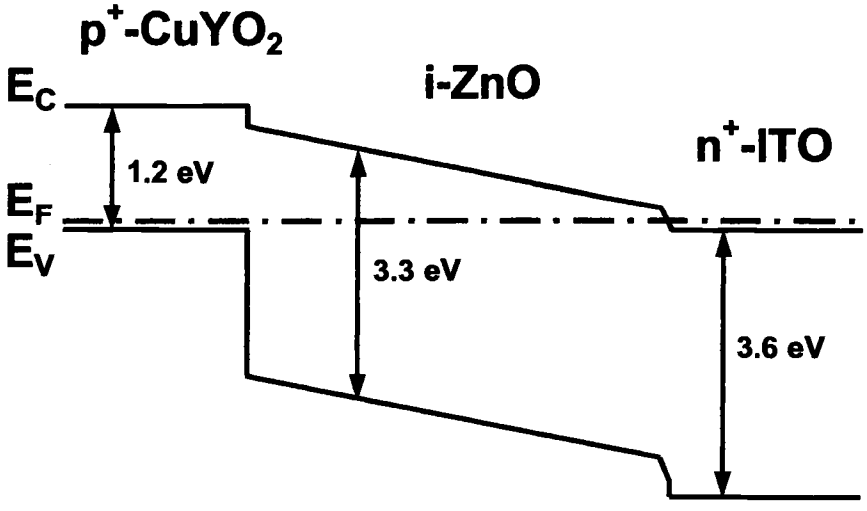

Figure 4.2: Equilibrium energy band diagram for a $CuYO_2$:Ca / ZnO / ITO p-i-n heterojunction diode.

Sketching the $CuYO_2$ portion of the energy band diagram shown in Fig. 4.2 is more difficult since there is some uncertainty regarding the band structure of $CuYO_2$. Figure 4.3 shows $(\alpha h\nu)^{1/2}$ and $(\alpha h\nu)^2$ plots of the absorption edge of an undoped $CuYO_2$ thin film for estimation of the indirect and direct allowed optical bandgaps, respectively (as described in Section 3.2.1). This results in estimates of ~1.2 eV (indirect) and ~3.6 eV (direct), in agreement with those reported by Benko and Koffyberg for $CuYO_2$:Ca from photoelectrochemical measurements. [110] These results are also consistent with optoelectronic assessment and electronic structure calculations of Yanagi *et al.* who find for $CuAlO_2$, a similar delafossite material, an indirect bandgap at ~1.8 eV and a direct bandgap at ~3.5 eV. [24]

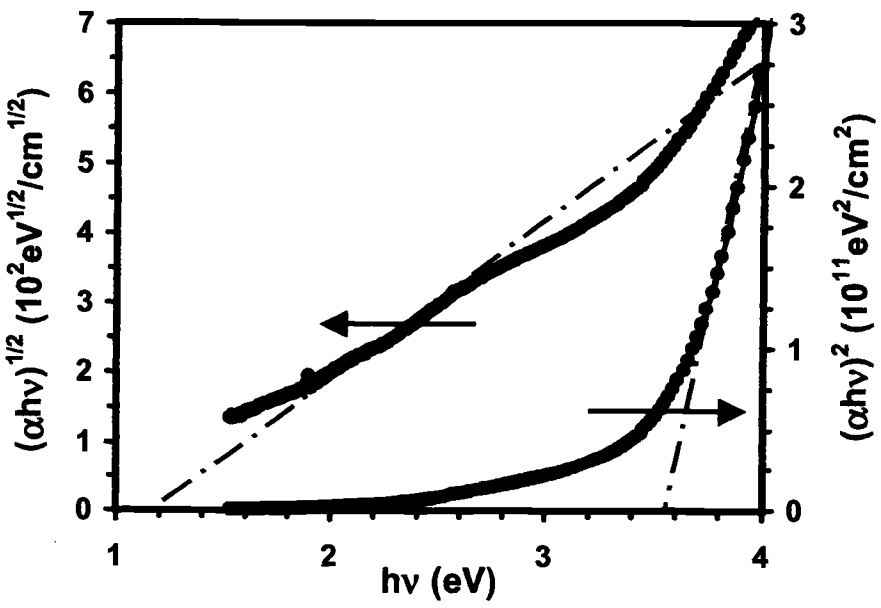

Figure 4.3: $(\alpha h\nu)^{1/2}$ and $(\alpha h\nu)^2$ plots of the absorption edge of an undoped $CuYO_2$ thin film for estimation of the indirect and direct allowed optical bandgaps, respectively. This results in an indirect bandgap of ~1.2 and a direct bandgap of ~3.6 eV.

However, these results are inconsistent with an electronic structure calculation made by Mattheis, which indicates that the $CuYO_2$ minimum bandgap is direct at ~2.7 eV and that oxygen intercalation results in the formation of mid-gap impurity bands, thus decreasing the effective bandgap (note that the absolute value of the bandgap energy given by these calculations does not possess a high degree of reliability). [112] Additionally, from soft x-ray photoabsorption spectroscopy measurements, Cava *et al.* observe the emergence of new unoccupied bandgap states accompanying oxygen intercalation ($CuYO_2 \rightarrow CuYO_{2.55}$). [113] These measurements are interpreted to indicate that Cu atoms in $CuYO_2$ are in the Cu^{+1} oxidation state, characterized by a $2p^6 3d^{10} \rightarrow 2p^5 3d^{10} 4s^1$ photoabsorption transition, but that oxidized Cu atoms in $CuYO_{2.55}$ are in the Cu^{+2} oxidation state, characterized by a $2p^6 3d^9 \rightarrow 2p^5 3d^{10}$ photoabsorption transition. Thus, the results of Mattheis and Cava *et al.* suggest that the ~1.2 eV indirect bandgap estimated from optical absorption measurements could be an extrinsic effect due to midgap states arising from oxygen intercalation which is, in fact, employed to improve the conductivity of the $CuYO_2$ layer in the devices under consideration.

Nie *et al.* performed band structure calculations for $CuAlO_2$, $CuGaO_2$, and $CuInO_2$ [114]; these materials share the delafossite structure of $CuYO_2$. In all three cases, the minimum bandgap is found to be indirect, with energies of 1.97, 0.95, and 0.41 eV for $CuAlO_2$, $CuGaO_2$, and $CuInO_2$ respectively. However, when these band structures are combined with the calculated dipolar optical transition matrix element (indicating the probability of an optical transition), the predicted values for the apparent experimental optical bandgaps are 2.75, 2.70, and 3.12 eV, respectively. The experimentally-obtained optical bandgaps for these materials are 3.5, 3.6, and 3.9 eV, respectively (Table 2.2). These results indicate that in materials with the delafossite structure there may exist a large disparity between the minimum bandgap (establishing electrical behavior) and the apparent optical bandgap (establishing optical transparency). Such a scenario might explain the tendency of the

delafossites to exhibit a marked decrease in transparency with increasing doping; although lower-energy band-to-band transitions are quantum-mechanically forbidden, degenerate doping necessary to attain reasonable p-type conductivity introduces a large number of states near the valence band edge, and possibly self-compensating defects (Section 2.3.1) near the conduction band edge.

Such intentionally and unintentionally introduced defect states would provide efficient optical coupling to the conduction band and valence band, thus dramatically increasing optical absorption near the energy of the minimum bandgap from that seen in an equivalent undoped film. States with strong real-space localization (such as deep defect states) are characterized by quantum mechanical wave functions with a large degree of k-space dispersion. Momentum conservation is easily satisfied in optical absorption transitions between deep defect states and the valence or conduction bands, thus greatly amplifying the effective optical absorption coefficient at energies near that of the minimum bandgap.

Returning to Fig. 4.3, an appraisal of the literature seems to indicate that the strong absorption edge at ~3.6 eV corresponds to an allowed direct bandgap. The origin of the weak absorption edge at ~1.2 eV is less certain; it is most likely attributable to either an intrinsic, indirect and/or forbidden bandgap or to midgap states resulting from intentionally-introduced impurities and perhaps self-compensating defects. Regardless of the absorption mechanism, the bulk of the evidence seems to indicate that the bandgap or effective bandgap that establishes the $CuYO_2$ electronic behavior is approximately 1.2 eV, and certainly much smaller than that of the adjacent ZnO layer. Moreover, the Fermi level must be positioned near the valence band maximum since the hole concentration is quite large. Kelvin probe measurements of the $CuYO_2$:Ca films used in these diodes indicate that the valence band, E_V, is located ~5.3 to 5.8 eV below the vacuum level, E_{vac} (Section 3.2.3). Benko and Koffyberg obtain a similar value (5.3 ± 0.2 eV) using a photoelectrochemical measurement technique [110]. Based on these measurements, the electron affinity ($\chi = E_{vac} - E_C$) of the

$CuYO_2$:Ca layer is estimated to be ~4.1 to 4.6 eV. This is the energy band situation indicated in Fig. 4.2.

Two aspects of Fig. 4.2 merit further comment. First, note that the conduction band interfacial discontinuities should ideally be quite small, as indicated in Fig. 4.2, due to the similar electron affinity values of the ITO, ZnO, and $CuYO_2$ layers. Although the $CuYO_2$ / ZnO conduction band discontinuity could possibly be as large as ~0.9 eV (assuming an ideal interface and worst-case electron affinity mismatch), the valence band discontinuity at this junction is certainly larger, with a corresponding worst-case minimum of ~1.2 eV; the true valence band/conduction band discontinuity mismatch is probably much larger (i.e. $\Delta E_V \gg \Delta E_C$) than indicated by this worst-case estimate, since the uncertainty in the electron affinities of ZnO and $CuYO_2$ is quite large. Although interface nonidealities (interfacial dipole and/or charge) are quite possibly present, it is unlikely that their effect would be sufficient to annihilate such a large disparity between the conduction band and valence band discontinuities at the $CuYO_2$ / ZnO interface. Furthermore, forward bias current-voltage characteristics do not indicate a significant energy barrier to electron flow from the ZnO layer into the $CuYO_2$ layer (Section 4.2.2). Thus it appears, based on energy band considerations and experimental evidence, that the $CuYO_2$ / ZnO interface conduction band discontinuity is quite small (and the valence band discontinuity quite large) as depicted in Fig. 4.2. It should also be noted that abrupt interfacial band discontinuities are likely to be smoothed out to some extent by interdiffusion and compositional grading due to high temperature steps employed in the fabrication process. Secondly, as a consequence of the relatively large valence band discontinuity expected at the $CuYO_2$ / ZnO interface, forward bias (positive bias to $CuYO_2$) current is likely to be unipolar, due solely to electron injection at the ITO / ZnO interface; forward bias hole injection is inhibited by the large valence band discontinuity energy barrier at the $CuYO_2$ / ZnO interface. Thus, although this diode structure is denoted as a p-i-n heterojunction, its electrical behavior differs from that of a conventional p-i-n homo-

junction diode, in which bipolar carrier injection and recombination in the i-layer is the dominant current mechanism. [57]

4.2.2 DC current-voltage characteristics

Figure 4.4 presents typical current-voltage (I-V) curves for two types of $CuYO_2$:Ca / ZnO / ITO p-i-n heterojunction diodes in which the ZnO layer is either undoped or doped with Al. Figures 4.5 and 4.6 display corresponding forward bias log(I)-log(V) and ln(I)-V curves for the ZnO:Al device. Several features of these I-V characteristics are noteworthy.

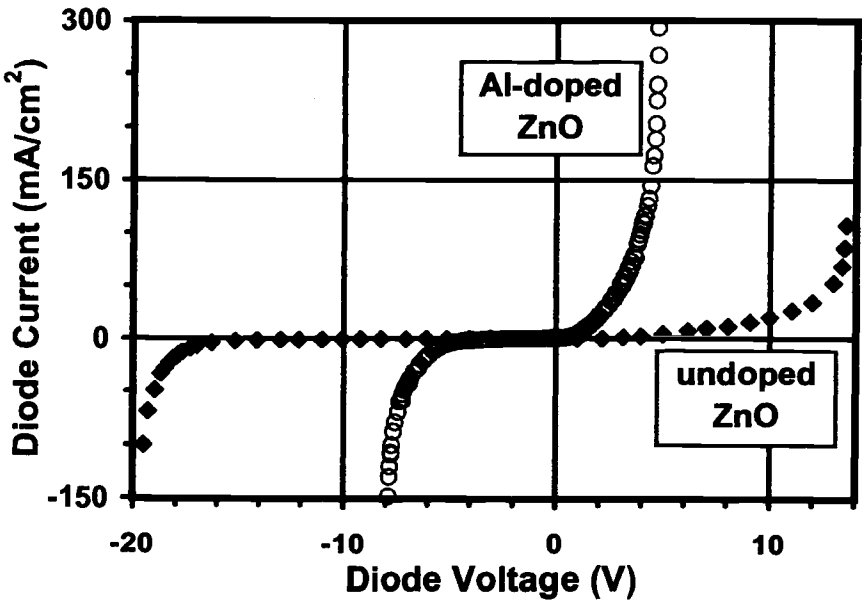

Figure 4.4: I-V characteristics for two types of $CuYO_2$:Ca / ZnO / ITO p-i-n heterojunction diodes in which the ZnO layer is either undoped or doped with Al.

First, these diodes clearly exhibit rectification. A maximum forward-to-reverse current ratio of ~60 occurs at ±4 V for the ZnO:Al structure, and at ±5 V for the structure containing undoped ZnO. In reverse bias, the initially small leakage current

is followed by a rather soft breakdown. Both diode structures are able to sustain a maximum current of ~10 mA (150 mA/cm^2) or more under both forward and reverse bias.

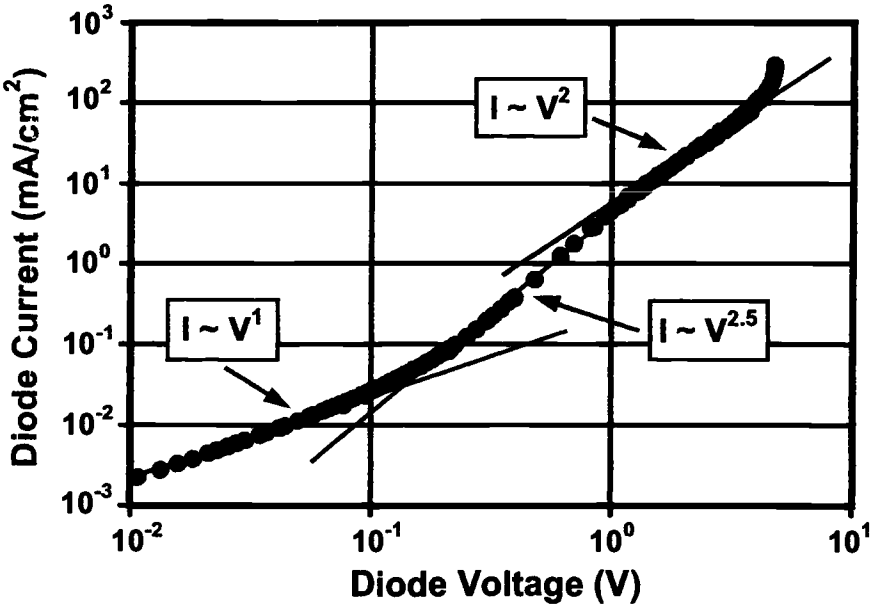

Figure 4.5: Forward bias log(I)-log(V) characteristics of a $CuYO_2$:Ca / ZnO / ITO p-i-n heterojunction diode in which the ZnO layer is Al doped. Three power law fits to different portions of the log(I)-log(V) curve are shown.

Second, Figs. 4.4 and 4.5 provide evidence that the series resistance of these devices is small and does not make a significant contribution to the measured I-V characteristics. An upper bound for the series resistance may be estimated from Fig. 4.4 as the inverse of the slope of the I-V curve at the largest forward bias; the maximum series resistance estimated in this manner is ~25 Ω for these diodes. Additional evidence that the series resistance actually must be smaller than this estimate is available from Fig. 4.5, when it is recognized that a log(I)-log(V) curve

should give rise to an I $\propto$ V^1 dependence at large forward bias if the diode is series-resistance limited; Fig. 4.5 clearly shows that this is not the case.

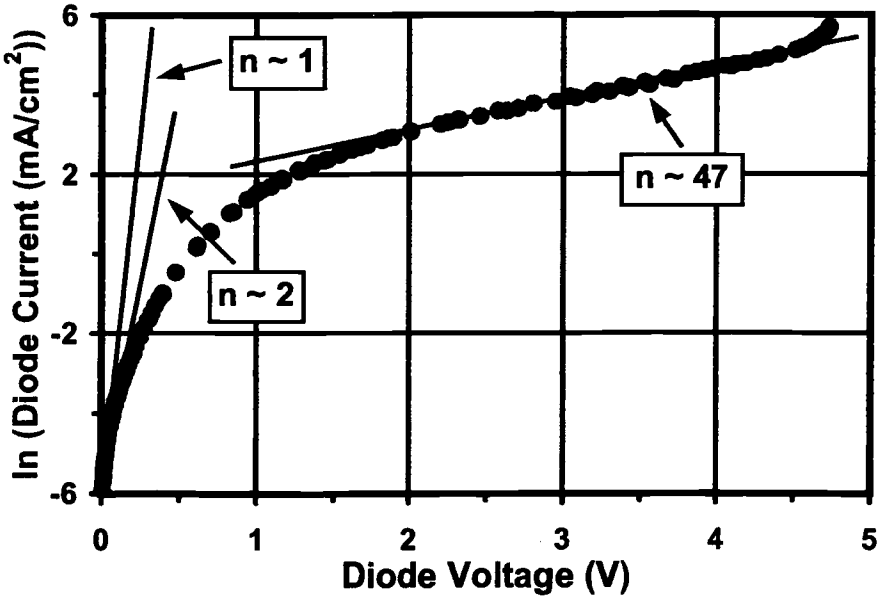

Figure 4.6: Forward bias ln(I)-V characteristics of a $CuYO_2$:Ca / ZnO / ITO p-i-n heterojunction diode in which the ZnO layer is Al doped. Exponential fit lines correspond to ideality factors n = 1, 2, and 47.

Third, Fig. 4.6 shows that the diode does not conform to the ideal pn junction forward-bias I-V relationship [57],

$$\ln(I) \propto \frac{q}{nkT}V, \tag{4.1}$$

where q is the electron charge, k is the Boltzmann constant, T is the temperature, and n is an ideality factor usually taking a value between one and two. An illustration of the futility of trying to fit a typical measured ln(I)-V curve with n equal to one or two is shown in Fig. 4.6. Observe that a significant portion of the ln(I)-V curve can be well fit for n equal to 47; such a result provides clear evidence against the

viability of employing an ideal pn junction exponential relationship to account for the measured diode I-V characteristics.

The power-law fits shown in Fig. 4.5 provide insight into the operative mechanisms responsible for the I-V trends of the $CuYO_2$:Ca / ZnO / ITO p-i-n heterojunction diodes. For forward bias voltages greater than $\sim$1 V, the current is proportional to V^2; this is the characteristic relationship expected for space-charge-limited current (SCLC), as discussed in Section 2.3.2. The $I \propto V^1$ characteristic observed for small voltages might be attributed to pre-SCLC ohmic conduction in the i-ZnO layer. However, it is also possible that this apparent relationship is merely coincidental (i.e attributable to contact effects), as it holds over only the first 100 mV of the forward-bias current-voltage curve. The $I \propto V^{2.5}$ may also be attributed to contact effects; however, if the $I \propto V^1$ relationship is indeed pre-SCLC bulk conduction, the $I \propto V^{2.5}$ region is seen as the onset of SCLC conduction, in which the electron quasi-Fermi level in the i-ZnO layer moves through a deep trap level to yield a power-law dependence greater than two. [72] Finally, at the largest applied forward biases, the log(I)-log(V) curve deviates from a square-law dependence, bending upward with a much greater slope; this regime is probably due to the onset of a SCLC trap-filled limit [72], where the electron quasi-Fermi level moves through a trap level, or perhaps (but less likely) to the onset of double injection or breakdown.

Thus, it appears that the forward bias current-voltage characteristics are dominated by the flow of SCLC in the i-ZnO region. The ratio of injected free electrons to total (free and trapped) injected electrons, θ (Section 2.3.2), can be calculated as a function of voltage,

$$\theta(V) = \frac{I(V)}{\frac{9}{8}\epsilon\mu\frac{V^2}{L^3}}, \tag{4.2}$$

where the denominator is the ideal trap-free SCLC relationship (Eq. 2.6). Figure 4.7 plots θ as a function of forward bias voltage for the $CuYO_2$:Ca / ZnO / ITO diode, with $\epsilon = 9.0\ \epsilon_0$ [57] and $\mu = 11.9\ cm^2/V\ s$ (Section 4.1).

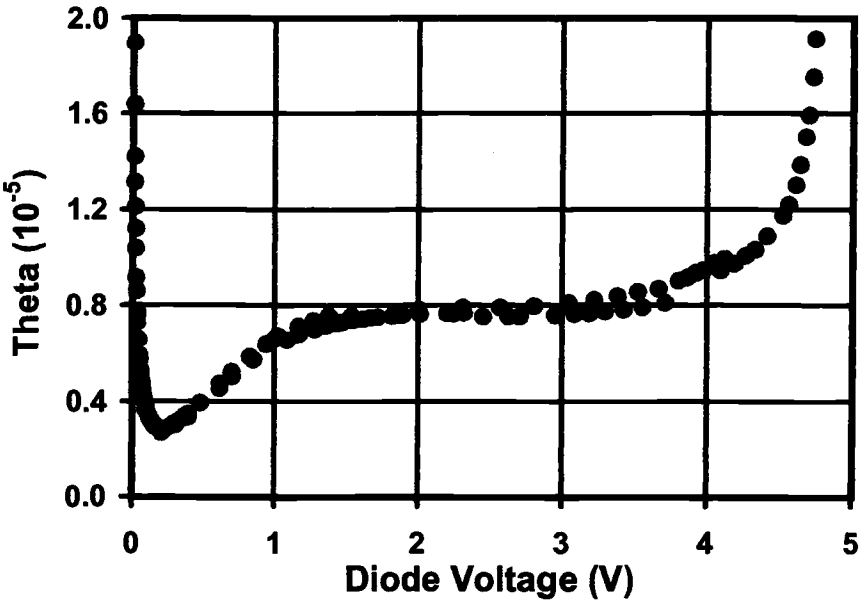

Figure 4.7: Forward bias calculated SCLC θ(V) for a $CuYO_2$:Ca / ZnO:Al / ITO p-i-n heterojunction diode.

The abrupt increase in θ beginning at ~3 to 4 V coincides with the quasi-Fermi level beginning to move through the trap level responsible for the shallow-trap SCLC current-voltage characteristics. The total injected charge per unit area (according to the ideal, simplified SCLC model) is given by [72]

$$Q = \frac{2}{3}\frac{\epsilon V}{t}, \tag{4.3}$$

where t and ϵ are the thickness and dielectric constant of the ZnO layer, respectively ($\epsilon_{ZnO} = 9.0\ \epsilon_0$ [57]). The average injected free electron concentration, n, is then given by

$$n = \theta n_{free+trapped} = \theta\frac{Q}{qt}, \tag{4.4}$$

where q is the electron charge. This expression can be used to approximate the free electron concentration when the quasi-Fermi level is in the vicinity of the trap level (~3.5 V in Fig. 4.7); the resulting value of n (~1.7×10^{11} cm^{-3}) can be used to

estimate the location of the trap level using the standard expression [57]

$$E_C - E_F = kT \ln\left(\frac{N_C}{n}\right), \tag{4.5}$$

where N_C is the conduction band effective density of states. N_C can be calculated from the density-of-states effective mass for electrons (m_{de}) as [57]

$$N_C \equiv 2\left(\frac{2\pi m_{de} kT}{h^2}\right)^{3/2} M_C, \tag{4.6}$$

where k is the Boltzmann constant, T is the temperature, h is the Planck constant, and M_C is the number of equivalent conduction band minima. Using values of $0.27m_0$ and 1 for the ZnO electron effective mass [57] and M_C, respectively, yields N_C equal to 3.5×10^{18} cm^{-3}. The trap depth can now be estimated using Eq. 4.5 to be ~0.44 eV. An estimate of the trap concentration can be obtained by realizing that the quasi-Fermi level moves through the trap level when the total injected space charge (Eq. 4.3) is on the order of the trap density; this approximation yields a trap concentration of ~2.1 to 2.7×10^{16} cm^{-3}.

If the transition from $I \propto V^1$ to $I \propto V^{2.5}$ at ~0.1 V does indeed correspond to a transition from ohmic to SCLC conduction, Eq. 2.10 can be used to estimate the equilibrium carrier concentration of the ZnO layer. Using $\theta = 8 \times 10^{-6}$ (Fig. 4.7) and $V_x = 0.1$ V in this expression yields an equilibrium free electron concentration of $\sim 6.4 \times 10^9$ cm^{-3}. An upper bound can be placed on the equilibrium free electron concentration by assuming that the $I \propto V^1$ and $I \propto V^{2.5}$ regions arise due to contact effects and using $V_x = 1$ V in Eq. 2.10, yielding a value of $\sim 6.4 \times 10^{10}$ cm^{-3}.

4.2.3 Capacitance characteristics

Figure 4.8 presents capacitance-voltage (C-V) characteristics at selected measurement frequencies between 100 Hz and 10 MHz. Figure 4.9 shows the measured capacitance-frequency (C-f) characteristics at reverse biases from 0 to -4 V. Capacitance measurements shown here are for an Al-doped ZnO device, but are typical of capacitance measurements for both undoped and Al-doped ZnO devices.

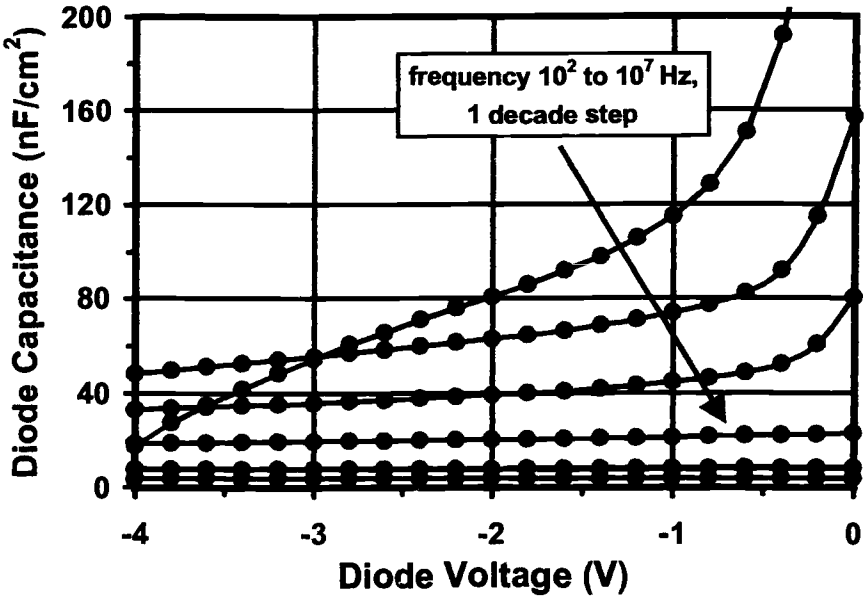

Figure 4.8: Reverse bias C-V characteristics of a $CuYO_2$:Ca / ZnO:Al / ITO p-i-n heterojunction diode obtained at frequencies of 100 Hz, 1 kHz, 10 kHz, 100 kHz, 1 MHz, and 10 MHz.

The capacitance of a typical trap-free diode is expected to decrease with increasing reverse bias, due to an increase in the depletion region width, and to be independent of the measurement signal frequency. Thus, the voltage dependence of the 100 Hz, 1 kHz, and 10 kHz curves shown in Fig. 4.8 is at least qualitatively consistent with the expected trend. In contrast, the voltage independence of the 100 kHz, 1 MHz, and 10 MHz curves and the frequency dispersion seen in all of the C-V curves are not expected. These anomalous trends are attributed to the presence of bulk traps and to measurement artifacts, as discussed in the following.

For a trap to contribute to the measured capacitance, both capture and emission of a carrier must occur quickly enough so that the trap is able to dynamically maintain a steady-state occupancy with respect to the measurement signal frequency. [105] Above a certain frequency for each trap, the trap can no longer follow the applied AC measurement signal so that it no longer contributes to the measured capacitance.

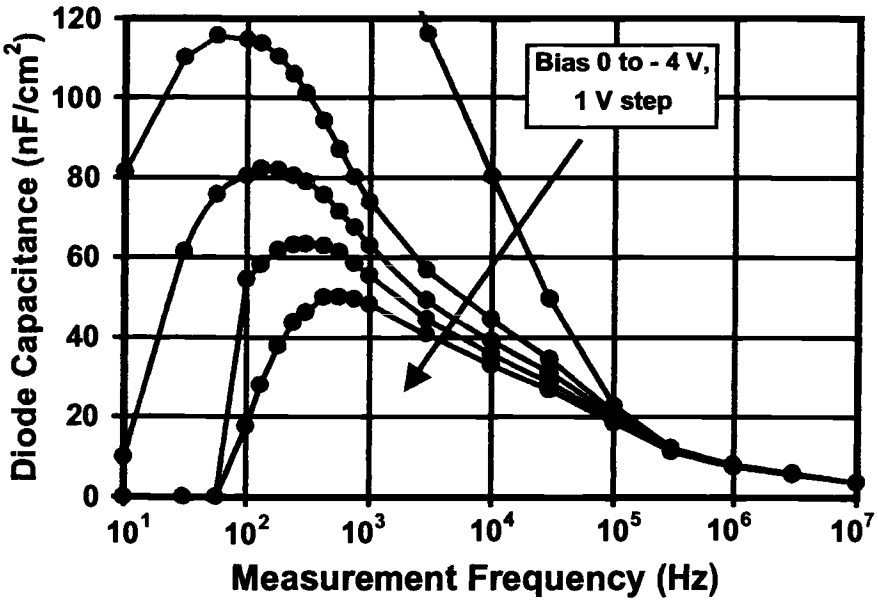

Figure 4.9: Reverse bias C-f characteristics of a $CuYO_2$:Ca / ZnO:Al / ITO p-i-n heterojunction diode for reverse biases of 0, -1, -2, -3, and -4 V.

In practice, trap emission (as compared to capture) usually establishes the steady-state trap occupancy. Assuming this to be the case, the maximum depth (distance below the conduction band minimum) beyond which an electron trap can no longer maintain steady state with an arbitrary measurement frequency may be estimated as [105]

$$E_{T,max} \approx kT \ln\left[\frac{\sigma_n v_{th} N_C}{f}\right], \tag{4.7}$$

where k is the Boltzmann constant, T is the temperature, σ_n is the trap capture cross section for electrons, v_{th} it the electron thermal velocity, N_C is the conduction band effective density of states, and f is the measurement signal frequency.

A decrease in capacitance corresponds to an increase in the effective distance across which AC charge modulation occurs; the measurement signal frequency determines the critical energy depth of the traps that are able to contribute to the capacitance by capturing and releasing carriers in response to the measurement signal. A

decrease in the measured capacitance can arise from either a DC bias voltage-induced increase in the steady-state depletion region width, or as a consequence of an increase in the AC measurement signal frequency, due to the inability of traps to follow the measurement signal.

With these ideas in mind, consider Fig. 4.9, which displays the capacitance frequency dependence with reverse bias voltage as a parameter. First, note that the frequency dependence is at least as strong as the voltage dependence. Thus, traps play an important role in establishing the capacitance trends shown in Fig. 4.9, as well as in Fig. 4.8. Next, note that the bias dependence is negligible above ~200 kHz; this disappearance of bias dependence indicates that charge modulation is taking place across a fixed spatial distance and that bulk traps are no longer able to respond. This situation clearly indicates that charge modulation takes place across the entire ZnO layer, however the magnitude of the capacitance at this point is somewhat troubling; it is significantly smaller than the expected capacitance of the entire ZnO layer (~32 nF/cm^2). The capacitance of the ZnO layer should be the smallest possible capacitance of this structure. Although the measured capacitance is expected to decrease due to parasitic RC effects, this should not occur until ~3 MHz; this is, in fact, seen in Fig. 4.9 (in this assessment it is important to recognize that in the device the parasitic R (ITO substrate resistance, ~15 Ω) and C (diode capacitance) are in series, whereas the capacitance measurement is performed with the impedance analyzer set to assume a parallel RC model; this results in a roll off in measured capacitance much earlier than expected from the RC time constant).

Realizing that this reduction in measured capacitance cannot be attributed to parasitic RC effects and that the effective thickness of the diode capacitor cannot be larger than that of the physical ZnO layer, the only remaining possibility is that the effective area of the diode capacitor becomes smaller than the physical area defined by the $CuYO_2$ region (Fig. 4.1) at high frequencies. Such an area is, in fact, defined by the In contact to the $CuYO_2$. Attaining the full capacitance defined by the $CuYO_2$

region requires that current injected at the In / $CuYO_2$ contact be able to move laterally throughout the $CuYO_2$ region in response to the measurement signal in order to charge and discharge the ZnO layer capacitance. The sheet resistance, R_{sh}, of the $CuYO_2$ is ~33 kΩ; the capacitance of the ZnO layer with an area defined by the $CuYO_2$ region is ~2.2 nF. A reasonable approximation for the resulting time constant, using $R \approx R_{sh}/4$, yields a corner frequency for the resulting RC roll off of ~50 kHz. Fig. 4.9 does indeed indicate a significant increase in attenuation of measured capacitance in this region (i.e. at ~30 kHz). Thus, the high-frequency capacitance trend seen in Fig. 4.9 can be understood as follows. For frequencies below ~10 kHz the measured capacitance is established by the area of the $CuYO_2$ region, and approaches the expected high-frequency asymptote of ~30 nF/cm^2. From ~30 kHz to ~1 MHz, the effective area (and thus the effective capacitance) decreases to that defined by the In contact (~20% to 25% of the $CuYO_2$ region area) due to the parasitic resistance of the lateral current path from the In contact throughout the $CuYO_2$ region (i.e. two-dimensional current flow). Finally, beginning at ~3 MHz, the measured capacitance again decreases due to the parasitic resistance of the ITO substrate.

Returning to the disappearance of bias dependence above ~200 kHz (Fig. 4.9), and recalling that this indicates that bulk traps are no longer able to respond to the measurement signal, Eq. 4.7 can be used to estimate the minimum trap depth in the ZnO bulk to be ~0.25 to 0.37 eV (assuming a neutral capture cross section of 10^{-16} to 10^{-14} cm^2).

The decrease in measured capacitance with decreasing frequency seen in Fig. 4.9 for low frequencies is also a measurement artifact. The diodes exhibit a relatively large reverse leakage current, which acts as a conductance in parallel with the diode capacitance. For high frequencies, the impedance of the diode capacitance ($Z_{cap} = (\omega C)^{-1}$) is much smaller (due to its inverse frequency dependence) than that of the parallel small-signal conductance ($Z_{cond} = dV/dI$), so that the impedance analyzer

can easily and unambiguously measure the capacitance. As the frequency decreases, however, Z_{cap} increases until it becomes comparable to Z_{cond} and eventually much larger, since Z_{cond} is not frequency dependent. Above some critical ratio, $|Z_{cap}|/Z_{cond}$, the impedance analyzer begins to lose its ability to extract the capacitance from the net measured impedance (the imaginary component of the net impedance becomes unmeasurable). In fact, the ratio $|Z_{cap}|/Z_{cond}$ evaluated at the low frequency capacitance peaks in Fig. 4.9 is essentially a constant at ~5 for all values of reverse bias. This effect is also responsible for the unexpected behavior of the 100 Hz curve in Fig. 4.8, decreasing rapidly and eventually dropping below the higher frequency curves as reverse bias is increased; the capacitance given by the impedance analyzer is much smaller than the true diode capacitance, and this effect becomes stronger with increasing reverse bias as the diode small-signal conductance increases.

Although Fig. 4.9 does not reveal a low frequency maximum capacitance below which all traps are able to respond to the measurement signal (due to the low frequency roll off discussed above), it is clear that additional traps continue to respond with decreasing frequency for frequencies as low as 100 Hz. Thus Eq. 4.7 indicates that the ZnO bulk contains traps as deep as ~0.45 to 0.57 eV (assuming a neutral capture cross section of 10^{-16} to 10^{-14} cm^2). Note that the range between the maximum and minimum trap depths obtained from the low frequency and high frequency capacitance characteristics contains the trap depth estimated in Section 4.2.2, ~0.44 eV, as indicated in Table 4.1.

Although capacitance measurements do not reveal the maximum trap depth (since traps continue to respond at the lowest frequencies for which the capacitance measurement provides valid data), the value obtained using SCLC theory analysis of the DC current-voltage characteristics (Section 4.2.2) provides an estimate of the maximum ZnO trap depth. Thus, a combination of the DC current-voltage and AC capacitance analyses indicates a range of electron traps starting at ~0.44 eV and extending ~70 to 190 meV toward E_C.

Table 4.1: Bulk ZnO electron trap depth estimates obtained from current-voltage and capacitance measurements.

Trap depth estimation method	DC current-voltage (SCLC theory)	Capacitance (low frequency)	Capacitance (high frequency)
Trap depth (eV)	0.44	0.45 - 0.57	0.25 - 0.37

Finally, note that the high frequency roll off in measured capacitance starting at ~20 kHz (due to the parasitic resistance from the In contact horizontally through the $CuYO_2$ film) could be easily avoided by providing a more conductive transparent top contact across the entire area of the $CuYO_2$. Since the $CuYO_2$ layer is degenerately doped, it is trivial to make ohmic contact using ITO or any other degenerately doped n-type transparent conductor.

4.3 Optical characterization

For optical transmission measurements, the diode structure is fabricated under identical conditions on a glass/ITO substrate, but without use of the shadow mask for deposition of the p-type $CuYO_2$:Ca. Figure 4.10 shows the optical transmission spectrum of a $CuYO_2$:Ca / ZnO:Al / ITO p-i-n heterojunction diode with a total thickness of 0.75 μm. The optical transmission is ~20% to 70% in the visible region of the electromagnetic spectrum. This compares to an optical transmission of ~20% reported by Sato *et al.* for their p-NiO / i-NiO / i-ZnO / n-ZnO p-i-n heterojunction diode [34] and 70% to 80% reported by Kudo *et al.* for their p-$SrCu_2O_2$ / n-ZnO p-n heterojunction diode. [84]

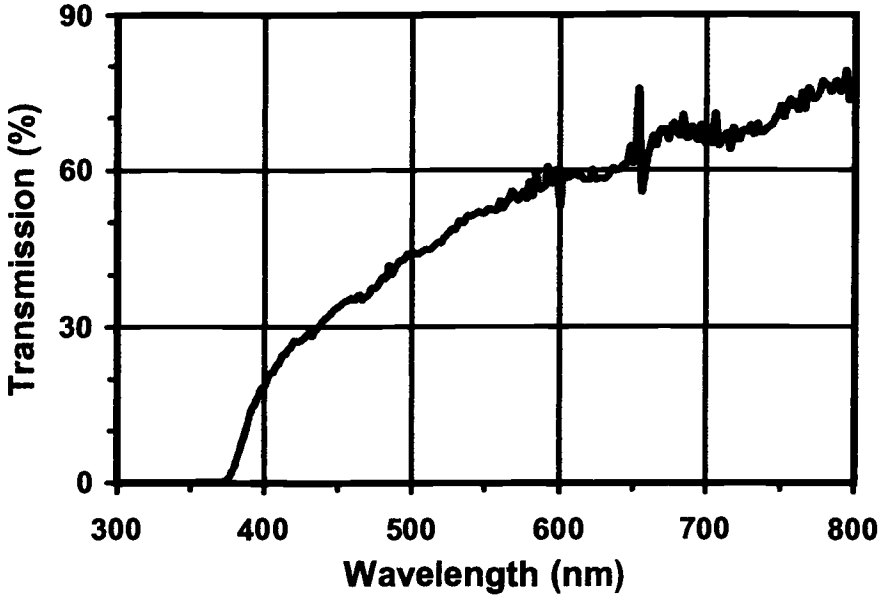

Figure 4.10: Optical transmission spectrum of a $CuYO_2$:Ca / ZnO:Al / ITO p-i-n heterojunction diode.

4.4 Conclusions

This chapter describes the results of a detailed electrical characterization study of transparent p-$CuYO_2$:Ca / i-ZnO / n-ITO p-i-n heterojunction diodes. Rectification is observed, with a forward-to-reverse current ratio as high as 60 in the range -4 to 4 V. As expected from energy band considerations, the forward bias current-voltage characteristics are dominated by the flow of space-charge-limited current (SCLC) in the i-ZnO layer with electron injection from the n-ITO / i-ZnO interface; forward bias hole injection is suppressed by the large hole injection energy barrier at the p-$CuYO_2$:Ca / i-ZnO interface. SCLC theory analysis is used to estimate the density and depth of bulk traps ($\sim$2.1 to 2.7 $\times$ 10^{16} cm^{-3} and $\sim$0.44 eV, respectively) that control the current-voltage characteristics.

Capacitance measurements show strong frequency dispersion and somewhat anomalous frequency dependence. The measured capacitance characteristics are at-

tributed to bulk traps in the i-ZnO layer and to measurement artifacts (low frequency roll off in measured capacitance due to the diode small-signal conductance, high frequency roll off due to two-dimensional current flow from the In contact through the $CuYO_2$:Ca layer, and higher frequency roll off due to the ITO substrate resistance). The trap depth range estimated from capacitance measurements (maximum trap depth ~0.45 to 0.57 eV, minimum trap depth ~0.25 to 0.37 eV) agree with the maximum trap depth obtained from SCLC theory analysis of current-voltage characteristics (~0.44 eV). The diode structure is semi-transparent, with a total thickness of 0.75 μm and an optical transmission of ~20% to 70% in the visible region.

5. FABRICATION AND CHARACTERIZATION OF HIGHLY TRANSPARENT ZnO-BASED THIN FILM TRANSISTORS

This chapter describes the fabrication and characterization of novel, highly transparent ZnO-based thin film transistors (TFTs). The average transmission in the visible region is ~90% or higher, far better than has been attained for previously reported semi-transparent transistors (Section 2.4.2). Figure 5.1 shows a substrate with three vertically oriented transparent TFTs, through which the OSU logo is clearly visible.

Figure 5.1: Three transparent TFTs on a 1 inch glass substrate, with the OSU logo clearly visible through the TFT structure (TFTs are oriented vertically). Soldered In contacts at the bottom corners provide contact to the bottom ITO layer.

The transparent TFTs are fabricated using ion beam sputtered ZnO (channel) and ITO (source/drain) layers on a 1 inch square glass substrate coated with a 200 nm

indium-tin-oxide (ITO) layer and a 220 nm aluminum-titanium-oxide (ATO) layer, which function as the gate electrode and gate insulator, respectively. The ZnO channel and ITO source/drain regions are patterned using Al shadow masks. The ITO source/drain and ZnO channel layer thicknesses are typically ~300 nm and ~100 nm, respectively.

Current-voltage measurements indicate fairly typical n-channel, enhancement mode behavior. Excellent drain current saturation is obtained, and the drain current on-to-off ratio is $\sim 10^7$. The experimentally extracted threshold voltage and channel mobility are ~10 to 20 V and ~0.3 to 2.5 cm^2/V s, respectively. The C-(V,f) characterization technique (described in Section 3.3.3) is employed to further elucidate TFT electrical characteristics; this section also serves to verify the validity of the C-(V,f) method.

Although the light sensitivity of these devices has not been studied in detail, several general traits are observed. Exposure to a typical ambient light intensity and spectrum has little to no observable effect on drain current characteristics. Direct exposure to ultraviolet (UV) radiation has a much stronger effect, due to the creation of electron-hole pairs by UV photons with energy greater than the ZnO bandgap. Light sensitivity is reduced by decreasing the ZnO channel layer thickness.

5.1 Fabrication and materials characterization

Figure 5.2 shows the typical device structure (hereafter referred to as structure 1). The 1-inch glass substrate, coated with a 200 nm sputtered ITO film and a 220 nm atomic layer deposition (ALD) ATO film, is supplied by Planar Systems, Beaverton, OR. The ITO is highly transparent and has a conductivity of $\sim 10^3$ to $10^4\ \Omega^{-1}\ cm^{-1}$. ATO is an engineered insulator developed by Planar Systems for use in alternating current thin film electroluminescent (ACTFEL) displays; a superlattice composed of alternating layers of Al_2O_3 and TiO_2 is capped on either end by an Al_2O_3 layer. The ITO layer serves as the TFT gate, and the ATO layer as the gate insulator. The

measured capacitance of the ATO layer is ~45 nF/cm^2, yielding a dielectric constant $\epsilon \approx 11\ \epsilon_0$. This analysis assumes the ATO thickness to be 220 nm, as specified by Planar Systems. However, Planar Systems also specifies an ATO dielectric constant of ~18 ϵ_0; clearly one or both of these specified values are in error.

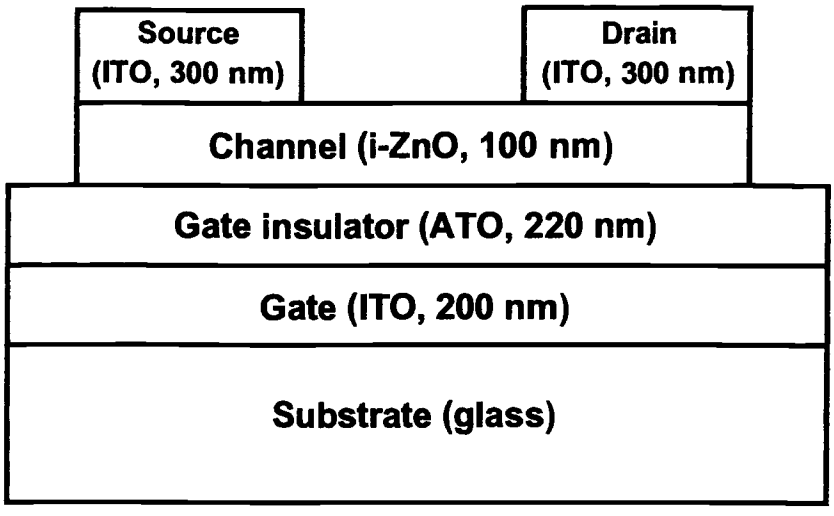

Figure 5.2: The typically employed TFT device structure (structure 1).

The ZnO channel and ITO source/drain electrode films are deposited via ion beam sputtering (Section 3.1.2) in 10^{-4} Torr of Ar/O_2 (80%/20%); the substrate is unheated during deposition. Shadow masks are used to pattern the ZnO channel and ITO source/drain electrodes. A 300°C RTA in Ar immediately prior to both the ZnO and ITO depositions serves to remove adsorbed contaminants from the exposed surface, yielding a noticeable improvement in film quality (particularly for ITO films). After deposition of the ZnO layer, a rapid thermal anneal (RTA) (typically 600 to 800°C in O_2) is employed to increase the ZnO channel resistivity, to improve the

electrical quality of the ATO / ZnO interface, and to enhance the crystallinity of the ZnO layer. Following deposition of the ITO source/drain electrodes, a 300°C RTA in O_2 is employed to improve the transparency of the ITO layer.

The choice of ambient accompanying the ZnO RTA has a smaller effect on TFT characteristics than might be expected. Although a thorough investigation of the effect of annealing ambient on device characteristics has not been carried out, characterization of several devices fabricated using Ar rather than O_2 during the ZnO RTA yields results quite similar to those obtained for analogous devices employing the typical O_2 RTA. As discussed in Section 2.2.1, ZnO conductivity is enhanced by an oxygen-deficient stoichiometry, so that an O_2 RTA is expected to serve as an important process step in attaining an insulating ZnO channel region. The ZnO RTA temperature, on the other hand, is perhaps the most important process step in establishing TFT characteristics. As discussed in Section 5.2.2, drain current saturation requires that the ZnO RTA be carried out at 700°C or higher (in either Ar or O_2). Although the mechanism responsible for this improvement in device characteristics has not yet been directly established, the most likely explanation is that a temperature of 700°C or higher is necessary to substantially crystallize the as-deposited ZnO layer, with a concomitant improvement in electrical transport and field-effect control of space charge in the ZnO channel.

The source/drain contacts to the ZnO channel can alternatively be made by selectively doping the source/drain regions of the ZnO channel. This was verified by depositing a thin (~5 nm) ITO layer using the source/drain shadow mask prior to depositing the ZnO channel layer; a high temperature (~600 to 700°C) RTA following the ZnO deposition is used to diffusion-dope the ZnO, forming n-ZnO source/drain regions. In a third variation of the TFT structure, the ITO source/drain electrodes are deposited prior to the ZnO channel layer; the ZnO channel layer is deposited conformally over the ITO source/drain electrodes and the channel region. Similar electrical characteristics are exhibited by each of these structures. Structure 1 (Fig. 5.2) is

preferable as it allows high temperature processing of the ZnO channel layer prior to deposition and low temperature processing of the ITO source/drain contacts.

Two shadow mask sets with different width-to-length ratios are used for TFT fabrication. The first (mask set 1) yields a channel width and length of 6200 μm and 3100 μm, respectively, for a width-to-length ratio of 2:1; the source/drain contact dimensions are 6200 μm x 6200 μm. The second (mask set 2) yields a channel width and length of 15000 μm and 1500 μm, respectively, for a width-to-length ratio of 10:1; the source/drain contact dimensions are 15000 μm x 1500 μm.

5.2 Electrical characterization

5.2.1 Energy band considerations

Figure 5.3 presents an equilibrium (zero bias) energy band diagram through the source (drain) electrode of a TFT fabricated according to structure 1 (Fig. 5.2). Note that, as discussed in Section 4.2.1, the ITO source electrode provides excellent electron injection into the i-ZnO channel layer.

The ATO layer is depicted as Al_2O_3 only (alternating TiO_2 layers are not indicated); since the ATO is capped on either end by an Al_2O_3 layer, it is the ZnO/Al_2O_3 interface that is important from the point of view of TFT operation, while the TiO_2 layers modify the dielectric constant and breakdown voltage of the ATO layer as a whole. The bandgaps of ITO, ZnO, and Al_2O_3 are 3.6 eV [55], 3.3 eV [58], and 9.5 eV [115], respectively. The band alignments at the ZnO / Al_2O_3 and Al_2O_3 / ITO interfaces are drawn somewhat arbitrarily; as long as the energy barrier is large enough to block electron injection into the Al_2O_3 gate insulator, the precise magnitude of the barrier is not important.

The equilibrium (zero bias) energy band diagram through the channel of a TFT fabricated according to structure 1 (Fig. 5.2) is shown in Fig. 5.4. Again, the band

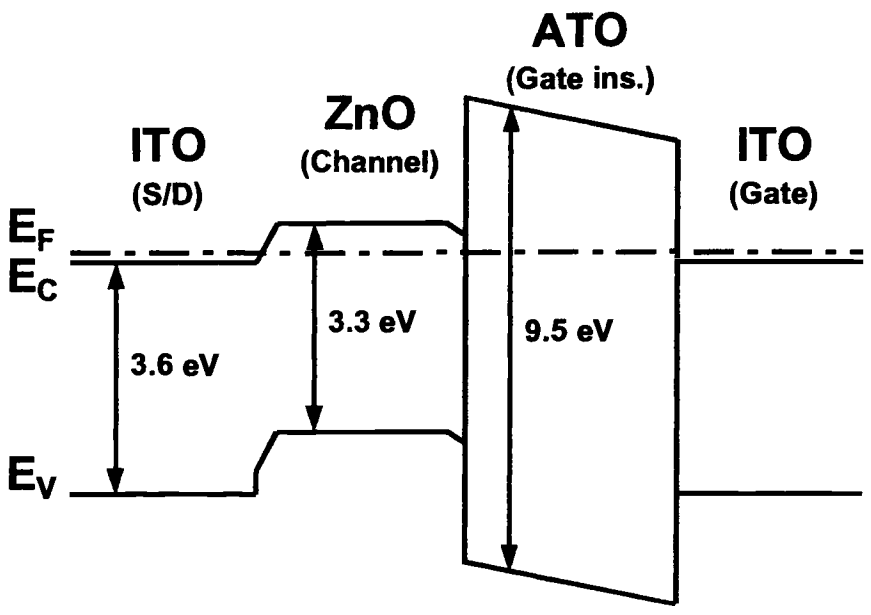

Figure 5.3: Equilibrium energy band diagram vertically through the source (drain) electrode of a TFT fabricated according to structure 1 (Fig. 5.2).

alignments at the ZnO / Al_2O_3 and Al_2O_3 / ITO interfaces as well as the band bending at the exposed ZnO surface are somewhat arbitrary.

5.2.2 DC current-voltage characteristics

Figure 5.5 shows the I_D-V_{DS} curves for a TFT fabricated according to structure 1 (Fig. 5.2), using mask set 2 (with a width-to-length ratio of 10:1), and employing 700°C (O_2) and 300°C (O_2) RTA cycles after the ZnO channel (100 nm) and ITO source/drain (300 nm) layer depositions, respectively. The corresponding log(I_D)-V_{GS} and log($|I_G|$)-V_{GS} characteristics are portrayed in Fig. 5.6.

Before proceeding with a discussion of Figs. 5.5 and 5.6, a brief comment is in order regarding measurement methodology. Transistor I-V characteristics are typically obtained using a curve tracer, whereas results reported herein employ a true DC measurement setup (a picoammeter with dual integrated DC voltage sources) and a

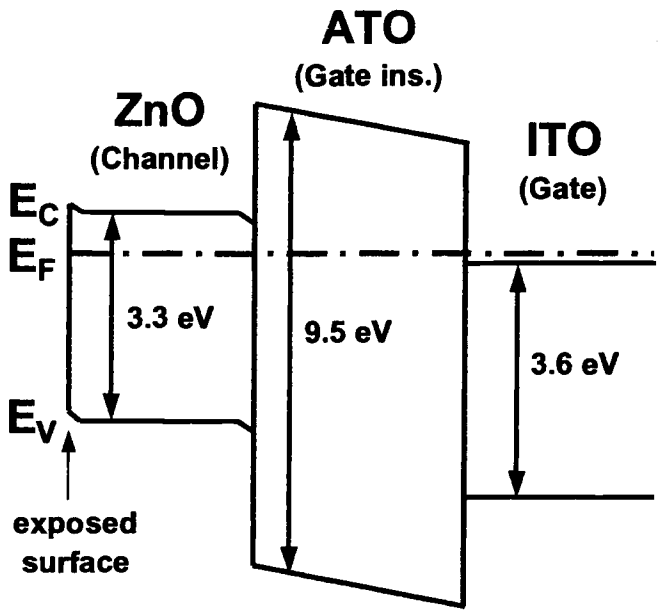

Figure 5.4: Equilibrium energy band diagram vertically through the channel region of a TFT fabricated according to structure 1 (Fig. 5.2).

relatively long settling time (e.g. ~10 seconds or longer) for each data point. The capacitance of these TFTs is much larger than that of a typical FET (as a consequence of the large device dimensions employed), so that a typical 60 Hz curve tracer drain voltage sweep is far too rapid to yield DC I_D-V_{DS} characteristics. In the TFT structure portrayed in Fig. 5.2, the gate completely overlaps the drain and source (in addition to the channel), so that the total gate capacitance for the TFT with I-V characteristics portrayed in Figs. 5.5 and 5.6 is ~30 nF. The maximum frequency at which the drain voltage can be switched (with no load capacitance, e.g. as in a curve tracer measurement) can be roughly estimated as

$$f_{max} \approx \frac{I_D^{avg}(V_{GS})}{2C\Delta V_{DS}}, \tag{5.1}$$

where V_{GS} is the gate voltage, $I_D^{avg}(V_{GS})$ is the average drain current (across the drain voltage sweep range) at a given gate voltage, C is the gate capacitance, and ΔV_{DS} is the change in drain voltage. Equation 5.1 is obtained by calculating the time

required to charge the gate capacitance to the maximum drain voltage (assuming a constant current equal to I_D^{avg}), and realizing that the time required to charge and then discharge the gate capacitance (i.e. one measurement cycle) is twice this value; the maximum frequency is equal to the inverse of the time required for one measurement cycle.

Table 5.1: Approximate maximum drain voltage switching frequency (with no load capacitance, e.g. as in a curve tracer measurement), estimated using Eq. 5.1, for the TFT with I-V characteristics portrayed in Figs. 5.5 and 5.6 (ΔV_{DS} and C are 40 V and 30 nF, respectively).

V_{GS} (V)	I_D^{avg} (μA)	f_{max} (Hz)
10	1.4	0.6
20	8.6	3.6
30	25	10.5
40	52	21.8

Table 5.1 estimates the maximum frequency at which the drain voltage can be swept to obtain DC current-voltage characteristics such as those illustrated in Figs. 5.5 and 5.6. Although this is admittedly a rough approximation, it is clear that a typical 60 Hz curve tracer measurement is not appropriate for DC I-V characterization of these TFTs. Finally it should be noted that, although the frequencies estimated in Table 5.1 are too small for practical application, a reduction in device dimensions acts to directly increase the maximum operating frequency (due to a reduction in gate capacitance). A reduction of the channel width and length to 150 μm and 15 μm, for example, would increase the maximum frequency values estimated in Table 5.1 by four orders of magnitude.

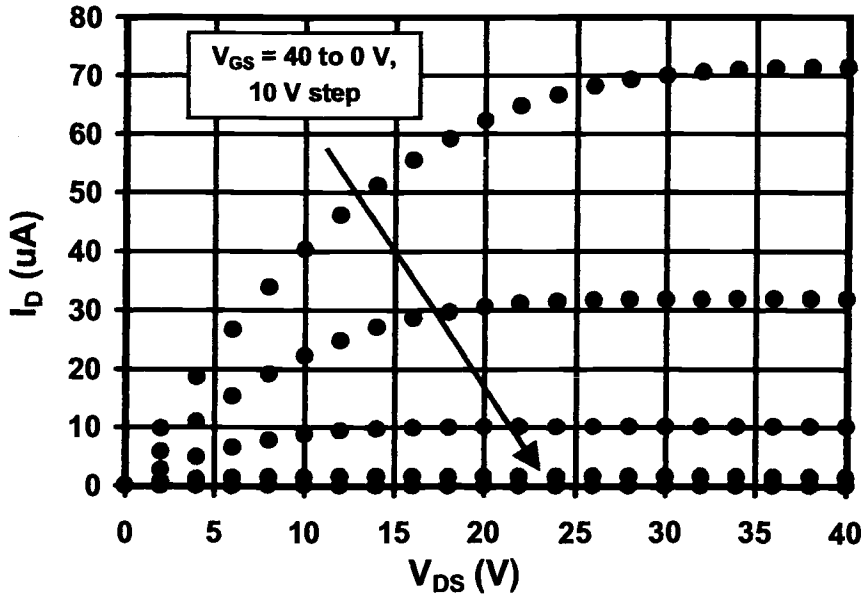

Figure 5.5: I_D-V_{DS} characteristics for a TFT fabricated according to structure 1 (Fig. 5.2), using mask set 2 (with a width-to-length ratio of 10:1). A 10 second settling delay is allowed at each point before taking a current measurement.

Returning to Figs. 5.5 and 5.6, note that this device exhibits "hard" saturation, indicating that the entire thickness of the i-ZnO channel can be depleted of free electrons. The TFT operates as an n-channel enhancement mode device; a positive gate voltage is required to induce a conducting channel, and channel conductivity increases with increasing positive gate bias. Figure 5.6 indicates a maximum drain current on-to-off ratio of $\sim 10^7$. The gate leakage current magnitude is also quite reasonable; since gate leakage current scales directly with gate area (while the drain current is not affected by absolute device dimensions for a given width-to-length ratio) the gate leakage current for a device of reduced dimensions appropriate for practical application is expected to be quite small.

The experimentally extracted effective mobility and saturation mobility, μ_{eff} and μ_{sat}, along with the corresponding threshold voltage estimates, V_T, for this device are displayed and discussed in Section 3.3.2 (Fig. 3.4). The estimated channel

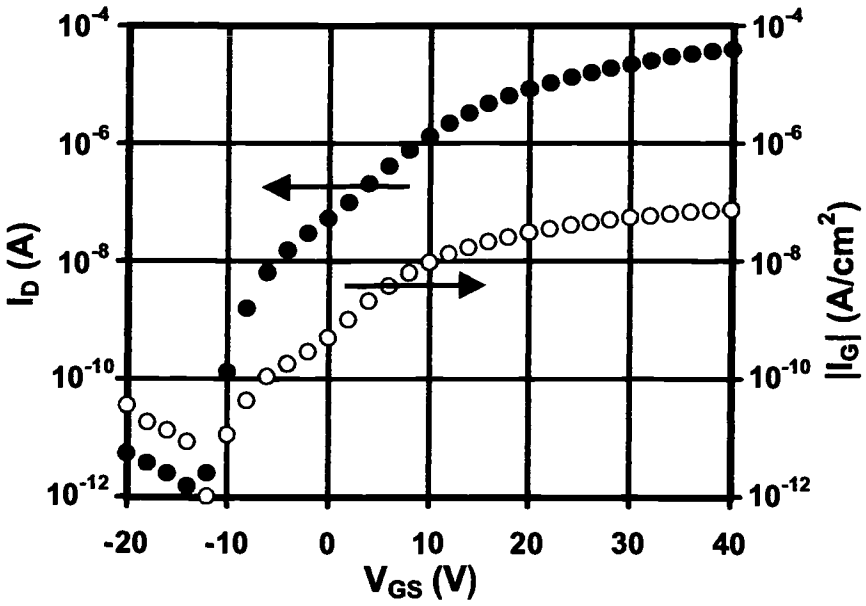

Figure 5.6: log(I_D)-V_{GS} and log($|I_G|$)-V_{GS} characteristics for a TFT fabricated according to structure 1 (Fig. 5.2), using mask set 2 (with a width-to-length ratio of 10:1). A 90 second settling delay is allowed at each point before taking a current measurement.

mobility and threshold voltage are 0.35 to 0.45 cm^2/V s and 10 to 15 V, respectively. Devices fabricated using the same process and employing mask set 1 (with a width-to-length ratio of 2:1) exhibit quite similar drain current characteristics (scaled as expected by their relative width-to-length ratios) and extracted mobility and threshold voltage. The estimated threshold voltage can be used to approximate the ZnO / ATO interface trap density according to

$$D_{it} = \frac{\epsilon_{ins} V_T}{q t_{ins}}, \tag{5.2}$$

where ϵ_{ins} is the gate insulator dielectric constant, q is the electron charge, and t_{ins} is the gate insulator thickness; the resulting ZnO / ATO interface trap density is ~2.75 to 4.15 $\times$ 10^{12} cm^{-2}. Equation 5.2 assumes that the TFT channel space charge is located exactly at the channel / gate insulator interface.

Despite this apparently successful estimation of threshold voltage, Fig. 5.6 shows measurable channel current for gate voltages as low as -10 V, far below the estimated threshold voltage obtained in Section 3.3.2 (10 to 15 V). This effect is attributed to a combination of typical pre-threshold interface channel current and residual bulk conductivity due to a non-negligible free electron concentration in the ZnO layer. Since this TFT structure employs source and drain contacts with the same conductivity type as the channel layer, there is not a reverse biased pn junction at the drain acting to suppress current flow through the channel layer bulk, as there is in a conventional MOSFET structure; the channel layer bulk acts as an alternate current path in parallel with the interface channel. Thus, the TFT can be treated as exhibiting two independent threshold voltages, one established by channel formation ($\sim$10 to 15 V) and the other established by depletion of the channel layer bulk ($\sim$-10 to -5 V).

The process employed in fabricating the device discussed above (with current-voltage characteristics depicted in Figs. 5.5 and 5.6) appears to be near the optimal process from an overall device performance perspective. In addition to demonstrating prototypical n-channel, enhancement mode TFT operation, this device does not exhibit significant variation of drain current with time or extended transient response with changing bias (as observed with alternate fabrication processes). The ZnO channel RTA temperature appears to exert the strongest effect on transistor electrical characteristics. If the ZnO channel RTA is carried out at a temperature of 600°C or lower (in either O_2 or Ar), the drain current saturation apparent in Fig. 5.5 is no longer observed, although some degree of gate-controlled modulation of the channel conductance is retained for ZnO RTA temperatures as low as 300°C. Figure 5.7 shows a typical set of I_D-V_{DS} characteristics for a TFT exhibiting non-saturating drain current; the device is fabricated according to structure 1 (Fig. 5.2), using mask set 2 (with a width-to-length ratio of 10:1), and employing 600°C (Ar) and 300°C (O_2) RTA cycles after the ZnO channel and ITO source/drain depositions. The ZnO

channel and ITO source/drain layer thicknesses are ~90 nm and ~230 nm, respectively.

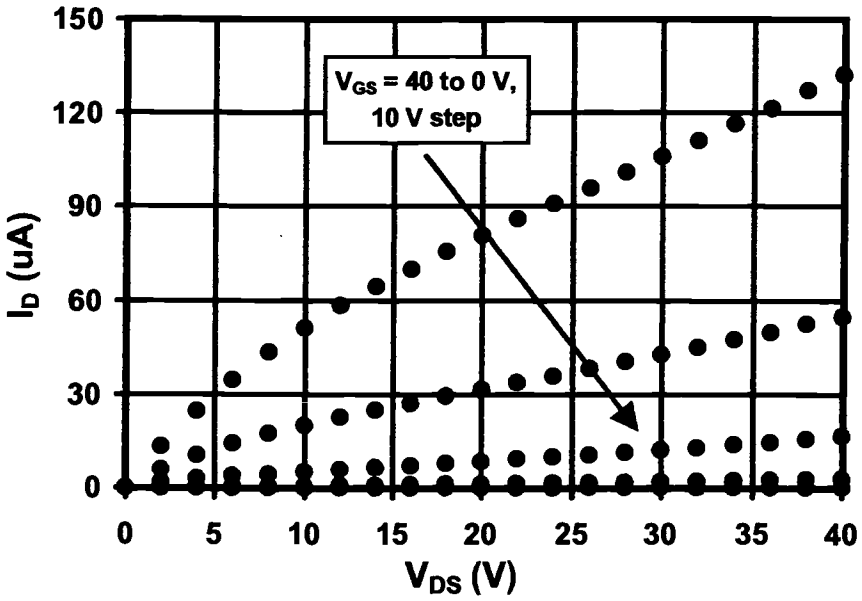

Figure 5.7: I_D-V_{DS} characteristics for a TFT fabricated according to structure 1 (Fig. 5.2), using mask set 2 (with a width-to-length ratio of 10:1). A 20 second settling delay is allowed at each point before taking a current measurement.

Additional improvement in TFT characteristics due to improved ZnO / ATO interface quality and enhanced ZnO layer crystallinity might reasonably be expected for ZnO channel RTA temperatures higher than 700°C, however the glass substrate is also expected to exhibit progressively worse softening and warping during the RTA cycle as the temperature is increased. Figure 5.8 portrays the I_D-V_{DS} curves for a TFT fabricated according to structure 1 (Fig. 5.2), using mask set 2 (with a width-to-length ratio of 10:1), and employing 800°C (O_2) and 300°C (O_2) RTA cycles after the ZnO channel (100 nm) and ITO source/drain (300 nm) layer depositions, respectively. Figure 5.9 shows the corresponding experimentally extracted effective mobility and

saturation mobility, μ_{eff} and μ_{sat}, along with the corresponding threshold voltage estimates, V_T. The threshold voltage (~10 to 20 V) is similar to that obtained with a 700°C ZnO channel RTA, however the mobility is significantly higher (~1 to 2.5 cm^2/V s). Along with this improvement in mobility, however, these devices exhibit a reduced degree of stability and reliability as compared to those employing a 700°C ZnO channel RTA; this is tentatively attributed to substrate softening-induced strain and damage to the TFT films, as discussed above.

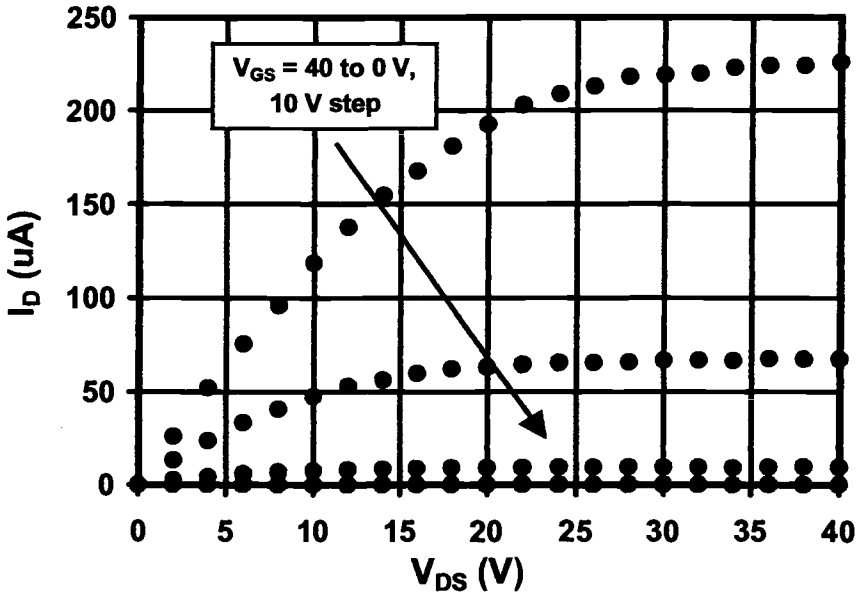

Figure 5.8: I_D-V_{DS} characteristics for a TFT fabricated according to structure 1 (Fig. 5.2), using mask set 2 (with a width-to-length ratio of 10:1) and employing an 800°C (O_2) ZnO RTA. A 10 second settling delay is allowed at each point before taking a current measurement.

The gate insulator (ATO) layer tends to be electrically shorted for approximately one in three as-fabricated devices, and is typically able to sustain a maximum voltage during testing of ~40 to 60 V. Since the ATO layer is generally quite reliable

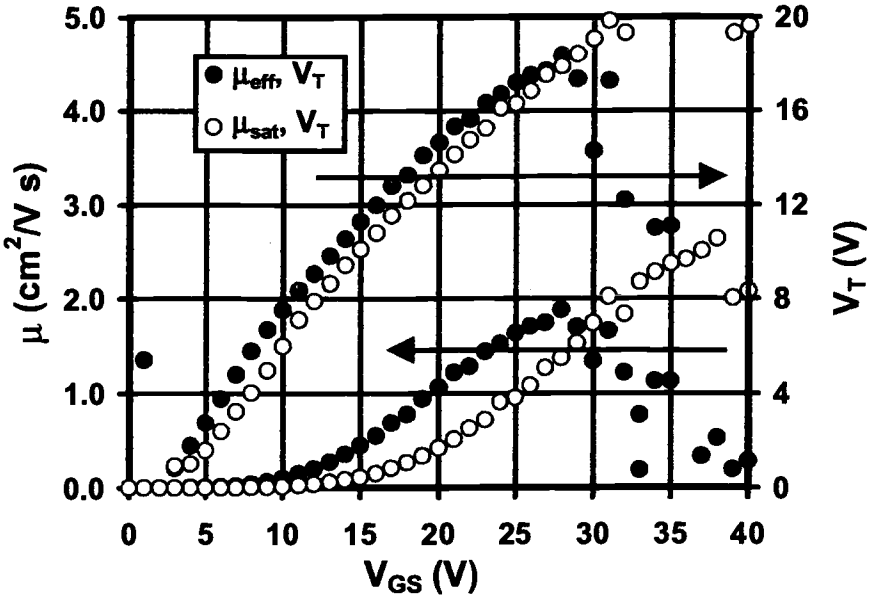

Figure 5.9: Experimentally extracted effective mobility, μ_{eff} ($I_D(V_{GS})$ measured with V_{DS} = 1 V), and saturation mobility, μ_{sat} ($I_D(V_{GS})$ measured with $V_{DS} = V_{GS}$), along with the corresponding threshold voltage estimates, V_T, for a TFT fabricated according to structure 1 (Fig. 5.2), using mask set 2 (with a width-to-length ratio of 10:1) and employing an 800°C (O_2) ZnO RTA. A 10 second settling delay is allowed at each point before taking a current measurement.

and typically exhibits a breakdown voltage of ~100 V or more, this diminished degree of reliability must be related to some aspect of the TFT fabrication process. The ion beam sputtering process seems a likely candidate, as some degree of exposure to high-energy ions and electrons certainly takes place. Attempts to reduce such effects by varying the physical orientation of the substrate during deposition do not have any noticeable effect. Further investigation is required to establish the nature of this apparent degradation of the ATO layer.

As the TFT structure is made up entirely of oxide films, it is no surprise that the device properties appear to be quite insensitive to extended atmospheric exposure. Although a detailed aging study has not been accomplished, no significant change in electrical properties is observed for devices exposed to atmosphere for as long as three

to four months; furthermore, direct exposure to water appears to have little effect on device characteristics.

Finally, note that although the voltages required for TFT operation are rather large as compared to those typically used with conventional FETs, the operating voltages can easily be reduced by decreasing the gate insulator thickness. The current insulator thickness of ~220 nm could certainly be reduced by a factor of four, and perhaps by as much as a factor of ten or more. Thus, the rather large operating voltages required for the devices realized here could be easily reduced to levels appropriate for practical applications.

5.2.3 Capacitance characteristics

Capacitance measurements are performed according to the C-(V,f) technique discussed in Section 3.3.3; notation used throughout this section is based upon that presented in Section 3.3.3. Figure 3.6 presents a C-(V,f) contour plot using the test structure depicted in Fig. 3.5, with an injector area (A_{inj}) of ~0.08 cm^2 and a semiconductor area (A_{sc}) of ~0.18 cm^2. The injector and semiconductor layers are ITO (300 nm) and ZnO (100 nm); the ZnO and ITO layer depositions are followed by 700°C (O_2) and 300°C (O_2) RTA cycles, respectively (the process is identical to that used to fabricate the TFT with DC I-V characteristics depicted in Figs. 5.5 and 5.6). Figures 5.10 and 5.11 portray the corresponding capacitance-voltage (C-V) and capacitance-frequency (C-f) plots.

Note the capacitance plateaus at C_{ins}^{sc} (forward bias [$\gtrsim$10 V], low frequency [$\lesssim$ 1 kHz]), C_{ins}^{inj} (remainder of the forward bias region), and $C_{sc,ins}^{inj}$ (reverse bias), as discussed in Section 3.3.3, with capacitance values of ~7.8, 3.5, and 2.3 nF, respectively. The ratio of C_{ins}^{sc} (Eq. 3.41) to C_{ins}^{inj} (Eq. 3.42), ~2.25, is equal to the ratio of the ZnO and ITO areas, as expected. Equation 3.41 (or 3.42) yields a dielectric constant of ~11 ϵ_0 for the ATO layer (assuming the ATO thickness to be exactly 220 nm, as specified by Planar Systems). Equation 3.43 can be used to estimate the dielectric

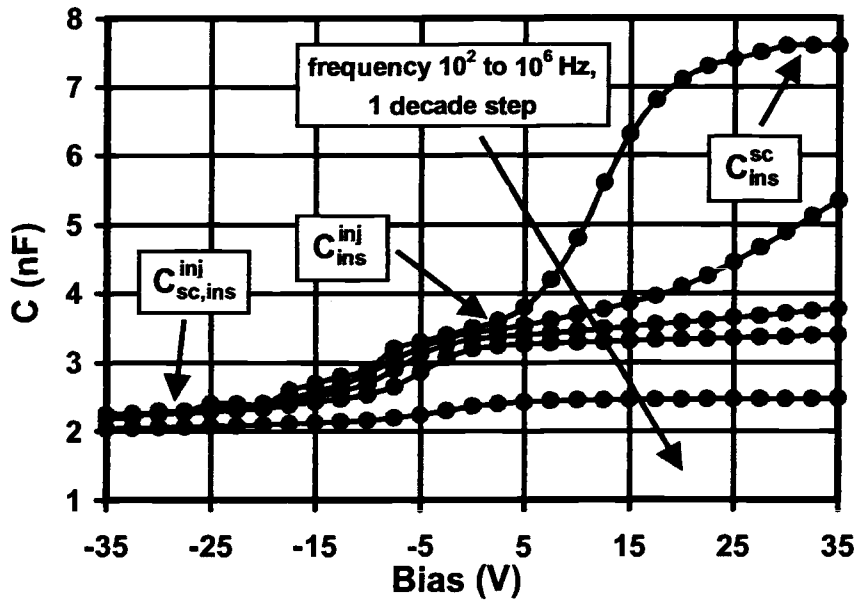

Figure 5.10: Capacitance-voltage characteristics corresponding to the contour plot depicted in Fig. 3.6 for frequencies of 100 Hz, 1 kHz, 10 kHz, 100 kHz, 1 MHz, and 10 MHz. Capacitance plateau notation is defined in Section 3.3.3.

constant of the ZnO layer, yielding a value of ~9 to 10 ϵ_0, in agreement with the expected value of 9.0 ϵ_0. [57] The high frequency capacitance roll off is attributed to the ITO injector layer lateral resistance from the physical point contact throughout the remainder of the injector layer area, R^{lat}_{inj} (Fig. 3.9c). The reverse bias high frequency roll off at ~1 MHz indicates an effective resistance of ~400 Ω; this is a reasonable value, since the 300°C (O_2) RTA employed to improve the transparency of the ion beam sputtered ITO layer tends to yield a modest reduction in conductivity.

As discussed in Section 3.3.3 (Eq. 3.44), the ZnO layer carrier concentration can be estimated from the change in bias voltage (ΔV_{depl}) required to attain depletion. For $\Delta V_{depl} \approx 10$ V (Fig. 5.10), the resulting ZnO carrier concentration is ~2.75 × 10^{17} cm^{-3}, corresponding to a resistivity and sheet resistance of ~2.3 Ω cm and 230 kΩ/□, respectively (assuming a mobility of ~10 cm^2/V s). However, as discussed in Section 3.3.3, this estimate applies only to the ZnO region directly beneath the

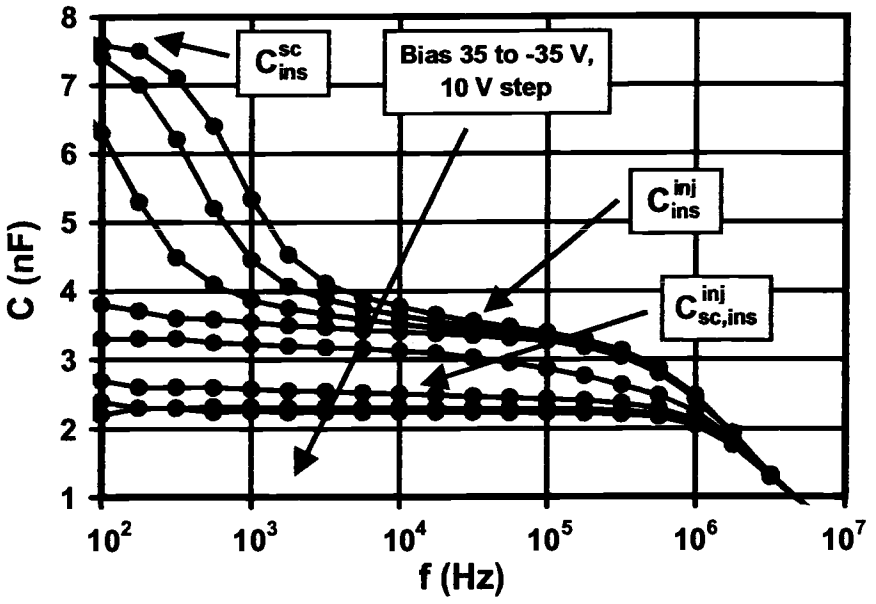

Figure 5.11: Capacitance-frequency characteristics corresponding to the contour plot depicted in Fig. 3.6 for bias voltages of -35, -25, -15, -5, 5, 15, 25, and 35 V. Capacitance plateau notation is defined in Section 3.3.3.

ITO layer. Since exposed ZnO surfaces are strongly affected by adsorbed oxygen (as discussed in Section 2.2.2), it is quite reasonable to assume that the exposed ZnO region (i.e. the channel region in the TFT structure) does indeed contain far fewer carriers than the ITO-covered region. This might occur due to depletion resulting from negative surface charge or as a result of more complex interactions occurring during deposition and processing of the ITO layer.

Further evidence that the carrier concentration is different in the exposed ZnO region is provided by the I_D-V_{GS} characteristics presented in Fig. 5.5, which indicate a channel resistance of ~700 kΩ to 300 kΩ (for gate voltages from 10 V to 30 V and small drain voltage) for a TFT fabricated using the same process as employed for the C-(V,f) structure presently under consideration. Since the width-to-length ratio for this TFT is 10:1, this channel resistance can be compared to one-tenth of the sheet resistance estimated above based on the ZnO layer carrier concentration

estimate (assuming, for the moment, that this estimate does indeed apply to the exposed ZnO layer region), yielding a resistance of ~23 kΩ. Since this resistance is more than an order of magnitude smaller than the experimental TFT channel resistance, it is clear that the exposed ZnO region does not exhibit such a large carrier concentration. Furthermore, Figs. 3.6 and 5.10 clearly show that the maximum low frequency capacitance plateau is not immediately observed when a forward bias is applied so as to undeplete the ZnO layer. Rather, a forward bias approximately equal to the estimated TFT threshold voltage (~10 to 15 V) must be applied before the capacitance increases from its intermediate, undepleted value, C_{ins}^{inj}, to the maximum plateau, C_{ins}^{sc}, (in particular, note the 100 Hz curve in Fig. 5.10). The lateral bulk resistance of the exposed ZnO layer, R_{sc}^{lat}, is clearly much larger than that of the induced channel, R_{chan}, so that the ZnO layer carrier concentration estimated from C-(V,f) data for the ZnO region beneath the ITO layer is indeed significantly larger than that of the exposed ZnO region. Conductivity measurements for similarly processed ZnO films also support this conclusion, indicating extremely large values for resistivity (i.e. $\rho \gtrsim 10^8$ Ω cm). These results indicate that the TFT source and drain regions retain a much higher conductivity than the channel region, so that electron injection and extraction is easily and efficiently accomplished while simultaneously achieving a highly insulating channel region.

5.3 Optical characterization

Figure 5.12 shows the optical transmission spectrum of a typical transparent TFT. The ZnO and ITO thicknesses are 100 and 300 nm, respectively; the ZnO and ITO RTA cycles are 700°C (O_2) and 300°C (O_2). The average optical transmission in the visible region of the electromagnetic spectrum is ~90%. The source/drain ITO layer is responsible for much of the absorption witnessed in Fig. 5.12; the channel region, without the ITO source/drain contacts, exhibits even higher transparency.

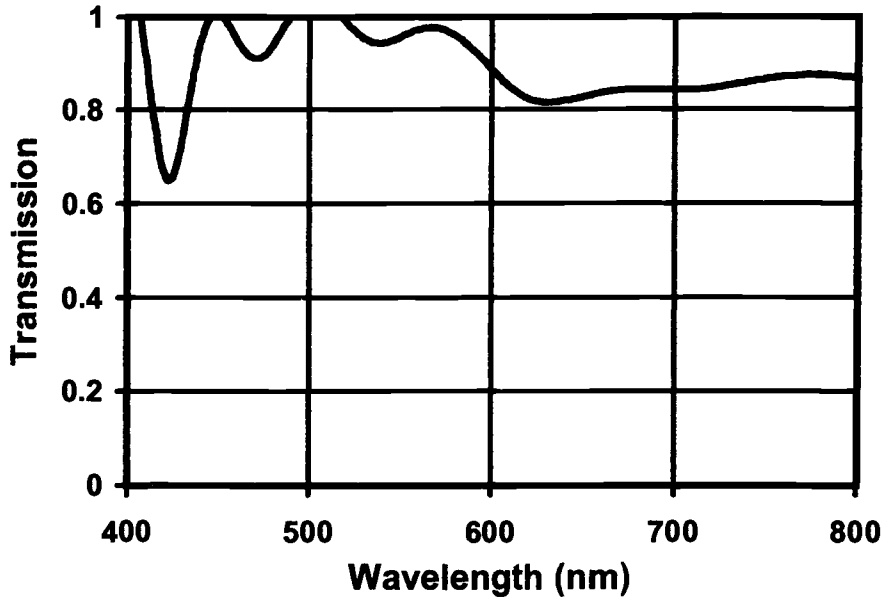

Figure 5.12: Optical transmission spectrum of the source/drain region of a transparent TFT. The ZnO channel and ITO source/drain thicknesses are 100 and 300 nm, respectively.

Although the light sensitivity of these devices has not been studied in detail, several general traits are apparent. Exposure to typical ambient light intensity has little to no effect on current-voltage characteristics; as expected, the channel light sensitivity decreases with decreasing ZnO channel layer thickness. A device fabricated with a channel thickness of ~15 to 20 nm and employing 700°C (O_2) and 300°C (O_2) RTA cycles for the ZnO and ITO layers, respectively, exhibits an increase in drain current due to ambient light exposure of ~1% for V_{DS} and V_{GS} equal to 40 V (the current-voltage characteristics of this device are essentially the same as those portrayed in Fig. 5.5, for an analogous device with a 100 nm ZnO channel layer).

Furthermore, the ZnO films used in the TFT structure exhibit the persistent photoconductivity (PPC) discussed in Section 2.2.2 to varying degrees, depending upon the fabrication process employed. Although strong sensitivity to ultraviolet (UV) radiation is not desirable for many TFT applications, it is possible that this

anomalous effect could be creatively applied to yield beneficial results. A series of papers by Coldren, Davis, and others reports the use of ZnO films in acoustic surface wave (ASW) memory devices; field effect action on the ZnO across a SiO_2 insulator layer is combined with UV illumination to yield charge storage memory with retention times as long as a day. [45, 116, 117, 118, 119, 120, 121] The results of a cursory investigation indicate that the TFTs reported in this chapter exhibit a similar effect; a persistent change in channel conductance can be induced by simultaneous UV illumination and the application of a gate bias. This effect is undoubtedly related to the anomalous PPC exhibited by ZnO (Section 2.2.2), with space charge at exposed surfaces and grain boundaries modified by adsorption, chemisorption, and photodesorption of oxygen. Further investigation is required to fully understand the mechanism responsible for this behavior and to evaluate its potential for use in practical applications.

5.4 Conclusions

This chapter presents the fabrication and characterization of novel, highly transparent ZnO-based thin film transistors (TFTs). The average transmission in the visible region is ~90% or higher, far better than has been attained in previously reported semi-transparent transistors (Section 2.4.2).

Current-voltage measurements indicate fairly typical n-channel, enhancement mode behavior. Rather large operating voltages (~40 V) are employed. However, these voltages are directly dependent on the gate insulator thickness which can certainly be reduced by a factor of four or more, yielding a much more desirable range of operation. Excellent drain current saturation is obtained, and the drain current on-to-off ratio is $\sim 10^7$. The experimentally extracted threshold voltage and channel mobility are ~10 to 20 V and ~0.3 to 2.5 cm^2/V s, respectively (mobility increases with ZnO annealing temperature). Although gate-controlled modulation of the chan-

nel conductance is maintained for ZnO annealing temperatures as low as 300°C, drain current saturation requires a temperature of 700°C or higher.

The capacitance-(voltage, frequency) [C-(V,f)] characterization technique (described in Section 3.3.3) is employed to further elucidate TFT electrical characteristics; this section also serves to verify the validity of the C-(V,f) method. C-(V,f) measurements indicate that the ZnO source/drain regions (covered by the ITO source/drain contacts) exhibit a carrier concentration and conductivity much larger than that of the ZnO channel region (where the ZnO surface is exposed).

Although the light sensitivity of these devices has not been studied in detail, several general traits are observed. Exposure to a typical ambient light intensity and spectrum has little to no observable effect on drain current characteristics. Direct exposure to ultraviolet (UV) radiation has a much stronger effect, due to the creation of electron-hole pairs by UV photons with energy greater than the ZnO bandgap. Light sensitivity is reduced by decreasing the ZnO channel layer thickness; TFTs with a channel layer thickness of ~20 nm exhibit drain current characteristics nearly identical to those observed for devices with a 100 nm channel, while light sensitivity is greatly reduced.

6. CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

6.1 Conclusions

The goal of this thesis has been, in large part, to provide an initial demonstration of the feasibility of constructing active electronic devices based upon transparent material systems. This goal has been achieved, most strikingly, in the fabrication of ZnO-based thin film transistors (TFTs) with an average transparency above ~90% throughout the visible portion of the electromagnetic spectrum; this is, in fact, the first report of the fabrication of a highly transparent transistor. These transistors exhibit prototypical n-channel, enhancement mode TFT operation, confirming that conventional electronic device behavior can, indeed, be realized using transparent material systems.

This thesis has also focused on electrical characterization of transparent electronic devices. A novel technique for characterization of carrier injection into an insulator and of interface channel formation, the capacitance-(voltage, frequency) [C-(V,f)] technique, is proposed; the C-(V,f) method is employed in characterization of ZnO-based TFT structures. A detailed electrical characterization study of $CuYO_2$ / ZnO / ITO p-i-n heterojunction diodes is carried out; this effort represents the first such detailed study of a transparent or semi-transparent diode. Electrical characterization of these diodes yields insight into the likely operational mechanisms responsible for the behavior of previously reported transparent and semi-transparent diodes, for which electrical characterization has generally been lacking. The results of this characterization study indicate that the development of transparent diodes should focus on p-i-n structures.

Finally, several theoretical issues pertinent to experimental results presented herein are elaborated in some detail. In particular, energy band analysis of the de-

generate semiconductor / insulator heterojunction yields insight into the mechanisms underlying charge injection into an insulator. Although this analysis relies upon the direct application of basic heterojunction energy band theory, the results are somewhat novel, and yield important implications for the analysis of heterojunctions where carrier injection into an insulator is achieved.

6.2 Recommendations for future work

As is the case for any research effort, the completion of this thesis has left many questions unanswered. The purpose of this section is to summarize potential directions for further research based upon that presented in this thesis.

6.2.1 Transparent thin film transistors

The fabrication of highly transparent ZnO-based TFTs represents a significant achievement, with considerable technological potential. As such, further exploration is certainly warranted. Most obviously, the device structure and fabrication process reported herein should be optimized. A careful study of device characteristics for a series of channel layer thicknesses would be quite useful; both electrical characteristics (e.g. threshold voltage) and light sensitivity should improve with decreasing channel thickness, as indicated by preliminary results reported in this thesis.

The TFT annealing process is extremely important in establishing device performance; optimization of the annealing process is likely to yield improved device performance. Furthermore, if optimal performance can be attained without exceeding processing temperatures of ~500°C, the value of this technology is greatly increased from a manufacturing perspective. In addition to rapid thermal annealing, other annealing methodologies (e.g. furnace annealing and hydrothermal annealing) should be explored. The annealing gas ambient provides an additional parameter whose effects on device performance and stability should be explored. Substrate heating during

ZnO deposition should also be explored as an alternate route to achieving enhanced crystallinity and device performance at moderate processing temperatures.

The TFT gate insulator (ATO) sustains damage at some point in the TFT fabrication process, yielding unexpected insulator instability and a relatively low breakdown voltage. The cause of this apparent insulator damage should be established and corrected; since insulator damage is tentatively attributed to high energy ions and electrons in the ion beam sputtering process, the fabrication of an identical structure using an alternate deposition method (e.g. RF sputtering) might yield a simple resolution to this issue.

Alternate TFT gate insulator materials should be explored in the ZnO-based TFT structure. Perhaps the most obvious choice is Al_2O_3, since the Al_2O_3 cap layers on the ATO insulator layer presumably act to establish the chemical and electronic nature of the TFT channel interface. Other potential insulator materials include SiO_2, Si_3N_4, and silicon oxynitride. The extent to which the insulator thickness can be reduced should also be investigated, since a reduction in insulator thickness corresponds to a direct reduction in TFT operating voltages.

Although the shadow mask patterning employed for TFT fabrication to date is quite attractive in the initial evaluation of candidate TFT material combinations, the ZnO-based structure exhibits sufficient promise as a viable technology that the time investment required to realize more sophisticated test structures is certainly warranted. This requires that a lithography methodology be developed to pattern, minimally, the ZnO layer. If doped ZnO is employed (in the place of ITO) for the gate, source, and drain electrodes, a single chemical etch process should suffice (with the gate insulator a blanket layer). With a lithography process in place, reasonable device dimensions can be attained; characterization of such devices should yield a better indication of practical performance parameters such as maximum operating frequency and transient switching characteristics.

Due to the sensitivity of the ZnO surface to ambient gases (particularly oxygen), passivation of the exposed ZnO surface should be explored as a route to the attainment of ZnO-based TFTs with long-term stability. In addition to protecting the ZnO surface from contamination and damage, such a passivation layer should establish well-defined and stable surface characteristics and suppress oxygen diffusion to and from the ZnO surface. Surface passivation should minimize the anomalously large persistent photoconductivity (PPC) often observed in ZnO, since this phenomenon is generally attributed to surface oxygen adsorption/photodesorption.

The ZnO persistent photoconductivity (PPC) effect should be investigated as a possible route to achieving an electrical/optical memory element. Gate-controlled modulation of ZnO channel charge provides an added degree of control in harnessing the ZnO PPC effect so as to obtain predictable and repeatable cycling behavior. Preliminary investigation indicates that PPC in the ZnO TFT channel is indeed influenced to some degree by the application of an appropriate gate voltage, although further work is required to establish the details of this interaction.

Finally, alternative material systems should be explored using a similar TFT structure and fabrication process, particularly in view of the fact that the simplicity of the TFT test structure and shadow mask patterning employed herein lends itself to a rapid and efficient development cycle. Therefore, although some degree of care should be employed in selecting potential material combinations, the best course of action probably consists of simply cycling through as many potential material combinations as possible in order to identify the most promising candidates for further development. Both p-channel and n-channel operation should be pursued; p-channel operation opens to door to complementary circuit applications. There are many potential channel materials that should be evaluated in the TFT structure. Potential n-channel materials include SnO_2, ZnS, SrS, and BaS; potential p-channel materials include NiO, Bi_2O_3, BaCuSF, and many of the delafossites (which can often be made much more transparent as insulators than as conductors). Note that, in many if

not all cases, attaining efficient electron or hole injection into the channel insulator may present a greater challenge than attaining a mobile carrier accumulation layer (channel).

6.2.2 Transparent diodes

Further transparent diode work should focus on p-i-n heterojunction structures, where one or both of the n- and p-type injectors exhibit efficient injection into the intermediate insulating layer. Rectification can be attained with either single or double injection. Double injection, however, opens the door to low voltage DC injection electroluminescence (EL), where electrons and holes injected at opposite ends of an insulating phosphor layer produce light output arising from radiative recombination.

6.2.3 Characterization

Since the capacitance-(voltage, frequency) [C-(V,f)] method was conceived quite late in the process of completing this thesis, its capabilities and limitations as a characterization technique have not been established, nor fully developed. The C-(V,f) method appears to be an attractive technique, as it lends itself readily to a rapid and efficient material system evaluation methodology. Perhaps most significantly, the characterization of charge injection into an insulator using this method can be accomplished using AC measurements; this allows the use of a test structure that offers a number of fabrication and material compatibility benefits. Further utilization of the C-(V,f) method, however, requires that it be more completely developed into an established characterization technique.

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