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Title: Lowpass and Bandpass Current-Mode Delta-Sigma DACs Employing Mismatch-Shaping.

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Richard Schreier

Abstract approved:

Delta-sigma modulators are currently a very popular technique for making high-resolution analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). These oversampled data converters have several advantages over conventional Nyquist-rate converters, including an insensitivity to many analog component imperfections, a simpler antialiasing filter and reduced accuracy requirements in the sample and hold. A recent development in the realm of delta-sigma-based ADC and DAC systems is the use of multilevel (as opposed to binary) quantization. This development owes its existence to the discovery of a variety of techniques which cause linearity errors of the embedded multilevel DAC to be attenuated in the frequency band of interest.

This thesis presents several methods for shaping the DAC element mismatch error and reducing the dynamic error in the band of interest. To demonstrate the effectiveness of the proposed algorithms, a current-mode unit element DAC is designed and used as a test bed. Both theoretical analysis and experimental results show that these methods can greatly attenuate the noise in the band of interest. The methods presented in this thesis will allow high performance, high-frequency wideband delta-sigma modulators to be constructed.

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Lowpass and Bandpass Current-Mode Delta-Sigma DACs Employing Mismatch-Shaping

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Lowpass and Bandpass Current-Mode Delta-Sigma DACs Employing Mismatch-Shaping

Chapter 1. Introduction

This thesis deals with the application of mismatch-shaped multibit DACs for delta-sigma modulators. The goal of the thesis is to introduce new mismatch-shaping algorithms and to verify their effectiveness in real systems. The knowledge gained will help to extend the application range of delta-sigma modulators.

1.1 Motivation

The increased use of digital signal processing in integrated circuits has driven the development of analog-to-digital and digital-to-analog converters (ADCs and DACs) [1] to serve as interfaces between the analog and digital domains.

Delta-sigma modulation [2] is currently a very popular technique for making high-resolution ADCs and DACs. These oversampled data converters have several advantages over Nyquist-rate converters, including an insensitivity to many analog component imperfections, a simpler anti-aliasing filter and reduced accuracy requirements in the sample-and-hold. Delta-sigma modulator circuits feature oversampling, noise-shaping and often one-bit quantization. Although the initial uses of delta-sigma modulators were in the audio field, the development of bandpass modulators opened up the application range to systems which convert intermediate-frequency (IF), or even radio-frequency (RF), analog signals directly to digital form. Examples of such systems include radar, personal communication systems and instrumentation.

Conventionally, delta-sigma modulators adopt one-bit quantization due to the inherent linearity of a one-bit DAC. However, multibit quantization can greatly improve

the performance of the modulator in terms of higher signal-to-noise ratio (SNR) and higher operating bandwidth [3]. Unfortunately, the DAC linearity required for these benefits to be realized is usually well beyond that which is practical and presents a major limitation to the use of multibit delta-sigma modulators. Nonetheless, several techniques have been presented which can avoid this limitation. In this thesis, one such method, mismatch-shaping, will be described in detail and applied to both lowpass and bandpass modulators.

Most delta-sigma modulators in production today are implemented by discrete-time circuits, with switched-capacitor (SC) circuits implementations being by far the most popular However, for high-speed applications where highly accurate sampling may not be available, continuous-time circuits offer several advantages. To exploit the advantage of multi-bit quantization in a continuous-time modulator, a new mismatch-shaping scheme needs to be developed which can deal with dynamic and static errors effectively.

These considerations provide the motivation for the investigation of several mismatch-shaping schemes, as well as the design and test of a current-mode unit element DAC to verify the proposed algorithms.

1.2 Thesis Outline

Chapter 2 provides an overview of the delta-sigma technique and the state of the art. Chapter 3 describes the principle of mismatch-shaping in detail and compares the proposed new algorithms with those already in existence. In Chapter 4 a current-mode unit-element DAC (UEDAC1) is tested to identify major error sources. The design of a second-generation unit element current-mode DAC (UEDAC2) is described in Chapter 5. Experimental results are illustrated in Chapter 6 which confirm the effectiveness of the schemes proposed in this thesis. Better performance in terms of linearity and speed has also

been achieved through the design of UEDAC2. Chapter 7 summarizes the thesis and gives directions for future work.

Chapter 2. Delta-Sigma Background

This chapter presents the material necessary to understand delta-sigma modulators in general and this thesis in particular. Starting with a brief review of analog-to-digital conversion, the discussion progresses to first-order, and then high-order delta-sigma modulators. Bandpass delta-sigma modulators are presented as generalizations of lowpass discrete-time modulators. The advantages of multi-bit quantization in delta-sigma modulators are covered, followed by a brief review of existing schemes for overcoming the linearity limitation of multi-bit quantization. A review of the state-of-the-art in delta-sigma converters concludes this chapter.

2.1 Analog-to-Digital Conversion

An analog-to-digital converter (ADC) [1] is a system that converts an analog quantity, such as voltage or current, into a digital quantity. A clock is used to sample the input signal and to initiate the conversion. Nyquist's sampling theorem states that the minimum sampling frequency $f_{s,min}$ should be at least two times the signal bandwidth f_B in order to make recovery of the signal possible. An anti-alias filter is required to remove components above $f_s/2$ which might otherwise alias into the signal band.

An ideal n-bit linear ADC has 2^n quantization steps. Assuming an input signal range of ± 1, the quantizer step height, or the value of the least-significant-bit, is $\Delta = 2/(2^n - 1)$. Assuming that Δ is small, the error e between the input analog quantity and the corresponding quantized value has the statistics of a random variable uniformly distributed over $[-\Delta/2, \Delta/2]$. Under these assumptions the mean-square value of e, i.e. the power of the error signal, is $\sigma_e^2 = \Delta^2/12$. The largest sine-wave signal which does not overload the ADC has an amplitude of 1 and a power of -3 dB. A simple calculation then

shows that the maximum signal-to-noise ratio (SNR) of an ideal n-bit linear ADC with a sine-wave input is therefore approximately $6n$ dB.

In a conventional Nyquist rate ADC or DAC (digital-to-analog converter), higher resolution is achieved by using smaller step sizes. However, small steps require the use of precisely-matched analog components. As a result, the practical limit with current (untrimmed) circuit techniques is about 11 bits of resolution. Trimmed circuits can achieve 16 or more bits of resolution, but are expensive. In a Nyquist rate ADC or DAC, precision analog circuits, such as high-gain op amps, linear integrators, etc., have no opportunity to exert their power because a complete conversion must be performed in every clock period. Delta-sigma modulation increases the sampling rate (above the Nyquist rate) to provide the freedom that allows the features of precision analog circuits to be exploited.

Oversampling [2] is simply the process of sampling faster than the Nyquist criterion requires. If the signal occupies the band from DC to f_B and the sampling rate is f_s, the oversampling ratio R is defined as $R = f_s/(2f_B)$. Oversampling eases the anti-alias filter design since a wide transition band is created by the increased separation between the signal band and its first alias. For an ADC with broadband quantization noise, oversampling also reduces the amount of in-band quantization noise. This allows the conversion to be more accurate than the resolution of the quantizer. Specifically, an increase in resolution of 0.5 bit results from each octave increase in the oversampling ratio. As the next section will show, delta-sigma modulation improves significantly on this trade-off.

2.2 First-Order Delta-Sigma Modulator

A first-order delta-sigma ($\Delta\Sigma$) converter (MOD1) [2], consisting of an analog integrator, a single-bit quantizer (comparator), a single-bit DAC and a digital decimation

filter, is shown in Figure 2.1. One may view the "delta" and "sigma" as referring to the analog operations in the system loop: subtraction of the fed back output signal from the input signal and accumulation (integration) of the differences. In order for the output of the integrator to be bounded, the DC component of the feedback must be exactly the same as that of the input signal. If this is true, the first-order converter has ideally unlimited resolution, at least for DC signals. The digital lowpass decimation filter removes the out-of-band noise and produces a high-resolution digital representation of the input.

The output of MOD1 in the z domain is

$$V(z) = z^{-1}U(z) + (1 - z^{-1})E(z) , \tag{2.1}$$

where V is a discrete-time binary-valued signal, U is a discrete-time continuous-amplitude signal and E is the quantization error [4]. According to Eq. (2.1), the quantization error is frequency-shaped by the function $H(z) = 1 - z^{-1}$. This *noise transfer function* (NTF) has a zero at DC and thus suppresses the quantization noise in the vicinity of DC. The spectrum of the output of MOD1 shown in Figure 2.2 clearly shows this effect.

Assuming that E is white with power σ_e^2, the in-band noise power for MOD1 is

$$N_0^2 = \frac{\sigma_e^2}{\pi}\int_0^{\frac{\pi}{R}} |H(e^{j\omega})|^2 d\omega \approx \frac{\sigma_e^2}{\pi}\int_0^{\frac{\pi}{R}} \omega^2 d\omega = \frac{\sigma_e^2 \pi^2}{3R^3} , \tag{2.2}$$

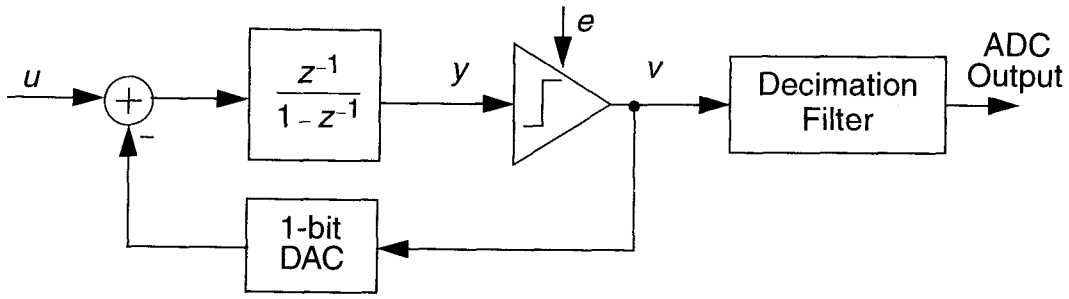


Figure 2.1: MOD1: A first-order delta-sigma ADC.

where $\sigma_e^2 = \frac{\Delta^2}{12} = \frac{1}{3}$, if e is uniformly distributed in $[-1, 1]$.

Eq. (2.2) predicts that an octave (factor of two) increase in R will increase the SNR by 9 dB (= 1.5 bits by the 6 dB = 1 bit rule). With an oversampling ratio of 100, the rms noise level in the band of interest should be on the order of 10^{-3}, or -60 dB. In principle, the in-band noise can be made as small as desired, simply by making R large enough. Thus, MOD1 has potentially unlimited accuracy, independent of component matching errors and many other non-idealities. In general, the resolution of a delta-sigma converter is improved by clocking faster (which is easy) and not by making larger, more sensitive analog circuitry (which is hard). In practice, the achievable linearity is limited by the resolution of the analog components.

A switched-capacitor implementation of MOD1 is shown in Figure 2.3. The integrator is realized by 1 opamp, 2 capacitors and 4 switches; the DAC by 2 reference

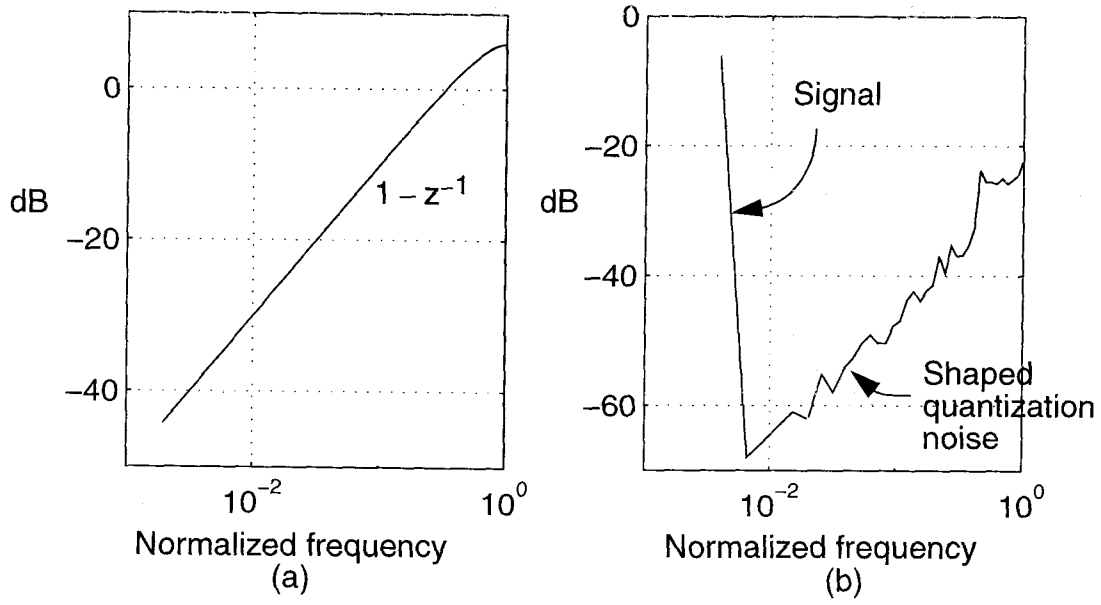


Figure 2.2: (a) The frequency response of $1 - z^{-1}$, and (b) the simulated spectrum of a first-order delta-sigma modulator with a sine-wave input shows the shaping of quantization noise.

voltages and 2 switches; and the quantizer by a simple comparator and a D flip flop. The analog circuitry is seen to be quite trivial.

An important property of single-bit modulators is what is often referred to as "inherent linearity" [5]. This property comes from the fact that the input-output transfer curve of any static two-level DAC can be modeled exactly by a straight line joining the two points on the curve. A binary DAC is therefore ideal and cannot introduce errors other than simple offset and gain errors. These errors do not introduce distortion and the conversion is "linear."

One important phenomenon observed in MOD1 is that the output will be periodic with rational DC inputs [6][7][8]. With an irrational DC input, MOD1's output is not periodic. In both cases, however, the quantization noise has a discrete spectrum, rather than the white spectrum assumed in Eq. (2.2). The methods used to whiten the noise include dithering the quantizer [9][10], chaotic modulation [11][12][13] and multi-bit quantization. The first two methods degrade the average SNR somewhat, with dithering providing the least degradation for a given immunity to limit cycles. Multi-bit quantization is the most attractive since it increases the modulator's resolution while simultaneously reducing the

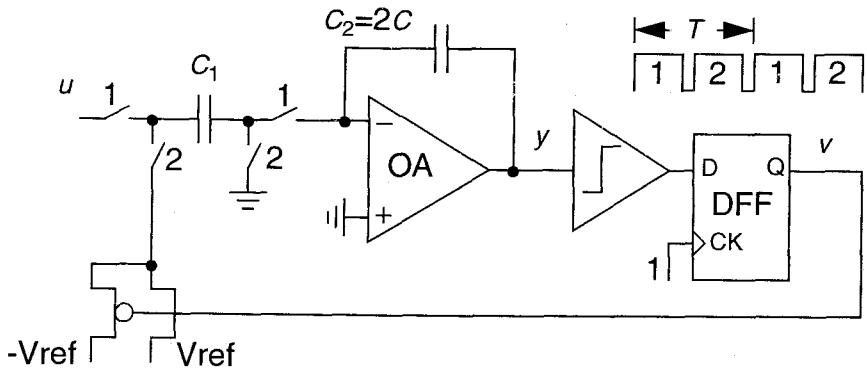


Figure 2.3: A switched-capacitor implementation of MOD1.

modulator's susceptibility to limit cycles. However, multi-bit quantization has generally been avoided because it destroys the inherent linearity property of the feedback DAC. This thesis shows how to overcome this obstacle.

The primary disadvantage of MOD1 is that a high oversampling ratio is needed to achieve high resolution. For example, if we want 16-bit resolution with single-bit quantization, the oversampling ratio must be about 1500. Except for very low-frequency applications, a high oversampling ratio leads to a high sampling frequency and thus difficulties in implementation. As the next section will show, the oversampling ratio requirement for a given resolution can be relaxed if higher-order and/or multi-bit delta-sigma modulators are used.

2.3 High-Order Delta-Sigma Modulators

A general model of a discrete-time single-quantizer delta-sigma modulator is given in Figure 2.4. This figure shows that such a system consists of three basic parts: a loop filter, a quantizer and a feedback DAC. Modeling the quantizer with $V = Y + E$, the output of the modulator is

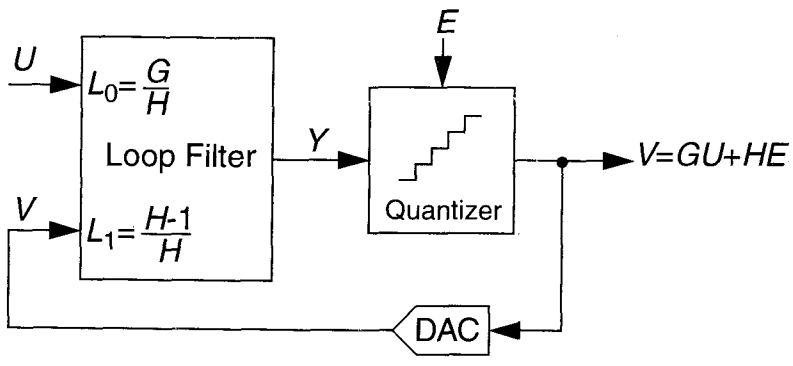


Figure 2.4: A general model of a discrete-time single-quantizer delta-sigma modulator.

$$V(z) = G(z)U(z) + H(z)E(z), \tag{2.3}$$

where $G(z)$ and $H(z)$ are the signal transfer function (STF) and noise transfer function (NTF), respectively, of the modulator. To achieve spectral separation between signal and noise, the STF must be approximately one in the band of interest whereas the NTF must be approximately zero.

The simplest high-order delta-sigma modulator is the double-loop, or second-order, delta-sigma modulator [14], shown in Figure 2.5 [15]. The signal transfer function $G(z)$ and the noise transfer function $H(z)$ of this modulator are

$$G(z) = \frac{z}{z^2 + (-1 + \alpha + \beta + \gamma)z + (1 - \beta - \gamma)} \quad \text{and} \tag{2.4}$$

$$H(z) = \frac{z^2 + (-2 + \alpha + \beta)z + (1 - \beta)}{z^2 + (-1 + \alpha + \beta + \gamma)z + (1 - \beta - \gamma)}. \tag{2.5}$$

In the standard case, $(\alpha, \beta, \gamma) = (0, 0, 1)$, and so $H(z) = (1 - z^{-1})^2$. This modulator will be referred to as MOD2. Again assuming that E is white with power σ_e^2, the noise power in the band of interest is

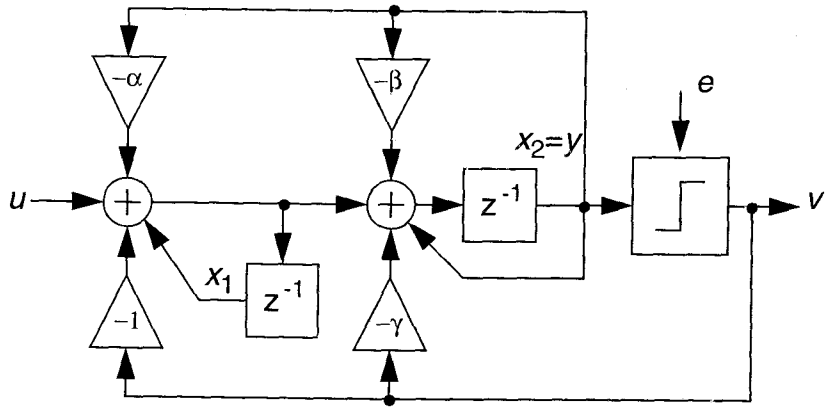


Figure 2.5: A general second-order delta-sigma modulator.

$$N_0^2 = \frac{\sigma_e^2}{\pi}\int_0^{\frac{\pi}{R}} |H(e^{j\omega})|^2 d\omega \approx \frac{\sigma_e^2}{\pi}\int_0^{\frac{\pi}{R}} \omega^4 d\omega = \frac{\sigma_e^2 \pi^4}{5R^5}, \tag{2.6}$$

and thus MOD2 achieves a 15 dB (2.5 bit) increase in the SNR for each octave increase in R— 6 dB (1 bit) per octave better than the first-order modulator.

The above technique can be extended to higher order modulators by adding more feedback loops to the circuit. In general, when a modulator has L loops and is not overloaded, it can be shown that the in-band rms modulation noise power is

$$N_0^2 = \frac{\sigma_e^2}{\pi}\int_0^{\frac{\pi}{R}} |H(e^{j\omega})|^2 d\omega \approx \frac{\sigma_e^2 \pi^{2L}}{2L+1} \cdot \frac{1}{R^{2L+1}} \tag{2.7}$$

when the NTF takes the form

$$H(z) = (1 - z^{-1})^L. \tag{2.8}$$

Eq. (2.7) shows the modulation noise falls by $6L + 3$ dB for every doubling of the sampling frequency, thus providing $L + 0.5$ extra bits of resolution. Although the NTF in Eq. (2.8) can exhibit exceedingly high SNR when L is large, it is not achievable in practice because a modulator with this kind of NTF is not stable with a binary quantizer for L greater than 2.

At the moment, there is no rigorously proven criterion for choosing an $H(z)$ which ensures the stability of a binary modulator. One way to design a high-order and stable modulator employing a binary quantizer is to lower $\|H\|_\infty$, the maximum gain of the NTF. Lee [16][17] claimed that if $\|H\|_\infty$ is less than 2, then the modulator is stable. Based on this rule of thumb, numerous high-order modulators have been designed. In [16] an optimization program was used to minimize the value of in-band noise power subject to stability constraints. It was found that there is a simple qualitative relationship among

$\|H\|_\infty$, the stable input range and the attenuation of the NTF. In particular, if a higher value for the $\|H\|_\infty$ constraint is used, then the input range is smaller but the attenuation of NTF in the band of interest is higher. Another way to maintain the stability of high-order modulators is through the use of multi-bit quantization, a tactic which will be explored in Section 2.5, "Multi-bit Delta-Sigma Modulators," on page 16.

2.4 Bandpass Modulators

A lowpass delta-sigma modulator places NTF zeros near $\omega = 0$ in order to null quantization noise in a narrow band around DC. Noise-shaping can be extended to the bandpass case simply by placing the NTF zeros at a non-zero frequency ω_0. Quantization noise is nulled in a narrow band around ω_0, and the output bit-stream accurately represents the input signal in this narrow band. A system which achieves this result is called a *bandpass delta-sigma modulator* [19][20][21]. Figure 2.6 compares the pole/zero locations of the NTFs for lowpass and bandpass modulators. As was the case for lowpass modulators, the oversampling ratio of a bandpass modulator is defined as $R = f_s/2f_B$, but now f_B corresponds to the width of the band about the center frequency.

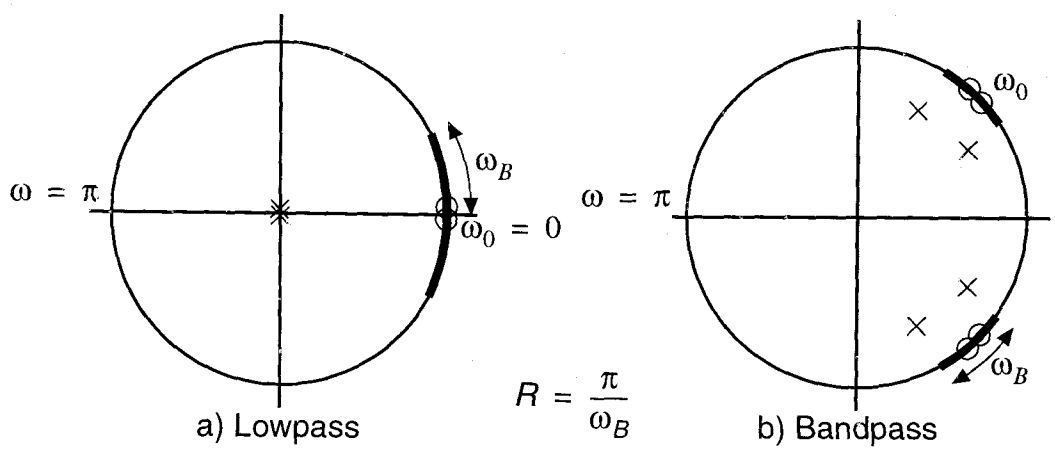


Figure 2.6: The passband and pole/zero locations of the noise transfer functions for a) lowpass and b) bandpass ΔΣ modulation.

The obvious advantage of a bandpass delta-sigma modulator is that the sampling frequency is only several times ($2\pi/\omega_0$) greater than the signal center frequency ω_0. A direct implementation of a lowpass delta-sigma modulator for an intermediate-frequency (IF) or radio-frequency (RF) narrow band signal would result in a sampling rate which is much higher than that required by a bandpass modulator.

A conceptual diagram of a bandpass delta-sigma ADC is illustrated in Figure 2.7. A narrowband analog input is converted directly to a 1 bit oversampled digital signal with noise-shaping around the passband. The decimation filter suppresses the out-of-band quantization noise and downsamples the 1 bit signal to yield a baseband digital signal. The decimation filter for a bandpass modulator is similar to that of a lowpass modulator.

The primary motivation for the development of bandpass converters is their ability to convert modulated narrowband signals directly to digital form. Examples of systems where this operation is important include radar, digital communication and measurement systems. In the context of these systems, early conversion to digital at either the IF or even the RF stage results in a more robust system with improved IF-strip testability and provides opportunities for coping with multiple broadcast/data formats. As shown in Figure 2.8, the competing "zero-IF" receiver architecture does quadrature mixing with analog components

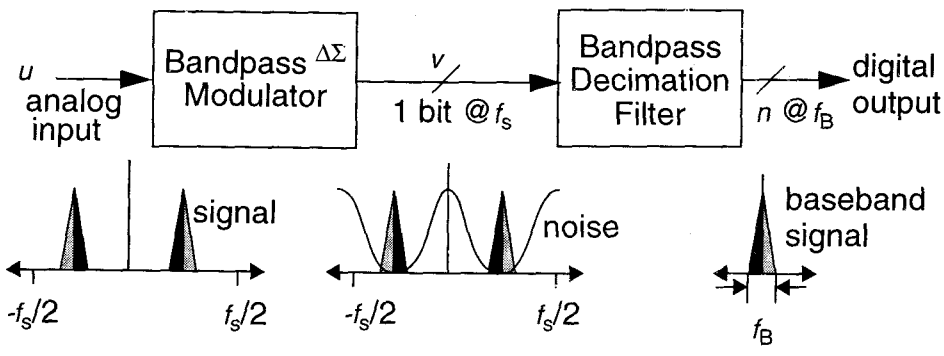


Figure 2.7: A diagram of a bandpass delta-sigma ADC.

while the bandpass modulator does such mixing digitally. Since it is hard to maintain quadrature with analog components but it is easy to keep digital signals in perfect quadrature, systems (such as digital communication systems) which rely on the separation between I and Q are more ideal if mixing is done digitally.

Again, assuming the quantization noise is white with power σ_e^2, the in-band noise power for a bandpass modulator of order $2n$ where

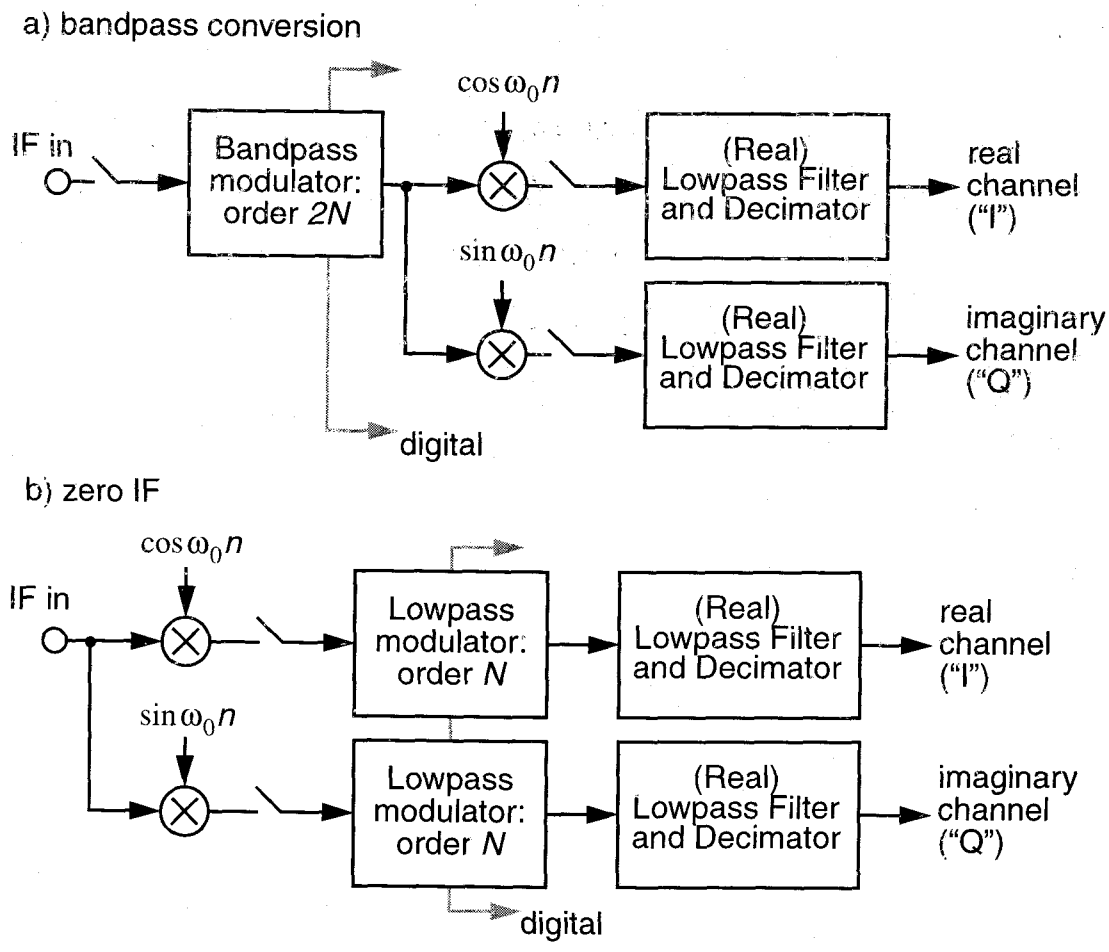


Figure 2.8: Comparison of radios using a bandpass delta-sigma ADC or the "zero IF" architecture.

$$H(z) = \frac{(z - z_0)^n (z - z_0^*)^n}{D(z)}, \tag{2.9}$$

is

$$N_0^2 = \frac{\sigma_e^2}{\pi} \int_{\omega_0 - \frac{\pi}{2R}}^{\omega_0 + \frac{\pi}{2R}} |H(e^{j\omega})|^2 d\omega \approx \frac{\sigma_e^2}{\pi} \int_{-\frac{\pi}{2R}}^{\frac{\pi}{2R}} \frac{(\omega \cdot 2\sin\omega_0)^{2n}}{|D(e^{j\omega_0})|^2} d\omega$$

$$= \frac{\pi^{2n}\sigma_e^2}{(2n+1)R^{2n+1}} \cdot \frac{(2\sin\omega_0)^{2n}}{|D(e^{j\omega_0})|^2}. \tag{2.10}$$

As with a lowpass modulator of order n, the resolution of a bandpass modulator of order $2n$ increases by $n + 0.5$ bits with every octave increase in R. The design considerations for a bandpass NTF are the same as those for lowpass NTFs.

Figure 2.9 shows the spectrum of the output of a sixth-order bandpass delta-sigma modulator with a center frequency $\omega_0 = \frac{\pi}{4}$. The in-band sine wave input is faithfully

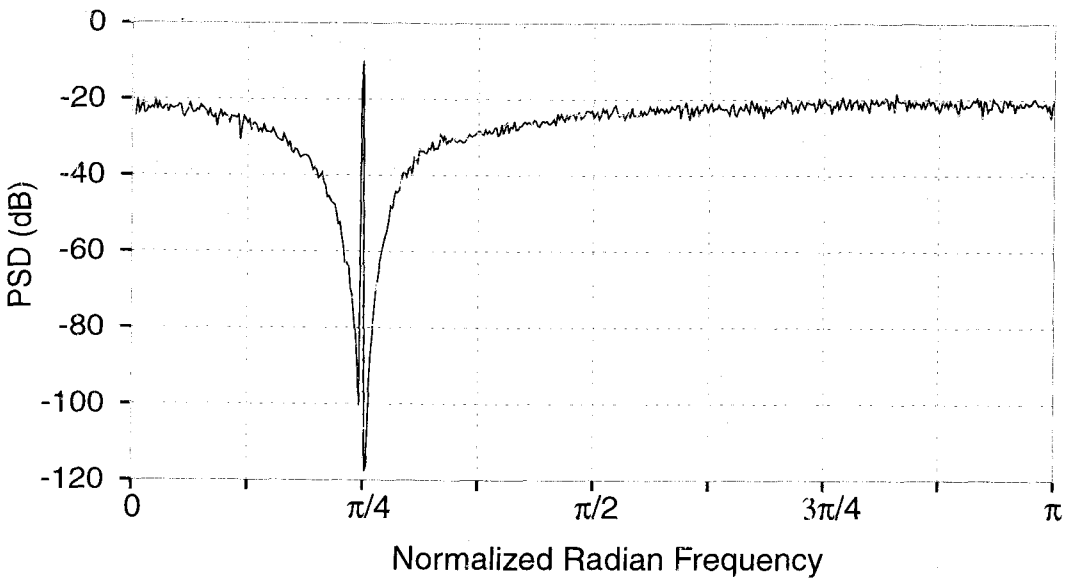


Figure 2.9: The spectrum of the output of an example sixth-order modulator with a -10 dB peak input (relative to the DAC feedback levels). The bandwidth associated with each point is π/512 radians.

reproduced, yielding a spectral line inside a noise valley, but outside this valley large amounts of quantization noise would dominate any out-of-band signal components.

Bandpass delta-sigma modulators are most attractive for the conversion of high-frequency narrowband signals to digital form [20]-[26]. In Chapter 6 a sixth-order bandpass delta-sigma DAC will be designed and implemented.

2.5 Multi-bit Delta-Sigma Modulators

The constraint on $\|H\|_\infty$ for high-order delta-sigma modulators results from the limited dynamic range of a one-bit quantizer, which produces a large amount of noise compared to a multi-bit quantizer. Therefore, an obvious improvement is to use a multi-bit quantizer in place of the one-bit quantizer in Figure 2.4. With the increased number of quantizer levels and the accompanying reduction in the quantization noise power, the $\|H\|_\infty$ constraint can be loosened and the performance of the modulator improved. For example, an ideal fifth-order lowpass delta-sigma modulator with a 3-bit quantizer is stable when $\|H\|_\infty = 6.25$ and achieves a SNR of 114 dB at an oversampling ratio of 32. But a binary delta-sigma modulator requires $\|H\|_\infty = 1.6$ to be stable and only 70 dB SNR can be achieved at an oversampling ratio of 32.

A second advantage of multi-bit quantization is that the output of a multi-bit delta-sigma modulator is a smoother waveform that more closely resembles the desired signal than the full-scale, PWM-like square-wave output of a single-bit modulator. This accurate tracking in the time-domain allows a DAC system to use a less aggressive analog reconstruction filter and gives a continuous-time ADC system lower sensitivity to feedback jitter.

Unfortunately, the inherent linearity property of the DAC is lost, and the linearity requirements are severe. Assuming E_{DAC} is the noise introduced by the DAC, the linear model of a multi-bit delta-sigma modulator is

$$V = GU + HE + (H-1)E_{DAC}, \tag{2.11}$$

where $(H-1)E_{DAC} \approx -E_{DAC}$ in the band of interest. The performance of the modulator is limited by the larger of E_{DAC} and the noise-shaped E signal. Typically, the error of the DAC is dominant since it is caused by the mismatch among the analog components and matching better than 11 bits is difficult. Despite this apparently fatal flaw, the potential of multi-bit quantizers for achieving high performance has driven the search for solutions, several of which will be described in the next section.

2.6 Existing DAC Architectures for Improved Linearity

Digital correction [27] has been proposed and demonstrated as one means for allowing multi-bit quantization. This technique assumes that the DAC errors are fixed, and available as digital quantities. In this approach, E_{DAC} is digitally added to the modulator output, resulting in $V + E_{DAC} = GU + HE + HE_{DAC}$. This simple operation results in noise-shaped DAC errors. The drawbacks of the digital correction scheme are the need for a calibration cycle, the requirement that the DAC errors not be subject to drift and the use of more complex digital circuitry.

Other techniques which have received attention include the use of element randomization, individual level averaging, and more recently, noise-shaped element usage. The principle behind these schemes is to convert the element mismatch error from a DC error into a wide-band noise by choosing different elements to represent a digital input code at different times, a process referred to as *dynamic element matching* (DEM). With randomized element usage [28], the mismatch error is converted to a white noise, instead

of the harmonic tones which may exist if no randomization is used. However, randomized element usage does not preserve the shaping of the noise and the SNR improvement is limited. In contrast, the individual-level-averaging schemes of Leung [29], [30], the noise-shaped element usage of Kwan and Adams [31] and the element rotation scheme of Story [32], Jackson [33], Baird and Fiez [34][35] represent major steps to improve the SNR in the passband compared to dynamic element randomization while avoiding the generation of tones. Although each of these schemes were derived independently, they all result in the same remarkable feature: first-order noise-shaped DAC errors. The main contribution of this thesis is to generalize the first-order results in a variety of ways, including arbitrary shaping (lowpass/bandpass) and arbitrary implementation (discrete-time/continuous-time). The existing techniques and their generalizations will be discussed in Chapter 3.

2.7 Benchmarks

Some current delta-sigma ADC benchmarks are summarized and plotted in Figure 2.10. Except [40] (which is implemented in InP HBT technology), all the others are silicon CMOS implementations. [36][37][38][39][41][42][47]. Compared with other types of data converter (such as flash, pipelined, algorithmic, etc.), delta-sigma ADCs achieve the highest resolution, with 20.5 bits of dynamic range being the highest value reported [36]. It should be noted that single-bit quantization is still quite popular in low-frequency applications [36][38]. However for high speed applications, delta-sigma modulators employing multi-bit quantization become indispensable [37][39][41].

2.8 Summary

Delta-sigma modulation has three key features: *oversampling*, *noise-shaping* and (until recently) *one-bit quantization*. Oversampling means sampling at a rate above the Nyquist rate, and the oversampling ratio is typically greater than 64. Noise-shaping means attenuating the quantization noise at those frequencies which are of interest, and is achieved

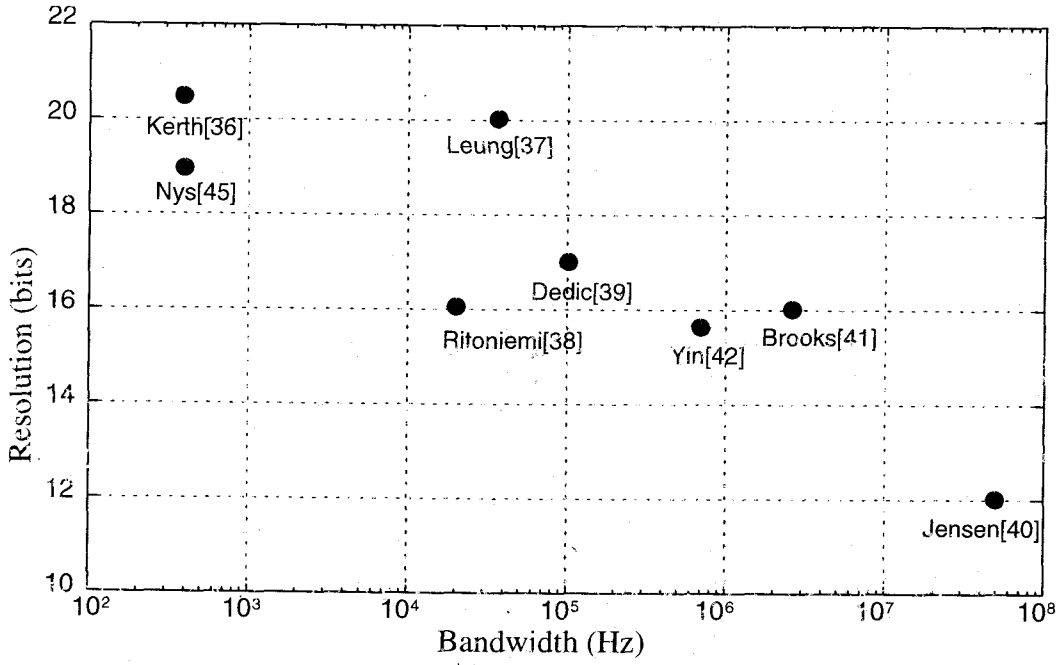


Figure 2.10:Delta-sigma ADC resolution vs. signal bandwidth.

by embedding a quantizer in a feedback loop. One-bit quantization means that the modulator output is only one bit wide and gives rise to the inherent linear property of delta-sigma modulators.

Modulators can be designed which faithfully reproduce signals near DC (lowpass modulators) or near a non-zero frequency (bandpass modulators). Modulators can also make use of multi-bit quantization, but doing so puts stringent linearity requirements on the internal multi-bit DAC.

To convert a delta-sigma modulator's bit-stream output to standard PCM data, a decimation filter is needed. This filter removes the out-of-band quantization noise and produce noise-free data at a reduced sampling rate.

Chapter 3. Advanced Mismatch Shaping

In this chapter, the principle of mismatch-shaping is covered in detail. Several existing schemes are examined and their performance compared. Two new mismatch-shaping schemes, bandpass mismatch shaping and modified mismatch shaping, are presented and analyzed theoretically. Bandpass mismatch shaping is useful in the context of a discrete-time bandpass delta-sigma modulator, while modified mismatch shaping is intended for use in a continuous-time lowpass modulator. Lastly, the implementation of these newly developed schemes are considered.

3.1 Principle of Mismatch Shaping

To realize the possible high performance of delta-sigma modulators with multi-bit quantization, we have to overcome the DAC linearity limitation. An effective way to achieve this goal is through the use of *mismatch shaping* [34][35]. Mismatch shaping refers to the process of applying the noise-shaping principle to the errors caused by element mismatch [43][44]. By modulating the element control signals in a manner analogous to $\Delta\Sigma$ modulation, the errors caused by element mismatch are endowed with a noise-shaped spectrum.

Figure 3.1 shows the system diagram of a multibit delta-sigma DAC together with a mismatch-shaping unit element DAC. The upper portion of the diagram depicts an ordinary delta-sigma modulator realized with the error-feedback structure, while the lower portion depicts the key part of the mismatch-shaped multibit DAC: the element selection logic. The two blocks are drawn in a manner which emphasizes their similarity. The signals in the element selection logic that are vectors are denoted with bold text and heavy lines. The output of the selection logic controls the unit-element DAC and the selected elements

are summed to form the output of DAC. Figure 3.2 is a conceptual diagram of an M+1 level DAC employing M unit elements.

The modulator block accepts a finely-quantized signal, u, and produces a coarsely-quantized signal, v. Denoting the Z-transform of the quantizer error by $E(z)$, the output of the modulator is:

$$V(z) = U(z) + H_1(z)E(z). \tag{3.1}$$

Thus, the output of the modulator is equal to its input plus an error term which, by suitable choice of H_1, the NTF of modulator, can be designed to have a small magnitude in

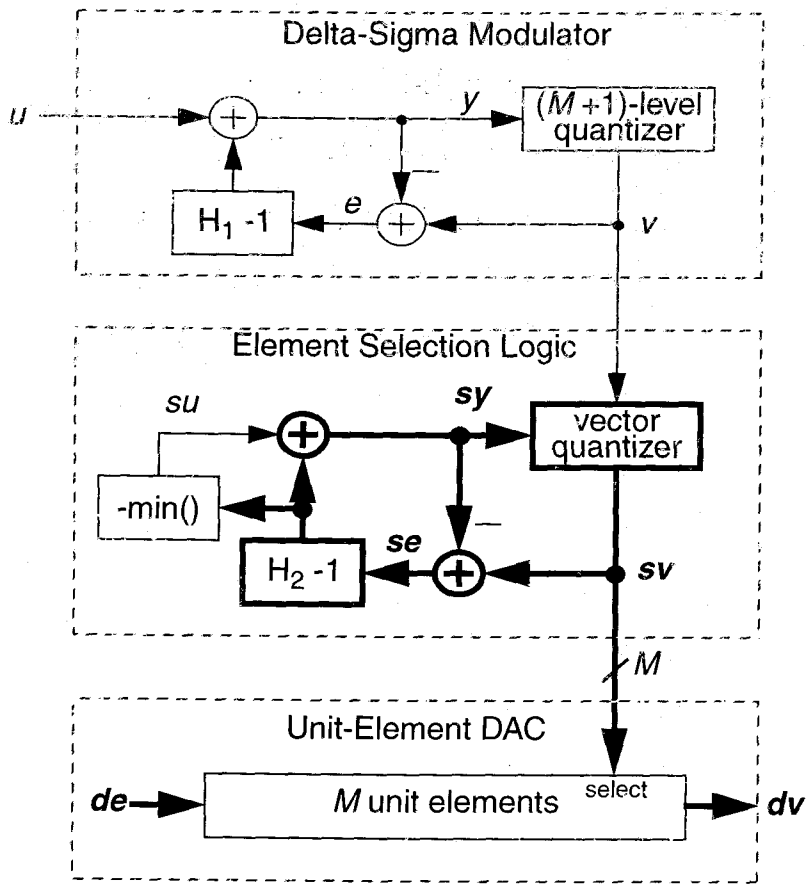


Figure 3.1: The system diagram of a multibit delta-sigma DAC, showing the digital delta-sigma modulator, the element-selection logic and the unit-element DAC.

a selected frequency range. For the purpose of this discussion, assume that v is quantized to one of the M+1 integers in $[0, M]$. Using multibit quantization with $M \geq 2^N$, a high-order NTF $H_1(z) = (1 - z^{-1})^N$ can be realized without regard to the restriction imposed by the Lee criterion [16]; the stability of the modulator is guaranteed.

At each time step n, the element selection logic determines which $v(n)$ of the M unit elements will be used to form the analog output value. The output of the selection logic is $\boldsymbol{sv}$, a $1 \times M$ vector containing v ones and M-v zeros. Each unit element in the DAC is controlled by a specific component of $\boldsymbol{sv}$, so the output of the DAC will be an analog version of v plus an accumulated error term due to element mismatch. It is the function of the selection logic to ensure that the error term has a shaped spectrum.

The selection vector, $\boldsymbol{sv}$, is computed in a manner analogous to that which produces v, namely each component of $\boldsymbol{sv}$ is the output of a modified delta-sigma modulator realized

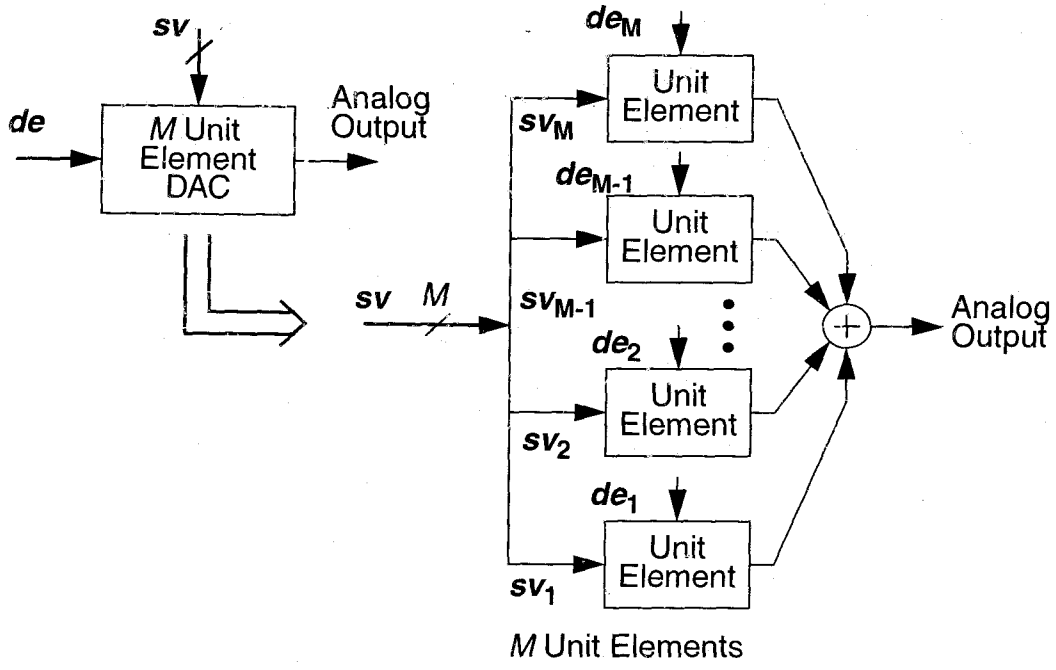


Figure 3.2: A conceptual diagram of an M+1 level DAC employing M unit elements.

with the error feedback structure. The main modification is in the vector quantizer, but this modification does not affect the basic operation of the element selection logic. A discussion of the vector quantizer and the *su* input will be delayed until later.

Observing that ***sv*** is computed in a manner analogous to that which produces *v*, the output of the selection logic may be written immediately as

$$\boldsymbol{SV}(z) = SU(z)\begin{bmatrix}1 & \cdots & 1\end{bmatrix} + H_2(z)\boldsymbol{SE}(z). \tag{3.2}$$

Now, let ***de*** be a (fixed) $1 \times M$ vector containing the difference between the value of each unit element in the DAC and the mean of all the elements. As a result of this definition, the sum of the components of ***de*** is precisely zero:

$$\begin{bmatrix}1 & \cdots & 1\end{bmatrix} \bullet \boldsymbol{de} = 0, \tag{3.3}$$

where $\boldsymbol{a} \bullet \boldsymbol{b}$ represents the scalar (dot) product of two vectors.

Since the error between the actual output of the DAC and its ideal output is $\boldsymbol{sv} \bullet \boldsymbol{de}$, the DAC error is

$$SV(z) \bullet \boldsymbol{de} = \left[SU(z)\begin{bmatrix}1 & \cdots & 1\end{bmatrix} + H_2(z)\boldsymbol{SE}(z)\right] \bullet \boldsymbol{de} = SU(z) \cdot 0 + H_2(z)(\boldsymbol{SE}(z) \bullet \boldsymbol{de})$$
$$= H_2(z)(\boldsymbol{SE}(z) \bullet \boldsymbol{de}). \tag{3.4}$$

The above equation shows that static DAC errors are shaped by the transfer function H_2, provided, of course, that the ***se*** signal is bounded. This result is independent of the *su* input signal, the operation of the vector quantizer and most importantly, the errors in the unit elements.

Based on the element usage requirement $v(n)$ and on the contents of the vector $\boldsymbol{sy}(n)$ (which can be interpreted the 'desired usage' of each element in the array at time step n), the vector quantizer sets certain elements of $\boldsymbol{sv}(n)$ to one. Thus, $\boldsymbol{sv}(n)$ is the 'actual usage' of the element in the array. The error of this quantization operation, $\boldsymbol{se}(n)$, is fed back through an array of H_2-1 filters and added to the scalar-valued selection logic input, $su(n)$ to form subsequent samples of $\boldsymbol{sy}(n)$. In the original version of this system, $su(n)$ is equal to the negative minimum value of the filter outputs, thus all components of $\boldsymbol{sy}(n)$ are positive, with the smallest component equal to zero. The addition of a scalar to all elements in the $\boldsymbol{sy}$ vector does not disturb the noise-shaping property of the selection logic; its purpose is simply to reduce the magnitude of the signals which need to be stored and processed. The vector quantizer can be implemented with a sorting function block: it selects the largest $v(n)$ number of elements from its input vector $\boldsymbol{sy}(n)$ and sets the corresponding elements of $\boldsymbol{sv}(n)$ to one. The operation of sorting the largest value of $\boldsymbol{sy}(n)$ minimizes the instantaneous magnitude of the quantization error vector $\boldsymbol{se}(n)$.

By combining Eq. (3.1) and Eq. (3.4), we find that

$$DV(z) = U(z) + H_1(z)E(z) + H_2(z)(\boldsymbol{SE}(z) \bullet \boldsymbol{de}). \tag{3.5}$$

This equation shows that the DAC output is equal to the modulator input plus two error terms. The first error term is the quantization noise of the $(M+1)$-level quantizer, shaped by the noise transfer function H_1 of the modulator. The second error term is the element mismatch error, multiplied by the selection error and shaped by the mismatch-shaping function H_2.

Like regular delta-sigma modulators, the selection logic loop around the vector quantizer cannot be delay-free, so $H_2 - 1$ must be strictly causal (first impulse-response coefficient zero) [45]. This consideration results in the realizability constraint

$$H_2(\infty) = 1. \tag{3.6}$$

Furthermore, like regular delta-sigma modulators, the element selection logic is subject to instability. The *su* input sequence, the value of H_2 and the quantizer algorithm all affect the stability of the element selection logic. As a result, proving the stability of the selection logic is a much more difficult problem than proving the stability of a simple binary delta-sigma modulator. Although a proof of the stability of the selection logic is an unsolved problem, simulations can be used to ensure that the selection logic is stable.

Figure 3.3 shows the MATLAB [70] simulation result for a third-order delta-sigma modulator with an 8-element DAC. Here a 1% mismatch error is assumed to exist. When no mismatch-shaping is employed, as shown in Figure 3.3(a), an increased noise floor and generation of harmonic tones results. When first-order mismatch-shaping is used (i.e. $H_2(z) = 1 - z^{-1}$), the noise floor and harmonics are first-order shaped and decreased dramatically, as Figure 3.3(b) shows.

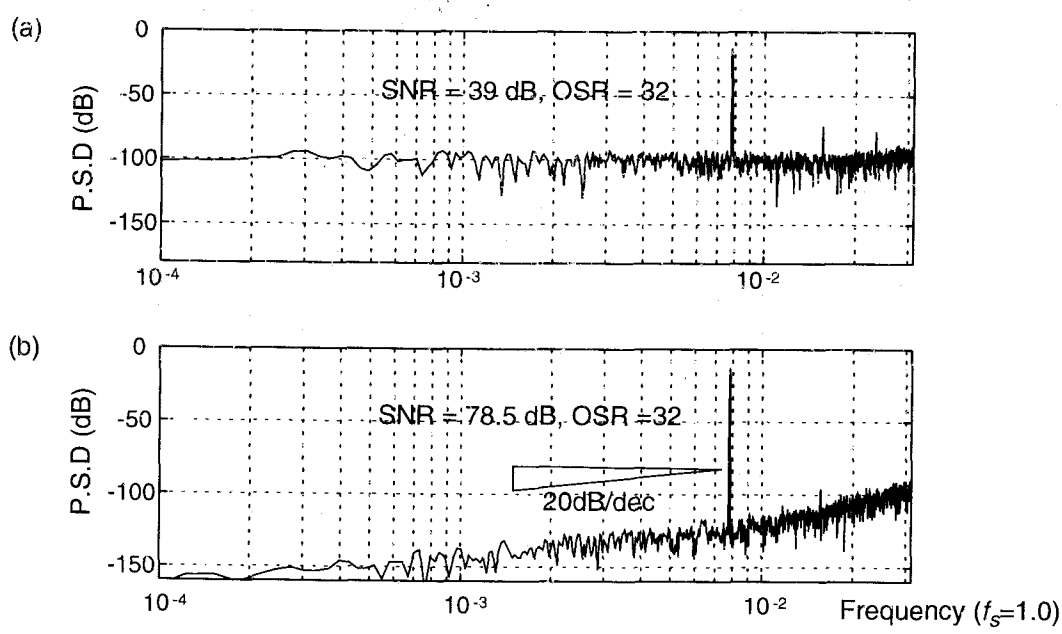


Figure 3.3: Simulation results for an 8-level delta-sigma DAC with 1% mismatch error: (a) without shaping (b) with first-order mismatch shaping.

Although the structure shown in Figure 3.2 works in principle, a direct implementation of it may have several difficulties. First, note the signals denoted with bold text and heavy lines are vectors, implying a huge amount of logic and arithmetic operations. Second, the vector quantizer and the '-min()' block require sorting operations. Even though there are some partial-sorting algorithms [53] (a novel partial sorting algorithm will be introduced in the next section), their implementation still requires a huge amount of hardware. Third, first-order mismatch-shaping is usually adequate; second-order and higher order mismatch-shaping are not necessary in most applications. Therefore, a simpler and more efficient way of implementing the mismatch shaping function is desirable. In the next section, we will review such a scheme.

3.2 First-Order Lowpass Mismatch Shaping

Figure 3.4 shows the element usage patterns when no mismatch-shaping and first-order shaping are used. In this figure, the 8 elements are arranged in a row, and the shaded elements are the ones selected at time step n. The output is formed by summing the contributions from the shaded elements, the number of which equals the input $v(n)$. In Figure 3.4(a), the elements are selected in a thermometer-code manner: at each time step

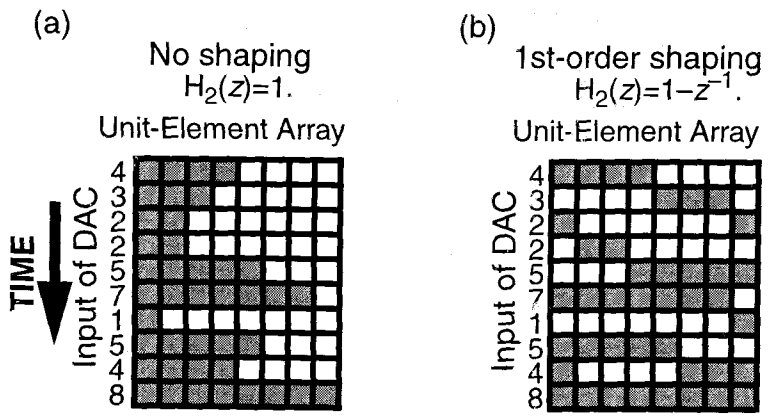


Figure 3.4: Element selection patterns for an 8-element DAC: (a) no shaping (b) shap

the first $v(n)$ elements are chosen. In Figure 3.4(b), the elements are chosen according to the element rotation [33] or the *data weighted averaging* (DWA) algorithm [34][35]. In the DWA algorithm, the next $v(n)$ elements are chosen. When the end of the array is reached, selection rewinds to the first element. As the spectral plot of Figure 3.3 shows, DWA results in first-order (20 dB/decade) shaping of the low-frequency, mismatch-induced noise present in the output of a $\Delta\Sigma$ DAC. Note that the harmonics caused by mismatch error are decreased significantly, indicating that a highly linear DAC has been realized.

DWA implements a first-order mismatch-shaping transfer function (MTF)

$$H(z) = 1 - z^{-1} \tag{3.7}$$

in an efficient manner. To see why DWA is equivalent to first-order mismatch-shaping, assume we have M unit elements in the DAC. Denote the element selection control signal as $ptr(n)$, which is the integral of the input signal $v(n)$. The output is formed by subtracting two adjacent $ptr(n)$s, which means that elements from $ptr(n-1)$ and $ptr(n)$ are used at time n. Although $ptr(n)$ will overflow constantly, this has no significance since we are only interested in the difference of two successive $ptr(n)$s. Whenever overflow happens, $ptr(n)$ wraps back to the start of the array, which is equal to the $mod(M)$ operation. The overflow can not happen twice within one step n, if $v(n)$ is bounded between 0 and M. Denote the integral nonlinearity (INL) introduced by the nonideal unit elements as $inl(n)$:

$$inl(n) = \sum_{i=0}^{ptr(n)-1} sv_i(n) \cdot de_i, \tag{3.8}$$

where $sv_i(n)$ is the element selection signal ($sv_i(n)$=1 when the element is selected, otherwise $sv_i(n)$=0).

Therefore, the output $dv(n)$ can be written as:

$$dv(n) = (ptr(n) + inl(n)) - (ptr(n-1) + inl(n-1)). \tag{3.9}$$

By definition in this algorithm, $ptr(n) - ptr(n-1)$ is the input signal $v(n)$, so

$$dv(n) = v(n) + inl(n) - inl(n-1) \text{ and} \tag{3.10}$$

$$DV(z) = V(z) + INL(z)(1 - z^{-1}). \tag{3.11}$$

Therefore, the second term in Eq. (3.11) is the integral nonlinearity of the DAC shaped by a first-order highpass mismatch shaping function. Another way to view the operating principle of the DWA is shown in Figure 3.5 [46]. The input signal $v(n)$ is integrated, the mismatch error is then added and the sum then differentiated. The result is that the signal term is unchanged but the mismatch error is first-order shaped.

A theoretical analysis is given in [48] which relates the in-band power of the mismatch error σ_e^2 with the variance of the mismatch σ_w^2. It was shown that when elements are selected randomly, the mismatch noise has a white spectrum between 0 and $f_s/2$ with f_s being the sampling frequency. The maximum resolution obtained is given by

$$N_1 = \log 2(\sqrt{(M \cdot R)/3}/\sigma_w) \text{ bits,} \tag{3.12}$$

where R is the oversampling ratio.

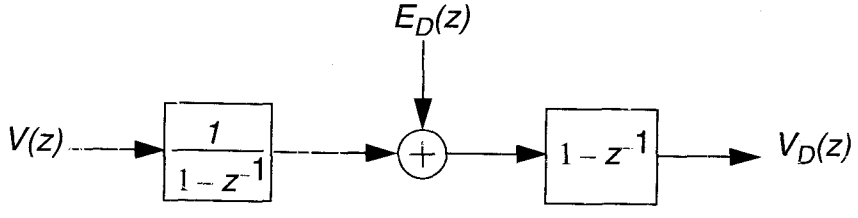


Figure 3.5: Theoretical model for DWA.

By using the element rotation scheme and assuming a random input signal, the mismatch noise has a white spectrum with the total noise power given by:

$$\sigma_e^2 = \sigma_w^2 \cdot (1 - 1/M)^2 \cdot M/12 \ . \tag{3.13}$$

Thus, the maximum achievable resolution is

$$N_2 = \log 2\left(\frac{\sqrt{M \cdot R^3 \cdot 3}}{\pi \cdot \sigma_w \cdot (1 - 1/M)}\right). \tag{3.14}$$

It can be seen that the improvement of using first-order mismatch shaping is significant: the in-band noise power is lowered by a factor of $3R/(\pi \cdot (1 - 1/M))$. When R equals 32 and M equals 16, we get about a 30 dB improvement.

3.3 Bandpass Mismatch Shaping

A bandpass delta-sigma modulator benefits from multi-bit quantization in the same way as its lowpass counterpart: wider input dynamic range and better stability, much higher performance and closer resemblance of the desired output in the time domain. However, as is the case with a lowpass modulator, the linearity and the SNR of a multi-bit bandpass modulator is limited by the DAC. In this section, several existing schemes for bandpass mismatch shaping are reviewed and a new mismatch shaping scheme which has better performance and which can be implemented more efficiently is presented.

3.3.1 Existing bandpass mismatch shaping techniques

In [49], Henderson and Nys showed one way to implement a second-order mismatch shaping transfer function for a bandpass delta-sigma modulator which has center frequency at $f_s/4$. The sought-after mismatch-shaping function is

$$H(z) = 1 + z^{-2} . \tag{3.15}$$

Figure 3.6. shows the architecture of the DAC which implements their dynamic element matching (DEM) technique. The analog part of the DAC is composed of an array of unit elements which can individually contribute positively or negatively to the output. Activation of the elements is controlled by the DEM algorithm. The generation of the element selection vector is performed over a number of steps. At each step the DEM algorithm decides the sign of contribution of the elements and the final output is obtained by accumulating the total contribution of the elements over the conversion cycle. It was pointed out in [49] that an arbitrary mismatch shaping function could be implemented in this manner.

Although the effectiveness of this approach was demonstrated by simulation in [49], the method suffers from two drawbacks. First, it requires several steps in each cycle

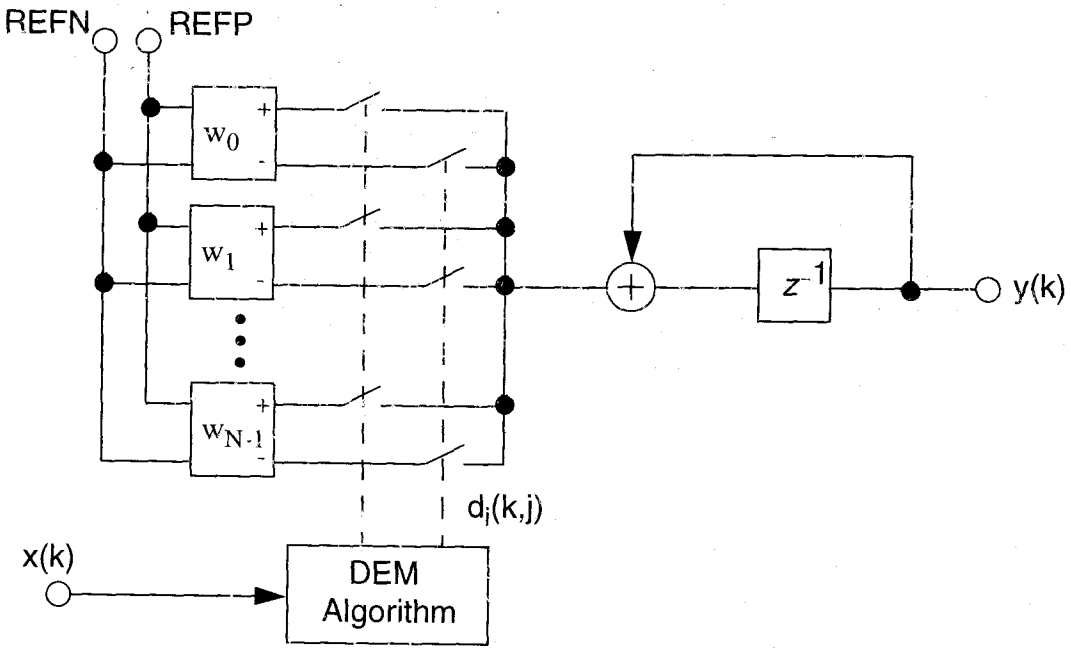


Figure 3.6: Architecture used in [49] for arbitrary mismatch shaping.

to generate the element selection bits, reducing the speed of the DAC. Second, the implementation requires a considerable amount of digital hardware.

Lindfors proposed an *N*-path DEM for multi-bit bandpass delta-sigma modulators in [50]. This method is based upon the *N*-path filter principle, as shown in Figure 3.7 [50]. In this figure, each path implements a first-order high-pass transfer function:

$$H_i(z) = 1 - z^{-1},\ \text{i=1,2,...,N.} \tag{3.16}$$

Each clock frequency equals f_s/N, where the system clock frequency is f_s. By using four path filters in parallel, the overall transfer function becomes

$$H(z) = 1 - z^{-4}. \tag{3.17}$$

Thus, four zeros (notches) are obtained by the 4-path filtering transformation from Eq. (3.16) to Eq. (3.17). The frequency response of $H(z)$ in Eq. (3.17) is shown in Figure 3.8. The zeros at $f_s/4$ and $3f_s/4$ can suppress the mismatch noise in the band of interest of a bandpass delta-sigma modulator with center frequency $f_s/4$.

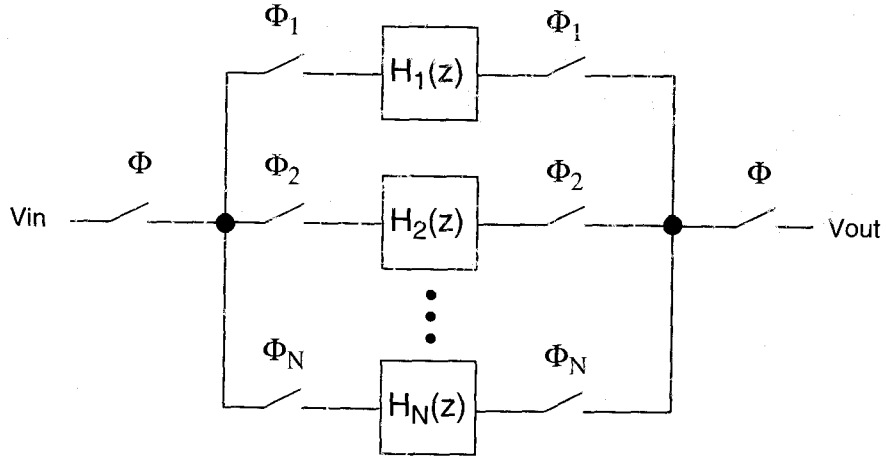


Figure 3.7: A general *N*-path filter.

This scheme can perform the element selection in a single step at each cycle. Compared with the algorithm in [49], this 4-path transformation method can be implemented more efficiently and higher speed can be obtained. However, this algorithm has a significant drawback: the mismatch transfer function in Eq. (3.17) has four zeros spread around the unit circle and only the two zeros at $f_s/4$ and $3f_s/4$ are useful in reducing the mismatch noise in the band of interest. The existence of two unwanted zeros (at DC and $f_s/2$) makes it more difficult to push the noise out of the band of interest. Therefore, the shaping of the mismatch noise is not as effective as the method proposed in [50]. After a comparison between the mismatch-shaping transfer function in Eq. (3.15) and Eq. (3.17), the authors in [49] shows that the in-band mismatch noise power is 6 dB higher than the method of [50]. The scheme proposed in this thesis can overcome the drawbacks of these two methods and is explained in next section.

3.3.2 Proposed algorithm for bandpass mismatch-shaping

Although there exists several ways to design a bandpass modulator from a prototype lowpass modulator [3], the most common way (and probably the easiest way) is through the $z \rightarrow -z^2$ transformation. In this way, the band center is located at $f_s/4$. To effectively shape the noise in the band of interest caused by mismatch error, the mismatch shaping function should take the form:

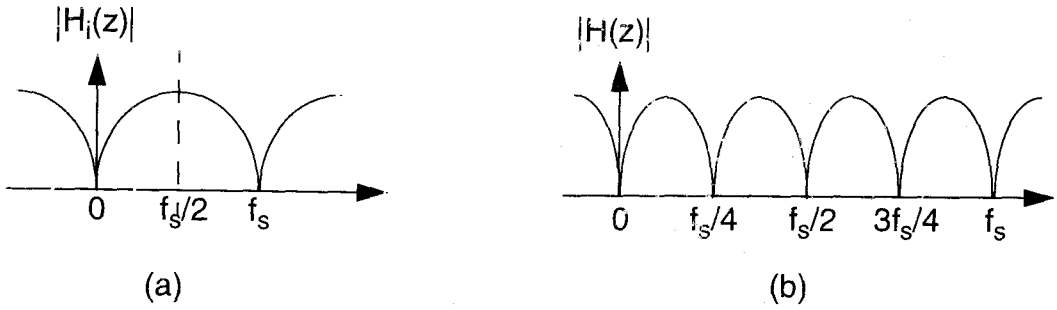


Figure 3.8: Frequency response of the transfer function: (a) before 4-path transformation; (b) after 4-path transformation.

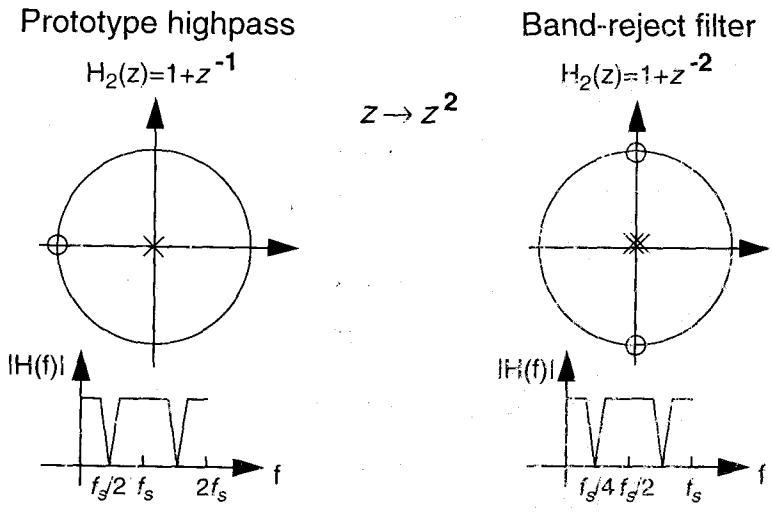


Figure 3.9: Two path transformation of $H_2(z)$.

$$H_2(z) = 1 + z^{-2}. \tag{3.18}$$

While a direct implementation of Eq. (3.18) using the structure depicted in Figure 3.1 is difficult, a simple and effective scheme can be achieved if we first consider implementing

$$H_2'(z) = 1 + z^{-1}. \tag{3.19}$$

A two-path transformation $z \rightarrow z^2$ on H_2' will implement the desired MTF. Figure 3.9 illustrates the principle of this two-path transformation: the zeros of $H_2'(z)$ at π are mapped to $\pm\pi/2$, providing the desired notch at $\omega_0 = \pi/2$. One way to implement H_2' is shown in Figure 3.10. Rather than rotating forward into the least recently used elements as in DWA, this scheme rotates back and forth through the most recently used elements in a time-interleaved fashion. The reason for reusing the most recently used elements is due to the MTF we plan to implement: the impulse response of $H_2' = 1 + z^{-1}$ is {1,1}, indicating the errors made in the last step need to be repeated. The simulation

result shown in Figure 3.10(b) confirms the effectiveness of this mismatch-shaping algorithm in a bandpass application.

The proposed bandpass mismatch shaping can also improve the linearity of the delta-sigma modulator. To see this, a two-tone simulation is performed since the harmonics of a single test tone are outside the band of interest. Since the band center is at $f_s/4$, only third-order intermodulation products (IM3) can be observed in the band of interest. Figure 3.11 shows the simulation result of a third-order modulator with 17 quantization levels. The frequencies of the two input signals are at $0.2482f_s$ and $0.2518f_s$, respectively.

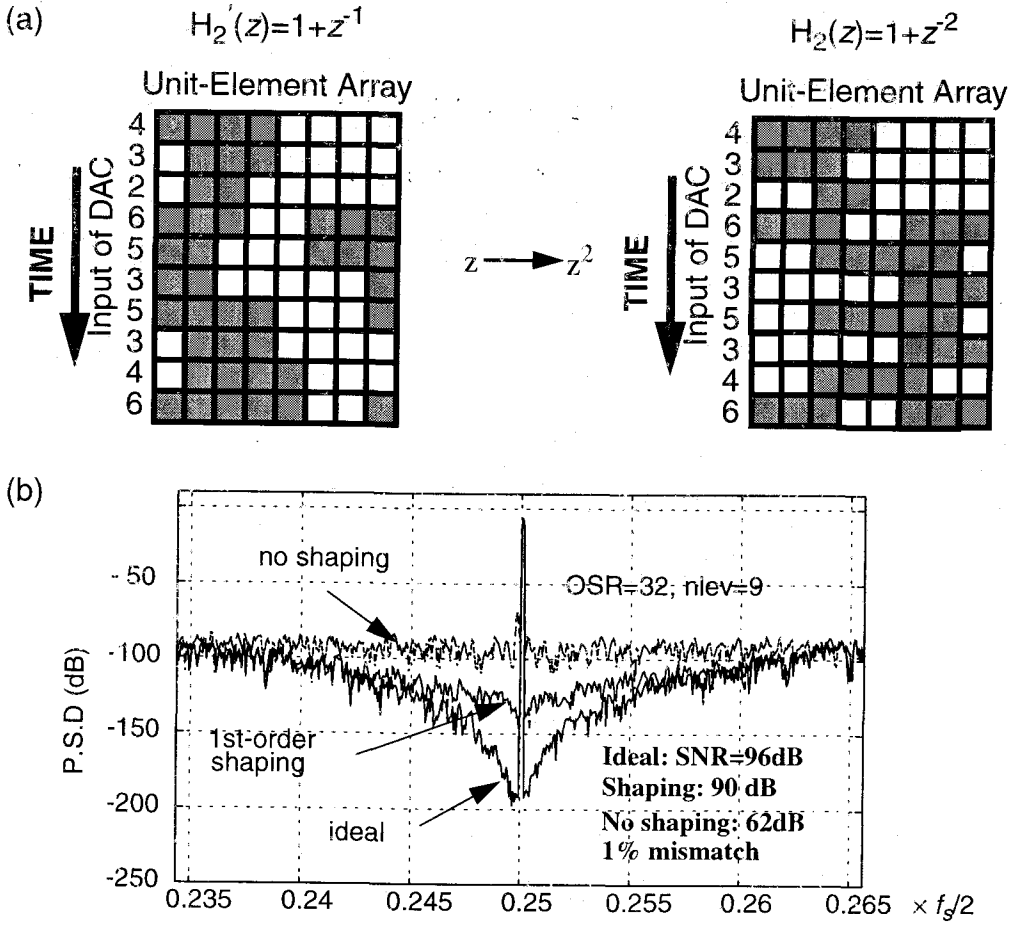


Figure 3.10: Bandpass mismatch-shaping for an 8-element example: (a) selection algorithm; (b) simulation results.

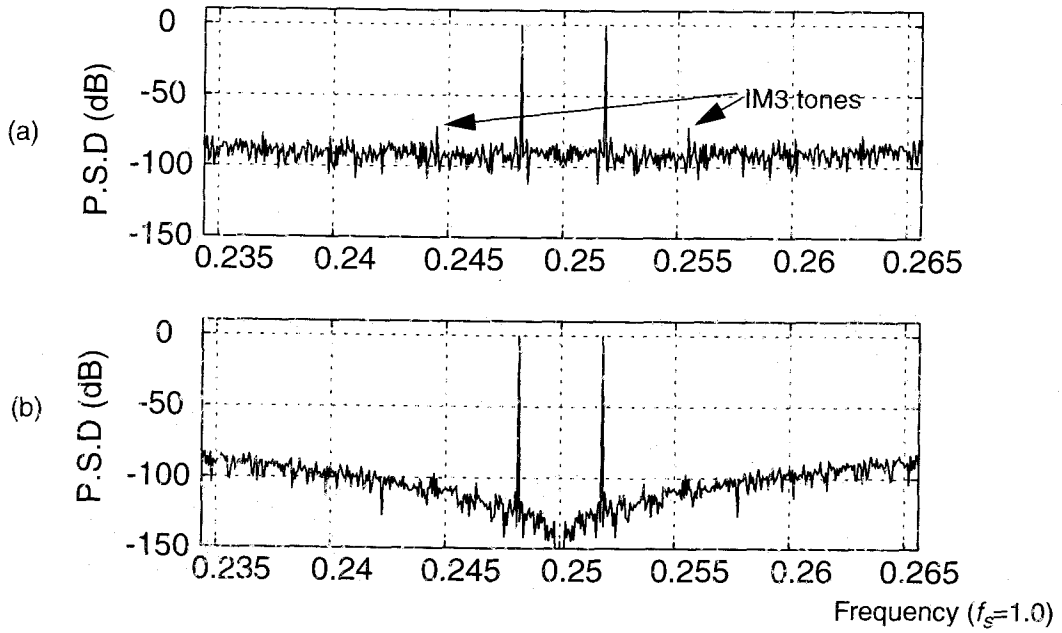


Figure 3.11: Bandpass modulator with two-tone simulation: (a) no shaping; (b) mismatch shaping. Element mismatch error is 1%.

It can be seen that mismatch shaping decreases the IM3 term by over 20 dB, indicating that the linearity of the modulator is greatly improved.

Figure 3.12 gives the simulation results showing the relationship between the variance of element mismatch error and in-band noise power. A sixth-order bandpass modulator with 17-level quantization is assumed. The improvement in the SNR (at an oversampling ratio of 32) with mismatch-shaping is more than 20 dB for element errors exceeding 1%.

3.4 Modified Mismatch Shaping

3.4.1 Motivation

In the previous sections, various mismatch shaping schemes were discussed. First-order mismatch shaping was found to yield a highly linear DAC, presuming the errors

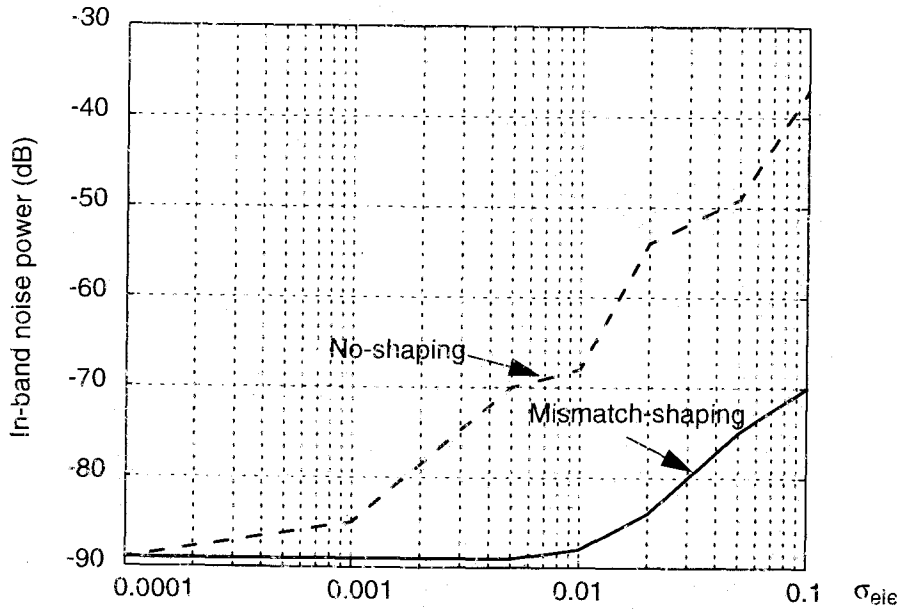


Figure 3.12: In-band noise power vs. element mismatch variance σ_{ele}.

introduced by the DAC are static. In a discrete-time implementation (such as a switched capacitor DAC), only the final value at which the output settles is sampled and processed by the next stage; the exact settling process is not important. However, in continuous-time circuits the DAC output settling process does have a direct effect on the modulator's output spectrum. In this case, both the static error and the dynamic error can degrade the system's performance. Since first-order mismatch-shaping requires that elements turn on and off more often, it increases the DAC switching activity and hence the errors caused by non-ideal DAC dynamics. Therefore, a new mismatch-shaping technique (which will be referred to as modified mismatch shaping) is needed to overcome this disadvantage of first-order mismatch-shaping.

3.4.2 Dynamic error model

In a 1-bit continuous-time DAC, the output can only be considered to be linearly related to its input if the rise and fall dynamics (illustrated in Figure 3.13(a)) are perfectly complementary. Any deviation from this ideal behavior amounts to the addition of a

switching error waveform $e_s(t)$ at every switching transition. The error signal $e_s(t)$ can be found by referring to the model (a 'waveform generator') shown in Figure 3.13(b). In this figure, the output $v(t)$ generates the continuous-time waveform $v_{01}(t)$, $v_{10}(t)$, $v_{00}(t)$ and $v_{11}(t)$ according to its input digital control signal $s_0(n)$ and $s_1(n)$. The truth-table shown in Table 3.1 describes this relationship. The output $v(t)$ can be written in the form

Table 3.1:Truth table of the waveform generator shown in Figure 3.17(b)

$s_0(n)$	$s_1(n)$	$v(t)$
0	0	$v_{00}(t)$
0	1	$v_{01}(t)$
1	0	$v_{10}(t)$
1	1	$v_{11}(t)$

$$v(t) = w_0(t) + w_1(t) \cdot s_1 + w_2(t) \cdot (s_1 - s_0) + w_3(t) \cdot |s_1 - s_0| \quad , \qquad (3.20)$$

where $w_0(t)$, $w_1(t)$, $w_2(t)$ and $w_3(t)$ are waveforms to be determined. It can be seen that the first three terms in Eq. (3.20) represent a linear transformation from the discrete-time to the continuous-time domain, whereas the fourth term involves a nonlinear operation.

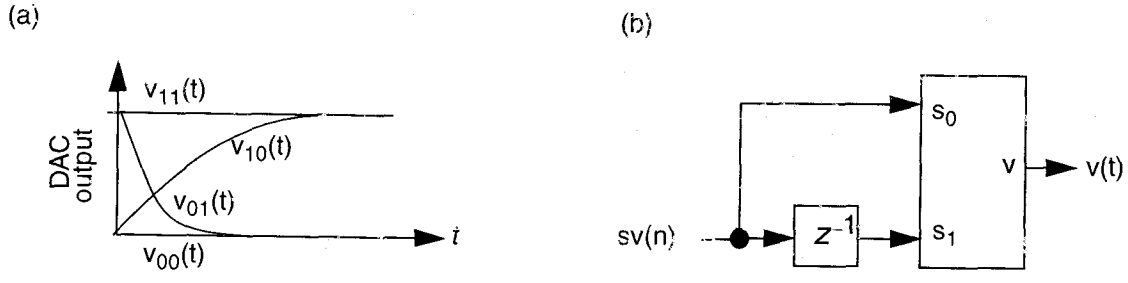


Figure 3.13: Dynamic error in a continuous-time unit element DAC: (a) element switching waveforms; (b) waveform generation model.

The w_i waveforms (i=1,2,3,4) can be solved by relating Eq. (3.20) with Table 3.1

$$v_{00}(t) = w_0 \tag{3.21}$$

$$v_{11}(t) = w_0 + w_1 \tag{3.22}$$

$$v_{01}(t) = w_0 + w_1 + w_2 + w_3 \tag{3.23}$$

$$v_{10}(t) = w_0 - w_2 + w_3. \tag{3.24}$$

Solving Eq. (3.21) to Eq. (3.24) gives

$$w_0(t) = v_{00}(t) \tag{3.25}$$

$$w_1(t) = v_{11}(t) - v_{00}(t) \tag{3.26}$$

$$w_2(t) = (v_{01}(t) - v_{10}(t) + v_{00}(t) - v_{11}(t))/2 \tag{3.27}$$

$$w_3(t) = (v_{01}(t) + v_{10}(t) - (v_{00}(t) + v_{11}(t)))/2. \tag{3.28}$$

Thus, knowing $w_3(t)$ allows us to predict the dynamic error term $e_s(t)$ associated with a given sv signal

$$e_s(t) = \sum_{n=-\infty}^{\lfloor t \rfloor} |sv(n) - sv(n-1)| w_3(t-n), \tag{3.29}$$

where $\lfloor t \rfloor$ stands for the integer value of time variable t.

In a continuous-time DAC composed of unit elements whose dynamics are independent and identical, errors caused by nonideal element switching dynamics can be modeled as shown in Figure 3.14. The output of the $|x|$ block is the number of elements which switch at that time period. If there is no switching activity at time step n, then there is no switching error introduced. Thus, the errors introduced by switching dynamics are proportional to the number of switching events.

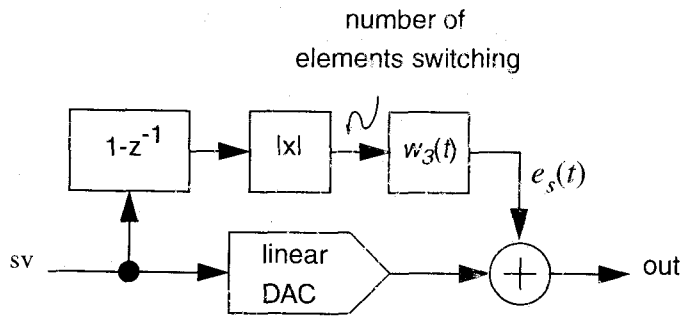


Figure 3.14: Dynamic error model for a continuous-time unit element DAC.

The above argument has been validated with simulations. Figure 3.15 shows the simulation results using the model in Figure 3.14. A third-order lowpass modulator with 9-level quantization employing no-shaping and first-order mismatch shaping is used to generate the *sv* vector. It is assumed that no mismatch exists in the unit element DAC, but that a 0.1% rise/fall mismatch error exists. The generation of second-order harmonic distortion (especially in the first-order shaping case) is due to the absolute value function

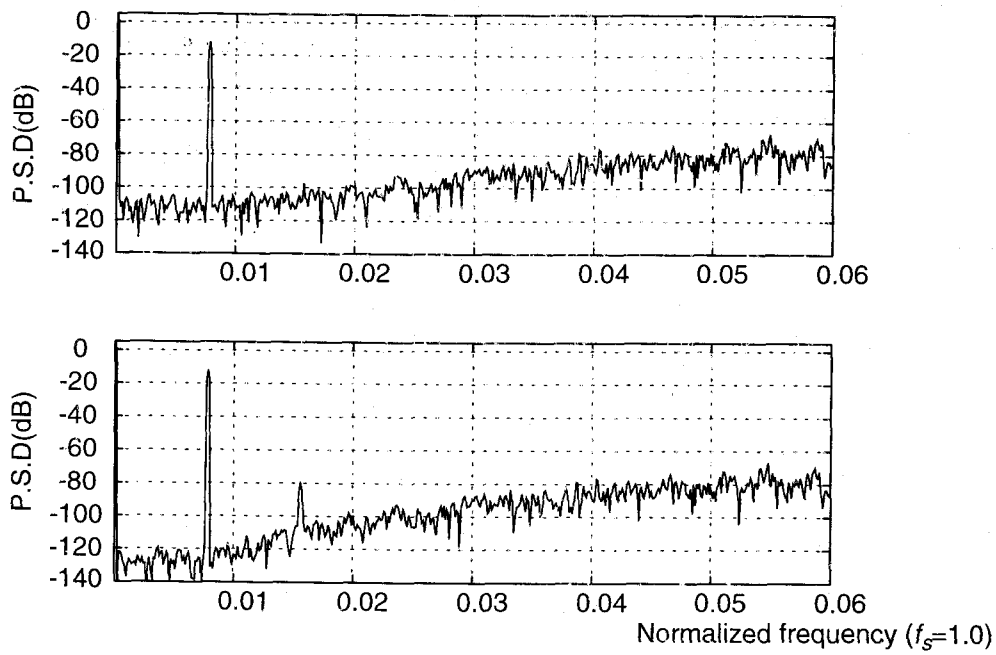


Figure 3.15: Simulation results for the discrete-time model in Figure 3.14: (a) no-shaping; (b) first-order shaping (DWA). The dynamic error is assumed to be 0.1%.

$|x|$, which is responsible for even-order harmonics. Since first-order shaping (DWA) tends to switch elements more frequently, DWA is more sensitive to dynamic errors than the no-shaping case. This explains the higher second-order harmonic distortion in Figure 3.15(b). This model will be used later to derive and simulate the modified mismatch shaping algorithm.

A simplified set of v_{xx} waveforms and the resulting $w_3(t)$ are shown in Figure 3.16(a) and (b). Assuming a transition (either from '0' to '1' or from '1' to '0') occurs at each clock cycle, Figure 3.17 shows that $e_s(t)$ is a periodic signal whose spectrum has tones at multiples of the clock frequency f_s which are shaped by the *sinc* function. The exact waveform of $w_3(t)$ (which depends on the actual v_{xx}) only changes the envelop shown in Figure 3.17(d). Therefore, for constant switching activity, $e_s(t)$ has no effect on the output signal; it only introduces tones at DC and at multiples of the clock frequency. However, if the number of switching events is not periodic, but is instead related to the input signal (as is the case in our delta-sigma modulator and DAC), harmonic distortion and an increased noise floor will occur. Although the return-to-zero (RZ) method can be used to

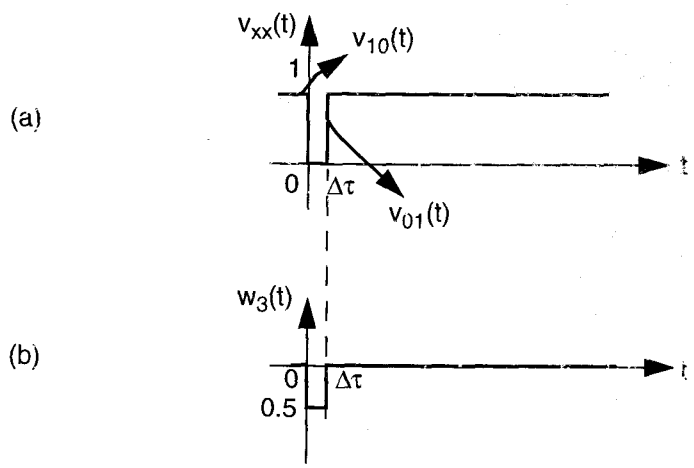


Figure 3.16: (a) Waveform of $v_{xx}(t)$; (b) waveform of $w_3(t)$.

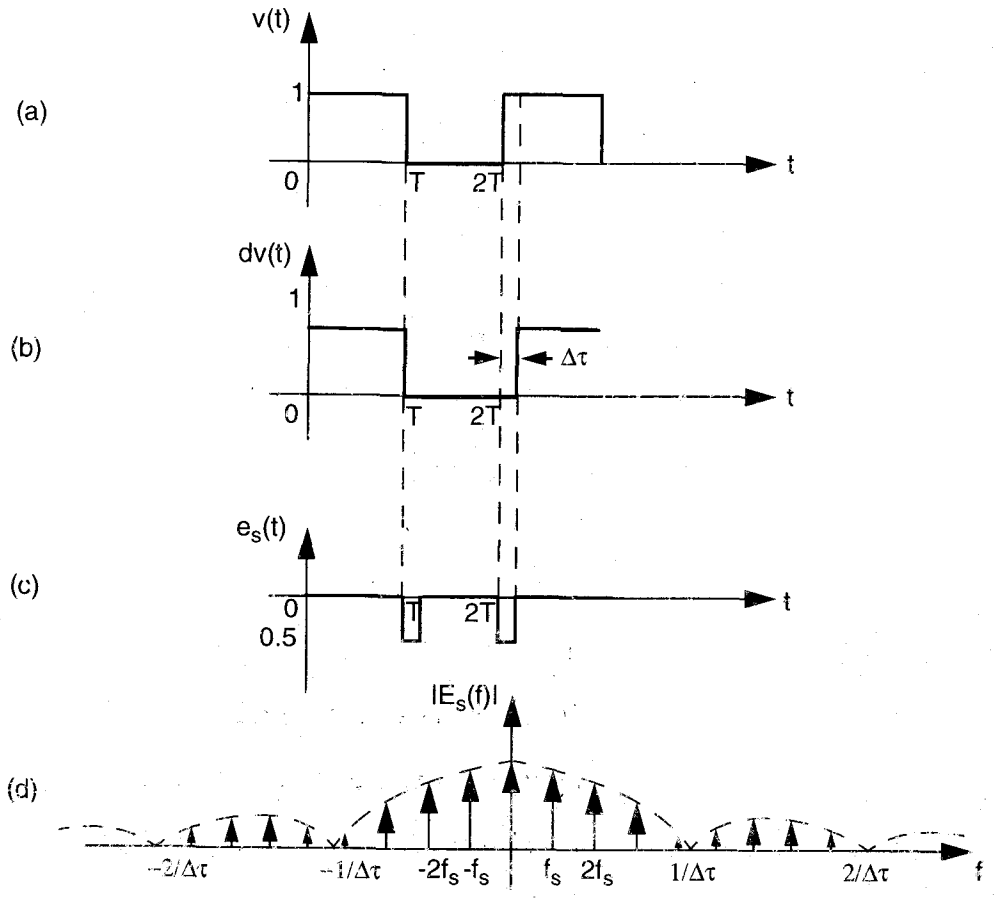


Figure 3.17: Waveforms and spectra of signals assuming a transition at each clock cycle: (a) Waveform of $v(t)$; (b) waveform of $dv(t)$; (c) waveform of $e_s(t)$; (d) spectrum of $e_s(t)$.

avoid the settling dynamics, it eliminates the advantages associated with a smooth time-domain waveform. Modified mismatch shaping can overcome this problem.

3.4.3 Modified mismatch shaping algorithm

According to the foregoing argument, if we make the number of switching events per period a constant, then non-complementary rise/fall dynamics introduce tones at DC and multiples of the clock frequency. This forms the basis of the modified mismatch shaping (MMS) algorithm. The goal of MMS is to:

i) Reduce the dynamic error by making the number of switching events constant

at each clock cycle;

ii) Maintain the effectiveness of shaping on the static mismatch error.

Assume $v(n)$ is the output of a delta-sigma modulator with M+1 quantization levels ($0 \le v(n) \le M$). Define $rem(n)$, $on(n)$ and $off(n)$ as the number of elements which remain on, are turned on, or are turned off, at time step n, respectively. Lastly, let L be the number of elements which switch at each time step. Therefore,

$$on(n) - off(n) = v(n) - v(n-1) \tag{3.30}$$

$$on(n) + off(n) = L \tag{3.31}$$

$$rem(n) + on(n) = v(n). \tag{3.32}$$

By solving these equations, we have:

$$on(n) = (L + v(n) - v(n-1))/2 \tag{3.33}$$

$$off(n) = (L - v(n) + v(n-1))/2 \tag{3.34}$$

$$rem(n) = (v(n) + v(n-1) - L)/2. \tag{3.35}$$

The constraints $on \ge 0$, $off \ge 0$ and $rem \ge 0$ impose restrictions on the input $v(n)$ and the choice of L. Specifically, $v(n)$ and L should satisfy

$$|\Delta v(n)| \le L \tag{3.36}$$

$$v(n) + v(n-1) \ge L. \tag{3.37}$$

The requirement that $on(n)$, $off(n)$ and $rem(n)$ be integers adds further restrictions on $v(n)$. Specifically, if L is even, $v(n)$ must either be a sequence of even numbers or a sequence of odd numbers. These restrictions can be avoided if L can be adjusted dynamically. There are four possible conditions under which those parameters need to be adjusted:

i) When the sum of number of elements to be turned on ($on(n)$) and the number of elements already on ($v(n-1)$) is greater than the total number of elements M, i.e.

$$on(n) + v(n-1) > M. \tag{3.38}$$

In this case, the following adjustments need to be made to ensure proper operation:

$$on(n) = M - v(n-1) \tag{3.39}$$

$$off(n) = M - v(n) \tag{3.40}$$

$$L = 2M - v(n-1) - v(n). \tag{3.41}$$

ii) When the number of elements to be turned off at time n ($off(n)$) is less than the number of elements which are already on at time $n-1$ ($v(n-1)$):

$$off(n) > v(n-1). \tag{3.42}$$

This condition will occur when $v(n)$ and $v(n-1)$ are small. Therefore, the switching activity L needs to be decreased, leading to the following adjustment:

$$on(n) = v(n) \tag{3.43}$$

$$off(n) = v(n-1) \tag{3.44}$$

$$L = on(n) + off(n). \tag{3.45}$$

iii) When $on(n) < 0$ In this case,

$$on(n) = 0 \tag{3.46}$$

$$off(n) = v(n-1) - v(n) \tag{3.47}$$

$$L = v(n-1) - v(n). \tag{3.48}$$

iv) When $off(n) < 0$. In this case,

$$off(n) = 0 \tag{3.49}$$

$$on(n) = v(n) - v(n-1) \tag{3.50}$$

$$L = v(n) - v(n-1). \tag{3.51}$$

The implementation of MMS can be best understood by referring to Figure 3.18. This figure takes the general form of the mismatch shaping system of Figure 3.1, except that the vector quantizer (VQ) now takes into account the relations of Eq. (3.33) to Eq. (3.35) when it decides which elements to turn on or turn off. This extra requirement adds state information to the VQ; no longer does the VQ base its decisions solely on the current value of the input $v(n)$ and the current value of the "desired element usage" vector $\boldsymbol{sy}(n)$. The procedure is summarized below:

i) Calculate the number of elements to turn on/off.

ii) From the elements which are on, de-select the $off(n)$ elements with the smallest $\boldsymbol{sy}(n)$ components, i.e. those elements with the least "desired usage."

iii) From the elements which are off, select the $on(n)$ elements possessing the largest $\boldsymbol{sy}(n)$ components, i.e. those elements with the greatest "desired usage."

In this algorithm, by keeping the switching activity nearly constant, the detrimental effects of dynamic errors are reduced. Meanwhile, the noise-shaped element usage is still

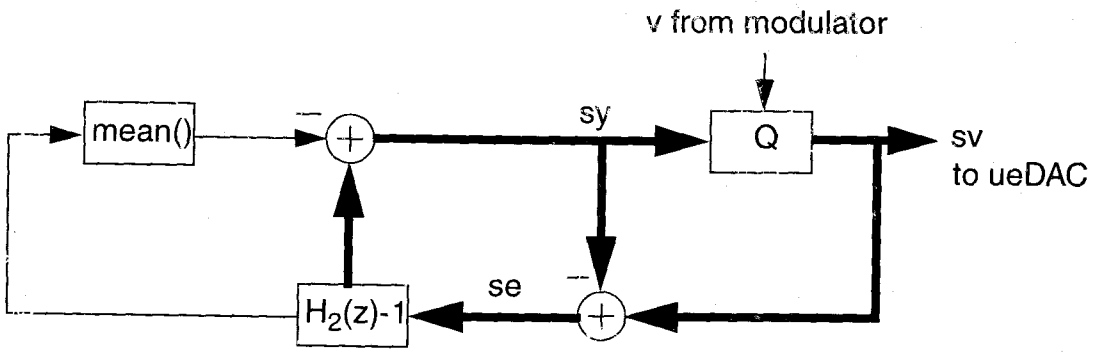


Figure 3.18: Block diagram of modified mismatch shaping (MMS).

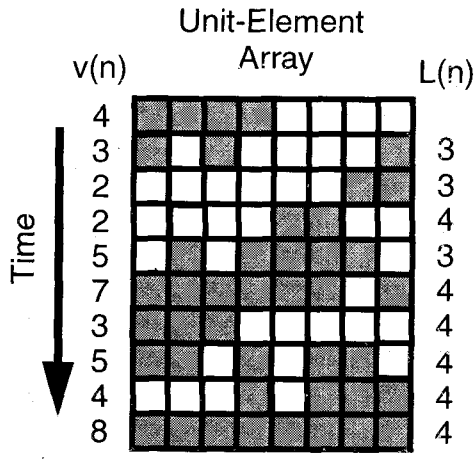


Figure 3.19: One example of element usage pattern in MMS.

preserved by feeding the 'desired element usage' vector *sy(n)* into a feedback loop. The danger is that the extra constraints on the vector quantizer Q might make the ESL unstable. Fortunately, simulations indicate that the MMS algorithm yields a stable ESL.

Figure 3.19 shows one example of the element usage pattern when MMS is applied. Here the initial value of L is 4. It can be seen that the number of switched elements at each time step is fairly constant (either 3 or 4). Since the number of elements which switch state at each time step is not fixed, the dynamic error is not truly constant. To make the number of elements which switch constant, the output of the driving modulator must be restricted, as described earlier. Since such constraints effectively reduce the resolution of the multi-bit quantizer, the number of elements which switch has been allowed to vary.

3.4.4 Simulation results

Results of a MATLAB simulation of the above algorithm are shown in Figure 3.20. Here, a third-order $\Delta\Sigma$ modulator with a 9-level quantizer generates $v(n)$. The DAC is assumed to have 1% mismatch error and 0.1% dynamic error. As the middle plot shows, DWA can improve the SNDR by about 10 dB over the non-shaped case (61 dB vs. 50 dB),

but a strong second harmonic will still be present. By making the number of elements which switch nearly constant, MMS is able to eliminate the second harmonic and improve the SNDR by another 10 dB. A careful study of Figure 3.20 shows that MMS provides a trade-off between the degradation caused by static error and that caused by dynamic error. Compared with DWA, MMS decreases the harmonic distortion at the cost of a slightly higher noise floor at low frequencies. Thus, MMS is most useful in systems where both dynamic error and static error coexist, such as a continuous-time current-mode DAC.

3.5 Implementation Considerations

In this section, implementations of lowpass, bandpass and modified mismatch shaping are explained.

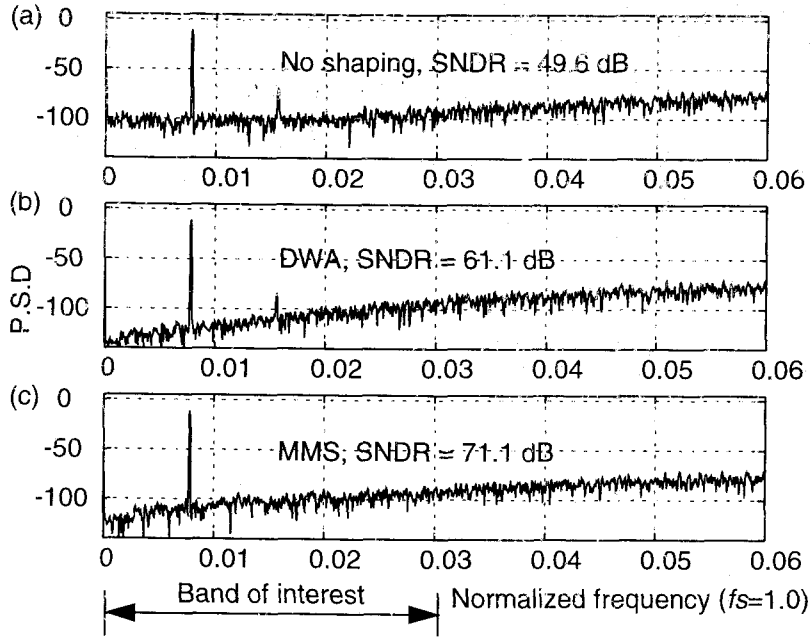


Figure 3.20:. Simulation results for (a) no mismatch-shaping; (b) first-order shaping; (c) MMS.

3.5.1 Lowpass mismatch shaping

According to the algorithm described in Section 3.2, first-order lowpass mismatch shaping requires the following steps:

i) The input signal $v(n)$ is converted to a positive number: $v'(n)=v(n)+M/2$;

ii) The new pointer location $ptr(n)$ is computed: $ptr(n)=\text{mod}(ptr(n-1)+v'(n),M)$;

iii) The element selection vector is generated by selecting elements between $ptr(n)$ and $ptr(n-1)$.

An implementation of this algorithm for an M=16-elemented DAC is shown in Figure 3.21. Since the addition in step (ii) needs to be done modulo M, the accumulator used can be implemented with an ordinary full adder which allows overflow naturally, assuming M is a power of 2. The *'Tro_16'* block converts the input $v(n)$ from a bipolar signal to a positive- numbered signal. The 5-bit full adder serves as the *ptr* accumulator while the EXOR logic block and the thermometer encoder (labeled as *'Therm'*) perform the differentiation function. This implementation requires fewer than 200 gates, which is a very

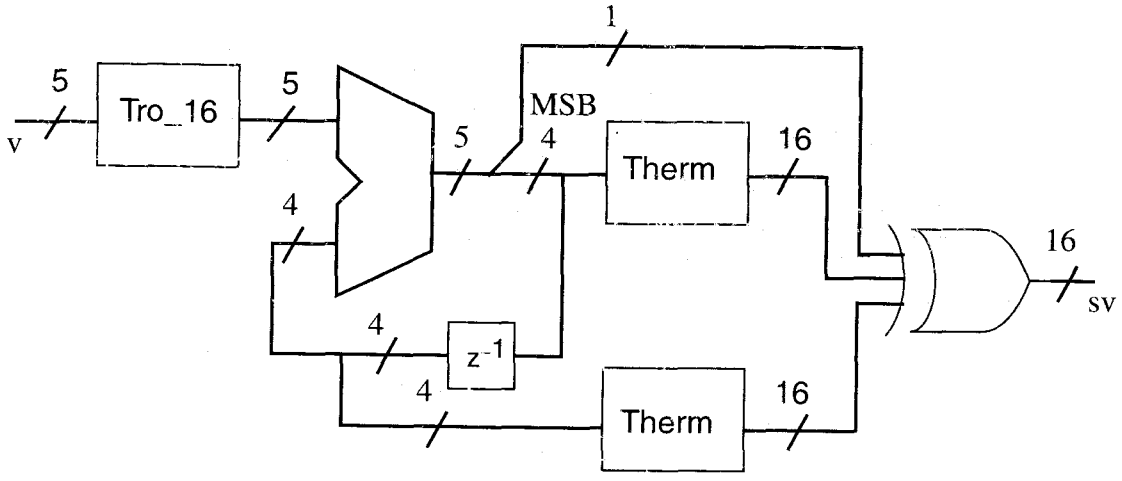


Figure 3.21: An implementation of the element rotation logic for lowpass mismatch shaping.

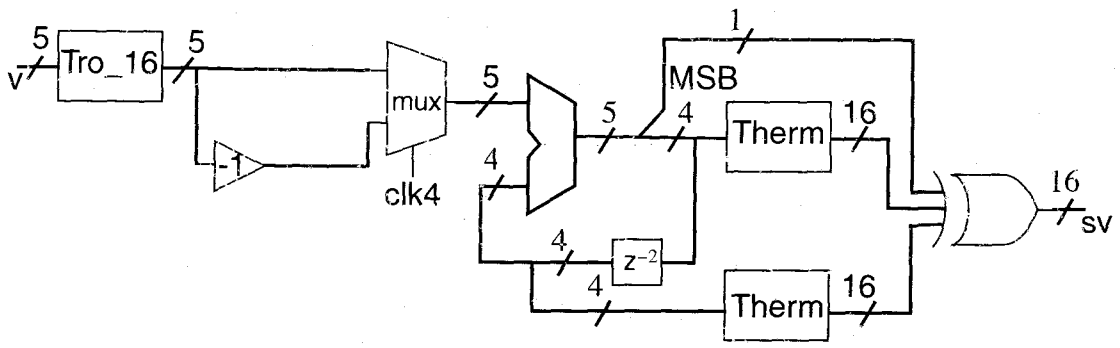


Figure 3.22:An implementation of bandpass element selection logic.

small amount. For larger M, the hardware cost is dominated by the thermometer decoder and the EXOR gates.

3.5.2 Bandpass mismatch shaping

The implementation of second-order bandpass mismatch shaping is quite similar to the above, requiring only a doubling of the number of registers and a more complicated *ptr* updating circuit, as shown in Figure 3.22. Since the element index pointer $ptr(n)$ alternatively increases and decreases by $v'(n)$, both $v'(n)$ and $-v'(n)$ are computed. The multiplexer '*mux*' selects v' or $-v'$ according to the period-4 signal *clk4*.

3.5.3 Modified mismatch shaping

A direct implementation of the system shown in Figure 3.18 results in a huge amount of hardware, especially for the sorting function of the vector quantizer. Since the system will be implemented on a Xilinx field programmable gate array (FPGA) [51], the algorithm must be simplified so that the logic is within the capacity of the FPGA.

First, consider the *mean()* block. Its purpose is to reduce the magnitude of the $\boldsymbol{sy}$ vector by a scalar so that the error vector $\boldsymbol{se}$ remains bounded. Since the scalar used for normalization can be anything, it suffices to simply subtract $\boldsymbol{sy}_1(n)$ from $\boldsymbol{sy}(n)$. The

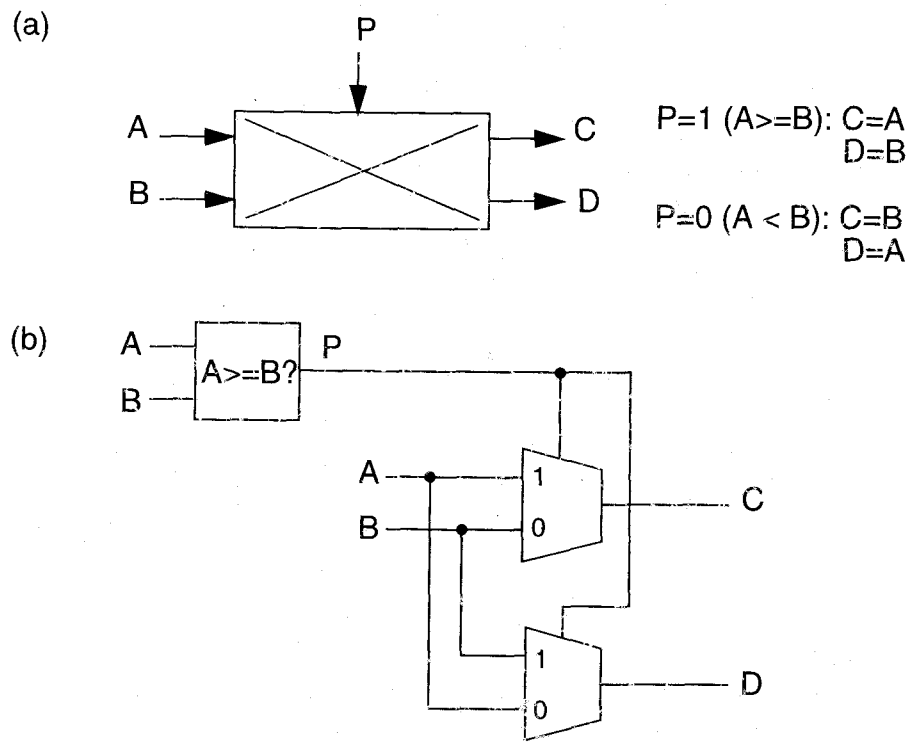


Figure 3.23: Swapper cell used in sorting block: (a) symbol; (b) logic schematic.

components of $\boldsymbol{sy}(n)$ are no longer positive-only, but the goal of removing a common component from $\boldsymbol{sy}(n)$ is achieved.

Next, the sorting function which is used in the vector quantizer block needs to be simplified. A complete sorting of M k-bit numbers in one clock cycle requires about

$$\frac{\log M(\log M+1)}{2}\cdot\frac{M}{2}\cdot 24k \tag{3.52}$$

logic gates [55]. When M=8 and k=3, this accounts for about 1728 gates. Fortunately, the modified mismatch shaping algorithm does not require a full sorting of all the elements in the $\boldsymbol{sy}(n)$ vector. Instead, as shown in Section 3.4.3, only a few elements (namely $off(n)$ and $on(n)$) need to be sorted out. From Eq. (3.31), both off and on must be less than or equal to L, which is 4 in our application. Therefore, a partial sorting block which selects the four smallest numbers is all that is required.

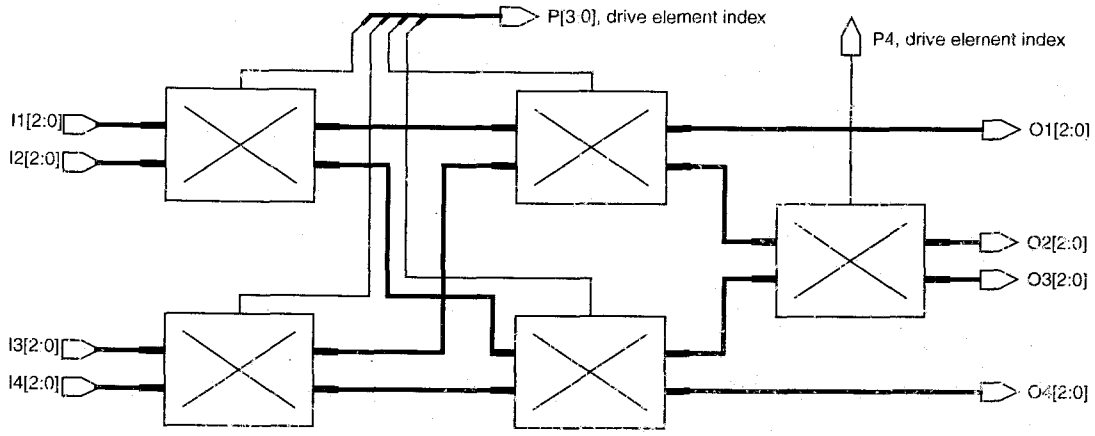


Figure 3.24: Sorting block for 4 input ('*sort_4*').

Instead of sorting the elements in several steps, as is commonly used in some applications [52], a one-step sorting algorithm is developed. This algorithm is based on the use of a swapper cell, which is shown in Figure 3.23. This cell determines which input is larger and routes that input to the top (C) output. The cell has a 1-bit output signal P which indicates if the inputs were swapped or not. A four-element complete sorting block (called '*sort_4*') is shown in Figure 3.24. It is the building block for the 8-element partial sorting block shown in Figure 3.25. It can be seen that only the first four smallest elements are sorted in a strict sense, whereas the other elements may or may not be in correct order. The effectiveness of this partial-sorting vector quantizer has been simulated and verified.

From the algorithm described in Section 3.4.3, two sorting operations need to be performed for a given input $v(n)$. One determines the elements to be turned on, the other determines the elements to be turned off. To save hardware, these two operations can be multiplexed in time. Therefore, the '*sort_8*' block only needs to identify the smallest numbers, since the four maximum numbers can be found with the same block by just reversing the sign of the input signals.

The timing graph for MMS is shown in Figure 3.26. For a given *v(n)*, the entire operation requires four phases to generate the corresponding ***sv(n)***. The critical operation includes the partial sorting and turning on/off operations in $\Phi 2$ and $\Phi 3$ within the vector quantizer. The system diagram of the vector quantizer is shown in Figure 3.27. When the *'CLK'* signal is high, the *'on_off_cal'* block calculates the value of *on* and *off* using Eq. (3.33) and Eq. (3.34). When any one of the restrictions shown in Eq. (3.36) and Eq. (3.37) is violated, the *'on_off_cal'* block will automatically determine the appropriate value of *on* and *off*, using Eq. (3.38) to Eq. (3.51). During $\Phi 2 = 1$, the elements with the smallest desired usage are sorted out by the *'sort_8'* and *'sort_8ind'* blocks and turned off.

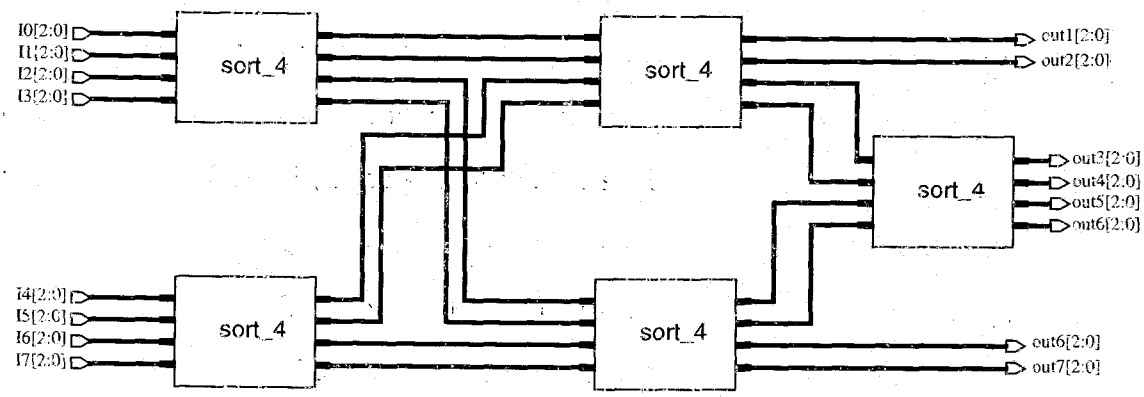


Figure 3.25: Partial sorting block for 8 inputs (*'sort_8'*).

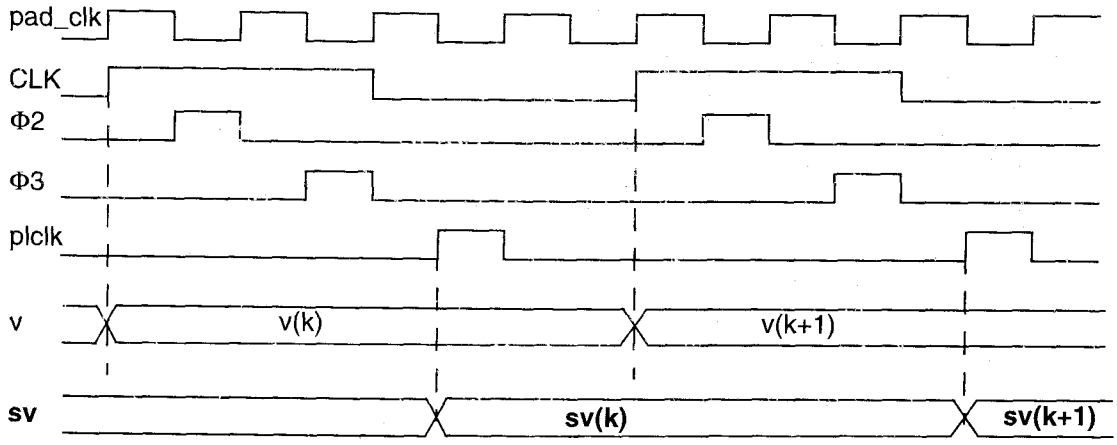


Figure 3.26: System timing for MMS.

During $\Phi 3 = 1$, the elements with the highest desired usage are identified and turned on. The *sv* vector is latched at the rising edge of *plclk* and is then ready to drive the DAC.

The complete schematic of the MMS element selection logic is shown in Figure 3.28. It follows the structure of Figure 3.18 with $H_2(z) = 1 - z^{-1}$. The number of gates used for MMS is about 3000 (the partial sorting block consumes about 750 gates), which is within the capacity of the FPGA XC4010E used in this application.

3.6 Summary

Mismatch shaping can push the mismatch-induced error of a multi-bit $\Delta\Sigma$ data converter out of the band of interest in much the same way as a $\Delta\Sigma$ modulator shapes quantization noise. In this chapter, the principle of general mismatch shaping was

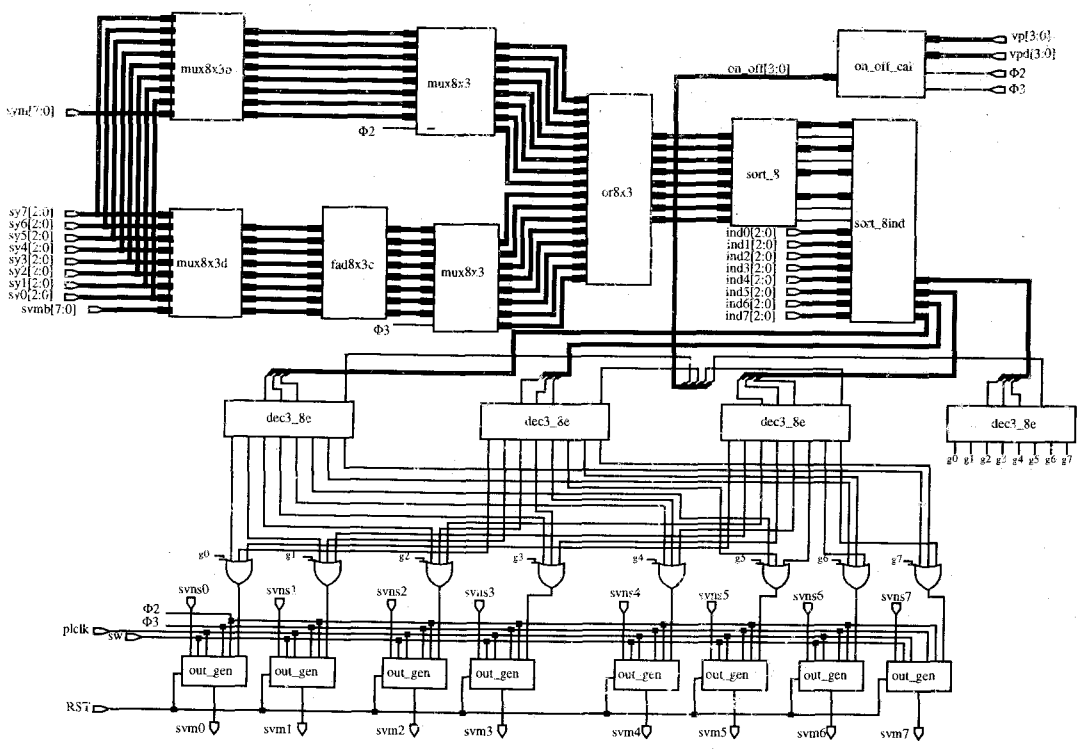


Figure 3.27: Schematic of vector quantizer Q.

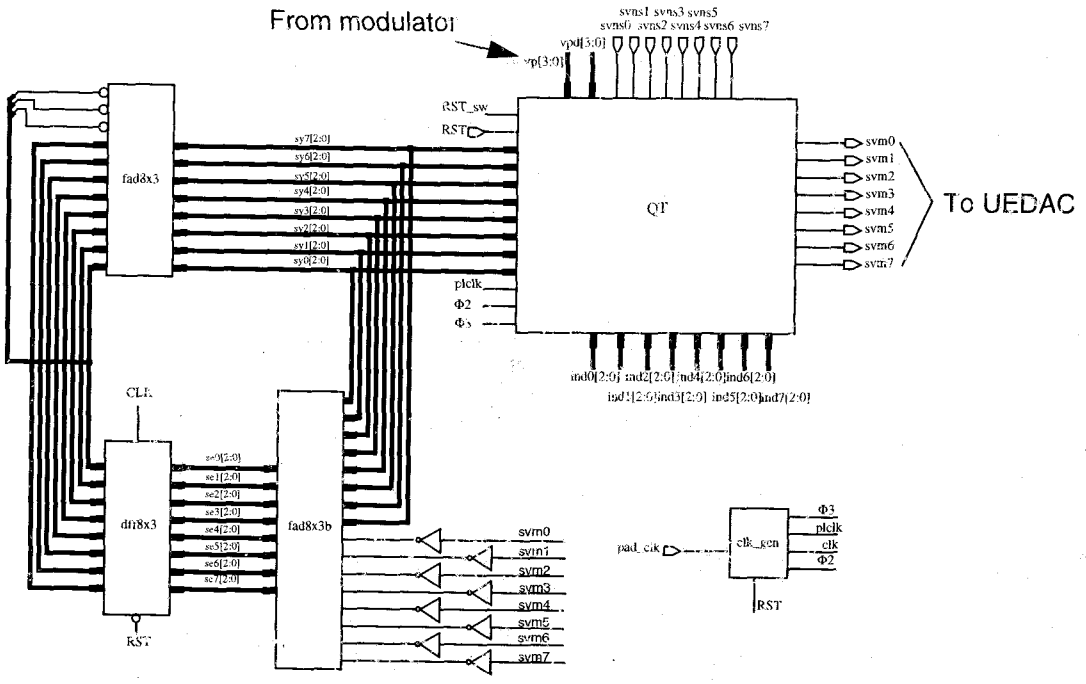


Figure 3.28: System schematic of MMS.

introduced. Algorithms for first-order lowpass and second-order bandpass mismatch shaping were given. An improved algorithm, namely modified mismatch shaping, was developed to address the dynamic error in a continuous-time system. Simulations were used to validate these methods and their hardware implementations were examined.

Chapter 4. Test of Current-Mode Unit Element DAC (UEDAC1)

In the last chapter, the principle and algorithms for mismatch shaping were described. In this chapter the performance of a current-mode unit element DAC (UEDAC1) is evaluated. UEDAC1 is used as a test bed for the mismatch shaping algorithms presented in the last chapter. Error source analysis is performed which calls for the design of a new unit element DAC.

4.1 Current-mode Unit Element DAC (UEDAC1)

4.1.1 Circuit description

The first version of a current-mode unit element DAC (UEDAC1) was designed by Jose da Silva [54] and fabricated in the Orbit 1.2 μm CMOS process. A system diagram of the DAC is shown in Figure 4.1(a). UEDAC1 consists of 16 differential regulated-cascode current sources, each of which constitutes a unit element. A unit element drives one of its two output nodes according to its input sv. Eq. (4.1) and Eq. (4.2) describe the input-output relation of UEDAC1:

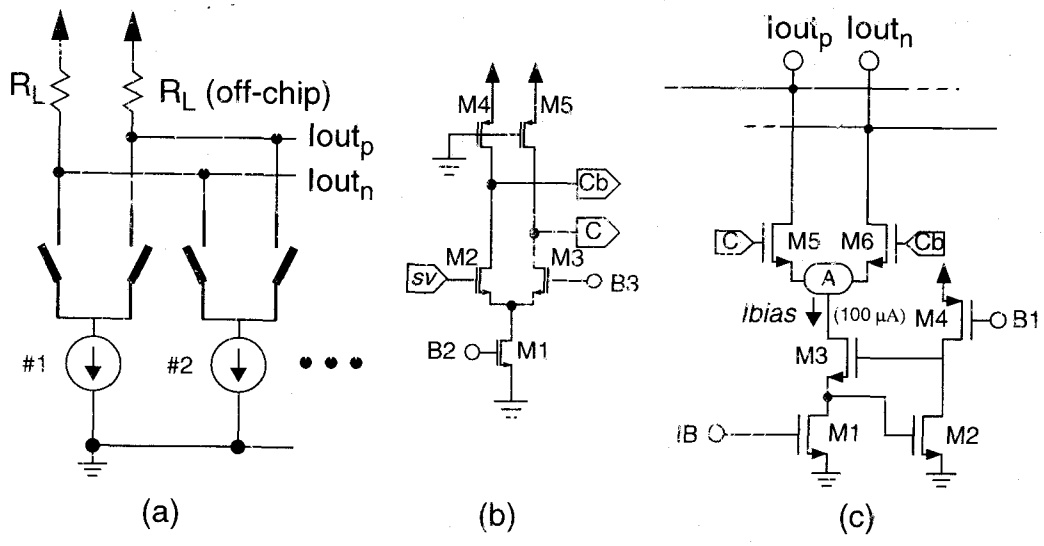


Figure 4.1: Unit-element DAC (UEDAC1): (a) system diagram (b) clock driver (c) unit-element.

$$Ioutp = Io \times \Sigma sv \tag{4.1}$$

$$Ioutn = Io \times (16 - \Sigma sv), \tag{4.2}$$

where Io is the current in each current source.

The schematic for the clock driver and unit element are shown in Figure 4.1(b) and Figure 4.1(c), respectively. The clock driver converts the input digital signal into a pair of differential signals which quickly steer the current from one output branch to the other. A regulated cascode structure is used in each current source to make the output current of each source constant. The transistor sizes are shown in Table 4.1.

Clock Driver	
M_1	20/2
$M_{2,3}$	50/1.2
$M_{4,5}$	7/1.2

Unit Element	
M_1	30/10
$M_{2,3}$	50/3
M_4	4.2/1.2
$M_{5,6}$	10/1.2

Table 4.1:Transistor dimensions of UEDAC1

4.1.2 Test results

First, a DC test is performed to measure the value of individual current sources; the result (normalized to $Io = 100uA$) is shown in Figure 4.2. The matching of the current sources is σ=0.67%. Due to the floor plan of the layout, there exists an even symmetry in the value of the current sources. As we shall see later in this chapter, this has a direct effect on the modulator output spectrum.

To verify the effectiveness of a mismatch-shaping algorithm, the unit element DAC is used as the DAC following a third-order lowpass multi-bit delta-sigma modulator. The design of the delta-sigma modulator is straightforward with the help of the "delta-sigma

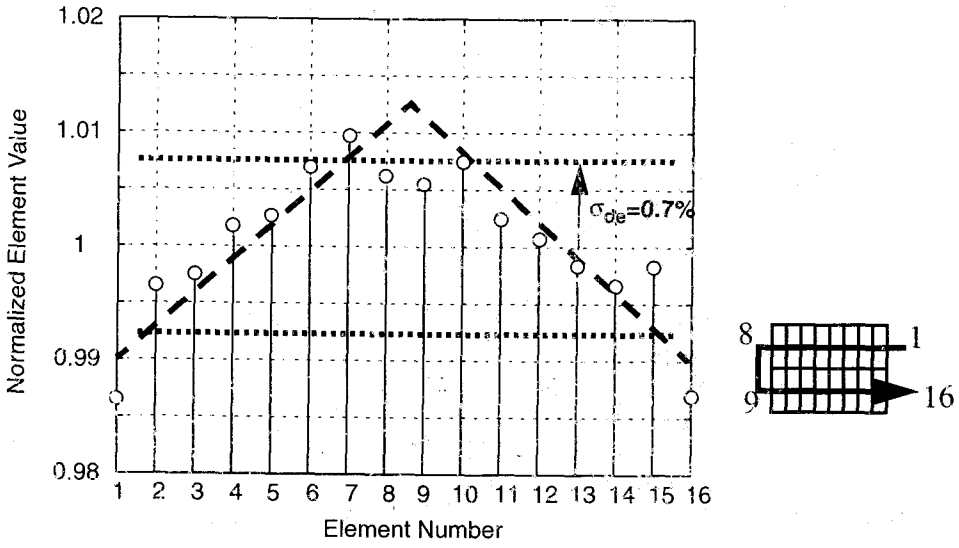


Figure 4.2: Matching of the current sources, reflecting the layout shown on the right.

toolbox" [56]. The modulator is implemented in "cascaded integrators with feedback (CIFB) topology with 17 quantization levels (corresponding to 16 unit elements). Its block diagram is shown in Figure 4.3. The designed SNR is 100 dB with an oversampling ratio of 32. Figure 4.4 shows the modulator output spectrum and output waveform for a half-scale input.

The performance of UEDAC1 and the 3rd-order delta-sigma modulator is measured using the test setup depicted in Figure 4.5. A digitized sinusoidal signal is stored in an EPROM. The interpolation filter can be omitted in this configuration because the input

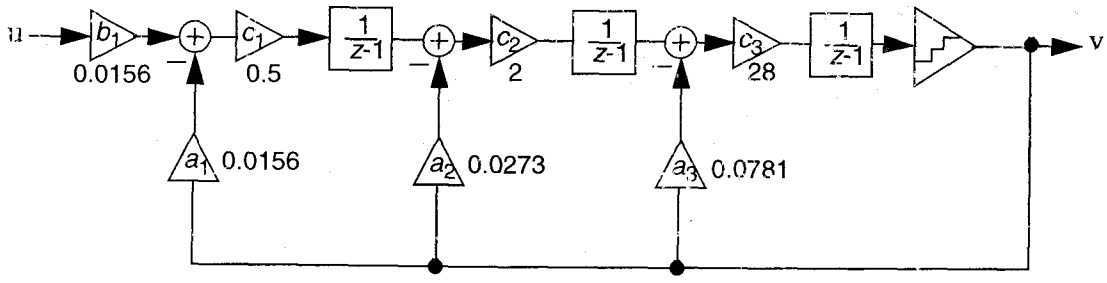


Figure 4.3: Block diagram of the third-order delta-sigma modulator.

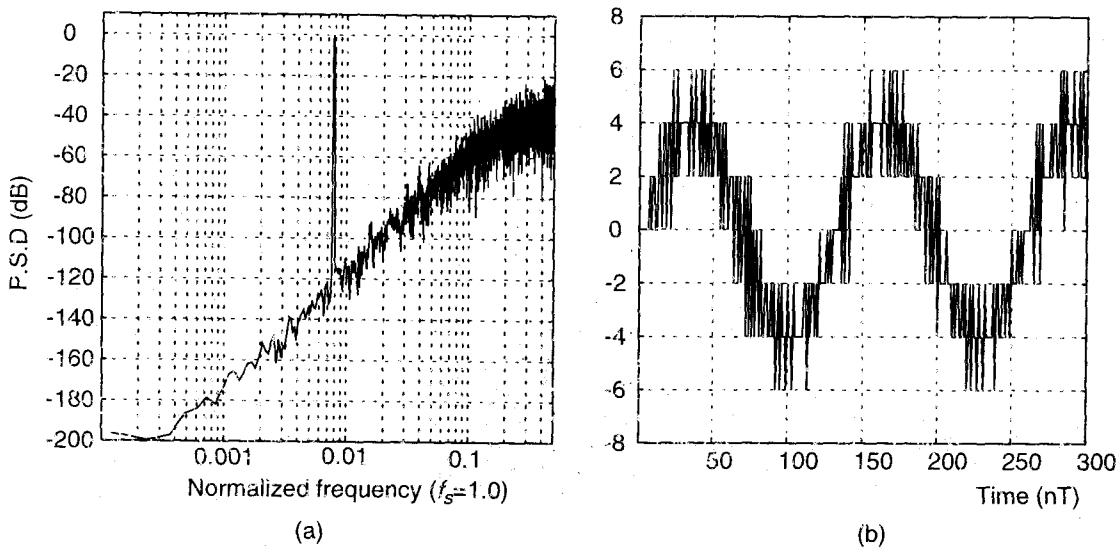


Figure 4.4: Simulated result of the third-order 17-level modulator with a half-scale input: (a) spectrum (b) time-domain waveform.

signal is stored in its oversampled form in the EPROM. The modulator and element selection logic (ESL) are implemented on a Xilinx field programmable gate array (FPGA). The element selection vector *sv* is used to drive the UEDAC1, and the output is observed directly on an HP3585B spectrum analyzer. By virtue of the flexibility of the FPGA, various orders of modulator and various mismatch-shaping algorithms can be implemented and tested conveniently, although not at the clock rate that could be achieved with a custom IC.

The measured output spectrum is shown in Figure 4.6 for a low sampling frequency. Compared with the no-shaping case, first-order mismatch-shaping suppresses the

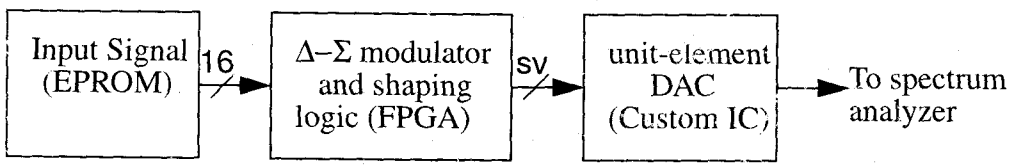


Figure 4.5: System used to implement and test the mismatch-shaping algorithm and UEDAC.

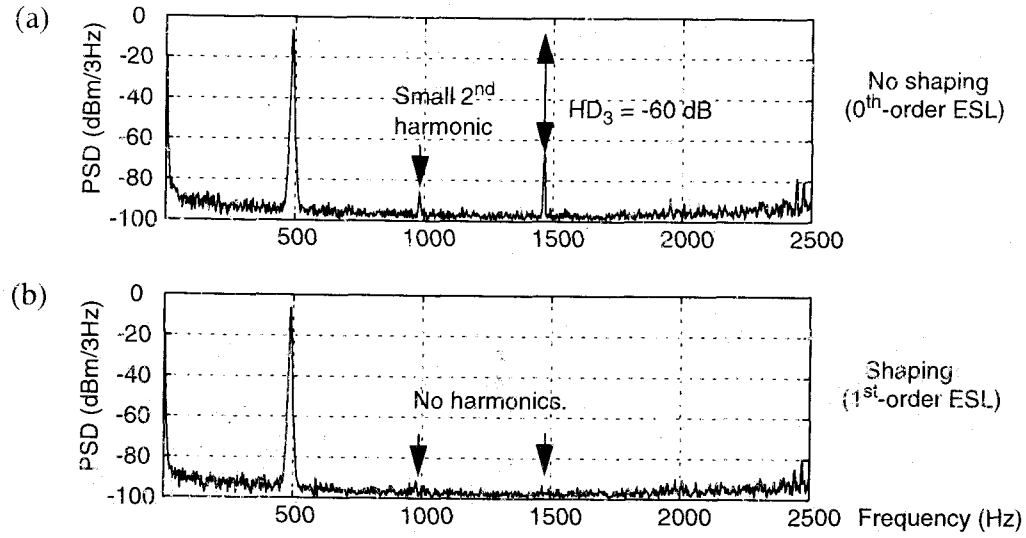


Figure 4.6: Measured UEDAC1 spectrum: (a) no shaping; (b) shaping.

harmonics of the DAC by more than 30 dB. Therefore, the linearity of the multi-bit delta-sigma modulator is greatly improved. Note that only a small second-order harmonic is visible when plain thermometer coding is used. This phenomenon can be attributed to the nearly even symmetry of the current sources, which precludes even-order harmonics. This conclusion has been verified by MATLAB simulation. Of course, a DC offset on the sine wave would effectively destroy the even symmetry and then cause a second-order harmonic to appear.

If the sampling frequency is increased, mismatch shaping fails to provide improved performance. Figure 4.7 shows the measured second-order harmonic distortion (HD_2) as a function of the sampling frequency f_s. The theoretical HD_2 is also shown in this plot. Theoretically, mismatch-shaping should shape the mismatch-caused errors in the band of interest (demonstrated as the suppression of the harmonics and in-band noise), independent of f_s. However, measurements show that mismatch-shaping only works well at low sampling frequencies (i.e. $f_s < 100\,\text{kHz}$). A particularly disturbing discovery is that even though the 3rd harmonic is generally suppressed when shaping is used, the 2nd harmonic increases. The degradation of the mismatch-shaping performance indicates that other error

sources dominate the element mismatch error. An analysis of potential error sources is performed in the next section.

4.2 Error Analysis of UEDAC1

4.2.1 Element mismatch error

Element mismatch error is a major error source in a multi-bit delta-sigma DAC. Mismatch results in linearity degradation and an increased noise floor in the band of interest. According to our experiment, at low sampling frequencies the element mismatch

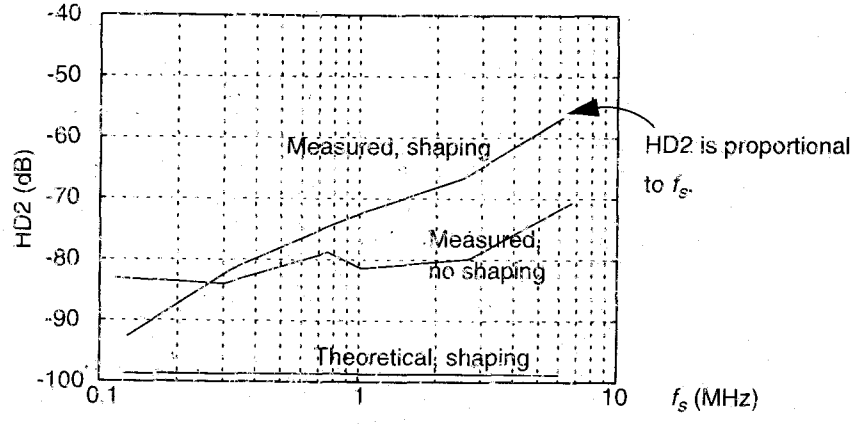


Figure 4.7: Measured HD_2 vs. sampling frequency for UEDAC1.

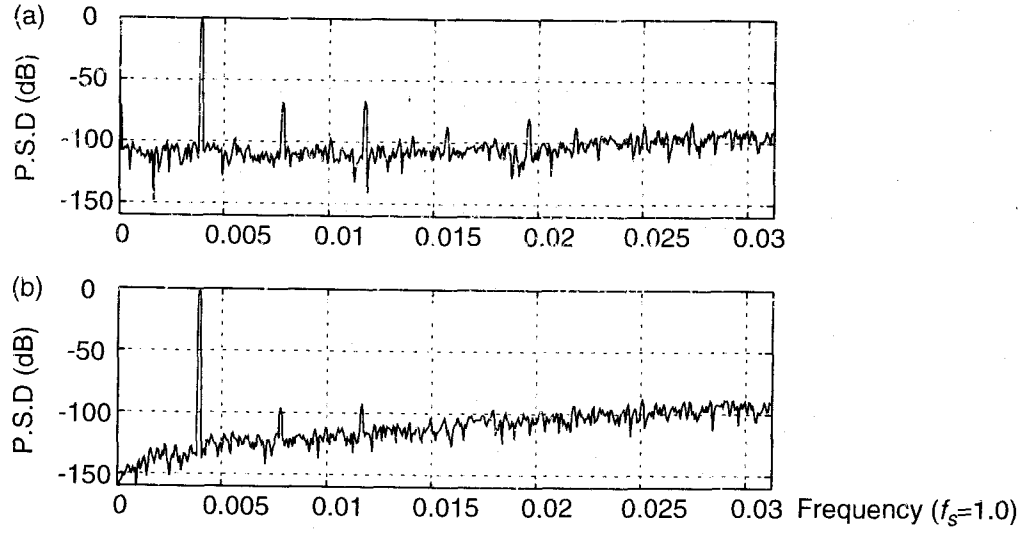


Figure 4.8: Simulated spectrum with measured element value:
(a) no shaping; (b) shaping.

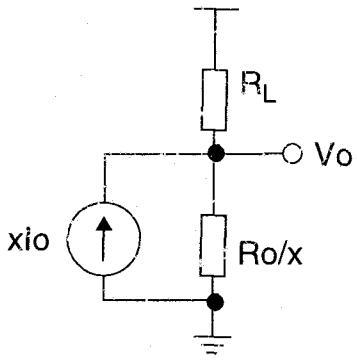


Figure 4.9: Model for finite output impedance distortion calculation.

error is the dominant error source. This deduction has been verified through simulation by feeding the current values measured in Section 4.1.2 to the simulation program. Figure 4.8 shows the predicted performance of the DAC before and after the application of mismatch-shaping. It should be noted that in the no-shaping case, the measured HD_2 is actually better than the HD_2 predicted by simulation. An explanation is given in [57] to account for this discrepancy. In short, a 0.07 uA measurement error is sufficient to increase the degree of even symmetry to the point where the simulated HD_2 is reduced to that observed in the measured spectrum. With mismatch-shaping applied, the simulations predict HD_2 = −95dB and HD_3 = −100dB, which agrees with the experiment. Of course, the increase of HD_2 with f_s cannot be explained by the element mismatch error. Another explanation needs to be found.

4.2.2 Finite output impedance

The finite output impedance of each current source in UEDAC1 has a direct impact on the linearity of the DAC. A model to quantify this effect is shown in Figure 4.9. Here the DAC is modeled as a current source with a current value Io and a finite output impedance Ro. x is the input to the DAC, it is a non-negative number and indicates x elements need to be turned on. R_L is the off-chip resistor. When an input x is applied, the output voltage Vo becomes

$$V_o = xI_o \cdot \frac{R_L R_o}{R_o + xR_L}. \tag{4.3}$$

If $R = R_o/R_L$ is the relative resistance, Eq. (4.3) becomes

$$V_o = \frac{x}{1+\frac{x}{R}} I_o R_L. \tag{4.4}$$

Using Taylor series to expand Eq. (4.4), we get:

$$Vo \cong xI_o R_L \cdot \left(1 - \frac{x}{R} + \frac{x^2}{R^2}\right) = \left(x - \frac{x^2}{R} + \frac{x^3}{R^2}\right) I_o R_L \tag{4.5}$$

$$HD_2 = \frac{x}{R}, x \in [0, M] \tag{4.6}$$

where M is the number of unit element.

Thus, the finite output impedance of each current source can produce harmonic distortion. For example, in our experiment the off-chip load resistance is chosen to be $R_L = 560\Omega$ and the current source output impedance is $R_o > 10M\Omega$, thus $R > 17800$. An estimation from Eq. (4.6) results in a second-order distortion $HD_2 = -85\text{dB}$.

The above argument has been confirmed using simulations. Figure 4.10 shows the simulation result under the condition $R = 17800$. It is clear that the finite impedance of the current source not only degrades the linearity, but also increases the in-band noise floor and reduces the SNR by almost 20 dB. Since the error caused by the finite output impedance is frequency-independent, it should be observed in all measurements, regardless of the sampling frequency. However, in our measurement, the degradation of the linearity caused by this error source is not present at low sampling rates. Therefore, it can be concluded that the finite output impedance of the current source is not a limiting factor in

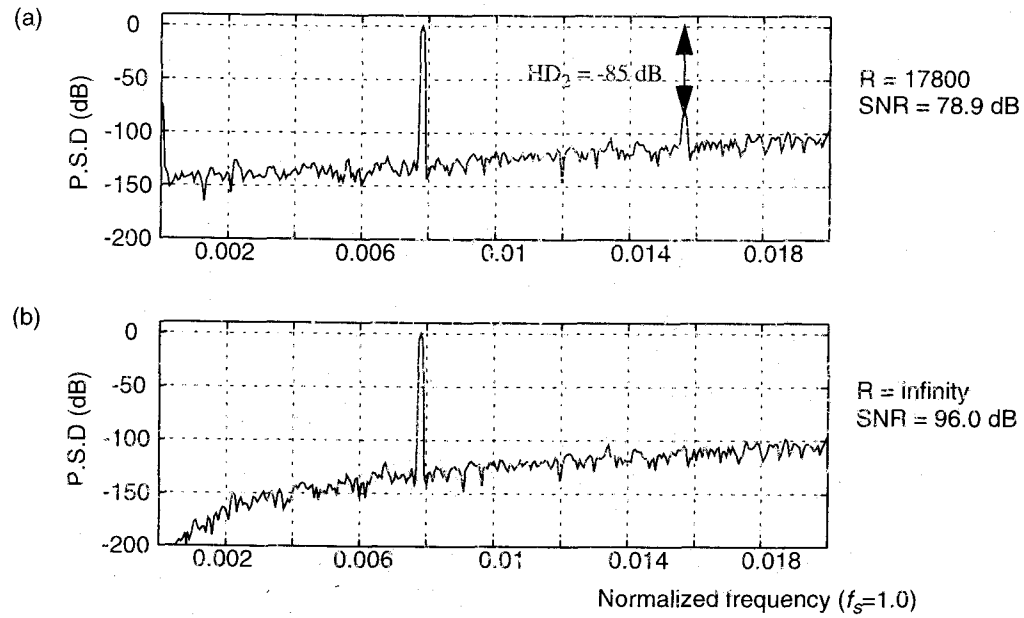


Figure 4.10: Simulated spectrum considering finite output impedance: (a) R = 17800; (b) R = infinity.

the performance of the UEDAC. According to our simulation, the output impedance of the current source should be greater than $30M\Omega$ to make $HD_2 \leq -90\text{dB}$ and $SNR \geq 87\text{ dB}$.

4.2.3 Clock jitter

The effect of clock jitter on the sampling function of an ADC has been well studied [58], with the conclusion that if clock jitter is random, it will introduce a white noise whose in-band power can be computed in the following way. Assume a sinusoidal input signal

$$x(t) = A\sin 2\pi f_x t, \tag{4.7}$$

due to jitter, the sampling instant is shifted by δ, so that the error signal $e(t)$ becomes

$$e(t) = x(t+\delta) - x(t) \approx 2\pi f_x A\delta \cdot \cos 2\pi f_x t. \tag{4.8}$$

If δ is a random variable with zero-mean and standard deviation σ_j, then the jitter error power is

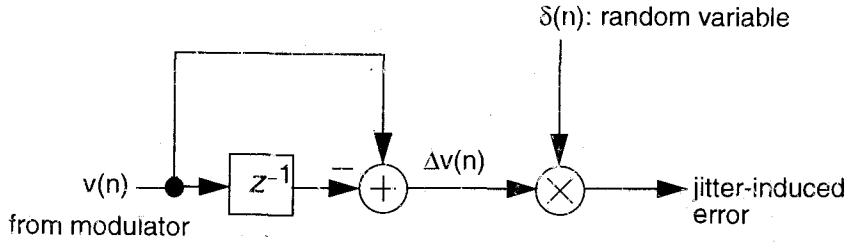


Figure 4.11: Model for clock jitter simulation and analysis.

$$P_J = E[e^2(t)] = E[4\pi^2 f_x^2 A^2 \delta^2 \langle \cos 2\pi f_x t \rangle^2] = 2\pi f_x^2 A^2 \sigma_j^2 \quad . \tag{4.9}$$

In a delta-sigma modulator, the jitter noise power within the band of interest benefits from oversampling:

$$\sigma^2 = \frac{2\pi \cdot f_x^2 \cdot A^2 \cdot \sigma_j^2}{R}, \tag{4.10}$$

where R is the oversampling ratio. This result applies to a delta-sigma DAC as well.

In the ΔΣ DAC, due to the inherent oversampling behavior, the clock jitter problem can be as a severe problem. A model is used to simulate the effect of clock jitter on the performance of the DAC, as shown in Figure 4.11. A simulation result is shown in Figure 4.12 to demonstrate the effect of clock jitter on the SNR of the DAC. It can be seen that as predicted by Eq. (4.10), the roll-off of the SNR is 20dB per decade of rms jitter. It is also interesting to note that increasing the number of DAC levels can help to reduce the jitter power. Having more levels helps because the step sizes are reduced.

The above analysis and simulation does not consider the effect of element mismatch, which dominates the performance of UEDAC1 when no shaping is employed. If we assume there exists a 1% mismatch between the 16 unit elements and rms clock jitter is independent of the sampling clock period (which is reasonable since it is mostly caused

by crystal phase noise, power/ground bounce, etc.), then at the low frequency range, UEDAC1 with mismatch-shaping can effectively shape the mismatch noise and harmonic power in the band of interest. The noise introduced by clock jitter dominates in baseband. But for the no-shaping DAC, the SNR is dominated by mismatch-caused noise and shows little dependence on the clock frequency.

The analysis above has been verified by simulation. Figure 4.13 shows the behavior of the DAC under test versus clock jitter when a 1% element mismatch exists. It is obvious that in the shaping case, the SNR of the DAC is much more sensitive to the jitter problem than in the no-shaping case, where the mismatch noise is dominant at baseband and the jitter-introduced noise is masked. However, when the jitter value is large enough, the two curves coincide with each other.

By comparing Figure 4.7 and Figure 4.13, it can be shown that at 1MHz clock frequency, UEDAC1 has about 70 dB SNR which corresponds to 4ns clock jitter (RMS value). The possible cause of this relatively large value can be attributed to the delay caused

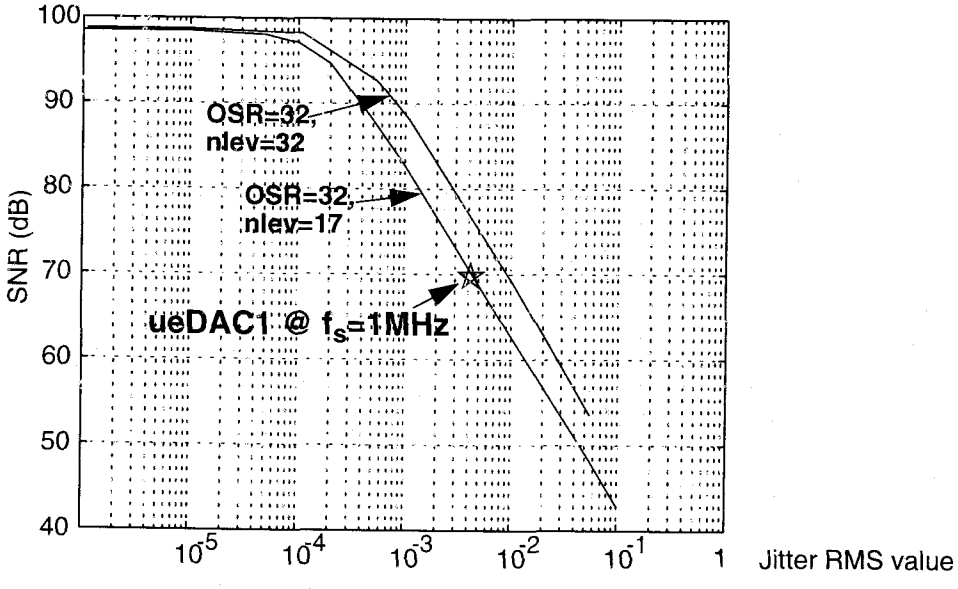


Figure 4.12: SNR vs. Clock jitter for the modulator under test (f_o=f_s/128).

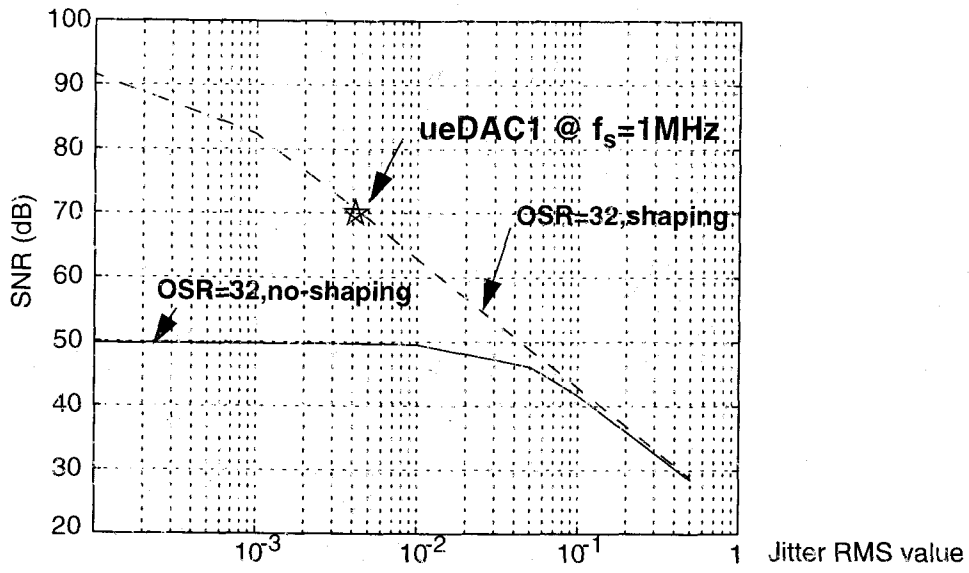


Figure 4.13: SNR vs. clock jitter with 1% mismatch error (f_o=f_s/128).

by Xilinx logic, since no on-chip latches are used before the digital signals reach the clock driver.

The assumption that the jitter is 'white' cannot explain the fact that HD_2 is proportional to the clock frequency. An explanation could be that the jitter is correlated with the input signal, which is quite possible since the clock signals can be 'smeared' by the digital output bit-stream from the modulator as they all come from the same Xilinx board. Each bit-stream contains a signal component and may interact with the clock generator and buffer through power supply bounce, thus making the clock jitter dependent on the signal and leading to harmonic distortion.

The above argument has been verified by simulation. A model which incorporates the correlation of clock jitter with input signal is shown in Figure 4.14. Assuming the clock jitter is correlated with input digital signal stream (multiplied by P, the correlation coefficient in the model of Figure 4.14), the output of the DAC will contain harmonic distortion, as shown in Figure 4.15. In this plot, the second-order harmonic (HD_2) versus

clock jitter correlation coefficient P is shown. When mismatch-shaping is employed, the HD_2 generated by clock jitter is dominant and exhibits a 20 dB/decade slope, while the mismatch-introduced HD_2 is dominant in the no-shaping case.

Although we can not determine experimentally if the correlation of clock jitter with input signal is the cause of the frequency dependent HD_2 in the shaping case, the simulation results make an important point: it is critical to use a 'clean' clock signal with

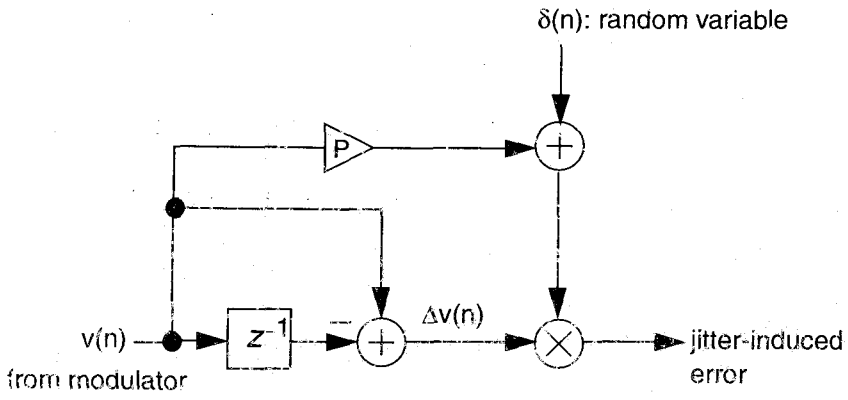


Figure 4.14: Model when clock jitter is correlated with input signal.

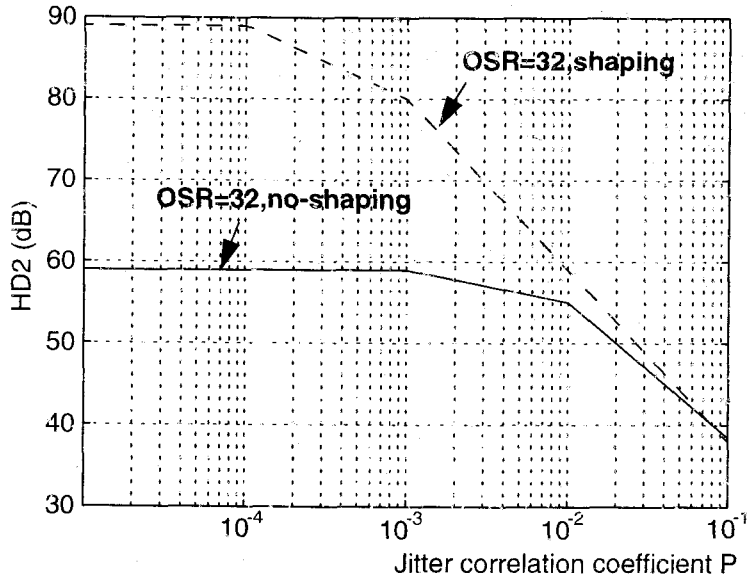


Figure 4.15: HD_2 vs. clock jitter with 1% mismatch error (f_o=f_s/128).

as little jitter as possible, and to separate the clock signal from the input digital line in the layout, etc. These issues will be addressed in the design of the second-generation unit-element DAC (UEDAC2) in Chapter 5.

4.2.4 Interactions

There are two categories of interactions which may cause distortion in the UEDAC: interactions among unit elements and interaction between individual unit elements and the reference voltage. A mechanism for the latter type of interaction can be better understood by referring to Figure 4.16, which is a redrawn version of a unit element current source together with the bias circuit shared among all unit elements. During each switching transition, the voltage at node A has considerable swing due to the source follower operation. This voltage excursion may be coupled through the C_{gd} of M_3 to the gate of transistor M_{2a} (i.e. node B) and influence the biasing node IB. The voltage gain from node B to IB is approximately

$$\frac{V_{IB}}{V_B} \approx \frac{g_{ds1a}}{g_{m1a}}, \tag{4.11}$$

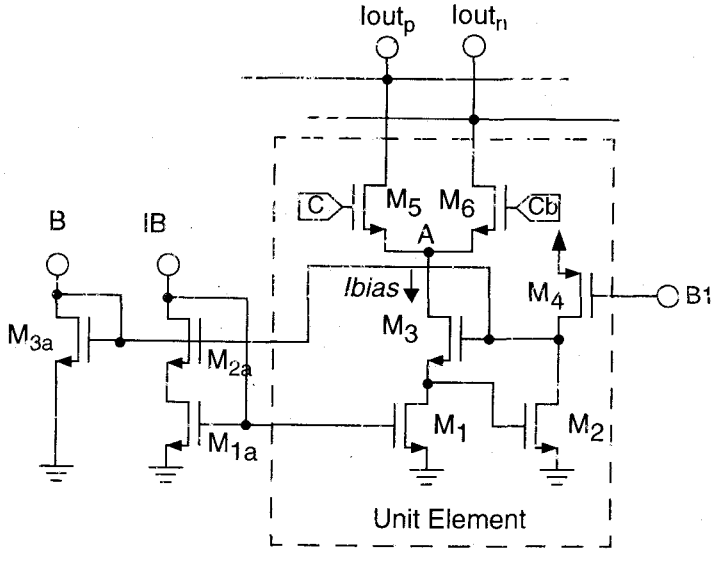


Figure 4.16: Unit element current source and its biasing circuitry.

where g_{m1a} and g_{ds1a} are the transconductance and output conductance of transistor M_{1a}, respectively. The gain calculated from Eq. (4.11) is on the order of 0.01~0.001. Although this is quite a small value, when considering harmonic distortions below -80 dB, it is not a negligible error source.

The second interaction stems from the corruption of the reference current by the input signal. Remember that when mismatch-shaping is applied, each component of the selection vector becomes a delta-sigma sequence encoding the desired sine wave, as shown in Figure 4.17. Thus, 16 high-amplitude digital signals containing spike energy at the output frequency (f_1) all converge on the IC when mismatch-shaping is used. Any coupling between these signals and the reference current will result in an f_1 component on the reference. Since the reference is a multiplicative input to the system, a $2f_1$ component will therefore be created at the output. In order for the amplitude of the resultant HD_2 to be proportional to frequency, the degree of coupling must also be proportional to frequency, suggesting a capacitive coupling to the reference input. To check this possibility, in [57] several checks were made, namely:

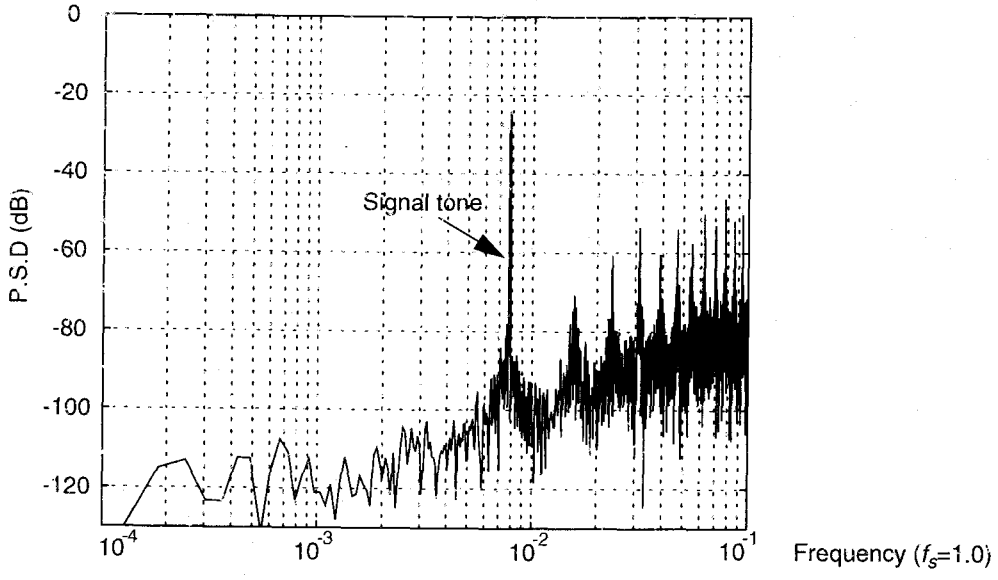


Figure 4.17: Spectrum of each element selection signal.

i) The IB pin was bypassed with a large capacitor:

ii) The amplitude of the f_1 component was measured as a function of frequency and compared against the test results of Figure 4.7.

The conclusion was that although there did exist an f_1 component on the IB pin and it could be eliminated by adding the bypass capacitor, this f_1 component is not responsible for the generation of the frequency dependent HD_2. In other words, the corruption of the reference by the signal is not the limiting factor in the mismatch-shaped configuration.

Nevertheless, the above discussion still brings up several issues which need to be considered in the design of UEDAC2, namely the local current biasing structure and scrambling or coding/decoding of the input selection digital signal. These points will be covered in more detail in Section 4.3.

4.2.5 Mismatched rise/fall delay

In the former sections, several explanations were offered to address the frequency dependence of the harmonic distortion (especially HD_2). One possible answer was signal-dependent clock jitter. As it is not easy to directly measure and quantify the jitter effect in the experiment, other sources of error also need to be considered. Specifically, the settling dynamics of the DAC may contribute to this frequency dependent harmonic distortion, as explained below.

As described in Section 3.4, that the process of converting a discrete-time signal into a continuous-time waveform is a nonlinear operation unless the rise and fall characteristics of the waveform are complementary. In real circuits, however, it is not easy to make this happen. Figure 4.18 shows an HSPICE simulation of the step response of the

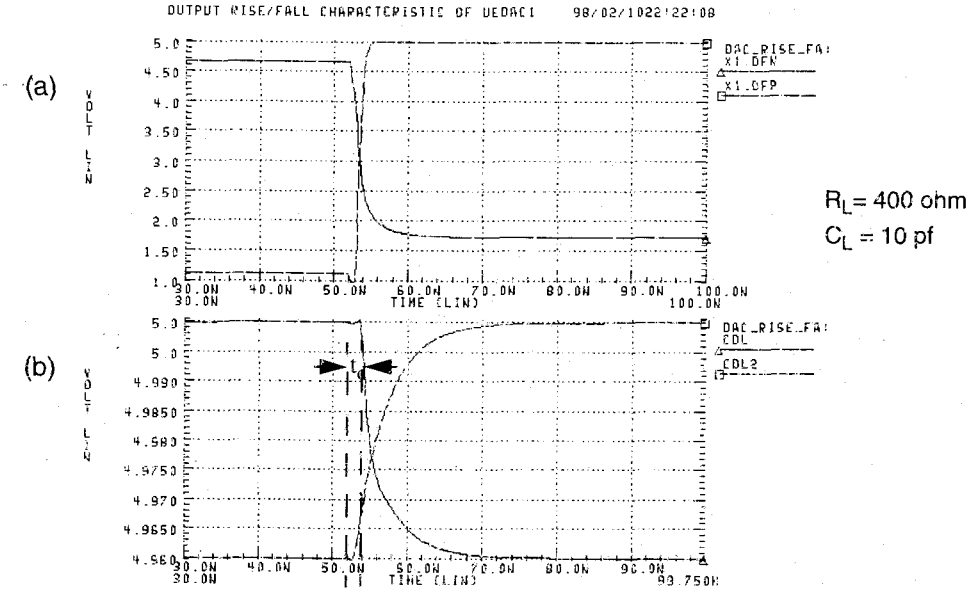


Figure 4.18: HSPICE simulation for the UEDAC1 switching characteristics: (a) differential clock driver; (b) output step response.

clock driver and the resulting output voltage. Although in principle the output characteristic shown in Figure 4.18(b) could be directly measured, the large load capacitance disguises the exact dynamic settling process [57]. Meanwhile, the package and bond wire inductance also cause ringing which makes the observation even more difficult. Therefore, we resort to HSPICE simulation for a detailed analysis and then verify the conclusion through indirect measurement.

Referring to Figure 4.18(b), there exists an inherent delay $t_d \cong 2ns$ between the rise and fall waveforms. At first glance it seems that the non-symmetrical differential clock driving signal shown in Figure 4.18(a) is the cause of trouble, but a careful study of the unit-element's settling process reveals that this rise/fall delay is inherent and unavoidable in this clock driver and unit element structure, even with perfectly symmetrical differential clock driving signals. The reason for this can be explained clearly by referring to Figure 4.19: if the driving clock signals go up and down simultaneously, then the transistor which is already on (M_5) behaves as a source follower and the current flows through it starts

to decrease (which causes the corresponding output voltage to ramp up) as soon as its gate voltage goes down. The voltage at node A will follow the gate voltage of M_5 and goes down. Since M_1 and M_3 constitute a nearly ideal current source, the current *Ibias* flowing through them remains almost unchanged regardless of the voltage excursion at node A. The parasitic capacitor C_p will discharge and compensate for the reduced current of M_5, making the total current *Ibias* unchanged. Therefore, the transistor which was formerly off (M_6) has to wait until the differential driving signals enter the cross-point region before it starts to steer the current. Thus, the rise waveform will always precede the fall waveform and introduce rise/fall mismatch (delay); exact symmetry in the differential driving signal does not help.

With the model presented in Chapter 3, we can calculate the error signal waveform $w_3(t)$, using Eq. (3.29) and the simulated output waveform shown in Figure 4.18(b). The error signal is shown in Figure 4.20(a). As we expect, there contains a huge amount of low frequency energy in $w_3(t)$, which can be seen from its spectrum shown in Figure 4.20(b).

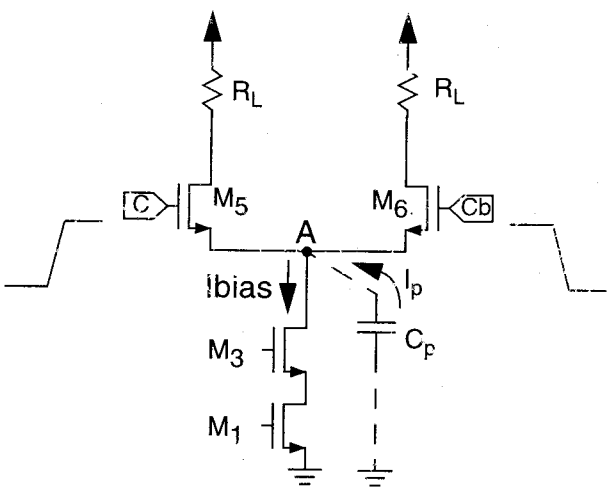


Figure 4.19: Effect of parasitic capacitance on the rise/fall characteristic.

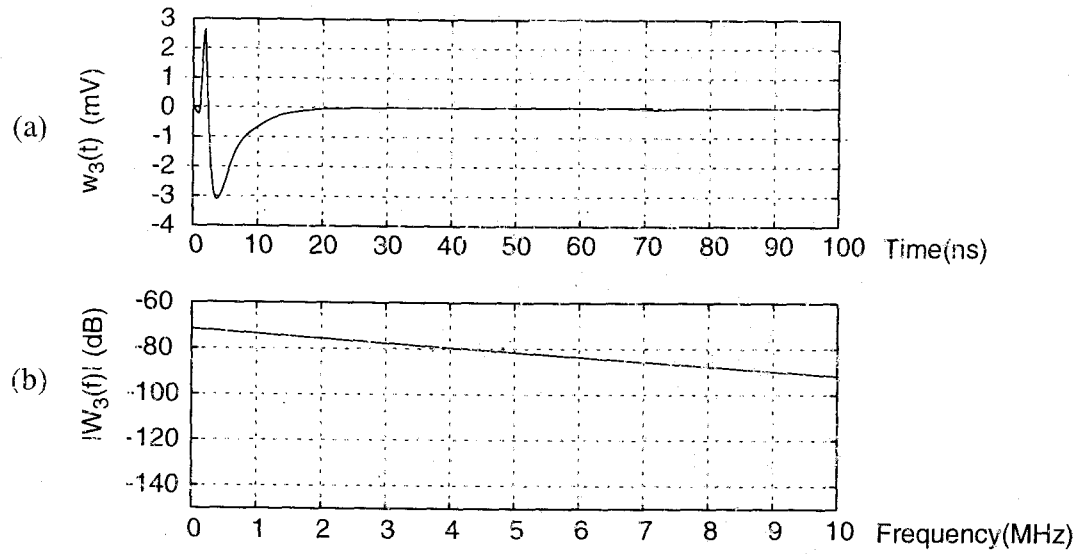


Figure 4.20: Signal $w_3(t)$ calculated from HSPICE simulation: (a) waveform; (b) spectrum.

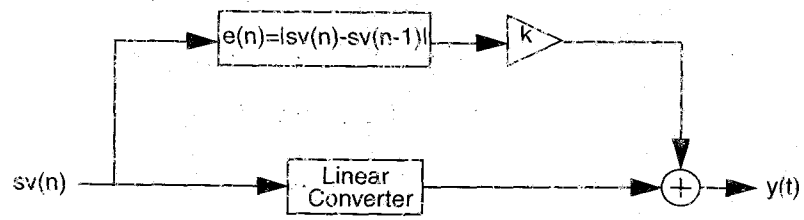


Figure 4.21: A theoretical model for mismatch rise/fall delay t_d.

A simplified model is developed to address this rise/fall mismatch delay and to analyze its effect on the performance of the overall system, as shown in Figure 4.21. In this model, an ideal DAC transforms the discrete-time input sequence $sv(n)$ into a continuous-time output $y(t)$, which contains an error term k from the rise/fall delay time. The error term is only dependent on the absolute value of the change in sv. When sv is unchanged, no error term will be introduced. The coefficient k can be calculated empirically in the following way. First, the in-band error energy is calculated by integration of $|W_3(f)|^2$

$$E_e = \int_0^{f_b} |W_3(f)|^2 df . \tag{4.12}$$

The coefficient k can be obtained simply by

$$k = \sqrt{E_e}, \tag{4.13}$$

where f_b is the width of the band of interest. Using the waveform shown in Figure 4.20(a), we get $k = 0.0012$.

This simplified model can be used in simulation to describe the generation of dynamic errors and compare their effect on various mismatch-shaping techniques. One of the simulation results is shown in Figure 4.22. The dynamic error coefficient k is chosen to be 0.1% from the calculation made in Eq. (4.12) and Eq. (4.13). It can be seen that the mismatched rise/fall delay introduces HD_2 in the shaping condition, whereas it has much less effect in the no-shaping case. The reason for this phenomenon can be best understood with the model: since the dynamic error is caused by the number of elements which switch in each period, and first-order mismatch-shaping switches the elements more frequently than the no-shaping case, the shaping algorithm is more sensitive to dynamic error than the no-shaping case. Furthermore, since the ratio of the dynamic error (i.e. mismatched rise/fall delay) to the sampling period decreases as the sampling rate increases, the harmonic

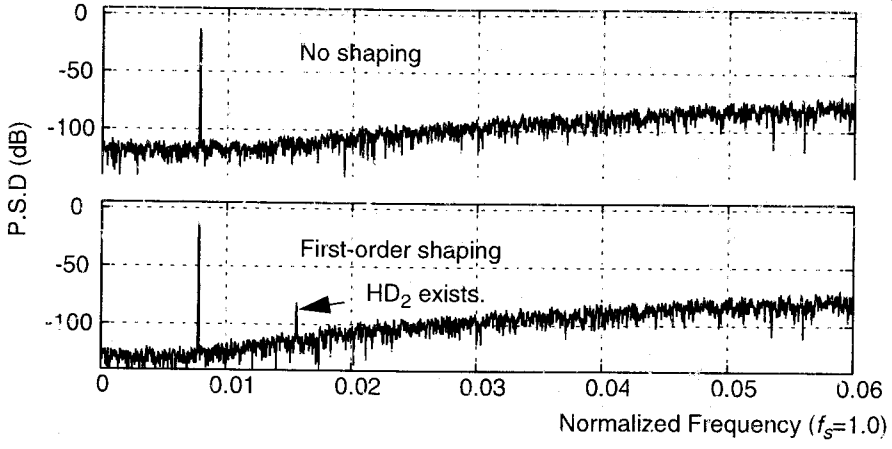


Figure 4.22: MATLAB simulation using the dynamic error model with 0.1% mismatch rise/fall delay (f_o=f_s/128).

distortion (more specifically, HD_2) will also increase proportionally to the sampling frequency. This offers another explanation for the 20 dB/dec slope of HD_2 observed in Figure 4.7.

As can be seen in Figure 4.18(b), the mismatched rise/fall delay is about 2ns. When the sampling frequency is 500 kHz, this delay corresponds to 0.1% dynamic error. From the simulation shown in Figure 4.22, we saw the HD_2 is about 70 dB down from full-scale. This agrees with our measurement result in Figure 4.7, where HD_2 is about -73 dB with a 500 kHz clock frequency. Thus, rise/fall mismatch is the major source of error which causes the frequency dependent harmonic distortion.

4.3 Summary

In this chapter various factors which may affect the performance of UEDAC1 were examined. Generally, there are two types of errors which need to be considered. The first type are errors which do not depend on the clock frequency, such as finite output impedance of the current source and element mismatch. The other type of error is the dynamic error, which includes clock jitter and mismatched on/off delay. Mismatched on/off delay is identified as the most likely source of error which limits the high speed application of UEDAC1. It has been found that the static error caused by element mismatch can be effectively shaped through first-order mismatch-shaping, whereas the dynamic error is more disastrous in high-frequency applications and is worsened by existing mismatch-shaping schemes. Circuit-level improvements and/or system level modifications are needed to overcome these limitations.

Chapter 5. Design of the Second Current-Mode DAC (UEDAC2)

In Chapter 4, the first-generation DAC (UEDAC1) was described, characterized and analyzed. Its linearity was found to be limited at high frequencies by dynamic effects (namely mismatched rise/fall delay). In this chapter, a new current-mode unit element DAC (UEDAC2) is designed. The primary goal of UEDAC2 is to operate at higher frequency with higher SNR and SNDR (signal-to-nose & distortion ratio).

5.1 Block Diagram of UEDAC2

As Figure 5.1 shows, UEDAC2 consists of 16 equal-valued current sources. The digital input signal sv_i (i=1,2,...,16) comes from a delta-sigma modulator and each bit controls a single current source. The current is summed up at the output node and an off-chip resistor load R_L converts the current to an output voltage. The design specifications of UEDAC2 are listed in Table 5.1.

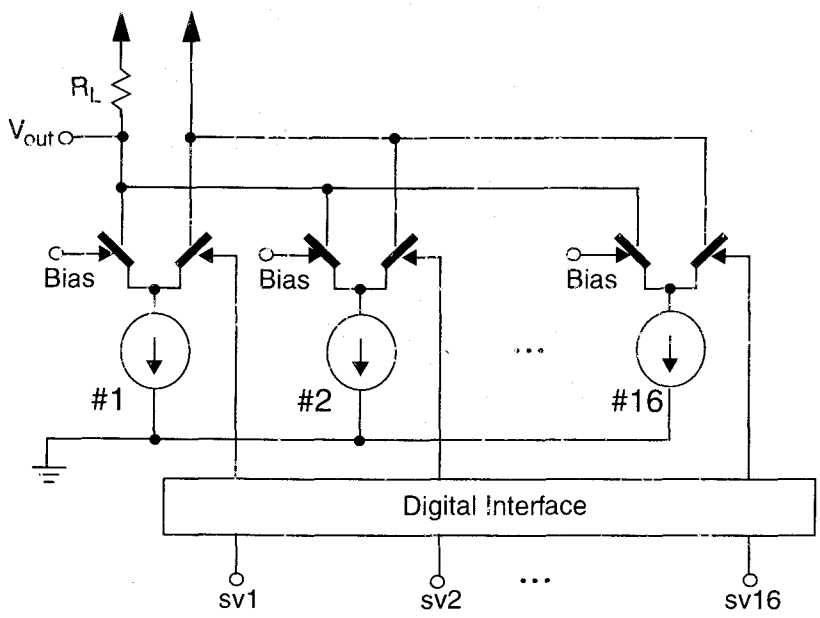


Figure 5.1: Block diagram of UEDAC2.

Table 5.1:Design specifications for UEDAC2

Max. Clock Frequency	10 MHz
DAC Resolution	4-bit
DAC Accuracy	10-bit
Band of Interest	150 kHz
SNDR	>80 dB
Bias Current Per Cell	250 μA
Power Consumption	24 mW
Power Supply	5 V
Chip Package	40 pin

The load resistance and output swing are kept low so that high-frequency operation can be achieved.

5.2 Switch Driver: Single-Ended vs. Differential

The function of the switch driver in a current-mode DAC is twofold: first, to transform the input digital signal into a driving signal which yields fast current steering; second, to provide a driving signal which yields complementary rise/fall dynamics. The second requirement is especially important for the DAC to operate at high sampling rates.

Generally, switch drivers come in two kinds: differential drivers and single-ended drivers. The most commonly used structure is the differential driver, which provides a differential driving signal to make the current-steering process fast. This is a significant advantage of the differential switch driver. However, special care must be taken to design the driving waveforms, otherwise non-complementary rise/fall dynamics may severely limit the DAC's linearity in high speed applications, as we have already observed in Section 4.2.5.

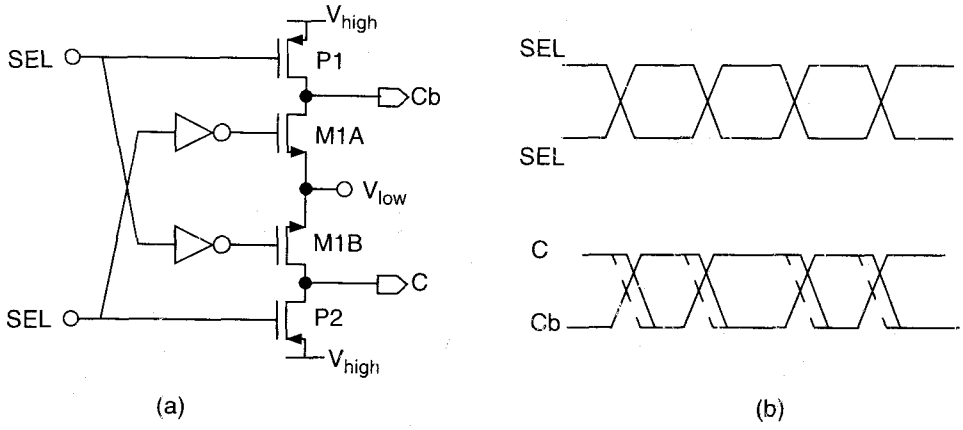


Figure 5.2: Improved clock driver: (a) schematic; (b) waveform.

Figure 5.2 shows an improved design which helps to minimize the rise/fall mismatch. The basic idea is to make the rising driving signal go up before the falling driving signal goes down, thus making the formerly 'off' switch easier to turn on and minimizing the rise/fall delay time t_d. Meanwhile, by making the swing of the differential driving signal small (peak-to-peak 1V), the voltage modulation at the common source node A (see Figure 4.19) can be reduced leading to a lower output glitch current (caused by the charging/discharging of the parasitic capacitance at node A) and faster settling. HSPICE simulation is performed to validate this structure, as shown in Figure 5.3(b). It can be seen

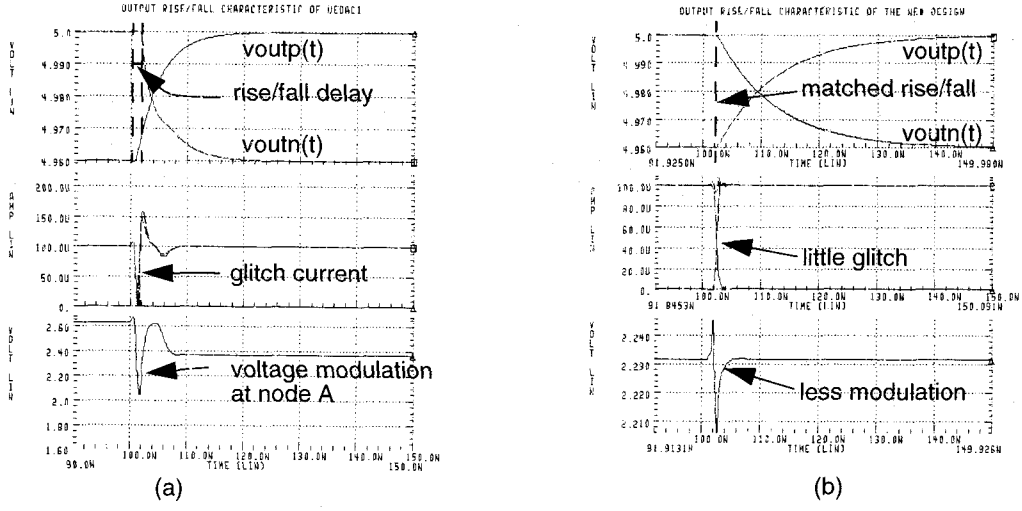


Figure 5.3: HSPICE simulation: (a) UEDAC1 design; (b) improved design.

that the rise/fall delay is almost zero and the voltage swing at node A is greatly reduced, compared with the original design of UEDAC1 shown in Figure 5.3(a).

The single-ended switch driver can also be operated at high speed, if it can be designed properly together with the current source. Compared with the differential structure, the single-ended driver has the following advantages:

i) The single-ended driver does not require an extra switch driver stage and is therefore simpler;

ii) The rise/fall delay of the output waveform can be controlled by adjusting the threshold voltage in the single-ended structure;

iii) There is no clock feedthrough to the output node. Thus, the interaction of elements turning on/off is minimized and so is the high frequency noise;

iv) Clock feedthrough on the driving side can enhance the on/off operation at the other side. Therefore, high speed operation can be achieved.

The above advantages lead to the choice of a single-ended driver structure for UEDAC2. The schematic of the single-ended driver is shown in Figure 5.4, together with the current source and bias circuitry. Its design will be discussed in detail in the next section.

5.3 Unit element design

The schematic of the unit element is shown in Figure 5.4. The differential transistor pair M_1 and M_2 forms the single-ended switch driver. M_3 and M_4 are the current source and cascode transistors, respectively. M_5 to M_{11} constitute the biasing circuitry which determines the current value in each element. Table 5.2 shows the size of the transistors.

Although the matching requirement in UEDAC2 is not critical, good matching is still desired since better matching produces less mismatch noise and distortion in the baseband even when mismatch shaping logic is applied. Current source matching has been well studied. In [60][61], some design issues with respect to current source matching are given with emphasis on transistor threshold voltage V_{th} and area. It is favorable to design the transistor with large overdrive voltage (V_{dsat}=V_{gs}-V_{th}) and large area $W \times L$ for better matching. In our design, we choose V_{dsat}=0.8V and $W \times L = 37.8\,\mu m \times 3.6\mu m$.

As analyzed in Section 4.2.2, on page 60, the output impedance of the current source should be high enough to achieve the desired SNR/SNDR. When no mismatch error exists, a MATLAB simulation shows that at least $30M\Omega$ is required for SNDR > 90 dB, if the load resistance is 300Ω. This leads to the use of a cascode current source. In our design, M_2 is biased in the saturation region and thus M_2, M_3 and M_4 constitute a triple-cascode current source which has an output impedance over $350M\Omega$, thereby eliminating this error source.

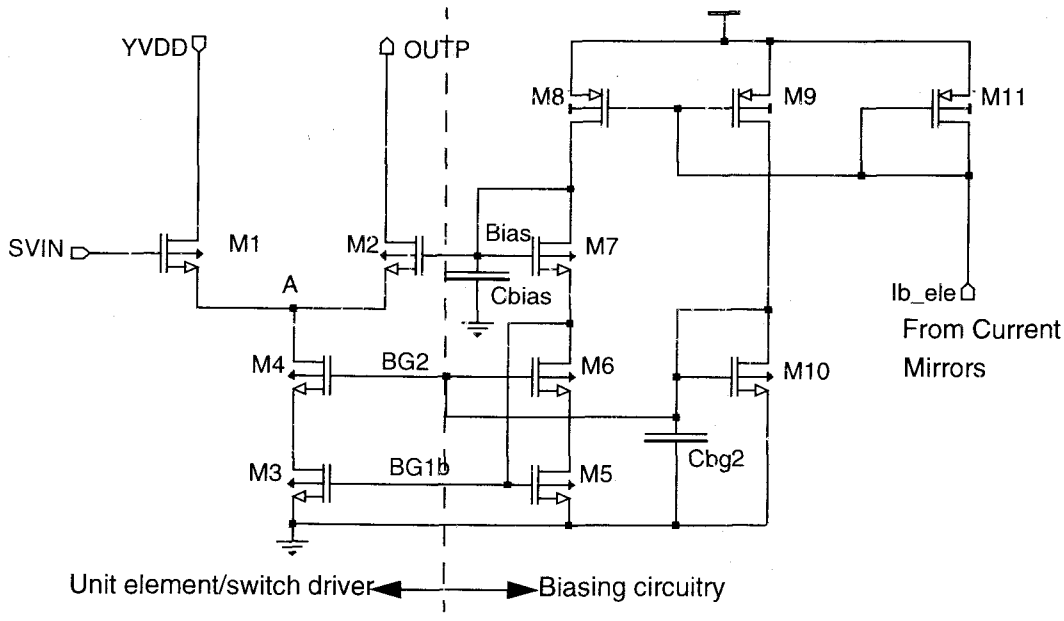


Figure 5.4: Unit element, clock driver and biasing circuitry.

Table 5.2:Transistor dimensions for a unit element.

M_1	33.3/1.8
M_2	33.3/1.8
M_3	37.8/3.6
M_4	42/4.2
M_5	7.2/3.6
M_6	8.4/4.2

M_7	6/1.8
M_8	45/1.8
M_9	45/1.8
M_{10}	4.2/2.4
M_{11}	22.5/1.8

In the design of UEDAC1, each current source is biased using a gate voltage which is common to all elements and which also goes off-chip. This may be a problem since the biasing node is a high impedance node which picks up substrate noise, cross-coupled noise and interference from nearby elements. In the new design, local biasing is used to ensure each element operates independently. Meanwhile, current biasing using current mirrors instead of voltage biasing is used in the design. In this way, less noise can be picked up since the current bias node is a low-impedance node (in the range of $1/g_m$, where g_m is the transconductance of the diode-connected transistor).

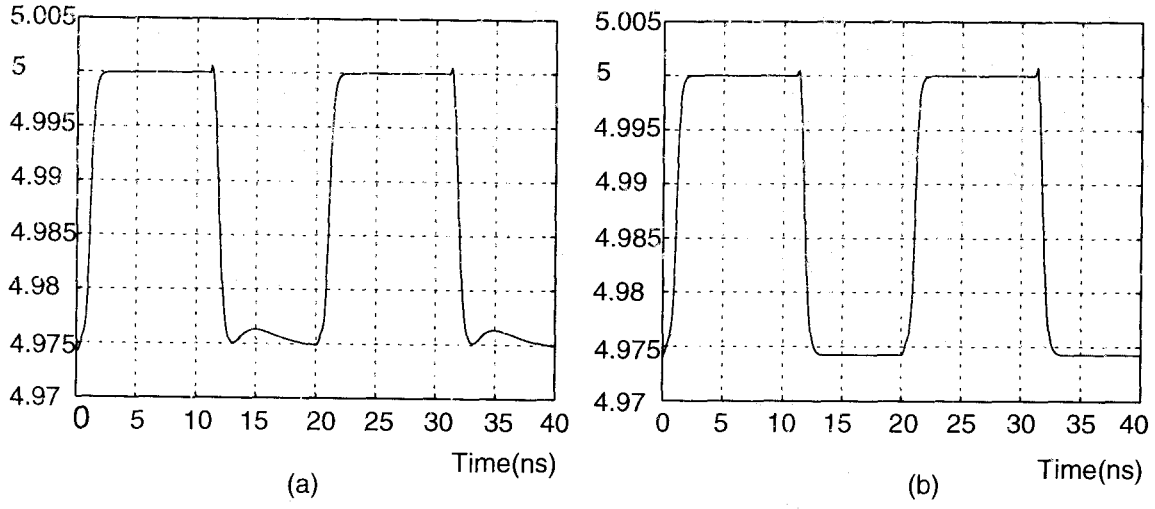


Figure 5.5: Output waveform from simulation: (a) without damping capacitors; (b) with damping capacitors.

Although larger R_L gives larger signal swing, there are several issues which need to be considered. First, R_L cannot be too large when the DAC is operating at high speed, since the time constant $R_L C_L$ limits the settling time at the output node. Second, the ratio R_{out}/R_L has to be big enough to avoid the SNDR limitation. Thus, with a given R_{out}, the value of R_L is limited. Lastly, M_2 has to be in saturation when it is turned on. Therefore, the voltage swing at output node cannot be so large as to cause M_2 to come out of the saturation region. In UEDAC2, we choose R_L between 100Ω and 500Ω.

In Figure 5.4, the capacitor *Cbias* and *Cbg* serve as damping capacitors for the biasing network. As the differential pair M_1 and M_2 operates in large-signal mode, during each switching transient the common node A has approximately a $1V$ excursion. As the charge is fed through C_{dg} and C_{gs} of M_4 and M_2 respectively, the voltage at node *Bias* and *BG2b* will be disturbed. As the voltage gain from node *Bias* to node *BG1* is

$$A_v = \frac{1}{1 + g_{m5}/g_{m7}} \approx 0.5, \tag{5.1}$$

the bias current flowing through M_3 and M_4 is affected which results in long output voltage settling, as shown in Figure 5.5(a). By adding damping capacitors *Cbias* and *Cbg*, *Bias* and *BG2b* becomes dominant poles and the voltage variation at these nodes is suppressed, resulting in faster settling at the output node, as shown in Figure 5.5(b).

The thermal noise of each current source should be kept low so that it does not become a dominant noise source at the output of UEDAC2. Based upon the schematic shown in Figure 5.4, we can see that M_3 contributes most of the noise power to the output node:

$$\overline{v_n^2} = \overline{i_n^2} \cdot R_L^2 \cdot f_B, \text{ and} \tag{5.2}$$

$$\overline{i_n^2} = \overline{i_3^2} + (\overline{i_8^2} + \overline{i_9^2})25 + \overline{i_{11}^2} \cdot 100, \tag{5.3}$$

assuming the output impedance of current source $r_{out} \gg R_L$, R_L is the load resistance and equals to 300Ω and f_B is the band of interest. At worst case, 16 current sources all on and the total output noise can be estimated as

$$\overline{v_{tot}^2} = \overline{i_n^2} \cdot R_L^2 \cdot f_b \cdot 16 = 3.48 \times 10^{-10} V^2. \tag{5.4}$$

if f_B = 20kHz is taken. Thus, the thermal noise contribution (about -97 dB) is comparable when compared with the quantization noise (around -100 dB).

5.4 Improved Digital Interface

The digital interface latches the 16-bit input *sv* vector to drive the unit elements. The block diagram of the digital interface is shown in Figure 5.6. It consists of two parts: a clock driver and a D-flip-flop (DFF). As discussed in Section 4.2.4, it is important to decorrelate the input *sv* vector using some randomly generated signal (an encode/decode process) to avoid signal-dependent clock jitter and harmonic distortion. The encoding logic is on the Xilinx board. It consists of a pseudo random generator [62] which produces a random signal SD. The schematic of the generator is shown in Figure 5.7. The number of D-flip-flops in Figure 5.7 is set to be $m = 17$ and the tap node is at $n = 14$. Thus, the cycle length for the pseudo random bit stream (PRBS) is 131071, which is long enough to effectively whiten the spectrum of the input *sv* vector. The decoding logic is fairly simple — only EXOR gates, as shown in Figure 5.6(a).

The DFF utilizes true single phase logic (TSPL) instead of the commonly used static logic. The reason for choosing TSPL logic is that [63]:

i) It requires only 1 clock phase and this simplifies the clock generation circuitry.

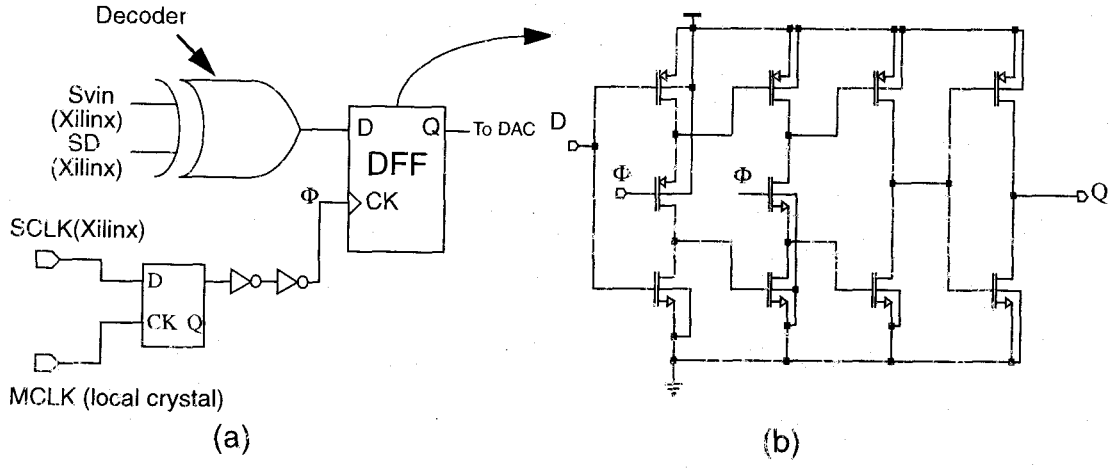


Figure 5.6: Digital interface: (a) decoder and clock generator; (b) TSPL DFF.

ii) The fan-in is low and presents less load to the clock driver.

iii) The clock-to-Q delay is low, minimizing the opportunity for clock jitter to be introduced.

The DFF is shown in Figure 5.6(b). When the clock is low, the first stage precharges. When the clock goes high, the second stage evaluates and passes the signal to the driver stage. As we can see, the load for the clock signal is quite low (only two gate capacitors) and this presents a significant advantage for the clock generating circuitry, since the generation of clock jitter depends heavily upon the delay through the clock generation circuitry.

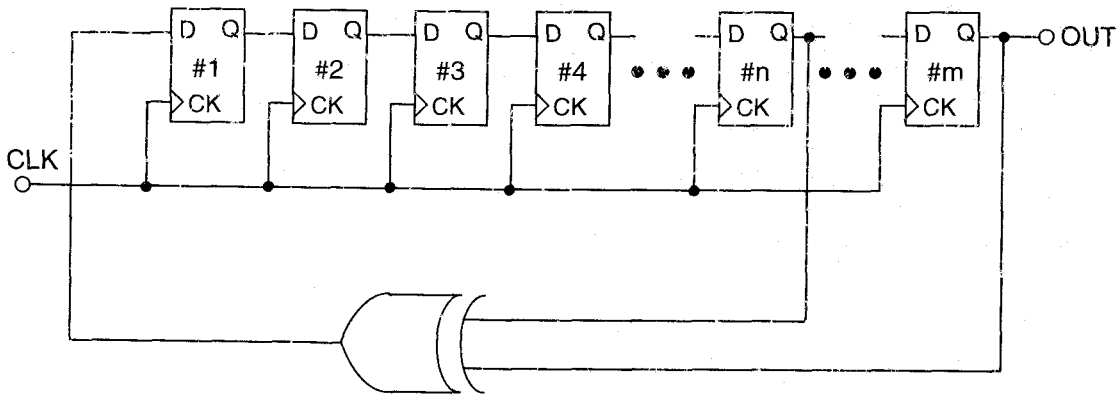


Figure 5.7: Pseudo random bit stream generator.

Clock jitter manifests itself as jitter on the output signal. To minimize the jitter on the output, a crystal-generated 'master' clock (*MCLK* in Figure 5.6) is used to re-time the clock signal from Xilinx board (*SCLK* in Figure 5.6). The delay time through the clock generating circuitry τ_d should be minimized since the power supply and ground bounce may change it and thereby cause clock jitter. In our design, τ_d = 3ns when $VDD = 5V$. A 10% VDD variation causes $\Delta\tau_d$ = 0.12ns. This corresponds to a 0.04% rms clock jitter at a sampling frequency of 10MHz. Comparing with Figure 4.12, we see that 89dB SNR can still be achieved.

5.5 Opamp and Test Cell

For the purpose of comparison between two different biasing schemes, an opamp-biased element has been included as a test cell, which is shown in Figure 5.8. The architecture shown in Figure 5.8 is similar to the one described in [64], but here an NMOS differential pair is used to enhance the switching speed. This cell takes *sv*16 as its digital input signal and produces the output voltage *OUT_TE*. A control signal *CTRL* determines two bias modes for this cell: when *CTRL* is high, the current flowing through this cell is determined by an opamp-controlled network; when *CTRL* is low, the current of this cell is mirrored as in the other unit elements. The transistor dimensions of the test cell is shown in Table 4.3.

The advantage of using opamp-controlled biasing is that it is possible to precisely control the current of the current source. Referring to Figure 5.8, the negative feedback action causes the voltage at node *INP* to be equal to V_{ref}, thus:

$$I_{ref} = \frac{VDD - V_{ref}}{R_{ref}}. \tag{5.5}$$

Since R_{ref} and V_{ref} can be adjusted off-chip, this gives a very convenient way to set the cur-

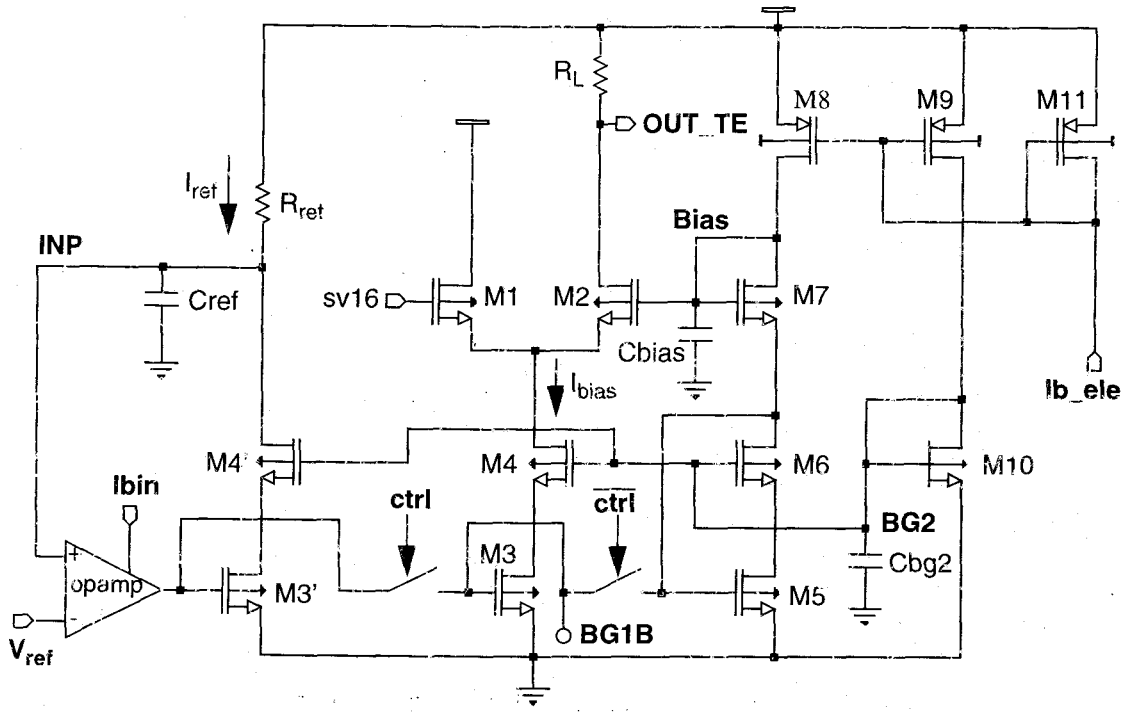


Figure 5.8: Test cell with opamp-controlled biasing circuitry. Only nodes labeled in bold font can be directly measured outside of the chip.

Table 4.3: Transistor dimension of the test cell.

M_1	33.3/1.8
M_2	33.3/1.8
M_3	37.8/3.6
M_4	42/4.2
M_5	7.2/3.6
M_6	8.4/4.2
M_4'	42/4.2

M_7	6/1.8
M_8	45/1.8
M_9	45/1.8
M_{10}	4.2/2.4
M_{11}	22.5/1.8
M_3'	37.8/3.6

rent of a current source to the desired value. In fact, this biasing structure allows the DAC to be used as an MDAC (multiplying DAC).

The accuracy of Eq. (5.5) depends on the DC gain and DC offset of the opamp. The bandwidth of the opamp plays a role when an AC signal is applied to V_{ref} and loop stability

needs to be guaranteed. A two-stage opamp with RC tracking compensation is designed; the schematic is shown in Figure 5.9. M_1~M_4, M_5 and M_8 forms the first stage, M_6 and M_7 constitutes the second stage. M_9 and C_c are used to realize left half plan (LHP) zero which

Table 4.4:Transistor dimensions of the opamp.

M_1	6/1.8	M_{11}	3/1.8
M_2	6/1.8	M_{12}	15.6/1.8
M_3	12/1.8	M_{13}	9.6/2.4
M_4	12/1.8	M_{14}	7.8/1.8
M_5	9.6/2.4	M_{15}	7.8/1.8
M_6	48/1.8	M_{16}	2.4/2.4
M_7	15.6/1.8	M_{17}	6/1.8
M_8	7.8/1.8	M_{18}	24/1.8
M_9	6/1.8	M_{19}	6/1.8
M_{10}	48/1.8	M_{20}	24/1.8

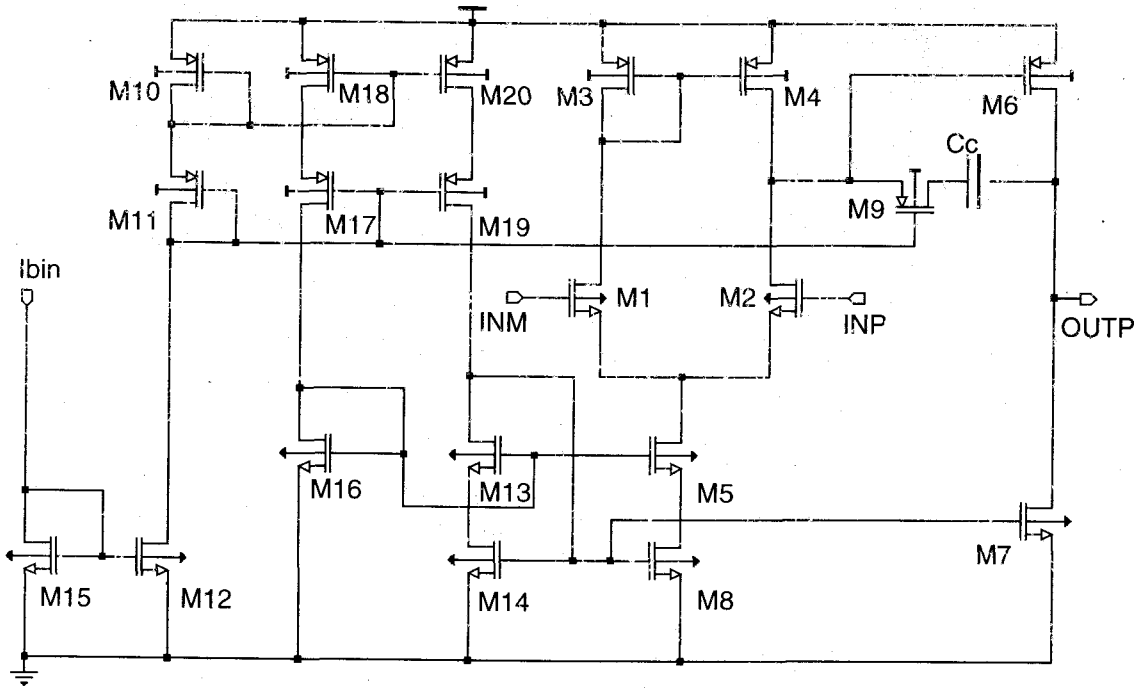


Figure 5.9: Two stage opamp with RC tracking compensation.

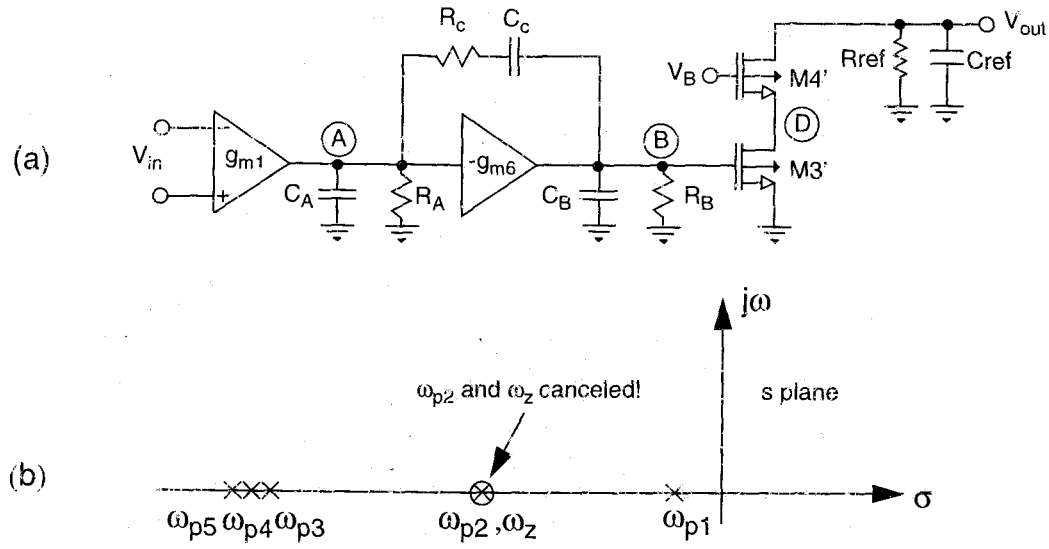


Figure 5.10:Simplified model for opamp-controlled loop: (a) schematic; (b) pole/zero location.

cancels the corresponding pole caused by pole-splitting action. M_{10}~M_{12} are used to bias the gate voltage of M_9 in such a way that the on-resistance of M_9 is insensitive to temperature and manufacturing variations (so-called 'tracking compensation' [65]). Since the opamp is used in a non-inverting configuration, a low voltage cascode current mirror (M_5, M_8, M_{13} and M_{14}) is used to increase the CMRR (common mode rejection ratio) of the opamp without reducing the common-mode input signal range significantly. HSPICE simulation shows 95 dB CMRR (assuming a perfectly matched input pair) can be achieved. The transistor sizes are listed in Table 4.4.

Since the opamp is used in a configuration where extra poles exist in the feedback branch (i.e. cascode amplifier stage with M_3', M_4', R_{ref} and C_{ref}), special care must be taken to optimize the overall feedback system. A model to analyze the overall system is shown in Figure 5.10(a), with the corresponding pole/zero location shown in Figure 5.10(b). In Figure 5.10(a), R_A, R_B and C_A, C_B represent the total resistance and capacitance at node A and B, respectively. Including the cascode amplifier stage, the overall opamp-controlled

system contains three stages: the two-stage opamp forms the first and second stage, while the cascode amplifier becomes the third stage. The dominant pole (ω_{p1}) is caused by the pole-splitting action of C_c:

$$\omega_{p1} = \frac{g_A g_B}{g_{m6} C_c} \tag{5.6}$$

while the second dominant pole $\omega_{p2} = 1/(R_{ref} C_{ref})$ is caused by the output node of cascode amplifier due to its heavy capacitance load. The LHP zero ω_z is caused by the RC compensation and is equal to:

$$\omega_z = \frac{1}{C_c(R_c - 1/g_{m6})} \tag{5.7}$$

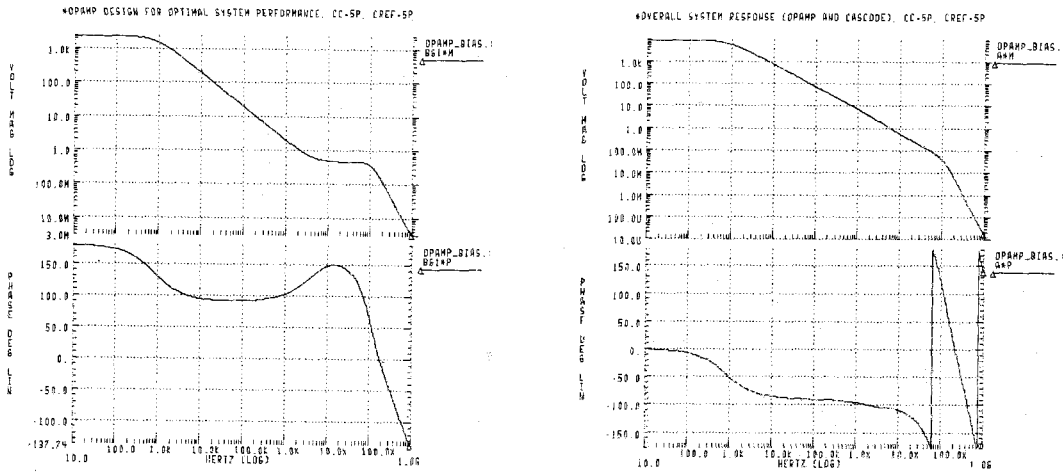
ω_{p3}, ω_{p4} and ω_{p5} are poles at much higher frequencies:

$$\omega_{p3} = \frac{g_B}{C_B + C_A} \cdot \frac{g_{m6}}{g_B} \tag{5.8}$$

$$\omega_{p4} = \frac{1}{C_A \cdot R_c} \tag{5.9}$$

$$\omega_{p5} = \frac{g_{m4}}{C_D} \tag{5.10}$$

In contrast to standard opamp design, where the LHP zero is used to cancel ω_{p3} (which is the pole after pole splitting by C_c), ω_z is used to cancel ω_{p2} instead. Although this leads to non-optimal compensation of the opamp itself, the stability and bandwidth of the overall system can be optimized and improved. Figure 5.11 shows the simulated frequency response of the opamp and the overall system, assuming C_{ref}=5pF. C_c is chosen to be 5pF as well. It can be seen from Figure 5.11(b) that an acceptable system frequency response is achieved. This is the major reason why a two-stage opamp instead of a folded-cascode opamp structure is adopted in this specific application.



(a) (b)

Figure 5.11:HSPICE simulation results: (a) opamp; (b) opamp and cascode amplifier.

The closed-loop frequency response of the opamp-controlled loop when imperfect pole/zero cancellation occurs (due to incorrect parasitic capacitance *Cref*, for example) can be analyzed in the following way: ignoring the high frequency poles ω_{p3}, ω_{p4} and ω_{p5}, the open-loop transfer function of the entire control system (including opamp and cascode amplifier) can be written as:

$$A(s) = \frac{A_0(1 + s/\omega_z)}{(1 + s/\omega_1)(1 + s/\omega_2)} \tag{5.11}$$

$$A_0 = A_1 \cdot A_2 \tag{5.12}$$

where A_1 is the DC gain of the opamp ($A_1 \approx 1800$) and A_2 is the DC gain of the cascode amplifier ($A_2 \approx 5.0$). The closed-loop response can be written as:

$$A_{CL}(s) = \frac{A(s)}{1 + A(s)}$$

$$= \frac{A_0\omega_1\omega_2(1 + s/\omega_z)}{s^2 + (A_0\omega_1\omega_2 + \omega_z\omega_1 + \omega_z\omega_2)s/\omega_z + (A_0 + 1)\omega_1\omega_2} \tag{5.13}$$

Eq. (5.13) can be formulated into a standard second-order system:

$$A_{CL}(s) = \frac{A_0\omega_1\omega_2(1 + s/\omega_z)}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} \tag{5.14}$$

where Q is the quality factor and ω_o is the resonant frequency:

$$Q = \frac{\sqrt{(A_0 + 1)\omega_1\omega_2}}{A_0 \cdot \omega_1\omega_2/\omega_z + \omega_1 + \omega_2} \tag{5.15}$$

$$\omega_o = \sqrt{A_0\omega_1\omega_2} \tag{5.16}$$

Thus, it can be seen from Eq. (5.14) that imperfect cancellation of pole/zero leads to phase lead and complex poles, a fact which will be confirmed later in Section 6.2, opamp test.

5.6 Summary

The second version of current-mode unit element DAC (UEDAC2) is described. A single-ended switch driver is adopted to allow fast switching and to facilitate threshold voltage adjustment, while cascode transistors are used to improve output impedance. Special considerations are given in the digital interface design, aiming at reducing interference and clock jitter. An opamp-controlled bias cell is also included in UEDAC2 for comparison purposes. The chip is fabricated in the Orbit 1.2 μm CMOS N-well, double poly process and occupies $2000um \times 2000um$. A floor plan of the chip is shown in Figure 5.12

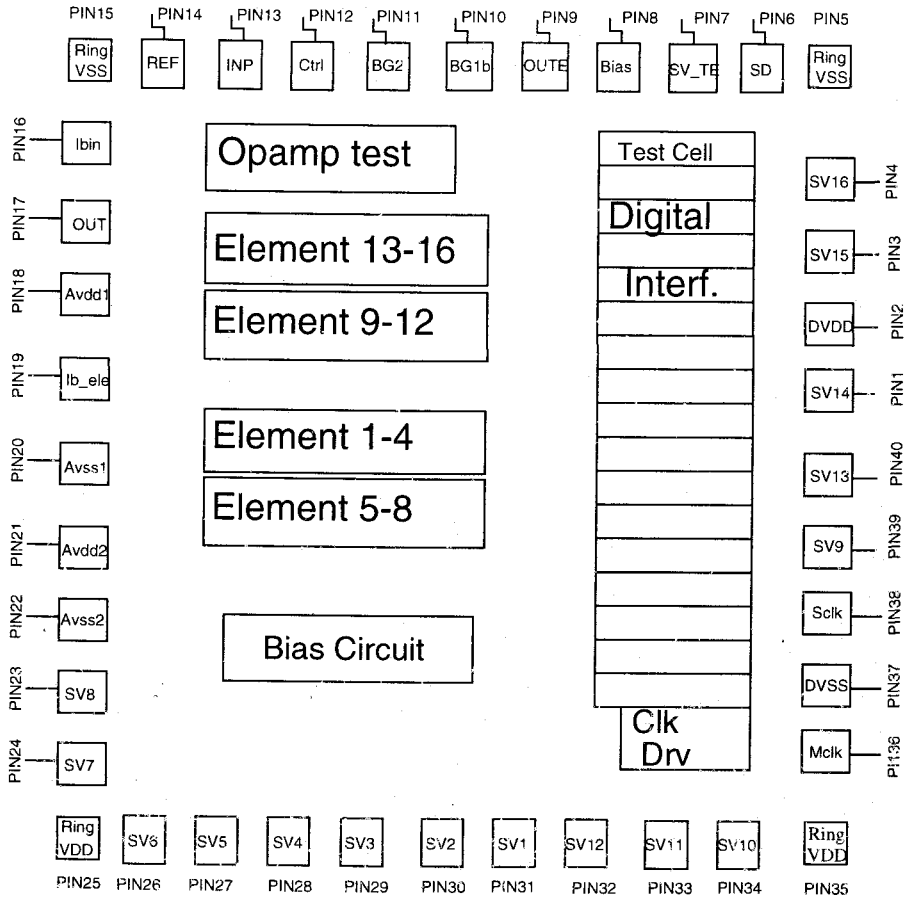


Figure 5.12:UEDAC2 floor plan.

Chapter 6. Test of UEDAC2

In this chapter, UEDAC2 is tested following the methodology of UEDAC1 and using the same test setup. First, DC testing is performed to measure the matching of the current sources and their output impedance. Then, the opamp is tested with its controlled current cell; both DC and AC performance are evaluated. Dynamic testing is then performed and all of the proposed mismatch shaping algorithms (lowpass, bandpass and modified mismatch shaping) are experimentally verified. Finally, an improved test setup makes measurement of the delta-sigma DAC's SNR possible.

6.1 UEDAC2 DC Test

Figure 6.1 shows the measured element values for one UEDAC2 chip, normalized to a nominal value of 250 μA. The standard deviation is 1.22%, which is twice that of UEDAC1. Furthermore, the distribution of the element mismatch looks random, instead of exhibiting the even symmetry seen in UEDAC1. To account for the above observations,

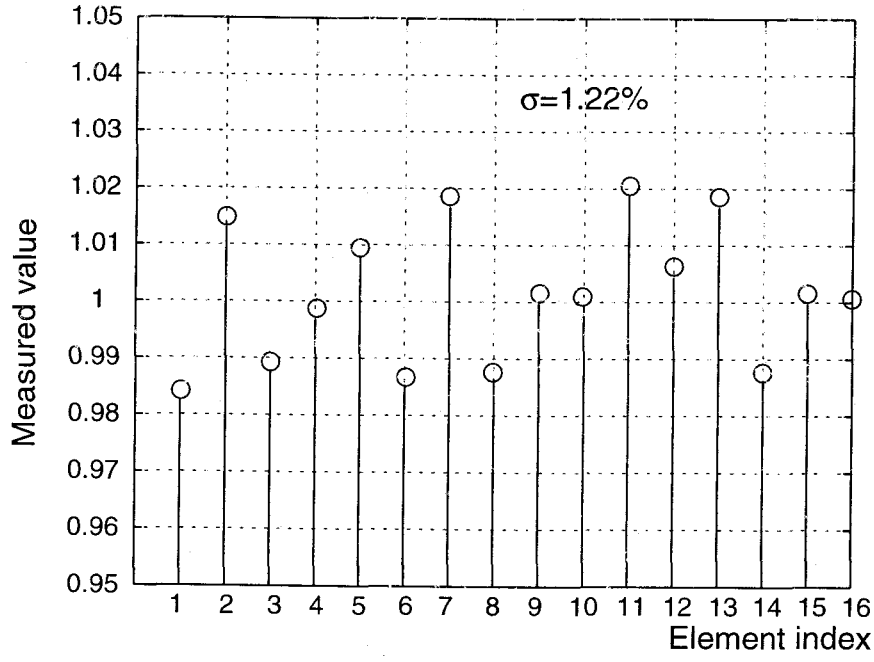


Figure 6.1: Measured UEDAC2 current source values (normalized to 250 μA).

remember that UEDAC2 utilizes current-mirror biasing, i.e. each element is independently biased. The bias current in the main biasing circuitry (which consists of 16 current mirrors) is mirrored four times before it is replicated in the unit element current source. The mismatch between all these current mirrors (threshold, geometry, process variation, etc.) disguises any systematic distribution which might have otherwise been present. Although the matching of UEDAC2 is worse than UEDAC1, our main concern throughout the design of UEDAC2 was to minimize interactions and dynamic errors. Thanks to the benefits of mismatch-shaping, the larger static errors should not be a performance-limiting factor.

The output impedance of UEDAC2 is measured with the help of a high precision volt/current meter, the Keithley Model 619 Electrometer/Multimeter [66]. This instrument has an input impedance of over 20TΩ and has a resolution of 5.5 digits. Thus, it can be used to accurately measure the output impedance of the current source in UEDAC2, which was not possible with UEDAC1 using an ordinary voltmeter.

The set-up for output impedance measurement is shown in Figure 6.2. By applying an adjustable voltage source V_t, we can measure the corresponding current change I. An

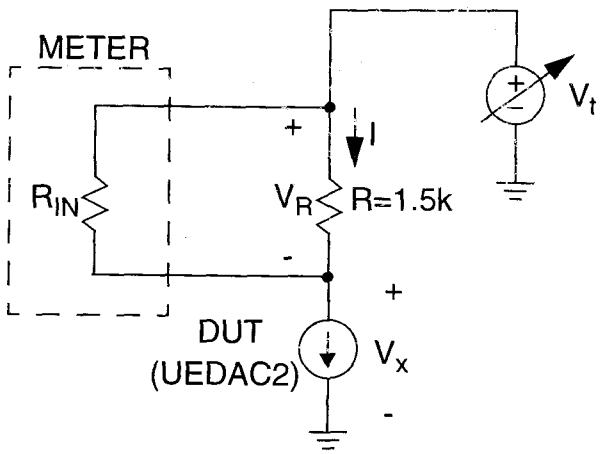


Figure 6.2: Test set-up for measurement of output impedance of UEDAC2.

off-chip resistor R is used to monitor the current-source's current. The output impedance r_{out} of the current source is

$$r_{out} = \frac{\Delta V_x}{\Delta V_R} R, \tag{6.1}$$

where ΔV_x and $\Delta V_R = R \cdot \Delta I$ are the voltage variation across the current source and the resistor R, respectively. Eq. (6.1) can be further simplified to

$$r_{out} = \frac{\Delta V_t}{\Delta V_R} R, \tag{6.2}$$

where ΔV_t is the voltage change of voltage source V_t. The relative error introduced by the simplification of Eq. (6.2) is

$$\varepsilon = \frac{R}{r_{out}} < 10^{-5}, \tag{6.3}$$

which is negligible in our measurement. The loading effect of the voltmeter in this test set-up can be safely ignored, since the input impedance of the meter is over $20T\Omega$.

Due to the triple cascode structure, the measured output impedance of UEDAC2 is very high, about $300M\Omega$. This value is sufficiently large that any effect caused by finite output impedance will be negligible.

6.2 Opamp Test

First, the DC gain of the opamp is measured. Since the opamp and the cascode amplifier are connected inside the chip, the only measurable nodes are V_{ref} and *INP*. Meanwhile, only the closed-loop gain (A_{cl}) can be measured; the open-loop gain (A_o) has to be calculated from the closed-loop gain result. Figure 6.3 shows the model for calculation. Assuming no offset, the output voltage V_{out} can be expressed as

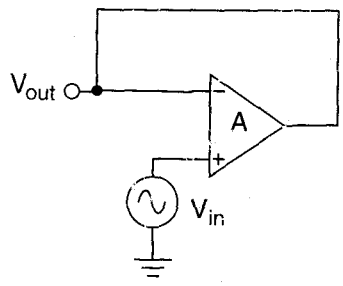


Figure 6.3: Opamp close-loop measurement model.

$$V_{out} = \frac{A_o}{A_o + 1} V_{in} . \tag{6.4}$$

Whereas the DC offset V_{off} can be measured by subtracting V_{in} with V_{out}

$$V_{off} = V_{in} - V_{out} . \tag{6.5}$$

A_o can be measured by

$$A_o = \frac{\Delta V_{out}}{\Delta V_{in} - \Delta V_{out}} \tag{6.6}$$

The measured DC offset using Eq. (6.5) is about 20 mV. This is a relatively large offset, compared with a commercial product (for example, the LF353, a wide bandwidth dual JFET input operational amplifier, has an offset about 6 mV). The reason for this large offset is mainly due to the geometry mismatch, since the size of the input differential pair is quite small in this design (6.0 μm × 1.8μm).

With the help of the high-precision Keithley 619 voltmeter, A_o can be measured through Eq. (6.6). The measured A_o is about 6000, which includes both the DC gain of the opamp and the cascode gain stage. Since the gain of cascode stage is about 4.0 (which can be measured by observing the voltage gain from '*BG1b*' to '*INP*'), the gain of the opamp is about 1500. This deduction is further verified by the AC test shown below.

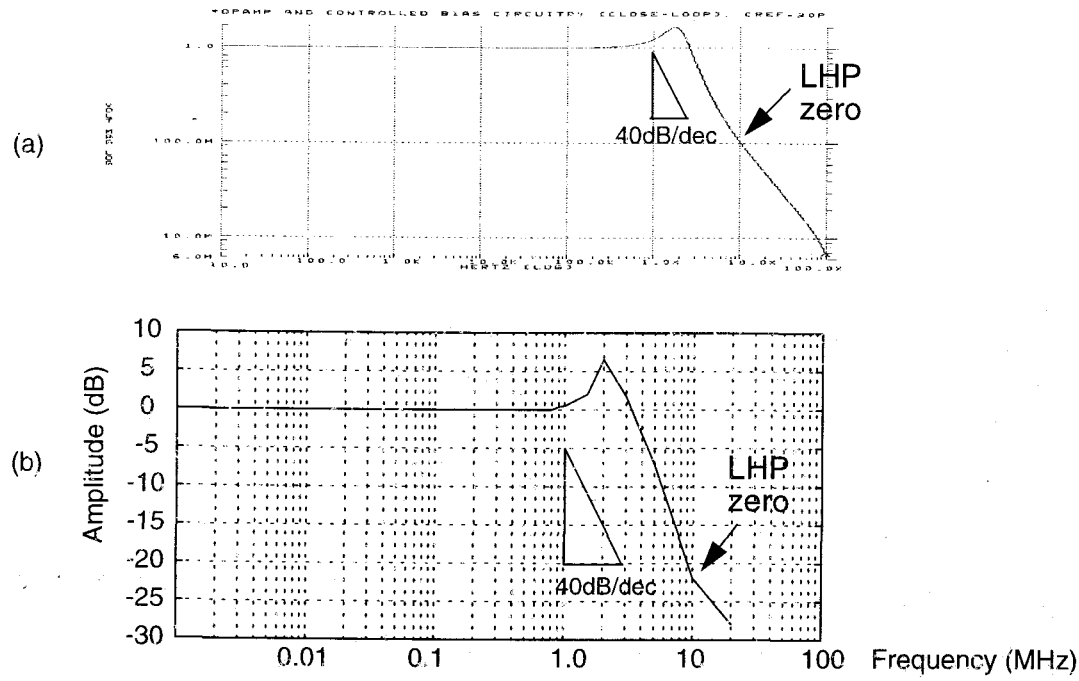


Figure 6.4: Closed-loop frequency response of the opamp-controlled loop: (a) HSPICE simulation result; (b) experimental result. A load capacitance of 30 pF is assumed in the simulation.

The closed-loop frequency response is measured by observing the output voltage while sweeping input signal from DC to 20 MHz. Figure 6.4 shows the simulated (with 30 pF load capacitance) and measured opamp-cascode amplifier closed-loop frequency response. The peak around 2MHz indicates the existence of complex poles. The quality factor Q_p and resonant frequency f_o can be calculate using Eq. (6.7) and Eq. (6.8) [67]:

$$A_p = 20\log\frac{Q_p}{\sqrt{1-1/(4Q_p^2)}} \tag{6.7}$$

$$f_o = \frac{\omega_p}{\sqrt{1-\xi^2}}, \tag{6.8}$$

where A_p is the maximum overshoot in dB, $\xi = 1/(2Q_p)$ is the damping factor. The result is $Q_p = 1.93$ and $f_o = 2.066\,\text{MHz}$. The agreement between the simulated result and the experimental result suggests the opamp meets our design specifications in terms of DC gain and bandwidth. As pointed out in Section 4.3.4, due to the existence of the heavy

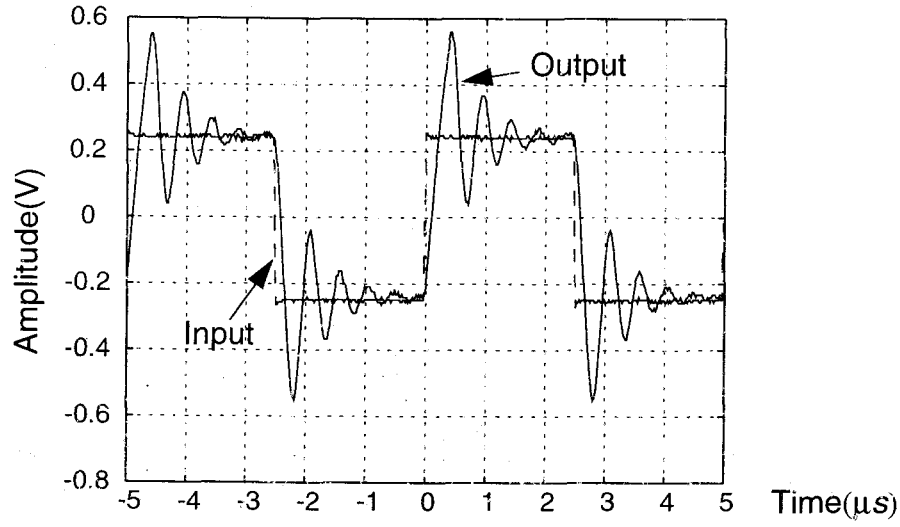


Figure 6.5: Measured step response of the opamp-controlled loop.

capacitive load at the output node (which could not be determined exactly during the design phase), the zero and pole do not cancel each other, leading to peaking in the frequency response.

The step response is also measured for the opamp-cascode amplifier loop. One result is shown in Figure 6.5. There is a relatively large overshoot in the step response (about 50% of the peak value). Using Eq. (6.8) and Eq. (6.9), we can calculate the damping factor ζ and resonant frequency ω_0 [67]:

$$r_p = 1 + e^{-\pi\xi/\sqrt{1-\xi^2}}, \tag{6.9}$$

where r_p is the maximum overshoot. The calculation gives $\xi = 0.23$ and $\omega_o = 2.05\,\text{MHz}$, which agrees with our frequency response measurement quite well. Therefore, it can be concluded that the measured opamp (together with its controlled biasing loop) meets the DC and AC specifications of our design and can be used to adjust the bias current of the test cell.

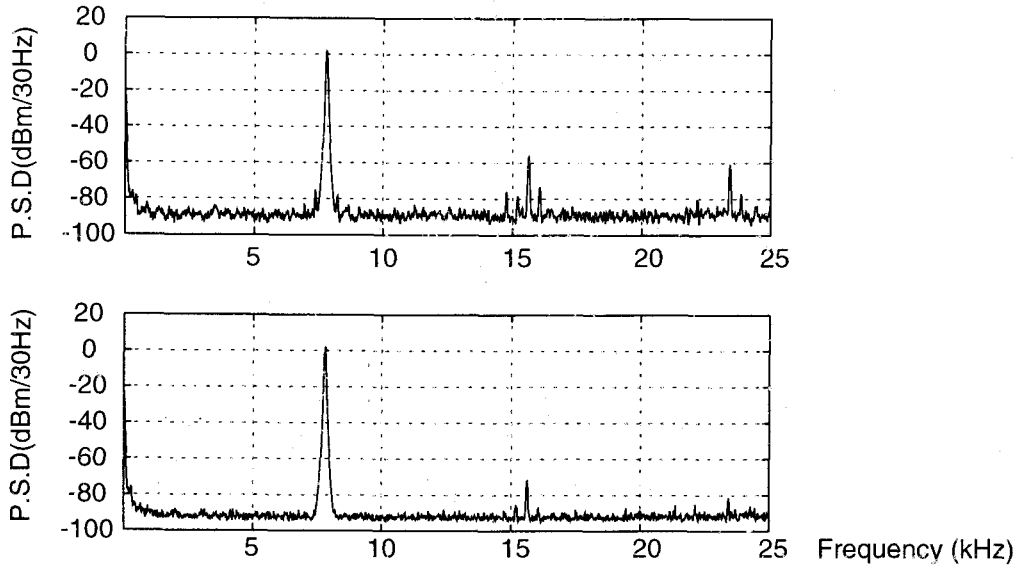


Figure 6.6: Measured spectrum of UEDAC2 at f_s=500kHz: (a) no-shaping; (b) first-order shaping (non-optimal bias).

6.3 UEDAC2 Dynamic Test

6.3.1 Lowpass mismatch shaping

First, the performance of the DAC is measured with lowpass mismatch shaping. Figure 6.6 shows the measurement when the DAC is clocked at f_s = 500KHz. When no shaping is employed, the observed harmonic distortion is HD_2 =-60 dB and HD_3 =-65 dB, respectively. After mismatch shaping is applied, the harmonic distortion decreases significantly, but the second harmonic is still visible.

The measured HD_2 as a function of the sampling frequency is shown in Figure 6.7, where the ideal (simulated), no-shaping and first-order shaping conditions are compared. As we have seen before in the test of UEDAC1, when first-order mismatch shaping is applied, HD_2 is proportional to the clock frequency, eventually exceeding the no-shaping level. This frequency dependence indicates that dynamic effects dominate the static mismatch error when the DAC is operating at high speed.

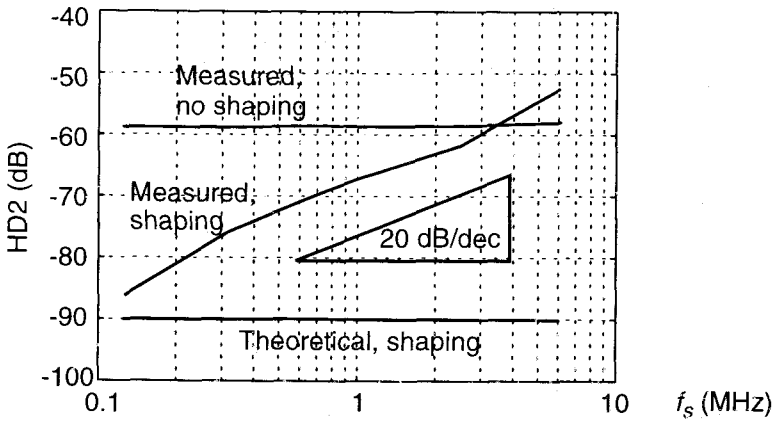


Figure 6.7: Measured HD_2 of UEDAC2 as a function of the sampling frequency (V_{bias} is not optimized).

To verify experimentally that the source of dynamic error is unequal on/off delay, the spectrum analyzer's output can be observed while the threshold voltage of the single-ended clock driver (V_{bias} in Figure 5.4) is adjusted. Figure 6.8 compares the measured spectra at two values of V_{bias}. Referring to Figure 5.4, increasing the bias current value leads to higher V_{bias}, while decreasing the bias current results in lower V_{bias}. Since the bias voltage changes the symmetry of the output waveform, its value has a direct effect on the linearity of the DAC.

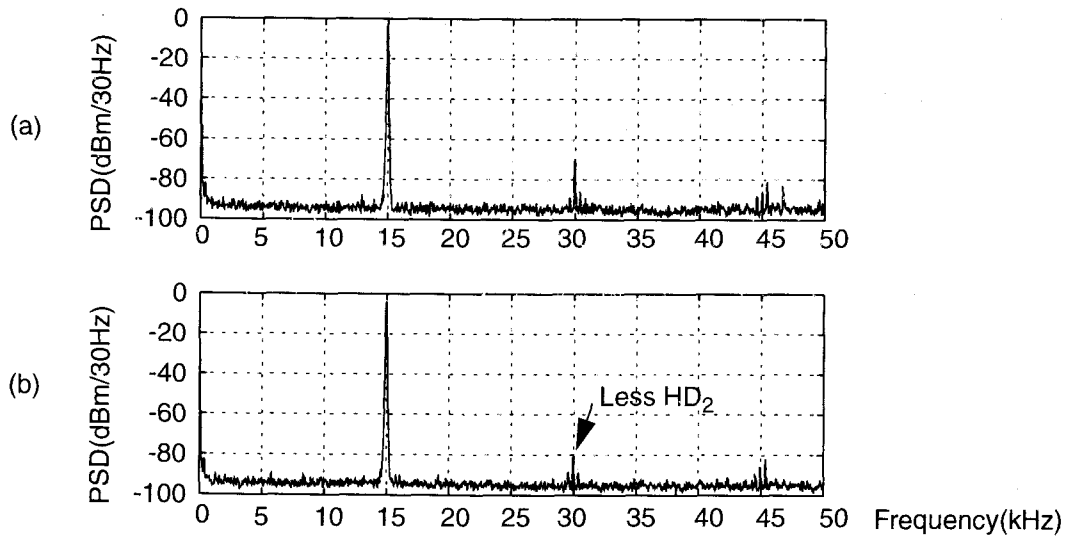


Figure 6.8: Effect of adjusting V_{bias} on HD_2 of UEDAC2 (f_s=2MHz): (a) before adjustment; (b) after adjustment.

A further measurement indicates that there exists an 'optimal' bias voltage V_{bias_opt} for minimum HD_2. Figure 6.9 shows the measured HD_2 versus V_{bias} at f_s=2MHz. It can be seen that V_{bias_opt} is around 3.7 V. At first glance it seems that this result is illogical: if the input digital signal has a 0~5V swing and the power supply for the DAC is also 5V, then V_{bias_opt} should be around the mid-point of the power supply (about 2.5V). An explanation for this apparent contradiction is the following: with the nominal bias current (25 uA), V_{bias} is around 4.07V. Assume the input digital signal has finite rise/fall time (as shown in Figure 6.10), it takes a certain time t_{dr} to turn on M_1(i.e. to steer current from M_2) when D_{in} goes high. When D_{in} goes low, it takes only t_{df} to turn off M_1 and turn on M_2. Since t_{dr} is larger than t_{df}(the exact amount also depends on the edge rates of the input digital signal), a non-symmetrical output voltage waveform results and this asymmetry causes distortion. It thus makes sense to shift the threshold voltage V_{bias} to 2.5V to make the rise/fall delays equal. However, the discharge current I_p from parasitic capacitance C_p will flow through current source I_o, which tends to compensate the current flowing through M_2. This effect delays the output fall waveform. These two effects coexist in the DAC and act conversely

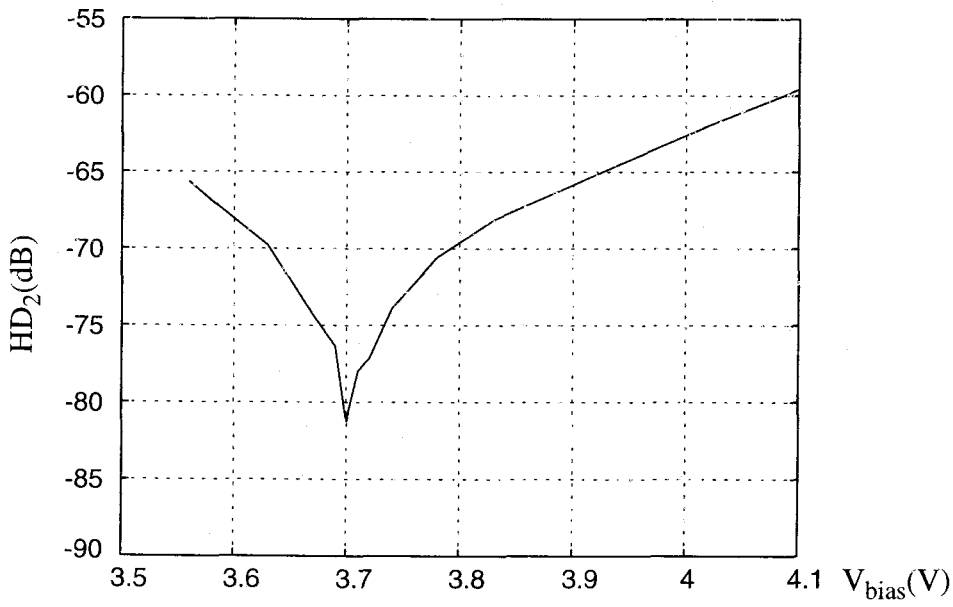


Figure 6.9: Measured HD_2 versus V_{bias} (f_s=2MHz).

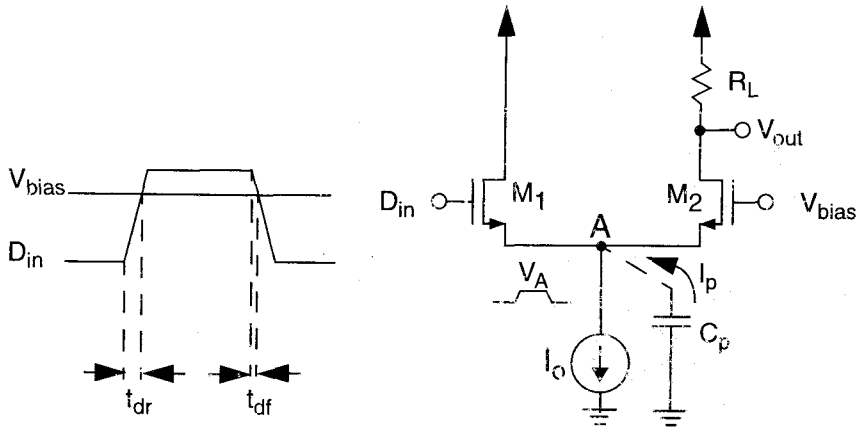


Figure 6.10: Rise/fall characteristic of UEDAC2.

to each other. Thus, V_{bias_opt} can not be chosen to be 2.5V, otherwise the I_p effect will dominate and result in delayed fall time; V_{bias_opt} can not be too high (such as 4.07V), since the threshold voltage delay will become dominate. Therefore, according to HSPICE simulation, for best rise/fall symmetry, V_{bias_opt} should be around 3.70V.

The above analysis has been verified by HSPICE simulation as well. Figure 6.11 shows the output waveform *outp(t)* and *outn(t)* of one element in UEDAC2. It can be seen that higher V_{bias} (4.07V) or lower V_{bias} (2.5V) results in mismatched rise/fall waveforms. Only when V_{bias} is around 3.70V does the output waveform become nearly symmetrical. Figure 6.11(b) also shows the calculated error signal $e_s(t)$ (using Eq. (3.29)) with $V_{xx}(t)$ waveforms imported from HSPICE simulation. Three different bias conditions are compared, together with the spectra of $e_s(t)$ shown in the third row of the same picture. Only under the optimal bias condition does $e_s(t)$ have a 'doublet' waveform which contains little low-frequency energy, which translates into little in-band noise power. By using Eq. (4.12) and Eq. (4.13), we can get the in-band noise power P_e and the error coefficient

k listed in Table 4.5. The sampling clock frequency is 20 MHz. It can be seen that optimal biasing results in more than a hundred- fold reduction in the in-band noise power.

Table 4.5:Calculated in-band noise power and error coefficient

V_{bias}(v)	2.5	4.07	3.7
P_e	$3.0\text{x}10^{-4}$	$2.16\text{x}10^{-4}$	$1.48\text{x}10^{-6}$
k	0.0173	0.0147	0.0012

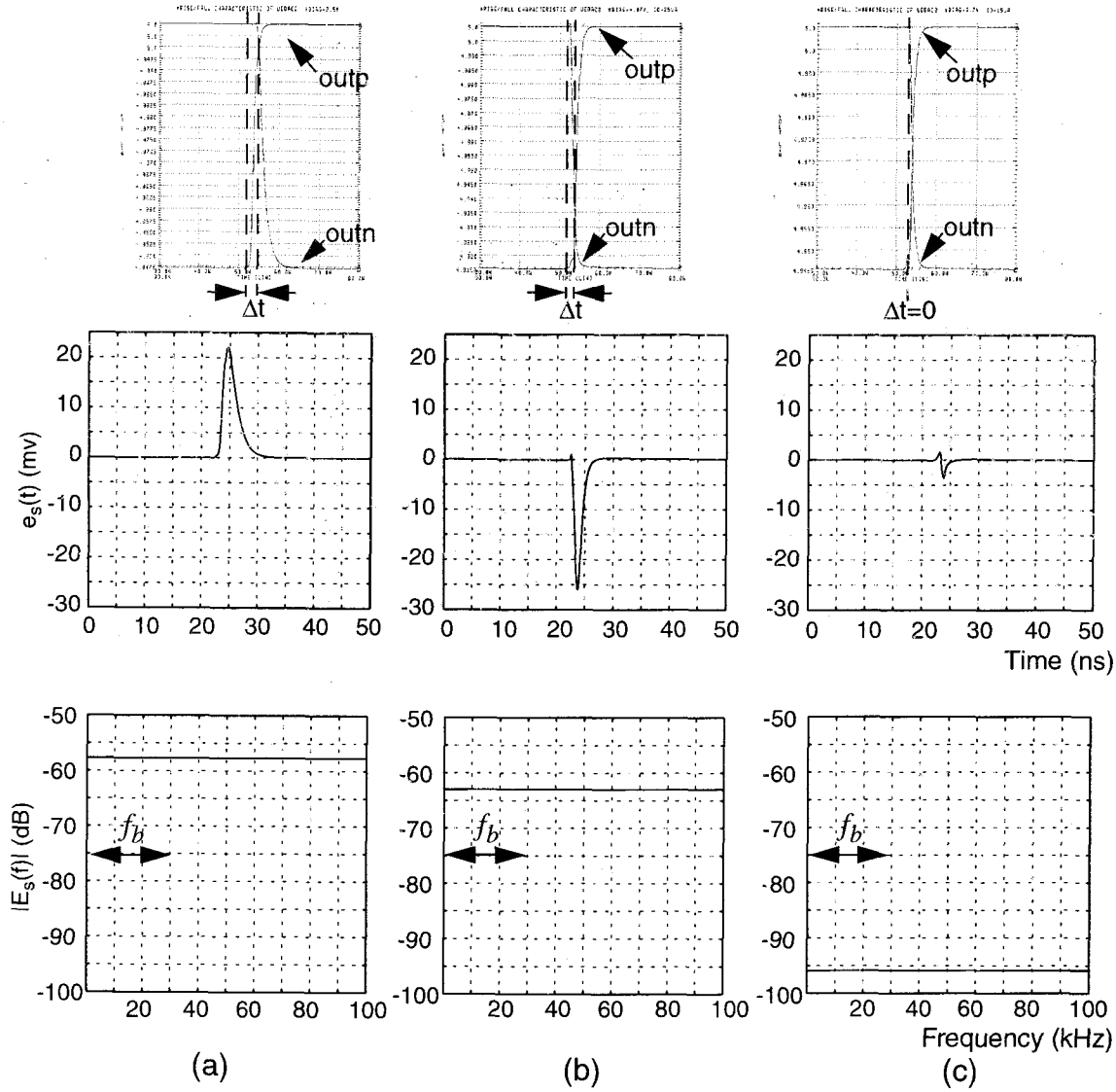


Figure 6.11: Rise/fall characteristic of UEDAC2: (a) V_{bias}=2.5V; (b) V_{bias}=4.07V; (c) V_{bias}=3.70V. The first row shows output waveforms, the second row shows the error signal $e_s(t)$ and the third row shows the E_s(f) spectrum. f_b is the band of interest.

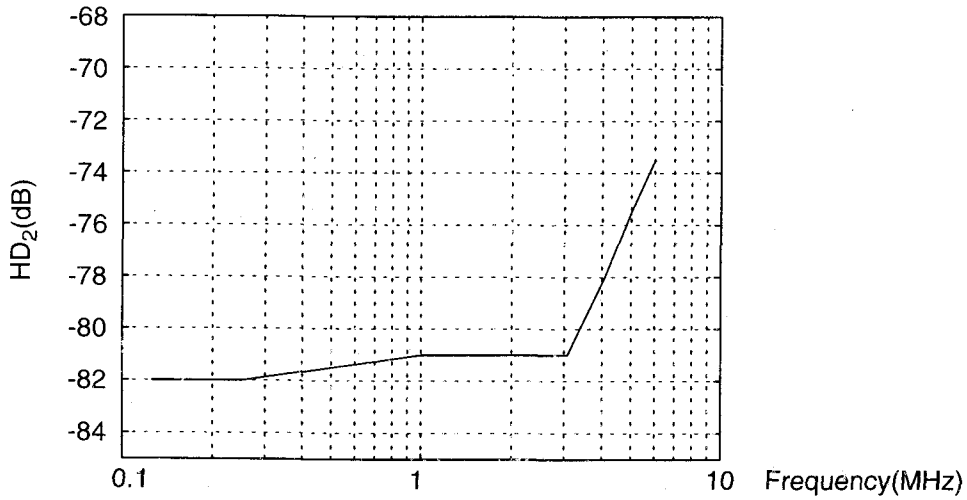


Figure 6.12: HD_2 versus sampling frequency under optimal bias condition.

With the optimal threshold voltage, the HD_2 of the DAC with mismatch-shaping is improved by 10 dB. Figure 6.12 shows the measured HD_2 versus sampling frequency under the optimal bias condition. It has been observed that V_{bias} has to be lowered to get optimal performance as f_s increases. Thus, even though the linearity of the DAC can be improved by careful adjustment of the threshold voltage, this is not a reliable method in practice. Section 6.3.3 will show that modified mismatch shaping (MMS) offers a more elegant solution.

6.3.2 Bandpass mismatch shaping

To test the effectiveness of the bandpass mismatch-shaping algorithm, a sixth-order bandpass modulator with 17 level quantization is designed and implemented. A simple $z \rightarrow -z^2$ transformation applied to the prototype third-order lowpass modulator results in the structure shown in Figure 6.13. This bandpass modulator has its center frequency located at $f_s/4$ and preserves all the characteristic of the lowpass modulator (such as SNR, stability, etc.).

Figure 6.14 shows the measured spectrum of the bandpass delta-sigma DAC when clocked at f_s = 500 kHz. A zoomed-in measurement is shown in Figure 6.15. It can be seen in this figure that after bandpass mismatch shaping is applied, the noise floor decreases by about 14 dB. As was the case for the lowpass DAC test, the measurable in-band SNR is limited by the spectrum analyzer. A more accurate SNR measurement will be performed later, with the help of a notch filter.

Since the signal is applied near $f_s/4$, all the signal harmonics are located outside the band of interest, but the intermodulation terms can be observed in the experiment. In Figure 6.15(a), a single-tone test is performed. Because of folding, the third-order and fifth-

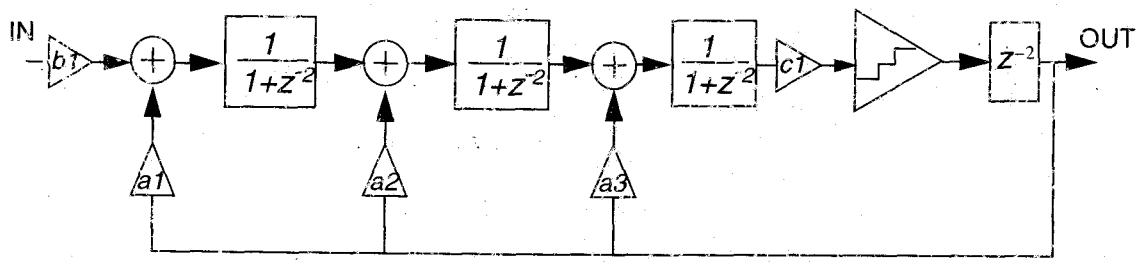


Figure 6.13: System diagram of a 6th-order bandpass delta-sigma modulator.

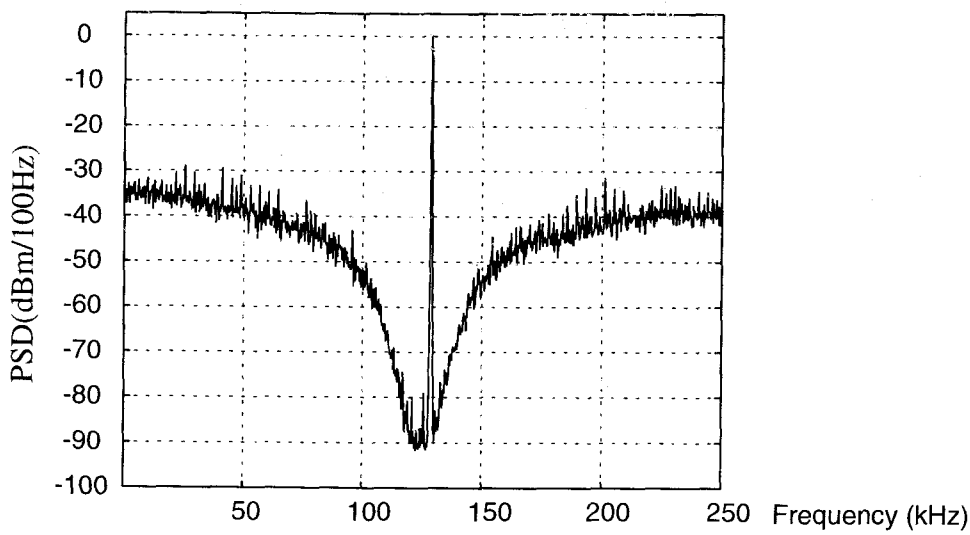


Figure 6.14: Measured spectrum of the 6th-order bandpass DAC (f_s=500kHz).

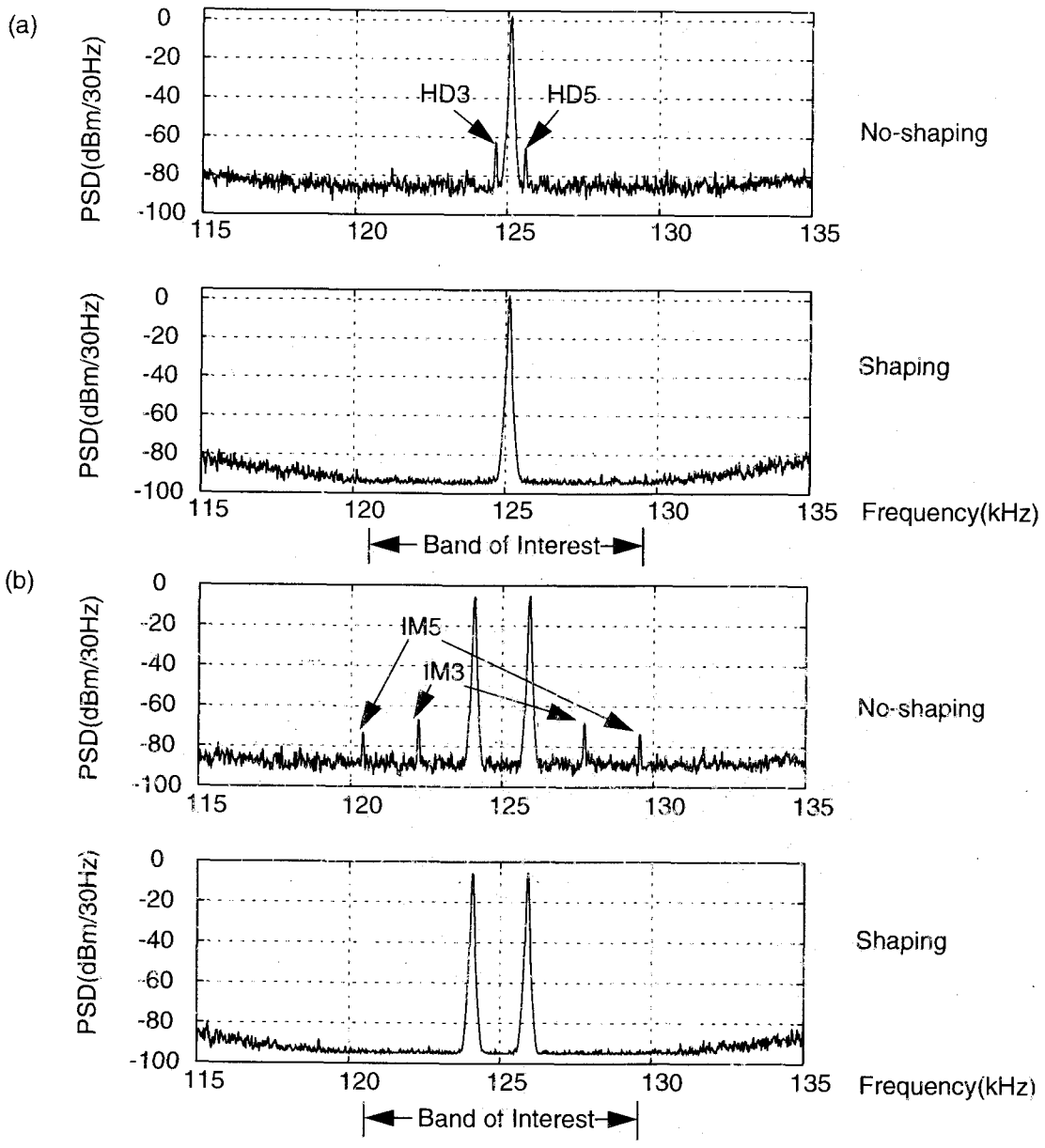


Figure 6.15: Measured spectrum of bandpass delta-sigma DAC at f_s=500kHz: (a) single-tone test; (b) two-tone test.

order harmonics occur at offsets $-3\Delta f$ and $+5\Delta f$, respectively, where Δf is the offset of the fundamental from the center frequency.

After mismatch shaping, HD3 and HD5 are reduced from -64 dB and -69 dB to less than -95 dB. Thus, mismatch-shaping greatly improves the linearity of the bandpass DAC in our experiment.

The above argument is further verified with a two-tone test shown in Figure 6.15(b). The third-order and fifth-order IM products are found to be

$$IM3 = 2f_1 - f_2 \text{ and } \quad IM3 = 2f_2 - f_1 \,. \tag{6.10}$$

$$IM5 = 3f_1 - 2f_2 \text{ and } \quad IM5 = 3f_2 - 2f_1 \,, \tag{6.11}$$

assuming $f_2 > f_1$. Again, after mismatch shaping, these IM terms are suppressed by more than 20 dB.

The effect of dynamic error on the output of a bandpass delta-sigma DAC is also examined. It is found that the mismatch shaping DAC shows the same degree of sensitivity to mismatched rise/fall characteristic as the no-shaping DAC does. This conclusion is drawn from the fact that as the threshold voltage V_{bias} varies, the measurable in-band noise and intermodulation products (which are out of band) remain almost the same. The exact effect of the dynamic error on the SNR will be investigated further with the notch filter.

The reason for this immunity to the dynamic error for a bandpass mismatch-shaping DAC is due to the algorithm employed: the element selection algorithm in bandpass mismatch shaping is to use the elements repeatedly, therefore, the element switching activity is almost the same whether shaping is applied or not. This can be best illustrated by referring to Figure 6.16, which compares the element selection methods between mismatch shaping and no shaping. Since the dynamic error is proportional to the element switching activity, the dynamic error is the same. Figure 6.17 shows the simulation result which supports the above analysis.

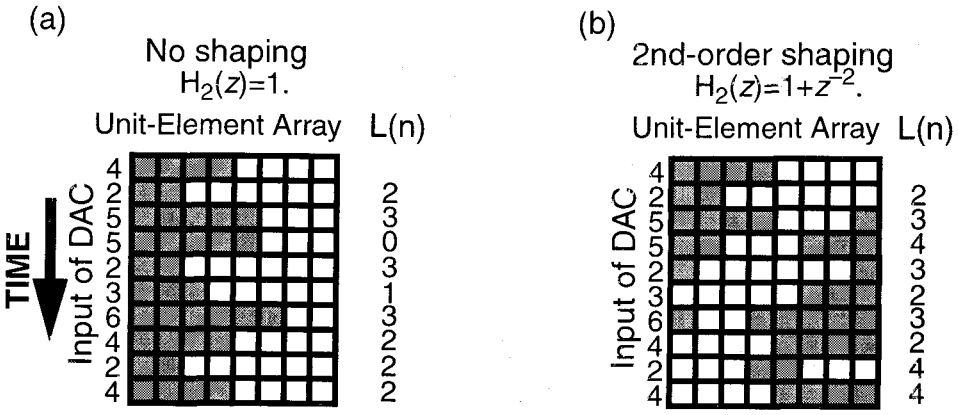


Figure 6.16: Comparison of the element selection patterns and switching activity: (a) no mismatch shaping; (b) mismatch shaping. L(n) denotes number of elements switching in each clock cycle.

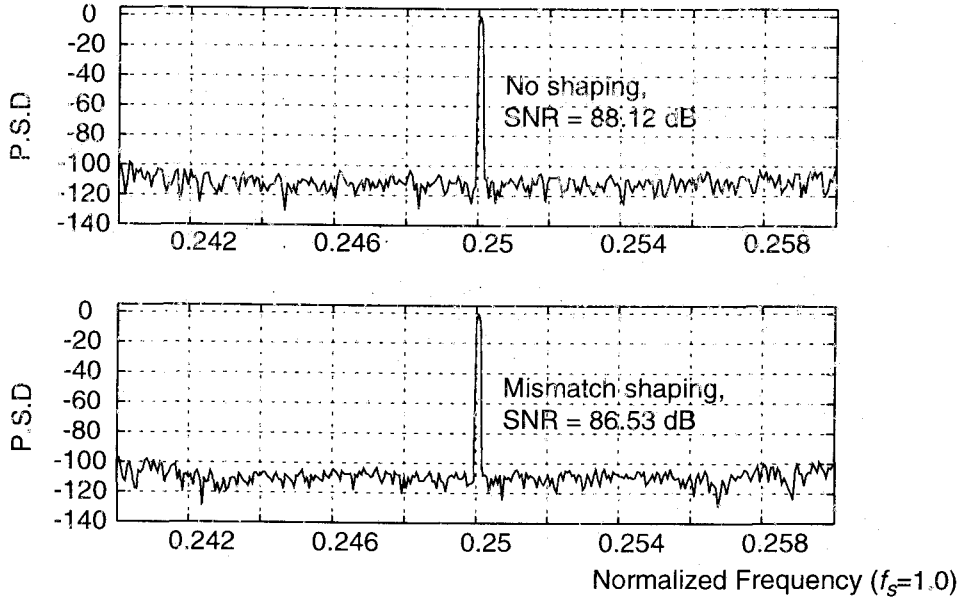


Figure 6.17: Simulated effect of 0.1% dynamic error on a bandpass delta-sigma DAC: (a) no mismatch shaping; (b) mismatch shaping.

6.3.3 Modified mismatch shaping

As discussed in Section 6.3.1, dynamic errors limit the performance of a lowpass mismatch shaping DAC, especially at high sampling frequencies. Optimal biasing can improve the linearity, but it is not an attractive method because of the need for tuning.

Modified mismatch shaping (MMS), a system-level algorithm proposed in Chapter 3, offers a better solution.

UEDAC2 is used as a test bed for MMS testing. Due to the limited hardware capacity of the XC4010E, only eight out of sixteen unit elements of UEDAC2 are used for the verification of MMS. Thus, a 9-level delta-sigma DAC replaces the 17-level prototype. The experimental result for f_s=2MHz is shown in Figure 6.18. First-order mismatch shaping attenuates the noise floor and reduces harmonic distortion when compared with the no-shaping case, but HD_2 is still about -73 dB. After MMS is applied, it attenuates the noise floor and virtually eliminates the harmonic distortion. Over 85 dB of spurious free dynamic range (SFDR) is achieved.

Since the MMS algorithm tries to reduce the dynamic error, it is inherently insensitive to dynamic effects such as mismatched on/off delay. The experimental results

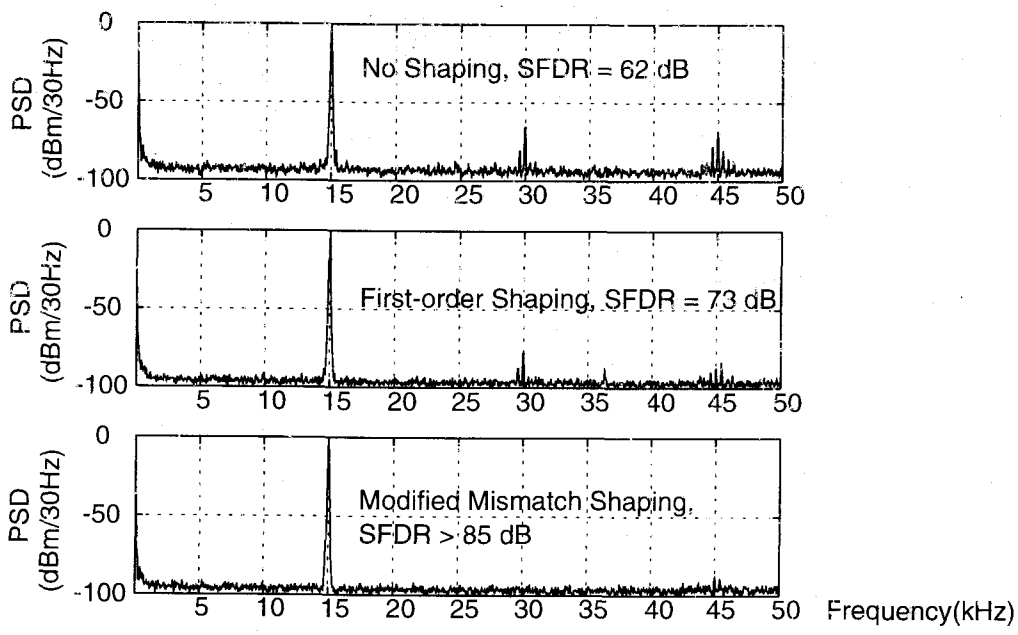


Figure 6.18: Measurement of the 9-level lowpass delta-sigma DAC (f_s=1.92MHz): (a) no shaping; (b) first-order shaping; (c) modified mismatch shaping.

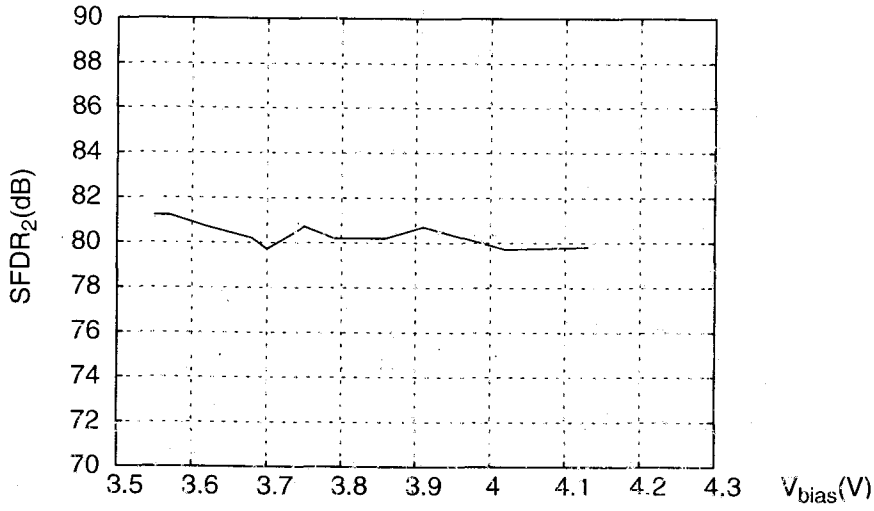


Figure 6.19: HD_2 versus threshold voltage V_{bias} when MMS is applied.

of Figure 6.19, where HD_2 is plotted as a function of V_{bias}, show that HD_2 is virtually independent of V_{bias}, confirming that element dynamics are irrelevant.

Figure 6.20 shows the measured HD_2 versus sampling frequency when MMS is applied. For comparison purposes, the HD_2 with first-order shaping (without optimal bias) is also plotted on the same graph. This graph shows that a significant improvement can be obtained, especially at high sampling frequencies.

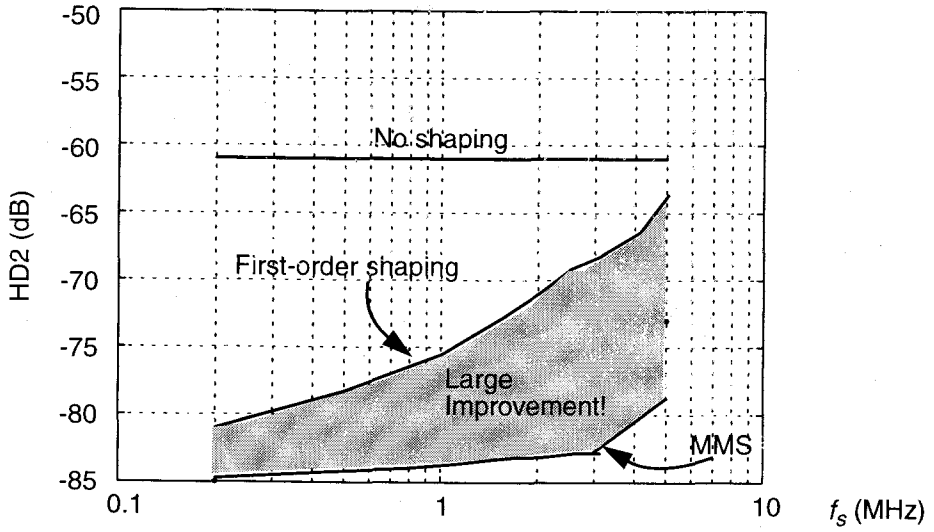


Figure 6.20: Measured HD_2 versus sampling frequency.

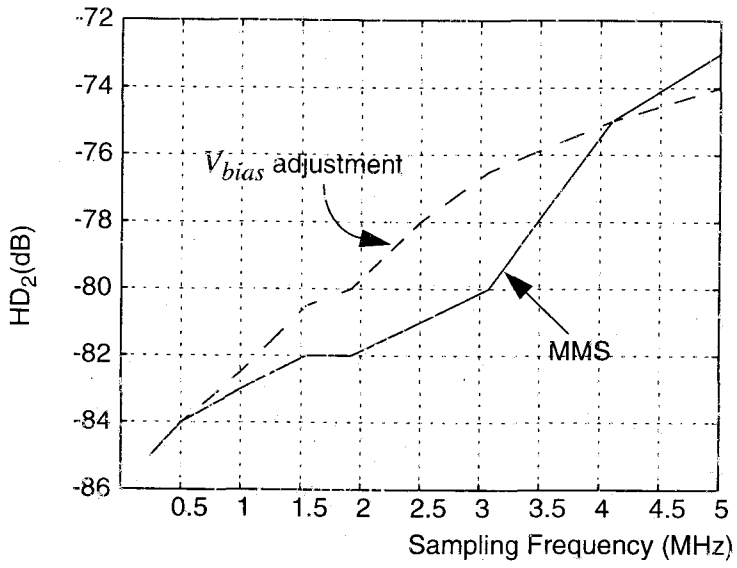


Figure 6.21: Measured HD_2 versus sampling frequency with V_{bias} adjustment and MMS method.

It is necessary to compare the two methods used in our experiment to improve DAC linearity. One is the manual adjustment of V_{bias}, the other is the MMS algorithm. Figure 6.21 shows the comparison of the measured HD_2 with V_{bias} adjusted at each sampling frequency to give the lowest HD_2 with the MMS algorithm. At low sampling frequencies, both methods provide the same performance in terms of linearity. But as f_s increases, the DAC using MMS method has a smaller HD_2 compared with the V_{bias} adjustment method. When the sampling frequency goes into the range over 4MHz, MMS generates larger HD_2 and its performance degrades rapidly as the sampling frequency increases further. The reason for this degradation is due to the speed limitation of the FPGA we used in our experiment: as the MMS method involves intensive digital computation (namely sorting), the FPGA used in this experiment can not operate accurately at such high speed. However, if MMS is implemented in a custom IC with today's advanced submicron technology, it is quite practical to operate MMS correctly at a much higher speed.

6.4 Notch Filter for SNR Measurement

It has been demonstrated that mismatch shaping can reduce the harmonic distortion in a multi-bit delta-sigma DAC. Since the SNR cannot be directly measured by the spectrum analyzer when a large signal tone exists, other approaches must be taken for this measurement. In this section, the SNR is measured after notching out the signal.

The principle of using a notch filter for SNR measurement is that by removing the signal tone at the output of the DAC, the spectrum analyzer will not be overloaded by the presence of a large signal. In our test setup, a second-order active RC notch filter, shown in Figure 6.22 [68], is designed and implemented. The notch filter implements the following transfer function:

$$H(s) = \frac{s^2 + \omega_o^2}{s^2 + (\omega_o s)/Q + \omega_o^2} \tag{6.12}$$

where Q is the quality factor and ω_o is the notch frequency. In our implementation, we choose $f_o = \omega_o/(2\pi) = 3.9\,\text{kHz}$, $Q = 0.707$. The numbers shown in parentheses in Figure 6.22 are the actual element values used in the circuit. The LF353 is selected for the opamp due to its high speed (4MHz gain-bandwidth product) and high linearity (0.02%

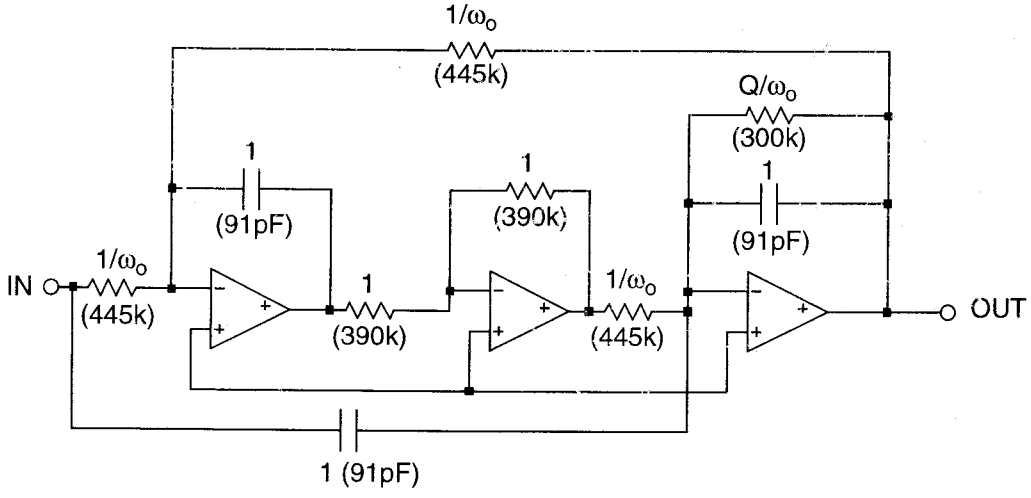


Figure 6.22: A second-order notch filter for SNR measurement.

distortion with 15V peak to peak output) [69].

The notch filter is implemented on the test board to notch out the signal tone at 3.91 kHz, when a 500 kHz sampling frequency is applied. The measured notch filter frequency response is shown in Figure 6.23. It should be noted that due to resistor and capacitor tolerances, the position of the notch and the height of the dip will be affected. Special care has been taken to minimize these effects.

The SNR of the 17-level DAC is measured when first-order mismatch shaping and no shaping are employed. It is found that the measured noise floor from the spectrum analyzer is about -124 dBm/Hz when first-order shaping is used. This gives 85 dB SNR in an 8 kHz bandwidth. When no mismatch shaping is employed, the in-band noise floor can be directly measured without the notch filter (in fact, after the notch filter is adopted, we observed the same noise floor as the noise floor directly observed at the output of UEDAC2). Under this condition, the SNR is only 73 dB.

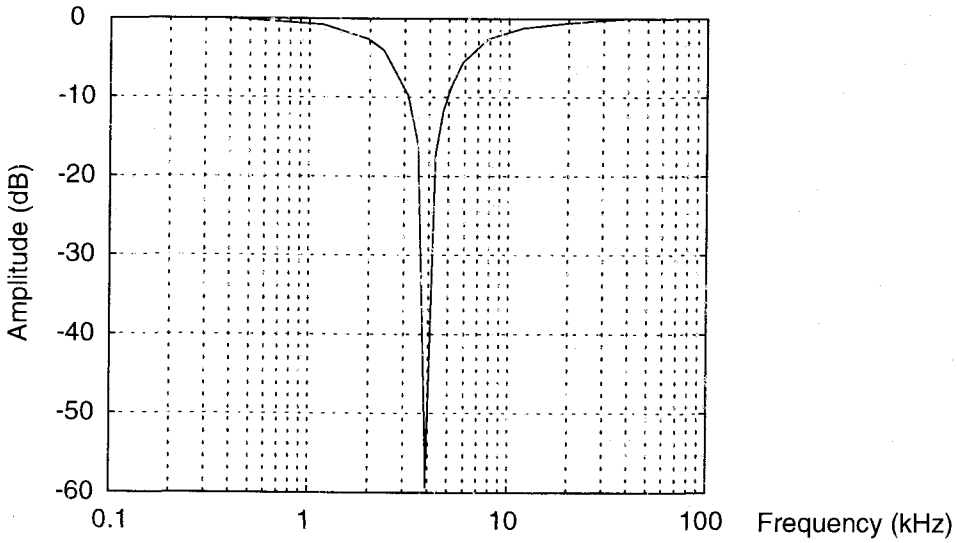


Figure 6.23: Measured notch filter frequency response.

The noise contribution of the notch filter itself is also measured. It is found that with zero input to the DAC, the noise floor at the output of UEDAC2 is -143 dBm/Hz (referenced to a 50Ω resistor), but the noise floor at the output of the notch filter is -123 dBm/Hz. Thus, the notch filter contributes about 20 dB of noise in the band of interest, which sets the fundamental limit in our overall SNR measurement. Choosing a low-noise operational amplifier or redesigning the notch filter using passive elements and smaller resistors would help to reduce the noise contributed by the notch filter.

It is also found that there exists a 'critical' value for the output swing of the DAC. When the amplitude of the sine wave output exceeds $1.2V_{p\text{-}p}$ (or -2.0 dBm in terms of power), the observed noise floor at the output of the notch filter goes up about 10 dB. Two possible error sources might be responsible for this abrupt increase of the noise floor: one is the DAC itself which introduces this large amount of noise above a certain bias current level (or operates in large signal mode); the other one is the notch filter which produces higher noise when it takes a large input from UEDAC2. Experiments have been carried out to identify the actual source of trouble: the extra noise floor with large output signal does

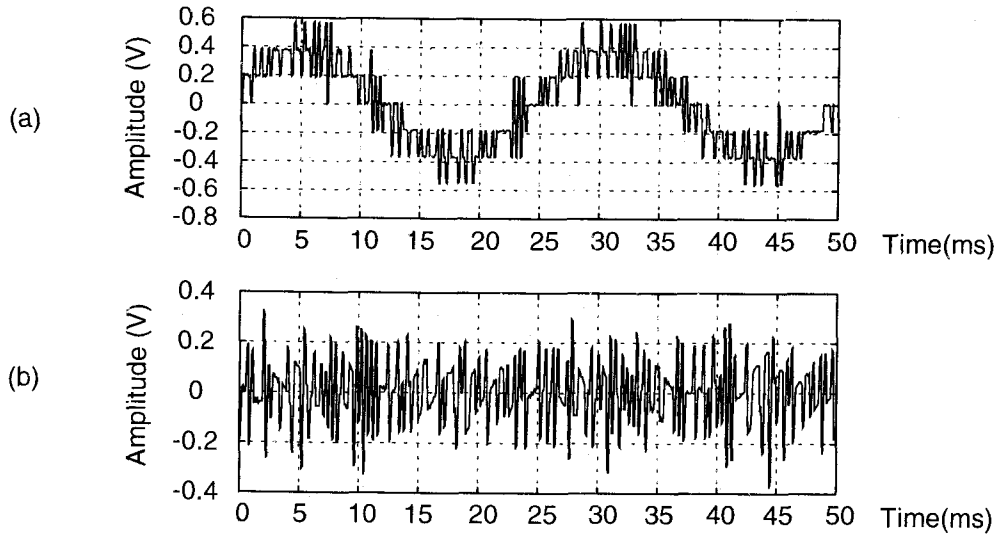


Figure 6.24: Measured UEDAC2 waveform: (a) before notch filter; (b) after notch filter.

not come from the DAC itself, since when we change the bias current and load resistor, this 'critical' signal level does not change: it is always around 1.2V peak-to-peak regardless of the bias current and load resistance. Therefore, these extra noise must come from the notch filter. As shown in Figure 6.24(a), the output of UEDAC2 consists of step-like signals, which can drive the opamp into the nonlinear operation region and result in an increased noise floor.

The analysis above has been verified by adding a passive lowpass filter after UEDAC2 and before the notch filter. A first-order RC filter is used to suppress the high frequency noise before it is fed into the notch filter. As we expected, the 'critical' value of the output increases; now a 2.4 V_{p-p} output can be tolerated without overloading the notch filter. Thus, the highest measurable SNR in this configuration is about 88 dB.

It has been shown in previous sections that dynamic errors have a significant effect upon the linearity of the DAC when mismatch-shaping is employed. However, the effect of dynamic error on the SNR of the DAC is not so obvious. In our experiment, when we adjust the threshold voltage V_{bias} by changing the bias current, we don't observe any significant change of the noise floor at the output of the notch filter when first-order mismatch shaping is applied. This agrees with our simulations which suggest that dynamic errors have much greater effect on distortion than on the noise level of the DAC.

The SNR of a bandpass delta-sigma DAC is also measured. As in the lowpass case, the noise floor of the DAC can only be measured after the notch filter is applied. An 85 dB SNR is measured when the modulator is operated at f_s=500 kHz and OSR=32.

Finally, the SNR performance of zero-order mismatch shaping, first-order mismatch shaping and modified mismatch shaping with a 9-level delta-sigma DAC are

compared in Figure 6.25. In this graph, an optimal threshold voltage is used to give the best linearity for first-order shaping. When no shaping is applied, mismatch error introduces large amount of noise in the band of interest and the notch filter's dip can be clearly identified in Figure 6.25(a). When first-order mismatch shaping is applied, as discussed before, the in-band noise is limited by the notch filter. Over 85 dB SNR can be measured. When MMS is applied, we can see there is a slightly increase in the noise floor at the upper portion of the band of interest. This is due to the compromise inherent in the MMS algorithm: minimizing the dynamic effects causes a slightly degradation in the effectiveness of the mismatch shaping. This results in an SNR about 82 dB for MMS. The slight SNR degradation for MMS is consistent with the simulation results of Chapter 3.

In Chapter 5, scrambling of the input **sv** vector was used in the design of the digital interface of UEDAC2 to minimize crosstalk and interference between the elements and the reference current. In the experiment, UEDAC2 shows the same linearity and SNR when scrambling is enabled and disabled under mismatch-shaping condition. This suggests that

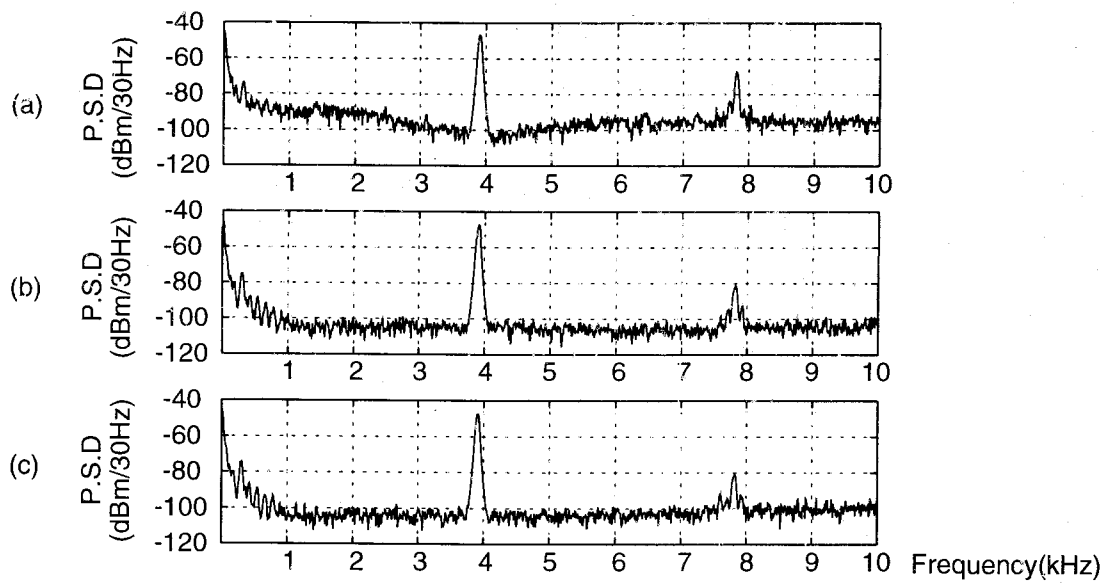


Figure 6.25: Measured UEDAC2 spectrum after the notch filter: (a) no-shaping; (b) first-order shaping; (c) modified mismatch shaping.

thanks to careful layout, the interference of the analog and digital portion of the system is not a significant error source.

6.5 Summary

In this chapter the second generation unit element DAC (UEDAC2) is used to experimentally verify various mismatch shaping algorithms. Measurements show that first-order mismatch-shaping can improve the SNR and linearity by more than 10 dB, compared with the no-shaping condition. The linearity provided by first-order shaping is limited at high speed applications due to dynamic effects. Modified mismatch shaping has been proven to be an effective way of minimizing the dynamic effects while shaping the element mismatch error in the band of interest, at the cost of a slightly increased noise floor. Compared with UEDAC1, UEDAC2 with optimal bias has over ten times better linearity in high frequency applications.

Chapter 7. Conclusions

7.1 Summary

Delta-sigma ADCs and DACs were introduced in Chapter 2. The advantages of multi-bit quantization were highlighted and existing mismatch-shaping methods were briefly reviewed.

In Chapter 3, the principle of mismatch-shaping was introduced, followed by an illustration of lowpass mismatch-shaping and the newly proposed bandpass mismatch-shaping. To overcome the static mismatch error and dynamic error existing in a continuous-time multi-bit delta-sigma modulator, modified mismatch shaping was developed. The implementation considerations for these mismatch-shaping schemes were covered.

In Chapter 4, the first version of a unit-element DAC (UEDAC1) was tested. Experimental results confirmed the effectiveness of lowpass mismatch shaping algorithm at low frequencies. Various error sources were analyzed in order to find the cause of the high- frequency performance degradation. Mismatched on/off delay was identified as the major source of error.

A second version of the unit-element DAC (UEDAC2) was designed in Chapter 5. The goal was to achieve higher performance at higher speed, compared to UEDAC1. A single-ended switch driver was adopted in the design for fast switching and the flexibility of on/off delay adjustment. Local current biasing and an improved digital interface was developed to minimize the effect of clock jitter and the interaction between the unit elements and the reference current.

In Chapter 6, UEDAC2 was tested with the proposed mismatch shaping schemes. The experimental results further confirm the effectiveness of those mismatch shaping algorithms. A higher linearity (over 80 dB SNR and SFDR) delta-sigma DAC operated at higher speed (up to 20 kHz signal band), has been achieved through the use of the modified mismatch shaping.

7.2 Future Work

Modified mismatch shaping tries to minimize the dynamic error by making the switching events per period nearly constant. An obvious improvement would be to make the number of switching events per period have a noise-shaped spectrum. First-order modified mismatch shaping suffers approximately 3dB noise penalty compared with the DWA algorithm. Thus, the development of a second-order MMS could help to achieve better suppression of the in-band noise.

Further theoretical work can be done to deepen the understanding and improve the performance of the mismatch-shaped DAC. The stability of high-order systems, the design of optimal vector quantizers (including dithering), the use of non-unit elements, and the optimal realization of the selection logic are all fertile areas for study.

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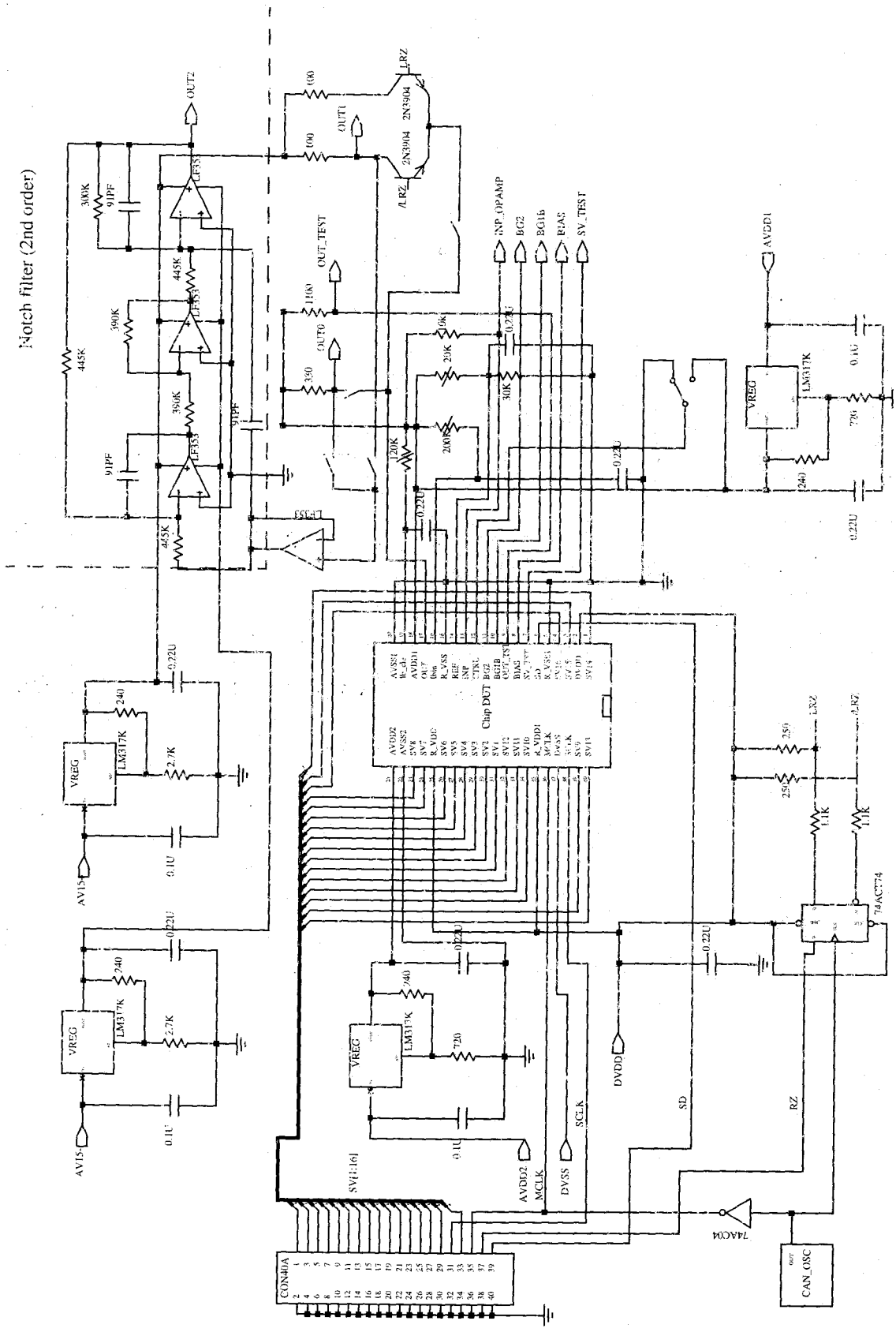
APPENDIX . Schematic of the Test Board