AN ABSTRACT OF THE THESIS OF

Terry E. McMahon for the degree of Master of Science in Electrical and Computer Engineering presented on June 10, 1994.

Title: Design, Fabrication and Characterization of Complementary Heterojunction Field Effect Transistors.

Approved: Redacted for Privacy

Stephen M. Goodnick, Advisor

Complementary delta-doped AlGaAs/GaAs Heterojunction Field Effect Transistor (CHFET) devices and circuits were fabricated using MBE and a 2μ non-planar gate recess process. Several schemes were used in an attempt to improve the performance of the p-channel HFETs. These included delta-doping, carbon-doping and dipole-doping. Circuits and individual n- and p- channel devices were fabricated on a stacked delta-doped complementary structure. The circuits failed to perform due to complications with adjusting the threshold voltage. However, Individual devices were successfully characterized, p-channel devices with extrinsic transconductances up to 14 mS/mm, n-channel devices with extrinsic transconductances up to 120 mS/mm and a unity power gain bandwidth of 5.5 GHz.

Design, Fabrication and Characterization of Complementary Heterojunction Field Effect Transistors

by

Terry E. McMahon

A THESIS
submitted to
Oregon State University

in partial fulfillment of
the requirements for the
degree of

Master of Science

Completed June 10, 1994
Commencement May 1995

APPROVED:

Redacted for Privacy

Professor of Electrical and Computer Engineering in charge of major

Redacted for Privacy

Head of Department of Electrical and Computer Engineering in charge of major

Redacted for Privacy

Dean of Graduate School

Date thesis is presented June 10, 1994

Typed by Terry E. McMahon

Table of Contents

List of Figures

List of Tables

Design, Fabrication and Characterization of Complementary Heterojunction Field Effect Transistors

1. Introduction

There is increasing interest in the development of complementary technology for GaAs. Up to now, Si CMOS technology has acted as the catalyst for the development of analog and digital integrated circuits. The high-speed advantage of GaAs has attracted the use of complementary heterojunction field effect transistors (CHFET) in analog and digital circuit applications. However, there is a lack of complementary technology for GaAs because of the poor performance associated with the p-channel devices due to their low hole mobilities. In GaAs, there is a large difference in the electron and hole mobilities, which results in a large mismatch in the gain of n- and p-channel devices with the same gate dimensions. Improved hole mobilities were successfully obtained using pseudomorphic InGaAs HFETs here at Oregon State University, thus improving the performance of the p-channel HFETs.

1.1 Historical Development

The foundation for the HFET was developed on the concept of superlattices studied by Esaki et al [1] in the late 1960s. This group was first to suggest that enhanced mobilities could be obtained in a superlattice structure of GaAs/AlGaAs when electrons are transferred from the doped AlGaAs system to an undoped GaAs system. A few years later in 1978, a group from Bell Laboratories (Dingle et al [2]) observed higher mobilities in the heterojunction of a GaAs/AlGaAs system using the concept of modulation doping. Modulation doping is based on the separation of electrons from their source impurity

dopant by selectively doping the AlGaAs layer of the heterostructure. The modulation doped heterostructure forms the basis of a large class of HFET structures. In 1980, the first of the HFET devices was fabricated on modulation doped heterostructures (MODFET), followed by circuits soon thereafter [3]. Since then, substantial effort has been made to improve the performance of the HFET, and research and development continues to this day.

Submicron InGaAs/AlGaAs n-channel HFETs have been reported with room temperature transconductances on the order of 920 mS/mm [4]. Typical noise figures of 1.9 dB at 60 GHz and maximum gains of 13.0 dB at 60 GHz and 9.2 dB at 92 GHz, corresponding to an f_{max} of 270 GHz, have been demonstrated in n-channel devices [4]. Other reports show noise figures of 2.5 dB with an associated gain of 4.7 dB at 92.5 GHz [5], which demonstrates the pseudomorphic HFETs exceptional microwave characteristics.

In comparison, the InGaAs/AlGaAs p-channel HFETs have been reported with substantially lower room temperature transconductances on the order of 113 mS/mm [6], as expected due to the lower hole mobilities of p-channel devices.

1.2 Operation of a MODFET

One particular HFET configuration under investigation in this research is the MODFET. The conventional MODFET is a heterostructure consisting of two different material systems: an undoped GaAs layer and a doped AlGaAs layer grown epitaxially in a continuous crystal structure (see figure 1.1). In a MODFET, a channel forms in the undoped GaAs by carrier transfer from ionized impurities (donors/acceptors) near the interface of the heterojunction. The carriers diffuse from the higher bandgap AlGaAs material to the lower bandgap GaAs material, and are confined by a triangular energy well at the heterojunction. The carriers form a thin planar active channel parallel to the

heterojunction interface and produce what is known as a two dimensional electron/hole gas (2DEG or 2DHG).

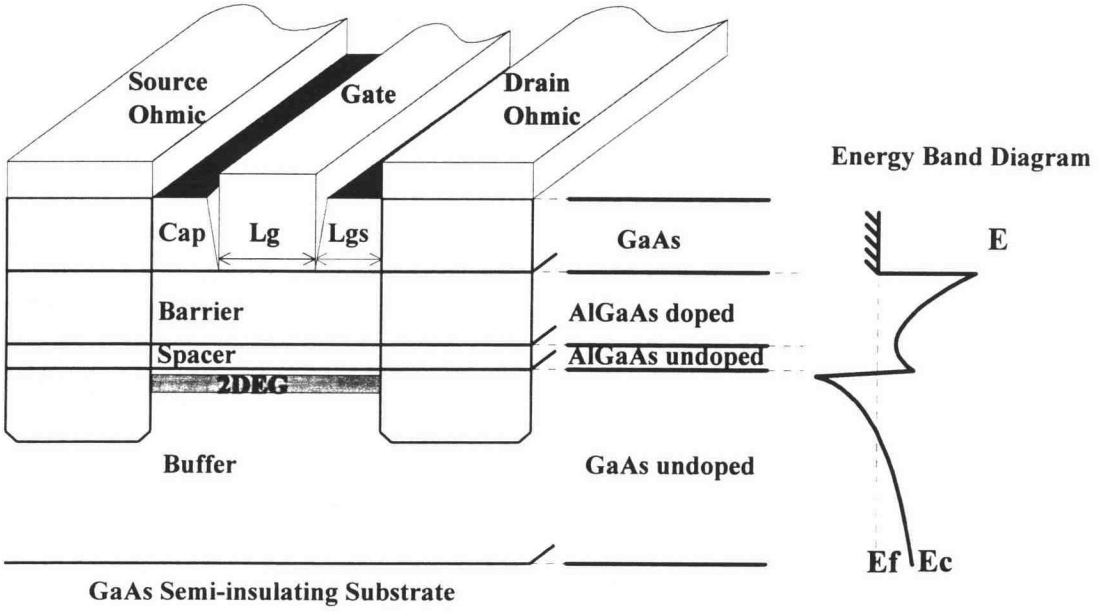

Figure 1.1. Cross-sectional view of a MODFET and the associated energy band diagram.

The MODFET consists of four distinct layers: the buffer, spacer, barrier and cap. The buffer layer consists of an unintentionally doped GaAs active layer where the two dimensional electron/hole gas resides. The buffer layer serves as the channel between source and drain contacts in the device. To further reduce the impurity scattering in the MODFET, an undoped AlGaAs spacer layer lies between the undoped GaAs buffer layer and the doped AlGaAs barrier layer to separate the carriers from the donors. The separation reduces the scattering potential and thus increases the carrier mobility and velocity. A doped AlGaAs barrier layer supplies carriers for channel conduction and aids Schottky barrier formation. A GaAs cap, placed on the doped AlGaAs barrier layer, protects it from oxidation and enhances ohmic contact to the channel.

Improved hole mobilities and room temperature (300K) electron mobilities, which in turn give improved device performance, can be achieved by the addition of a thin

pseudomorphic InGaAs layer grown on the GaAs buffer layer, which serves as the active layer where the 2DEG/2DHG resides [7,8]. In the pseudomorphic structure, the carriers diffuse from the higher bandgap AlGaAs material to the lower bandgap InGaAs material, and are confined by a quantum well at the heterojunction.

This structure, shown in figure 1.2, is known as the pseudomorphic or strained layer MODFET. The saturation velocity in InGaAs is greater than that in GaAs. For n-channel structures, the 300K electron mobility is higher in InGaAs than in GaAs ($\mu_{n300k}^{InGaAs} > \mu_{n300K}^{GaAs}$) due to the lower electron mass. However, at 77K the electron mobility is less in InGaAs than in GaAs ($\mu_{n77k}^{InGaAs} < \mu_{n77K}^{GaAs}$) due to alloy scattering. In p-channel devices, the 300K hole mobility in InGaAs is larger than that of GaAs ($\mu_{p300k}^{InGaAs} > \mu_{p300K}^{GaAs}$) due to the strain-induced splitting of the light and heavy hole valance bands [4]. At 77K, although alloy scattering is still present, the hole mobility remains larger in InGaAs than in GaAs ($\mu_{p77k}^{InGaAs} > \mu_{p77K}^{GaAs}$) due to the splitting of the valance bands.

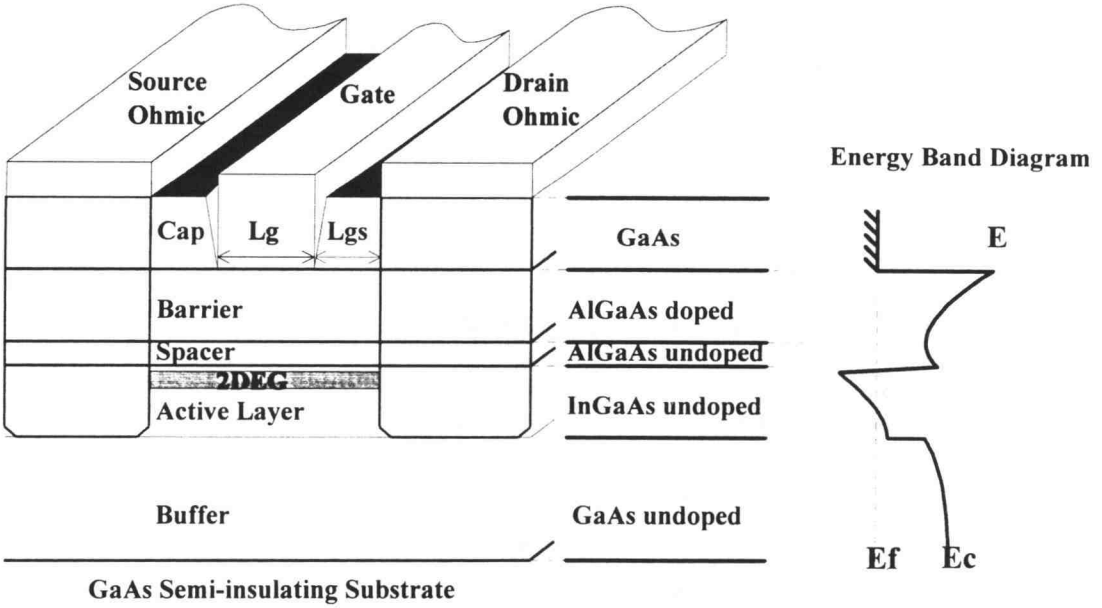

Figure 1.2. Cross-sectional view of a pseudomorphic MODFET and the associated energy band diagram.

A Schottky barrier gate, placed between the source and drain on the doped AlGaAs layer, modulates the two dimensional electron gas in the undoped GaAs material (or InGaAs material for pseudomorphic structures). When a voltage higher than the threshold voltage is applied to the gate, carriers accumulate at the interface and form the two dimensional electron/hole gas. Application of a bias between the source and drain ohmic contacts allows current to flow between source and drain, and is controlled by the bias on the gate.

1.3 Current-Voltage Characteristics of the MODFET

The current-voltage characteristics of the MODFET can be expressed using a charge control model summarized by Shur [9]. For long channel MODFETs in the linear and saturation regions, the general expression for current is based on the approximation that the transverse potential variation parallel to the channel is much larger than the longitudinal potential variation perpendicular to the channel. This condition corresponds to the gradual channel approximation.

Consider a n-channel device for simplicity. The 2DEG density in the channel is given by

$$n_s = \frac{C_o}{q}(V_g - V_c(x) - V_t) \tag{1.1}$$

where C_o is the gate capacitance given by

$$C_o = \frac{\varepsilon}{d + \Delta d} \tag{1.2}$$

$V_c(x)$ is the channel potential, V_t is the threshold voltage, ε is the permittivity of the $Al_XGa_{1-X}As$ and Δd is the separation of the AlGaAs interface to the 2DEG. The source to drain current I_{ds} is given by

$$I_{ds} = qn_s v(x) W, \tag{1.3}$$

where W is the gate width and $v(x)$ is the electron velocity as a function of electric field in the channel expressed by a two-piece linear approximation [10]

$$\begin{aligned} v &= \mu_n E \qquad E<E_c \\ v &= v_s \qquad E>E_c, \end{aligned} \tag{1.4}$$

where μ_n is the low field mobility, v_s the saturated velocity and E_c is the critical field. In short channel devices, the current saturates due to velocity saturation before pinchoff is reached. For this case, the saturation current is given by

$$I_{dsat} = \beta V_o^2 \left(\sqrt{1 + \left(\frac{V_g - V_t}{V_o} \right)^2} - 1 \right) \tag{1.5}$$

where

$$\beta = \frac{\mu_n W C_o}{L} \tag{1.6}$$

$$V_o = \frac{L v_s}{\mu_n} \tag{1.7}$$

in which v_s corresponds to the saturated velocity, W is the gate width, L is the gate length, μ_n is the 2DEG carrier mobility.

For a short channel device, V_g-V_t>>V_o, and equation 1.5 is approximately

$$\lim_{L \to 0} I_{dsat} = \beta V_o \left(V_g - V_t \right) \tag{1.8}$$

which is linear in (V_g-V_t). In a long channel device, the square root in equation 1.5 may be expanded to give

$$\lim_{L \to \infty} I_{dsat} = \frac{\beta}{2} \left(V_g - V_t \right)^2 \tag{1.9}$$

which is the same square law behavior as found in long channel Si MOSFETs. The transconductance in the saturation region is given by

$$g_m = \frac{\delta I_{dsat}}{\delta V_g} = \frac{\beta(V_g - V_t)}{\sqrt{1+\left(\frac{V_g - V_t}{V_o}\right)^2}}. \qquad (1.10)$$

In the absence of other parasitic effects, the unity gain frequency f_{max} is given by the same expression as a MOSFET

$$f_{max} = \frac{g_m}{2\pi C_o}. \qquad (1.12)$$

A representational plot of equation 1.10 is shown by the solid curve in figure 1.3. However, in actual devices, the AlGaAs layer may become populated as the gate is forward biased. This gives rise to a parasitic parallel conduction which degrades the transconductance as shown by the dashed curve in figure 1.3.

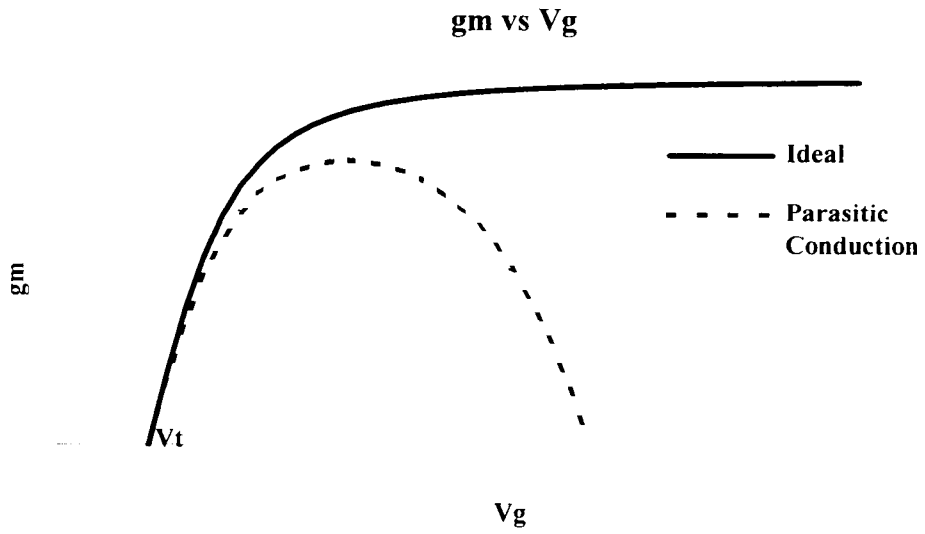

Figure 1.3. Transconductance as a function of gate voltage showing non-ideal parasitic conduction effect.

1.4 Equivalent Circuit Model of the HFET

In any real device, parasitic resistances and capacitances are present as well as the intrinsic behavior discussed in the previous section. Such effects are often represented in a lumped parameter, equivalent circuit model. A number of such models appear in the literature (see for example Yeager et al. [11]). One such model is Cioffi's charge based model shown in figure 1.4 for a n-channel MODFET [12].

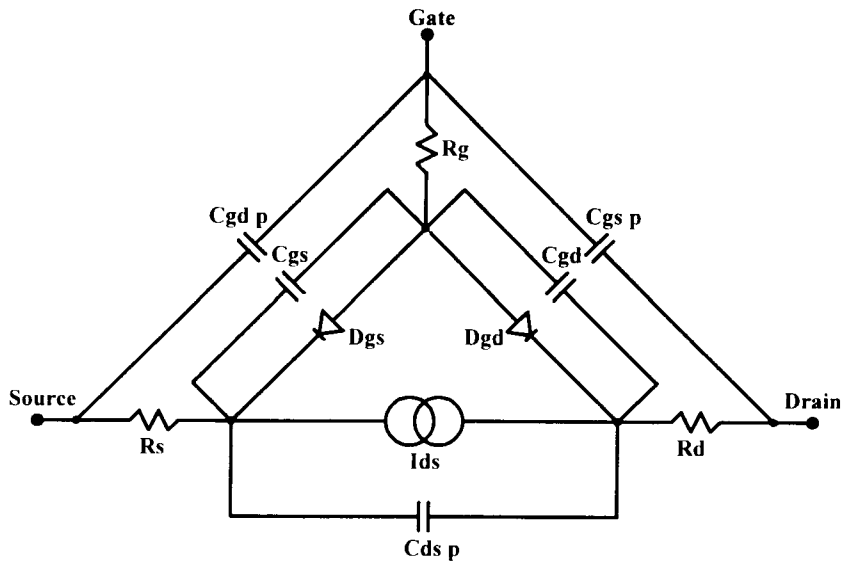

Figure 1.4. Cioffi et al. circuit model representation of an n-channel MODFET.

The intrinsic behavior of the current source I_{ds} in the model was described in the previous section. The two diodes, D_{gs} and D_{gd}, in the model represent the two metal-semiconductor junctions from gate to source and from gate to drain. A detailed discussion on these junctions is given in section 4.3. C_{gs} and C_{ds} represent the fringe capacitance from gate to source and gate to drain, while C_{gsp}, C_{gdp} and C_{dsp} represent the parasitic interelectrode capacitances. R_s, R_d and R_g are series resistances which characterize the ungated portion of the channel between the source to the edge of the gate

and between the drain to the edge of the gate as well as the non-zero contact resistance. Further discussion on these parameters will appear in chapters 4.1 and 4.2 in connection with devices fabricated for the present work.

1.5 Advantages/Disadvantages

GaAs semiconductor devices are capable of operating at microwave frequencies, which gives them a definite speed advantage over Si, because of their high mobility and carrier velocity. Metal semiconductor field effect transistor (MESFET) technology is the most widespread GaAs technology currently used.

The MESFET, previously the fastest field effect transistor technology before the HFET, uses a doped GaAs structure to generate carriers. In the MESFET, the active channel region is heavily doped. Therefore, ionized impurity scattering reduces the carrier mobility and limits the carrier velocity. However, in the HFET, the carriers reside in the undoped GaAs material and are unencumbered by the impurities in the doped AlGaAs material. As a result, ionized impurity scattering is reduced, and the carrier mobility and velocity can be increased. As indicated by equations 1.10 and 1.11, the increase in carrier mobility and velocity give HFETs superior device performance compared to the MESFETs in terms of gain and frequency response.

The disadvantages of HFET technology are the cost of fabrication and, in relation to Si, the cost of substrate materials. The HFET requires precise crystal growth techniques, such as molecular beam epitaxy (MBE), to obtain heterolayers with sharp interfaces, which is relatively expensive. One of the main disadvantages of all GaAs technology is the lack of complementary circuit technology comparable to Si technology. The problem is the poor performance of the p-channel devices due to the low hole mobility as compared to the electron mobility in GaAs.

1.6 Goal of Research

The present goal of this research is to develop complementary circuit technology for GaAs using HFETs. The focus of this thesis is the design, fabrication and characterization of n- and p-channel HFET devices on the same wafer for further use in analog and digital circuit designs. Several schemes were tried and tested to improve the performance of the p-channel HFETs. These included delta-doping, carbon-doping and dipole-doping.

Complementary devices described in this thesis were successfully developed in house and fabricated at Oregon State University using a 2μ non self-aligned process. Individual n- and p-channel devices and circuits were fabricated on a stacked delta-doped complementary structure. The circuits failed to perform due to complications with adjusting the threshold voltage. However, individual devices were successfully characterized, p-channel devices with transconductances up to 14 mS/mm, n-channel devices with transconductances up to 120 mS/mm and unity power gain bandwidths of 5.5 GHz.

To begin, in chapter 2, a review of some of the structures used to develop the CHFET are presented. Process design, fabrication, and layout of devices, circuits and testing structures are detailed in chapter 3. Processing techniques, including a few of the problems involved, are also addressed. Chapter 4 discusses electrical characterization of the devices, which includes ohmic contacts, series resistance, Schottky barriers, threshold voltage control and mobility measurements. Chapter 5 presents representative experimental device characteristics and results obtained in this research including DC and high frequency S-parameter measurements. Finally, chapter 6 presents conclusions drawn from the research and suggestions for improvement.

2. HFET Structures Used in the Present Research

The CHFET devices studied in this thesis were fabricated on MBE grown heterostructures on GaAs substrates. All MBE growths were performed by Don Schulte and Leon Ungier of Oregon State University. The basic complementary structure consists of two epi-layers for both n-channel and p-channel HFET's arranged in a stacked formation to accommodate a non self-aligned process. The first epi-layers investigated for use in developing complementary technology were the conventional GaAs/AlGaAs uniformly doped structures for both n- and p-channel devices. Several other doping profiles were investigated and will be discussed briefly in the next few sections. In an attempt to improve the performance of the CHFET, pulsed- or delta-doped, carbon-doped and dipole layer structures were implemented for the present work. Ideally, the complementary technology was to be carried out on pseudomorphic delta doped InGaAs/AlGaAs heterostructures in this research in an attempt to improve the n- and p-channel device performance. However, difficulties in realizing high mobility n-channel devices in this system led to consideration of GaAs/AlGaAs devices only.

2.1 GaAs/AlGaAs HFET

Conventional GaAs/AlGaAs heterostructures were first implemented as a benchmark for other structures. The GaAs/AlGaAs was one of the first structures used to fabricate HFETs [3]. Although the performance of the p-channel devices is relatively weak, these structures are ideal to use when developing the design process for the CHFET due to their simplicity and reliability.

The GaAs/AlGaAs heterostructures were grown on semi-insulating GaAs substrates (see figure 2.1). This heterostructure consists of a non-doped GaAs active layer and a silicon or beryllium doped (Si for n-type and Be for p-type) $Al_XGa_{1-X}As$

barrier layer separated by an undoped $Al_XGa_{1-X}As$ spacer layer. A thin doped GaAs cap lies on top of the doped $Al_XGa_{1-X}As$ for surface passivation and enhancement of the ohmic contact to the active layer.

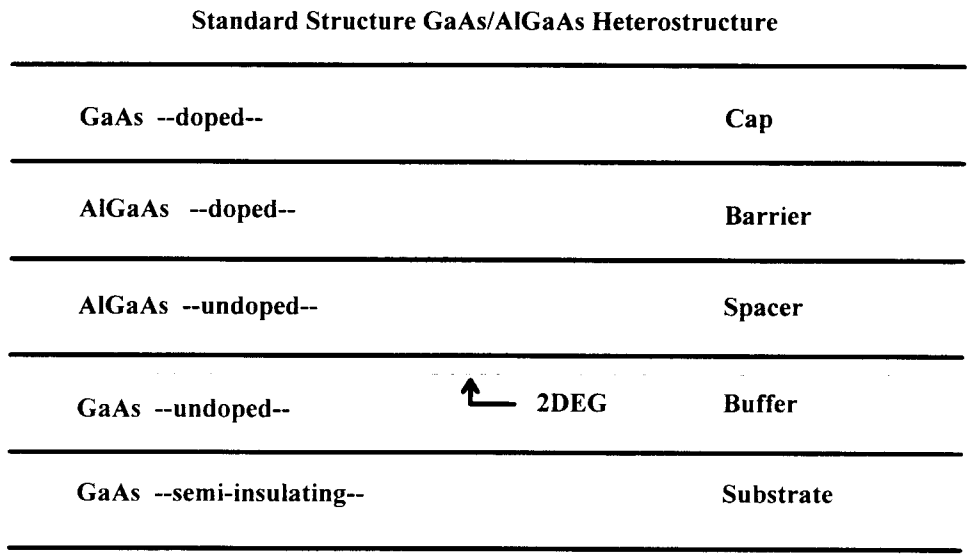

Figure 2.1. Layer structure of an uniformly doped standard GaAs/AlGaAs heterostructure.

A typical energy band diagram of the standard GaAs/AlGaAs structure is shown in figure 2.2. Carriers are confined in a triangular potential well formed at the interface of the GaAs and AlGaAs heterostructure.

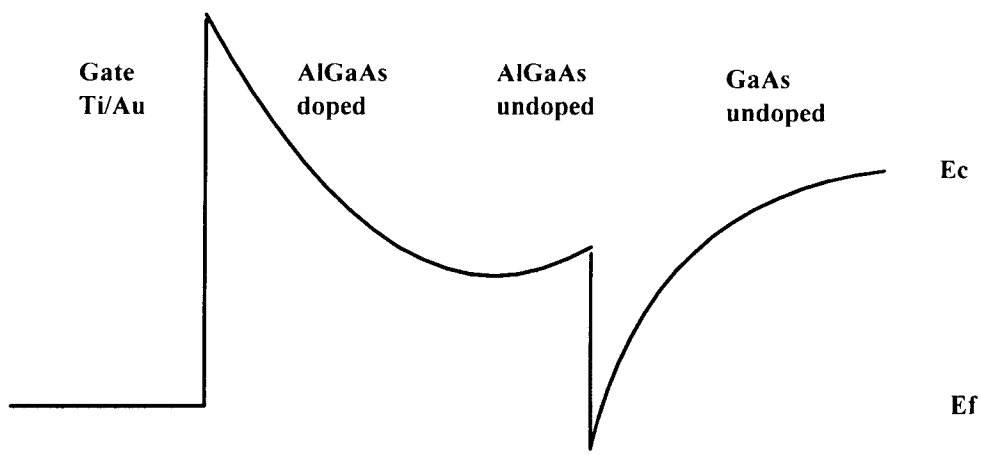

Figure 2.2 Energy band diagram of typical uniformly doped GaAs/AlGaAs structure.

2.2 Pseudomorphic InGaAs/AlGaAs HFET

InGaAs/AlGaAs pseudomorphic structures also have greater carrier confinement due to the greater band offset in the InGaAs/AlGaAs structures as compared to the standard GaAs/AlGaAs structures [13]. The typical layers of the InGaAs/AlGaAs pseudomorphic structure are shown in figure 2.3. In this structure, an unintentionally doped GaAs buffer is grown on a semi-insulating GaAs substrate, followed by a thin layer of narrow bandgap InGaAs grown pseudomorphically on the GaAs. The heterojunction is formed with an undoped $Al_XGa_{1-X}As$ spacer layer followed by a doped (Si or Be) AlGaAs barrier layer and capped with a doped GaAs layer.

Pseudomorphic InGaAs/AlGaAs Heterostructure

GaAs --doped--	**Cap**
AlGaAs --doped--	**Barrier**
AlGaAs --undoped--	**Spacer**
InGaAs --undoped--	**Quantum Well**
GaAs --undoped--	**Buffer**
GaAs --semi-insulating--	**Substrate**

Figure 2.3. Layer structure of uniformly doped pseudomorphic InGaAs/AlGaAs heterostructure.

A characteristic energy band diagram for a typical pseudomorphic structure is shown in figure 2.4. Carriers in this structure are confined in a quantum well formed by the AlGaAs/InGaAs/GaAs systems.

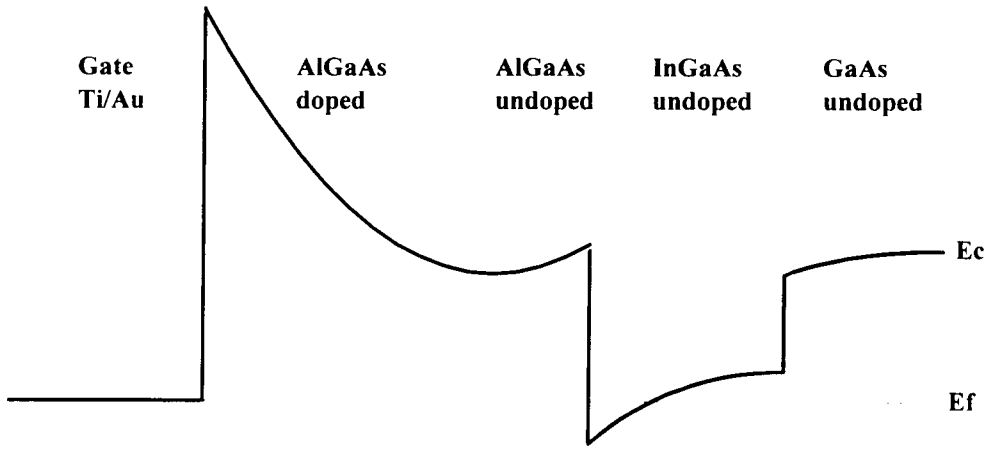

Figure 2.4. Energy band diagram of a typical uniformly doped pseudomorphic InGaAs/AlGaAs structure.

2.3 Delta Doping Profiles

Delta doping uses a very narrow width of highly doped AlGaAs which serves as the source of the carriers in the device. Ideally, a doped pulse is a partial monolayer of dopant atoms in a plane yielding a doping profile which approximates a delta function. Delta doped MODFET's provide improved channel confinement, reduced parallel conduction at high gate voltages and reduced peak electric field, which leads to higher channel density and higher channel drift velocities [14]. These structures also exhibit reduced trapping effects, improved threshold voltage control and high breakdown characteristics. In addition, this doping technique improves charge transfer to the active region of the devices and reduces charge accumulation in the low mobility AlGaAs

barrier region. The reduction of excess charge in the barrier region is especially important to the design of high quality p-channel devices. The advantages of delta-doped MODFETs are manifested in higher transconductances and improved current drive capabilities at a wider range of gate biases as compared to standard uniformly doped structures.

To achieve the delta layer in the epitaxial growth, the growth is stopped by shuttering off the group III (gallium and aluminum) ovens and opening the dopant shutter to deposit a fractional monolayer of dopant atoms while maintaining an arsenic background flux. The dopant sources are typically silicon (Si) or beryllium (Be) for n- or p-type semiconductors, respectively. Silicon is a group IV atom, predominately substituting gallium (Ga) sites, thereby making it a donor atom. Beryllium is a group II double acceptor atom. However, beryllium is difficult to confine in a delta plane due to its relatively small atomic size (which leads to a high diffusivity). Therefore, it is desirable to find an alternative p-type dopant which has a lower diffusivity. One such dopant is carbon.

2.4 Carbon Doping Profiles

The need for a stable (non-diffusing) acceptor at high doping levels in heterostructures has generated much interest in the use of carbon as an acceptor impurity in GaAs. Currently, the most widely used acceptor dopant in GaAs is beryllium . However, at high doping levels, beryllium exhibits surface segregation, significant diffusion and self compensation [15].

As an unintentional doping source, carbon is sometimes regarded as a problem in GaAs. High background levels can degrade electron mobility through ionized impurity scattering and result in thermal conversion of semi-insulating substrates to p-type after annealing [16]. Used as an intentional dopant, carbon has an extremely low diffusion

coefficient at the highest doping levels in GaAs. This indicates that carbon doping may be an attractive substitute for beryllium doping in GaAs.

Carbon-doping is accomplished using a gas source of carbon techtrabromine (CBr_4). Using constant pressure through a precision leak valve, CBr_4 is introduced at the GaAs surface where it is 'cracked' into elemental carbon and CBr_2. The elemental carbon predominately substitutes arsenic sites, thereby making it an acceptor. Several carbon doped structures were fabricated here at Oregon State University in an attempt to further improve the performance on the p-channel devices as discussed later.

2.5 Dipole Layers

A serious limitation with HFETs is the gate current through the Schottky diode gate. The diode, shown in figure 1.4 as D_{gs} and D_{gd}, has a high resistance under reverse bias (above the turn on voltage) and a low resistance under forward bias. Gate leakage is due to conduction through these diodes under small forward biases. The gate leakage current effectively decreases the drain current and effectively reduces the device transconductance and speed.

In p-channel structures, there is a lower barrier confinement height than in n-channel structures due to a smaller valence-band discontinuity at the heterointerface. The lower barrier confinement height results in conduction (gate leakage) through the AlGaAs barrier layer under smaller forward biases.

However, gate leakage may be minimized by increasing the effective Schottky-barrier height at the heterointerface using a so called 'dipole layer' [17, 18]. In an n-channel device, a dipole is formed using two pulsed doped planes, n^{++} and p^{++}, in the barrier layer. The additional p-type doping in the vicinity of the gate contact increases the effective Schottky barrier height. The p-channel structure is similar except the doping

planes are reversed. Several dipole HFETs were fabricated in an attempt to further improve device performance discussed later in section 4.3.

2.6 Complementary HFET Structures

There are several methods of realizing n- and p-channel devices together in HFET technology. One is to use a self aligned process in which ion implantation is used to define the source and drain regions on each side of an existing gate metallization, thereby minimizing the source-to- and drain-to-gate spacings [19]. This has the advantage of reduced parasitic resistances associated with the source-to- and drain-to-gate spacings. However, due to the limited availability of ion implantation, a non-planar recess etch process was used here.

Shown in figure 2.5 is a typical C-HFET structure, grown for the present work, consisting of a delta doped GaAs/AlGaAs p-channel structure stacked on a n-channel structure. The p-channel structure is delta doped with beryllium, while the n-channel structure is delta doped with silicon. The two structures are separated by approximately 500Å of intrinsic 50 percent AlGaAs. The separation layer serves as a stop etch layer for selectively etching away the p-channel structure in order to reveal the n-channel structure. Using a citric etch to selectively etch GaAs from AlGaAs, and HF to selectively etch AlGaAs from GaAs, the n-channel structure is revealed by etching away the p-channel structure layer by layer (see chapter 3).

The corresponding complementary pseudomorphic structure is shown in figure 2.6. This structure is similar to the previous one with the exception of the InGaAs layer sandwiched between the delta doped AlGaAs and the undoped GaAs active layer.

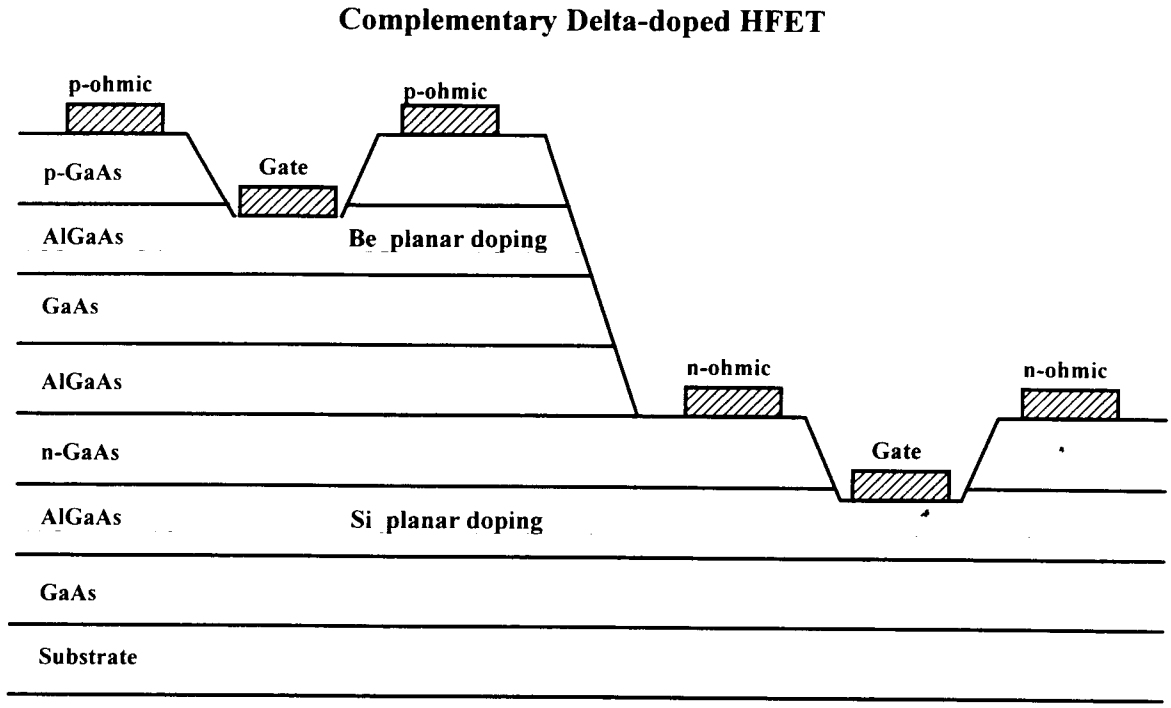

Figure 2.5. Cross section of a complementary delta-doped HFET structure.

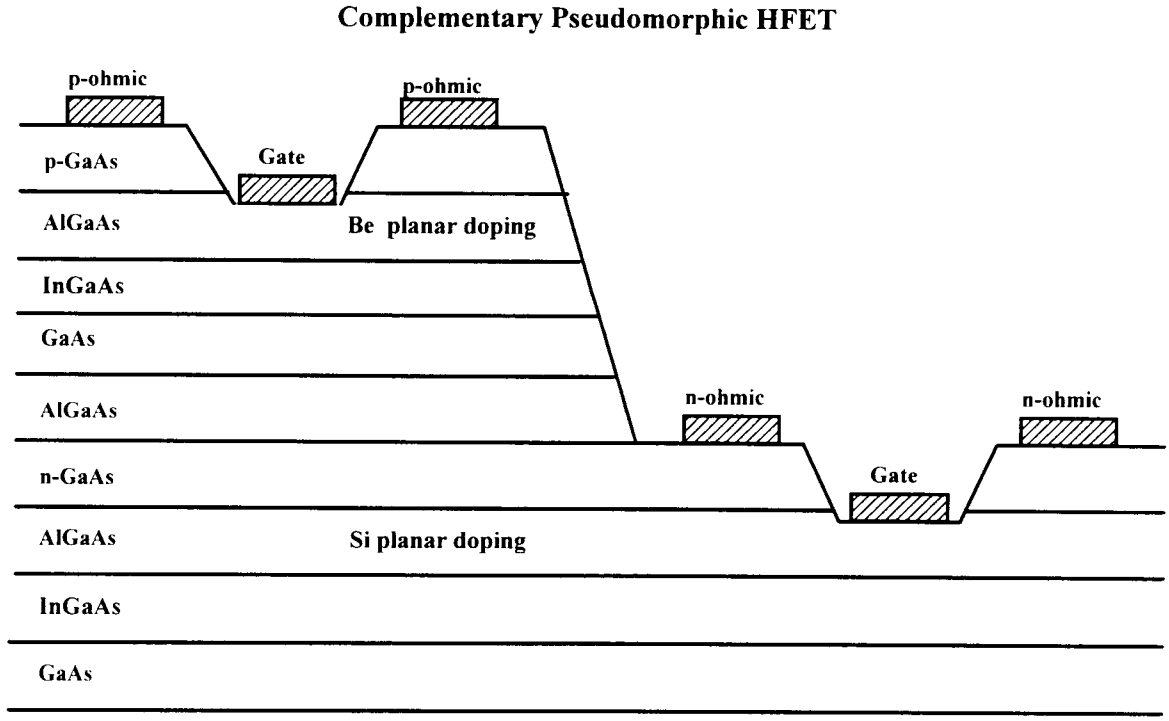

Figure 2.6. Cross section of a complementary pseudomorphic HFET structure.

3. Process Design and Fabrication

An understanding of the process technology and heterostructures applied in the HFET and CHFET used here were summarized in the previous chapter. This chapter overviews the procedure developed for processing material into working devices. The discussion begins with some of the process design issues that effect overall performance. Following this, the experimental techniques are explained to give insight into the fabrication process followed by details of processing steps involved in fabricating devices. Finally, a discussion on the layout of the photomask set is presented.

3.1 Process Design

Some of the primary limiting factors in CHFET device performance are poor ohmic contacts, low Schottky barrier heights, large series resistances and parasitic capacitances. Poor ohmic contacts contribute large resistances, which are detrimental to device performance. Substrate leakage also tends to be a problem, and degrades the device performance, as does gate leakage. All of these effects are material and fabrication dependent. Thus, the desired goal is to minimize these effects when designing a process for fabrication of CHFET structures without degrading the intrinsic device behavior.

Parasitic resistances and capacitances reduce the device performance, and directly relate to device geometry. Large source-to- and drain-to-gate spacings contribute high series resistance and limit the external transconductance. Capacitive coupling between the source-to- and drain-to-gate regions reduces overall device performance. To reduce these parasitic elements, it is necessary to minimize the source-to- and drain-to-gate regions and maximize the spacing between the source-to- and drain-to-gate pads.

The selection of a contact-metal system for ohmic contact to GaAs has several requirements [20]. The most important of these is that the GaAs must be doped by the metal system to produce a degenerate surface layer. Others important factors are that the metal systems have good electrical and thermal characteristics, good adherence, no interface reaction, ambient environment inertness, and a convenient alloying temperature. For the n-type contact, a metallization of Ni/AuGe/Au (a eutectic alloy of 88% Au and 12% Ge) was used in the course of this research. Nickel was used as a wetting agent and to aid in the diffusion of the dopant, germanium, into the GaAs. For the p-type contacts, a metallization of Ti/Zn/Au was used. Zinc is the p-type dopant, while the titanium served as a wetting agent to obtain better adherence to the GaAs. Both metal-contact systems were thermally evaporated.

On GaAs the fermi-level is 'pinned' by intrinsic interface states. The Schottky barrier height is independent of the metal-contact system used due to this pinning. However, it is important that the metal-contact system used have good electrical behavior, good adherence, no interface reaction, ambient environment inertness and rectifying behavior. The Schottky gates were formed by thermally evaporating a refractory metallization of titanium and gold.

3.2 Fabrication

The fabrication process entails preliminary sample preparation and several photolithographic steps involving wet etching and liftoff techniques. Device fabrication was implemented in-house at Oregon State University using the clean room facilities. These facilities include a MBE system, projection mask aligner with a 2μ resolution, thermal evaporator, thermal annealing furnace and plasma-enhanced chemical vapor deposition (PECVD) system.

3.2.1 Sample preparation

Lithography was done on a Canon projection aligner set up for 2" wafers. To conserve on material and cost, it was necessary to first cleave the MBE grown material into samples approximately 1cm by 1 cm. Most of the material was mounted on the growing blocks with indium solder. Originally, the cleaved samples were mounted on 2" silicon wafers with indium solder to accommodate the aligner. However, this idea was abandoned because the samples could not be mounted flat enough for proper focusing with the mask aligner. Instead, a 2" wafer chuck with a recess to accommodate a 1cm by 1 cm sample was manufactured for the mask aligner to eliminate the flatness problem. However, in order to use this special wafer chuck, it was necessary to remove the solder from the backside of the material. This removal involved mounting the layered structure side of the material to a polishing block with 'crystal bond' and polishing indium off the backside of the material. The procedure often slightly damaged the surface of the material, but it was still a more desirable result than a tilted surface. This problem was later overcome by growing the epi-layers on solderless blocks.

3.2.2 Lithography

Basically, there are two types of lithography techniques used in processing: a liftoff process and a wet etching process. Both techniques are based on the process of applying photoresist to the sample and patterning the resist by imaging a mask pattern on the surface using ultraviolet light. It is necessary for the sample to be coated with an even layer of photoresist when using either lithography technique. Variations in the thickness of the photoresist results in inconsistencies between devices across the processed sample. Therefore, a uniform coat of photoresist is applied to the sample by spinning the sample on its center axis. If the resist is correctly applied, minimal defraction rings in the

photoresist across the sample can be observed, with exceptions along the edges and in the corners of the coated sample.

3.2.3 Liftoff technique

The liftoff technique is used to define metallization patterns on the sample. It is used in the current MODFET process to define the ohmic, gate and bonding pad metals. To begin, resist is applied to the sample and is patterned by exposure through a mask. The sample is then soaked in chlorobenzene to harden the upper-most layer of the resist. This hardened layer undercuts in the developer less than the resist which lies beneath it, and a protruding top edge profile is obtained during development. Metal is applied to the surface of the sample using thermal evaporation. Acetone is used to dissolve the resist, and the metal which lies on top of the resist is 'lifted off' of the sample, leaving behind only the metal in contact with the sample's surface (see figure 3.1). The liftoff technique is sensitive to the edge profile of the patterned resist. Therefore, without a proper undercutting edge profile, the solvent may be unable to dissolve all of the resist and liftoff will not occur.

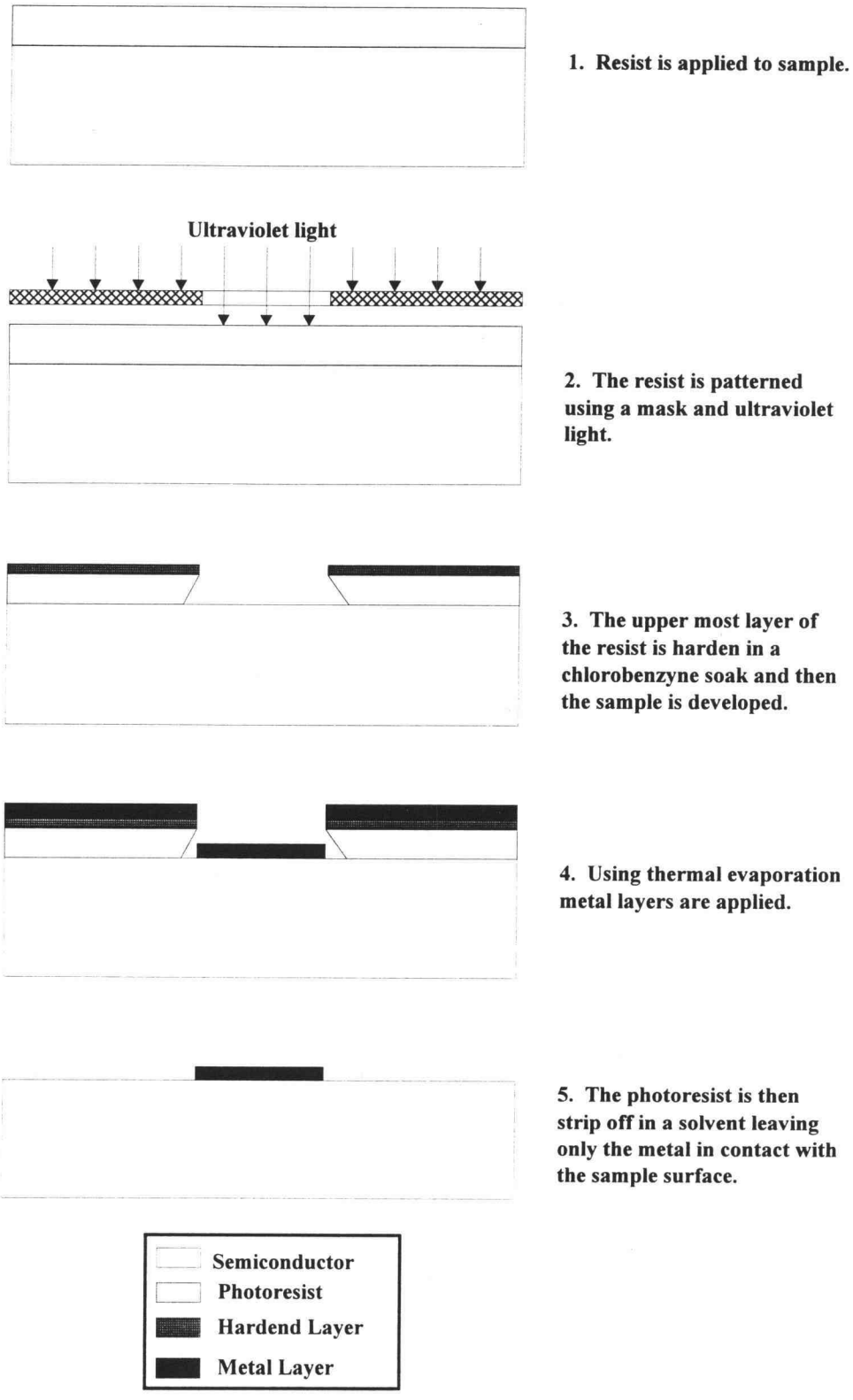

Figure 3.1. Typical liftoff procedure.

3.2.4 Wet Etching

For the MODFET process, wet etching is used to define the mesa and gate recess, and to open windows in SiO_2. Wet etching is a technique in which material is removed using a liquid etchant (see appendix for list of etches). To begin, resist is applied to the sample, patterned by exposure through a mask and then developed. All of the exposed area is etched away when immersed in the etchant. The resist is then stripped away and only the desired pattern remains (see figure 3.2).

Most wet etchants operate by first oxidizing a semiconductor surface and then dissolving the oxide in an acid, which results in the removal of material. Basically, the dissolution rate of the material is either reaction limited or diffusion limited.

When the dominant etching mechanism is reaction limited, the dissolution of material is limited by the rate at which chemical reactions take place on the surface of the material. Reaction limited etches have the following characteristics:

i) Etch rate is linearly dependent with the etching time.
ii) Etch rate is unaffected by stirring or agitation.
iii) Etch rate is temperature dependent (typically etch rate $\propto e^{-1/T}$).
iv) Small changes in proportion of etchant components result in large changes in etch time.
v) Etchant gives faceted surface structure characteristic of the materials crystal properties.

For diffusion limited etching, the dissolution rate of the material is controlled by the rate at which reaction products can be removed from the surface or the rate at which active etching components are transported to the surface. Diffusion limited etches have the following characteristics:

i) Etch rate is proportional to the square root of the etching time.
ii) Etch rate increases with stirring or agitation.
iii) Etch rate is relatively unaffected by temperature variations.
v) Etching is isotropic with respect to crystal orientation.

All etches used in the in-house MODFET process are reaction limited etches. Before wet etching a sample, a calibration of the etchant is required to obtain the etch rate. For reaction limited etches, the etch rate is calculated by the following:

$$\text{Etch Rate (um/min)} = \frac{\text{Thickness of material removed (um)}}{\text{Etch time (min)}} \qquad (3.1)$$

A selective etch removes one material faster than another. Therefore, for etches such as the citric etch, the selectivity of the etchant is an important consideration. The selectivity is given by the following:

$$\text{Selectivity} = \frac{\text{Etch Rate of material 1}}{\text{Etch Rate of material 2}} \qquad (3.2)$$

The calibration is performed by etching on several pieces of the material and varying the time in the etchant between pieces. An etch rate is obtained by taking a global average of the relationship given above.

However, several ambient conditions can effect the calibration. The temperature of the etch, the light, and surface contamination such as oxides should be considered when performing a calibration or an etch on a sample. Often, an oxide etch of 1 part ammonia hydroxide to 3 parts deionized water is used prior to any etching or liftoff procedure to remove surface oxides.

It is recommended that etchants be replaced regularly and discarded soon after use. Hydrogen peroxide based etches tend to degenerate quickly and should be mixed fresh as needed.

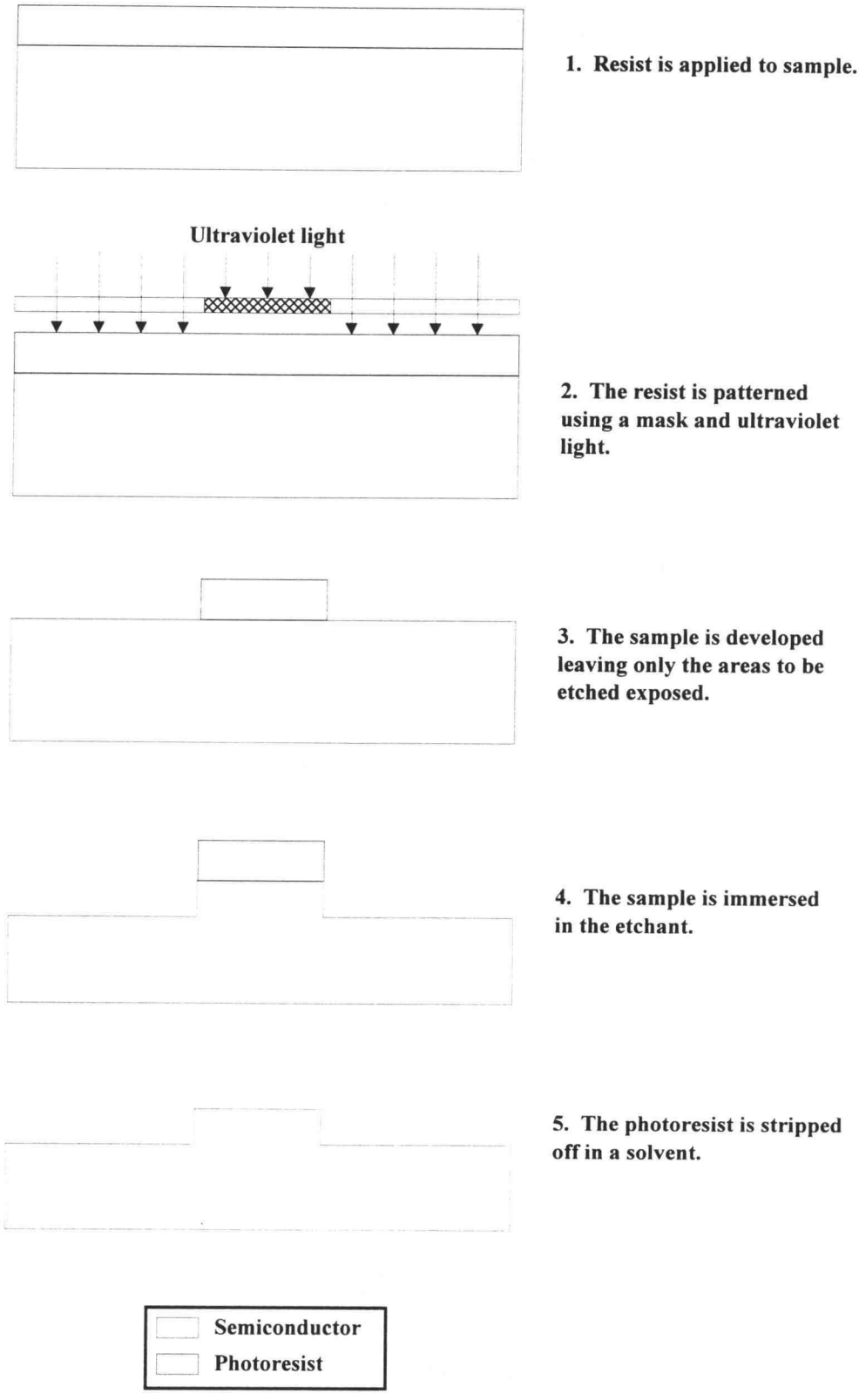

Figure 3.2. Typical wet etching technique.

3.3 Typical Process

Currently, n- and p-channel devices, and CHFET circuits have been fabricated on the same substrate. Described hereafter in detail is the current in-house process for fabrication of CHFET structures. The procedure requires 10 photolithographic mask levels consisting of several liftoff and wetting etching procedures.

3.3.1 Level 1: n-material Reveal

The n-material reveal patterns are used to define the regions of the n-channel devices. Using citric acid and hydrofluoric acid (HF) etchants, the GaAs, InGaAs and AlGaAs layers of the p-channel material can be selectively removed to reveal the n-channel material in the stacked structure. Using the wet etching techniques mentioned earlier, the procedure is as follows:

1.) Clean the sample in acetone, methanol, deionized water and N_2 dry.

2.) Center the sample on spinner, apply photoresist and spin @ 5000 rpm for 30 seconds.

3.) Soft Bake 5 minutes @ 85C to remove solvents.

4.) Following alignment the resist is exposed through the mask with ultraviolet light at setting 9.5 on the projection aligner.

5.) Develop sample in developer.

6.) Soft Bake 5 minutes @ 120C to remove any remaining solvents.

7.) Dip sample in NH_4OH:H_2O Mix 1:3 for 20 seconds to remove any surface oxides and rinse with deionized water.

8.) Etch sample in citric acid:H_2O_2 10:1 for 20 seconds to remove p-channel cap layer and rinse in deionized water.

9.) Etch sample in 45% HF for 10 seconds to remove p-channel AlGaAs barrier and spacer layer and rinse in deionized water.

10.) Etch sample in citric acid:H_2O_2 10:1 for 60 seconds to remove p-channel InGaAs active region and/or GaAs buffer layer thus exposing the n-channel cap layer, then rinse in deionized water.

11.) Clean the sample in acetone, methanol, deionized water and N_2 dry.

3.3.2 Level 2: n-ohmic Contact Metallization

The ohmic metallization patterns the source and drain regions of the n-channel devices. Applying the liftoff technique mention earlier, the procedure is as follows:

1.) Clean the sample in acetone, methanol, deionized water and N_2 dry.

2.) Center the sample on spinner, apply photoresist and spin @ 5000 rpm for 30 seconds.

3.) Soft bake the sample for 25 minutes @ 85C to remove solvents from resist and to enhance surface adhesion.

4.) Following alignment the resist is exposed through the mask with ultraviolet light at setting 9.5 on the projection aligner.

5.) Soak sample in a chlorobenzene solution for 5 minutes to harden upper layer of resist.

6.) Develop sample in developer.

7.) Soft Bake 5 minutes @ 85C to remove any remaining solvents.

8.) Dip sample in NH_4OH:H_2O Mix 1:3 for 20 seconds to remove any surface oxides and rinse with deionized water.

9.) Evaporation of ohmic metals:
n-type ohmics: 100Å Ni/500Å AuGe/1500Å Au.

10.) Place sample in acetone to liftoff excess metals, rinse with methanol, deionized water and N_2 dry.

3.3.3 Level 3: p-ohmic Contact Metallization

The ohmic metallization patterns the source and drain regions of the p-channel devices. The metallization is applied and then alloyed to provide low resistance contact to the channel of the device. Both n- and p-ohmics are alloyed simultaneously and for the same time interval using the procedure as follows:

1.) Clean the sample in acetone, methanol, deionized water and N_2 dry.

2.) Center the sample on spinner, apply photoresist and spin @ 5000 rpm for 30 seconds.

3.) Soft bake the sample for 25 minutes @ 85C to remove solvents from resist and to enhance surface adhesion.

4.) Following alignment the resist is exposed through the mask with ultraviolet light at setting 9.5 on the projection aligner.

5.) Soak sample in a chlorobenzene solution for 5 minutes to harden upper layer of resist.

6.) Develop sample in developer.

7.) Soft Bake 5 minutes @ 85C to remove any remaining solvents.

8.) Dip sample in $NH_4OH:H_2O$ Mix 1:3 for 20 seconds to remove any surface oxides and rinse with deionized water.

9.) Evaporation of ohmic metals:
p-type material-100Å Ti/150Å Au/500Å Zn/1500Å Au.

10.) Place sample in acetone to liftoff excess metals, rinse with methanol, deionized water and N_2 dry.

11.) Anneal ohmics in forming gas:

4.5 minutes @ 450C

12.) Dip sample in $NH_4OH:H_2O$ Mix 1:3 for 20 seconds to remove surface oxides and rinse in deionized water.

13.) Measure contact resistance of test patterns. Continue processing the sample if the contact resistance is acceptable.

3.3.4 Level 4: Mesa Isolation

The mesa isolation electrically isolates one device from another. This involves etching away regions of the active layer, leaving only mesas of active layer in desired locations. The mesa is patterned by using an ammonia hydroxide based etch and using the wet etching technique mentioned earlier. The procedure is as follows:

1.) Clean the sample in acetone, methanol, deionized water and N_2 dry.

2.) Center the sample on spinner, apply photoresist and spin @ 5000 rpm for 30 seconds.

3.) Soft Bake 5 minutes @ 85C to remove solvents.

4.) Following alignment the resist is exposed through the mask with ultraviolet light at setting 9.5 on the projection aligner.

5.) Develop sample in developer.

6.) Soft Bake 5 minutes @ 120C to remove any remaining solvents.

7.) Etch sample in $NH_4OH:H_2O_2:H_2O$ Mix 2:1:100 for 60 seconds and rinse in deionized water.

8.) Clean the sample in acetone, methanol, deionized water and N_2 dry.

9.) Use the Alpha-stepper surface profiler to confirm the depth of the etch is sufficient for isolation.

3.3.5 Levels 5 and 6: Gate recess and metallization

The gate, which modulates the charge in the channel, is defined between the region of the source and drain of the device. The procedure for the n- and p-channel gate recess and metallization is identical with the exception of the composition of the citric etchant. First, an opening is defined in the GaAs cap using a citric etchant mixed according to barrier layer composition of Al. Then, using metal evaporation, the gate is deposited in the recess on top of the AlGaAs barrier layer. The undercutting effect of the citric etch ensures the gate metal is not in contact with the GaAs cap. However, this is not a true gate recess since only the cap is removed. Wet etching is difficult to control when trying to recess a short distance through a layer of material. Therefore, only selective etching is done between the GaAs cap and the AlGaAs spacer. The wet etching procedure is as follows:

1.) Clean the sample in acetone, methanol, deionized water and N_2 dry.

2.) Center the sample on spinner, apply photoresist and spin @ 5000 rpm for 30 seconds.

3.) Soft bake the sample for 25 minutes @ 85C to remove solvents from resist and to enhance surface adhesion.

4.) Following alignment the resist is exposed through the gate metallization mask with ultraviolet light at setting 10 mask aligner.

5.) Soak sample in a chlorobenzene solution for 5 minutes to harden upper layer of resist.

6.) Develop sample in developer.

7.) Soft Bake 5 minutes @ 85C to remove any remaining solvents.

8.) Dip sample in NH_4OH:H_2O Mix 1:3 for 20 seconds to remove any surface oxides and rinse with deionized water.

9.) Etch GaAs cap off in Citric Acid:H_2O_2
--2:1 ratio to selectively etch GaAs from $Al_XGa_{1-X}As$ x = 0.27
--10:1 ratio selectively etch GaAs from $Al_XGa_{1-X}As$ x = 0.5

10.) Evaporation of gate metal:
500Å Ti and 500Å Au

11.) Place sample in acetone to liftoff excess metals, rinse with methanol, deionized water and N_2 dry.

3.3.6 Level 7: First Level Passivation

The passivation layer protects the surfaces of the material from chemical and physical abuse. The silicon dioxide (SiO_2) is deposited using PECVD. Using a dilute solution of buffered hydrofluoric acid, the SiO_2 windows are defined through the SiO_2 to allow the interconnects to contact the ohmic pads and gate metallizations. The procedure is as follows:

1.) Using CVD, deposit 1000 Å SiO_2 to the surface of the sample.

2.) Clean the sample in acetone, methanol, deionized water and N_2 dry.

3.) Center the sample on spinner, apply HMDS/photoresist and spin @ 5000 rpm for 30 seconds (the HMDS allows the photoresist to adhere to the SiO_2).

4.) Soft Bake 5 minutes @ 85C to remove solvents.

5.) Following alignment the resist is exposed through the mask with ultraviolet light at setting 9.5 on the projection aligner.

6.) Develop sample in developer.

7.) Soft Bake 5 minutes @ 120C to remove any remaining solvents.

8.) Etch sample in buffered $HF:H_2O$ Mix 1:10 approximately 60 seconds and rinse with deionized water.

9.) Clean the sample in acetone, methanol, deionized water and N_2 dry.

3.3.7 Level 8: Interconnects Metallization

This level defines the connections from the gate or ohmics to the bonding pads of the devices and circuits. A metallization of titanium and gold is patterned on the surface of the first passivation layer. The procedure is as follows:

1.) Clean the sample in acetone, methanol, deionized water and N_2 dry.

2.) Center the sample on spinner, apply HMDS/photoresist and spin @ 5000 rpm for 30 seconds (the HMDS allows the photoresist to adhere to the SiO_2).

3.) Soft bake the sample for 25 minutes @ 85C to remove solvents from resist and to enhance surface adhesion.

4.) Following alignment the resist is exposed through the mask with ultraviolet light at setting 9.5 on the projection aligner.

5.) Soak sample in a chlorobenzene solution for 5 minutes to harden upper layer of resist.

6.) Develop sample in developer.

7.) Soft Bake 5 minutes @ 85C to remove any remaining solvents.

8.) Dip sample in $NH_4OH:H_2O$ Mix 1:3 for 20 seconds to remove any surface oxide and rinse with deionized water.

9.) Evaporation of bonding pad metals:
500Å Ti/1500Å Au.

10.) Place sample in acetone to liftoff excess metals, rinse with methanol, deionized water and N_2 dry.

3.3.8 Level 9: Second Level Passivation

In some of the circuits or devices, bridges over previous metallizations are necessary (i.e. connecting the sources together of a 6 gate RF transistor.) The second passivation layer isolates the first interconnect metallization from the second in order to form these bridges. The SiO_2 is deposited using PECVD. Using a dilute solution of buffered hydroflouric acid, the SiO_2 windows are defined through the SiO_2 to allow the final metallization to interconnect any remaining devices or circuits (i.e. multiply sources on an RF transistor), and to allow the bonding pads to contact the first metallization. The procedure is as follows:

1.) Using CVD, deposit 1000 Å SiO_2 to the surface of the sample.

2.) Clean the sample in acetone, methanol, deionized water and N_2 dry.

3.) Center the sample on spinner, apply HMDS/photoresist and spin @ 5000 rpm for 30 seconds (the HMDS allows the photoresist to adhere to the SiO_2).

4.) Soft Bake 5 minutes @ 85C to remove solvents.

5.) Following alignment the resist is exposed through the mask with ultraviolet light at setting 9.5 on the projection aligner.

6.) Develop sample in developer.

7.) Soft Bake 5 minutes @ 120C to remove any remaining solvents.

8.) Etch sample in buffered HF:H_2O Mix 1:10 approximately 60 seconds and rinse with deionized water.

9.) Clean the sample in acetone, methanol, deionized water and N_2 dry.

3.3.9 Level 10: Bonding Pads Metallization

This level defines the bonding pads and interconnect bridges of the devices and circuits. A metallization of titanium and gold is patterned on the surface of the passivation layer, typically of dimensions 100μ by 100μ, in order to probe the devices or wire bond the devices into a package. The procedure is as follows:

1.) Clean the sample in acetone, methanol, deionized water and N_2 dry.

2.) Center the sample on spinner, apply HMDS/photoresist and spin @ 5000 rpm for 30 seconds (the HMDS allows the photoresist to adhere to the SiO_2).

3.) Soft bake the sample for 25 minutes @ 85C to remove solvents from resist and to enhance surface adhesion.

4.) Following alignment the resist is exposed through the mask with ultraviolet light at setting 9.5 on the projection aligner.

5.) Soak sample in a chlorobenzene solution for 5 minutes to harden upper layer of resist.

6.) Develop sample in developer.

7.) Soft Bake 5 minutes @ 85C to remove any remaining solvents.

8.) Dip sample in $NH_4OH:H_2O$ Mix 1:3 for 20 seconds to remove any surface oxide and rinse with deionized water.

9.) Evaporation of bonding pad metals: 500Å Ti/1500Å Au.

10.) Place sample in acetone to liftoff excess metals, rinse with methanol, deionized water and N_2 dry.

3.4 Layout of Test Structures and Devices

While maintaining a general understanding of the epi-layer structure involved, the desired device performance, and the limiting factors involved with device geometries mentioned above, devices and testing structures were produced on a photomask set. These include:

i) Transmission Line Measurement (TLM) structures.
ii) RF transistors with multiple gate lengths and gate-to-source spacings.
iii) DC characterization MODFET's with multiply gate lengths and gate-to- source spacings.
iv) Van der Pauw Structures.
v) Hall Bars.
vi) Interconnect Integrity Structures.
vii) FatFET.

Also included in the photomask set were several circuits. These include:

i) Invertors (3 different configurations).
ii) Current sources (2 different configurations).
iii) Gain stage.
iv) Ring oscillator.

Using Mentor Graphics Tools on an Apollo workstation, a photomask set was laid out in collaboration with Don W. Schulte. Du Pont Photomask produced the photomask set using the graphics files created here. Actual structures fabricated in the course of this research using the photomask set are shown in figures 3.3 through 3.8.

To characterize the individual device characteristics, an array of dc testing transistors were developed with gate-source spacings of 1.5, 2.0, 3.0 and 4.0μ and gate lengths of 1.5, 2.0, 3.0, 4.0 and 5.0μ (see figure 3.3). The special alignment marks used in aligning the gate metalization are shown in the upper corners of this figure. To characterize the RF characteristics, a set of 2-, 4- and 6-fingered RF transistors were developed with gate-source spacings of 1.5, 2.0 and 3.0μ and gate lengths of 1.5, 2.0 and 3.0μ (see figure 3.4). The layout of these transistors were such that to accomodate 3 mil

high precision HP cascade microprobes. Also included in this section of the layout are a thru and short calibration standard used in calibration of the HP8510 Network Analyzer.

Characterization and testing structures are shown in figure 3.5. A Hall bar and Van der Pauw structure were developed for low temperature material characterizations. A TLM structure was developed to evaluate the ohmic contacts. Also shown in this figure are a few structures used to aid in the fabrication process. These include a gate recess structure which is used in conjunction with a surface profiler to measure the depth of the gate recess and a structure consisting of long interconnect lines running over mesas of various spacings used to determine the interconnect integrity.

The circuits were layed out in two different forms. First, an 11-stage ring oscillator, a gain stage, two different current sources and three different invertor configurations were combined to accomodate a 27 pin lead package as shown in figure 3.6. In this form several circuits could be packaged for evaluation in one lead frame. The other form consisted of the same circuits laid out individually as shown in figure 3.7. Also shown in this figure are the alignment marks that aid in the alignment of mask levels as well as define the cleaving planes for separating the devices and circuits for packaging.

The layout of all the devices and circuits is shown in figure 3.8. In the first column of this figure are the n-channel devices and in the second column are the p-channel devices. The complementary circuits shown in the lower half of the figure are identical in either column. The entire layout consisted of 2 sets of what is shown in figure 3.8.

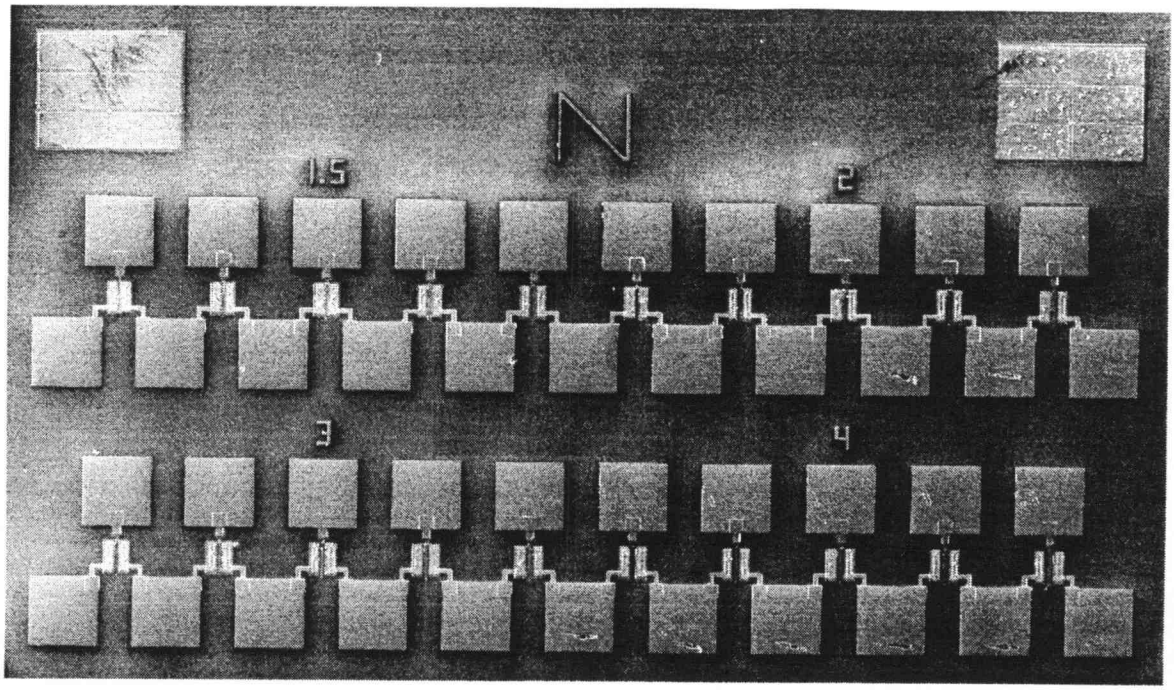

Figure 3.3. A SEM image of the DC array test structure. Gate lengths are 1.5, 2.0, 3.0, 4.0 and 5.0μ and gate-source spacings are 1.5, 2.0, 3.0 and 4.0μ. Bonding pads are of dimensions 100μ x 100μ.

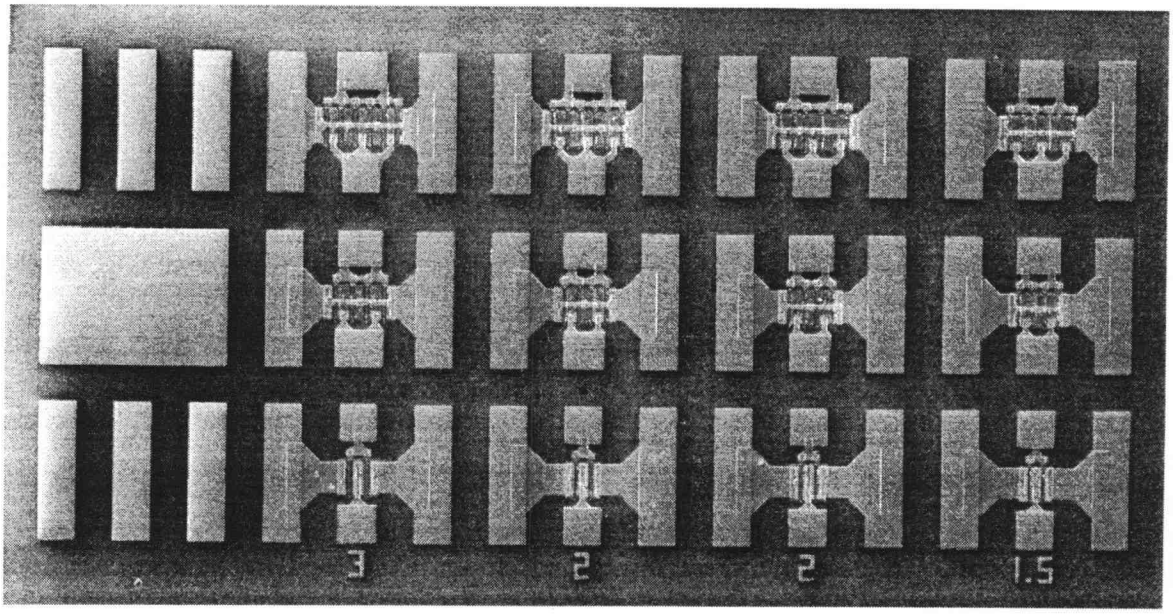

Figure 3.4. A SEM image of the RF array test structure. Gate lengths are 1.5, 2.0 and 3.0μ and gate-source spacings are 1.5, 2.0 and 3.0μ. 3 mil pitch calibration standards (right), 6-finger RF (top row), 4-finger RF (center row) and 2-finger RF (bottom row).

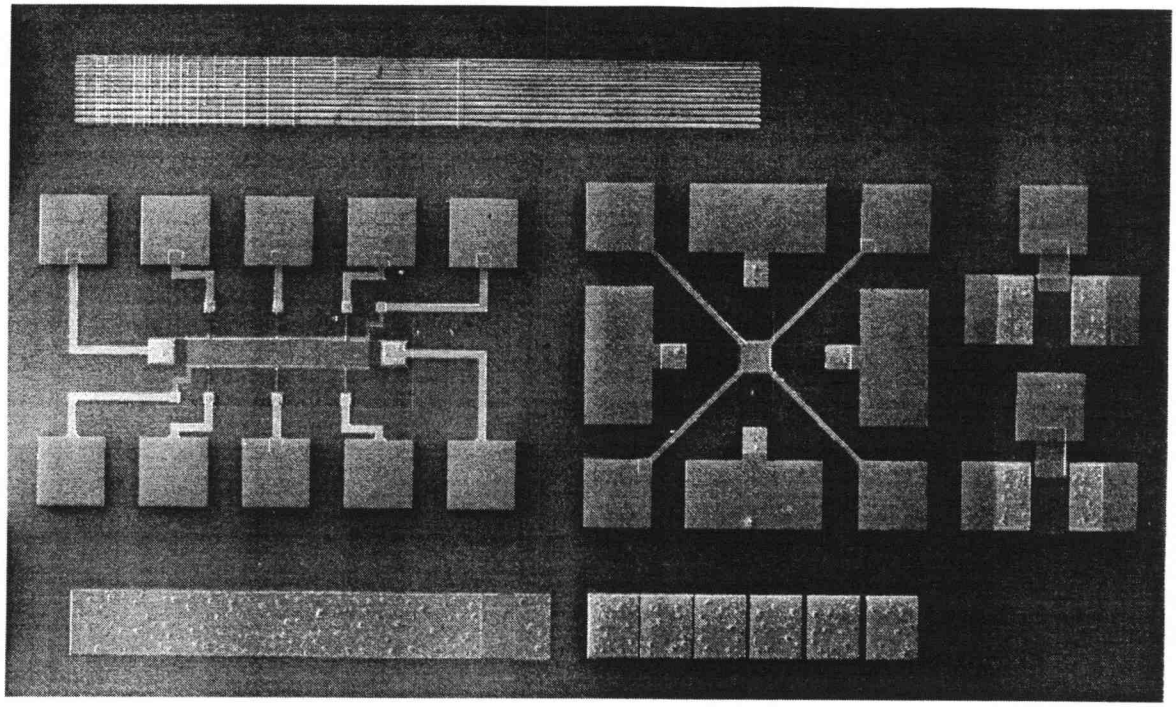

Figure 3.5. A SEM image of characterization and test structures. Interconnect integrity structure (top), Hall Bar structure (center left), Van der Pauw strucuture (center), FAT-FET (center right), Gate Recess Test structure (bottom left) and TLM structure (bottom right).

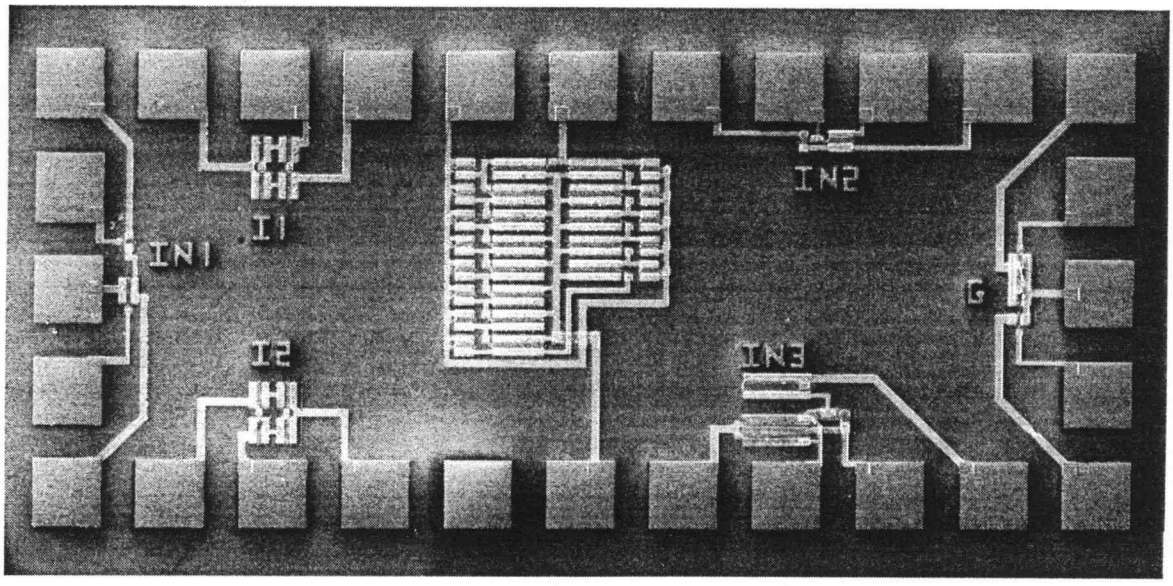

Figure 3.6. A SEM image of individual circuits set up for a 27 pin lead package. An 11-stage ring oscillator (center), two current source configurations (above and below right), a gain stage (center right) and three invertor configurations (left). Bonding pads are of dimensions 100μ x 100μ.

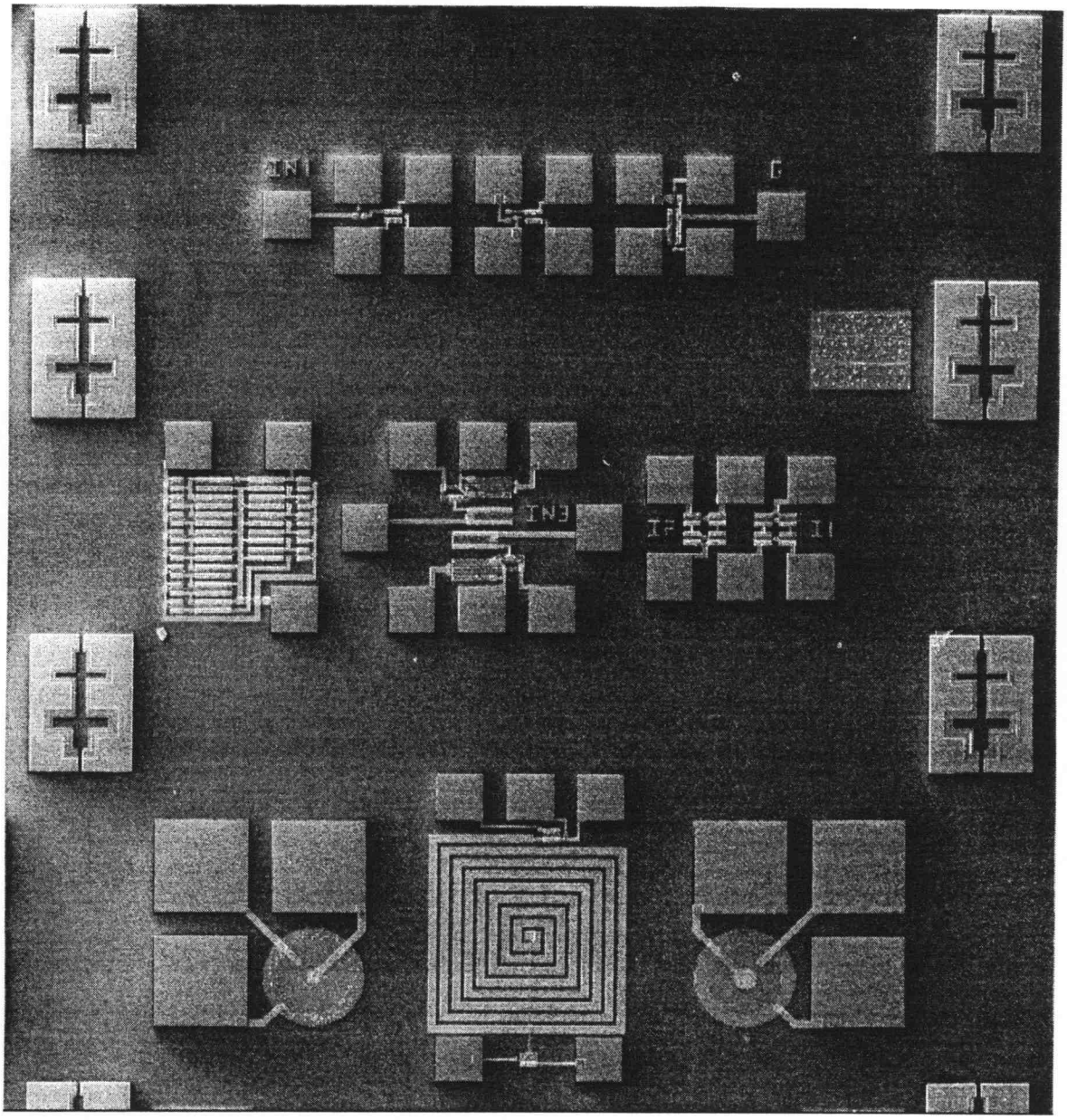

Figure 3.7. A SEM image of Individual circuits. Alignment marks aid in the alignment of mask levels as well define the cleaving planes for separating the devices and circuits for packaging. Invertor1 (top left), Invertor2 (top center), Gain Stage (top right), 11-stage Ring Oscillator (center left), Invertor3 (center), Current Source 1 and 2 (center left), n-channel Corbino Disk (bottom left), Inductor (bottom center) and p-channel Corbino Disk (bottom right).

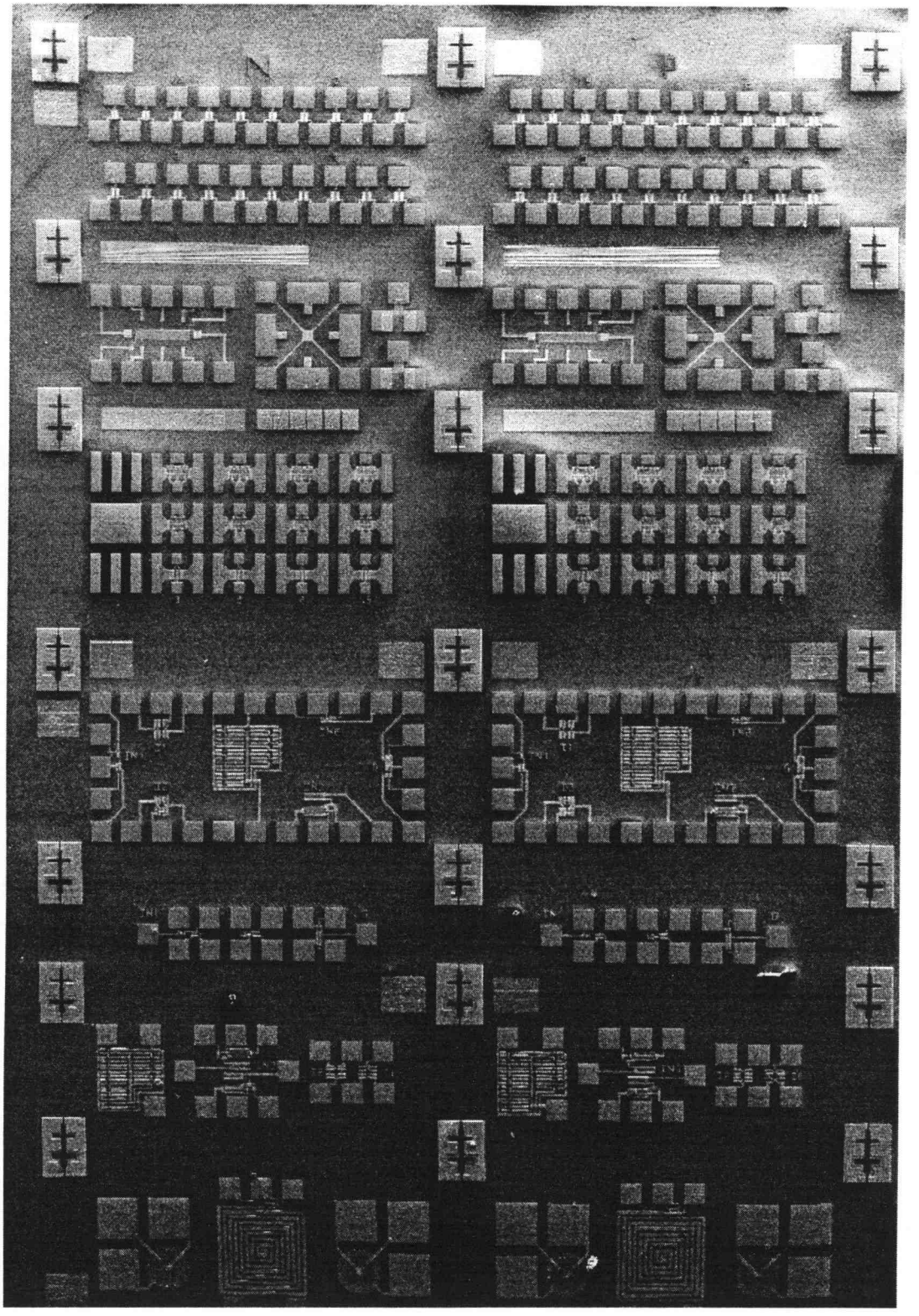

Figure 3.8. A SEM image of the layout of all devices and circuits. In the first column are the n-channel devices and in the second column are the p-channel devices. The complementary circuits are identical in either column.

4. Material and Electrical Characterization

Two of the most important elements of field effect GaAs device technology are ohmic contacts and the Schottky barrier gate because of their considerable influence on overall device performance. The method of characterization of the two components is presented first, followed by a discussion of the results obtained in this research. Series resistance also contributes the to overall device performance. Its influence and a method of extraction is presented. Next, a look at the threshold voltage and its importance in realizing complementary technology. The chapter concludes with a discussion and results on mobility measurements.

The ohmic contacts, series resistance, Schottky barrier contacts and threshold voltages were characterized electrically using a HP4145B Parametric Analyzer. Measurements were performed at room temperature. The mobility was characterized at 77K and 300K using a Keithly nanocurrent source, nanovoltmeter, and a HPIB interface with a computer in order to analyze and store the data.

4.1 Ohmic Contacts

To take full advantage of the high mobility of the 2DEG/2DHG that forms near the heterointerface of the MODFET structure, an ohmic contact must be made such that the contact resistance is very small compared to the device resistance. Minimal ohmic contact resistance ensures that most of the voltage is dropped across the semiconductor device and not across the contacts. Ohmic metallization should penetrate to the active layer and form extremely low resistance ohmic contact to the 2DEG/2DHG. At the same time, a smooth surface morphology must be maintained with minimal lateral spreading which otherwise could short out devices.

The standard method to quantitatively assess the performance of metal-semiconductor contacts is to measure the specific contact resistance ρ_c (ohm/cm^2). The transmission line measurement (TLM) offers a convenient way to measure ρ_c. A basic TLM structure consists of several ohmic contact pads of equal dimensions separated by increasing distances (see figure 4.1).

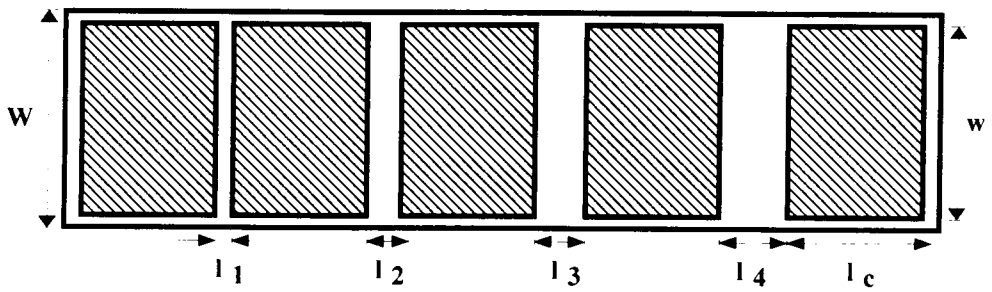

Figure 4.1. Basic TLM structure.

For a single layer planar analysis, a two contact measurement is made on a single layer planar structure. This planar structure consists of a top metal layer, an interfacial layer or a conducting layer which has been alloyed directly under the metal, and a bulk conducting layer. It is assumed that all contact resistance is due to the interfacial layer, hence the term single layer planar structure. It is also assumed that the width of the mesa W is equal to the width of the contact w (W≈w).

By measuring the total resistance R_T between any two contacts, of length l_c and width w, and plotting as a function of spacing **l**, an equation for line of R_T and **l** is found (see figure 4.2). The total resistance measured between any two given contacts is given by

$$R_T = \frac{R_s l}{W} + \frac{2R_i L_T}{W} \qquad (4.1)$$

where R_i (ohm/sq) is the sheet resistance of the interfacial material directly under the contact and R_S (ohm/sq) is the sheet resistance of the conducting layer outside the contact region and L_T is the transfer length. One can eliminate the resistance of the region between the contacts by extrapolating this line to **l** = 0. A reasonable estimate of the total specific contact resistance is given by

$$2R_C = \frac{2R_i L_T}{W} \tag{4.2}$$

as shown in figure 4.2. The transfer length L_T is estimated at the intersection of the **l** axis at $R_T = 0$ and under the assumption of $R_i = R_S$. However, the interfacial layer is degenerately doped by alloying, thereby making $R_i << R_S$ and the above assumption strictly valid.

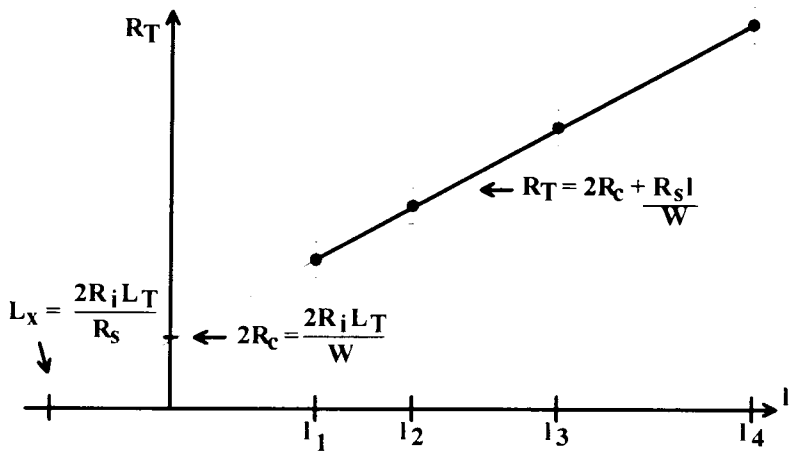

Figure 4.2. Plot of the total resistance vs. ohmic pad spacing.

To understand the transfer length, observe the current lines and notice they are not parallel near the metal contacts in planar devices (see figure 4.3). The current density is higher on the inner sides of the contacts causing current crowding effects. If a bias is

applied, a current will flow between the contacts and most of the current enters the contact within the distance of the quantity known as the transfer length.

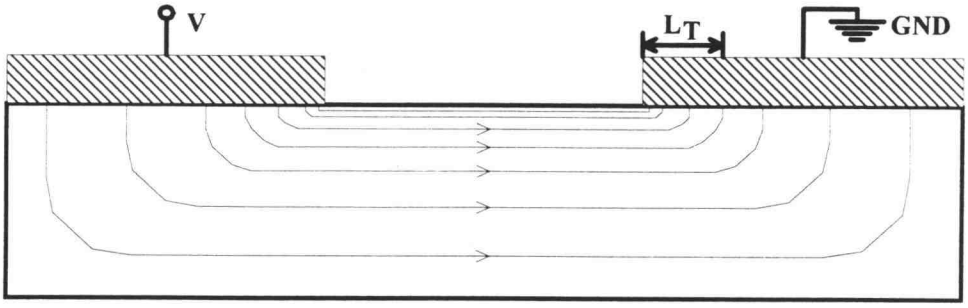

Figure 4.3. Current crowding effects in a single layer TLM structure.

A major problem with the TLM is it requires the measurement of large resistance values varying small amounts for different spacings. Also, photolithography introduces processing variations, and the exact spacing and dimensions of the defined contacts are usually slightly different than expected. Processing variations of 0.5-1.0μ were not uncommon in this research. Therefore, large errors may be introduced when the contact resistance and transfer length from the intercepts are determined. A more accurate technique, not presently used here, is the four terminal contact resistivity measurement using a four terminal Kelvin resistor [21].

The TLM structures used in this research were five ohmic metal contacts 100μ wide and 50μ in length place on a 104μ wide mesa (W≈w). The separation between each pad (i.e. l_1, l_2, ...) was 2, 4, 6 and 8μ respectively. Measurements were performed on a HP4145B parameter analyzer. The voltage was swept from -1 to 1 volt between each contact, and the current was simultaneously measured to obtain the current-voltage characteristics (this voltage range provided linear I-V characteristics).

Contact resistances on the order of 0.1 Ωmm have been reported for n-channel devices and 1 Ωmm for p-channel devices [20]. The best contact resistances obtained

from the TLM patterns in this research are on the order of 1.0 Ω mm for n-type ohmic contacts and 1.1 Ω mm for p-type ohmic contacts. Variations of measurement across the sample were seen in all the samples studied in this research. Structures in a vicinity of one another electrically behaved similarly, however structures spatially separated by large distances on the sample varied slightly. Table 4.1 summarizes representative results of contact resistance obtained in this research.

#Samples	Structure	Effective Contact Resistance ohm/mm
4	Be-doped GaAs/AlGaAs	5.1 ± 4.0
4	C-doped GaAs/AlGaAs	31.0 ± 5.0
2	Dipole-doped GaAs/AlGaAs	4.9 ± 2.1
4	Si-doped GaAs/AlGaAs	1.5 ± 0.5

Table 4.1 Device contact resistances obtained in this research.

As several samples in Table 4.1 show, the carbon doped (C-doped) AlGaAs structures processed in this study exhibit high ohmic contact resistances. Although the problem is unknown at this time, one possibility is surface segregation occurring while doping AlGaAs with carbon. Such segregation could cause a pile up of carbon at the interface of the AlGaAs and the GaAs cap layer and possibly create an impenetrable barrier for the dopants from the ohmic metallization. Hall samples have shown no problem with ohmic contacts to GaAs; however, there currently is a lack of evidence of how carbon doping behaves in AlGaAs. Further study into the carbon doped GaAs/AlGaAs contacts is being pursued.

The most serious problem noted in the fabrication of ohmic contacts was contamination. Present studies noted a correlation between the quality of ohmic contacts

and evaporator use. The thermal evaporator used to make ohmic contacts at Oregon State University is shared by several researchers for various types of projects. It was noted that after several days of consistent use for ohmic metal deposition only, the quality of ohmic contacts increased substantially. A suggestion to alleviate this problem would be the dedication of a thermal evaporator specifically for ohmic metal deposition.

4.2 Series Resistance

Ohmic contacts contribute only a part of the total resistance in a MODFET. Series resistances characterize the ungated portion of the channel between the source/drain to the edge of the gate as well as the contact resistances. The source and drain resistances, R_s and R_d shown in the equivalent circuit model figure 1.3, are key parameters in determining the performance of field effect transistors. These resistances have a strong influence on the external transconductance of the device as indicated by the following equation

$$g_{m_{EXT}} = \frac{g_{m_{INT}}}{1 + g_{m_{INT}} R_S}. \tag{4.3}$$

The source and drain series resistance are determined from a technique know as the "end" resistance measurement [9]. The basic idea of the end resistance measurement is shown in figure 4.4.

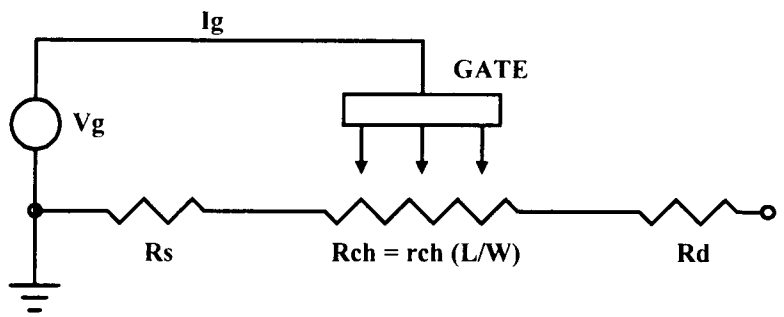

Figure 4.4. Schematic diagram of the end resistance measurement technique.

In this measurement, the gate current creates a voltage drop across the series resistance, the drain contact of the device acts as a probe. The end resistance is defined as

$$\frac{V_D}{I_g} \approx R_S + \frac{1}{2} R_{CH} \tag{4.4}$$

where the channel resistance (R_{CH}) is equal the distributed channel resistance which is equal to $r_{CH}L/W$, and where r_{CH} is the channel sheet resistance. The measured 'end' resistances are taken from the V_{ds} versus I_g curves with the source grounded and the drain floating, and then with the drain grounded and the source floating for several different values of gate length. R_s and R_d are then extracted from the total resistance versus gate length plot by extrapolating the data linearly to $L \rightarrow 0$, the point at which the channel length is equal to zero. As shown in figure 4.5, for a delta doped n-CHFET 2μ source-gate spacing devices, $R_s = 49\Omega$ and $R_d = 55\Omega$. For a delta doped p-CHFET 2μ source-gate spacing devices, shown in figure 4.6, $R_s = 275\Omega$ and $R_d = 265\Omega$. The difference between R_s and R_d is due to the misalignment of the gate. Table 4.2 summarizes representative results of series resistance obtained in this research. The series resistance was calculated as the average of the source and drain series resistance.

Structure	Drain Resistance (ohm)	Source Resistance (ohm)	Series Resistance (ohm)
Be-doped GaAs/AlGaAs	275±12	265±8	270±10
C-doped GaAs/AlGaAs	605±18	655±21	630±20
Dipole-doped GaAs/AlGaAs	325±15	295±11	310±13
Si-doped GaAs/AlGaAs	49±5	55±3	52±4

Table 4.2 Device series resistances obtained in this research.

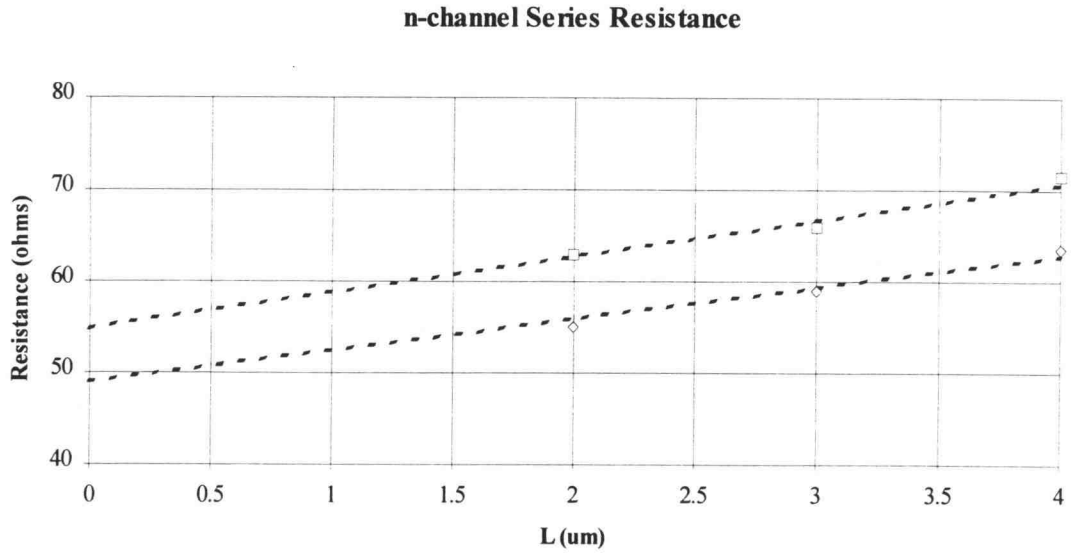

Figure 4.5. End resistance results for a 2μ source-gate spacing delta-doped Si n-CHFET.

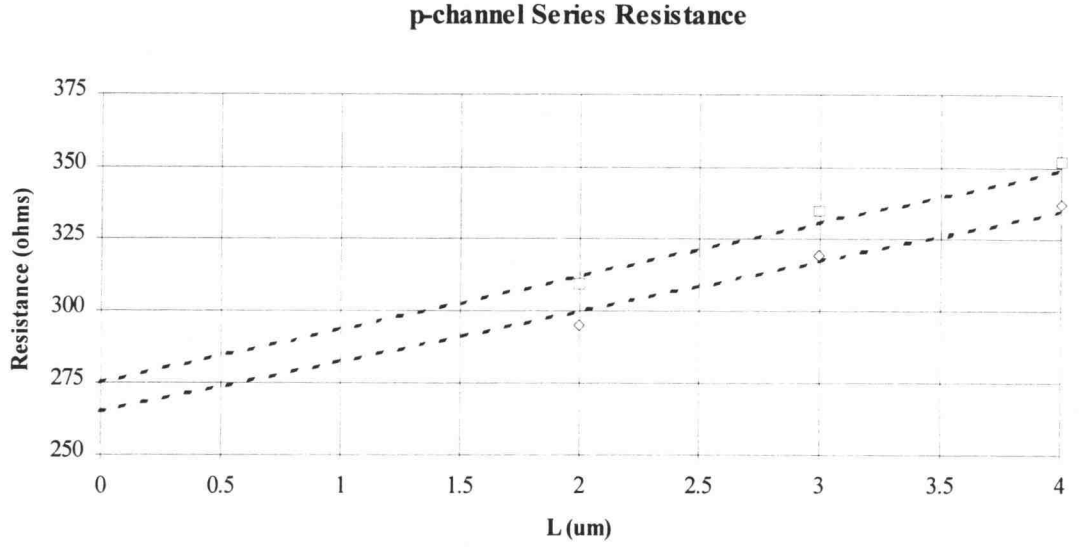

Figure 4.6. End resistance results for a 2μ source-gate spacing delta-doped Be p-CHFET.

4.3 Schottky Barrier Measurement

The Schottky gate has considerable influence on device performance. At voltages larger than 0.8 V and 0.6 V, for n- and p-type devices respectively, the gate leakage current in the MODFET becomes exceptionally high, which limits the maximum voltage swing. If the height was increased, the maximum voltage swing would increase as well as overall performance. This is especially important in the p-type MODFETs since their performance is inferior to the n-type MODFETs. To increase the effective Schottky barrier height in p-channel devices, dipole HFETs were fabricated on AlGaAs/GaAs MODFET structures.

When a metal and semiconductor are placed in contact with one another, a barrier forms to allow carrier flow only in one direction (the resulting junction is rectifying). In GaAs/metal contacts, the Fermi level is pinned at approximately midgap by interface states, and the Schottky barrier height is relatively independent of the type of metal used.

To determine the Schottky barrier height, it is necessary to first examine the dominate current mechanism, thermionic emission. The thermionic emission model of current transport is given by [22]

$$I = I_s \exp\left(\frac{qV}{nkT}\right)\left[1-\exp\left(\frac{-qV}{kT}\right)\right] \qquad (4.5)$$

where V is the applied voltage, T is the absolute temperature, q is the electron charge, k is Boltzmann's constant, I_S is the saturation current and n is the ideality factor. The ideality factor is approximately 1.0 for current flow due strictly to thermionic emission (indicating a perfect Schottky diode). However, the ideality factor is typically between 1.0 and 1.25 and increases with increased doping concentrations in the semiconductor.

For applied voltages of $V > \frac{3kT}{q}$ equation 4.5 reduces to

$$I = I_s \exp\left(\frac{qV}{nkT}\right). \tag{4.6}$$

The saturation current and ideality factor is obtained from a plot of log I versus V. The saturation current is found by extrapolating a line through the linear portion of the plot (excluding the series resistance associated with high currents) to the intercept of the current axis (see figure 4.7). The ideality factor is a given as function of the slope of this line

$$n = \frac{q}{kT}\left(\frac{\partial V}{\partial(\ln I)}\right). \tag{4.7}$$

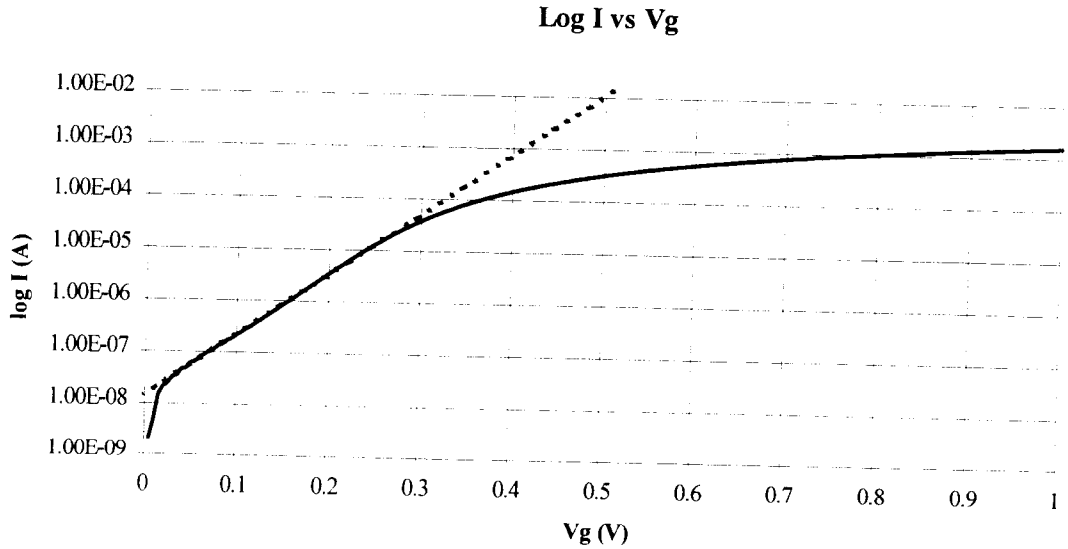

Figure 4.7. Log I vs. V_g for a p-channel MODFET.

Since thermionic emission over the barrier dominates, the current density for low to moderate dopings is a function of barrier height and temperature given by

$$J_S = A^* T^2 \exp\left[-q\left(\frac{\phi_B - \Delta\phi}{nkT}\right)\right], \tag{4.8}$$

where ϕ_B is the Schottky barrier height, $\Delta\phi$ is the image force correction (calculated for p- and n-type contacts to be 0.03 and 0.04 respectively) and A^* is the effective Richardson constant (8.16 for n-type and 74.4 for p-type contacts). Solving equation 4.8 for ϕ_B yields

$$\phi_B = \frac{nkT}{q}\ln\left(\frac{A^*T^2}{J_s}\right) - \Delta\phi\frac{nkT}{q}. \qquad (4.9)$$

Typically, the Schottky barrier height is on the order of 0.63 V for p-type $AlGa_XAs_{1-X}$ (X=0.5) and 0.82 V for n-type $AlGa_XAs_{1-X}$ (X=0.27) metal semiconductor junction [20]. The results obtained in this research have confirmed this value. From the Be-doped AlGaAs/GaAs sample, the Schottky barrier height of the Schottky gate was calculated to be on the order of ϕ_B=0.62 V with an ideality factor of n=1.4 (other p-type samples are in agreement also). For several Si-doped AlGaAs samples, the Schottky barrier height was calculated on the order of ϕ_B=0.80 V with an ideality factor of n=1.2.

The dipole sample was fabricated to improve the effective Schottky barrier height of the gate in order to obtain larger voltage swings. However, evaluation of this sample using the previous derivation for calculating Schottky barrier heights failed to confirm the increase in Schottky barrier height using such a structure. The Schottky barrier height of the Schottky gate on the p-type dipole-doped MODFET sample was calculated on the order of ϕ_B =0.65 V. This value is not a significant improvement as compared to a typical AlGaAs/GaAs structure.

However, the Schottky barrier measurement does not fully explain the results of the dipole MODFET. The purpose of the dipole structure is to increase the effective series resistance in forward bias so the current is reduced at high bias. Figure 4.8 shows a comparison of the gate current-voltage characteristics of a conventional and a dipole AlGaAs/GaAs MODFET with 4μ gate lengths.

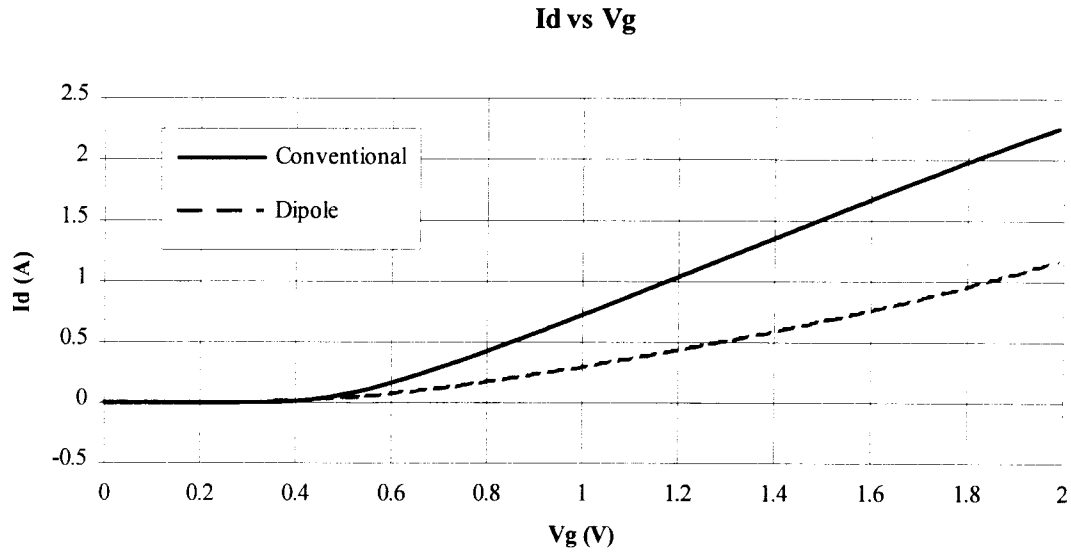

Figure 4.8. Gate current-voltage characteristics of a conventional and dipole MODFET.

As shown in this figure, the gate current at a gate voltage of 1.0 V is 0.72 mA for the conventional MODFET and only 0.30 mA for the dipole MODFET. This represents a 42 percent reduction in gate current in the dipole MODFET. This result indicates a dipole MODFET has a reduced forward-conduction gate current which leads to better performance than a conventional MODFET structure.

4.4 Threshold Control

In order to fully realize complementary circuits, a high degree of control is needed on the threshold voltage of the devices. In digital circuits, large variations in threshold voltages cause large variations in logic swing and poorer noise margins. In analog circuits, large variations in threshold voltages can render the circuits useless.

The threshold voltage is the gate voltage at which the channel is turned on and current begins to flow. The threshold voltage in a non planar technology can be controlled by recess etching. By recessing into the AlGaAs buffer region, the AlGaAs

begins to deplete. The further into this region the recess extends, the further depleted this region becomes. In depletion mode devices (normally on devices), the built-in voltage due to the Schottky barrier is not sufficient to completely deplete the channel with zero applied bias. For enhancement mode devices (normally off devices), the built-in gate voltage depletes the doped AlGaAs and overcomes the built-in potential at the heterointerface, which depletes the 2DEG/2DHG.

Wet etching techniques are often used in recess etching and were used in the present work as discussed in section 3.2.4. However, the major limitation of wet etching is the temperature dependency of the etch rate (typically etch rate $\propto e^{-1/T}$). Most etches are based on an exothermic reaction (releasing heat into the environment), which in turn changes the temperature of the etchant. In small quantities, the temperature could change drastically, therefore large batches of the etchant are needed to reduce the temperature gradient. Also, small changes in the proportion of etchant components can result in large changes in etch rates. This makes it extremely difficult to control the etch rate and etch a known distance within a specific layer of material, which in turn makes it extremely difficult to control the threshold voltage with good accuracy and reproducibility.

Dry etching is a more attractive alternative to recess etching than wet etching. Reactive ion etching (RIE) is one technique used to dry etch semiconductors. The RIE uses a plasma-generated directional ion bombardment as its etching mechanism. Unlike wet etching, it is highly directional (the vertical etch rate highly exceeds its lateral etch rate). However, the RIE is costly and was not available at this institution during the time of this research.

One way to set the threshold without wet or dry etching is to manipulate the material variables rather than use the fabrication process which recesses the buffer region. In delta-doped MODFETs, the threshold voltage is a function of the location of the delta plane in relation to the surface of the AlGaAs buffer layer and the doping density of the delta plane.

To calculate the threshold voltage for a delta-doped MODFET, we use an analytical model obtained by integrating Poison's equation using the depletion approximation. For instance, a p-type delta-doped MODFET from figure 4.8, gives potential V as

$$-qV = qV_g - q\phi_B + \Delta E_V - E_{fs}, \tag{4.10}$$

where E_{fs} is the distance from the fermi level to the base of the potential well (not shown on diagram). The surface potentials are given by

$$F(x) = F_s \qquad d_a<x<d \tag{4.11}$$
$$F(x) = F_s + qN_a \qquad 0<x<d_a.$$

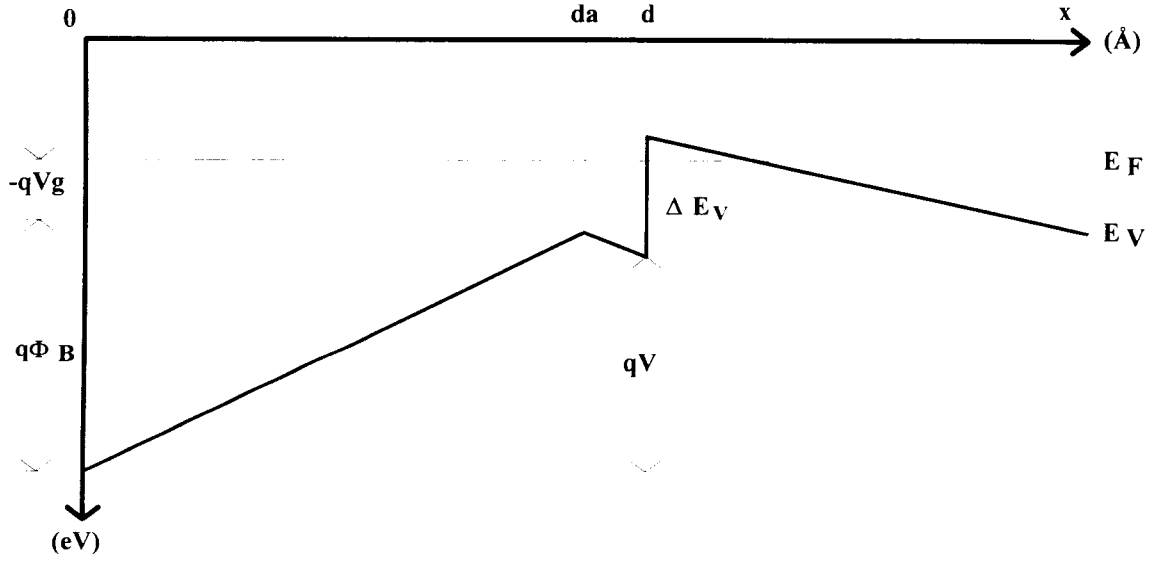

Figure 4.9. Valence band-edge diagram of a p-channel delta-doped MODFET.

The potential V is determined by integrating F(x) over 0 to d and substituting back into 4.10, this yields

$$qn_s = \frac{\varepsilon_1}{d}\left(-\frac{qN_a d_a}{\varepsilon_1} + V_g - \phi_B + \frac{\Delta E_v}{q} + \frac{E_{fs}}{q}\right) \tag{4.12}$$

which can be simplified to

$$qn_s = C_{eff}\left(V_g - V_T\right) \tag{4.13}$$

where

$$V_T = \frac{qN_a d_a}{\varepsilon_1} + \phi_B - \frac{\Delta E_v}{q}. \tag{4.14}$$

Using the equations above, an attempt was made to set the threshold in several delta doped MODFETs. Applying equation 4.14 to a known threshold voltage, the doping level (N_a) and location of the delta layer (d_a) are extracted. A Be-doped AlGaAs/GaAs structure was grown and fabricated to the specifications obtained from the calculations. The target threshold in the calculations in both samples was V_T=0.3V. The doping level was calculated to be 1E18 /cm3 and the location of the delta layer was 200 Å from the surface of the AlGaAs.

Results from the Be-doped sample differed from the targeted threshold. Evaluation of the Be-doped sample showed an average threshold voltage across the sample to be V_T=0.9 V, approximately 0.6 V off from the targeted threshold. An analysis was performed on equation 4.14 in order to understand the influence on the threshold voltage when the location and doping of the delta plane were slightly manipulated from calculated values. Results showed that if the location of the delta plane was off ±25Å from the specified distance, the threshold would shift by 0.14 V. Even more influential was the doping level in the delta plane. If the doping level in the delta plane deviated from the specified value by 30 percent, a shift of 0.4 V could be seen in the threshold voltage. In summary, the targeted threshold voltage is not that far off from the actual when the errors in the delta plane location and doping level are introduced.

4.5 Mobility Measurement

The mobility and carrier density of the material is one method used to characterize the material to check if it is suitable for further processing. Using the Van der Pauw Hall measurement, the sheet resistivity (Ω/sq), the ionized carrier densities (n_s) and mobilities (μ) are calculated for 77K and 300K for all samples grown by MBE here at Oregon State University. The Van der Pauw measurement allows the calculations of the sheet resistivity, carrier concentration and mobility of an arbitrarily shaped sample under the following conditions:

i) the contacts are sufficiently small.
ii) the contacts are located on the circumference of the sample.
iii) the sample is singly connected.
iv) the sample is uniformly thick.

To characterize the carrier density and mobility, ohmic contact metallizations are placed in the corners of a small 5 mm square sample of material (see figure 4.9). The sample is then annealed at 450C in a forming gas. With adequate ohmic contact to the sample, the measurement begins. First, a known current is passed through contacts A and B and the induced voltage is measured between contacts C and D. The measurement is repeated three more times passing known currents through contacts C and D, A and C, and B and D respectively, while measuring the induced voltages at contacts A and B, B and D, and A and C. These measurements are used to calculate the resistivity of the material. Next the hall mobility is determined by passing a known current through contacts A and D, then B and C, while measuring the induced voltage between contact B and C and A and D respectively. The measurement is performed with and without a magnetic field perpendicular to the sample with a positive and negative current. From the

resistivity measurement and the hall mobility measurement, the sheet carrier concentration is determined.

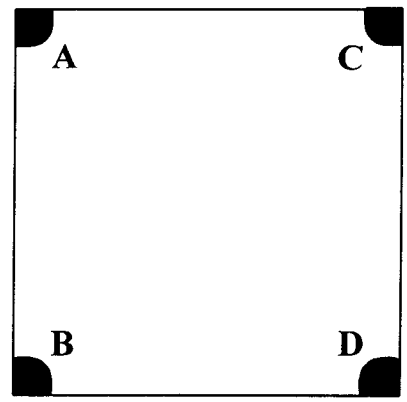

Figure 4.10. Van der Pauw test structure.

Van der Pauw measurements were performed on the same layer from which the devices were fabricated. A summary of these measurements on material of the CHFET and the single layer carbon- and dipole-doped HFETs are listed below in table 4.3.

Structure	**Mobility** **77 | 300K (cm2/V·s)**	**Sheet Concentration** **77 | 300K (1/cm2)**
Si-doped GaAs/AlGaAs	57190 | 6283	1.24E12 | 1.17E12
Be-doped GaAs/AlGaAs	1411 | 113	2.34E12 | 6.28E12
C-doped GaAs/AlGaAs	2380 | 101	5.32E11 | 4.04E12
Dipole-doped GaAs/AlGaAs	965 | 133	4.29E12 | 3.83E12

Table 4.3. Mobility and sheet carrier measurements.

5. CHFET Characterization Results

To date, several delta-doped CHFET structures were successfully grown, fabricated and characterized. As previously mentioned, the pseudomorphic layer structure was unavailable due to complications with the indium source in the MBE at the time of this research. However, the process outlined in this research directly parallels the fabrication of pseudomorphic layer structures.

To begin, results from a successfully fabricated CHFET are presented. The CHFET structure discussed is a delta-doped p- and n-type structure in a stacked formation. The individual devices and circuits on this sample were complete and in good appearance (see figures 3.3 through 3.8). However, the circuits did not function because of threshold voltage complications. Also shown are the current-voltage and transconductance characteristics of a carbon- and dipole-doped p-channel HFET. The DC and RF characterization of individual p- and n-type devices are presented, followed by a discussion of results.

5.1 n-device DC Characterization

DC characterizations were performed at room temperature and under no illumination. Current-voltage characteristics for n-channel CHFET devices having a gate-source spacing of 2μ and W/L = 95μ /2μ are shown in figures 5.1 through 5.3. The drain-to-source current (I_{ds}) as a function of gate-to-source voltage (V_{gs}) is shown in figure 5.1. These devices also exhibit excellent turn-off behavior as well as good behavior in the saturation region as shown by the flatness of the curve in this region indicating little leakage between the source and drain.

Shown in figure 5.2 is the extrinsic transconductance $g_{m_{ext}}$ as a function of gate voltage V_{gs}. The room temperature extrinsic transconductance for this device is 120

mS/mm. Measurements from section 4.2 yielded an average parasitic source resistance of approximately Rs= 52 ± 4Ω . Using this resistance in conjunction with equation 4.3, the intrinsic transconductance $g_{m_{int}}$ is calculated to be 297 mS/mm. Thus, considerable improvement in gain could be realized by reduced series resistance.

The gate voltage transfer characteristics (V_g versus the I_{ds}) are shown in figure 5.3. These characteristics show linear behavior associated with short channel devices. This figure shows the actual measured gate voltage transfer characteristics along with calculated values using equation 1.8 (saturation current for short channel devices) and results of mobility measurements taken from the same material (see section 4.5). The threshold voltage is calculated by extrapolating a line from the linear region of the curve V_{gs} versus the I_{ds} back to the x-axis and in this case is on the order of V_T = -0.75 V.

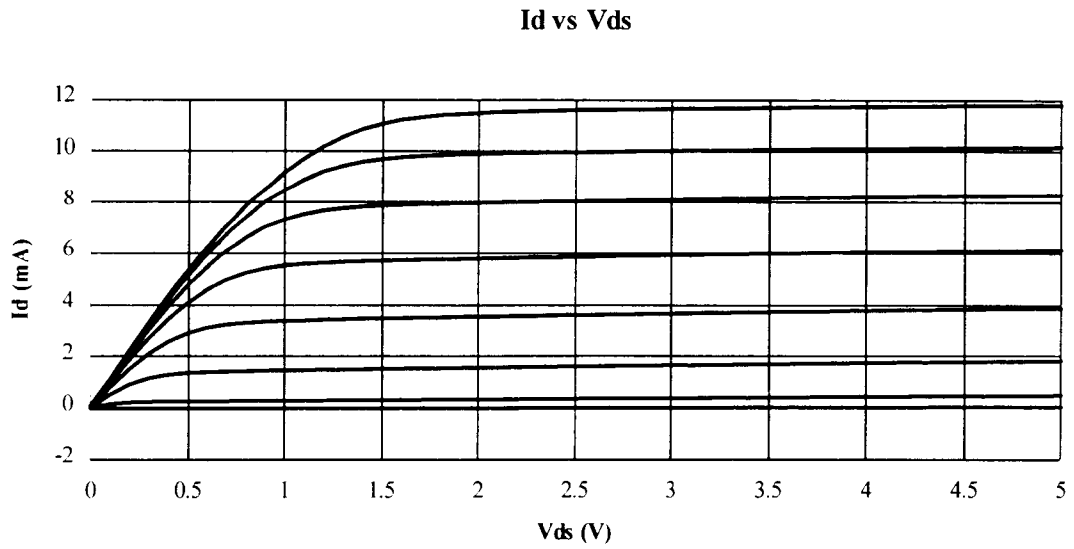

Figure 5.1. I-V characteristics of a 2μ source-gate spacing and a 2μ gate length Si delta-doped n-channel CHFET at 300K and unilluminated.

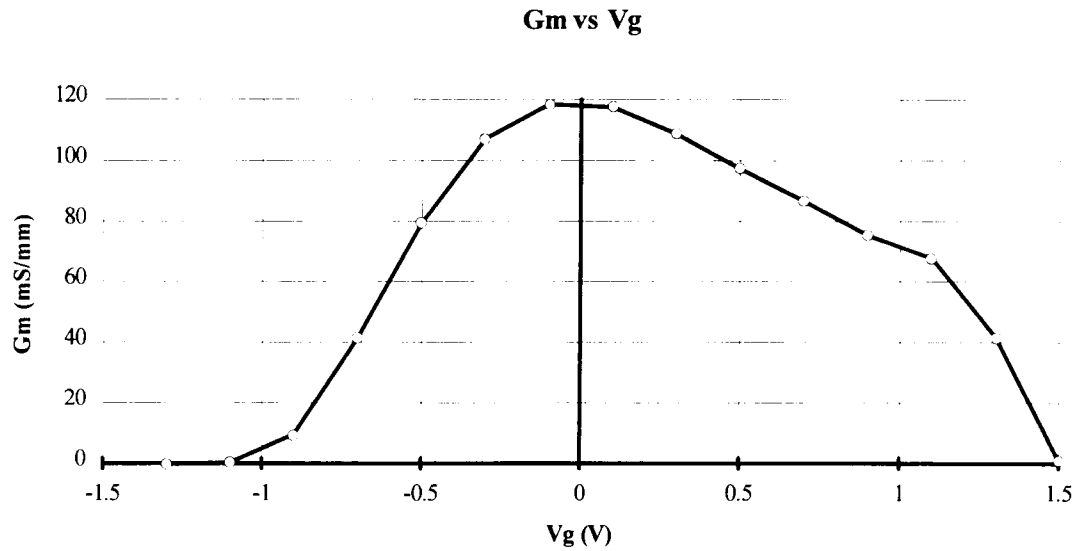

Figure 5.2. Extrinsic transconductance of a 2μ source-gate spacing and a 2μ gate length Si delta-doped n-channel CHFET at 300K and unilluminated.

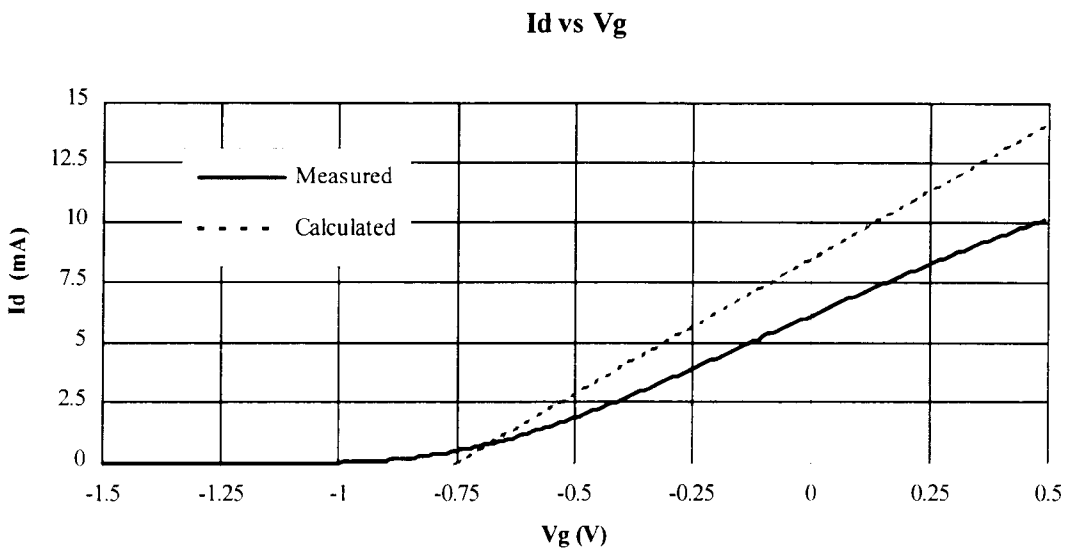

Figure 5.3. Gate voltage transfer characteristics of a 2μ source-gate spacing and a 2μ gate length Si delta-doped n-channel CHFET at 300K and unilluminated.

5.2 p-device DC Characterization

DC characterizations were performed at room temperature and under no illumination. Current-voltage characteristics for Be delta-doped p-channel CHFET devices having a gate-source spacing of 2μ and W/L = 95μ /2μ are shown in figures 5.4 through 5.6. Also shown, in figures 5.7 through 5.10, are the current-voltage characteristics and transconductance for a carbon- and dipole-doped HFET having a gate-source spacing of 2μ and W/L = 95μ /2μ. The drain-to-source current (I_{ds}) as a function of gate-to-source voltage (V_{gs}) is shown in figures 5.4, 5.7 and 5.9 for the Be delta-, dipole- and carbon-doped HFETs respectively. These characteristics show good turn-off behavior unilluminated with the exception of the dipole-doped structure. The dipole-structure could not be completely turned off, indicating a leakage current between the source and drain. This is evident in figure 5.8 by the slope of the current-voltage line in saturation. The current is associated with leakage through the substrate and is probably due to a material growth problem rather than processing. However, substrate leakage occurs in all three of these p-channel structures under illumination, this is probably due to a trapping effect in the p-type material.

Shown in figure 5.5 is the extrinsic transconductance $g_{m_{ext}}$ as a function of gate voltage V_{gs} for the Be delta-doped CHFET. The room temperature extrinsic transconductance for this device is 14 mS/mm. Measurements from section 4.2 yielded an average parasitic source resistance of approximately Rs= 270 ± 10Ω . Using this resistance in conjunction with equation 4.3, the intrinsic transconductance $g_{m_{int}}$ is calculated to be 22.5 mS/mm. Although the series resistance limits the transconductance, in this case it is still low regardless. The reason for this is due to the low mobility in the p-channel devices. The room temperature p-channel mobility was only 113 $cm^2/V\bullet s$ as compared to the n-channel material having a room temperature mobility of 6283 $cm^2/V\bullet s$ (see section 4.5). The extrinsic transconductances for the dipole- and carbon-doped

HFETs are shown in figures 5.8 and 5.10. The dipole-doped HFET shows a comparable transconductance to the Be-doped HFET. The carbon-doped HFET suffered from high ohmic contact, high series resistance and low room temperature mobility, therefore, it was expected to have lower transconductances as compared to the Be delta-doped CHFET.

The gate voltage transfer characteristics (V_g versus the I_{ds}) for the Be delta-doped CHFET are shown in figure 5.6. Similar to the Si n-channel CHFET, these characteristics show linear behavior associated with short channel devices. This figure shows the actual measured gate voltage transfer characteristics along with calculated values using equation 1.8 (saturation current for short channel devices) and results of mobility measurements taken from the same material (see section 4.5). The threshold voltage is on the order of V_T = 0.85 V and shifted approximately -0.1V under illumination.

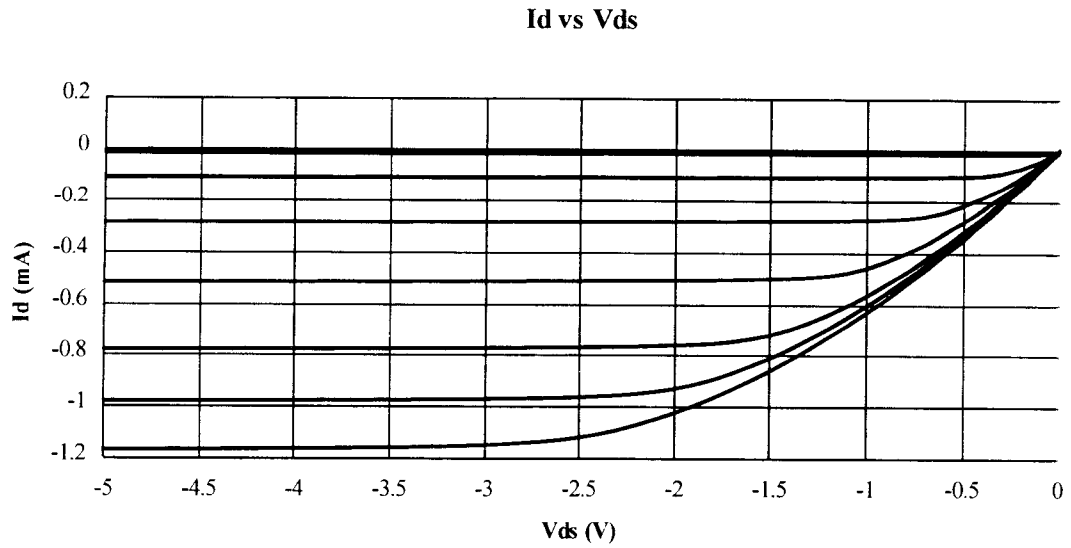

Figure 5.4. I-V characteristics for a 2μ source-gate spacing and a 2μ gate length Be delta-doped p-channel CHFET at 300K and unilluminated.

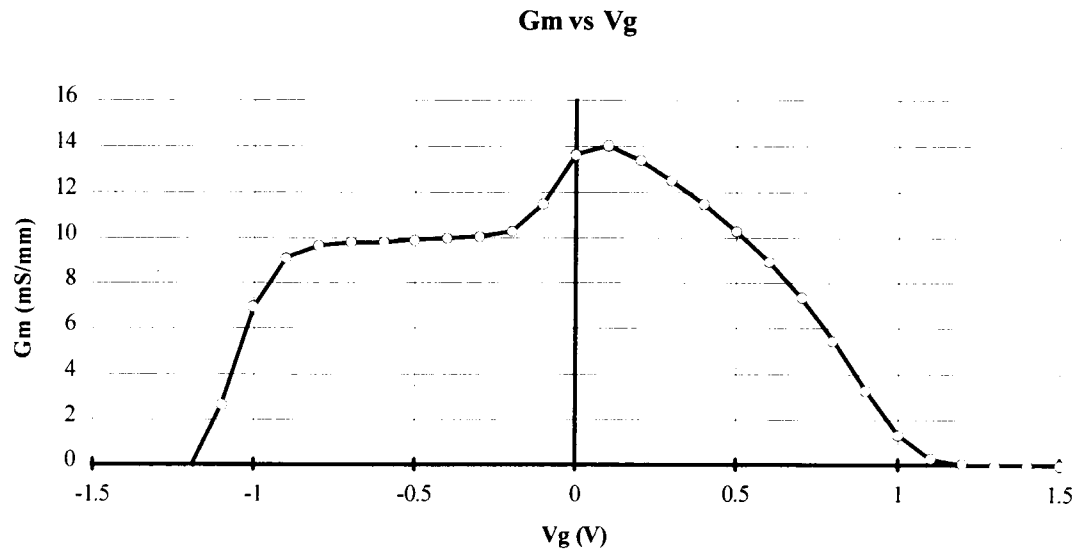

Figure 5.5. Extrinsic transconductance of a 2μ source-gate spacing and a 2μ gate length Be delta-doped p-channel CHFET at 300K and unilluminated.

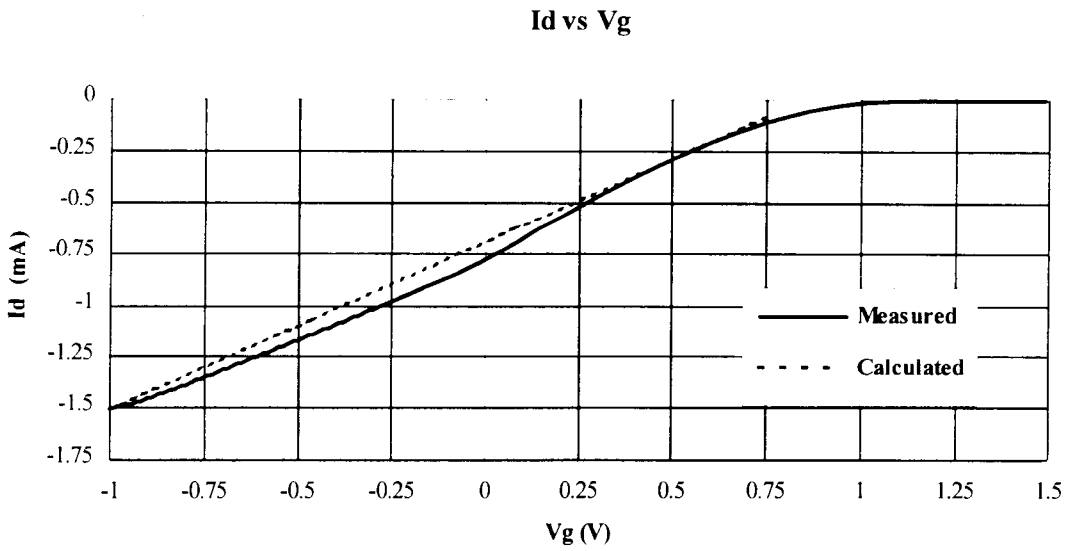

Figure 5.6. Gate voltage transfer characteristics of a 2μ source-gate spacing and a 2μ gate length Be delta-doped p-channel CHFET at 300K and unilluminated.

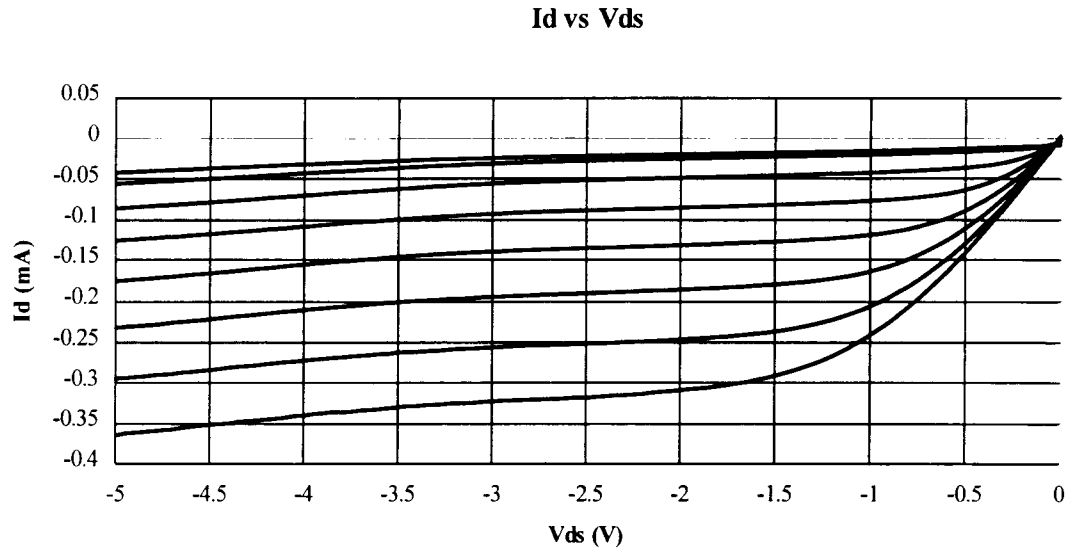

Figure 5.7. I-V characteristics of a 2μ source-gate spacing and a 2μ gate length dipole-doped p-channel HFET at 300K and unilluminated.

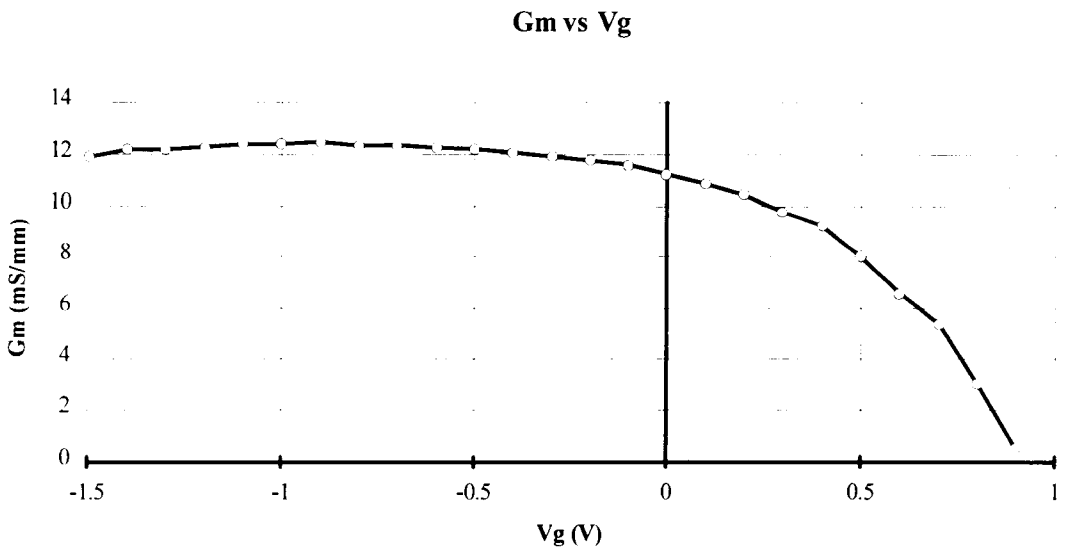

Figure 5.8. Extrinsic transconductance of a 2μ source-gate spacing and a 2μ gate length dipole-doped p-channel HFET at 300K and unilluminated.

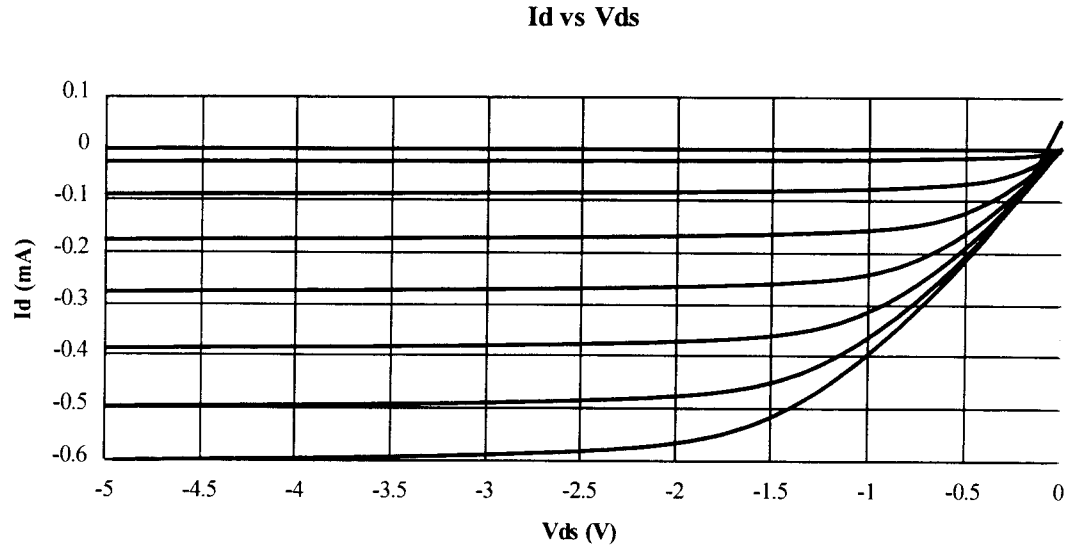

Figure 5.9. I-V characteristics of a 2μ source-gate spacing and a 2μ gate length carbon-doped p-channel HFET at 300K and unilluminated.

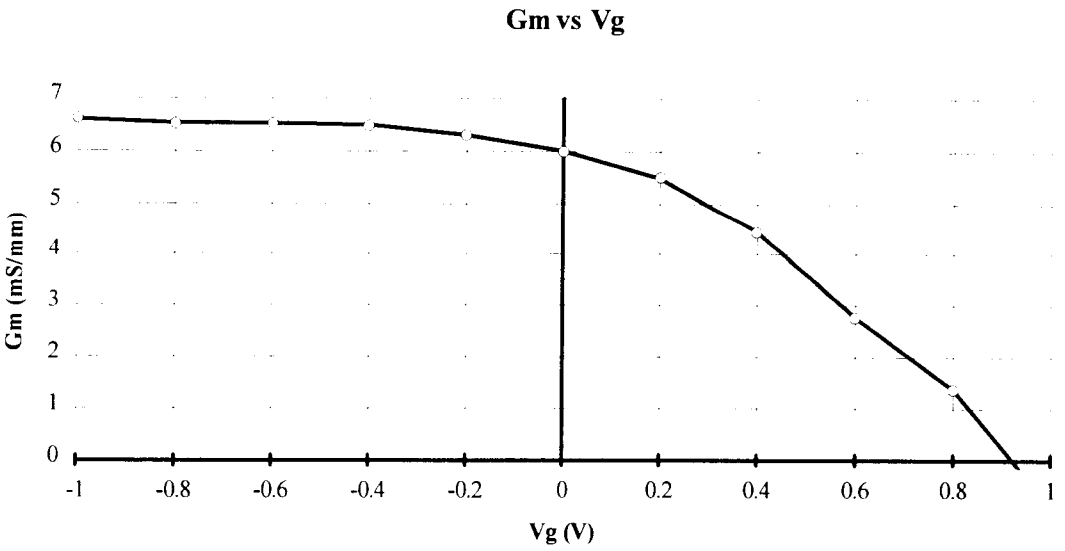

Figure 5.10. Extrinsic transconductance of a 2μ source-gate spacing and a 2μ gate length carbon-doped p-channel HFET at 300K and unilluminated.

5.3 High Frequency Characterization

The S-parameters used to characterize the RF transistors were extracted with a HP 8510B Network Analyzer. Using high precision HP cascade microprobes, a two fingered n-channel RF device with a 2u gate length and a 3u source-to-gate spacing was set up as a two-port network. The RF device was then tested at a frequency range between 100 MHz and 10 GHz. DC measurements were performed to determine optimum gate bias corresponding to the device's maximum transconductance. For the n-channel RF transistor, the maximum transconductance occurred at a gate bias of approximately 0.0 V. Figure 5.11 shows the measured S-parameter data for $|S_{21}|$. The unity gain bandwidth (F_T) of the device was approximately 5.54 GHz with a maximum transducer power gain of 30.3 dB at 1 GHz, for a drain-to-source bias of 5.0 V and a 0.0 V gate bias. However, the p-channel RF transistors performance was too low to be measured on the Network Analyzer; RF characterization could not be performed on these devices.

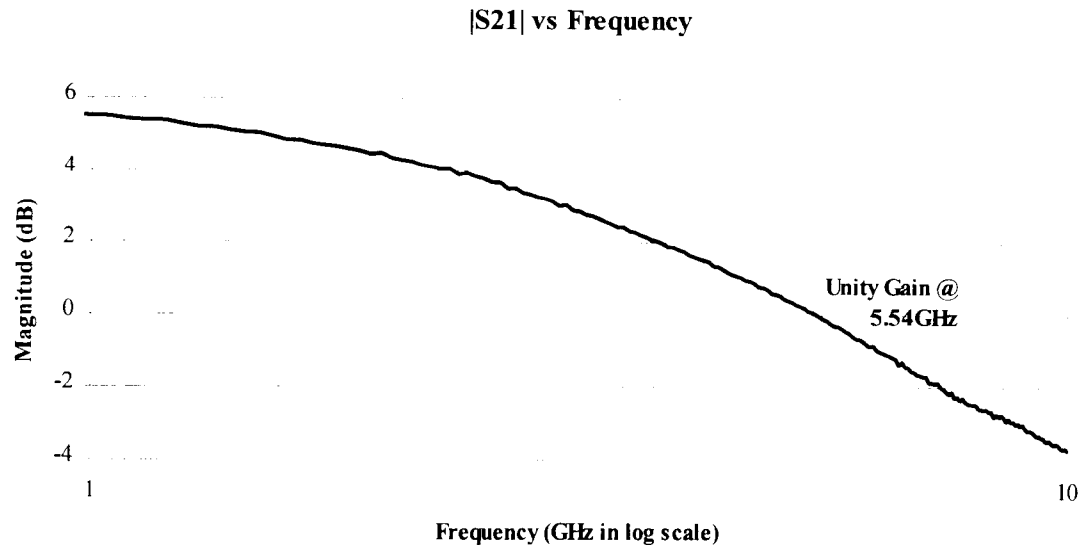

Figure 5.11. Measured S-parameter data of $|S_{21}|$ for a n-channel CHFET.

5.4 Discussion of Results

Measured and calculated data using linear behavior model for the saturation current is shown in figures 5.2 and 5.5 for n- and p-channel devices, respectively. These curves show fairly good agreement between one another within one order of magnitude, which is acceptable since the linear behavior model for the saturation current (equation 1.8) is only a first order approximation.

A large difference in the p-channel transconductance is evident when compared to the n-channel transconductance as shown in figures 5.2, 5.8, and 5.10 for p-channel and 5.5 for n-channel devices. The peak transconductance is substantially lower in the p-channel devices, which leads to a large mismatch in performance between the two devices. Through the use of strained layers, the p-type material mobility can be improved, thus narrowing the mismatch between the two devices (see section 1.2).

Through the course of this research, carbon-doping and dipole-doping were investigated to improve the performance of p-channel devices. The p-channel carbon-doped MODFETs showed extremely high ohmic contact and series resistances--these complications are discussed in the latter part of section 4.1. However, the dipole-doped MODFET increased the performance in p-channel devices by reducing the forward conduction gate current (see section 4.3). The dipole MODFET was grown and tested successfully on a single layer basis. Apart from the severe substrate leakage in the dipole-doped HFET, the transconductance was still comparable to the Be-doped HFET and proved to be a suitable replacement. However, when a CHFET structure was grown using a dipole p-type structure placed on top of a delta-doped n-type structure, complications with the MBE system occurred. The material grown was inconsistent in composition with previous samples obtained from the system, problems with fabrication occurred and time ran out for regrowth.

In the course of this research, numerous batches of transistors were fabricated and tested, most of which were used to optimize the layer structure of the CHFET for peak performance and to develop the current fabrication process. However, further optimization needs to be pursued. The threshold voltage in recent material growths could not be controlled with reasonable accuracy; therefore, the circuits on the structure , which rely on tight threshold control, were rendered useless. Efforts continue to this day to stabilize and set the threshold voltage accurately. The optimization and advancement of p-type device performance is an ongoing issue.

6. Conclusions

The goal of this research has been to develop complementary circuit technology for GaAs integrated circuit technology. The focus of this thesis has been on the design, fabrication and characterization of n- and p-channel HFET devices on the same wafer for further use in analog and digital circuit designs.

Complementary devices were successfully fabricated in-house at Oregon State University using a 2μ non self-aligned process. In summary, this thesis covers several heterojunction structures, processing techniques, electrical and material characterization, representative device characteristics and actual results on non-strained delta-doped complementary heterojunction field effect transistors. A summary of the best results are listed below in table 6.1.

Sample	77K u cm2/V·s	300K u cm2/V·s	Rc ohm/mm	Rs ohm	gm (ext) mS/mm	gm (int) mS/mm
Complementary n-channel structures						
Si delta-doped	57190	6283	1.1	52	120	297
Complementary p-channel structures						
Be delta-doped	1411	113	1.5	270	14	22.5
Single p-channel structures						
Carbon-doped	395	44	26.1	605	7	11.7
Dipole-doped	965	133	5.1	310	12.4	19.5

Table 6.1. Summary of results.

A few processing issues need to be resolved to further optimize the performance of the in house CHFETs, the first of which is accurately setting the threshold voltage. The threshold voltage can be set in a couple of different ways, by recessing the gate or

through material variables. Since the in house process uses only wet etching techniques, it is desirable to set the threshold voltage by manipulating growth parameters. However, manipulating these parameters has proven to be a difficult task since the MBE is used more in a research mode (several experiments) rather than a production mode (concentration on one growth). The outcome of the research demonstrates a need to set the threshold empirically using numerous samples with no variation in MBE growth (trial and error method). An attractive alternative would be to use a reactive ion etcher (RIE) to set the threshold by means of dry etching the gate recess. However, even then, stardardized growth is necessary.

Another problem encountered in this research has been high series resistance, especially seen in the p-channel structures. Based on end resistance and TLM measurements, the dominate part of this resistance stems from the drain-to- and source-to-gate spacings. Reducing this resistance is difficult to do in non-planar recess technology as presented in this thesis. A self-aligned planar technology utilizing ion-implantation, would significantly reduce the series resistance. The other contribution to the series resistance is introduced in the formation of ohmic contacts. Contamination introduced into the evaporation system has lead to high ohmic contact resistance. This problem has been alleviated through time and the constant use of one metal-contact system in the evaporation system.

In material related matters, the use of carbon-doped and dipole MODFETs has been explored as a means to further improve the performance of p-channel devices. The carbon-doped HFETs suffered from high ohmic contact and series resistance resulting in poor performance. The dipole-doped HFETs, with equivalent performance of delta-doped Be HFETs, have proven useful in reducing forward conduction gate current which leads to better performance. In addition, efforts have been made to improve the relatively poor performance in p-channel devices through the use of pseudomorphic structures. Although high quality pseudomorphic CHFET structure were not realized in-house at the

time of this research, the process design for non-strained delta-doped complementary material parallels the one necessary for fabricating pseudomorphic CHFETs. Further work in the area of pseudomorphic CHFET of fabrication would prove beneficial when the material becomes available.

Bibliography

1. L. Esaki, R. Tsu, IBM J. Res. Dev., Vol. 14, p.61-65, January 1970.

2. R.Dingle, G. L. Stormer, A. C. Gossard, and W. Wiemann, Appl. Phys. Lett. 33(7), pp.665-667, October 1978.

3. T Mimura, S. Hiyamizu, T. Fuji and K. Nanbu, Jap. J. Appl. Phys., vol. 19, no. 5, pp. L225-L227, May 1980.

4. P. Chao, M. S. Shur, R. C. Tiberio, K. H. George Duh, P. M. Smith, J. M. Ballingall, P. Ho and A. A. Jabra, IEEE trans. Electron Devices, vol ED-36, no.3, pp 461-471, March 1989.

5. K. L. Tan, R. M. Dia, D. C. Streit, A. C. Han, T. Q. Trinh, J. R. Velebir, P. H. Liu, T. Lin, H. C. Yen, M. Sholley and L. Shaw, IEEE Electron Device Lett., vol. EDL-11, no. 7, pp.303-305, July 1990.

6. P. P. Rudan, M. Shur, D. K. Arch, R. R. Daniels, D. E. Grider and T. E. Nohava, IEEE trans. Electron Devices, vol. ED-36, no.11, pp.2371-2378, November 1989.

7. J. J. Rosenberg, M. Benlamri, P.D. Kirchner, J. M. Woodall, and G. D. Pettit IEEE Electron Device Lett., vol. EDL-6, no. 10, pp.491-493, October 1985.

8. T. E. Zipperian and T. J. Drummond, Electron. Lett., vol.21, no.18, pp.823-824, August 1985.

9. M. Shur, "GaAs Devices and Circuits", Plenum Press, New York,1987.

10. K. Lee, M. S. Shur, T. J. Drummond, and H. Morkoc, IEEE trans. Electron Devices, vol. ED-30, no.3, pp.207-212, May 1983.

11. H. R. Yeagar, R. W. Dutton, IEEE trans. Electron Devices, vol. ED-33, no.5, pp.682-691, May 1986.

12. K. R. Cioffi, S. M. Kang, and T. N. Trick, IEEE International Symposium on Circuits and Systems, pp. 405-408, 1988.

13. A. A. Keterson, W. T. Masselink, J. S. Gedymin, J. Klem, C. Peng, and K. R. Gleason, IEEE trans. Electron Devices, vol. ED-33, no.5, pp.564-571, May 1986.

14. K. W. Kim, H. Tain and M. A. Littlejohn, IEEE trans. Electron Devices, vol. ED-38, no.8, pp.1737-1742, August 1991.

15. J. Zou, H. Dong, A. Gopinath and M. Shur, IEEE trans. Electron Devices, vol. ED-39, no.2, pp.250-256, Febuary 1992.

16. T. Akinwande, J. Zou, M. S. Shur, and A. Gopinath, IEEE Electron Device Lett., vol. EDL-11, no. 8, pp.332-333, August 1990.

17. C. Giannini, A. fischer, C. Lange, K. Ploog and L. Tapfer, Appl. Phys. Lett., 61(2), pp.183-185, July 1992.

18. R. J. Malik, R. N. Nottenberg, E. F. Schubert, J. F. Walker and R. W. Ryan, Appl. Phys. Lett., 53(26), p.2661-2663, December 1988.

19. N. C. Cirillo, Jr., J. K. Abrokwah, and M. S. Shur, IEEE Electron Device Lett., vol. EDL-5, no. 4, pp.129-131, April 1984.

20. R. K. Willardson and A. C. Beer, "Semiconductors and Semimetals", vol 15, Academic Press, New York, 1981.

21. R. Williams, "Gallium Arsnide Processing Techniques", Artech House, Ma, 1984.

22. J. R. Waldrop, Appl. Phys. Lett., 44(10), p.1002-1004, May 1984.

Appendix

List of Etches

Mesa Etch:

Purpose	Etches GaAs AlGaAs and InGaAs non selectively.
Chemical	$NH_4OH : H_2O_2 : H_2O_{(DI)}$
Mixture ratio	2 : 1 : 100
Etch rate	≈2000 Å/min

Native Oxide Etch:

Purpose	Etches native oxides from GaAs and AlGaAs surfaces
Chemical	$NH_4OH : H_2O_{(DI)}$
Mixture ratio	1 : 3
Etch rate	unknown
Comments	10-15 seconds is sufficient for stripping surface oxides

Silicon Dioxide etch:

Purpose	Etches SiO_2
Chemical	$HF_{(buffered)} : H_2O_{(DI)}$
Mixture ratio	1 : 10
Etch rate	≈1000 Å/min
Comments	Buffered HF- add 1 part HF (48%) to 4 parts unsaturated NH4F solution (ph≈4).

Citric Etch:

Purpose	Selectively etches between GaAs and AlGaAs systems.
Chemical	Citric acid : H_2O_2
Mixture ratio	2 : 1 (for 27% AlGaAs)
	10 : 1 (for 50% AlGaAs)
Etch rate	≈2500 Å/min
Comments	Blend citric acid to deionized water in the ratio of 1:1 by weight.

HF Etch:

Purpose	Used to selectively etch between AlGaAs and GaAs
Chemical	HF (48%)
Etch Rate	≈3000Å/min
Comments	10-15 seconds is sufficient for stripping 500Å of AlGaAs