AN ABSTRACT OF THE THESIS OF

Mankoo Lee for the degree of **Doctor of Philosophy** in **Electrical and Computer Engineering** presented on **May 31, 1990**.

Title: ANALYSIS AND MODELING OF GaAs MESFET's FOR LINEAR INTEGRATED CIRCUIT DESIGN.

Abstract approved : Redacted for Privacy

Professor Leonard Forbes

A complete Gallium Arsenide Metal Semiconconductor Field Effect Transistor (GaAs MESFET) model including deep-level trap effects has been developed, which is far more accurate than previous equivalent circuit models, for high-speed applications in linear integrated circuit design.

A new self-backgating GaAs MESFET model, which can simulate low frequency anomalies, is presented by including deep-level trap effects which cause transconductance reduction and the output conductance and the saturation drain current to increase with the applied signal frequency. This model has been incorporated into PSPICE and includes a time dependent I-V curve model, a capacitance model, a subthreshold current model, an RC network describing the effective substrate-induced capacitance and resistance, and a switching resistance providing device symmetry.

An analytical approach is used to derive capacitances which depend on V_{gs} and V_{ds} and is one which also includes the channel/substrate junction modulation by the self-

backgating effect. A subthreshold current model is analytically derived by the mobile charge density from the parabolic potential distribution in the cut-off region. S-parameter errors between previous models and measured data in conventional GaAs MESFET's have been reduced by including a transit time delay in the transconductances, g_m and g_{ds}, by the second order Bessel polynomial approximation. As a convenient extraction method, a new circuit configuration is also proposed for extracting simulated S-parameters which accurately predict measured data. Also, a large-signal GaAs MESFET model for performing nonlinear microwave circuit simulations is described.

As a linear IC design vehicle for demonstrating the utility of the model, a 3-stage GaAs operational amplifier has been designed and also has been fabricated with results of a 35 dB open-loop gain at high frequencies and a 4 GHz gain bandwidth product by a conventional half micron MESFET technology. Using this new model, the low frequency anomalies of the GaAs amplifier such as a gain roll-off, a phase notch, and an output current lag are more accurately predicted than with any other previous model.

This new self-backgating GaAs MESFET model, which provides accurate voltage dependent capacitances, frequency dependent output conductance, and transit time delay dependent transconductances, can be used to simulate low frequency effects in GaAs linear integrated circuit design.

ANALYSIS AND MODELING OF GaAs MESFET's FOR LINEAR INTEGRATED CIRCUIT DESIGN

by

Mankoo Lee

A THESIS

Submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

DOCTOR OF PHILOSOPHY

Completed: May 31, 1990

Commencement: June 1991

APPROVED:

Redacted for Privacy

Professor of Electrical and Computer Engineering in Charge of Major

Redacted for Privacy

Head of Department of Electrical and Computer Engineering

Redacted for Privacy

Dean of Graduate School

Date thesis is presented: May 31, 1990

Typed by: Mankoo Lee

ACKNOWLEDGEMENTS

I would like to express my sincere appreciation to Dr. Leonard Forbes, my major professor, for his helpful academic guidance, research discussions, generous consideration, and constant encouragement during this academic experience. My success in this endeavor can be largely attributed to his assistance.

I am grateful to other members of my Ph.D. Committee: Dr. James A. Van Vechten, Dr. Thomas K. Plant, Dr. Toshimi Minoura, and, especially, Dr. Vijai K. Tripathi for his generous concern throughout this research study.

Thanks are also extended to Mr. Thor Hallen of Tektronix for his helpful discussions and Mr. Raj Savara of TriQuint Semiconductor for providing test devices in fulfilling my research projects.

Finally, I would like to give special thanks to my father and my older sisters for their patience and encouragement during this period of study. In particular, to unforgettable deceased mother I wish to dedicate my thesis in memories of affection and gratitude.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF FIGURES (Continued)

LIST OF FIGURES (Continued)

LIST OF TABLES

ANALYSIS AND MODELING OF GaAs MESFET's FOR LINEAR INTEGRATED CIRCUIT DESIGN

CHAPTER 1

INTRODUCTION

As modern electronic technology advances into the range of microwave speed, GaAs has a tremendous advantage over most silicon technologies in terms of speed, power, and radiation hardness. The smaller effective mass of GaAs electrons, about 7 % that of silicon, makes the electron mobility almost six times higher than for silicon. For low electric field applications, the speed of GaAs devices is much higher, with electron velocities measured up to five times that of the comparable silicon devices[7]. The high mobility and high peak velocity of electrons are important properties in GaAs for realizing high-speed integrated circuits.

GaAs devices with very high transconductances and low input capacitances can obtain much higher gain bandwidth products that lead to switching speed of silicon. This makes GaAs an ideal candidate for high-speed switching devices. Many novel device structures have been proposed based on GaAs material and its advanced technologies, which lead to faster digital circuits and low noise high power microwave amplifiers, and also introduce new possible areas of applications such as three-dimensional integrated circuits.

However, often these new technologies involve greater process complexity and more stringent tolerances[8].

As GaAs advanced technologies give rise to new problems in device physics and modeling, it becomes essential to better understand device physics and to develop device models for GaAs circuit applications. It is also necessary to incorporate these models into a circuit simulator such as SPICE to properly simulate and design GaAs integrated circuits.

However, the only technology available for GaAs with any degree of commercial success to date has been a MESFET. Basically, this device has a metal gate directly on the active layer of semi-insulating GaAs, with highly doped source and drain. This leads to small capacitances associated with the gate, thereby giving high bandwidth products and high speeds. From the fiscal viewpoint, to avoid process complexity and to realize the speed advantages of GaAs, one of optimum GaAs devices is a conventional GaAs MESFET fabricated using ion implantation into semi-insulating substrates.

However, conventional GaAs MESFET's have some low frequency anomalies[1,9-14] which complicate the design of analog integrated circuits. Physically, these phenomena are related to deep-level trapping which occurs when electrons are scattered into traps near the channel/substrate transition region and to the surface state occupancy which can follow the applied signal[12]. Typical low frequency

effects observed in GaAs MESFET's have been referred to as a self-backgating effect, frequency dependent output conductance, current lag effect, and hysteresis and oscillations in the frequency domain. There is also the transit time delay effect produced between gate-to-source voltage and drain current in the time domain. This effect dominates the AC small signal MESFET behavior in operation near the cutoff frequency[3,15].

In respect to device modeling, these anomalies are closely related to the semi-insulating substrate-induced spreading resistances and capacitances which are functions of temperature and voltage. Voltage changes at the drain can modulate the backgate depletion layer through the substrate-induced spreading resistances and capacitances with multiple time constants[3,16]. Even though there are multiple time constants, an RC network, consisting of an effective substrate-induced resistance and capacitance, is included between drain and source through the internal backgating terminal. A transit time delay is considered in both the transient analysis and AC analysis. However, one of the principal limitations has been the lack of an easy and accepted technique of including low frequency anomalies with a symmetrical device model in GaAs integrated circuit simulations [1,3].

Based on the Statz I-V curve model [5] which already has well defined DC characteristics and an early saturation at low drain voltage, a self-backgating GaAs MESFET model

has been developed by including deep-level trap effects which cause transconductance reduction and the output conductance and the saturation drain current to increase with the applied signal frequency.

This model includes a time dependent I-V curve model, a capacitance model, an RC network describing the effective substrate-induced capacitance and resistance, and a switching resistance providing device symmetry. This I-V curve model affords new analytical I-V characteristic expressions to be discussed in chapter 3 and implies the requirement of a low EL2 concentration in the semi-insulating GaAs substrate for minimal low frequency anomalies. An analytical capacitance model describes the dependence of capacitance on V_{gs} and V_{ds} and is one which also includes the channel/substrate junction modulation by the self-backgating effect. To test the accuracy of the new models, the computed model data will be compared with measured data in detail.

Subthreshold conduction is important for describing high speed switching performance in many digital applications. Although a well-fitted empirical GaAs MESFET subthreshold current model[7] has been published, no analytical model has been proposed to describe the physical interpretations of conventional GaAs MESFET subthreshold conduction mechanisms. An analytical subthreshold current model has been developed. A transit time delay is also included in transconductances, g_m and g_{ds}, to reduce S-

parameter errors between previous models and measured data. This model has now also been incorporated into PSPICE as a new GaAs MESFET model.

Besides low frequency anomalies, one of the typical problems which complicates circuit design is an excessive low frequency (1/f) noise[18-22]. The silicon bipolar transistor is still considered superior to a GaAs MESFET in low frequency noise performance. In silicon bipolar transistors, under optimum conditions, the noise corner frequency may be of order 1 Hz whereas in some point-contact microwave devices it may be as high as several hundred MHz. Typical GaAs noise spectra had flicker noise corner frequency of order a few MHz. Despite significant improvement in the frequency and power performance of GaAs MESFET's over the years, the noise corner frequency of most of today's commercially available devices is not too different from the 50 MHz reported by Hooper et. al. in 1962 [22]. Measured noise spectra on a Tektronix MESFET are presented to investigate low frequency noise characteristics[32].

In aspects of linear GaAs MESFET circuit applications, there are many advantages of MESFET's but there are also some disadvantages. Depending on the active channel thickness, MESFET may be normally "on" (depletion-mode) or normally "off" (enhancement-mode). The depletion-mode MESFET (D-MESFET) was the most widely used device in the early 1980's for implementing GaAs IC's. D-MESFET's demonstrate

good performance characteristics but typically require two power supply voltages. They also require voltage level shifters to generate the negative voltages needed for switching from the positive drain voltages of the n-channel MESFET. This, of course, means support circuitry and another constraining factor for large scale integration.

In the enhancement-mode, the depletion layer is very thin and the current voltage characteristic is drastically affected. For a minor change in gate voltages above a certain voltage, about 0.5 V, the device begins to draw very high currents. This leads to very limited allowable logic swings and a poor device for switching control. The power MESFET, a modification used in power transfer where very high current flow is expected, has been recently found to have a strange drawback[8]. There have been reports of degradation of the performance characteristics due to light emissions at reverse biasing of these devices.

As GaAs technology has matured, analog IC design is the last bastion of GaAs, now that silicon dominates the digital applications[23]. This development suggests that a number of the precision analog MSI and LSI techniques successfully developed for silicon technology may also be applicable, with appropriate modifications, to GaAs technology. These circuits include operational amplifiers, switched-capacitor filters, A/D and D/A converters, and large-signal multipliers.

To insure future system integration, high-speed (100 MHz - 3 GHz) analog circuits should be fabricated in a technology which can achieve high density. Although the semi-insulating substrate in GaAs technology may improve device speed, it also increases wire-to-wire coupling capacitance which jeopardizes circuit density. Silicon, on the other hand, offers low cost, higher level integration, and better low frequency device characteristics. It has been dominant in analog circuits below 100 MHz bandwidth.

However, in spite of 1/f noise and unexpected low frequency effects, GaAs analog circuits above 1 GHz are a practical alternative for high-speed applications. As a linear IC design example, a 3-stage GaAs operational amplifier has been designed with the self-backgating MESFET model using a conventional half micron MESFET technology. Low frequency anomalies in conventional MESFET technologies have been problematic in the application of MESFET's in linear integrated circuits. Some of the effects observed in this GaAs operational amplifier are output current lag, long term transients in the time domain, and a gain roll-off and phase notch in the frequency domain. Using the new self-backgating MESFET model, the low frequency anomalies of this operational amplifier can be accurately predicted than with any other previous model.

OUTLINE OF THE THESIS

The objectives of the study described in this thesis are:

A. To characterize the anomalous effects in the low frequency range (DC to 300 Hz) comparing measured data and calculated model data to find the limitations of conventional GaAs MESFET's.

B. To develop a complete conventional GaAs MESFET model including deep-level trap effects using an analytical approach to determine the potential of GaAs MESFET technology at the different bias points of operation and the various applied signal levels for linear integrated circuit design.

C. To demonstrate the performance of a linear GaAs IC, which have been designed as a test vehicle using this new MESFET model and by using both simulation and measured data and to present design strategies for linear integrated circuits and comparing these to silicon technology to assess future high-speed GaAs applications.

This thesis consists of five chapters including this introductory chapter. In the second chapter, the anomalous characteristic analysis of conventional GaAs MESFET's is presented. Anomalies caused by deep-level traps in GaAs MESFET's such as a self-backgating, a drain current lag, etc. are addressed to investigate some persistent limitations in current GaAs technology. This provides more

precise knowledge of deep-level trap(EL2) effects in the channel and the semi-insulating substrate for modeling low frequency anomalies in GaAs MESFET's.

In the third chapter, the various new analytical models are proposed for predicting accurate conventional GaAs MESFET operations in a wide range of DC bias and applied signal frequency. A time dependent current-voltage model, a voltage dependent capacitance model, and a mobile carrier profile dependent subthreshold current model are presented for linear GaAs circuit design. Scattering parameter dependence on a transit time delay and a nonlinear large signal model are also described in detail for microwave GaAs circuit design. To test the accuracy of developed models, the computed model data has been compared with measured data at the end of each section.

In the fourth chapter, the utility of the self-backgating MESFET model developed in chapter 3 is demonstrated by simulation of and comparison to measured circuit anomalies of a 3-stage GaAs operational amplifier. Analog opamp design techniques are discussed by presenting several amplifier schemes for gain enhancement and high-performance current mirror circuits. The results and discussion are included at the end of chapter 4.

The last chapter includes conclusions and some suggestions for further research which might be more challenging than the aspects of this study.

CHAPTER 2

GaAs MESFET ANOMALOUS CHARACTERISTICS

2.1 INTRODUCTION

Early efforts to achieve the potential of GaAs MESFET technology were frustrated by some persistent limitations such as low frequency anomalies and higher levels of low frequency noise. The presence of the deep-level trap(EL2) in the conventional GaAs MESFET technologies causes anomalies[1,9,11]. Many low frequency anomalies discovered in GaAs MESFET's have been reported[9-14].

Typical low frequency anomalies observed in GaAs MESFET's have been referred to as (1) a self-backgating effect, (2) a drain lag effect, (3) frequency dependent output conductance, (4) hysteresis and oscillations, and (5) low frequency noise. These anomalies are mainly related to the deep-level trapping when electrons are scattered into traps at the edges of the Schottky gate junction and the channel/substrate junction. The physical origin and the electrical influence of these effects are investigated to find limitations to the performance of GaAs IC's.

2.2 THE ANALYSIS

2.2.1 Self-Backgating Effect

A self-backgating effect is very closely related to deep-level traps(EL2) in the channel and the bulk semi-insulating substrate. The starting material for MESFET's is

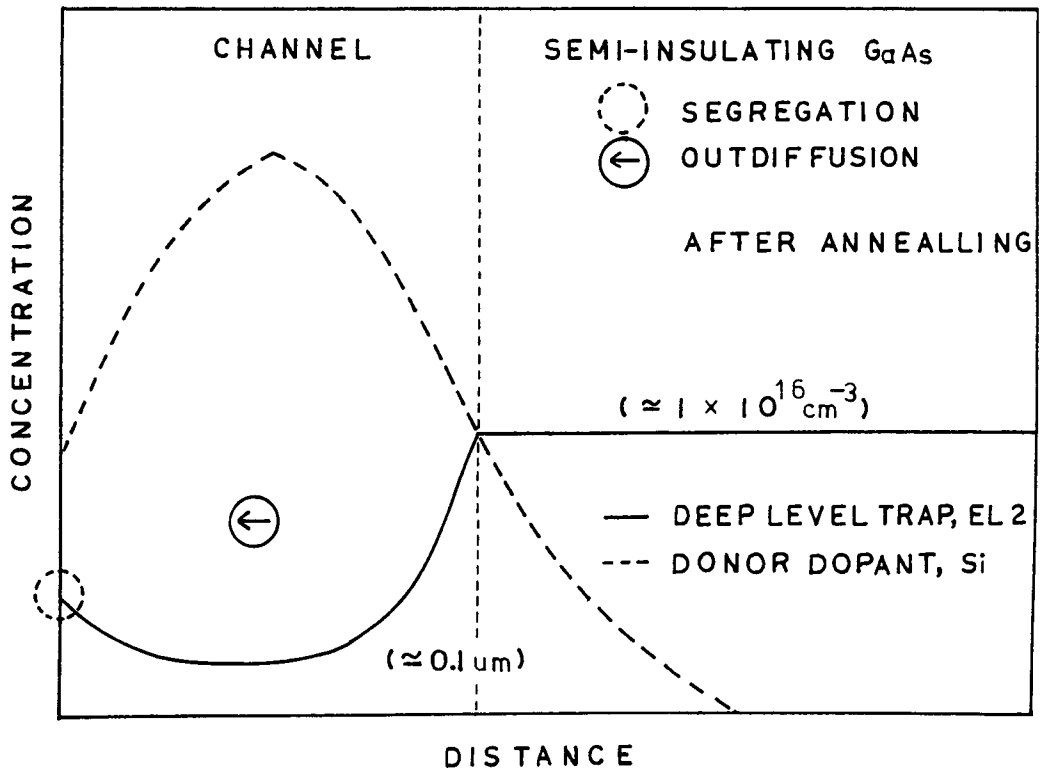


Fig. 2.1. The typical deep-level trap, EL2, and ion-implanting Si donor doping profiles both in the active channel and in the semi-insulating GaAs substrate after annealing.

a high purity GaAs semi-insulating substrate manufactured using the Liquid Encapsulated Czochralski(LEC) technique under arsenic rich conditions. These conditions favor the formation of the deep-level trap(EL2) which compensates the slightly p-type GaAs and produces semi-insulating material[40-42,48]. In a conventional GaAs MESFET technology, the active layer is normally formed by ion-implanting donor atoms(Si) for the n-type channel into the semi-insulating GaAs substrate with the EL2 concentration of 1 x 10^{16} cm^{-3}. The EL2 both in the active layer and in the substrate plays a key role in controlling many of the critical device parameters, in particular, frequency

dependent output conductance(g_{ds}) and frequency dependent transconductance(g_m). The optimization of EL2 is a technologically difficult task. Since an ion implantation often damages the native crystal lattice of a GaAs wafer, a number of deep-levels can be created both in the channel region and quite possibly in the substrate material in addition to those already present in the semi-insulating GaAs substrate. Fig. 2.1 shows the typical deep-level trap, EL2, and ion-implanting Si donor doping profiles both in the active layer and in the semi-insulating GaAs substrate after annealing. The annealing process step can reduce EL2 concentration in the active layer as a result of the outdiffusion and segregation of some of the deep-levels presented originally in the semi-insulating GaAs substrate.

Therefore, it is assumed that the EL2 concentration, a kind of lattice defect, As on Ga anti-site, is a constant in the back-gate region and the EL2 concentration in the active layer is quite low compared to Si dopant concentration in the ion implantation technology currently in use, as shown in Fig. 2.1. A deep donor level(EL2) is located just below the intrinsic mid-gap Fermi-level with a concentration of N_{EL2}. Fig. 2.2 shows the depletion regions and charge distribution of the self-backgating GaAs MESFET. The time dependent net negative charge concentration in the substrate (N^-_{teff}) and time dependent ionized positive charge concentration at the edges of depletion regions(N^+_{EL2}) at equilibrium are given by[43,44]:

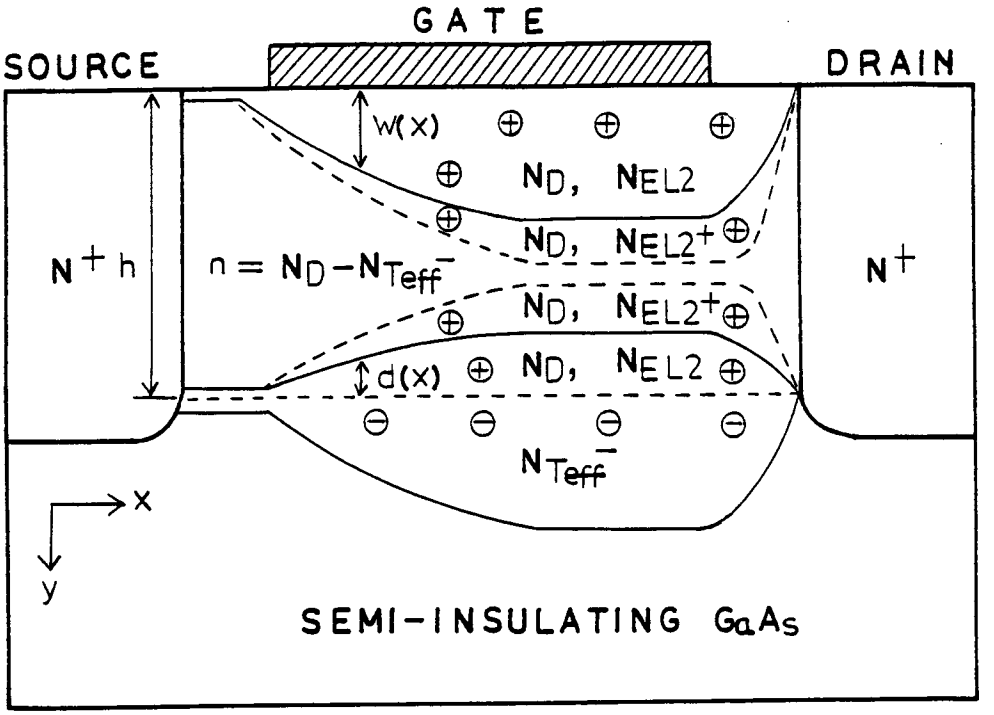


Fig. 2.2. The depletion regions and charge distribution of the self-backgating GaAs MESFET.

$$N^-_{teff} = N_{EL2}\left[\frac{e_{pel2}}{e_{pel2}+e_{nel2}} - \frac{1}{1+0.5\,e^{(E_{EL2}-E_f)/kT}}\right]\left[1-e^{-t/R_bC_b}\right] \quad (1)$$

$$N^+_{EL2} = N_{EL2}\left[1-\frac{1}{1+0.5\,e^{(E_{EL2}-E_F)/kT}}\right]e^{-t/R_bC_b} \quad (2)$$

where, e_{pel2} and e_{nel2} are emission rates for holes and electrons from the EL2 level, respectively, and R_bC_b is an effective time constant modeling the semi-insulating substrate. The time, t, is inversely proportional to the applied AC signal frequency, f. At low frequencies (DC, $t=\infty$), the electron in the channel will be trapped into ionized EL2 deep donors in the semi-insulating substrate causing pinch-off of the channel from the back side. This effect is so-called self-backgating effect. Therefore, this causes a

reduced thickness of the channel, maximized N^-_{teff} in the substrate, and a variation of N^+_{EL2} at the edge of the channel/substrate junction to allow for a corresponding fixed positive charge (N_D, N_{EL2}) for back side depletion region formation as shown in Fig. 2.2.

The time dependent terms of equations (1) and (2) can be derived by the rate equation of electron emission and R_bC_b relates to the electron capture rate and electron trap density in the substrate. Since a sidegating effect can be controlled by separating device to device spacings by more than 1 μm for 1 V power supply voltage on the layout and by isolation techniques in the process, a self-backgating effect which causes channel/substrate modulation becomes essential in modeling a floating backgating MESFET.

The self-backgating transconductance can be defined by the fraction of the transconductance which is contributed by feedback voltage between the self-backgating internal terminal to the source(V_{bs}). The self-backgating low frequency transconductance(g_{mbs}) can be defined as

$$g_{mbs} = \frac{dI_{ds}}{dV_{bs}} \Big| V_{ds} = \text{const}, V_{gs} = \text{const}. \qquad (3)$$

This is also a parasitic low frequency transconductance induced between the channel and the semi-insulating substrate.

2.2.2 **Current Lag Effect**

Makram-Ebeid et. al.[11] have proposed a mechanism to account for a drain lag effect in pulsed gate experiments on

MESFET's. Suppose that an ideal input pulse waveform is applied to a GaAs MESFET inverter, the initial rise time of the inverter is short but then a second time constant on the order of milliseconds appears to produce a long transient lag in the output waveform. Since this is a current lag in the time domain, this effect may also be accounted for by frequency dispersion. A drain lag effect is closely related to the semi-insulating substrate-induced spreading resistances and capacitances.

They depend on the capture and thermal reemission of carriers from these deep-level trapping sites and are functions of temperature and voltage. Voltage changes at the drain can modulate the channel/substrate junction through

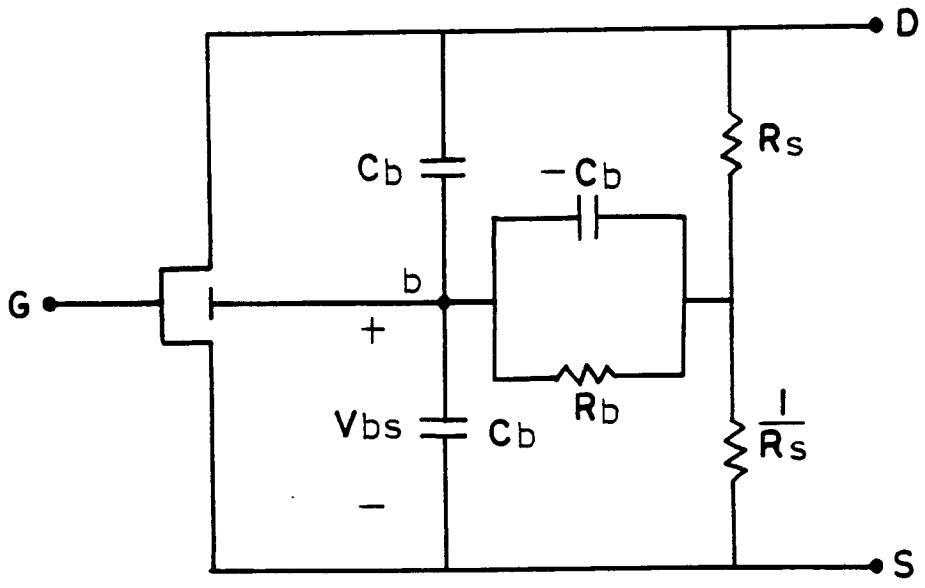


Fig. 2.3. A self-backgating GaAs MESFET equivalent 3-terminal circuit model.

the semi-insulating substrate-induced spreading resistances and capacitances with multiple time constants. The time constants associated with these traps depend on the frequency and the amplitude of the electric field in the channel. Under high field conditions, electrons are injected from the channel to the interface depletion regions. They are trapped when V_{ds} is increased and are reemitted when V_{ds} is decreased as long as the time transients are not shorter than the trap time constants. The drain lag effect is therefore a combination of electron injection and electron trapping[33].

Even though there are multiple time constants in the substrate, a single time constant is used, in which the RC

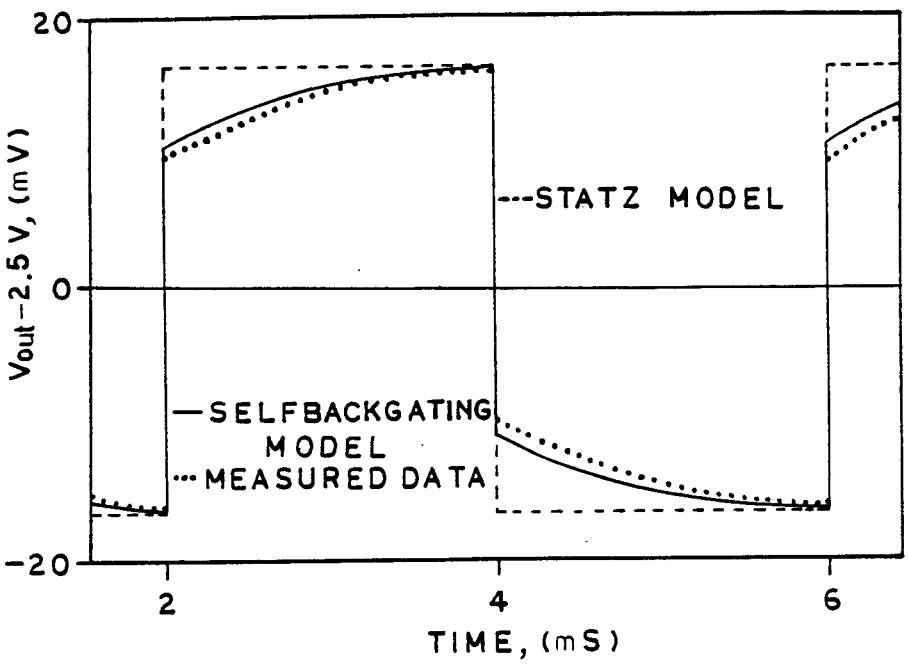


Fig 2.4. A drain lag effect in a step response of a GaAs linear inverter.

network consists of an effective substrate induced resistance and capacitance as shown in Fig. 2.3. The RC network description implies a capacitive and resistive coupling from the drain terminal to the internal self-backgate. By making $R_b = 0$ or a small conducting P substrate, the drain lag and self-backgating effects disappear. By setting $R_b = \infty$, a perfect insulating substrate, the self-backgating extends from DC to infinite frequency and the drain lag effect dominates with a very long setting tail in the transient response.

From the measured output conductance variation or by measuring the duration of a long setting tail in the time domain when an ideal step pulse is applied, values of R_b = 1 GΩ and C_b = 1.6 pF are obtained with a time constant of 1.6 msec. These parameters, R_b and C_b, can be adjusted as a variation of temperature affects the low frequency response. The RC circuit branch guarantees not to allow current flowing from drain to source through the semi-insulating substrate in the OFF state. Fig. 2.4 shows a drain lag effect in a step response of a GaAs linear inverter.

2.2.3 **Frequency Dependent Output Conductance**

When a GaAs MESFET with deep electron traps has a high drain bias applied, a charge will be developed between drain and source to support the electric field existing in the semi-insulating substrate. The electric field establishes positive charge on the drain side and negative charge around

the channel/substrate interface at the source end. This negative charge will increase the drain-to-source conductance in the saturation region[15,35].

The semi-insulating substrate is in fact filled with deep-level traps. The electrons will be injected from the source toward the drain. This injection of electrons will be limited by the accumulation of electrons at the trapping centers in the substrate below the source. This charge accumulation near the source will prevent a rise in output conductance at the low frequency. However, at the high

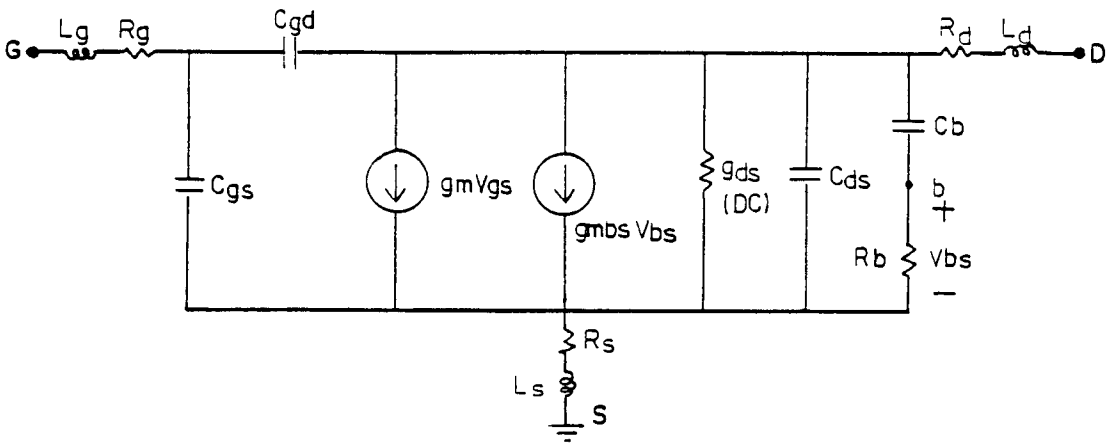


Fig. 2.5. A small-signal AC MESFET equivalent circuit model including a simple RC network for a self-backgating and a drain lag effect.

frequency, the traps in the substrate cannot respond quickly enough to the variation of the drain to source voltage. As a result, the drain-to-source conductance will be higher than that at the low frequency. Also it could be accounted for in

terms of an electrostatic feedback effect between the drain and the source of the MESFET via the bulk semi-insulating substrate, modulated by the capture and thermal emission of free electrons by defect centers residing near the channel/substrate interface region[34].

Fig. 2.5 shows a small-signal AC MESFET equivalent circuit model including a simple RC network for a self-backgating feedback and a drain lag effect. By calculation of the output admittance looking into the output port in Fig. 2.5, the frequency dependent output conductance ratio for a small signal input is given by[10,16]

$$\frac{G_{ds}(f)}{G_{ds}(o)} = \left\{ (g_{ds}(DC) + g_{mbs} + g_{bs}) \frac{f + f_\ell}{f + f_h} + 2\pi f C_{ds} \right\} / g_{ds}(DC) \qquad (4)$$

where,

$$g_{bs} = 1/R_b \ ,$$

$$f_\ell = 1/(2\pi R_b C_b) \ , \qquad f_h = \frac{1}{2\pi R_b C_b (1 + (g_{mbs}+g_{bs})/g_{ds})} \ .$$

Here, it is assumed that the gate is loaded with a very low external impedance compared to $1/\omega C_{gs}$ and neglecting the feedback effect of C_{gd} and the parasitic elements. This frequency dependent expression exhibits a one-pole and one-zero response below the bandwidth frequency(f_b) and can be interpreted with low frequency conductance and frequency dependent terms by trapping channel electrons into the substrate as described earlier.

Fig. 2.6 shows an output conductance comparison between measured data and computed model data as a function of frequency. Equation (4) can be interpreted with respect to the self-backgating three terminal MESFET model parameters in the following way. In the DC case, there is no feedback voltage, $V_{bs}(DC) = 0$, from the self-backgate. Also, the g_{bs} can be neglected because the substrate dielectric relaxation time constant is on the order of milliseconds and the anomalous effects are certainly within the bandwidth of the transistor. The output conductance at DC, $(G_{ds}(DC))$, is given by equation (4) as

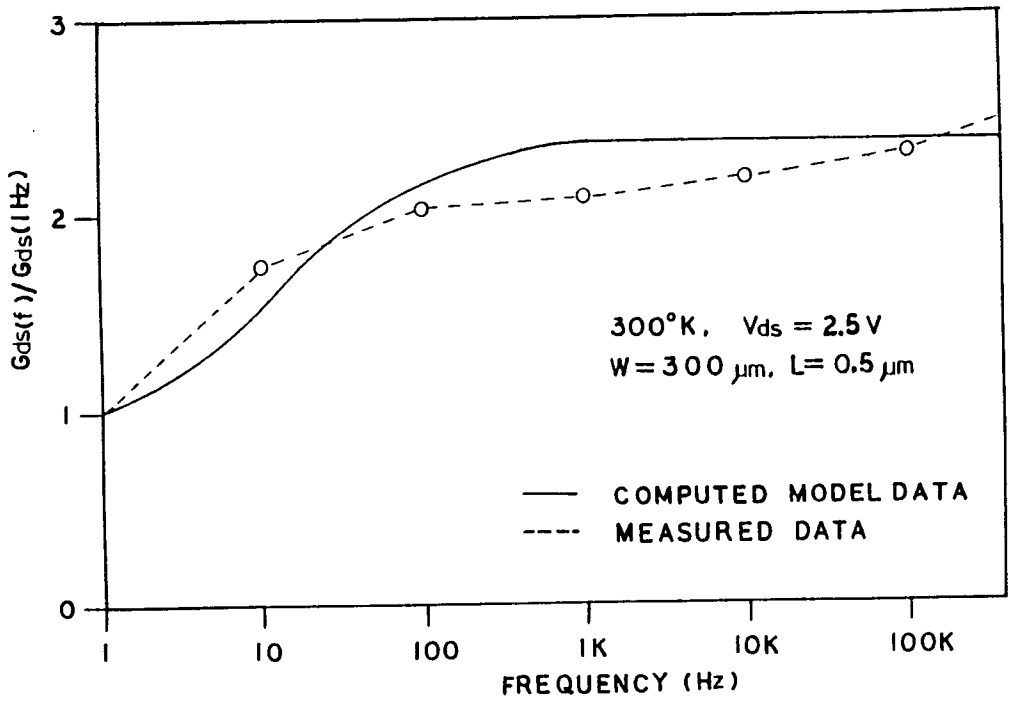


Fig. 2.6. An output conductance comparison between measured data and computed model data as a function of frequency.

$$G_{ds}(DC) = g_{ds}(DC), \qquad \text{for } f = 0 \qquad (5)$$

In the AC case for frequencies higher than the low frequency

effects(f_1) and up to the bandwidth frequency(f_b), the output conductance at AC, $G_{ds}(AC)$, is given by equation (4) as

$$G_{ds}(AC) = g_{ds}(DC) + g_{mbs}, \qquad \text{for } f_1 < f < f_b \qquad (6)$$

As the signal frequency approaches infinity above f_b, $G_{ds}(AC)$ is given by equation (4) as

$$G_{ds}(AC) = j2\pi f C_{ds}, \qquad \text{for } f_b < f < \infty \qquad (7)$$

Here, g_{mbs} can be interpreted with the output conductance difference between DC and AC by the self-backgating effect at the channel/substrate junction interface.

The output conductance variation, $G_{ds}(f)/G_{ds}(0)$, arises mainly from the channel/substrate junction which is a self-backgating effect which reduces the effective channel length 2.5 times more at the high frequency than at the low frequency. In the example given here the value of output conductance is 1.33 mS for the high frequency range for a GaAs MESFET with W = 300 μm and L = 0.5 μm.

2.2.4 **Frequency Dependent Transconductance**

The trapped carriers in deep-level traps cause a drop in the intrinsic transconductance, g_m, at the high frequencies. The dispersion in g_m of MESFET's could be considered as a low-pass filter type response which is caused by the presence of deep traps and surface states. Since surface states can be reduced by the gate recess and the surface p-type region, the deep level in the channel is

an important factor in determining the intrinsic transconductance in MESFET's.

For a fixed value V_{ds} and a small variation of V_{gs}, the transconductance g_m is defined as

$$g_m = \frac{dI_{ds}}{dV_{gs}} \Big| V_{ds} = \text{const.} \tag{8}$$

A variation of V_{gs} causes a change in the depletion width at the edge of the Schottky gate junction and a constant V_{ds}(DC) prevents the channel/substrate junction modulation. Therefore, the intrinsic transconductance of MESFET relates mainly to the boundary between the Schottky gate junction and the channel.

At the low frequency, deep-level traps at the edge of the Schottky gate junction emit electrons at an exponential rate because slow gate voltage variations shift the Fermi-level below the trap level. The charge variation of the Schottky gate junction depletion edge in the low frequency is given by:

$$\Delta Q_{lf} = [2q \epsilon (N_D + N^+_{EL2}) V_{\Delta w}]^{1/2} \tag{9}$$

where, $V_{\Delta w}$ is a voltage drop of changed depletion width at the edge of the Schottky gate junction. Since, at the high frequency, deep-level traps can not response quickly to the applied high frequency gate signal, the charge variation of the Schottky gate junction depletion region in the high frequency is given by:

$$\Delta Q_{hf} = [2q \epsilon N_D V_{\Delta w}]^{1/2} \tag{10}$$

If parasitic elements are neglected, then, the incremental drain current variation(ΔI_{ds}) is proportional to the charge variation of the Schottky gate junction depletion region. Therefore, the transconductance variation, $G_m(f)/G_m(o)$, can be derived by equations (9) and (10) as

$$\frac{G_m(f)}{G_m(0)} = \frac{\Delta Q_{hf}}{\Delta Q_{lf}} . \tag{11}$$

From equation (2), $N^+_{EL2} = N_{EL2} \exp(-t/R_bC_b)$, equation (11) can be converted into the frequency domain using a Laplace transformation as follows:

$$\frac{G_m(f)}{G_m(o)} = \sqrt{\frac{N_D}{N_D + N^+_{EL2}}} = \left[1 + \frac{N_{EL2}}{N_D\sqrt{1 + (f_\ell/f)^2}}\right]^{-1/2} \tag{12}$$

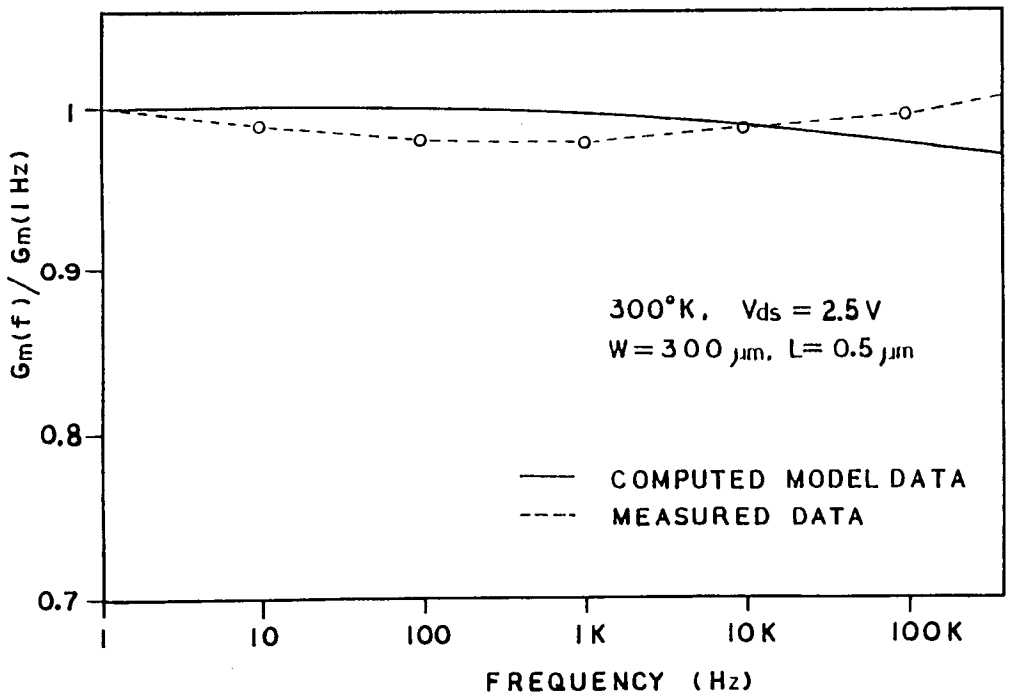


Fig. 2.7. A transconductance comparison between measured data and model data as a function of frequency.

Since the peak of the ion implantation doping profile is normally located near the center of the channel, N_{EL2} is much less than N_D. Therefore, this analysis predicts a smaller variation of $G_m(f)$ than that of $G_{ds}(f)$ under the normal bias condition. Fig. 2.7 shows a transconductance comparison between measured data and computed model data as a function of frequency. The transconductance variation, $G_m(f)/G_m(0)$, due to electron emission from EL2 in the depletion width change at the edge of the Schottky gate junction is negligible at room temperature.

2.2.5 **Hysteresis and Oscillation**

Hysteresis, a looping effect, occurs in the saturation region. GaAs MESFET's can exhibit hysteresis as a drift in the current with time and a change in the drain current as a result of a change in the self-backgating bias in the transient analysis. Typically, the origin of hysteresis is an electron trapping on EL2 levels at the semi-insulating substrate region interface[19]. A drain current tends to increase with EL2 ionization and decrease with EL2 trapping. This effect is strongly temperature and frequency dependent.

Fig. 2.8 shows a hysteresis characteristic comparison between measured data and simulated data using the transient analysis option and a small-signal AC MESFET equivalent circuit model as shown in Fig. 2.5. As expected, the simulation has shown hysteresis in the saturation region similar to the measured I-V curve. The hysteresis is

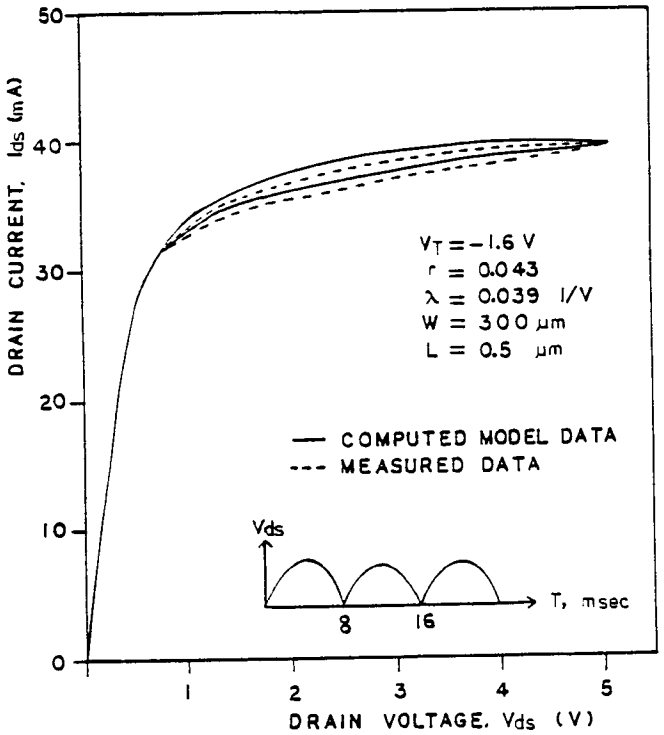


Fig. 2.8. A hysteresis characteristic comparison between measured data and simulated data using the transient analysis option.

drastically reduced when the amplitude of the drain-to-source voltage is limited to less than 1 V [36].

A low frequency oscillation can also occur in MESFET's with large metal drain pads that lie directly on the semi-insulating substrate[37]. Generally, the low frequency oscillations result from the field-enhanced capture of electrons by deep-level traps. The charge domains established by trapping move with a velocity dependent upon the current density and the time constant of the trap involved[13,14,38]. The frequency of the current oscillation is determined by the transit time of high field domains traveling between an electron injecting a drain and a source on the semi-insulating GaAs. Low frequency oscillations

observed in GaAs MESFET's are attributed to the high-field tunneling of electrons into traps in the Schottky gate depletion region and also attributed to the current oscillation associated with the release of electrons from the deep-level traps(EL2) in the substrate.

2.2.6 **Low Frequency Noise**

An excessive low frequency noise observed in GaAs MESFET's is one of the limitations for linear and microwave circuit applications. In particular, this severely limits the nonlinear microwave circuits such as oscillators and mixers, where a low frequency noise upconverts to become excessive. The origins of low frequency noise, flicker noise, in GaAs MESFET's have not been determined, although many mechanisms have been proposed. Some of the suggested origins are surface states, mobility fluctuations, bulk traps, a metal semiconductor interface, a channel/substrate interface, carrier number fluctuations, and an inter-valley transfer of hot carriers[19-22].

However, the low frequency noise in GaAs MESFET's originates mainly from two sources; one is surface related and the other is substrate related. The surface related low frequency noise is caused by trapping of electrons by surface states. The free surface region between the source and the gate, and that between the drain and the gate, may contribute to the low frequency noise via the fluctuation in the occupancy of the surface states present[19]. Smaller

gate length(L) produces more low frequency noise in GaAs MESFET's[18]. The substrate related noise is due to the deep-level trap at the channel/substrate interface. A fluctuation of the occupancy of deep-level trap(EL2) in the depletion regions of the Schottky gate junction and the channel/substrate junction is associated with long time constants and can contribute to a low frequency noise.

A GaAs MESFET in thermal equilibrium is directly subject to the laws of thermodynamics and its noise output is solely Johnson noise with a white spectrum. Thus, flicker noise can only occur in non-equilibrium situations in a GaAs MESFET subjected to applied bias voltages derived from a signal. A GaAs MESFET also generates a generation and recombination(g-r) noise which is characterized by a single trapping level. A g-r power spectrum which has a Lorenzian distribution is given by[45,48]

$$H(f)_{g-r} = 4\,\tau_o/(1 + 2\pi f\,\tau_o)^2 \qquad (13)$$

where, τ_o is a relaxation time involving a single trapping level. At low frequencies, this gives $H(f)_{g-r}$ varying as $1/f^2$ rather than as $1/f$, and so flicker noise cannot be explained in terms of noise processes associated with any single relaxation time.

If majority carrier conduction processes are dominant, the g-r of minority carriers has little effect. However, in depletion regions of the Schottky gate junction and channel/substrate junction, the fluctuation of minority

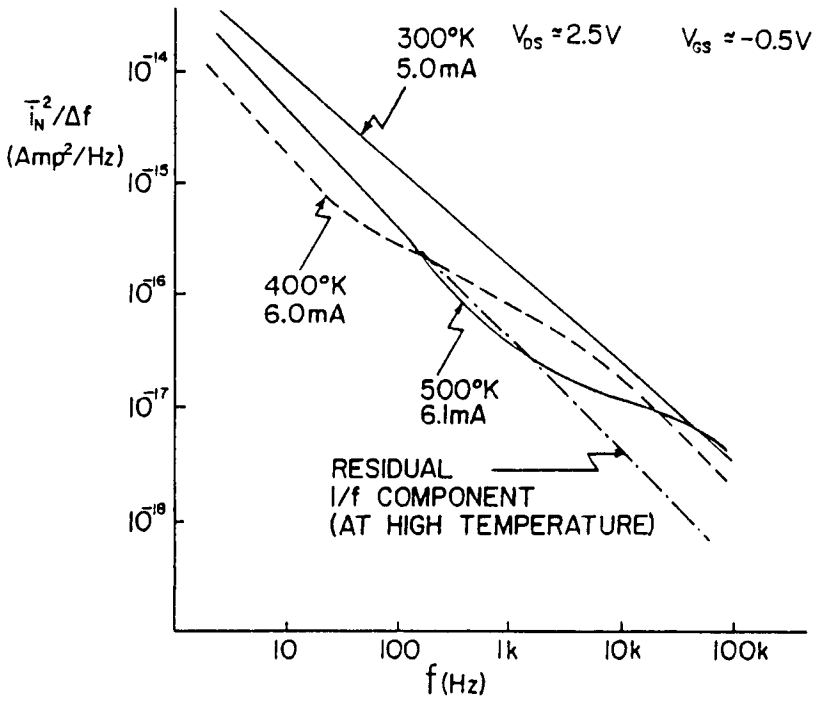


Fig. 2.9. Measured noise spectra on a Tektronix MESFET[32].

carriers has an appreciable effect on the potential distribution and produces a modulation of channel current in GaAs MESFET's. Generation-recombination noise or trapping noise is not easily identifiable in most measurements on GaAs MESFET's.

From the Hooge's experiment, a 1/f noise power spectrum which is proportional to 1/f is given by[46]

$$H(f)_{1/f} = \alpha/f \tag{14}$$

where, α is a Hooge's constant. A 1/f component in GaAs MESFET's is probably associated with surface states both outside and within the gate, and one which is peculiarly independent of temperature.

To derive an analytical 1/f noise power spectrum of GaAs MESFET's is very complicated but the carrier number fluctuation model[47] based on the carrier density fluctuations is generally accepted among other previous models. Fig. 2.9 shows measured noise spectra on the Tektronix MESFET[32]. The 1/f noise corner frequency of a MESFET is approximately 100 MHz for GaAs IC's. This is attributed to the well-known low thermal noise floor of GaAs MESFET's and the intrinsic high 1/f noise level in GaAs devices. A variety of physical mechanisms account for the high level of 1/f noise, including high trap density, short gate length, and low electron effective mass. To reduce low frequency anomalies and an excessive 1/f noise in GaAs MESFET's, several techniques have been attempted for fabricating noise hardness substrates such as a horizontal Bridgman wafer, and by modifying device structures such as a buried channel MESFET developed by L. Forbes, et. al.[32, 43]. In device layouts, low frequency noise can be also reduced by increasing the size of MESFET's at the expense of increasing power dissipation.

2.3 CONCLUDING REMARKS

The optimization of the EL2 concentration in a high purity semi-insulating GaAs substrate manufactured using the LEC technique might be useful for the improvement of the frequency dependent characteristics of conventional GaAs MESFET's as a result of the EL2 concentration reduction in

the active layer. Although there are some controversies in solving this problem, some of the techniques for optimizing EL2 are the heat treatment to anneal out deep-level traps in the active layer and the use of a uniformly doped epitaxial layer grown by the Molecular Beam Epitaxy(MBE) on the semi-insulating GaAs substrate.

First, the annealing of the active layer is a crucial process in which a surface preparation and an anneal cap deposition determine directly the uniformity of the active layer to optimize EL2 concentration. Deep-level traps tend to outdiffuse during annealing up to the surface, which implies that most of the low frequency anomalies are related to the surface and/or to the channel/substrate interface.

Second, the high quality epitaxial layer on the semi-insulating GaAs substrate can allow lower deep-level trap concentration as well as uniformly doped impurity concentration in the active layer. However, unlike the ion implantation technology currently in use, this technique has not yet been employed in the mass production of GaAs integrated circuits. The reason is that a major limitation of MBE and to a lesser degree that of other epitaxial deposition techniques is their relatively low throughput rates compared to the well established implantation technology.

Also, the change of the device structure can reduce low frequency anomalies as described earlier. The p-layer of a buried channel MESFET which forms a high barrier interface

with the n-channel has been shown not only to improve the output conductance and the low frequency channel noise, but also to eliminate a drain lag effect by L. Forbes et. al.[43]. A more advanced device is the GaAs p-well MESFET to reduce a sidegating effect. This device is achieved using a buried-channel structure within a p-well by implanting a p-type dopant behind a channel and a shallow p-type implanted region on the surface.

Since GaAs the p-well MESFET is isolated from surfaces by the shallow p-type region and the semi-insulating substrate, the channel is no longer influenced by traps associated with these regions and is free of transients following gate bias and/or drain bias changes, excess generation-recombination noise, and other phenomena related to deep-level trapping[32]. By adding a p-well to a buried channel MESFET, the p-well also plays an important role in reducing leakage current to the substrate and the backgating effect which is a decrease in drain current due to a narrowed conduction region in the channel as the negative backgate bias increases.

However, there are some difficulties that lead a low yield in the process and it requires p-well contacts which limit the application of the GaAs gate array design. Recently, improved interfaces have also been demonstrated with an undoped buffer layer or even an AlGaAs buried layer to eliminate a backgating effect and a light sensitivity. However, these solutions are not compatible with a fully-

implanted process. Therefore, a conventional GaAs MESFET discussed in this study might be the most appropriate candidate to achieve the potential of current GaAs IC's applications.

CHAPTER 3

NEW ANALYTICAL GaAs MESFET CIRCUIT MODELS

3.1 INTRODUCTION

A rapid development of GaAs integrated circuit technology requires the development of an accurate and simple device model for GaAs MESFET's. The purpose of developing such an equivalent circuit model of a GaAs MESFET is to provide an accurate simulation CAD tool for predicting, optimizing, and evaluating performances of linear integrated circuits. This requires an analysis of the physical phenomena involved in the device operation to exactly fix the limits of its use and to be aware of its limitations. The complexity in modeling GaAs MESFET's which have low frequency anomalies, unlike silicon devices, is reflected by the large number of different models in the literature[49-57].

S-parameters of GaAs MESFET's can be measured to extract an equivalent small-signal circuit model. This method, well-adapted to small signal microwave circuit design, can be applied to establish large-signal models for all possible gate and drain biasing conditions. However, this model does not provide some physical aspects of device operation and require the complex optimization routine.

2- or 3-dimensional numerical models are used to solve in each bias point of the device, the general transport equations including nonstationary effects. They are

particularly suitable for ultra-short gate length devices, but their extremely high CPU time requirements are making them practically unusable even for SSI digital IC simulation [56,58,59].

The presence of the deep-level trap(EL2) in conventional MESFET technologies causes the anomalies of self-backgating, drain current lag, hysteresis, and oscillation in the low frequency operation of MESFET's. Few attempts have been made to incorporate these except a self-backgating effect into circuit simulators in GaAs MESFET's linear and microwave circuit design[16]. Also, little attention is usually paid to well fitted DC I-V characteristics in an analytical model and the low frequency behaviour of the output conductance. A simple RC network can account for this effect in a first order approximation.

One of the principal limitations has been lack of an accepted technique for including self-backgating effects. For the implementation of this model into PSPICE, a time dependent threshold voltage including this self-backgating effect has been developed based on modification of the Statz DC model. an analytical approach has been used for the capacitance model which describes the dependence on V_{gs} and V_{ds} by driving the stored charge in the linear, saturation, and pinch-off regions. The model is one which also includes the channel/substrate junction modulation by changes of the drain-to-source voltage.

Also, for describing high-speed switching performance in the linear IC applications, an analytical subthreshold current model for a self-backgating GaAs MESFET has been included in this chapter. S-parameter errors between previous models and measured data in conventional GaAs MESFET's have been reduced by including a transit time delay in the transconductances, g_m and g_{mbs}, in the well-defined self-backgating MESFET model. As a convenient test vehicle, the new test fixture is also proposed for extracting simulated S-parameters which accurately predict measured data. Finally, a nonlinear large-signal model is discussed for MMIC designs. The proposed self-backgating model has been focused on providing a new GaAs MESFET model for PSPICE for linear and microwave circuit design and one which includes deep-level trap effects.

3.2 THE NEW MODELS

3.2.1 Current-Voltage Curve Model

The most important features of the current-voltage curve model are an accurate description of the drain current in the saturation region and the drain-to-source voltage required at the onset of current saturation. One of the difficulties in modeling the current-voltage characteristics is that the saturation drain current and hysteresis are functions of frequency and temperature.

Several authors have suggested GaAs MESFET's models to incorporate in the SPICE circuit simulator. A JFET model

developed by Schichman-Hodges has been most widely used to simulate GaAs MESFET's circuits. The drain current voltage relationship of the JFET model is given by[58]

$$I_{ds} = \beta[2(V_{gs} - V_t) - V_{ds}]V_{ds}(1 + \lambda V_{ds}), \quad \text{for } V_{ds} < (V_{gs} - V_t) \qquad (1)$$

$$I_{ds} = \beta(V_{gs} - V_t)^2(1 + \lambda V_{ds}), \text{ for } V_{ds} > (V_{gs} - V_t). \qquad (2)$$

However, this model has a number of drawbacks for accurate prediction of the circuit behavior over widely varying values of I_{dss} and V_{ds} even though it works moderately well in the design of GaAs MESFET analog circuits when the GaAs MESFET is operated near a saturated current, I_{dss}. Another crucial drawback in analog circuit designs is that we can not control accurate g_m, g_{ds}, and I_{dss} simultaneously in SPICE because of its lack of model parameters.

An analytical GaAs MESFET model developed by Curtice employed hyperbolic tangent functions to improve I-V characteristics below saturation[57]. The drain current-voltage relationship of the Curtice model exclusive of parasitic resistances is approximated by

$$I_{ds} = \beta(V_{gs} - V_t)^2(1 + \lambda V_{ds})\tanh(\alpha V_{ds}) \qquad (3)$$

where, β and α are parameters related to the gain factor and channel length modulation similar to these of a

JFET model. "α" is a parameter to adjust the knee zone of the I-V curve where the MESFET moves from the linear region to the saturation region. This model gives an improved description in the knee zone where there are apparent deviations in the JFET model and its equations have continuous DC current and its derivatives(g_m, g_{ds}) for all regions of device operation.

However, even with an arbitrary setting of parameter α, the Curtice model still has difficulties in determining the voltage at which the drain current characteristics saturate. The drawback of the Curtice model is that transconductance is no longer predicted accurately using a square-law relationship between I_{ds} and V_{gs} which is often significantly different than measured data. Based on the Curtice model, the improved I-V curve models are proposed by Mckinley and Larson. The Mckinley model[51] has a current voltage relationship as follows:

$$I_{ds} = \beta(V_{gs} - V_t)^2(1 + \lambda V_{ds})\tanh(\alpha V_{ds}) + V_{ds}/R_{sh} \qquad (4)$$

where,

$$\alpha = \alpha_o \beta (\phi_b - V_t)^2 \frac{1 - [(\phi_b - V_{gs})/(\phi_b - V_t)]^{1/2}}{\beta(V_{gs} - V_t)} \qquad (5)$$

$$R_{sh} = (R_{sho}/2)[\exp\{(V_t - V_{gs})/(\eta kT/q)\} + 1]. \qquad (6)$$

The channel conductance at low drain-to-source voltages of the MESFET is modeled by α as a function of V_{gs} in equation

(5). This effect is due to the decrease in the size of the gate depletion region with increasing V_{gs} which increases channel conductance. In equation (6) for a subthreshold current empirically, R_{sho} is the parasitic drain-to-source shunt resistance at $V_{gs} = V_t$ and η is an empirical parameter similar to an ideality factor.

The other model based on modifications of the Curtice model is the Larson model[27] as follows:

$$I_{ds} = \beta(1 + \lambda kV_{ds})k(1/q)^q[(1 + q)(V_{gs} - V_t) - kV_{ds}]^q, \quad \text{for } V_{gs} - V_t > kV_{ds} \tag{7}$$

$$I_{ds} = \beta(1 + \lambda kV_{ds})(V_{gs} - V_t)^{1+q}, \quad \text{for } V_{gs} - V_t < kV_{ds} \tag{8}$$

where, q models the exponential dependence of I_{ds} with V_{gs} and exhibits square-law behavior when q = 1. The k models the early saturation phenomenon. However, q and k are empirical model parameters and are difficult to obtain by fitting measured data.

Statz et. al.[58] proposed that the drain current always saturates at the same voltage irrespective of the gate-to-source voltage which is different than conventional JFET or MOSFET models. This early saturation is a result of the fact that carriers in the channel reach the saturation velocity at even small voltage due to the high GaAs carrier mobility and as the channel length(L) is reduced. The Statz model has a current-voltage relationship as follows:

$$I_{ds} = \frac{\beta(V_{gs} - V_t)^2}{1 + B(V_{gs} - V_t)} [1 - (1 - \alpha V_{ds}/3)^3] \lambda (V_{ds} - 3/\alpha)$$

$$\text{for } V_{gs} > V_t,\ V_{ds} < 3/\alpha \qquad (9)$$

$$I_{ds} = \frac{\beta(V_{gs} - V_t)^2}{1 + B(V_{gs} - V_t)} \lambda (V_{ds} - 3/\alpha),$$

$$\text{for } V_{gs} > V_t,\ V_{ds} > 3/\alpha . \qquad (10)$$

The main advantage of the Statz model is to modify the square-law relationship of I_{ds} and V_{gs} by the introduction of a new model parameter, B, to adjust the transconductance without any variations of the output conductance in the saturation region. On the basis of measured data, however, the drain-to-source voltage $V_{ds}(sat)$ does not saturate exactly at the same drain-to-source voltage as the gate-to-source voltage changes. It is important for the I-V curve equation to produce the smooth functions free of discontinuities that could lead to non-convergence in circuit simulators. Statz et. al.[58,67] also proposed the improved DC I-V curve model as follows:

$$I_{ds} = \frac{\beta(V_{gs} - V_t)^2}{1 + B(V_{gs} - V_t)} (1 + \lambda V_{ds}) \tanh(\alpha V_{ds}) . \qquad (11)$$

This equation gives an accurate current and transconductance representation of the device with smooth continuous transitions at the threshold voltage important for convergence of time-domain analysis. However, as described

earlier, frequency dependent $I_{ds}(f)$ and hysteresis observed commonly in conventional GaAs MESFET's are not included in equation (11).

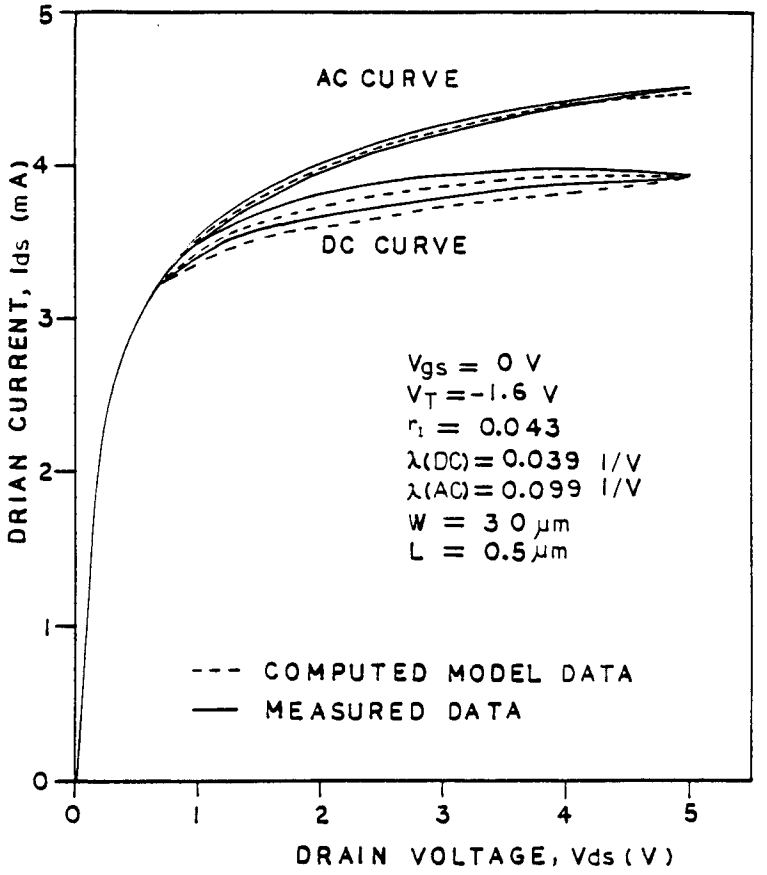


Fig. 3.1. Frequency dependent $I_{ds}(f)$ comparison between measured data and computed model data as a function of frequency

An analytical I-V curve model has been developed by including deep-level trap effects. Using the assumption of a uniform doping profile and a gradual channel approximation with the depletion region formation including the channel/substrate junction as shown in Fig. 2.2, the drain current in the linear region can be expressed as follows[61,62]:

$$I_{ds}(x) = qW(N_D - N^-_{teff})(h - w(x) - d(x))\ \upsilon(x) \qquad (12)$$

where, W is the channel width, h is the channel depth, $N_D - N^-_{teff}$ is the effective channel electron concentration including trapped electrons (N^-_{teff}) from the channel to the substrate at the low frequency, d(x) is the depletion region width toward a channel from the channel/substrate junction interface, and w(x) is the depletion region width at the Schottky gate junction.

$$d(x) = \left[\frac{2\epsilon\ R}{q(N_D+N_{EL2})}\ (V(x)+V_b)\right]^{1/2} \qquad (13)$$

$$w(x) = \left[\frac{2\epsilon}{q(N_D+N_{EL2})}\ (V(x)+\phi_b-V_{gs})\right]^{1/2} \qquad (14)$$

where, V(x) is the potential at point(x), V_b is the built-in potential of the channel/substrate junction, ϕ_b is the barrier height of the Schottky gate junction, and R is the ratio expressed in terms of N^-_{teff} in the substrate and $N_D + N_{EL2}$ in the depletion region of the active layer from the channel/substrate junction as follows:

$$R = \frac{N^-_{teff}}{N_D + N_{EL2} + N^-_{teff}}\ . \qquad (15)$$

By using a simplified velocity saturation mechanism[7]

$$\upsilon(x) = \frac{\mu E_x}{1+\mu E_x/\upsilon_s} \simeq \frac{\mu E_x}{1+\mu V_{ds}/L\upsilon_s} \qquad (16)$$

where μ is the low field mobility, υ_s is the saturation velocity of the electron in the channel, L is the channel length, and $Ex = dV/dx$ is the longitudinal field in the channel. If the source and the parasitic resistances are neglected, integrating from x = 0 to x = L yields the analytical expression for the I-V curve in the linear region as follows:

$$I_{ds} = \frac{qW\mu(N_D - N_{teff}^-)}{L + \mu Vds/\upsilon_s} \int_o^{V_{ds}} (h - w(x) - d(x))\, dV$$

$$= \frac{A}{L + \mu \frac{V_{ds}}{\upsilon_s}} \left[\frac{V_{ds}}{V_p} - \frac{2}{3} \left(\frac{V_{ds} + \phi_b - V_{gs}}{V_p} \right)^{\frac{3}{2}} + \frac{2}{3} \left(\frac{\phi_b - V_{gs}}{V_p} \right)^{\frac{3}{2}} \right.$$

$$\left. - \frac{2}{3}\sqrt{R} \left\{ \left(\frac{V_{ds} + V_b}{V_p} \right)^{\frac{3}{2}} - \left(\frac{V_b}{V_p} \right)^{\frac{3}{2}} \right\} \right] \qquad (17)$$

where, V_p is the pinch-off voltage and A is a constant as given by:

$$A = \frac{W\mu q\, (N_D + N_{EL2})\, h^3}{2\epsilon} (N_D - N_{teff}^-) \,. \qquad (18)$$

For a given V_{gs}, the maximum current I_{dssat} occurs at the point where the channel is pinched off when $V_{dssat} = V_p - (\phi_b - V_{gs})$. Therefore, I_{dssat} can be obtained at the onset of saturation.

$$I_{dssat} = \frac{A}{3\left\{ L + \frac{\mu V_p}{\upsilon_s} (1-a) \right\}} \left[1 - 3a + 2a^{\frac{3}{2}} - 2\sqrt{R} \left\{ (1-a+b)^{\frac{3}{2}} - b^{\frac{3}{2}} \right\} \right] \qquad (19)$$

where, $a = (\phi_b - V_{gs})/V_p$ and $b = V_b/V_p$. For drain voltages beyond V_{dssat}, we apply a channel length modulation for the output conductance increase with the effective channel(L_{eff}) as given by

$$L_{eff} = L - h\left[\frac{V_{ds}}{V_p} + a - 1\right]^{1/2}. \tag{20}$$

From equations (19) and (20), the analytical expression for the I-V curve in the saturation region is given by

$$I_{ds} = \frac{A\,(1 - 3a + 2a^{3/2})}{3\left\{L_{eff} + \frac{\mu V_p}{v_s}(1-a)\right\}} - \frac{2\sqrt{R}\,A\{(1-a+b)^{3/2} - b^{3/2}\}}{3\left\{L_{eff} + \frac{\mu V_p}{v_s}(1-a)\right\}}. \tag{21}$$

Thus, we can represent equation (21) with the simplified form including deep-level trap effects[1].

$$I_{ds} = I_{ds1} - I_{ds2}\left[\frac{N^-_{teff}}{N_D + N_{EL2} + N^-_{teff}}\right]^{1/2} \tag{22}$$

where, I_{ds1}, the first term of equation (21), is similar to the conventional analytical I-V curve model with a gradual channel approximation and abrupt depletion layer. The second term of equation (22) exhibits the current reduction which can follow the applied signal due to the self-backgating effect at the channel/substrate interface. For a low N^-_{teff}, the self-backgating effect will be minimal.

To implement this time dependent I-V curve model into a circuit simulator with a low pass filter network having time constant R_bC_b as shown in Fig. 2.3, the threshold voltage

dependence on the EL2 concentration is derived as follows[61,62]:

$$|V_t| \simeq |V_{to}| - C\sqrt{N^+_{EL2}} - D\,N^+_{EL2} = |V_{to}| - r_2\sqrt{V_{bs}} - r_1 V_{bs} \qquad (23)$$

where, V_{to} is the threshold voltage without the self-backgating effect and C and D are positive constants related to the channel doping profile and r_1 and r_2 are first- and second-order self-backgating parameters to be determined by measurement. N_{EL2} is dependent on the induced feedback voltage, V_{bs}($\simeq V_{ds}\ \exp(-t/R_bC_b)$) at the internal self-backgating node. Therefore, a model can be developed as a modified Statz DC model including this new threshold voltage with a self-backgating effect[2]:

$$I_{ds} = \frac{\beta(V_{gs} - V_{to} + r_1V_{bs} + r_2\sqrt{V_{bs}})^2}{1 + B(V_{gs} - V_{to} + r_1V_{bs} + r_2\sqrt{V_{bs}})}(1 + \lambda V_{ds})\tanh(\alpha V_{ds}). \qquad (24)$$

This time dependent I-V curve model has been incorporated into PSPICE. The saturation currents $I_{ds}(f)$ for both DC and AC curves as shown in Fig. 3.1 are compared to measured data at 0.1 Hz and 100 kHz. Lower hysteresis and a higher saturation current in the AC curve in comparison to the DC curve are both predicted and observed. If the period of the applied signal is longer than R_bC_b, electrons are trapped when the drain-to-source voltage increases and are reemitted when the drain-to-source voltage decreases. This causes more

hysteresis at low frequency than at high frequency in the I-V curve as shown in Fig. 3.1.

By differentiating equation (24) and using the small-signal AC circuit model as shown in Fig. 2.4, the small signal model parameters can be derived for the saturation region[16].

$$g_m = \frac{dI_{ds}}{dV_{gs}} = \frac{\beta V_{gseff}(2 + BV_{gseff})}{\{1 + BV_{gseff}\}^2}(1 + \lambda V_{ds}) \tag{25}$$

$$g_{mbs} = \frac{dI_{ds}}{dV_{bs}} = (r_1 + r_2/\sqrt{4V_{bs}})\, g_m \tag{26}$$

$$g_{ds}(DC) = \frac{dI_{ds}}{dV_{ds}}\Big|_{V_{bs}=0} = \frac{\beta\lambda(V_{gs} - V_{to})^2}{1 + B(V_{gs} - V_{to})}(1 + \lambda V_{ds}) \tag{27}$$

where g_{mbs} is defined as the self-backgating transconductance, the effective gate voltage is $V_{gseff} = (V_{gs} - V_{to} + r_1 V_{bs} + r_2 V_{bs}^{1/2})$, and $g_{ds}(DC)$ is the low frequency output conductance as shown in Fig. 2.4. The self-backgating parameters, r_1 and r_2, can be found by measuring the output conductance at DC and AC and transconductance at the quiescent V_{gs}, V_{ds}, and time average $V_{bs} = V_{ds}/2$. From equations, (25), (26), and equation (4) in chapter 2,

$$r_1 + r_2/\sqrt{4V_{bs}} = \frac{G_{ds}(AC) - G_{ds}(DC)}{g_m}. \tag{23}$$

Our measured data yields $G_{ds}(DC)$ = 1.33 mS, $G_{ds}(AC)$ = 3.3 mS, and g_m = 45 mS at a typical bias of V_{gs} = 0 and V_{ds} = 2.5 V for a conventional MESFET with W = 300 μm and L =

0.5μm. From this we obtain $r_1 + 0.45r_2 = 0.043$, for example, $r_2 = 0.006$ if $r_1 = 0.04$. By measuring the duration of the long decay observed as a drain lag effect in the transient response or by measuring f_1 in the frequency dependent output conductance curve, the time constant R_bC_b can be obtained with the value of about 1.6 msec, which gives R_b = 1 GΩ and C_b = 1.6 pF.

This large value of R_b allows for the RC network not to appear from drain to source in the pinch-off region. Also, RC model parameters can be adjusted as a variation of temperature affects the low frequency response. However, a single time constant model displays a deeper and narrower phase peak in the simulation of GaAs IC's. This could be improved by employing a more complex filter network whose frequency response more closely matches the measured data. Therefore, there is a trade-off between equivalent circuit model complexity and accuracy of dispersion analysis.

3.2.2 Voltage Dependent Capacitance Model

Device capacitances play an important role in determining the performance of MESFET integrated circuits. Since the range of bias voltages, V_{gs} and V_{gd}, varies widely from logic "1" state to logic "0" state in the digital circuits and DC bias variations in the saturation are sensitive to shift operating points in the analog circuits, the capacitance model should be valid in the wide bias range for accurate GaAs linear integrated circuit design. The well-known Miller effect is highly dependent on an accurate determination of the gate-to-drain capacitance(C_{gd}).

Many versions of SPICE still use a simple capacitance model which describes capacitances of Schottky diodes connected between the gate and the source and the gate and the drain. Actually, two separate diodes, one between gate and source and a second between gate and drain are sufficient to correctly describe MESFET's in digital circuits since the usual frequency of operation is always less than $f_t/2$[33]. For example, the Curtice model treats the gate-to-source capacitance as a nonlinear capacitance represented by the diode junction capacitance.

Based on this simplification and assuming that the channel doping profile is flat and that the boundary of the depleted region is abrupt, these capacitances at the reverse bias are given by the well-known law[58]:

$$C_{gs} = \frac{C_{go}}{(1 - V_{gs}/\phi_b)^{1/2}} \qquad (29)$$

$$C_{gd} = \frac{C_{go}}{(1 - V_{gd}/\phi_b)^{1/2}} \tag{30}$$

where, C_{go} is the zero bias capacitance and is given by

$$C_{go} = (1/2)WL\left(\frac{\epsilon q N_D}{2\phi_b}\right). \tag{31}$$

However, the channel has a finite thickness (h) and the capacitance decreases rapidly near the threshold voltage V_t. The dependence of C_{gs} and C_{gd} on V_{ds} is not considered in this simple model. To overcome the dependence on V_{ds}, the gate-to-source capacitance can be represented as follows[56]:

$$C_{gs} = \frac{C_{go}}{(1 - V_{gs}/\phi_b)^{Mgs}} + C_x V_{ds} \tag{32}$$

where, M_{gs} is the diode ideality factor and C_x is a parameter to account for the effect of V_{ds} on the gate-to-source capacitance. This representation of C_{gs} as a function of both V_{gs} and V_{ds} is more accurate than that of a simple model in equation (29). Using the proper values of these model parameters, one can keep the C_{gs} equal to C_{gd} for zero drain-to-source voltage, which reflects the symmetry of drain and source terminals with respect to the gate. However, the empirical expression of equation (32) is still

difficult to fit the actual device characteristics accurately because the behavior for GaAs MESFET is complicated by the early onset of a carrier velocity saturation.

The C_{gs} is the rate of the change of the free charge on the gate electrode, $- Q_g$, with respect to V_{gs} at the constant V_{gd}. Similarly, the C_{gd} is the rate of the change of the free charge on the gate electrode with respect to V_{gd} at the constant V_{gs}. Therefore, C_{gs} and C_{gd} can be defined analytically by

$$C_{gs} = - \frac{dQ_g}{dV_s} = \frac{dQ_1}{dV_s} + C_{sw} \tag{33}$$

$$C_{gd} = - \frac{dQ_g}{dV_d} = \frac{dQ_1}{dV_d} + C_{sw} \tag{34}$$

where C_{sw} is the sidewall capacitance to be determined and Q_1 is the space charge under the gate region.

Using the assumptions of a uniform doping profile, Takada et. al.[63] were first to proposed the analytical capacitance model which describes the nonlinear voltage dependent gate capacitances, C_{gs} and C_{gd}. They defined transition voltages, V_{tr1} and V_{tr2}, that classify the interpolation region between the after and before pinch-off region, $V_{gs} < V_t + V_{tr1}$, the gate to source capacitance can be expressed as[63]

$$C_{gs} = WL(8)^{-1/2}[qN_D\epsilon/(\phi_b - V_{gs})]^{1/2} \quad (30)$$

where $C_{sw} = \pi\epsilon W/2$ is the side wall capacitance. For the transition region, $V_t - V_{tr2} < V_{gs} < V_t + V_{tr1}$,

$$C_{gs} = C_{po}(V_{gs} = V_t - V_{tr2}) + [C_{sw} + WL(8)^{-1/2}\{qN_D\epsilon/(\phi_b - (V_t + V_{tr1}))\}^{1/2} - C_{po}(V_{gs} = V_t - V_{tr2})][\{V_{gs} - (V_t - V_{tr2})\}/(V_{tr1} + V_{tr2})\}] \quad (36)$$

where,

$$C_{po} = \epsilon W \tan^{-1}[(\phi_b - V_t)/(V_t - V_{gs})]. \quad (37)$$

C_{po} is the C_{gs} capacitance after the channel is completely pinched off($V_{gs} < V_t - V_{tr2}$). Since the drain and the source are symmetric with respect to the gate, the expressions describing the gate to drain capacitance C_{gd} can be derived with the same form as those for C_{gs}.

For the nonuniform doping profile in ion-implanted GaAs MESFET, Chen et. al.[64] developed an analytical model which takes into account the Gunn domain formation and backgating. However, this model's expressions are quite complicated and do not included the channel/substrate junction modulation due to the deep-level effects. Recently the channel depth has been more reduced and the doping concentration has been more increased to obtain the high performance characteristics of GaAs MESFET's. This results in the low pinch-off voltage and the high transconductance. Therefore, the use of an effective uniform doping condition provides enough accuracy for high performance GaAs MESFET's.

Using an effective uniform doping condition, we have developed an analytical capacitance model which describes the dependence on V_{gs} and V_{ds} by deriving the stored charge in the linear, saturation, and pinch-off regions. This model is one which also includes the channel/substrate junction affects on the capacitances, C_{gs} and C_{gd}, which are functions of V_{ds} and V_{gs}. Fig. 3.2 shows the self-backgating MESFET space charge distribution before and after pinch-off. The stored charge in region I is a function of the gate-to- source and drain voltages. The gradual channel approximation is still approximately correct and the mobility is nearly constant in the linear region. The incremental position in the x direction in region I is given using equations (12) and (16) as

$$dx = qW(N_D - N_{teff}^{-})\ (h - w(x) - dx)\ \frac{\mu dV}{(1 + \mu V_{d_1}/L_1 \upsilon_s) I_{ds_1}}. \qquad (38)$$

Here, L_1 is the channel length in region I and V_{ds1} is the voltage drop cross region I. Then, the charge in region I, Q_1, can be obtained assuming a uniform doping and equation (38).

$$Q_1 = \int_0^{L_1} Wqw(x)\ (N_D + N_{EL2})\ dx$$

$$= \int_0^{L_1} q^2W^2\ (N_D + N_{EL2})\ (N_D - N_{teff}^{-})\ (h - w(x) - d(x))\ \frac{L_1 \mu dV}{(L_1 + \mu V_{ds_1}/\upsilon_s) I_{ds_1}}. \qquad (39)$$

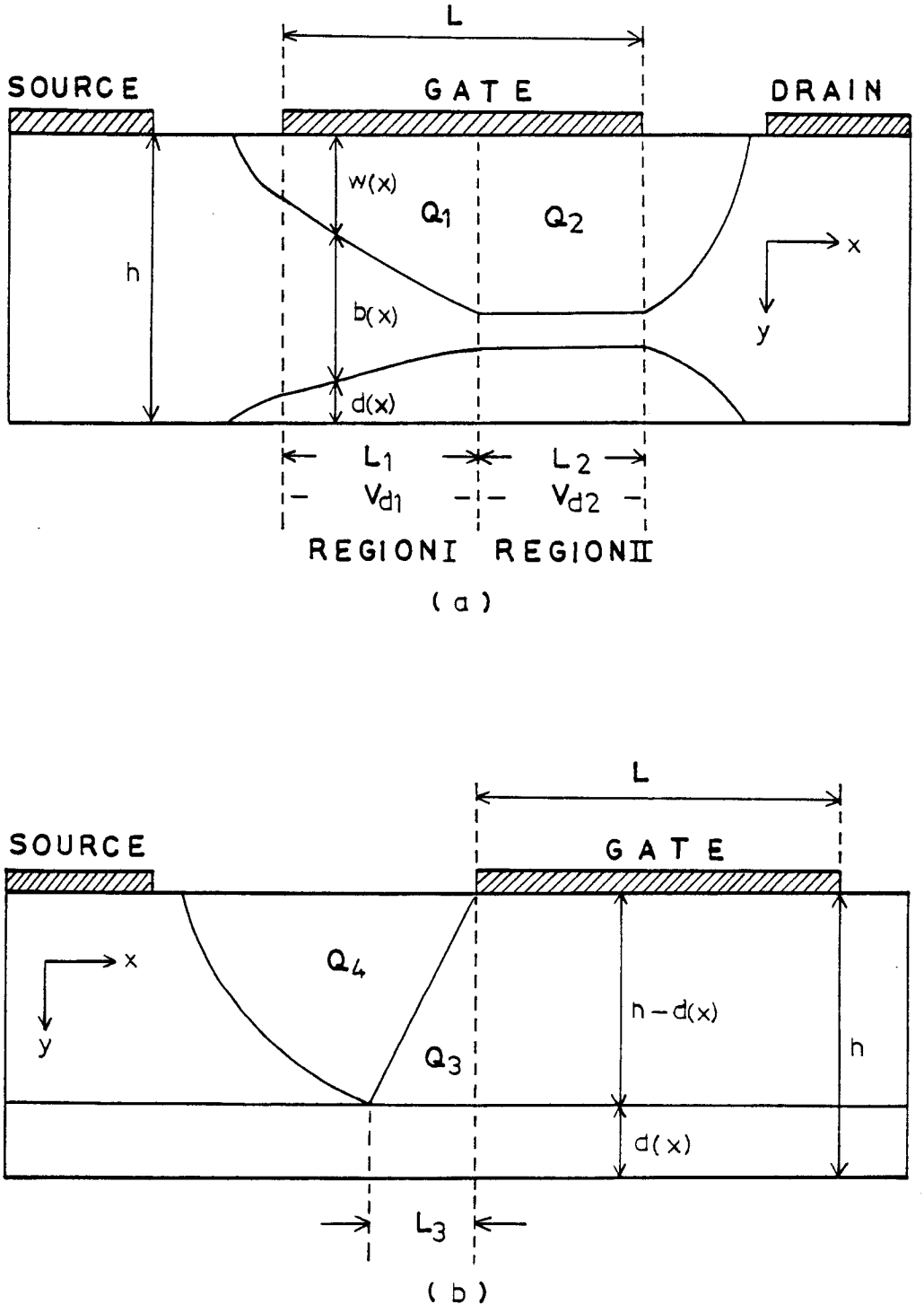


Fig. 3.2. Self-backgating MESFET space charge distribution with two asymmetrical depletion regions (a) before pinch-off (b) after pinch-off.

Since the differentiation of the drain voltage dV can be obtained by equations (13) and (14) as follows:

$$dV = \frac{q(N_D+N_{EL2})}{\epsilon} w(V)\,dw(V) = \frac{q(N_D+N_{EL2})}{\epsilon R} d(V)\,dd(V) \tag{40}$$

the drain current I_{ds1} in region I is given by equation (17) as

$$I_{ds_1} = \frac{qW(N_D-N_{teff}^-)}{L_1 + \mu V_{d1}/\upsilon_s} \cdot \frac{q(N_D+N_{EL2}}{\epsilon}\left[\int_{V_s}^{V_{d1}} (h-w(v))\,dw(v) - \frac{1}{R}\int_{V_s}^{V_{d1}} d^2(v)\,dd(v)\right]$$

$$= \frac{q^2W\mu(N_D-N_{teff}^-)(N_D+N_{EL2})}{\epsilon(L_1 + \mu V_{d1}/\upsilon_s)} \cdot \left[\frac{h}{2}\left(w^2(Vd_1) - w^2(V_s)\right)\right.$$

$$\left. - \frac{1}{3}\left(w^3(V_{d1}) - w^3(V_s)\right) - \frac{1}{3R}\left(d^3(V_{d1}) - d^3(V_s)\right)\right]. \tag{41}$$

Therefore, the stored charge, Q_1, in region I can be derived as follows:

$$Q_1 = WL_1q(N_D+N_{EL2})$$

$$\frac{\frac{h}{3}(w^3(V_{d1})-w^3(V_s)) - \frac{1}{4}(w^4(V_{d1})-w^4(V_s)) - f(V_{d1},V_s)}{\frac{h}{2}(w^2(V_{d1})-w^2(V_s)) - \frac{1}{3}(w^3(V_{d1})-w^3(V_s)) - \frac{1}{3R}(d^3(V_{d1})-d^3(V_s))} \tag{42}$$

where, $f(V_{d1}, V_s)$ is defined by

$$f(V_{d1},V_s) = 2\sqrt{R}\left[\frac{\epsilon}{q(N_D+N_{EL2})}\right]\left[\frac{V_{d1}^3-V_s^3}{3} + \frac{(\phi_b-V_g+V_b)(V_{d1}^2-V_s^2)}{2} + V_b(\phi_b-V_g)(V_{d1}-V_s)\right]. \tag{43}$$

In region II, just at the boundary with region I, the current can be calculated assuming a simplified velocity saturation mechanism as [65]

$$I_{ds_2} \simeq q\mu(N_D - N^-_{teff}) b_1 W E_s \tag{44}$$

where E_s is the longitudinal field which just causes carrier velocity saturation and b_1 is the channel thickness at that point and is given by

$$b_1 = h - w(V_{d1}) - d(V_{d1}) . \tag{45}$$

If we equate equations (41) and (44) to require current continuity at the junction between region I and II, then

$$L_1 = -\frac{\mu V_{d1}}{v_s} + \frac{q(N_D+N_{EL2}) \left\{ \frac{h}{2} \left(w^2(V_{d1}) - w^2(V_s)\right) - \frac{1}{3} \left(w^3(V_{d1}) - w^3(V_s)\right) - \frac{1}{3R} \left(d^3(V_{d1}) - d^3(V_s)\right) \right\}}{E_s \epsilon \left(h - w(V_{d1}) - d(V_{d1})\right)} \tag{46}$$

where V_{d1} is given by[66]

$$V_{d1} = V_d - V_s - \frac{2h}{\pi} E_s \sinh\left[\frac{\pi(L-L_1)}{2h}\right] . \tag{47}$$

Therefore, the simplified charge in region II, Q_2, can be obtained by

$$Q_2 \simeq W(L-L_1)\, w(V_{d1})\, q(N_D+N_{EL2}) . \tag{48}$$

After pinch-off, the channel region under the gate is almost depleted and only the lateral charge variation as shown in Fig. 3.2(b) contributes to C_{gs} and C_{gd} [63]. The lateral charges, Q_3 and Q_4, can be derived by

$$Q_3 = 1/2\ q(N_D+N_{EL2})\ W(h-d(x))L_3 = W\epsilon\ f_1(V_s)f_2(V_s) \tag{49}$$

$$Q_4 = W\epsilon\ \ (\phi_b-V_g+V_s)\theta = W\epsilon\ (\phi_b-V_g+V_s)\ \tan^{-1}\left[\frac{f_1(V_s)}{f_2(V_s)}\right] \tag{50}$$

where, L_3 represents the lateral distance due to the extended depletion region on the source side as shown in Fig. 3.2(b) and

$$\theta = \tan^{-1}\left[\frac{h-d(x)}{L_3}\right] \tag{51}$$

$$f_1(V_s) = \sqrt{V_p} - \sqrt{R(V_b+V_s)} \tag{52}$$

$$f_2(V_s) = [(\phi_b-V_g-V_p-RV_b) + V_s(1-R) + 2\sqrt{V_pR(V_b+V_s)}]^{1/2} \tag{53}$$

Therefore, the analytical capacitances, C_{gs} and C_{gd}, are given by

- before pinch-off

$$C_{gs} = \left.\frac{\partial(Q_1+Q_2)}{\partial V_s}\right|_{V_d,\ V_g = \text{const}} + C_{sw} \tag{54}$$

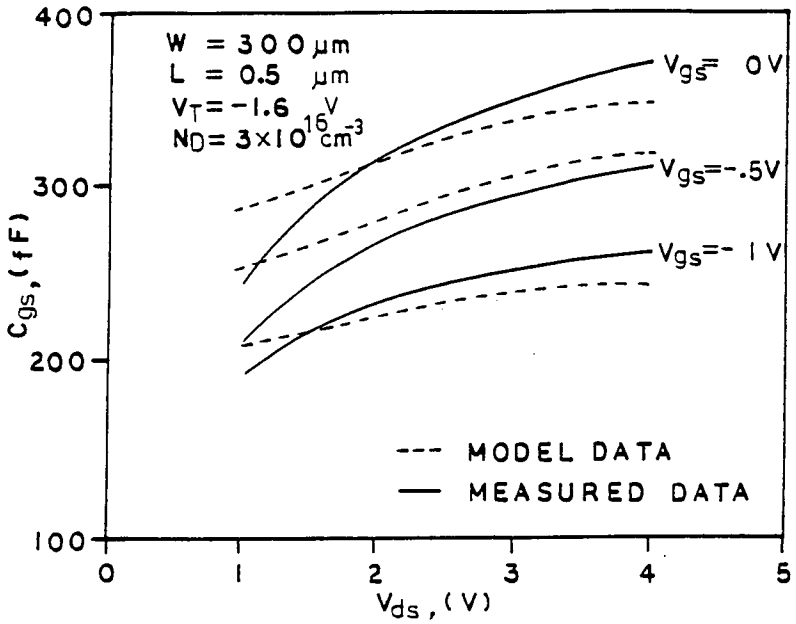


Fig. 3.3. Voltage dependent $C_{gs}(V_{gs}, V_{ds})$ comparison between measured data and computed model data.

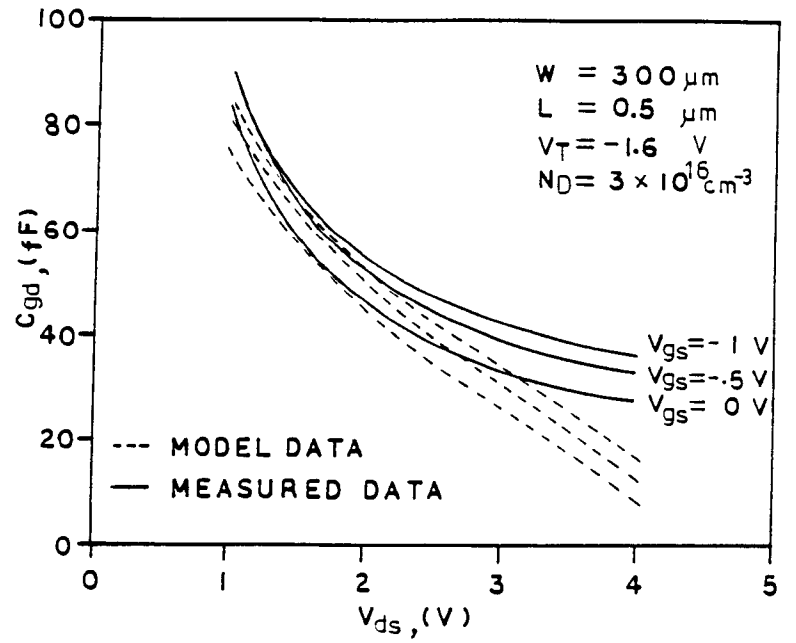


Fig. 3.4. Voltage dependent $C_{gd}(V_{gs}, V_{ds})$ comparison between measured data and computed model data.

$$C_{gd} = \left[\frac{\partial Q_1}{\partial V_{d1}} + \frac{\partial Q_2}{\partial V_{d2}}\right]\Bigg|_{V_s,\ V_g = \text{const}} + C_{pf} \tag{55}$$

- after pinch-off

$$C_{gs} = \frac{\partial (Q_3+Q_4)}{\partial V_s}\Bigg|_{V_d,\ V_g = \text{const}} \tag{56}$$

$$C_{gd} = \frac{\partial (Q_3+Q_4)}{\partial V_d}\Bigg|_{V_s,\ V_g = \text{const}}. \tag{57}$$

Note that the pinch-off capacitance, C_{pf}, of equation (55) can be replaced by C_{sw} if $Q_2 = 0$ (linear region).

Figures, 3.3 and 3.4 show the voltage dependent $C_{gs}(V_{gs}, V_{ds})$ and $C_{gd}(V_{gs}, V_{ds})$ comparisons between measured data and computed model data . The measured $C_{gs}(V_{gs}, V_{ds})$ and $C_{gd}(V_{gs}, V_{ds})$ data, in Figures 3.3 and 3.4, was obtained by measured S-parameter data taken from representative half-micron gate length MESFET test devices (fabricated by TriQuint Semiconductor - standard product) and was optimally fitted by the computer optimization program FETFITTER of Cascade Microtech, Inc.. The measurement was performed by TriQuint Semicomductor of Beaverton, Oregon. The computed model data was obtained by a simple BASIC program on the IBM personal computer to compare with the measured data. In the given example here, we have used a uniform channel doping concentration of 3 x 10^{16} cm^{-3}, EL2 concentraion of 1 x 10^{16} cm^{-3}, and a channel depth of 1 μm for a conventional GaAs MESFET with W = 300 μm and L = 0.5 μm. Model data

corresponds to the measured data except in the high drain voltage saturated region. The reason for this discrepancy may be the rapid reduction of charge variation in the high voltage drain end. This capacitance analysis can be used to reduce error more than in Larson's case[15] by including the channel/substrate junction charge modulation. At V_{ds} = 0 V and V_{gs} = 0 V, C_{gs} and C_{gd} are both about 250 pF as predicted in Figures 3.3 and 3.4.

3.2.3 Subthreshold Current Model

As circuit density increases, power dissipation caused by MESFET subthreshold conduction must be kept small. For that reason, a GaAs FET tends to switch from a "barely on" state to an "almost off" state. Therefore, it is important to model the MESFET accurately in the subthreshold region to calculate inverter noise margins, gain, and device capacity[26].

Two mechanisms caused by leakage current in the pinch-off region are MESFET subthreshold conduction and Schottky diode reverse bias conduction. At the high negative gate bias, Schottky diode reverse bias conduction by the drift current at the gate to the drain junction dominates MESFET subthreshold conduction which mainly causes the lateral diffusion current from the channel mobile charge gradient in the depleted channel region.

Fig. 3.5 shows the cross section of self-backgating GaAs MESFET in the subthreshold region. An analytical subthreshold current model has been developed by a solution of Poisson's equation including mobile electrons and deep-level traps in the channel solved in one dimension along an axis normal to the gate of the MESFET. The effective uniform doping concentration(N_D) is used for the narrow n-channel depth with EL2 concentration(N_{EL2}) and the effective negative charges(N^-_{teff}) in the semi-insulating GsAs substrate.

Fig. 3.6 shows the self-backgating GaAs MESFET energy band diagram (a) and channel electron distribution (b) in the subthreshold regime. In the subthreshold regime the edges of the depletion regions of the Schottky gate junction and the channel/substrate(high-low) junction meet, depleting the structure and forming a parabolic minimum in the electron potential[67]. In this regime the mobile charge density which causes a subthreshold conduction is much less than the fixed ionized dopant density. Therefore, by solving Poisson's equation in the regions above and below y = h, ρ = + $q(N_D + N_{EL2})$ and - qN^-_{teff}, respectively, $\phi(y)$ is given by parabolic functions as follows:

$$\phi(y) = \phi_c - \frac{q(N_D + N_{EL2})}{2\epsilon}(y - y_c)^2, \qquad 0 < y < h \tag{58-1}$$

$$\phi(y) = \frac{qN^-_{teff}}{2\epsilon}[y - (h + dp)]^2, \qquad h < y < h + dp \tag{58-2}$$

where, the channel depth y_c and the minimum potential ϕ_c at $y = y_c$ are given by

$$y_c = (1 + S)h - [(Sh)^2 + \frac{2S\epsilon}{q(N_D + N_{EL2})}(V_{gs} - V_t + \gamma V_{ds})]^{1/2} \tag{59}$$

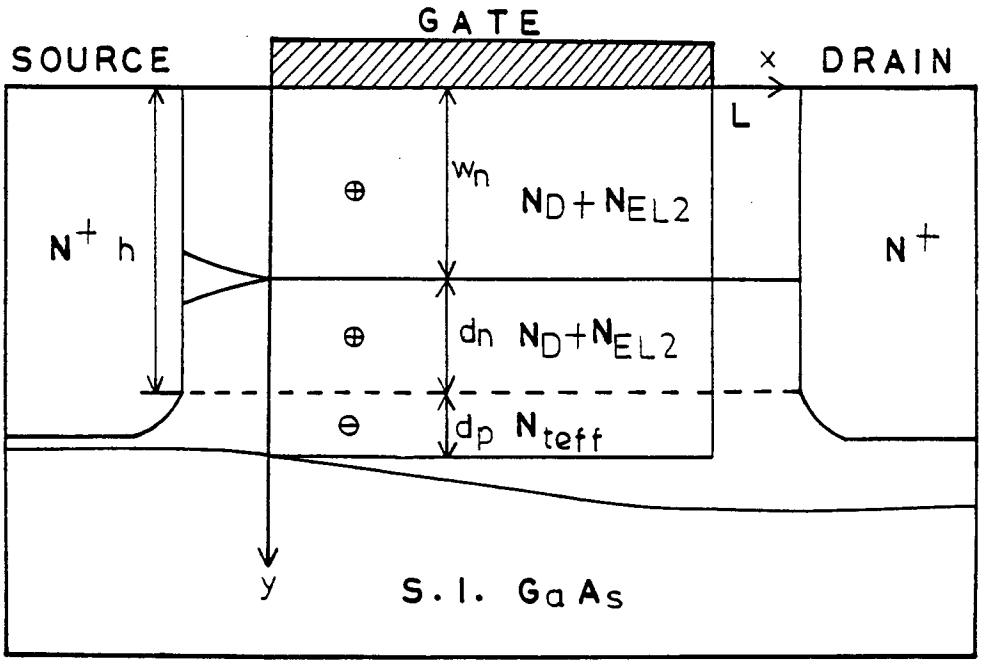


Fig. 3.5. The cross section of the self-backgating GaAs MESFET in the subthreshold region.

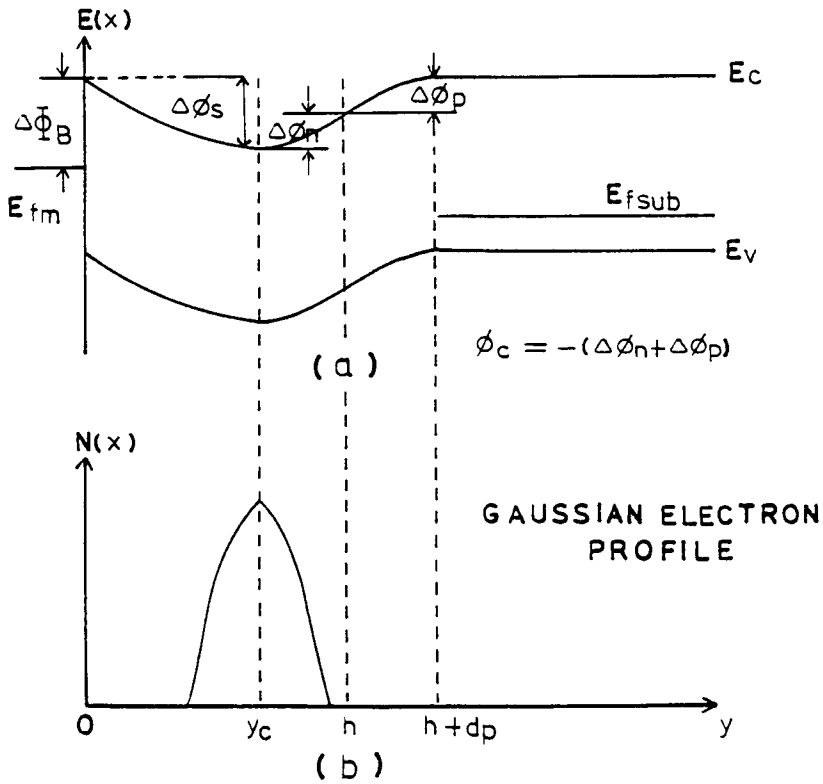


Fig. 3.6. The self-backgating GaAs MESFET energy band diagram (a) and channel electron distribution (b) in the subthreshold region.

$$\phi_c = (1 + S)[(\frac{qN^-_{teff}h^2}{2\epsilon} + V_{gs} - V_t + \gamma V_{ds})^{1/2} - (\frac{qN^-_{teff}h^2}{2\epsilon})^{1/2}]^2 \quad (60)$$

where, γ is the threshold voltage correction factor due to the channel length modulation and S is $N^-_{teff}/(N_D + N_{EL2})$.

To derive mobile channel charge(Q_{ch}), Poisson's equation is solved using Brew's method[68] including the exponential terms representing mobile electrons in the channel and mobile holes in the semi-insulating substrate. The electron density in the channel and the hole density in the semi-insulating substrate are given by

$$n = n_i \exp[\beta(\phi - \phi_{fn1})] \quad (61)$$

$$p = n_i \exp[\beta(\phi_{fn2} - \phi)] \quad (62)$$

where, ϕ_{fn1} and ϕ_{fn2} are the electron quasi-Fermi level at the channel and the semi-insulating substrate, respectively and $\beta = q/kT$. The n_i is the carrier density in intrinsic GaAs. Therefore, the Poisson's equation can be expressed by

$$\frac{d^2\phi}{dy^2} = + \frac{qn_i}{\epsilon} \exp[\beta(\phi - \phi_{fn1})], \qquad 0 < y < h \quad (63)$$

$$\frac{d^2\phi}{dy^2} = -\frac{qn_i}{\epsilon} \exp[\,\beta(\,\phi_{fn2} - \phi\,)], \qquad h < y < h + dp. \quad (64)$$

First, we can solve equation (63) for the channel using the identity:

$$\frac{1}{2}\frac{d}{dy}\left(\frac{d\phi}{dy}\right)^2 = \left(\frac{d\phi}{dy}\right)\left(\frac{d^2\phi}{dy^2}\right) \quad (65)$$

where, $\phi = \phi_s$ at $y = 0$, $\phi = \phi_h$ at $y = h$, and $\phi = \phi_c$ and $d\phi/dy = 0$ at $y = y_c$. After some calculations, we can get the electric fields at the $y = 0$ and $y = h$.

$$\left.\frac{d\phi}{dy}\right|_{y=0} = (2)^{1/2}(\beta L_b)^{-1} r'[\exp\{\beta(\phi_f - \phi_{fn1})\}(\exp(\beta\phi_c) - \exp(\beta\phi_s))]^{1/2} \quad (66)$$

$$\left.\frac{d\phi}{dy}\right|_{y=h} = (2)^{1/2}(\beta L_b)^{-1} r'[\exp\{\beta(\phi_f - \phi_{fn1})\}(\exp(\beta\phi_h) - \exp(\beta\phi_c))]^{1/2} \quad (67)$$

where, r' is $n_i/(N_D + N_{EL2})$, ϕ_f is the Fermi level of electrons in the channel in equilibrium, and L_b is the channel Debye length length. Q_{ch} is found using Gauss's law, which states that the electric fields multiplied by the dielectric permittivity is equal to the charge, giving rise to these electrical fields in equations (66) and (67). Similarly, from equation (64), we can find the substrate

mobile charge Q_{sub} by hole in terms of N_{teff}^{-}. If we neglect Q_{sub}, the total charge of depletion region in the subthreshold region is given by

$$Q_{ch} = Q_{ch1} + Q_{ch2} \tag{68}$$

where

$$Q_{ch1} = \epsilon \frac{d\phi}{dy}\Big|_{y=0} \tag{69}$$

$$Q_{ch2} = \epsilon \frac{d\phi}{dy}\Big|_{y=h}. \tag{70}$$

If we assume no drift current, then there is only lateral current, which must be strictly a diffusion current in the subthreshold region. Diffusion current is driven by the gradient of electron density in the channel. We neglect the diffusion current by the gradient of hole density in the semi-insulating substrate. The reason is that hole mobility is much less than electron mobility in GaAs. The diffusion current density is defined by

$$J_{diff} = qD \frac{dn}{dx}, \qquad D = \frac{kT}{q}\mu . \tag{71}$$

Therefore, the subthreshold lateral diffusion current can be derived as follows:

$$I_{sub} = \frac{W\mu}{\beta} \frac{dQ_{ch}}{dx} = \frac{(8)^{1/2} Wr' \mu \epsilon}{\beta^2 L L_b} [1 - \exp(-\beta V_{ds}/2)]$$

$$[\{\exp(\beta \phi_s/\eta) - \exp(\beta \phi_c/\eta)\}^{1/2} + \{\exp(\beta \phi_h/\eta) - \exp(\beta \phi_c/\eta)\}^{1/2}] \quad (72)$$

where, η is an ideality factor of about 2 for diffusion as an empirical parameter.

For Schottky diode reverse bias conduction, we used the reverse diode current equation described by an expression given by Dunn[69].

$$I_d = A J_r V_d \exp(-\beta \delta V_d) \quad (73)$$

for $V_d < 0$ where J_r is the diode reverse current and δ is the reverse-bias Schottky-barrier-lowering coefficient.

Fig. 3.7 shows channel electron distribution dependence on V_{gs} and V_{ds} for the subthreshold current model. The channel charge gradient, which is caused by the applied voltages gives lateral diffusion current as the main mechanism of the subthreshold current in the pinch-off region. The peak value of the channel electron distribution decreases and the point of minimum potential moves toward the substrate when the negative gate-to-source voltage increases. As the drain-to-source voltage increases, the standard deviation of the channel electron distribution

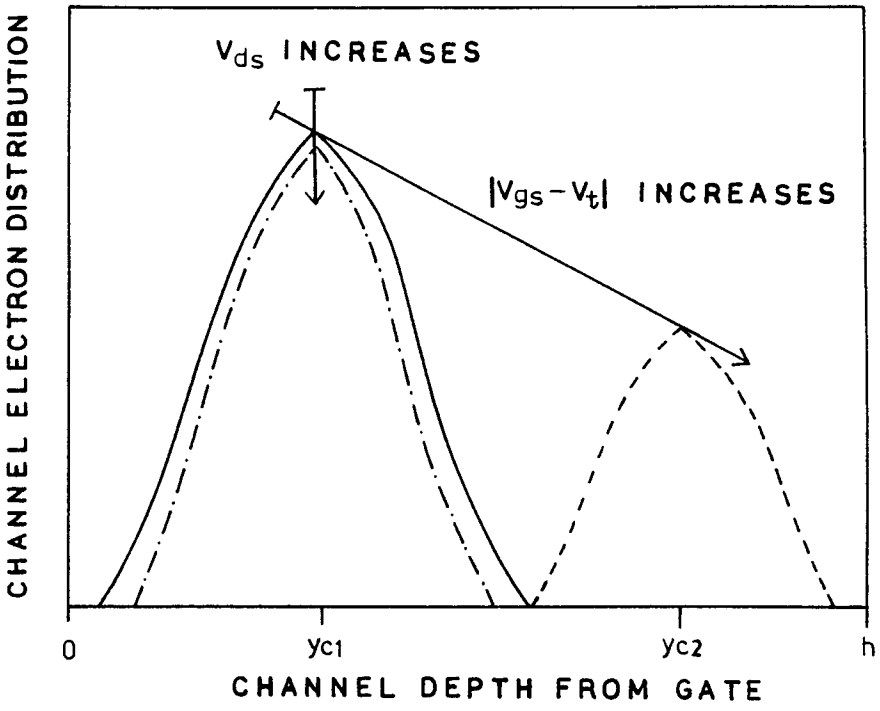


Fig. 3.7. Channel electron distribution dependence on V_{gs} and V_{ds} for subthreshold current model.

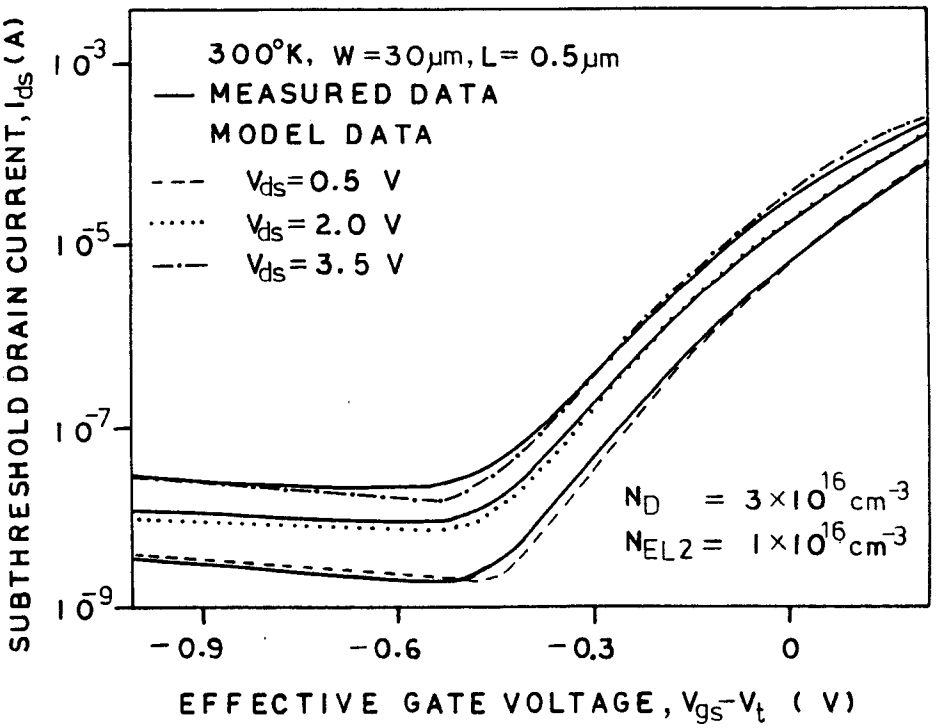


Fig. 3.8. A subthreshold current comparison between measured data and computed model data.

tends to reduce due to the self-backgating effect[1,3] at the drain side.

This analysis gives the exponential relationship for I_{sub} vs. V_{gs} and the nearly linear relationship for I_{sub} vs. V_{ds}. Fig. 3.8 shows a subthreshold current comparison between measured data and computed model data. At high negative Vgs, Schottky-diode reverse leakage current, a drift current in the gate-to-drain junction dominates the lateral diffusion current in the depleted channel region. The subthreshold conduction region has been defined as the regime of lateral current flow from the threshold voltage down to the onset of gate voltage at which I_{sub} begins to increase due to this drift current.

In the example given here V_t is -1.4 V for I_{sub} = 10 μA at V_{ds} = 2 V for a device size of W = 30 μm and L = 0.5 μm and Fermi level pinning constant value of ϕ_s = 0.65 eV, the slope of log(I_{sub}) vs. V_{gs} in the model yields 9 at 300 K which corresponds to that of measured data which is 7. The reason for the difference may be due to the assumption of an effective uniform doping concentration and neglecting the hole diffusion current in the semi-insulating substrate.

3.2.4 Transit Time Delay vs. S-parameters

The transit time delay of the drain current which is controlled by the gate and self-backgating voltages is one of the important effects in the transient and AC operation for high frequency GaAs MESFET circuit applications. Although some circuit simulators for MMIC design have incorporated this transit time effect[31], in GaAs MESFET models, there are still difficulties in finding a well-defined MESFET model which includes channel/substrate junction modulation in the microwave frequency range and the effective delay system function for incorporating the transit time delay as a group delay.

The drain current $I_{ds}(V_{gs}(t),\ V_{ds})$ should be altered to $I_{ds}(V_{gs}(t-\tau),\ V_{ds})$, where τ is equal to the transit time under the gate[49].

$$I_{ds}(V_{gs}(t-\tau),V_{ds}) \simeq I_{ds}(V_{gs}(t),V_{ds}) - \tau \frac{d}{dt} I_{ds}(V_{gs}(t),V_{ds}) . \qquad (74)$$

In the frequency domain rather than the time domain, we can generally define a transit time delay as a group delay which can be obtained by differentiating the phase response $\phi(\omega)$ by angular frequency (ω) as follows:

$$\tau = - \frac{d\phi(\omega)}{d\omega} . \qquad (75)$$

For finite time delay in the small-signal model for high frequency operation, $g_m(new)$, now including time delay

effects, can be modeled in the frequency domain from equation (74) by

$$g_{mbs}(new) = g_{mbs}\ (1-j\omega\tau) \simeq g_{mbs}\ e^{-j\omega\tau}\ , \qquad \text{for } \omega\tau < 1. \tag{76}$$

Similarly, $g_{mbs}(new)$, due to a self-backgating effect which causes a reduced thickness of the channel allowing pinch-off of the channel from the backside as the drain-to-source voltage increases, can be obtained by including transit time delay in the frequency domain.

$$g_m(new) = g_m(1-j\omega\tau) \simeq g_m\ e^{-j\omega\tau} \qquad , \qquad \text{for } \omega\tau < 1. \tag{77}$$

This effect is important to include in any small signal model of device behavior if operation near cutoff frequency (f_t) is a possibility. To realize this transit time delay in a circuit simulator, we can apply an approximation method to the system function with a time delay given by

$$H(s) = E\ e^{-s\tau} = E/(\sinh s\tau + \cosh s\tau) \tag{78}$$

where E is an amplitude of the delay system function and s = jw. However, the direct insertion of this simple expression into the circuit simulator is not easy because of its complex mathematical value. From the network analysis, the higher order Bessel filter network can be synthesized to obtain the accurate linear delay network which consists of

passive elements. Using this approximation method to reduce the complexity for modifying the PSPICE source program, we can obtain a second order Bessel polynomial in the denominator of equation (78). Since the transit time delay is related to the drain current in the transient analysis and the transconductances, g_m and g_{mbs}, in the AC analysis in the circuit simulator PSPICE, we can obtain g_m(new), g_{mbs}(new), and $I_{ds}(V_{gs}(t-\tau), V_{ds})$ including a time delay effect by multiplying g_m, g_{mbs}, and $I_{ds}(V_{gs}(t), V_{ds})$ by a second order Bessel filter function into PSPICE.

Consider a self-backgating GaAs MESFET with transmission lines attached both at the gate side with transit time delay τ_1 and at the drain side with transit time delay τ_2. The overall elements of the scattering parameter are given by

$$S'_{ij} = |S_{ij}|\, e^{-j\{\theta ij + \omega(\tau i+\tau j)\}} \quad , \qquad \text{for } i,j = 1,2 \tag{79}$$

where $|S_{ij}|$ and θ_{ij} are the magnitude and the phase of self-backgating GaAs MESFET with transit time delay effects and $\omega(\tau_i+\tau_j) = \omega\sqrt{\epsilon u}\ (\ell_i+\ell_j)$represents phase shifting by the attached lossless transmission line with lengths of ℓ_i and ℓ_j .

However, to avoid impedance matching problems using the method of transmission lines attached at the gate and the drain for transit time delay effects, our method is to include a transit time delay in the transconductance(g_m) and the self-backgating transconductance (g_{mbs}) in the proposed

self-backgating 3-terminal AC MESFET circuit model. The value of g_{mbs} can be determined by measuring the output conductance at DC and AC and realizing an additional drain current($g_{mbs}V_{bs}$) flows due to the self-backgate voltage(V_{bs}) at high frequency. To realize this transit time delay in a circuit simulator, PSPICE, we have applied an approximation method to the system function. A second order Bessel filter function which is more linear in the phase than that of the constant delay function and which is more gradual in the amplitude cutoff than that of the constant delay Butterworth filter is utilized.

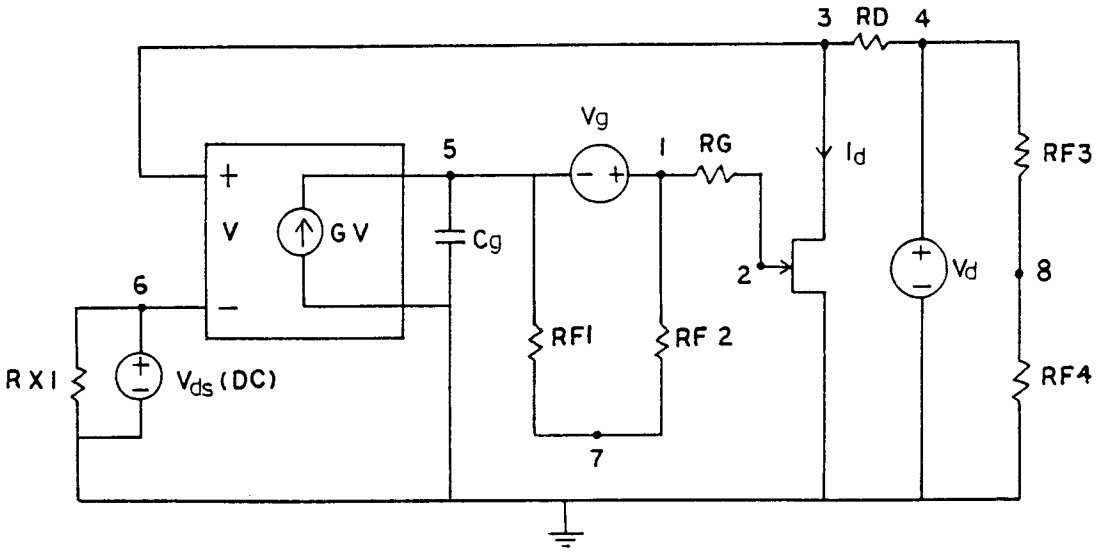


Fig. 3.9. A circuit configuration for S-parameter extraction using AC simulations in PSPICE.

Fig. 3.9 shows a circuit configuration for S-parameter extraction using AC simulations in PSPICE. This circuit configuration for S-parameters is presented which consists

of two AC signal sources, V_g and V_d, superimposed upon appropriate DC bias at the gate and drain. A matched reference impedance(Z_o = 50 Ω) and the low pass filter at the gate prevents feedback of high frequency components from the drain[70]. S_{11} can be defined by the input reflection coefficient with the output port terminated by a matched load, $Z_o = 1/Y_o$ and is given by

$$S_{11} = \frac{Z_{in} - Z_o}{Z_{in} + Z_o} \quad . \tag{80}$$

where Z_{in} is the input driving impedance looking into the gate terminal and can be derived using a small signal AC equivalent circuit model neglecting parasitic elements.

$$Z_{in} = \left[y_{11} - \frac{y_{12}y_{21}}{y_{22} + Y_o} \right]^{-1} . \tag{81}$$

The elements of the Y-matrix, y_{11}, y_{12}, y_{21}, and y_{22}, are given by

$$y_{11} = j\omega(C_{gs}+C_{gd}) \ , \qquad y_{12} = -j\omega C_{gd} \ , \qquad y_{21} = g_m \, e^{-j\omega\tau} - j\omega C_{gd} \ ,$$

$$y_{22} = \left\{ \frac{j\omega C_b(1+R_b g_{mbs} \, e^{-j\omega\tau})}{1 + j\omega C_b R_b} + j\omega(C_{ds}+C_{gd}) + g_{ds} \right\} .$$

S_{21}, the forward insertion gain, can be obtained when port 2 is terminated with $R_d = Z_o$ and $V_o = 0$(AC) and $V_g = 2E_{o1}$(AC) with $R_s = Z_o$ connected to port 1. S_{21} is given by[71]

$$S_{21} = \frac{V_2}{E_{o1}} = \frac{2y_{21}Y_o}{(Y_o+y_{22})\ (y_{11}+Y_o) - y_{21}y_{12}} \tag{82}$$

where V_2 is the output node voltage. Similarly, S_{22} is the output reflection coefficient and S_{12} is the reverse

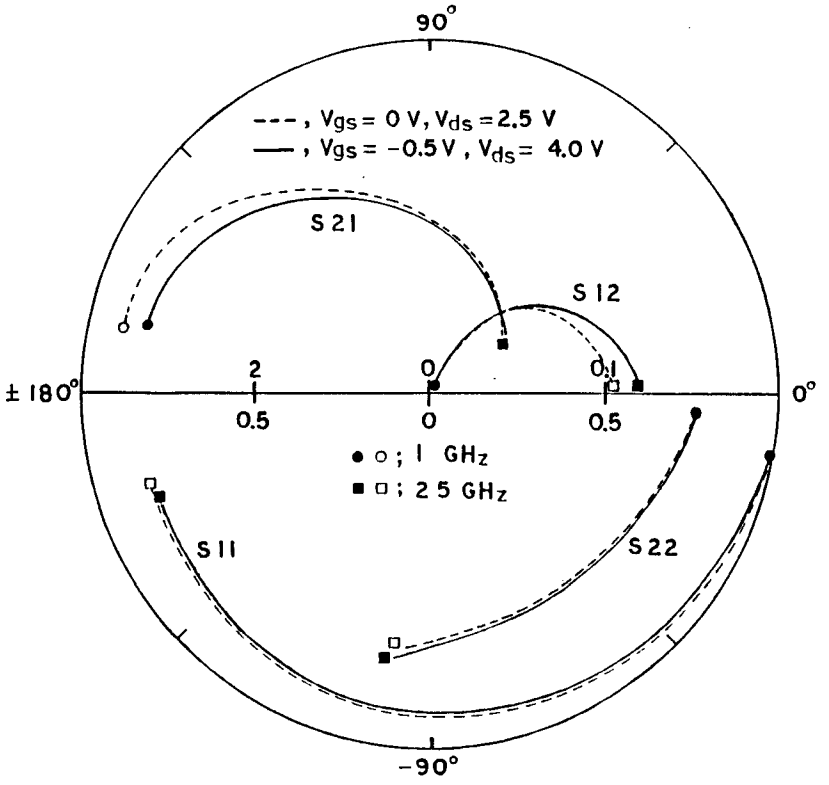


Fig. 3.10. Measured S-parameter data at both V_{gs} = 0 V, V_{ds} = 2.5 V and V_{gs} = -0.5 V, V_{ds} = 4.0 V.

insertion gain with the input port terminated in a match load, and they are given by

$$S_{12} = \frac{V_1}{E_{o2}} \tag{83}$$

$$S_{22} = \frac{Z_{out} - Z_o}{Z_{out} + Z_o} \tag{84}$$

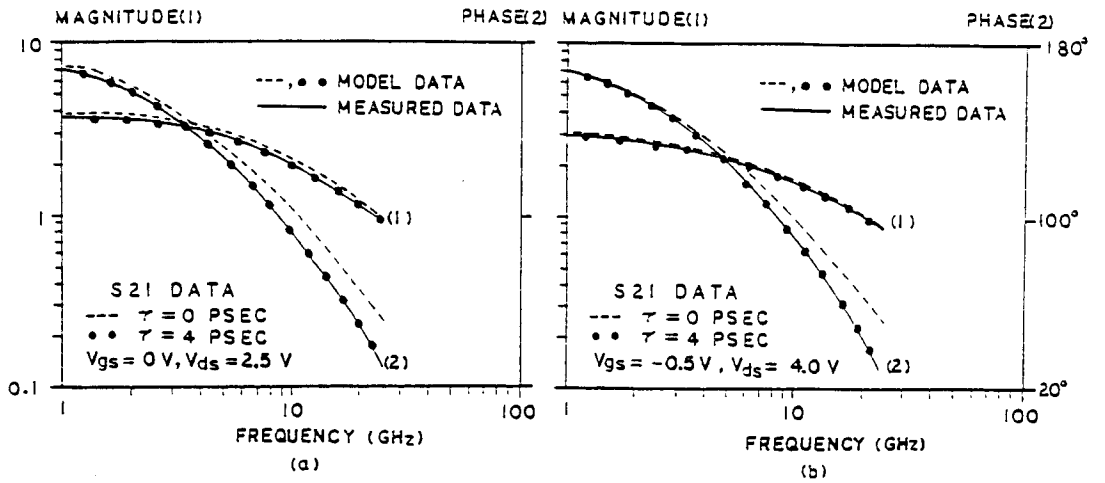


Fig. 3.11. Comparison between S_{21} measured data and computed model data at (a) V_{gs} = 0 V and V_{ds} = 2.5 V, (b) V_{gs} = - 0.5 V and V_{ds} = 4.0 V.

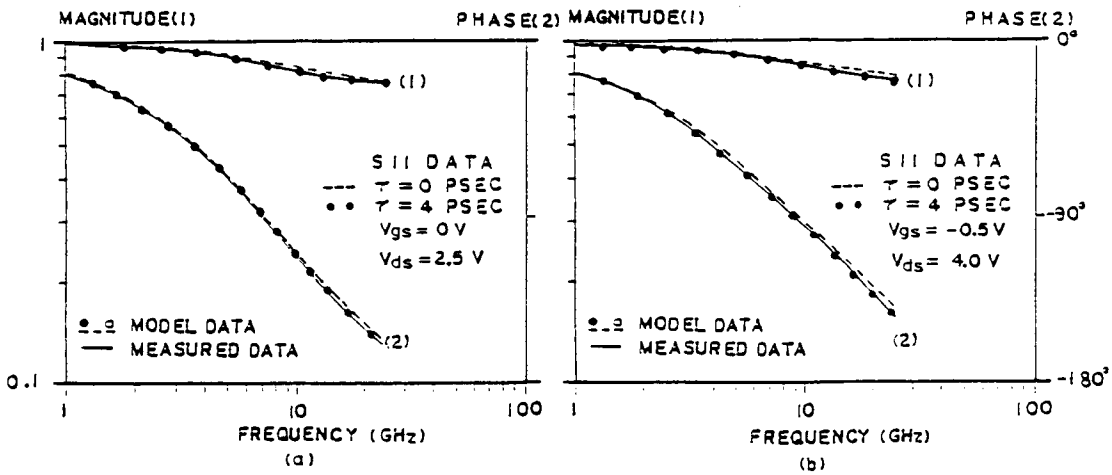


Fig. 3.12. Comparison between S_{11} measured data and computed model data at (a) V_{gs} = 0 V and V_{ds} = 2.5 V, (b) V_{gs} = - 0.5 V and V_{ds} = 4.0 V.

where Z_{out} is the output driving impedance looking into the drain terminal and V_1 is the input node voltage with voltage magnitudes of V_g = 0(AC) and V_d = $2E_{o2}$(AC). Since y_{21} and y_{22} are dependent on the transit time delay, this analysis predicted the phase shift of S-parameters. However, the phase shift of S-parameters is also related to the parasitic elements of the actual GaAs MESFET. We can extracted the computed S-parameters from AC simulations using PSPICE employing the self-backgating MESFET model and the parasitic elements of the actual GaAs MESFET in the circuit configuration as shown in Fig. 3.9. Fig. 3.10 shows measured S-parameter data at both V_{gs} = 0 V, V_{ds} = 2.5 V, and V_{gs} = -0.5 V, and V_{ds} = 4.0 V at the frequency range of 1 GHz to 25 GHz. The measured data for S_{21} and S_{12} is more sensitive than that of S_{11} and S_{22} to bias voltages changes. At these two particular bias conditions, we have compared S_{21} and S_{11} measured data and self-backgating model data for a conventional GaAs MESFET with W = 300 μm and L =0.5 μm as shown in Figures 3.11 and 3.12 (fabricated by TriQuint Semiconductor - standard product). For both bias conditions there are no discrepancies between measured S-parameters and computed model S-parameters if we incorporate a transit time delay of 4 psec in the self-backgating model. In both cases, the magnitudes of S-parameters are almost independent of a transit time delay. However, the phase of S_{21} shows an apparent deviation if the different values of τ = 0 psec and τ = 4 psec are used. Therefore, the inclusion of a transit

time delay which accounts for the delay under the gate and the self-backgate gives a better fit to the data and, in particular, can match S_{21} phase with minimal error which is hard or impossible to achieve unless a transit time delay is included. If only voltage dependent capacitance values are utilized, it is not possible to achieve a good fit to the S_{21} phase shift.

3.2.5 Nonlinear Large-Signal Model

The large-signal GaAs MESFET model has been described for analysis of microwave nonlinear networks. At small-signal levels, the behavior of GaAs MESFET's may be effectively modeled by a circuit with ordinary linear elements, and the circuit model can be retained for large signal conditions if the proper elements are modified to reflect the large-signal behavior[24,25,30,60,72]. Fig. 3.13 shows a large-signal MESFET model with the input and output matching networks. This model employs both linear and nonlinear elements which are characterized by measurement or modeling.

In linear elements, parasitic resistances associated with the GaAs MESFET(R_g, R_d, and R_s) can be measured using an automated Fukui approach[73]. The inductance values associated with bonding wire connections(L_g, L_d, and L_s) are analytically determined. The self-backgating GaAs MESFET model, consisting of capacitances between the source, gate, and drain(C_{gs}, C_{gd}, and C_{ds}), linear transconductance, output conductance and transit time delay for the drain current is used in this large signal model. An internal charging resistance(R_i) is also included for large signal model accuracy.

The main nonlinear element for the GaAs MESFET is the drain current. Since drain current is the ultimate source for the power delivered to the output load, deviations from linear behavior in this current will have the largest effect. Nonlinear drain current can be expressed based on a

modified Statz model for a large signal model as follows:

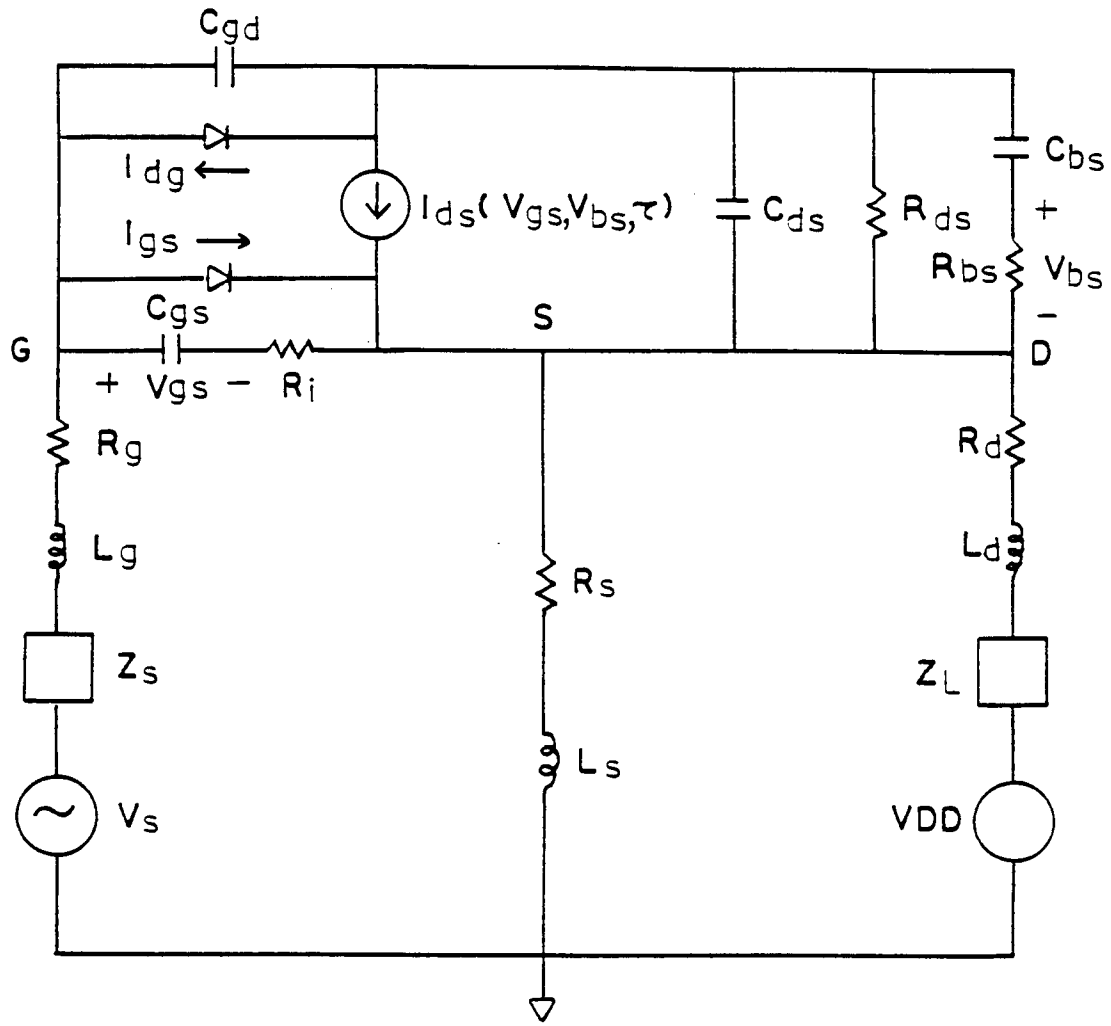


Fig. 3.13. A large-signal MESFET model with the input and output matching network.

$$I_{ds} = \frac{\beta [V_{gs}(t-\tau) - V_t + r_1 V_{bs}(t-\tau) + r_2 \{V_{bs}(t-\tau)\}^{1/2}]^2}{1 + B[V_{gs}(t-) - V_t + r_1 V_{bs}(t-\tau) + r_2 \{Vbs(t-\tau)\}^{1/2}]} \tanh[\alpha V_{ds}(t)]. \quad (85)$$

However, if the GaAs MESFET operates at normal bias region, the drain current as a function of V_{gs} and V_{bs} can be described by a power series with order-dependent transit time delays.

$$I_{ds} = (g_{m1}V_{gs} + g_{mbs1}V_{bs})\exp(-j\omega\tau_1) + (g_{m2}V_{gs}^2 + g_{mbs2}V_{bs}^2)\exp(-j\omega\tau_2) + \cdots \quad (86)$$

where g_{m1}, g_{m2}, $\cdots$, and g_{mbs1}, g_{mbs2}, $\cdots$ are real coefficients and τ_1, τ_2, $\cdots$ are time delays. For low distortion levels, a higher order power series can be truncated. In addition at the extremes of positive gate voltage and large positive drain voltage, respectively, the nonlinear forward-bias current and gate-to-drain breakdown current flow. The effect, in both cases, is to limit the current delivered to the load and to clip the output voltage waveform[28]. Therefore, these currents will also affect the gain compression at large-signal levels and contribute to the harmonic content in the current and voltage waveforms.

In the large signal simulations the Schottky diodes are characterized by modeling the standard diode equation with the addition of a term representing the avalanche breakdown[56].

$$I_d = I_{sat}[\exp(\beta V_d) - 1 - \exp\{-\beta(V_d + V_B)\}] \quad (87)$$

where β is q/kT and V_B is the avalanche breakdown voltage. I_{sat}, the reverse saturation current, is generally unknown; however, due to the exponential dependence on V_d, its exact value is not very important, and may be taken in the range of several nA.

In this model, the nonlinear current I_d(drain current), I_g(forward-bias current), and I_b(gate-to-drain breakdown current), are assumed to be functions of the instantaneous internal gate voltage V_g and drain voltage V_d. This feature allows the use of, essentially, DC measurements to characterize these currents. As an example of use of the model, 300 μm x 0.5 μm gate conventional GaAs MESFET has been chosen to characterize these currents. Fig. 3.14(a) shows the gate-to-drain breakdown current characteristics and Fig. 3.14(b) illustrates the gate to source forward-bias current, which is assumed dependent on V_g only, and exhibits the typical Schottky-diode current behavior.

An analysis of the large-signal model as shown in Fig 3.13 results in coupled, complex, simultaneous algebraic equations, with V_g and V_d as the independent variables in the frequency domain. The matrix representation of the two complex equations can be derived as follows[25,72]:

$$\begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} \begin{bmatrix} V_{gs} \\ V_{ds} \end{bmatrix} = \begin{bmatrix} b_1(V_{gs}, V_{ds}) \\ b_2(V_{gs}, V_{ds}) \end{bmatrix} \tag{88}$$

where,

$$a_{11} = 1 + j\omega[(Z_2 + R_i)C_{gs} + (Z_1 + Z_s)(C_{gs} + C_{dg} + j\omega R_i C_{gs} C_{dg}$$

$$a_{12} = j\omega[-(Z_1 + Z_s)C_{dg} + Z_2[C_{ds} + C_{bs}/(1 + j\omega C_{bs} R_{bs})]$$

$$a_{21} = j\omega[Z_2C_{gs}-(Z_3+Z_1)(j\omega R_iC_{gs} + 1)\{C_{ds} + C_{bs}/(1+j\omega C_{bs}R_{bs})\}]$$

$$a_{22} = 1 + j\omega[Z_2\{C_{ds} + C_{bs}/(1+j\omega C_{bs}R_{bs})\} + (Z_3+Z_1)(C_{dg}+C_{gs})]$$

$$b_1(V_{gs}, V_{ds}) = - (Z_1+Z_2+Z_s)I_{gs} + (Z_1+Z_s)I_{dg} - Z_2I_{ds} + V_S$$

$$b_2(V_{gs}, V_{ds}) = - Z_2I_{gs} - (Z_3+Z_1)I_{gd} - (Z_2+Z_3+Z_1)I_{ds} + V_{DD}$$

and $Z_1 = R_g + j\omega L_g$, $Z_2 = R_s + j\omega L_s$, and $Z_3 = R_d + j\omega L_d$. The nonlinearity in this equation is contained in the elements I_{ds}, I_{dg}, and I_{gs}, which depend on V_{gs} and V_{ds}. The nonlinear currents dependence on V_{gs} and V_{ds} are given by.

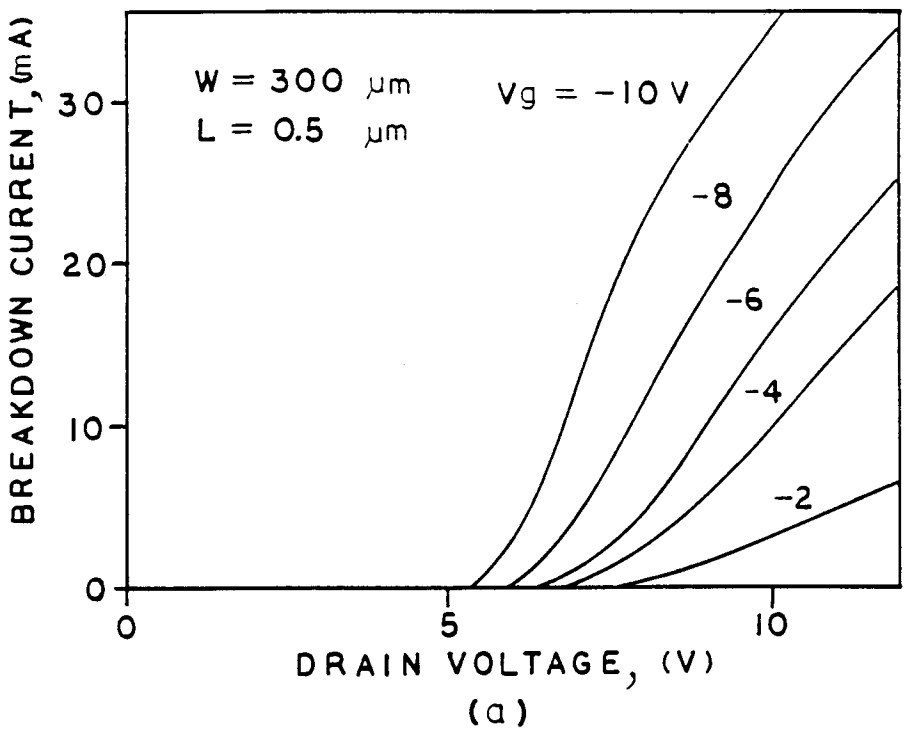
$$I_{ds} = g_m\exp(-j\omega\tau)V_{gs}+G_{mbs}\exp(-j\omega\tau)\frac{j\omega C_{bs}R_{bs}V_{ds}}{1 + j\omega C_{bs}R_{bs}} \qquad (89)$$

$$I_{gs} = I_{sat}[\exp(\beta V_{gs}) - 1 - \exp\{-\beta(V_{gs} + V_B)\}] \qquad (90)$$

$$I_{dg} = I_{sat}[\exp\{\beta(V_{ds}-V_{gs})\} - 1 - \exp\{-\beta(V_{ds} -V_{gs}-V_B)\}]. \qquad (91)$$

Matrix representation of equation (88) defines V_{gs} and V_{ds} only implicitly and the system is best solved computationally using an iterative technique.

In the time domain, since the expressions for inductance and capacitance must be put in terms of time



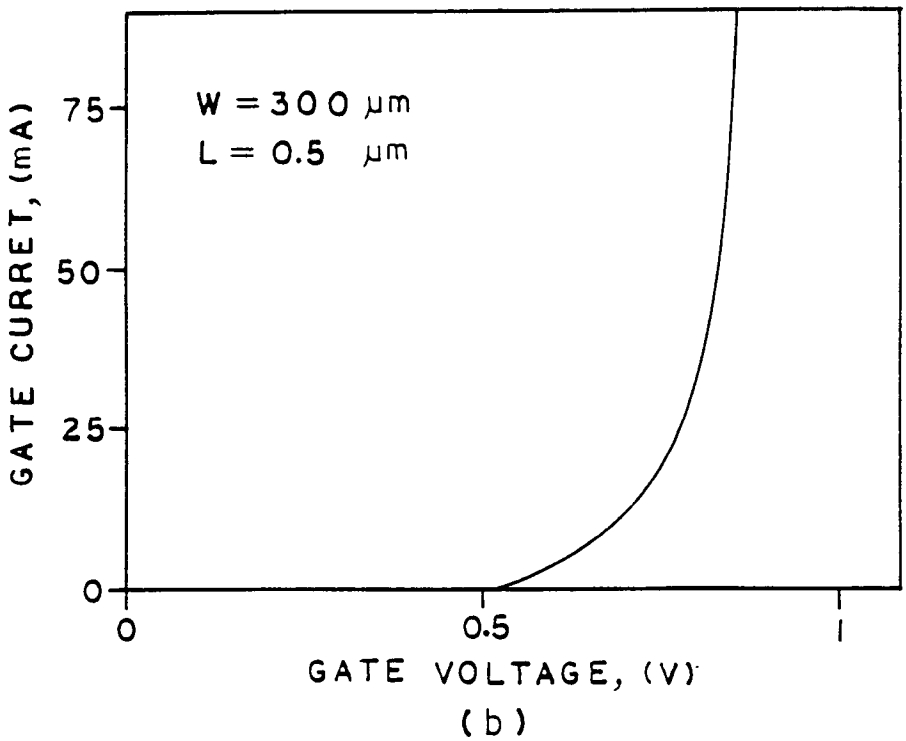


Fig. 3.14. A Schottky-diode current behavior (a) the gate-to-drain breakdown circuit characteristics (b) the gate-to-source forward-bias current characteristics.

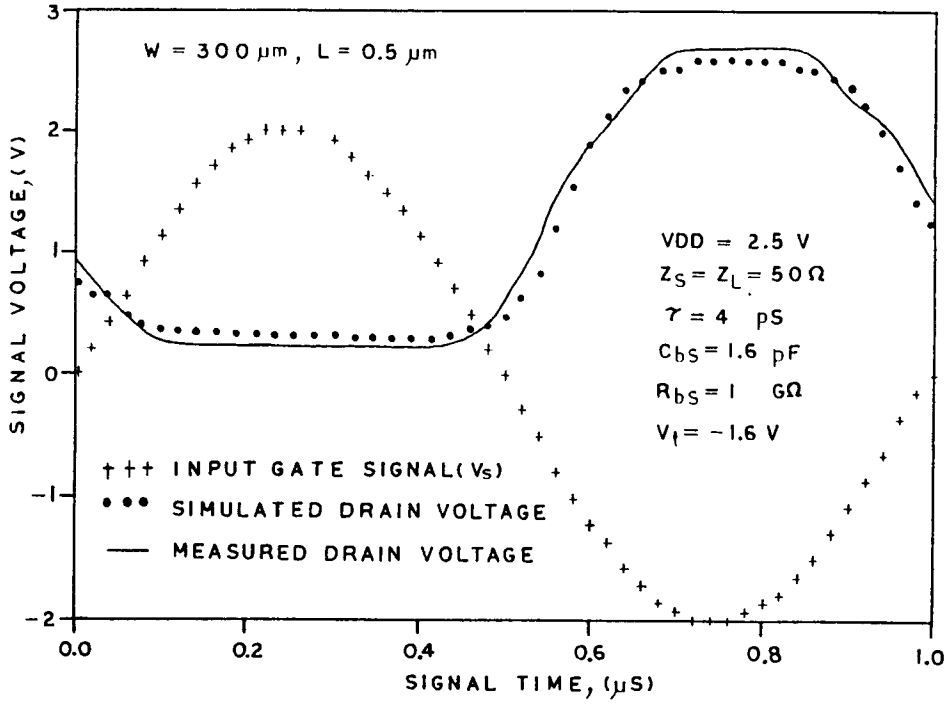


Fig. 3.15. AC large-signal characteristic comparison between measured data and simulated model data.

derivatives and integrals, the time domain expression for the large signal MESFET model may be more difficult to obtain than the simple expressions in the frequency domain. A large-signal RF sinusoidal signal is applied at the gate and the drain voltage waveform is measured to observe the harmonic content at large-signal levels. The absence of the higher harmonics in the measurement would mean that the drain voltage waveform must be a simple sinusoid[25]. To verify the large-signal MESFET model, PSPICE simulation has been performed using a nonlinear behavioral option in PSPICE with a subcircuit approach. Fig. 3.15 shows the AC large-signal characteristic comparison between measured data and simulated model data.

3.3 THE RESULTS AND DISCUSSION

A new three-terminal self-backgating GaAs MESFET model has been developed with a frequency dependent I-V curve and voltage dependent capacitances by presenting channel/substrate junction modulation as an essential feature of a conventional GaAs MESFET. This model can simulate low frequency anomalies by including deep-level trap effects. These cause transconductance reduction due to electron emission from EL2 in the depletion wide change at the edge of the Schottky gate junction and the output conductance to increase due to the time dependent net negative charge concentration in semi-insulating substrate as a result of self-backgating effects with the applied signal frequency. This model affords new analytical I-V characteristic expressions in equations (17) and (21) in this chapter and implies the requirement of a low EL2 concentration in the semi-insulating GaAs substrate for minimal low frequency anomalies. This model has been incorporated into PSPICE and includes a time dependent I-V curve model, a capacitance model, an RC network describing the effective substrate induced capacitance and resistance, and a switching resistance providing device symmetry. An analytical capacitance model describes the dependence of capacitance on V_{gs} and V_{ds} and is one which also including the channel/substrate junction modulation by the self-backgating effect.

An analytical subthreshold model has been developed by

including the channel/substrate junction modulation due to deep-level traps(EL2) and the Fermi-level pinning at the Schottky gate junction. The threshold voltage dependence on Vds due to self-backgating effect determines the nearly linear relationship between the lateral diffusion current and V_{ds}. A comparison of the slope of $\log(I_{sub})$ vs. V_{gs} shows reasonable agreement between measured data and model data. As an extension of the self-backgating AC small-signal MESFET model, a large-signal MESFET model has been developed for design of nonlinear building blocks, such as mixers and limiting amplifiers.

S-parameter errors between previous models and measured data in conventional GaAs MESFET's have been reduced by the including a transit time delay in the transconductances, g_m and g_{mbs}, in a well-defined self-backgating MESFET model. As a convenient extration method, a new circuit configuration has also been proposed for extracting S-parameters which accurately predict measured data. S-parameter comparisons for MMIC designs show good agreement between measured data and model data at the different bias conditions. This model can be used to simulate low frequency effects in GaAs linear integrated circuit design as well as to evaluate microwave characteristics for MMIC design.

CHAPTER 4

APPLICATION OF MODELS IN LINEAR GaAs CIRCUIT DESIGN

4.1 INTRODUCTION

As the viability of GaAs MESFET IC technologies becomes apparent through the demonstrated performance of high-speed digital circuits and microwave integrated circuits, considerable interest is being focused on the realization of precision analog integrated circuits. However, progress to date has been somewhat limited by device anomalous characteristics and a lack of accurate device models and design strategies. These anomalous characteristics have had a profound impact on the performance of precision analog circuits such as switched-capacitor filters and high-speed analog-to-digital(A/D) converters. Most conventional GaAs IC's are fabricated by direct ion-implantation into a semi-insulating GaAs substrate grown by the Czochralski method.

In the digital GaAs logic families, Schottky Diode FET Logic(SDFL) is the closest to commercial realization because it uses depletion-mode MESFET's leading to higher yields. Direct Coupled FET Logic(DCFL) circuits, however, offer the most potential for ultra high-speed operation and high current density. Several other logic families that have been, or are also, under consideration include composite logic, Source Coupled FET Logic(SCFL), and Tunnel Diode FET Logic(TDFL)[33,74,75,82]. Especially, the differential nature of SCFL improves the speed and noise margin immunity

to temperature and process variations to be utilized in LSI applications. One of the typical GaAs digital integrated circuit applications is the wide band digital signal processing system which consists of a preprocessor, a programmable signal processor, and a data processor[25]. GaAs digital integrated circuits will play an important role in preprocessors such as the demultiplexing and digital filtering, where the highest speeds are needed but where chip complexity is not a dominating factor.

GaAs microwave integrated circuits have become the standard active electronic device for analog microwave circuits above 1 to 2 GHz. Monolithic GaAs IC's have moved into the mainstream of high-frequency and high-speed instruments, and a wide variety of instrument types and manufacturers have come to market using GaAs IC technology. One of the most important features of MMICs is the capability to provide several circuit functions integrated into a single chip which offers extraordinary advantages in terms of size, weight, cost, and reliability. Much effort has been put into MMIC research, development, and production because of the potential huge advantages to be gained in their employments[76]. Even at relatively low frequencies in the 1 GHz frequency range, GaAs is favored over Si for certain applications even though integrated Si devices can achieve the required performance. The most notable advantage is that of superior radiation hardness in both nuclear and space applications.

DC-coupled analog integrated circuits which are sensitive to low frequency anomalous effects and, in some cases, to the device linearity are characterized by a lower integration density, but they process broadband, and small or large signals. A low frequency noise is the most severe limitation to the performances of wideband amplifiers, baseband oscillators, and low noise mixers below 1 MHz. A sidegating offset limits the design of the very high gain, densely packed amplifiers that would oscillate because of positive feedback. Consequently, the current lag effect on fast comparators for A/D converters affects a dynamic offset voltage for low frequency input signals[33]. The main advantages in analog circuit application in comparison to silicon technology lie with sampled-analog applications making use of the ability of GaAs MESFET's to be used both as fast switches and as linear devices.

This chapter begins with a discussion of analog opamp design techniques. Short channel GaAs devices exhibit a lower ratio of transconductance to output conductance which directly affects intrinsic voltage gain, and a variety of techniques are developed to overcome these limitations. Also, a new set of current mirrors are presented that are optimized for implementation in GaAs technology.

In the next section, as an application of the new models described in the chapter 3, a linear IC design example is demonstrated by simulation of and comparison to the measured characteristics of a 3-stage GaAs operational

amplifier fabricated by a conventional half micron MESFET technology. The main results are the gain and phase response as a function of frequency, the transient response with an ideal input pulse, and oscillator characteristics of the 3-stage GaAs operational amplifier. Compared to general purpose monolithic silicon bipolar opamps, this broad band GaAs amplifier has high frequency performance, low gain due to low g_m, and worse offset voltages. In the design of this GaAs opamp, we first used a double-ended cascode differential stage, a second single-ended cascode differential stage for high gain, interstage level shifters compatible with depletion-mode GaAs MESFET DC characteristics, and, finally, an internal compensation technique with forward blocking composed of a source follower and a feedback capacitance for stability.

4.2 THE APPLICATION

4.2.1 Analog OPAMP Design Technique

The GaAs operational amplifier has characteristics similar to general-purpose silicon operational amplifiers but exhibits a higher unit gain frequency. The major drawbacks of this opamp are low open-loop gain and low common-mode-rejection ratio. For the general purpose opamp, some characteristics should be required such as an open-loop gain of at least 1000, wide power supply operating range, and a common-mode input voltage range and output voltage

swing that increase with supply voltage[77]. Temperature compensation technique for stable phase margin have to be considered in the design as well. The NMOS opamps literature does provide some circuit analogies for MESFET designs. The analogies exist because both technologies yield low gain per stage amplifiers which forces the use of double-ended to single-ended converters, cascode designs, and current bleeders to achieve high open-loop gain. The 0.5 μm depletion-mode GaAs MESFET has a g_m/g_{ds} of about 9.3 when a MESFET is in saturation and the 1.0 μm silicon MOSFET has that of 11 at the saturation region[79]. Since g_m/g_{ds} is proportional to gate length, gate length could be increased in portions of the circuit which are inherently wide-band, to begin with such as active loads and source followers. The NMOS device is used to realize level shifting of several volts between the gate and the source. However, the level shift of the GaAs MESFET is restricted to less than 0.7 V using the forward Schottky diode characteristic. Because of this, GaAs MESFET current mirrors and interstage level shifters will have a different topology than NMOS designs.

To enhance the intrinsically low GaAs MESFET voltage gain at high frequency, the schematics of single-ended inverting amplifiers are presented in Fig. 4.1 with effective circuit modification. These circuit variations include cascodes for increasing voltage gain, g_m enhanced cascodes, and double cascodes with a long gate active FET

load[78]. Amplifier 1 is a basic common source amplifier with a depletion-mode MESFET load whose gain is given by

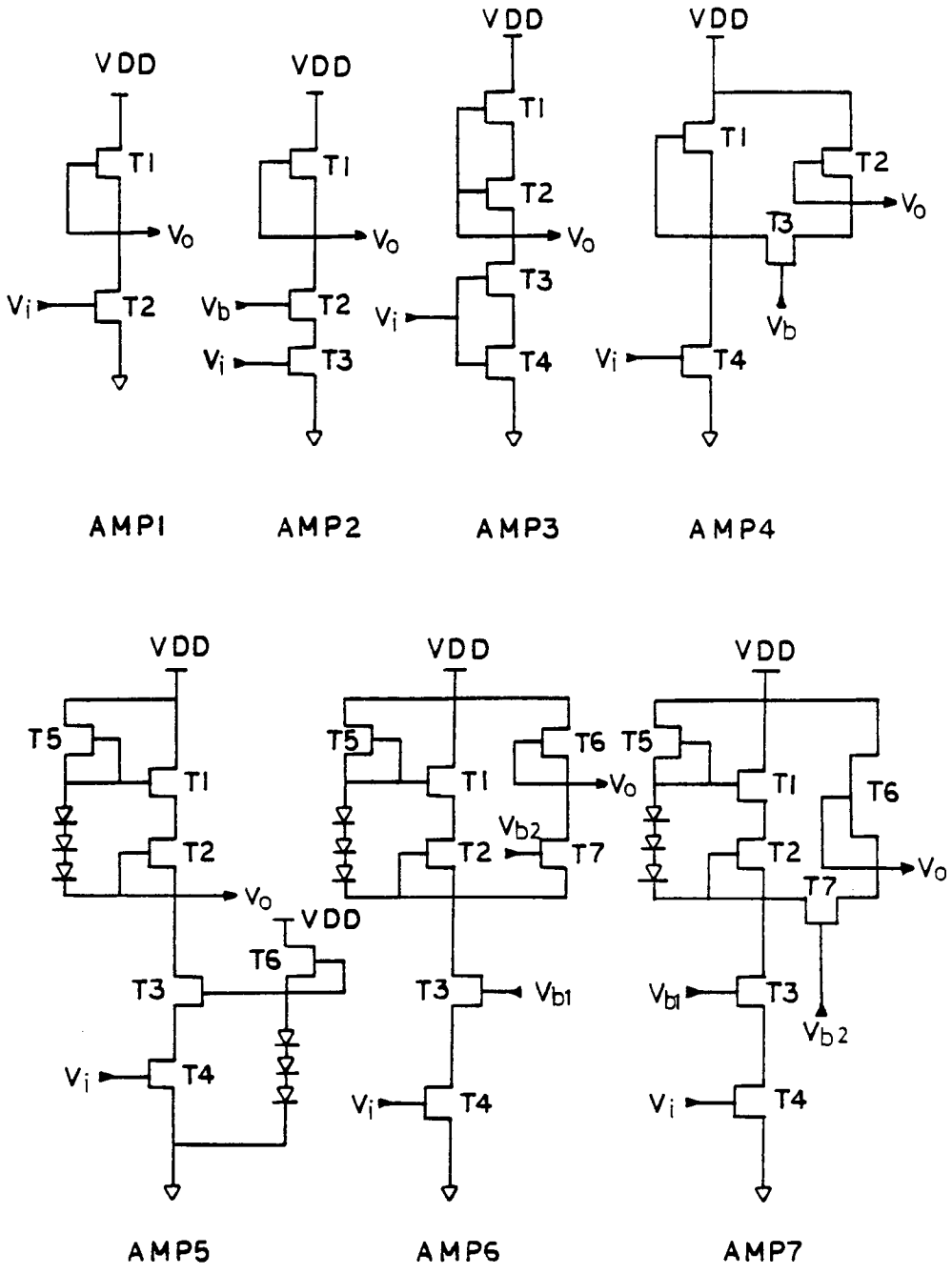


Fig. 4.1. The schematics of single-ended inverting amplifiers with effective circuit modification.

$$A_{v1} = \frac{- g_{m2}}{g_{ds1} + g_{ds2}} . \qquad (1)$$

The gain of amplifier 1 is limited because g_{gs1} and g_{ds2} are large in short-channel devices, especially at high frequencies. Therefore, the gain is smaller than desirable for a high performance analog circuit. The use of a cascode gain stage is a popular technique in analog integrated circuit design to improve the gain and the bandwidth. The gain of the cascode amplifier, amplifier 2, is given by

$$A_{v2} \simeq \frac{- g_{m3}}{g_{ds1}} . \qquad (2)$$

Amplifier 3 produces a gain enhancement by exploiting the early saturation phenomena that are typically observed in short-channel depletion-mode GaAs MESFET's[34,80]. In the self-booth strapped active load(T1 & T2), the threshold voltage of the feedback MESFET(T1) is made more negative than the primary(T2), to ensure that the latter is biased to operate in the current saturation region to realize the full benefit of technique. If both transistor T1 and T2 are in the saturation region, then T2 acts like a source follower, keeping the drain-to-source voltage across T1 constant. The resulting output conductance of the load can be approximated by

$$g_{out} \simeq \frac{g_{ds1}}{1 + g_{m2}/g_{ds2}} . \qquad (3)$$

This is a significant improvement over other gain enhancement techniques in short-channel MESFET's. The corresponding relationship between transistor widths and threshold voltages may be approximated to[34]

$$\frac{W_{T2}}{W_{T1}} = \left(\frac{V_{t1}}{V_{t1} - V_{t2}} \right)^2 . \qquad (4)$$

It is apparent that if a single threshold voltage were used, it would not be possible to achieve current saturation in the primary FET, as the ratio W_{T2}/W_{T1} would be too large to be implemented in practice. If this enhancement is applied to both the driver and the load of amplifier 3, the gain of amplifier 3 is given by

$$A_{v3} \simeq - g_{m4} / \left(\frac{g_{ds1}}{1 + g_{m2}/g_{ds2}} + \frac{g_{ds3}}{1 + g_{m4}/g_{ds4}} \right) . \qquad (5)$$

This circuit can also reduce the power dissipation which is only slightly higher than that of amplifier 1, but the bandwidth of the circuit is slightly degraded by Miller capacitance contribution of T3. Amplifier 4 is based on an application of an NMOS gain enhancement technique[81]. In this circuit, a large current flows through transistor T4,

increasing its transconductance, while a smaller current flows through T2, resulting in a reduced drain-to-source conductance. Transistor T1 acts as a current source, supplying the extra current to T4. As a result, the gain of this stage can be approximated by

$$A_{v4} \simeq \frac{-g_{m4}}{g_{ds2}} . \qquad (6)$$

The disadvantage of this technique is that the DC level of output voltage and the power dissipation are higher than the other techniques. Amplifier 5 is a cascode amplifier with a modified load which provides the appropriate DC bias for load transistors. The gate T1 follows the source of T2. The conductance looking into the source of T2 would be g_{ds2}, only if the drain was at small-signal ground. Indeed, it is not, but rather is following the source voltage at a gain slightly less than one. This greatly reduces the current and effectively decreases the load conductance(G_{load}) to

$$G_{load} \simeq \frac{g_{ds1}}{2 + g_{m2}/g_{ds2}} . \qquad (7)$$

Since the driving conductance(G_{drive}) can be obtained by a similar procedure when V_{in} is tied to ground, the gain of amplifier 5 is given by:

$$A_{v5} \simeq -g_{m4}/\left(\frac{g_{ds1}}{2 + g_{m2}/g_{ds2}} + \frac{g_{ds3}}{2 + g_{m4}/g_{ds4}} \right) . \qquad (8)$$

However, the gain is somewhat less in the actual circuit because the circuit accomplishes the level shifter consisted of T5, and T6. Since this is also a cascode stage, the gate-to-drain capacitance of T4 is not multiplied by the voltage gain of the amplifier due to the Miller effect, and it appears that there is no reduction in bandwidth compared to amplifier 1. Amplifiers 6 and 7 are double cascode amplifier without and with a long gate active load, respectively to obtain higher a voltage gain than any other previous scheme. However, one typical disadvantage of these amplifiers is a circuit stability problem. Fig. 4.2 shows a simulated voltage gain characteristic comparison of single ended inverting amplifiers by PSPICE circuit simulation using the new self-backgating GaAs MESFET model. The differential amplifier is often used in preference to the simple ended amplifier by virtue of its relatively large common mode rejection ratio. Here, the differential amplifier techniques will not be described in detail since the previous techniques for the enhancement of single-ended amplifier voltage gain can be applicable to differential amplifiers as well.

For shifting the dc level of a signal in the negative direction, it suffices simply to insert the appropriate number of forward biased Schottky diodes into the source of

the source-follower MESFET as shown in Fig. 4.3(a). Although it is possible to choose the current density in the diodes by specifying the diode area and the sizes of the MESFET's, the range of adjustment of the voltage across each is rather

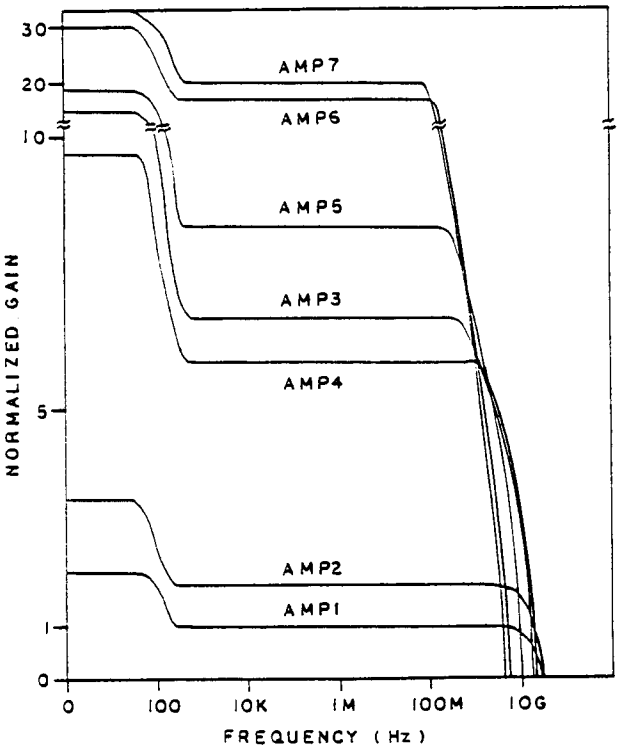


Fig. 4.2. Simulated voltage gain characteristic comparison of single-ended inverting amplifiers.

small, approximately 0.65 V. The diodes should, in practice, be chosen to ensure as low as possible an output impedance for the source follower, a high bandwidth. To shift the signal level in the positive direction, the diode chain can be used in reverse as shown in Fig. 4.3(b). In this circuit the impedance at the foot of the diode chain is too low to connect to any normal circuit, so a source follower is used to raise the impedance. Transistor T2 acts as a circuit source balancing that of both transistor T1 and T3. Its width should be the sum of the widths of those MESFET's[33].

Some high-performance GaAs MESFET current mirrors are shown in Fig. 4.4 which exploit the high speed of GaAs technology. The desirable properties of a current mirror are low input impedance and accurate current scaling. The typical depletion-mode GaAs MESFET current mirror circuit as shown in Fig 4.4(a), is based on a modification of that of enhancement-mode NMOS technology. A chain of forward-biased diodes is used to shift the level of the gate with respect to the drain by a fixed voltage. A current source is employed to keep the diodes in the forward biased region. The limitations of the technique arise from the use of the current source transistor, T2, to maintain the appropriate drain-to-gate voltage. Therefore, the minimum input current I_{in} is limited to the I_d, which is the current that biases the forward-biased level shifting diodes. Also, the maximum input current is limited to the value that causes the gate diode to draw significant forward-biased current. The ratio of currents between the output and the input is adjusted by varying the widths of the devices T1 - T4. In particular, if the effects of channel length modulation are neglected and

if $\beta_3/\beta_1 = \beta_4/\beta_2 = \gamma$, then

$$I_{out} = I_{in} = \gamma \tag{9}$$

and the small-signal input impedance of the current mirror is approximately $1/g_{m1}$. This current mirror can be employed to yield open-loop current amplifiers with extremely low

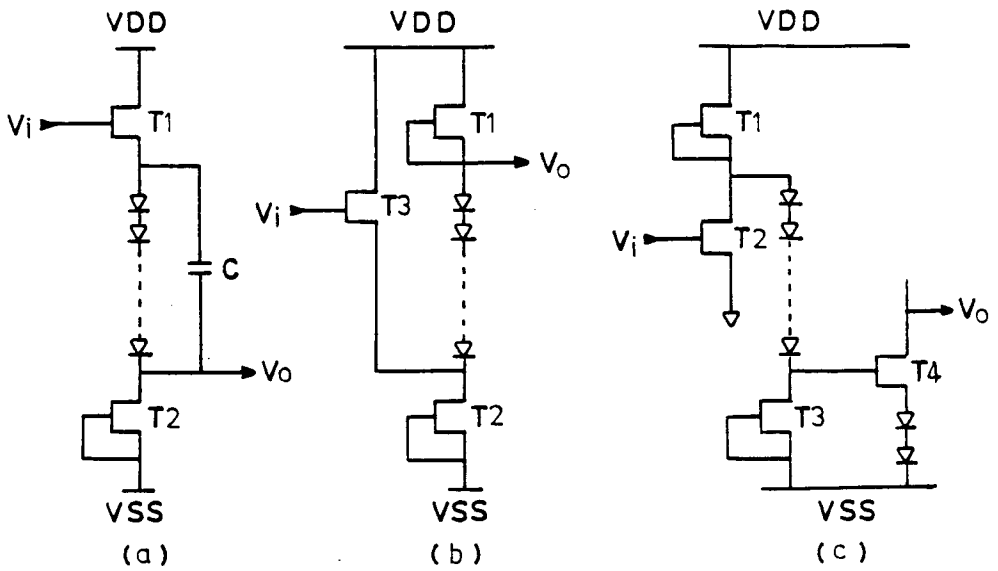


Fig. 4.3. The schematics of GaAs MESFET level shifting circuits.

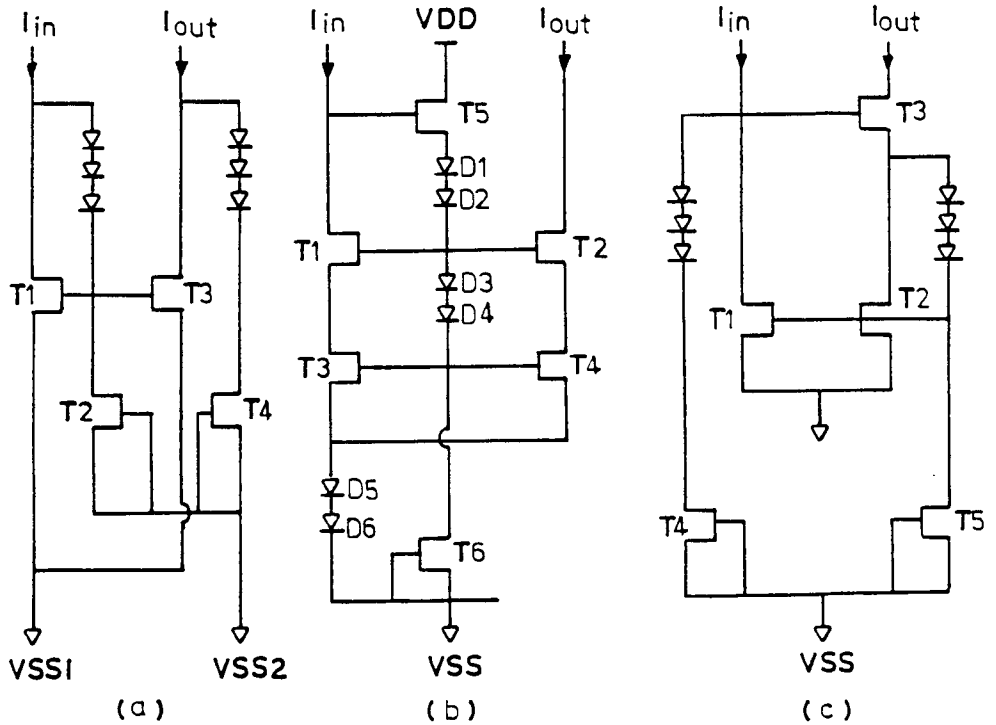


Fig. 4.4. The schematics of GaAs MESFET current mirror circuits.

distortion because γ is valid over a wide range of input currents. Also, the small-signal current gain can be demonstrated to be

$$\frac{I_{out}}{I_{in}} = \frac{g_{m3}}{g_{m1} + g_{ds1} + g_{ds2}} \cdot \frac{g_l}{g_l + g_{ds3} + g_{ds4}} \qquad (10)$$

when the effects of diode resistance are neglected. Here gl is a load conductance. In addition, the small-signal input and output conductances are given by

$$g_{out} = g_{ds3} + g_{ds4} \qquad (11)$$

$$g_{in} = g_{m1} + g_{ds3} + g_{ds4} . \qquad (12)$$

Fig. 4.4(b) shows a more advanced GaAs MESFET current mirror circuit[77]. If T3 is the same width as T4 and if all FET's are in saturation, then I_{out} is equal to I_{in}. Transistors, T1 and T2, are included to decrease the apparent output conductance of T3 and T4 and diode D1 and D2 provide a level shift sufficient to maintain T6 in saturation. Likewise, D3-D6 are used to maintain T1, T3, and T4 in saturation. T1-T4 are chosen to be the same width, and that width is picked so that the FET's will have zero gate-to-source voltage with a nominal drain current of I_{in}.

The output impedance and linearity of the current mirror can be improved through a technique similar to the Wilson current mirror often employed in bipolar or MOSFET circuits. This technique linearizes the circuit through

negative feedback, resulting in a more accurate transfer function and reduced distortion. A schematic of a GaAs MESFET Willson current mirror is shown in Fig. 4.4(c). Here, the forward-biased diode technique described for the simple current source has been employed again to keep the input device in saturation. The small-signal output conductance of this GaAs depletion-mode Willson current mirror can be given to be approximately[35,81]

$$g_{out} = \frac{g_{ds5}(g_{ds3} + g_{ds4})}{g_{m5}} \tag{13}$$

which is a substantial improvement over the simple current mirror scheme. Another manifestation of the increased output impedance of the GaAs Wilson current mirror is the reduced distortion which the circuit exhibits at high levels of the drain-source conductance.

4.2.2 **Linear IC Design Example - GaAs OPAMP**

This section has dealt with the extensive subject of GaAs amplifier design and particularly design of the 3-stage GaAs amplifier using the new self-backgating MESFET model, as described in chapter 3, which can simulate the low frequency anomalies of this GaAs amplifier. The design of the GaAs amplifier is significantly different from that in NMOS or CMOS technologies because of the unique properties of GaAs depletion-mode MESFET's. In particular, GaAs amplifier suffers from intrinsically low voltage gain and high threshold voltage non-uniformity which cause large off-set voltage. Since forward-biased Schottky diodes must be employed for level-shifting, the high series resistance of these diode can result in a great deal of gain degradation.

As a linear IC design example, a 3-stage GaAs operational amplifier has been designed using the new self-backgating MESFET model. This GaAs amplifier also has been fabricated by TriQuint Semiconductor, Inc. of Beaverton, Oregon using their conventional half micron MESFET technology. The GaAs operational amplifier has three inverting stages, series-shunt feedback, and internal compensation with forward blocking to achieve unique stability. The low frequency anomalies of the GaAs operational amplifier are accurately predicted using the new self-backgating MESFET model. An overall schematic of the 3-stage GaAs operational amplifier is shown in Fig. 4.5. The

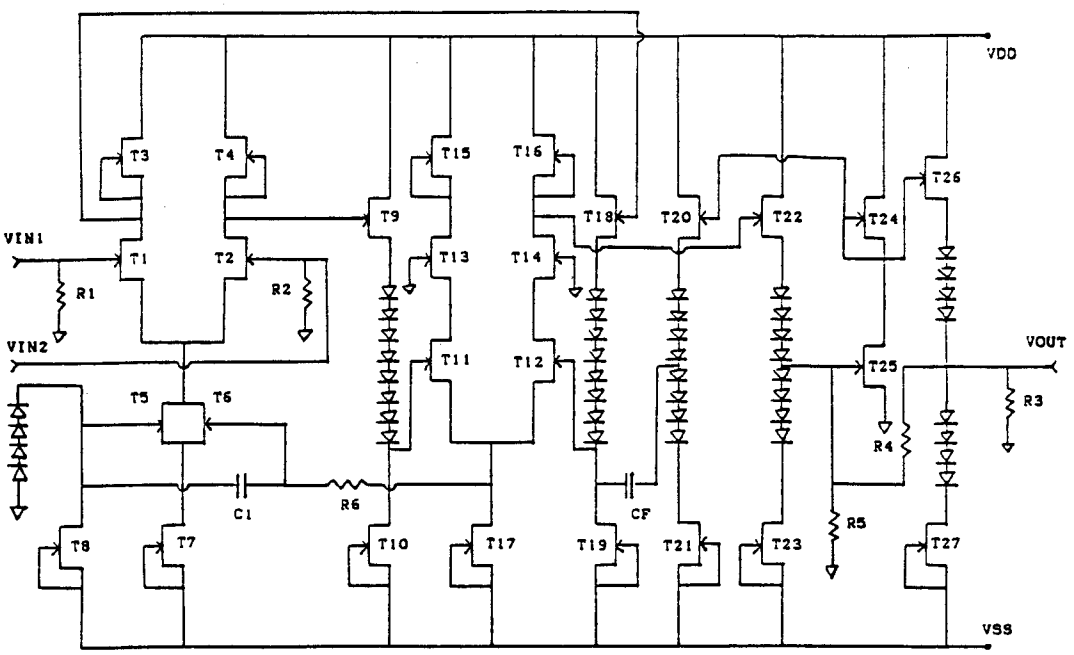


Fig. 4.5. An overall schematic of 3-stage GaAs operational amplifier.

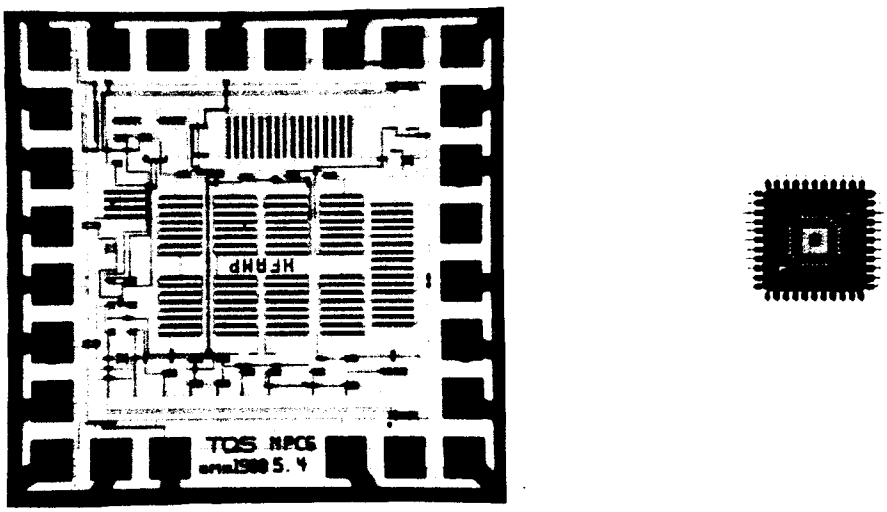


Fig. 4.6. The fabricated and packaged 3-stage GaAs operational amplifier.

fabricated and packaged 3-stage GaAs operational amplifier is shown in Fig. 4.6.

The 3-stage GaAs operational amplifier has a series shunt negative feedback loop at the output stage for stability and bandwidth improvement. The input stage(amplifier 1) is a source-coupled double-ended differential amplifier whose output signals are applied to a second stage single-ended differential amplifier(amplifier 2). The second stage is a cascode amplifier which provides high gain and wide bandwidth at high frequency. Frequency compensation feedback is applied through a source follower and a capacitor from the third stage(amplifier 3) output to one of the cascode amplifier inputs. This compensation scheme is internal pole splitting compensation with forward blocking, similar to Miller compensation[83]. The output stage drives a 50 Ω resistor to accommodate large DC currents for wide output voltage swing. A voltage regulator at the input stage and interstage level shifters with diodes are utilized for adjusting DC bias levels.

The differential and common mode gains of the input stage are given by:

$$A_{dm1} = \frac{- g_{m1}}{g_{ds3} + g_{ds1}} \tag{14}$$

$$A_{cm1} = \frac{- g_{m1}/g_{ds3}}{1 + g_{ds1}/g_{ds3} + R_s(g_{m1} + g_{ds1})} \tag{15}$$

where

$$R_s = \frac{2(g_{m5} + g_{m6} + g_{ds5} + g_{ds6}) + 2g_{ds7}}{g_{ds7}(g_{ds5} + g_{ds6})} \quad (16)$$

Two input signals, V_{in1} and V_{in2}, are connected with input protection and matching by a 50 Ω resistor. A source-coupled current source(T5, T6, and T7) is used to obtain an accurate DC operating voltage of - 2.5 V from a voltage regulator using series diode voltage drops. Mismatch induced offset is an important aspect of the performance of the differential amplifiers and produces differential voltage at the output that is indistinguishable from the signal being amplified. The offset voltage of a GaAs amplifier, which is defined as the differential input voltage required to bring the differential output voltage to zero, is a critical parameter associated with transistor mismatches of an input stage. For the input stage of this GaAs amplifier, by ignoring parasitic resistance effects, the offset can be approximated to be[81]

$$V_{off} = V_{t1} - V_{t2} + (\beta_3/\beta_1)^{1/2} V_{t3} - (\beta_4/\beta_2)^{1/2} V_{t4} \quad (17)$$

where the devices are assumed to be in saturation and β_1- β_4 correspond to the gain factors of transistors, T1-T4, in the input stage. Therefore, identical transistors(T1, T2, T3, and T4) have been used with I_{dss} = 2.1 mA, g_m = 2.3 mS, and g_{ds}

= 0.17 mS at the DC bias voltages of V_{ds} = 2.5 V and V_{gs} = 0 V. The second stage has higher gain than first input stage because there is no problem with the input offset. A cascode amplifier is a series connection of a common source amplifier and a common gate amplifier for good high frequency response. The differential and common mode gains of the cascode amplifier are given by

$$A_{dm2} = \frac{- g_{m11}(g_{m13} + g_{ds13})}{2g_{ds11}(g_{ds13} + g_{ds15}) + 2g_{ds15}(g_{m13} + g_{ds13})} \quad (18)$$

$$A_{cm2} = \frac{- g_{ds11}g_{m11}(g_{m13} + g_{ds13})}{2g_{ds13} + 2g_{ds15}[1 + X\, g_{ds11}(g_{m13} + g_{ds13})]} \quad (19)$$

where, $X = 1 + g_{m11}/g_{ds17} + 1/(g_{ds11} + g_{ds17})$. The output resistance of the cascode amplifier at the output node is $1/g_{ds15}$ = 3 KΩ. Feedback capacitance(C_F) for pole-zero cancellation is connected to the gate of T12 at the cascode amplifier input node. The gains of output stage are equal to those of input stage. Therefore, overall voltage gain of this GaAs amplifier including a series-shunt feedback at the output stage is approximately given by

$$A_v \simeq \frac{A_{dm1}\, A_{dm2}\, A_{dm3}}{1 + A_{dm3}\, R_5/(R_4 + R_5)} \quad . \quad (20)$$

A voltage regulator at the input stage and interstage level shifters with diodes are utilized for adjusting, accurately, DC bias levels. Diode sizes depend on the Schottky diode I-V characteristics in the forward region(L = 0.5 μm, W = 100 μm for V_d = 0.625 V and I_d = 2.1 mA).

The opamp is internally compensated such that single pole roll-off dominates the open-loop frequency response. Internal feedback compensation, as opposed to external compensation, is used for two reasons. First, the frequencies at which the compensation network must operate are so high (> a few GHz), that the parasitic series inductance to the external network would present an unacceptably large impedance at these frequencies. Second, feedback compensation is used because of the insensitivity of the unity-gain frequency to device parameters and because of the small required compensation capacitance. However, an internal feedback compensation can result in instabilities due to the right-half plane pole.

Frequency compensation feedback is applied through a source follower and a capacitor(C_F) which is used to create a dominant pole as well as to introduce a right-half plane zero in conjunction with the output resistance of the third stage amplifier. The new right-half plane zero caused by feed forward through C_F[83] degrades the pole response by 90 degrees at the high frequency, and also results in an overshoot of gain response. To eliminate this undesirable right-half plane zero and to get the desirable dominant

pole, we have had to choose C_F = 25 fF which is placed in series with a source follower. This opamp was drawn using the ICED graphics layout editor and analog standard cell library. Fig. 4.6 shows a chip photograph of the 3-stage GaAs operational amplifier.

In the PSPICE circuit simulations using a self-backgating 3-terminal small-signal AC MESFET circuit model, we have obtained amplifier performances for gain of A_V = 35 dB and a gain bandwidth product of f_t = 4 GHz with a ratio of g_m to g_{ds}, and of R = 13.6 which matches the actual transconductance values. Fig. 4.7. shows gain and phase response of the 3-stage GaAs operational amplifier as a

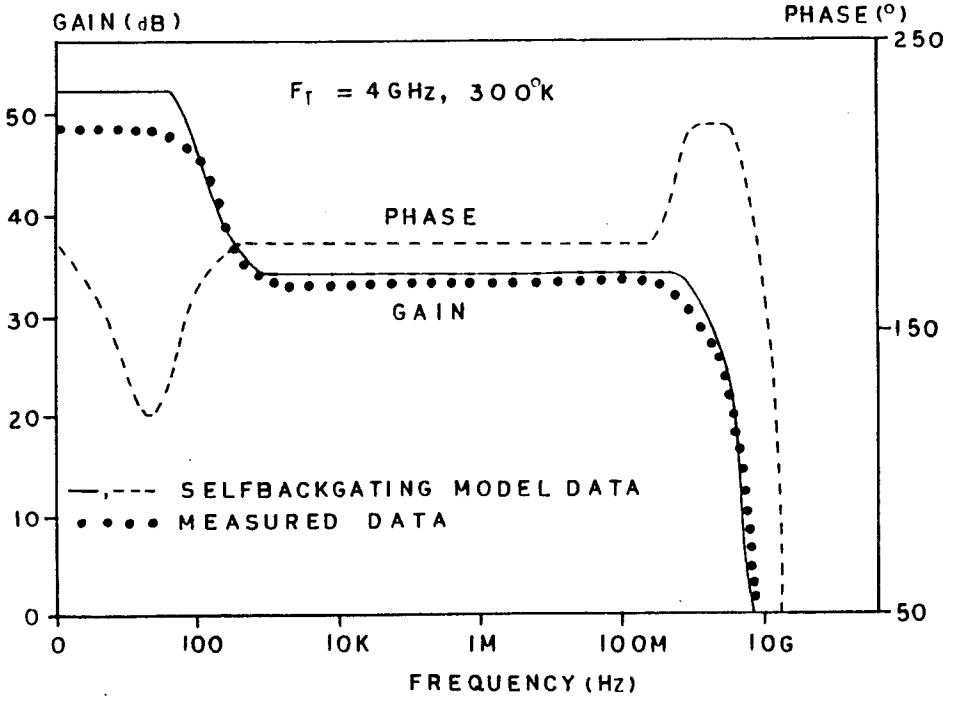


Fig. 4.7. Gain and phase response of 3-stage GaAs operational amplifier as a function of frequency.

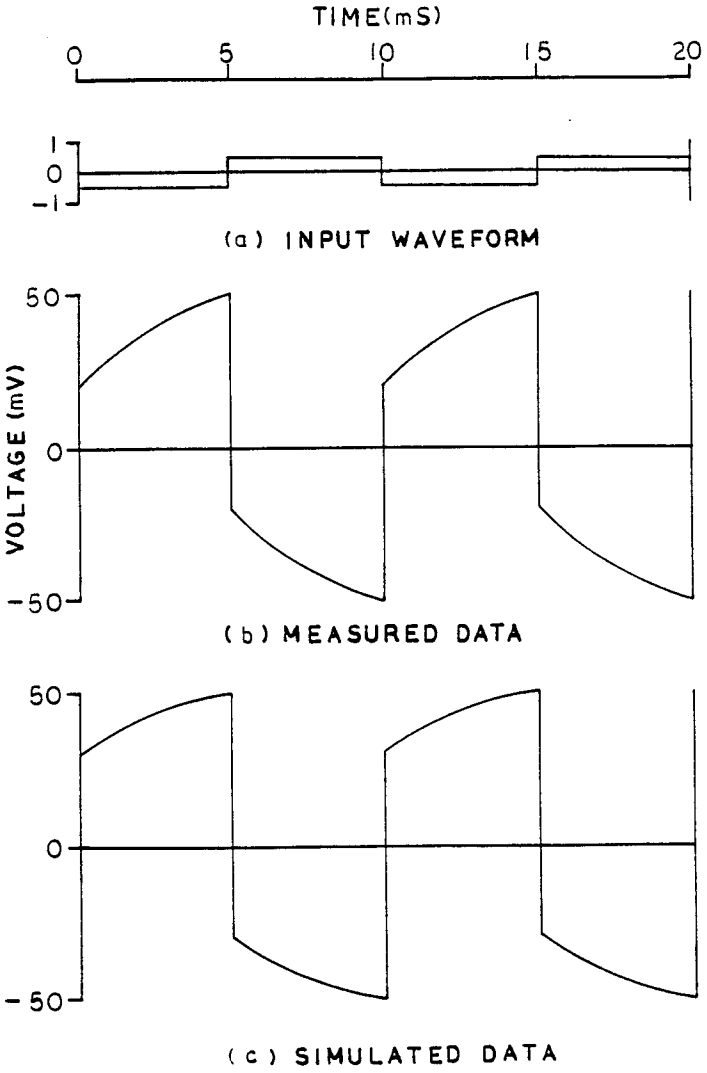
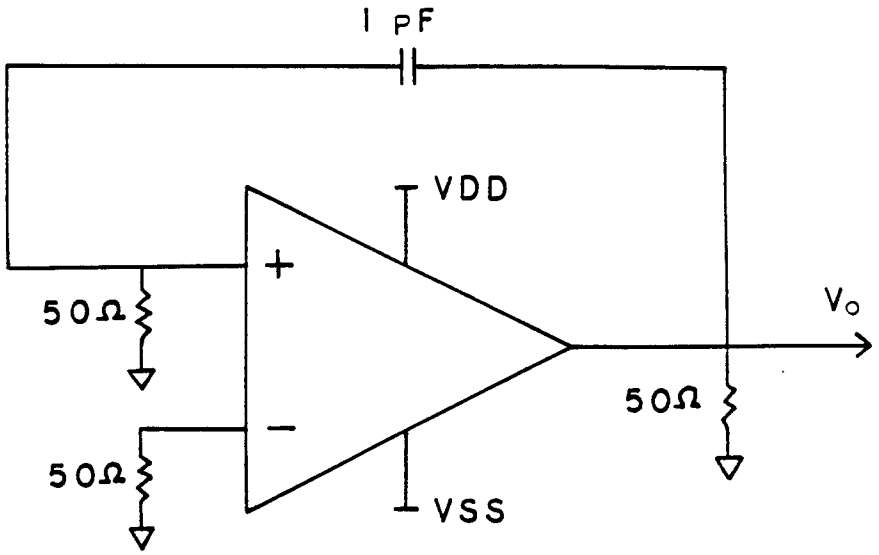
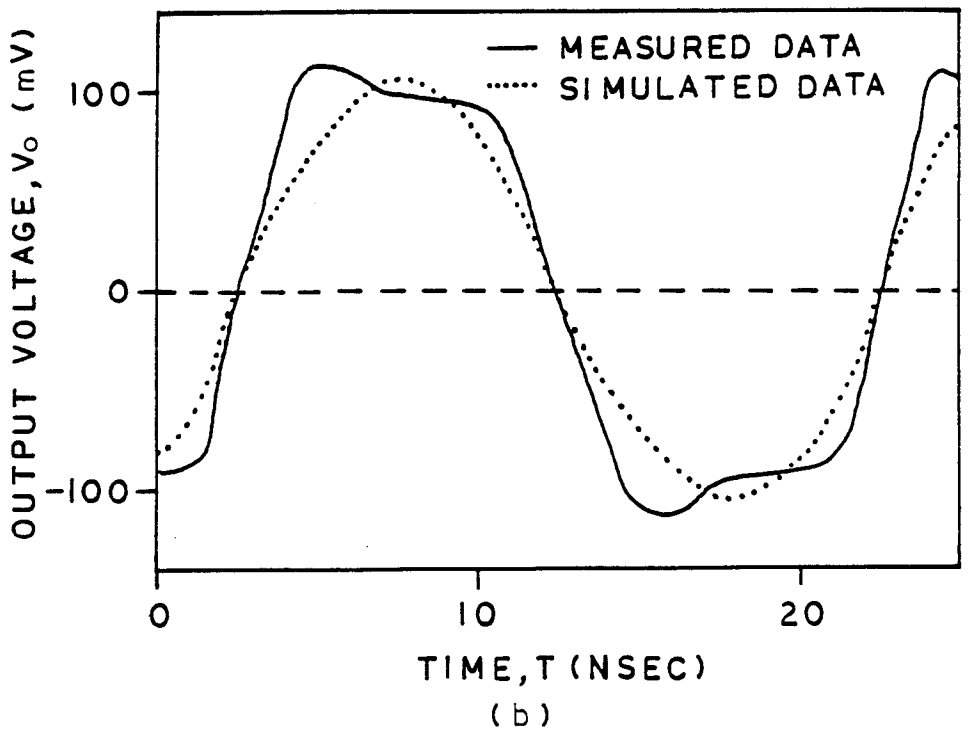


Fig. 4.8. A transient response of a 3-stage GaAs operational amplifier : (a) input waveform, (b) measured output waveform, and (c) simulated output waveform.

function of frequency, and Fig. 4.8 shows a transient response of a 3-stage GaAs amplifier. As shown in Figures, 4.7 and 4.8, measured data of this opamp corresponds to the model data except for a small discrepancy at low frequency. This may come from higher hysteresis in the low frequency region. Output current lag in the time domain and high low-



(a)



(b)

Fig. 4.9. An oscillator (a) schematic and (b) characteristic of 3-stage GaAs operational amplifier.

Electrical Parameters	Measured Data	Simulated Data		Units
		JFET Model	Self-Backgating Model	
Ids (Vds=2.5V)	4.1	4.7	4.2	mA
VT (Ids=30μA)	-1.6	-1.6	-1.6	V
Gm	4.5	6.0	4.6	mS
Gds	0.33	0.33	0.33	mS
R = Gm/Gds	13.6	18.2	13.9	-
Vd (Diode)	0.625	0.628	0.628	V
Is (Diode)	$5.0E^{-16}$	$2.6E^{-16}$	$2.6E^{-16}$	A
Av (H/L)	34/48	43	35/53	dB
ft	4	6	4	GHz
CF (Freq Comp)	25	50	25	FF
Cgs	34.5	34.5	32.1	FF
Cds	9.6	9.6	9.6	FF
Cgd	4.5	3.9	41.3	FF
Rs	9	9	9	Ω
Ls	0.2	1	1	pH
Ld	3.6	0	5.5	pH
Lg	4.6	0	6.3	pH
Output Node DC Bias	-0.01	-0.023	-0.007	V
Output Swing -0.1 < Vin < 0.1	-4 ~ 3.1	-3.8 ~ 4.9	-3.7 ~ 3.4	V
Pd (Power Dis)	0.46	0.454	0.456	W
Rin (Input Imp)	50	50	50	Ω
Ro (Output Imp)	32	31	33	Ω

Device parameters are based on W = 30 μm, L = 0.5 μm, and Vgs = 0 V, Vds = 2.5 V.

Table 4.1. The electrical characteristics of 3-stage GaAs operational amplifier.

frequency voltage gain in the frequency domain are both predicted and observed. The phase characteristic has an 80 degree margin around f_b = 1.5 GHz which is suitable and normal for opamp operation without high frequency instabilities. Fig. 4.9 shows oscillator characteristics of a 3-stage GaAs amplifier by connecting external feedback capacitance between the output terminal and the noninverting terminal. The simulated output voltage waveform is a sinusoidal wave with a period of 20 nsec and an amplitude of 100 mV. However, the measured output voltage waveform is a quite distorted sinusoidal wave with the same period as the simulated voltage output waveform. The reason may be due to the nonsaturated operation of some of the transistors which causes a signal distortion. Some of the electrical characteristics of the 3-stage GaAs operational amplifier are summarized in Table 4.1. We obtained a total power dissipation of 0.46 W with V_{dd} = 5 V and V_{ss} = - 5 V power supplies. For a range of input DC voltages of - 0.1 V to 0.1 V, the output voltage swing varies in the range of - 3.7 V to 3.4 V which allows for a suitable pulse response with a rise and a fall time of 0.1 nsec in the simulation, using the new self-backgating MESFET model. However, diode DC voltage drop in the interstage level shifters as well as transistor mismatches in the differential amplifiers are very sensitive functions of the DC bias or the operating points of the transistors. We also obtained output DC voltage(V_o) to the power supply voltage sensitivities such

as a V_o to V_{ss} sensitivity of - 1.4 V/V and a V_o to V_{dd} sensitivity of 1.4 V/V.

4.3 THE RESULTS AND DISCUSSION

We have developed a three-terminal self-backgating GaAs MESFET model and have used a high-speed GaAs operational amplifier as a linear IC design vehicle to verify low frequency characteristics observed in GaAs amplifiers. The low frequency range in the fabricated GaAs amplifier by TriQuint Semiconductor is about 0 to 300 Hz. The utility of the new self-backgating MESFET model is demonstrated by simulation of and comparison to measured data of the 3-stage GaAs amplifier's AC response, transient response, and oscillator characteristics.

In the PSPICE circuit simulations using this new model, we have obtained high-speed amplifier performances for a open-loop gain of A_v = 35 dB and a gain bandwidth product of f_t = 4 GHz in the high frequency region. The lower high-frequency gain is due to a lower ratio of g_m to g_{ds} of R = 13.6 which matches the actual transconductance values. As shown in Figures 4.7 and 4.8, the measured data of this GaAs amplifier corresponds to the model data except a small discrepancy in the low frequency region (DC - 300 Hz). The reason may be due to higher hysteresis and oscillations in the low frequency region.

The results of simulation by the self-backgating model also corespond to the measured characteristics in the output current lag, frequency dependent gain roll-off and phase notch, and power supply voltage sensitivities in this GaAs amplifier. In particular, output current lag with the time constant of 1.6 msec in the time domain and high low-frequency gain of about 50 dB in the frequency domain were both predicted and observed. The phase characteristic has an 80 degree margin around f_b = 1.5 GHz high is suitable and normal for operational amplifier operation without high frequency instabilities. The total power dissipation of 0.46 W has been obtained both in the measurement and in the simulation.

We have achieved excellent AC characteristics that are acceptable for a high-speed GaAs amplifier. However, high DC bias sensitivities due to input transistor mismatches and diode voltage differences in the level shifters are apt to limit this GaAs amplifier's performance. Also, this opamp design is meaningful in that the availability of LSI GaAs circuits has been tested using 27 MESFET's larger than previous SSI opamps. This new self-backgating MESFET model can be used to simulate GaAs linear integrated circuit designs. Also, this GaAs amplifier can be used as a corecell to extend analog circuit applications such as active filters, phase-locked loops, and A/D and D/A converters.

CHAPTER 5

CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

5.1 ACHIEVEMENTS

The objectives stated on page 8 have been successfully fulfilled. The main contributions[1-5] made throughout the course of this study can be summarized as follows:

1. We have presented channel/substrate junction modulation as the essential phenomena in a floating backgating MESFET including deep-level trap effects at the channel/substrate interface. A new self-backgating GaAs MESFET model has been developed which is able to simulate low frequency anomalies and to provide device symmetry in GaAs integrated circuit simulations. This allows a new analytical I-V characteristic equation which is quite different from previous models and implies a low EL2 concentration in the semi-insulating GaAs substrate for minimal low frequency anomalies.
2. Describing the depleted charge in the channel/substrate junction which affects the capacitances, C_{gs} and C_{ds}, as functions of V_{ds} and V_{gs}, the analytical capacitance model has been developed from the space charge distribution with two asymmetrical depletion regions in the linear, saturation, and pinch-off regions. This is necessary to provide accurate voltage dependent capacitances over a wide range of bias conditions for linear and microwave circuit design.

3. By including the channel/substrate junction modulation due to deep-level traps(EL2) and the Fermi-level pinning at the Schottky gate junction, an analytical GaAs MESFET subthershold current model has been proposed to describe the physical mechanisms of a conventional GaAs MESFET subthreshold conduction. Analysis shows that the channel mobile charge gradient caused by the applied voltages gives lateral diffusion current as the main conduction mechanism of the subthreshold current in the pinch-off region.

4. By incorporating a second order Bessel filter function as a group delay function into PSPICE, S-parameter phase errors between previous models and measured data in conventional GaAs MESFET's have been reduced by including a transit time delay in the transconductances, g_m and g_{mbs}, in this well defined self-backgating MESFET model. In particular, the important item, S_{21} phase, can be described accurately by transit time delay associated with the Schottky gate and the self-backgating in the high frequency regime at different bias conditions.

5 To demonstrate a utility of the self-backgating MESFET model for linear GaAs IC design, a 3-stage GaAs amplifier has been designed and also has been fabricated by a conventional half micron MESFET technology. This broadband GaAs amplifier has not only higher frequency performance, but also low gain due to low g_m, large offset voltages, and circuit anomalies such as output

current lag, frequency dependent gain roll-off and phase notch, and large power supply voltage sensitivities.

5.2 CONCLUSIONS

What follows are some conclusions of the work described in this thesis:

1. Since a sidegating effect can be controlled by separating device-to-device spacings by more than 1 μm for 1 V applied voltage on the layout or by isolation techniques in the process, a self-backgating effect which accounts for channel/substrate junction modulation becomes essential in modeling a conventional GaAs MESFET for accurate prediction of GaAs IC's performance. Analysis shows that transconductance variation, $G_m(f)/G_m(0)$, due to the electron emission from EL2 in the depletion width change at the edge of the Schottky gate junction, is negligible at room temperature. The output conductance variation, $G_{ds}(f)/G_{ds}(0)$, arises mainly from the channel/substrate junction which is a self-backgating effect which reduces effective channel length 2.5 times more at the high frequency than at the low frequency. The value of output conductance is 1.33 mS in a low frequency range of DC to 300 Hz and is 3.30 mS for the high frequency range for a GaAs MESFET with W = 300 μm and L = 0.5 μm. From the output conductance variation, values of R_b = 1GΩ and C_b = 1.6 pF were obtained with a time constant of

1.6 msec. The RC network consists of 2 internal nodes, where one simulates low frequency anomalies and the other one allows for the device symmetry by using a switching resistance(R_S) of about 10 GΩ. The drain current lag effect, the transient lag of the drain current, is caused by the charging or discharging of deep-level traps with multiple time constants at the interface between the channel and the semi-insulating substrate. These series of low frequency anomalies can be reduced by using a low EL2 concentration semi-insulating GaAs substrate. Therefore, for the optimal device design in a conventional GaAs MESFET technology, there is a trade-off between the processing complexity, which might be a low yield and a high cost, and the EL2 minimization which can be achieved by the heat treatment and the use of the epitaxial layer on the semi-insulating GaAs substrate.

2. A new 3-terminal self-backgating GaAs MESFET model has been developed with a frequency dependent I-V curve and voltage dependent capacitance model. The results of simulation by this model correspond to the measured characteristics in the frequency dependent transconductance and output conductance, drain current, and hysteresis in the saturation region as well as describe the voltage dependence of the capacitance. Lower hysteresis and a higher saturation current in the AC curve (100 KHz) as compared to the DC curve (0.1 Hz)

are both predicted and observed at the saturation region. The voltage dependent $C_{gs}(V_{gs}, V_{ds})$ and $C_{gd}(V_{gs}, V_{ds})$ comparisons show good agreement between measured data and computed model data with a uniform channel doping concentration of 3×10^{16} cm^{-3}, EL2 concentration of 1×10^{16} cm^{-3}, and a channel depth of 0.1 μm except in the high drain voltage saturation region for fitting $C_{gd}(V_{gs}, V_{ds})$. The reason may be the rapid reduction of charge variation in the high voltage drain end. This capacitance analysis can be used to reduce error more than in Larson's case[15] by including the channel/substrate junction charge modulation. This self-backgating MESFET model which provides accurate voltage dependent capacitances, and transit time delay dependent transconductances can be used to simulate low frequency effects in GaAs linear integrated circuit design in conventional MESFET technology.

3. Furthermore, for a complete GaAs MESFET model, an analytical subthreshold model has been developed and scattering parameter dependence on a transit time delay in a self-backgating GaAs MESFET model is described for MMIC design. The GaAs MESFET subthreshold characteristics have been analyzed with a self-backgating effect including deep-level traps and Fermi-level pinning at the Schottky gate junction to develop an analytical model. This analysis gives the exponential relationship for I_{sub} vs. V_{gs} due to the channel

electron charge gradient and the nearly linear relationship for I_{sub} vs. V_{ds} due to the threshold voltage dependence on V_{ds}. The subthreshold conduction region has been defined as the regime of lateral current flow from the threshold voltage(V_t) down to the onset of gate voltage at which the subthreshold current(I_{sub}) begins to increase due to a drift current. The slope of $\log(I_{sub})$ vs. V_{gs} in the model yields 9 at 300 K which corresponds to that of measured data which is 7. This model can be used to simulate the low current characteristics of conventional GaAs MESFET's. The previous phase and magnitude errors in S-parameter can be eliminated by incorporating a transit time delay of 4 psec in the self-backgating model. For both bias conditions at V_{gs} = 0 V, V_{ds} = 2.5 V and V_{gs} = - 0.5 V, V_{ds} = 4.0 V, there are no discrepancies between measured S-parameters extracted using AC simulation in PSPICE. The measured data for S_{21} and S_{12} is more sensitive than that of S_{11} and S_{22} to bias voltage changes. Therefore, the inclusion of transit time delay which accounts for the delay under the gate and the self-backgate gives a better fit to the data and, in particular, can match S_{21} phase with minimal error which is hard or impossible to achieve unless a time delay is included. A GaAs AC nonlinear large-signal model based on the self-backgating MESFET model has been developed. In the time domain, AC large signal characteristic comparisons show

good agreement between measured data and simulated model data. With the drain voltage of 2.5 V and the input signal at the gate which is a sinusoidal wave with a magnitude of 2 V and a frequency of 1 MHz, both measured data and simulated data have nonlinear characteristics in the time domain, which mean the harmonic distortions in the frequency domain. Also, the 2 x 2 matrix expression in terms of internal variables, V_{gs} and V_{ds}, are analyzed in the frequency domain. As a convenient method for extracting S-parameters, a new circuit configuration can be used to evaluate microwave characteristics of MESFET's for MMIC design.

4. The utility of the new self-backgating MESFET model is demonstrated by simulation of and comparison to measured data of a 3-stage GaAs operational amplifier for linear GaAs IC applications. In the PSPICE circuit simulations using this model, we have obtained amplifier performances for the open-loop gain at high frequencies of A_v = 35 dB and a gain bandwidth product of f_t = 4 GHz with a ratio of g_m to g_{ds} of R =13.6 which matches the measured data. Measured data of this opamp in the frequency domain corresponds to the model data except for a small discrepancy at low frequencies. This may come from higher hysteresis and oscillations in the low frequency region. Output current lag in the time domain and high low-frequency voltage gain in the frequency domain are both predicted and observed as anomalies

of GaAs amplifiers. We have obtained a total power dissipation of 0.46 W with V_{DD} = 5 V and V_{SS} = - 5 V power supplies. For a range of input DC voltages of - 0.1 V to 0.1 V, the output voltage swing varies in the range of - 3.7 V to 3.4 V which allows for a suitable pulse response with a rise and fall time of 0.1 nsec. The simulation results of the GaAs amplifier by this model correspond to the measured characteristics in the output current lag, frequency dependent gain roll-off and phase notch, and large power supply voltage sensitivities.

5.3 SUGGESTIONS FOR FUTURE WORK

In the GaAs MESFET modeling and circuit applications areas, there are many more advanced research for the improvement of device characteristics and for development of high performance circuits. What follows are some suggestions for future work that could be investigated.

1. All of the existing GaAs MESFET model are either completely empirical models or analytical models, such as the self-backgating MESFET model which use the assumptions of uniform doping concentrations and constant low field mobility in the channel. Therefore, more advanced GaAs MESFET models are needed which include nonuniformly doped impurity profiles and more accurately describe the carrier transport in the active region for accurate conventional GaAs MESFET models.

2. As discussed in chapter 3, the developed analytical capacitance model is a charge-based model including channel/substrate junction modulation due to the presence of EL2 in the substrate and can overcome inaccurate voltage dependent capacitance in previous models. Since the depleted charge in the channel including deep-level traps is time dependent, a non-quasi static capacitance model has to be considered for accurate transient analysis.
3. Traps dominate many aspects of GaAs MESFET behavior. Deep-level flaws at the surface and channel/substrate interfaces have to be investigated to solve noise and performance problems in conventional GaAs MESFET's. Low frequency anomalies dependence on temperature and the use of distributed resistive and capacitive networks for accurate semi-insulating models are recommended as interesting research areas.
4. Based on the self-backgating MESFET model, which has been verified by both prediction and observation in GaAs opamp's anomalies, analog GaAs IC's design strategies are presented in chapter 4. The realization of more advanced precision analog GaAs IC's is of considerable interest for a wide range of sample-analog applications including switched-capacitor filters, transversal filters, phase-locked loops, A/D converters, and D/A converters.

5. Developing the EL2 optimization techniques to reduce low frequency anomalies might be useful for the high performance of conventional GaAs MESFET's. Also, an interface of linear, microwave, and optical circuit modules will be an important factor for the system insertion of GaAs integrated circuits.

REFERENCES

[1] M.K. Lee, L. Forbes, T. Hallen, and P.Tuinenga, "An analytical self-backgating GaAs MESFET model including deep-level trap effects," IEEE IEDM Technical Digest, pp. 315-318, Dec. 1989.

[2] M.K. Lee, L. Forbes, and T. Hallen, "Design of a GaAs operational amplifier using self-backgating model including deep-level trap effects," Proc. IEEE Int. Sym. on Circuits and Systems, pp. 2287-2290, May 1990.

[3] M.K. Lee, and L. Forbes, "A self-backgating GaAs MESFET circuit model for low frequency anomalies; Part I: Sub-circuit implementation," Technical Report No. MERC. 1/89, Tektronix, Beaverton, OR, USA, May 1989.

[4] M.K. Lee and L. Forbes, "A self-backgating GaAs MESFET model for low frequency anomalies," IEEE Trans. Electron Devices, Oct. 1990 (in press).

[5] M.K. Lee and L. Forbes, "Scattering parameter dependence on a transit time delay in a self-backgating GaAs MESFET model," Proc. Asia-Pacific Microwave Conference, Sept. 1990 (in press).

[6] J.M. Golio, M.G. Miller, G.N. Maracas, and D.A. Johnson, "Frequency-dependent electrical characteristics of GaAs MESFET's," IEEE Trans. Electron Devices, vol. 37 , No. 5, pp. 1217-1227, May 1990.

[7] S.M. Sze, Physics of semiconductor devices, 2nd Ed., John Wileg & Sons, New York, 1981.

[8] A.K. Srivasta, "Gallium arsenide," IEEE Potentials, pp. 23-25, Oct. 1989.

[9] S.Ilhun and T.T. Wei, "Modeling deep-level traps in GaAs MESFET's," IEEE Trans. Electron Devices, vol. ED-36, pp. 632-640, Apr. 1989.

[10] C. Camacho-Penalosa, "Modeling frequency dependence of output impedance of a microwave MESFET at low frequencies," Electron. Lett., pp. 528-529, 1985.

[11] S.M.Ebeid and Minondo, "The roles of the surface and bulk of the semi-insulating in low-frequency anomalies of GaAs integrated circuits," IEEE Trans. Electron Devices, vol. ED-32, pp.632-642, Mar. 1985.

[12] P.H. Ladbrooke and S.R. Blight, "Low-field low-frequency dispersion of transconductance in GaAs MESFET's with implications for other rate-dependent

anomalies," IEEE Trans. Electron Devices, vol. ED-35, pp.257-266, Mar. 1988.

[13] D.J.Miller and M. Bujatti, "Mechanisms for low-frequency oscillations in GaAs FET's," IEEE Trans. Electron Devices, vol. ED-34, pp. 1239-1244, June 1987.

[14] H. Goronkin, G.N. Maracas, "Low frequency oscillations in undoped GaAs as a prove to deep level parameters," IEEE IEDM Technical Digest, pp. 182-185, 1984.

[15] L. Larson,"An improved GaAs MESFET equivalent circuit model for analog integrated circuit simulation," IEEE Trans, Microwave Theory Tech., vol. MTT-30, pp. 220-230, 1988.

[16] N. Scheinberg, R. Bryruns, and R. Goyal, "A low-frequency GaAs MESFET circuit model," IEEE J. Solid-State Circuits, vol. SC-23, pp.605-608, 1988.

[17] C.T.M. Chang, T. Vrotsos, M.T. Frizzell, and R. Carroll, "A subthreshold current model for GaAs MESFET's," IEEE Electron Device Lett., vol. EDL-8, pp. 69-72, Feb. 1987.

[18] C.Y. Chen, J. Bayruns, R.J. Bryruns, and N. Scheinberg, "Reduction of low-frequency noise in a DC-2.5 GHz GaAs amplifier," IEEE Int. GaAs IC Sym., pp. 289-292, 1988.

[19] C.Y. Su, H. Rohdin, and C. Stolte, "1/f noise in GaAs MESFETs," IEEE IEDM Technical Digest, pp.601-604, 1983.

[20] R.A. Pucel, D.J.Masse, and C.F. Krumn, "Noise performance of gallium arsenide field-effect transistors," IEEE J. Solid-State Circuits, vol. Sc-11, pp.242-255, Apr. 1976.

[21] A.F. Podell, "A functional GaAs FET noise model,' IEEE Trans. Electron Devices, vol. ED-28, pp.511-517, 1981.

[22] B. Hughes, N.G. Frenandez, and J.M. Gladstone, "GaAs FET's with a flicker-noise corner below 1 MHz," IEEE Trans. on Electron Devices, vol. ED-34, pp. 733-741, Apr. 1897.

[23] A.P. Podell, "GaAs for high-speed analog ICs," IEEE Int. Solid-State Circuits Conference Technical Digest, pp. 211, 1988.

[24] A. Madjar, "A fully analytical AC large-signal model of the GaAs MESFET for nonlinear network analysis and design," IEEE Trans. Microwave Theory Tech., vol. MTT-36, pp. 61-67, Jan. 1988.

[25] D.L. Peterson, A.M. Davio, and B. Kim, "A GaAs FET model for large-signal application," IEEE Trans. Microwave Theory Tech., vol. MTT-22, pp. 43-48, 1974.

[26] J.M. Golio, J.R. Hauser, and P.A. Blakey, "A large-signal GaAs MESFET model implemented on SPICE," IEEE Circuits and Devices Magazine, pp. 21-30, Sept. 1985.

[27] A. Madjar and F.J. Rosenbaum, "A large-signal model for the GaAs MESFET," IEEE Trans. Microwave Theory Tech., vol. MTT-29, pp. 781-788, Aug. 1981.

[28] R.S. Tucker and C. Rauscher, "Modeling the 3rd-order intermodulation distortion properties of a GaAs FET," Electronics Letters, vol. 13, pp. 508-509, Aug. 1977.

[29] A.M. Khadr and R.H. Johnston, "Distortion in high-frequency FET amplifiers," IEEE J. Solid-State Circuits, vol. SC-9, pp. 180-189, Aug. 1974.

[30] Y. Tajima, B. Wrona, and K. Mishima, "GaAs FET large-signal model and its application to circuit designs," IEEE Trans. Electron Devices, vol. ED-28, pp.171-175, Feb. 1981.

[31] TOUCHSTONE, User's manual, Version 1.3, EEsof, Westlake Village, CA, April 1985.

[32] L. Forbes, P. Canfield, R. Gleason, and A. McCamant, "Low frequency noise in GaAs FETs," Proc. Semi-Insulating III-V Materials Conf., pp. 392-396, 1984.

[33] Joseph Mun, (ED.), GaAs Integrated Circuits, Macmillan Publishing Co., New York, 1988.

[34] W.S. Lee and J. Mun, "Improved negative feedback technique to reduce drain conductance of GaAs MESFETs for precision analogue ICs," Electron. Lett., pp. 705-707, 1987.

[35] L. Larson, Galliun arsenide switched-capacitor circuits for high-speed signal processing, Ph.D. Thesis, Dept. of Electrical Engineering, University of California, Los Angeles, 1986.

[36] M. Rocchi, "Status of the surface and bulk parasitic effects limiting the performance of GaAs IC," Physics 129B, pp. 119-138, 1985.

[37] J.F. Wager and A.J. McCamant, "GaAs MESFET interface considerations, "IEEE Trans. Electron Devices, vol. ED-34, pp. 1001-1007, May 1987.

[38] Y. Fuisaki and N. Matsunaga, "The origin of gate hysteresis and gate delay of MESFETs appear under low frequency operation," IEEE Int. GaAs IC Sym., pp 235-238, 1988.

[39] S. Sriram and M.B. Das, "Characterization of electron traps in ion-implanted GaAs MESFET's on undoped and Cr-doped LEC semi-insulating substrates," IEEE Trans. Electron Devices, vol. ED-30, pp. 586-592, June 1983.

[40] P.F. Lindquist, "A model relating electrical properties and impurity concentrations in semi-insulating GaAs," J. Appl. Phys. 48(3), pp. 1262-1267, Mar. 1977.

[41] W.B. Leigh, J.S. Blakemore, and R.Y. Koyama, "Interfacial effects related to backgating in ion-implanted GaAs MESFET's," IEEE Trans. Electron Devices, vol. ED-32, pp. 1835-1841, Sept. 1985.

[42] C.P. Lee, "Influence of substrates on the electrical properties of GaAs FET devices," Proc. Semi-Insulating III-V Materials Conf. pp. 324-335, 1982.

[43] P.Canfield and L.Forbes, "Suppression of drain conductance transients, drain current oscillations and low-frequency generation-recombination noise in GaAs FET's using buried channels," IEEE Trans. Electron Devices, vol. ED-33, pp.925-928, 1986.

[44] C Kocot and C.Stolte, "Backgating effect in GaAs FET's," IEEE Trans. Microwave Theory Tech., vol. MTT-30, pp. 963-968, 1982.

[45] F.N.H. Robinson, Noise and fluctuations in electronic devices and circuits, Clarendon Press, Oxford, 1974.

[46] F.N. Hooge, "1/f noise in no surface effect," Phys. Lett. A, 29, pp. 139-140, 1969.

[47] P.O. Lauritzen, "Low frequency generation noise in junction field effect transistors," Solid-State Electron., vol. 8, pp. 41-58, 1965.

[48] G.M. Martin, J.P. Farges, G. Jacob, and J.P. Hallais, "Compensation mechanisms in GaAs," J. Appl. Phys. 51(5), pp. 2840-2852, May 1980.

[49] W. Curtice, "GaAs MESFET modeling and nonlinear CAD," IEEE Trans. Microwave Theory Tech., vol. MTT-36, pp. 220-230, 1988.

[50] H. Statz, P. Newman, I.Smith, R. Pacel, and H. Hauss, "GaAs FET device and circuit simulation in SPICE," IEEE Trans. Electron Devices, vol. ED-34, pp. 160-169, 1987.

[51] W.R. Makinley, "GASSIM: A circuit simulator for large signal GaAs circuit," IEEE Custom Integrated Circuit Conference, pp. 628-631, 1986.

[52] W.R. Curtice and R.L. Camisa, "Self-consistent GaAs FET models for amplifier design and device diagnostics," IEEE Trans. Microwave Theory Tech., vol. MTT-32, MTT-32, pp. 1573-1578, 1984.

[53] L.F. Eastman and M.S. Shur, "Substrate current in GaAs MESFET's," IEEE Trans. Electron devices, vol. ED-26, pp. 1359-1361, Sept. 1979.

[54] S. Liu and L.W. Nagel, "Small signal MOSFET models for analog circuit design," IEEE J. Solid-State Circuits, SC-17, pp. 983-998, Dec. 1982.

[55] S.G. Peltan, S.I. Long, and S.E. Butner, "An accurate DC SPICE model for the GaAs MESFET," Proc. IEEE Int. Sym. Circuits and Systems, pp. 6-10, 1982.

[56] N. Scheinberg, R. Bayruns, and S. Bhari, "MESFET model improves accuracy, cuts CPU time," Microwaves & RF, pp. 71-75, Apr. 1987.

[57] S.E. Sussman-fort, S.Narasimhan, and K. Mayaram, "A complete GaAs MESFET computer model for SPICE," IEEE Microwave Theory Tech., vol. MTT-32, pp. 471-473, Apr. 1984.

[58] L.W. Nagel, SPICE2: A computer program to simulate semiconductor circuits, Memorandum ERL-M520, Electronics Research Laboratory, University of California, Berkeley, 1982.

[59] E. Cohen, Program reference for SPICE2, Memorandum ERL-M592, Electronics Research Laboratory, University of California, Berkeley, 1976.

[60] M.Sango, O. Oitzalis, L. Lerner, C. McGuire, P. Wang, and W.Childs, "A GaAs MESFET large-signal circuit model for nonlinear analysis," IEEE Int. Microwave Sym. Dig., pp.1053-1056, 1988.

[61] M. Ogawa and T. Kamiya, "Device modeling of ion-implanted GaAs MESFET including compensation mechanism of SI substrate," Extended Abstracts of the 15th Conference on Solid State Devices and Materials, Tokyo, pp. 77-80, 1983.

[62] M. Ogawa and T. Kamiya, "Correlation between the backgating effect of a GaAs MESFET and the compensation

mechanism of a semi-insulating substrate," IEEE Trans. Electron Devices, vol. ED-32, pp.571-576, 1985.

[63] T. Takada, K. Yokoyama, M. Ida, and T. Sudo, "A MESFET variable-capacitance model for GaAs integrated circuit simulation," IEEE Trans. Microwave Theory Tech., vol. MTT-30, pp. 719-723, 1982.

[64] T. H. Chen and M.S.Shur, "A capacitance model for GaAs MESFET's," IEEE Trans. Electron Devices, vol. ED-12, pp. 883-891, 1985.

[65] R.E. Neidert and C.J. Scott, Computer program for microwave GaAs MESFET's modeling, NRL Report No.8561, Feb. 1982.

[66] A.M. Grebene and P.D. Gandhi, "General theory for pinched operation of the junction-gate FET, "Solid-State Electronics, vol. 12, pp. 573-589, 1969.

[67] J.D. Marshall and J.D. Meindl, "An analytical 2-D model for silicon MESFET's," IEEE Trans. Electron Devices, vol. ED-35, pp.373-383, Mar. 1988.

[68] J.R. Brews, Physics of the MOS transistor, Applied Solid State Science Supplement 2A, New York: Academic, pp. 1-120, 1981.

[69] H.A. Watson, Microwave semiconductor devices and their circuit applications, New York: McGraw-Hill, 1969.

[70] T. Hallen, private note, Tektronix, Beaverton, OR.

[71] F. Weinert, "Scattering parameters speed design of high-frequency transistors of circuits," Electronics, September 5, 1966.

[72] W.R. Curtice and M. Ettenberg, "A nonlinear GaAs model for use in the design of output circuits for power amplifiers," IEEE Trans. Microwave Theory Tech., vol. MTT-33, pp. 1383-1393, Dec. 1985.

[73] H. Fukui, "Determination of the basic device parameters of a GaAs MESFET," Bell Syst. Tech. J., vol. 58, pp. 771-778, Mar. 1979.

[74] Michael, Shur, GaAs device and circuits, Plenum Press, New York, 1987.

[75] R.C. Eden, "The development of the first LSI gate integrated circuits and the path to the commercial market," Proc. IEEE, vol. 76, pp.756-777, July 1988.

[76] T. Naegele, "Hard times in rad-hard," Electronics, pp. 82-88, May 1989.

[77] N. Scheinberg, "High-speed GaAs operational amplifier," IEEE J. Solid State Circuits, vol. SC-22, pp. 522-527, Aug. 1987.

[78] A.S. Fiedler, The design and computer simulation of a GaAs MESFET integrated operational amplifier," M.S. Thesis, Dept. of Electrical and Computer Engineering, University of California, Santa Barbara, 1984.

[79] W.Baechtold, "Si and GaAs .5 μm-gate Schottky barrier field-effect transistors, "Electronics Letters, vol. 9, pp. 232-234, May 1973.

[80] L.E. Larson, G.C. Temes, and S. Law, "Comparison of amplifier gain enhancement techniques for GaAs MESFET analogue integrated circuit," Electron. Lett., pp.1138-1139, 1986.

[81] L. E. Larson, J.F. Jensen, H.M. Levy, P.T. Greiling, and G. C. Temes, "GaAs differential amplifiers," IEEE Int. GaAs IC Sym., pp. 19-22, 1985.

[82] N. Kanopoulos, Galliun arsenide digital integrated circuits - a system perspective, Prentice-Hall, Inc., New Jersey, 1989.

[83] Yannis P. Tsividis and Paul Gray, "An integrated NMOS operational amplifier with internal compensation," IEEE J. Solid State Circuits, vol. SC-11, Dec. 1978.