AN ABSTRACT OF THE THESIS OF

Sung-Yong Kim (Name) for the Master of Science (Degree) in

Electrical Engineering (Major) presented on March 17, 1972 (Date)

Title: INFLUENCE OF SURFACE FIELDS ON SHALLOW PLANAR-JUNCTION BREAKDOWN VOLTAGES

Abstract approved: James C. Looney

The influence of surface fields on the breakdown voltage is studied experimentally for p^+-n silicon diodes with a junction depth of 0.5 μm in order to improve the curvature-limited breakdown of the diffused, shallow-collector junction of a microwave transistor.

Devices with a gap in the gate metal electrode are also studied to determine the feasibility of a simple fabrication process for a microwave transistor.

It is found that the breakdown voltage (BV) can be modulated by the voltage (V_G) of the metal electrode if the junction periphery is completely covered by the gate but not if there is a gap in the gate electrode.

Measurements are given which show that, in the region where the surface is depleted, the breakdown voltage is given by $BV = m\ V_G$ + constant.

The slope m approaches unity for low substrate impurity concentrations and for small oxide thicknesses.

Furthermore, the slope m is steeper for a circular diode than that of a rectangular diode; also, breakdown voltage is higher for a circular diode by 3% for 1 ohm-cm and 6% for 5 ohm-cm substrates.

For a high-voltage microwave transistor, the most desirable model is proposed in this project by the physical configuration in which the gate metal is connected to the diffused emitter or base region, and the disadvantages due to the parasitic capacitances are also discussed.

INFLUENCE OF SURFACE FIELDS ON SHALLOW PLANAR-JUNCTION BREAKDOWN VOLTAGES

by

Sung-Yong Kim

A THESIS

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Master of Science

June 1972

APPROVED:

Redacted for Privacy

Associate Professor of Electrical and Electronics Engineering
in charge of major

Redacted for Privacy

Head of Department of Electrical and Electronics Engineering

Redacted for Privacy

Dean of Graduate School

Date thesis is presented March 17, 1972

Typed by Erma McClanathan for Sung-Yong Kim

ACKNOWLEDGMENT

The author would like to express his deep appreciation to Professor James C. Looney for his suggestions and assistance during the course of this study; to Dr. S. B. Park and Mr. Woo Y. Kim for constant encouragement and support.

Encouragement from my parents is also acknowledged with deep gratitude.

TABLE OF CONTENTS

LIST OF APPENDICES

LIST OF FIGURES

Figure Page

INFLUENCE OF SURFACE FIELDS ON SHALLOW PLANAR JUNCTION BREAKDOWN VOLTAGE

I. INTRODUCTION

The development of silicon planar technology solved many of the stability and reliability problems of the semiconductor device but also brought along some new difficulties. The curvature of the planar junction near the surface increases the electric field. This results in the reduction of the reverse breakdown voltage of the planar p-n junction as compared to the respective bulk breakdown voltage of the equivalent plane junction (11, 12, 13, 21, 23).

Moreover, planar passivated junctions are influenced in several respects by the insulating layer and its surface (9, 16, 17, 18).

The purpose of this project is to increase the voltage capability of planar shallow junctions for microwave applications.

In silicon microwave transistors where junctions are extremely shallow (less than 0.5 micrometer (μm)) with very fine geometry, the breakdown voltage is almost always determined by the radius of curvature at the edge of the base.

Microwave transistors are further limited in selection of material by the collector capacitance versus depletion-layer transit-time tradeoff.

Present-day microwave transistors are usually built on 0.25 - to - 5 Ω-cm epitaxial material and almost all are planar silicon n-p-n (2:1174).

A silicon n-p-n transistor has a higher cutoff frequency because the minority carrier (electrons) mobility in the base region and majority scattering-limited velocity in the collector region are larger than the corresponding quantities for a p-n-p transistor (20:288).

However, small-signal microwave transistors which are built on 0.25-to-1 Ω-cm usually have a lower breakdown voltage ($\approx$20 v) because of the shallow diffusions used and thus highly susceptible to contamination. This limitation of shallow planar junction breakdown in the collector region can be circumvented to some degree by either including a guard ring or mesa etching if the edge of the mesa could be passivated effectively. But the method of mesa etching or a low angle beveling to reduce the lateral electric field on the surface of the p-n junction has stability difficulties owing to passivation problems. Also, this method consumes a large surface area, and the process is expensive.

A lightly doped deep guard ring around the junction has been used (4) in order to obtain the true bulk breakdown in the central region of the device. But this structure needs a special deep diffusion step for a guard ring and it is sensitive to the usual surface problems.

Ithantola (10) used a multiple-guard-ring (MGR) structure, which did not require a special deep diffusion step, for a reliable, high-voltage p-n junction. This structure is, however, best applicable to power devices with a large geometry (10:30).

A metallic field plate structure on top of the junction is studied in order to increase the curvature-limited breakdown voltage and eliminate the surface problems.

The effect of the surface field on the breakdown voltage of planar silicon junctions has been studied by many investigators (1, 3, 8, 19), yet insufficient information is available for its practical application to the microwave transistor.

An investigation of the effect of surface fields on the breakdown voltage is studied in this project for p^+-n diodes with a junction depth of 0.5 μm.

This paper is divided mainly into three parts. The first part deals with the theoretical considerations of junction breakdown, factors influencing surface breakdown and a technique of defining the surface problems.

The second part is concerned with design considerations and fabrication processes. All considerations in this part are done with the intention of applying to the microwave transistor. Thus 1 ohm-cm and 5 ohm-cm materials are used as the substrates and n-type epitaxial wafers with a low dislocation density are selected. Two types of

geometry configurations (circular and rectangular structures with approximately the same active area) are designed in order to investigate the different curvature effects on the junction breakdown due to different diffusion masks.

Three rectangular diodes, which have a different spacing between the gate metal and base contact lead, are designed to determine the feasibility of a simple fabrication process for a microwave transistor.

The effect of surface fields on the junction breakdown is studied in the gap region.

The third part is concerned with the experimental evaluation of the breakdown voltage versus the effective gate potential and investigation of spacing effect on the junction breakdown voltage.

The experimental results are also discussed in view of geometry characteristics, effects of substrate impurity concentration and oxide thickness.

Finally, the voltage enhancement, which is defined as the reverse breakdown voltage that results when the gate metal is connected to the diffused area, is studied from the slope of the characteristic curve.

II. BASIC BREAKDOWN MECHANISMS IN P-N JUNCTION

Reverse voltage breakdown in a semiconductor p-n junction may be defined operationally as the voltage point at which the reverse current increases drastically with a small increase in reverse voltage. Discounting surface effects, the two main mechanisms are zener breakdown (internal field emission) and avalanche breakdown which is due to carrier multiplication.

Appreciable current due to internal field emission occurs only at relatively high electric field strengths (16:257). In order to obtain such a high field, the junction must have relatively high impurity concentrations on both the p and n sides. In most cases, the breakdown in narrow junctions with a breakdown voltage below four volts is caused primarily by tunneling, and such a breakdown is generally referred to as the zener breakdown (24:357).

The avalanche multiplication (or impact ionization) is the most important mechanism in the junction breakdown, since the avalanche breakdown voltage imposes an upper limit on the reverse voltage for most diodes and on the collector voltage of all transistors (20:111).

If the field within the depletion region is not too high, the generation process of an electron-hole pair by thermal means will simply lead to the regular reverse current. However, if the electric field is high enough, the

generated electron and hole will gain enough kinetic energy before colliding with the lattice so that they will be able to shatter silicon-to-silicon bonds leading to the formation of other electron-hole pairs by the impact of the electron (6:193). In turn, they will again be able to ionize and create other electron-hole pairs in a like manner, and so on. This process is called the avalanche process.

Since the avalanche breakdown voltage is defined as the voltage where multiplication factor approaches infinity, the breakdown condition is derived by the ionization integral (20:113, 24:358). Owing to the strong dependence of the ionization rates on the field and the above breakdown condition, the breakdown voltage (BV), the maximum electric field (Em), and the depletion layer width (W) for a given semiconductor can be calculated.

Avalanche breakdown voltage was calculated by the following approximate equation (20:114) in order to define the plane junction breakdown voltage:

$$BV = 60(Eg/1.1)^{3/2}(N_B/10^{16})^{-3/4} \text{ volts} \qquad \text{(Eq. 1)}$$

where N_B is the ionized substrate impurity concentration and Eg is the energy band gap.

Thus, for the abrupt junction, the plane junction breakdown voltages (BV_{plane}) of 1 Ω-cm and 5 Ω-cm of n-type silicon were calculated as 96 and 330 volts respectively.

III. JUNCTION BREAKDOWN VOLTAGE IN THE PLANAR TECHNOLOGY

In the planar p-n junctions which are formed by the planar technology, the reverse I-V characteristics are, in fact, typically dominated by imperfections such as the structural imperfection, silicon-dioxide passivation, microplasma sites and the precipitates in the space-charge region of the p-n junction (12:175, 9:980). These imperfections result in limiting the breakdown voltage to lower than that expected from avalanche calculation on the doping level.

A nonuniform breakdown voltage which is caused by the localized current has no significance in this project because the breakdown due to microplasma site can be controlled within a volt or two of the bulk breakdown (4:1591).

The most dominant factor which reduces the breakdown voltage in a planar junction is the structural imperfection due to the lateral diffusion from an oxide window edge. This effect is most important for shallow junction devices.

Aside from this factor, planar oxide-passivated junctions are influenced in several respects by the insulating layer and its surface, which affect the space-charge region at the surface and result in a reduced breakdown voltage for p^+-n junctions (9:980). Since this is mainly

dependent on the device fabrication process and contamination control in the laboratory, it is difficult to predict quantitatively the surface effects on the breakdown voltage.

Thus, we have to carefully determine surface effects such as factors influencing surface breakdown due to the formation of an inversion layer or ionic motion. For this purpose, the flat-band condition is experimentally obtained for each sample using a C-V technique (25:49-56).

Junction Curvature Effect on the Breakdown Voltage

A planar junction fabricated by the planar technique is far from being a plane since solid-state diffusion from the oxide window proceeds approximately as far along the surface as into the depth of the semiconductor (6:197), forming the cylindrical and/or spherical region at the junction periphery as shown in Figure 1.

From Poisson's equation, the electric field at the junction periphery can be calculated, and the detailed diffusion profile has been worked out by Townsend and Strachan (23). Thus, the avalanche breakdown voltage has to be determined by this higher field intensity region at the corner because breakdown will commence at any region, no matter how small, where the maximum field reaches the critical field of the semiconductor material.

Considering our design and diffusion cycles, it is

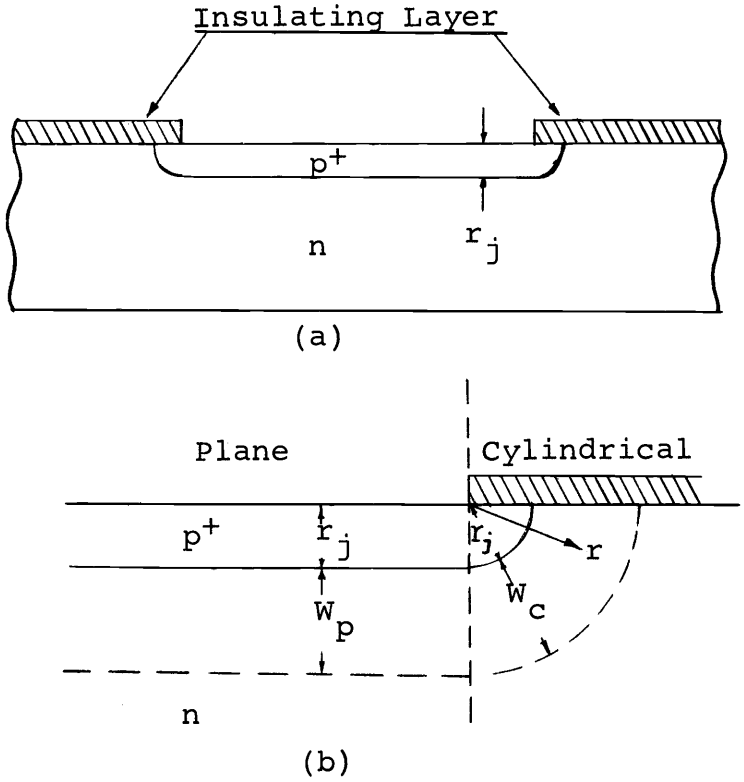


Figure 1. (a) Cross-section of planar diffused junction.
(b) Relationship between diffusion depth and radius of curvature at the periphery.

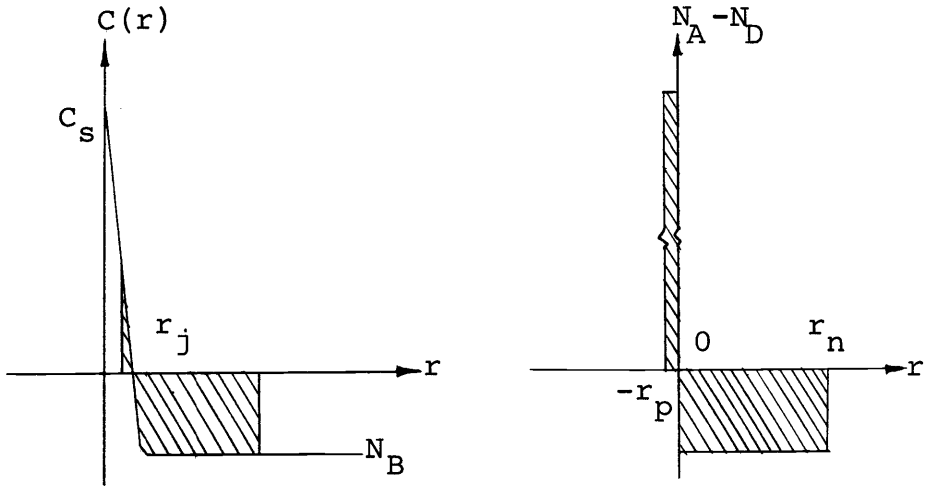


Figure 2. Impurity distribution and approximate charge density at the corner for p^+-n abrupt junction.
The space-charge layer penetrates essentially only into the substrate.

reasonable for the diffused junctions to be considered as cylindrical abrupt junctions.

However, the planar breakdown voltage will be calculated by the following equation (21:844).

$$BV = 60(Eg/1.1)^{3/2}(N_B/10^{16})^{-3/4} \times \left\{\left[(n+1+R)R^n\right]^{1/(n+1)} - R\right\} \text{ volts} \qquad \text{(Eq. 2)}$$

where n = 1 and $R = r_j/W$.

W is the corresponding depletion layer width (in micrometers) to the maximum field for different values of junction radius (r_j) and is given by

$$W = (10^{16}/N_B)(\epsilon/\epsilon_{si})(Em/1.6x10^5) \qquad \text{(Eq. 3)}$$

Because of the strong dependence of the ionization rates on the electrical field, the maximum field Em, for a given semiconductor, does not vary appreciably with the substrate impurity concentration and the radius of curvature.

It should be emphasized, however, that small variations in Em do not necessarily imply small variations in breakdown voltage since the space-charge layer width varies rapidly as a function of r_j for the abrupt junction. Therefore, breakdown voltage depends strongly on the radius of curvature because the field profile is unsymmetrical with respect to the metallurgical junction (21:841).

For the impurity concentration 10^{15} and $5.4x10^{15}$

atoms/cm^3 of n-type silicon with a junction depth of 0.5 μm, the planar breakdown voltages are calculated in Appendix I by Equations 2 and 3.

The planar breakdown voltages, which were calculated by Sze and Gibbon's formulae, were compared with Hilibrand's (Appendix II, Fig. a) and resulted in close agreement.

The planar breakdown voltages (BV_{planar}) of 34 and 52.5 volts were used in this project for 1 ohm-cm and 5 ohm-cm silicon materials respectively.

The theoretically calculated breakdown voltages of plane and planar junctions with a junction depth of 0.5 μm are summarized in Table II (Appendix III) for two different background doping levels.

Oxide Charge Effect on the Breakdown Voltage

In p-n junctions fabricated by the planar technique, the breakdown voltages and reverse current characteristics are affected by the oxide charges in the insulating layer and its interface states.

It has been shown that charges which are present at the surface of a p-n junction can alter the electric field in the depletion region because of field lines terminating at these surface charges instead of at ionized impurities in the silicon itself.

The breakdown of planar junctions often shows an avalanche drift instability in the form of "walk-out."

Walk-out is the process where the breakdown voltage drifts to higher values during avalanche. After avalanche has ceased, breakdown voltage will remain at its high value initially, but after a long period of time will recover to its initial value (9:980).

Soft characteristics are also frequently associated with oxide surface effects as well as metallic precipitates (5, 17, 18). Although these so-called instability phenomena depend on the quantity and degree of mobility, they are always observed as a bulk effect during our experiments.

Since the oxide-passivated surface is a non-ideal insulator, charges within the oxide, including those at the metal-oxide interface, can no longer be neglected in comparison with charges in the silicon space-charge region. Therefore, one has to consider the defect structure of the insulator and admit the possibility of a non-zero charge density within the insulator.

It is generally known that thermal oxidation results in predominantly donor-type surface states.

Thus, the oxide is known to exhibit a positive charge resulting in the accumulation of electrons at the surface. These charges can be due to traps in the insulator that electronically interact with silicon or metal, and they are therefore similar to surface states but with a three-dimensional distribution.

The migrating ions may originate from the oxide itself or from contamination that occurred during various

post-oxidation steps, especially the deposition of the metal electrode (15:49).

Other types of charges located at the interface can also exist in the oxide. These are the fixed charges which may be associated with ionic defects in the oxide or with interface states but do not participate in electron transfer processes across the interfaces.

All that is necessary here is to recognize the existence of all available charge sites in the insulator, as it will affect the depletion width at the surface, and hence, breakdown voltage.

The effect will be different for p^+-n and n^+-p junctions depending on the density and distribution of mobile ions and the background doping level.

The effects of oxide charges on p^+-n and n^+-p junctions are shown in Figure 3 without the metal electrode on top of the insulating film.

For p^+-n junctions, the positive charge acts to increase the field at the corner region of the junction and tends to accumulate the n surface resulting in a reduced depletion width at the surface, the overall effect being a reduced breakdown voltage.

For n^+-p junctions, the corner field is reduced and p surface tends to be depleted, resulting in an increased depletion width, and hence, an increased breakdown voltage.

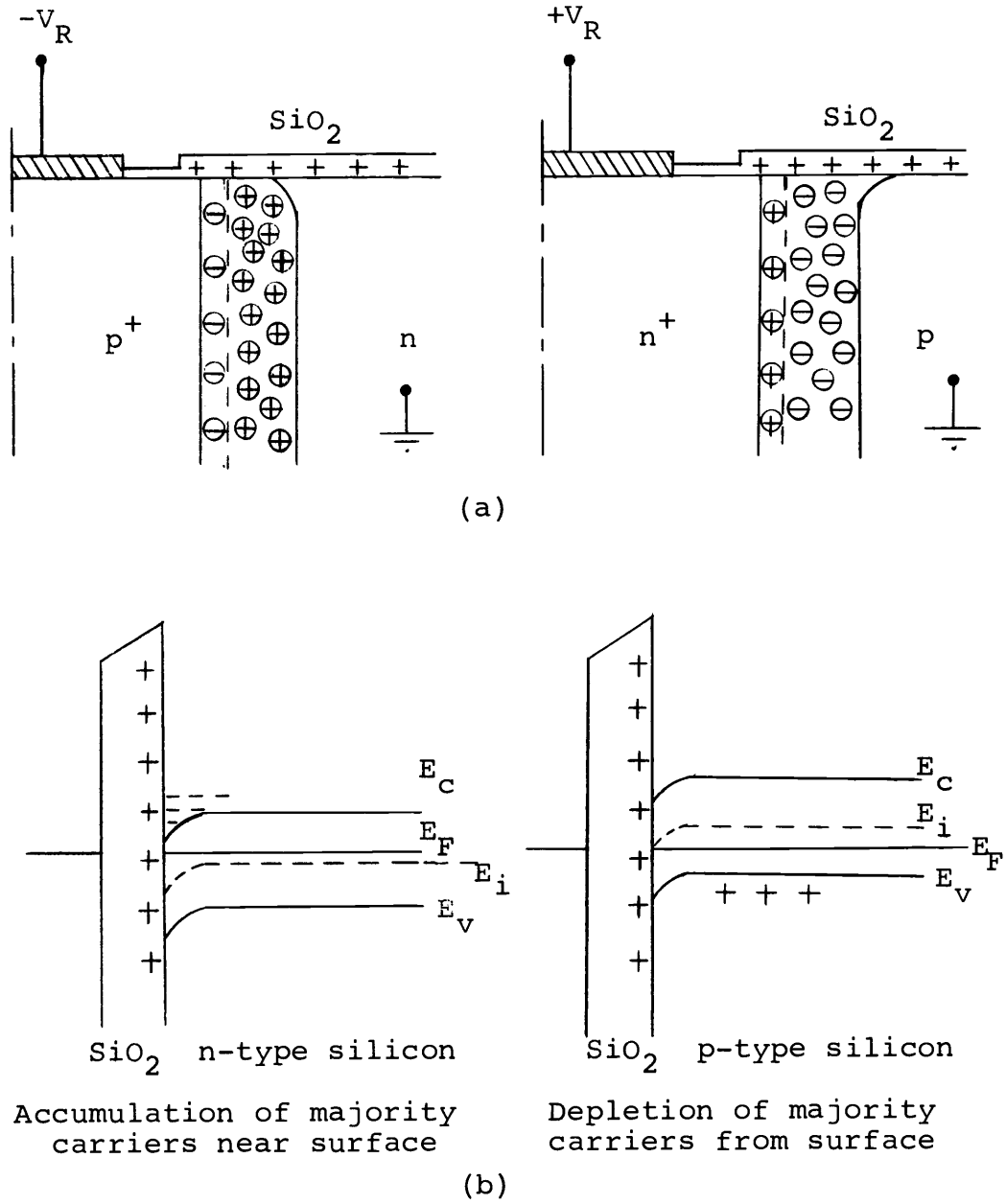


Figure 3. (a) Influence of a positive oxide charge on surface depletion width for p^+-n and n^+-p junctions.

(b) The corresponding energy-band diagrams.

IV. SURFACE FIELD EFFECT ON THE JUNCTION BREAKDOWN

The effect of a surface field on the breakdown voltage of a p-n junction has long been recognized by various investigators.

As discussed previously, the surface field effect is qualitatively the same as the effect of the oxide charge, indicating that the external surface potential has more control over the breakdown voltage than the oxide charge.

If a metal field plate is placed around the junction, its potential will influence the field distribution within the depletion region near the surface, bringing about a modulation in the junction breakdown voltage.

Grove et al. (8) solved numerically the potential distribution within that region of the p-n junction which is under the control gate and near the oxide-silicon interface from the two-dimensional Poisson equation and the Laplace equation.

In Figure 4, the outer gate voltage (V_{GO}) prevents charge migration on the oxide surface due to the potential applied to the inner gate.

From the theoretical model proposed by Grove et al. (8), the general observation can be described over a considerable range where the surface is depleted by the formula

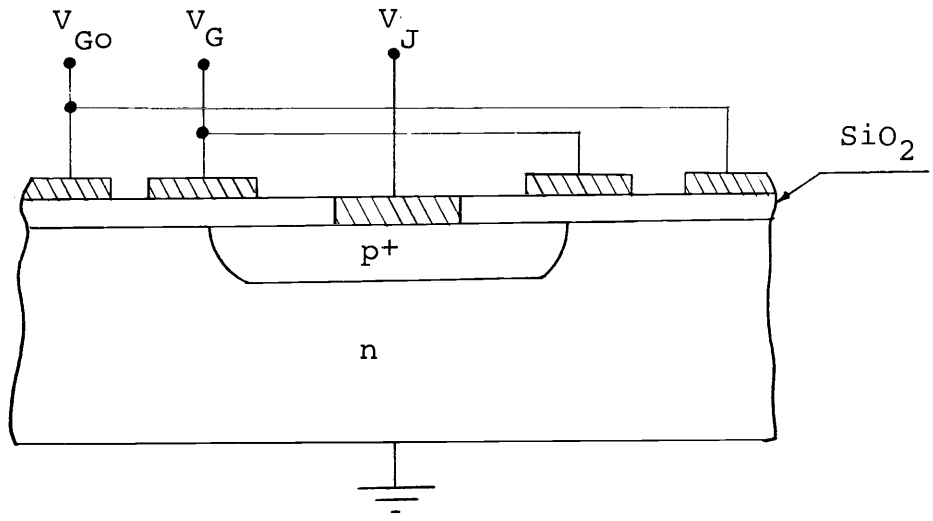


Figure 4. Cross-sectional representation of a gate-controlled planar p-n junction diode.

$$BV = m\ V_G + \text{constant}$$

$$= \frac{1}{1+3\ t_{ox}/W}\ V_G + \frac{3\ E_{crit}\ t_{ox}}{1+3\ t_{ox}/W} \qquad \text{(Eq. 4)}$$

where t_{ox} is the oxide thickness and E_{crit} is the critical field in the corner region.

Since the slope m is a function of the oxide thickness and the depletion width at the critical field, it approaches unity for low substrate impurity concentrations and for small oxide thicknesses.

More recently, H. C. de Graaf (3) investigated the relation between breakdown voltage and gate voltage experimentally as well as theoretically with a different physical model of MOS-transistor as shown in Figure 5.

In Figure 5, one side of the junction (A) is not

overlapped by the gate, making the bulk breakdown in this region independent of the gate voltage.

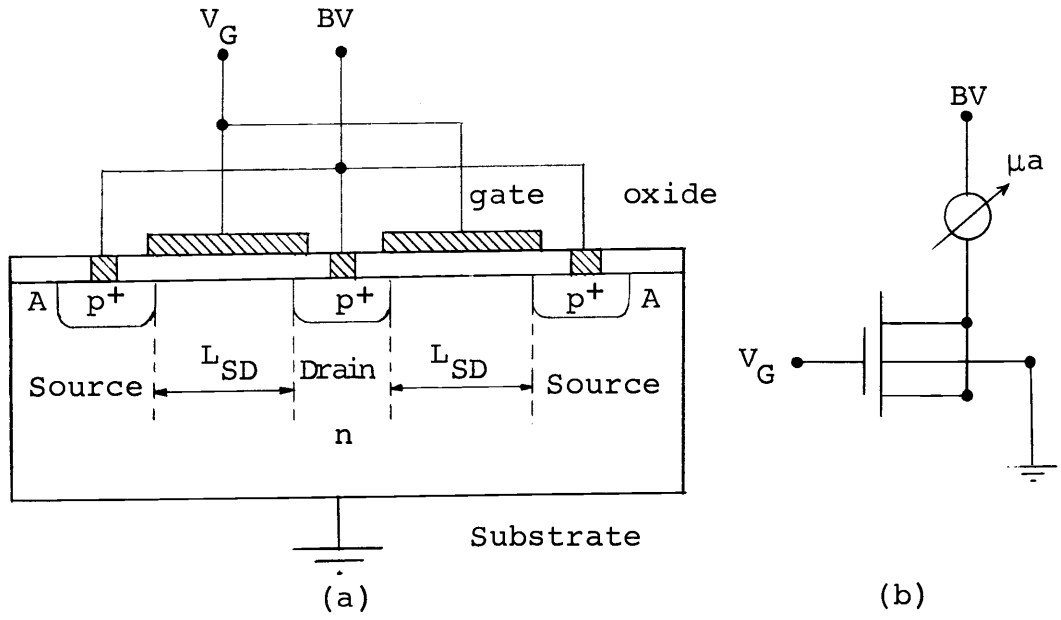


Figure 5. Cross-section of the circular geometry of the MOS transistor (a) and the circuit diagram (b).

For the model proposed by de Graaf, the breakdown voltage is given by

$$BV = V_G + \text{constant}$$

$$= V_G + E_{crit} \left(\frac{\epsilon_{si}}{\epsilon_{ox}} t_{ox} K\right)^{\frac{1}{2}} \qquad \text{(Eq. 5)}$$

where $\epsilon_{si}/\epsilon_{ox} = 3$ and K is the distance from the interface at which the electric field in the y-direction begins to deviate from zero. This distance (1.5-to-2.0 μm) is approximately independent of the x-direction, the substrate doping, the oxide thickness and the applied voltages.

In contrast to the result reported by Grove et al.,

de Graaf showed that within wide limits, the substrate doping and oxide thickness had no influence on the slope of the $BV\text{-}V_G$ curve. It is considered that the different results arise from the different theoretical models, as shown in Figures 4 and 5. In Figure 4, the gate overlapped the junction everywhere and thus the gate also modulates the junction curvature in the bulk (3:31).

These two cases will be compared with our results.

The role of the metal electrode on top of the insulating film is to establish a field normal to the silicon surface. However, there is an electronic interaction between the metal, insulator and semiconductor. Thus, even at zero applied voltage there is a charge separation between metal and silicon because of a difference of the electrochemical potential of electrons in these three regions.

Therefore, there will be an electrostatic potential variation from one region to another, as illustrated in Figure 6, for the case of an aluminum/silicon dioxide/n-type silicon.

The work function difference, which is the energy required to remove an electron from the Fermi level in a given material to vacuum, is defined as

$$\phi_M + V_{oo} = \chi - \phi_{so} + \frac{Eg}{2} + \phi_F$$

Thus, $$\phi_{MS} = \phi_M - (\chi + Eg/2 + \phi_F) = -(V_{oo} + \phi_{so}) \qquad \text{(Eq. 6)}$$

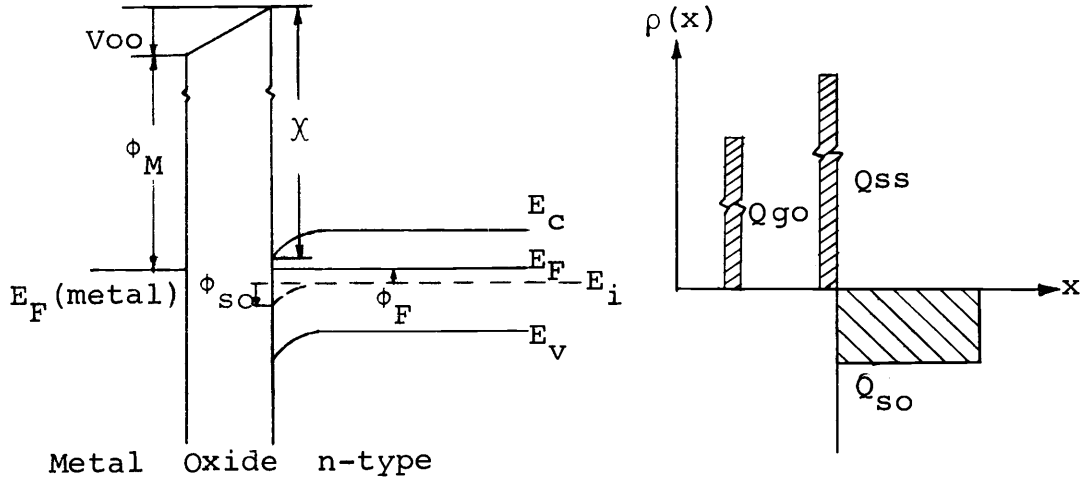


Figure 6. The effect of surface state charge and work function difference on the energy bands and the charge distribution in an MOS structure for zero gate voltage.

where ϕ_{so} : surface potential at $V_G = 0$

Voo : voltage drop across the oxide at $V_G = 0$

ϕ_F : Fermi potential

ϕ_M : the work function of metal

χ : electron affinity of the semiconductor

In this system, the work function differences for the impurity concentrations of 10^{15} and 5.4×10^{15} atoms/cm^3 are -0.3 and -0.26 volts respectively.

Here, however, even if the field plate is near substrate potential, the high field near the heavily doped region will reduce the breakdown voltage. This phenomenon is no longer negligible in the diffused shallow junction.

V. C-V TECHNIQUE

From both theoretical and practical viewpoints it is very important to investigate the stability of the charge distribution, as established by the oxidation and post-oxidation treatments, as well as the deposition of the metal electrode. Practically, the characteristics of the device are influenced by the ionic and electronic transport processes from one region to another under extreme working conditions; that is, elevated temperature and high electric field across the oxide.

The C-V technique, in which the capacitance of an MIS sample is measured as a function of the applied voltage, is a useful technique for measuring the degree of semiconductor surface passivation. This technique has been developed to a high degree of utility (25).

By an easy measurement of MIS capacitance using the C-V method, the various important semiconductor properties, which are impurity concentration, the density of ionized surface state and minority carrier life time can be determined.

For the purpose of our investigations, the surface state density and the impurity concentration of the sample were measured experimentally by the standard bias-temperature (BT) test. In a series of experiments, the effects of charge drift, which affect the breakdown voltage

characteristics, were measured.

In order to bring about a flat-band condition (no charge induced in the semiconductor), a negative voltage is applied to the metal electrode to counterbalance the work function difference and charges in the oxide layer.

When a gate voltage (V_G) is applied, an additional voltage drop (Vo) across the oxide and the surface potential (ϕ_s) appears, which alters the energy band diagram shown in Figure 6. Thus, the gate bias is given by

$$V_G = Vo - Voo + \phi_s - \phi_{so}$$

the work function difference from Equation 6,

$$V_G = Vo + \phi_s + \phi_{MS} \qquad \text{(Eq. 7)}$$

From Gauss's theorem, the charge neutrality of an MIS system may be expressed as

$$Qg + Qss + Qsc = 0 \qquad \text{(Eq. 8)}$$

where Qss, Qsc, and Qg indicate charge in surface states, semiconductor space-charge region, and metal electrode respectively. From Equations 7 and 8,

$$V_G - \phi_{MS} + \frac{Qss}{Cox} = \phi_s - \frac{Qsc}{Cox} \qquad \text{(Eq. 9)}$$

where $Cox = K_o\epsilon_o/t_{ox}$ is the oxide capacitance per unit area.

Thus, the flat-band voltage is given by

$$V_{FB} = \phi_{MS} - \frac{Qss}{Cox} \qquad \text{(Eq. 10)}$$

The above flat-band voltage is considered by assuming

that all available charges in the insulator exist at the silicon-silicon dioxide interface.

In practice, however, space charges, which can be due to several causes such as ionic contamination or traps ionized by irradiation, are distributed arbitrarily within the insulator as shown in Figure 7.

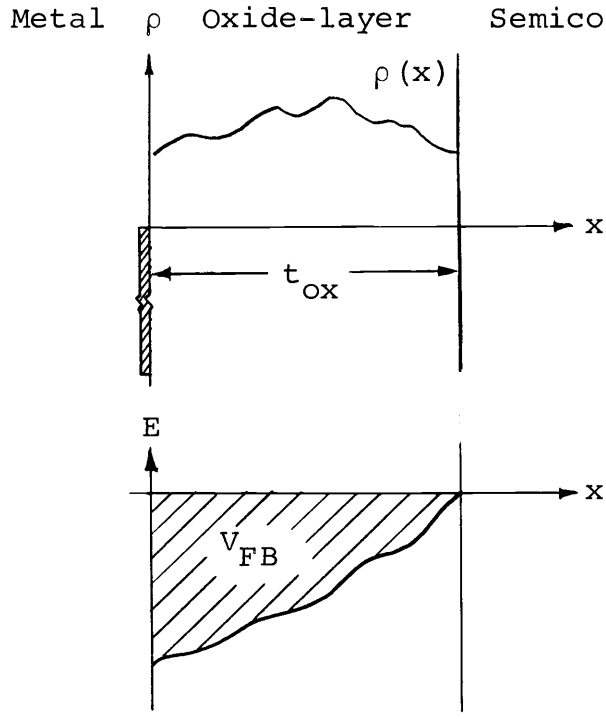


Figure 7. The effect of an arbitrary space-charge distribution within the oxide-layer.

Since the flat-band voltage not only depends on the density of charges but also on its location within the insulator, the effect of an arbitrary space-charge distribution has to be taken into account for the actual flat-band condition. Thus the actual flat-band voltage (V_{FB})

is given by

$$V_{FB} = \Phi_{MS} - \frac{Qss}{Cox} - \frac{1}{Cox}\int_{o}^{t_{ox}} \frac{x}{t_{ox}} \rho(x)dx \qquad \text{(Eq. 11)}$$

As a result, the flat-band voltage will correspond to the total translation along the voltage axis from $V_G = 0$ on the ideal C-V curve.

Under the bias-temperature stress, the various instability phenomena are observed in a MOS structure resulting in a shift and distortion of the C-V curve because of ion and electronic transport processes within the oxide layer.

Our results show that, even though ion drift instability was observed, no slow-trapping and surface-state instability were found.

After negative bias at the elevated temperature (150°C), the voltage difference (ΔV) between the ideal C-V curve and the measured curve at room temperature can be used to calculate the density of ionized surface states (Nss).

From Gauss's law, the density of surface states is

$$Nss(Vs) = \frac{Qss(Vs)}{q} = \frac{(Cox)\Delta V(Vs)}{q} \qquad \text{(Eq. 12)}$$

where Vs is the surface potential.

VI. DESIGN CONSIDERATION AND MASK LAYOUT

Since present-day microwave transistors are usually built on 0.25-to-5 Ω-cm material and almost all are silicon n-p-n structures, n-type silicon substrates with low resistivity and low dislocation density were selected.

For application to small-signal microwave devices, 1 ohm-cm <111> -oriented substrates were used and 5 ohm-cm <100> -oriented substrates were used to simulate power microwave devices.

The main purpose of this project was to find a way to increase the collector junction breakdown voltage of microwave transistors using surface fields at the junction periphery.

The experimental devices in this project were confined to diodes with junction depths of 0.4 to 0.6 μm. Experimental devices were constructed on a chip 0.114 x 0.114 sq. cm. in size. There were both circular and rectangular diodes surrounded with metal gate electrodes at the junction periphery.

In order to avoid overlapping of the gate and base contacts, there were also three rectangular diodes with spacings of 12.7 μm, 6.35 μm, and 3.175 μm between the gate metal and the base contact.

Also included on a chip was a double-diffused transistor with an emitter width of 25.4 μm.

The active area of the base region was designed as

small as allowable for the facilities used in the device fabrication, which was 0.128×10^{-3} sq. cm.

Both circular and rectangular structures with approximately the same area, which are applicable to present-day microwave transistors, were designed in order to find the effects of junction curvatures on avalanche breakdown voltage.

In addition to active devices, a diffused resistor of ten squares in the base region and another diffused resistor of 15 squares in the emitter region were included for the evaluation of each diffused layer.

A MOS capacitor as well as a gate-to-substrate capacitor of known geometry were provided to estimate oxide thickness, flat-band voltage and the impurity concentration of the sample. A 400:1 reduction was used in making the masks for high resolution. The 40:1 first reduction was followed by a 10:1 reduction with the step-and-repeat camera to give the final mask. The four masks used in this experiment were:

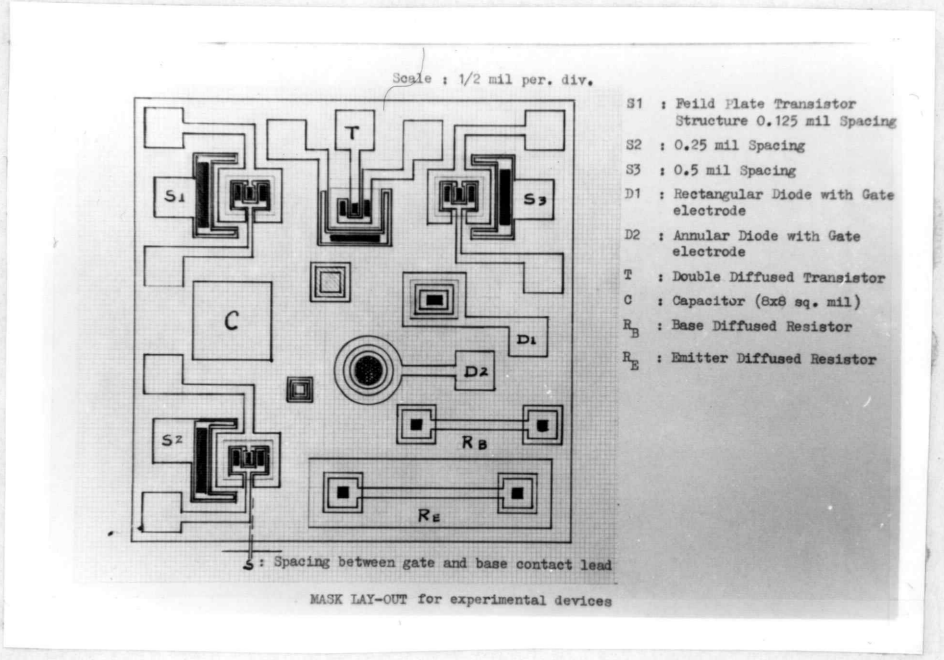
(1) The mask for base diffusion

(2) The mask for contact and emitter diffusion

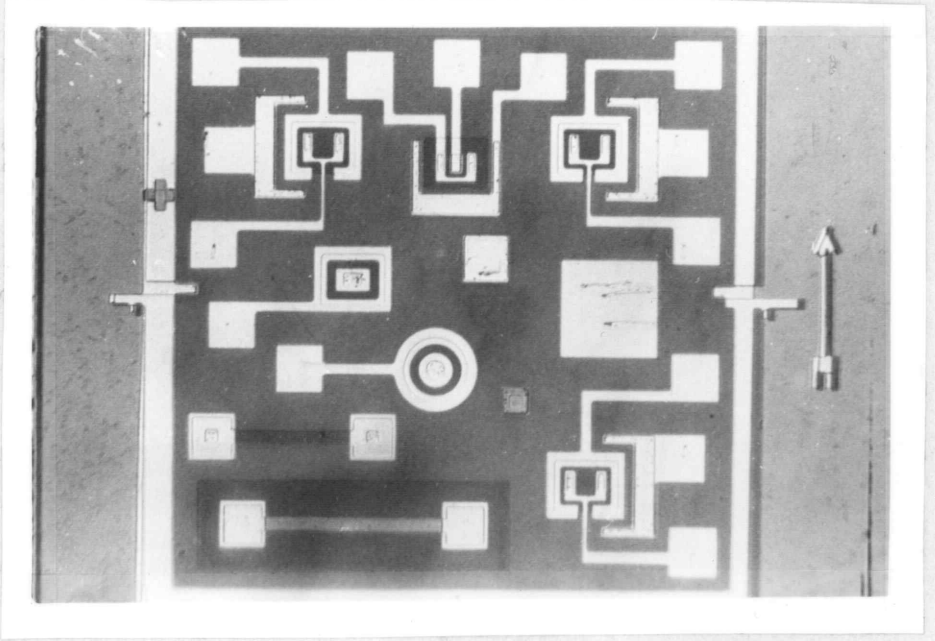
(3) The ohmic contact mask

(4) The mask for metal etching

The mask-layout of the experimental devices and a picture of an actual device fabricated with the planar technique are shown in Figure 8.



(a) Mask layout of experimental devices.



(b) Microphotograph of an actual chip.
(Mirror image of (a))

Figure 8. The mask-layout of experimental devices and the microphotograph of a sample chip.

VII. FABRICATION PROCESS

Fabrication procedures used in this experiment were the same as bipolar I.Cs.

The boron diffusion for the shallow base region was an important process for the creation of a stable device and hard reverse V-I characteristics.

In order to reduce the susceptibility to contamination, extreme care was taken in the initial oxidation and the deposition of the metal electrode as well as the handling of boron dopants in the device fabrication.

The following steps are the important processes used in this experiment.

(a) Initial Cleaning

The chemically polished slices were degreased and cleaned using successive rinses in TCE, acetone and deionized water, and then followed by successive rinses of hot H_2SO_4 for five minutes, running DI water and buffered HF for 20 seconds. Then it was followed by cleaning with DI water in the ultrasonic tank and drying with nitrogen.

(b) Initial Oxidation

Silicon-dioxide films were grown in the oxidation furnace at 1100°C immediately after the initial cleaning step. The oxides used in this project included dry oxide

and wet (steam grown) oxide on both <111> - and <100> -oriented silicon. Wet oxidation was employed with oxygen bubbling through a water bath which was kept at 96°C.

For thin oxide layers, dry oxygen was employed, and a combination of wet and dry oxidation processes was used for the thick oxide samples. The oxide thicknesses varied from 0.15 μm to 0.54 μm.

The samples were annealed for 20 minutes in a dry nitrogen ambient in the same furnace. This step will reduce significantly the surface state density and result in uniform impurity concentration at the surface of the substrate.

(c) Photoresist of Test Patterns

Positive photoresist (AZ-1350) and SiO_2 etching techniques were used to form the test patterns of circular and rectangular diodes. All test patterns were incorporated in the same fabrication mask to ensure identical processing for a given resistivity and junction depth.

In order to remove the photoresist on the patterns, the masking operation was followed by the cleaning step, which was established as a standard cleaning process prior to all high temperature operations such as the impurity deposition process and also as a cleaning step prior to metal deposition.

This cleaning step consisted of rinsing the surface

of the wafer in acetone, using a cotton swab and running DI water. It was then followed by soaking in hot H_2SO_4 for ten minutes. All treatment in the hot sulfuric acid was followed by etching the thin oxide layer, which might be formed during soaking, for a few seconds.

The final cleaning step was followed by ultrasonic cleaning with acetone.

(d) The Base Boron Diffusion

Since the collector junction characteristics of the shallow junction were important in this experiment, the corresponding base diffusion was carried out with great care in order to have a junction depth of 0.5 μm and good junction characteristic.

Also, it was found that the reverse V-I characteristics of the final devices were greatly dependent on the types of boron dopant rather than on the different oxidation processes; dry and wet oxidation or the oxidation through 20% HCl which was expected to reduce the sodium contamination. The effect of the boron system on the reverse characteristics will be discussed in the experimental results section.

Three types of boron dopants -- liquid boron-emulsion, boron nitride powder, and a boron nitride wafer -- were used in this project. In spite of the uniform doping, a high surface concentration and a thin oxide layer required

as masking, the boron emulsion source was abandoned after a trial period due to the poor junction characteristics and a large avalanche instability drift after the deposition of gate metal electrode.

A boron nitride wafer, 3.18 cm in diameter and 0.16 cm in thickness was degreased and cleaned with organic solvents and then oxidized for three hours at 950°C. The oxidation was required to establish the initial supply of the B_2O_3 film which was the active impurity source for the boron deposition. In order to maintain a constant source of B_2O_3, the boron deposition was carried out in a mixture of nitrogen and oxygen.

An oxide mask thicker than 0.25 μm was required in order to use the boron nitride wafer. However, boron nitride powder could be used with a thin oxide layer.

The deposition using a boron nitride wafer as well as boron nitride powder was carried out in a mixture of 283 cc/min. nitrogen and 47 cc/min. oxygen at 950°C for 20 minutes. The resulting surface concentrations were almost the same for both boron systems as $C_s \cong 5 \times 10^{19}$ atoms/cm^3.

The residual boron dopant at the surface was removed after the deposition process by boiling the silicon wafer in DI water for ten minutes and etching in buffered HF for five seconds.

In order to redistribute the impurity atoms according to the complementary-error function, a diffusion was made

at 1100°C in the boron diffusion furnace.

After a trial period, the base diffusion time was determined experimentally to be between seven to eight and one-half minutes. The resulting junction depth was evaluated by the angle lapping, staining and interferometry methods.

(e) Emitter and Ohmic Contact Diffusion

In this step, the usual two-step-diffusion was not used. However, for the shallow diffusion, $\sqrt{Dt}$ for the drive-in diffusion is not much larger than $\sqrt{Dt}$ for the predeposition. Thus we can not regard the extent of penetration of the predeposited profile to be negligibly small in comparison to that of the final profile resulting after the drive-in-diffusion step. Furthermore, this step was a low-temperature process so as to minimize the possibility of driving the base further into the substrate.

The predeposition step was carried out at 950°C for 20 minutes using a 2:1 solution (phosphorofilm : DI water) for the emitter and ohmic contact diffusions.

(f) Deposition of Metal Contact

Although aluminum in general is not suitable because of the difficulty in obtaining a clean shallow junction contact (2:1175), the vacuum deposition of aluminum has been used in this project. Aluminum deposition was

followed by an annealing at 400°C for ten minutes and by the metal etching to provide contact patterns.

The alloying at 530°C was not made in order to minimize the possibility of introducing aluminum in the diffused area and resulting in an electrically shorted junction. Finally, the test patterns for the measurements were prepared by the Al-etching technique, and the effective gate areas of 2.32×10^{-8} and 2.54×10^{-8} sq. cm. were made for the circular and rectangular diodes respectively.

VIII. EXPERIMENTAL MEASUREMENTS

The breakdown voltage of the planar junctions, BV_{planar}, was measured on a Tektronix Type-576 transistor curve tracer. BV_{planar} was measured as the voltage at which the reverse current reached 20 μa for the circular and rectangular diodes.

To provide the gate field effect on the junction breakdown voltage, a Trygon Dual Lab-Supply DL 40-1 was used in series with battery to obtain ±150 volts range.

In order to determine the surface state density, and hence the correction term $-\phi_{MS}+Qss/Cox$, a gate-to-substrate C-V measurement was made with a Tektronix Type-564 storage oscilloscope and a Type 3C66 plug-in. In this series of experimental measurements, the effects of mobile oxide charge on the reverse V-I characteristics were plotted on a Fairchild Model 6200-B curve tracer.

Experimental Determination of the Flat-Band Voltage

In order to obtain the direct relationship between the gate potential and curvature-limited breakdown voltage, it is necessary to determine the flat-band voltage, which results in a parallel shift of the breakdown voltage versus the gate potential curve along the voltage axis.

The magnitude of the correction term, $-\phi_{MS}+ Qss/Cox$ used, was based on the gate-to-substrate C-V measurement.

For this purpose, a standard bias-temperature (B-T) test was carried out.

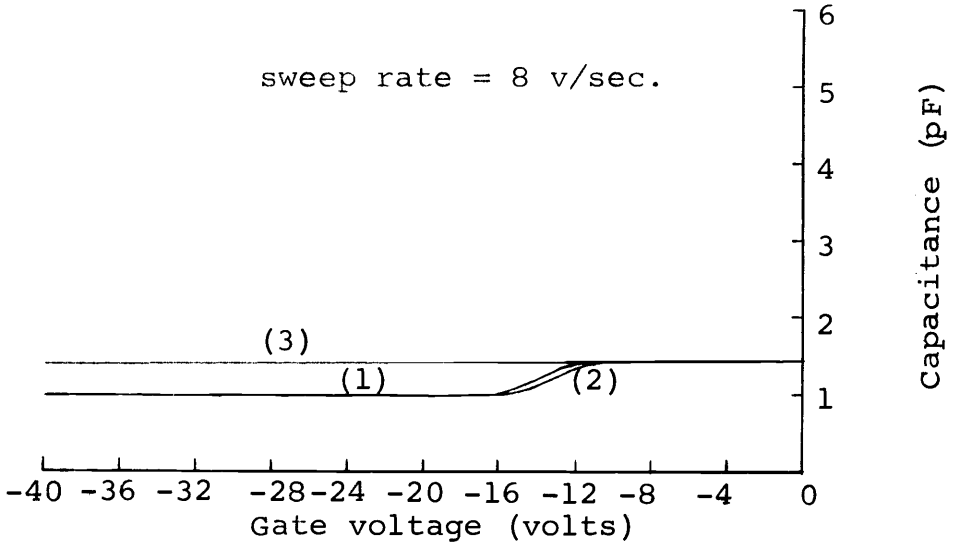
A negative B-T test at the relatively high temperature of 250°C was performed for ten minutes with -12 volts and a positive B-T test followed at 150°C for six minutes with +12 volts. Figures 9 and 10 show the C-V curves measured at room temperature and their corresponding reverse V-I characteristics.

Curves (1), (2) and (3) are the measurements at room temperature, after a negative and positive B-T test respectively. Apparently, the C-V measurement showed only ion drift instability which was due to the simple migration of positive ions within the oxide without trapping and/or generation phenomena at the interface.

The behavior of contamination due to the migration of sodium ions or of protons showed that a positive gate bias had a large effect, whereas a negative bias had a small one. It was, however, readily shown that the ion drift behavior influenced directly the reverse V-I characteristics in this experiment.

Since the effects of mobile positive ions depend on their location in the insulator, the mobile oxide charge will be attracted to the outer surface after a negative bias-temperature test. Thus the term, $\frac{1}{C_{ox}}\int_{o}^{t_{ox}} \frac{x}{t_{ox}} \rho(x)dx$ from Equation 11 has no contribution to the flat-band voltage.

A. C-V measurement



B. Reverse voltage-current characteristics

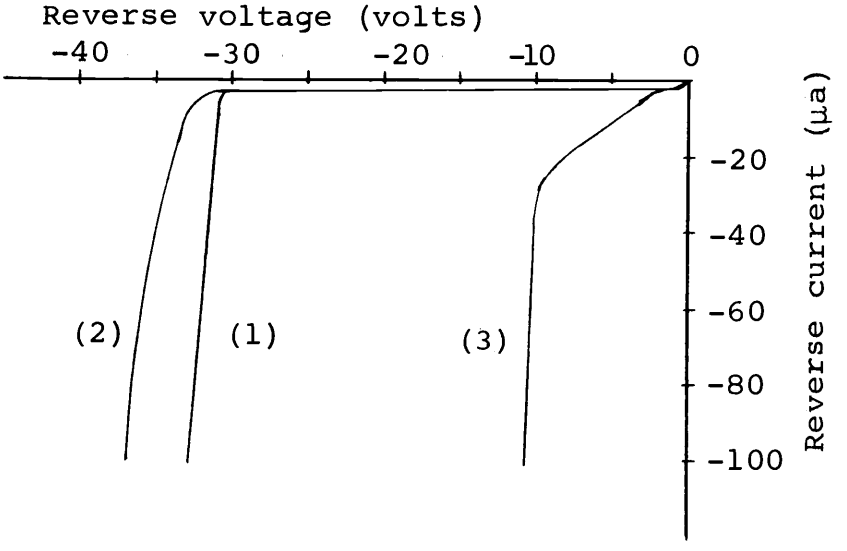
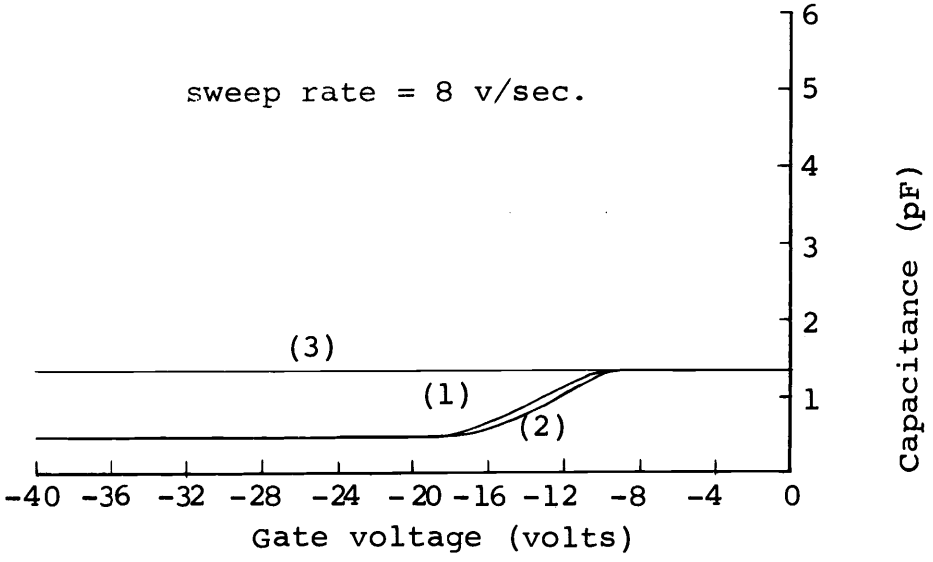


Figure 9. The C-V measurement and corresponding V-I characteristics of the rectangular diode for device No. 1 (1 ohm-cm substrate and t_{ox} = 0.3 μm).

Curve (1) initial measurement,
(2) after negative bias-temperature test,
(3) after positive bias-temperature test.

A. C-V measurement



B. Reverse voltage-current characteristics

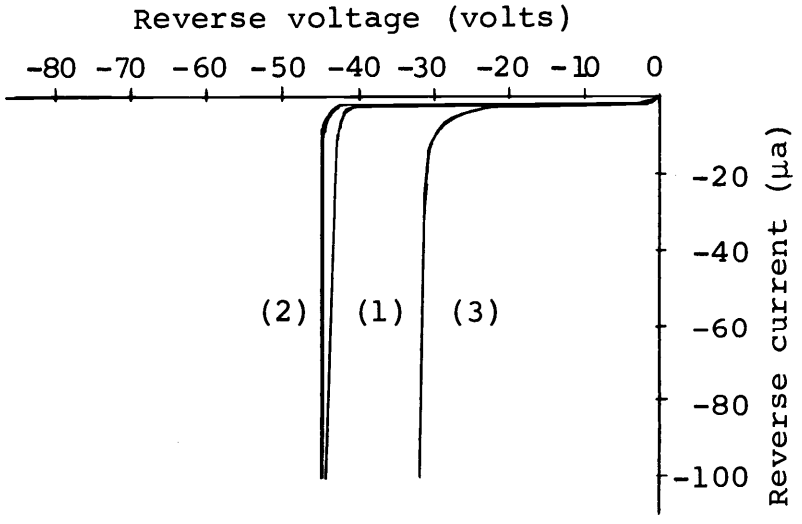


Figure 10. The C-V measurement and corresponding V-I characteristics of the rectangular diode for device No. 3 (5 ohm-cm substrate and t_{ox} = 0.3 μm).
Curve (1) initial measurement,
(2) after negative bias-temperature test,
(3) after positive bias-temperature test.

Figure 11 shows the normalized C-V curves for the rectangular diodes of 1 ohm-cm and 5 ohm-cm substrates.

Since the voltage at which C/Cox = 0.95 is offset one volt from flat-band voltage if the density of interface states is low (25, Part 2:46), the flat-band voltage is that voltage which is 1.0 volt positive of the 0.95 point for p-type and 1.0 volt negative for n-type structure. Thus, by comparing the normalized C-V curve with the ideal curve, the magnitude of the correction term $-\Phi_{MS}+Qss/Cox$ in the expression of flat-band voltage and the surface state density (Nss) were obtained by Equation 12.

Furthermore, a ratio of the minimum and maximum capacitance is related to the doping level of the sample with oxide thickness as a parameter.

The substrate impurity concentrations obtained by C-V technique were compared with those calculated from the four-point probe measurement on thin layers and resulted in coincidence for two different starting materials ($N_D=10^{15}$ and 5.4×10^{15} atoms/cm^3).

For device No. 1 (Figure 12 A), surface state density is calculated by Equation 12 as:

$$\Phi_{MS} = -0.26 \text{ volt and } Cox = 6.03\times10^{-9} \text{ F/cm}^2$$

and

$$Qss/Cox = V_{FB} + \Phi_{MS} = 8.96 \text{ volt.}$$

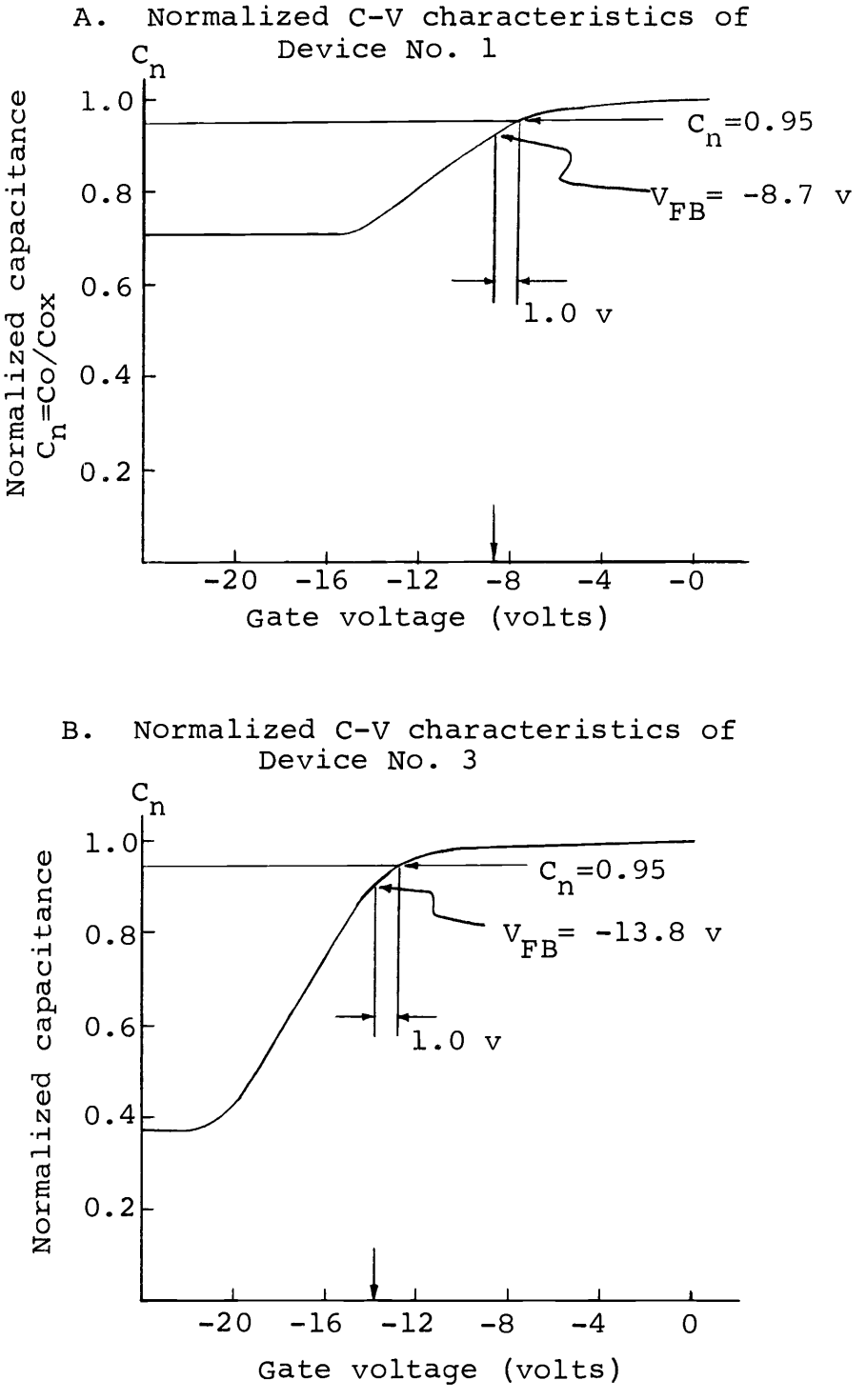


Figure 11. Normalized C-V curves for rectangular diodes of Devices No. 1 and 3 after negative aging (curve 2).

Thus the surface state density Nss is:

$$Nss = \frac{6.03\times10^{-9}\times8.96}{1.6\times10^{-19}} = 3.4\times10^{11} \text{ atoms/cm}^2$$

For device No. 3 (Figure 12 B),

$$\phi_{MS} = -0.3 \text{ volt and } Cox = 5.2\times10^{-9} \text{ F/cm}^2$$

and

$$V_{FB} + \phi_{MS} = 14.1 \text{ volt.}$$

$$Nss = \frac{5.2\times10^{-9}\times14.1}{1.6\times10^{-19}} = 4.5\times10^{11} \text{ atoms/cm}^2$$

In general, the interface states and mobile oxide charge depend on the laboratory contamination level and device fabrication processes.

However, the interface states will be determined approximately as a value fixed by the orientation of silicon crystal, oxidation and annealing conditions, while the mobile oxide charge has a large variation. In fact, the density of ionized states (both interface and oxide charge) were slightly different at each device even in the same wafer.

It was, however, observed that the amount that the breakdown voltage decreased after the deposition of the metal was approximately the same as that increased by applying a negative voltage on the gate by the amount of the flat-band voltage.

The Effects of the Boron System on the Reverse V-I Characteristics

It was shown in Figures 9(B) and 10(B) that the effects of oxide charge drift under bias-temperature stresses were found to influence the breakdown voltage. A positive stress to a p^+-n junction was found to cause a reduction in breakdown, while a negative stress caused an increase in breakdown voltage. Generally, the effects of a positive stress were much greater than those of a negative stress.

These effects, however, were found to be different, depending on the boron systems. Generally, stable junction characteristics were obtained when a device was fabricated by the boron nitride powder or wafer system. It was nevertheless observed that when the boron emulsion was used as a diffusion source, the device had a large reverse leakage current and a drastically reduced breakdown voltage.

Figure 12 shows the reverse V-I characteristics of 1 ohm-cm and 5 ohm-cm substrates for p^+-n diodes fabricated with the boron emulsion source. The curves (a), (b) and (c) are the measurements at room temperature, after negative and positive stresses respectively, which correspond to the curves (1), (2) and (3) in Figures 9 and 10.

Comparing these results with the cases using the boron nitride powder in Figures 9 and 10, the initial measurement

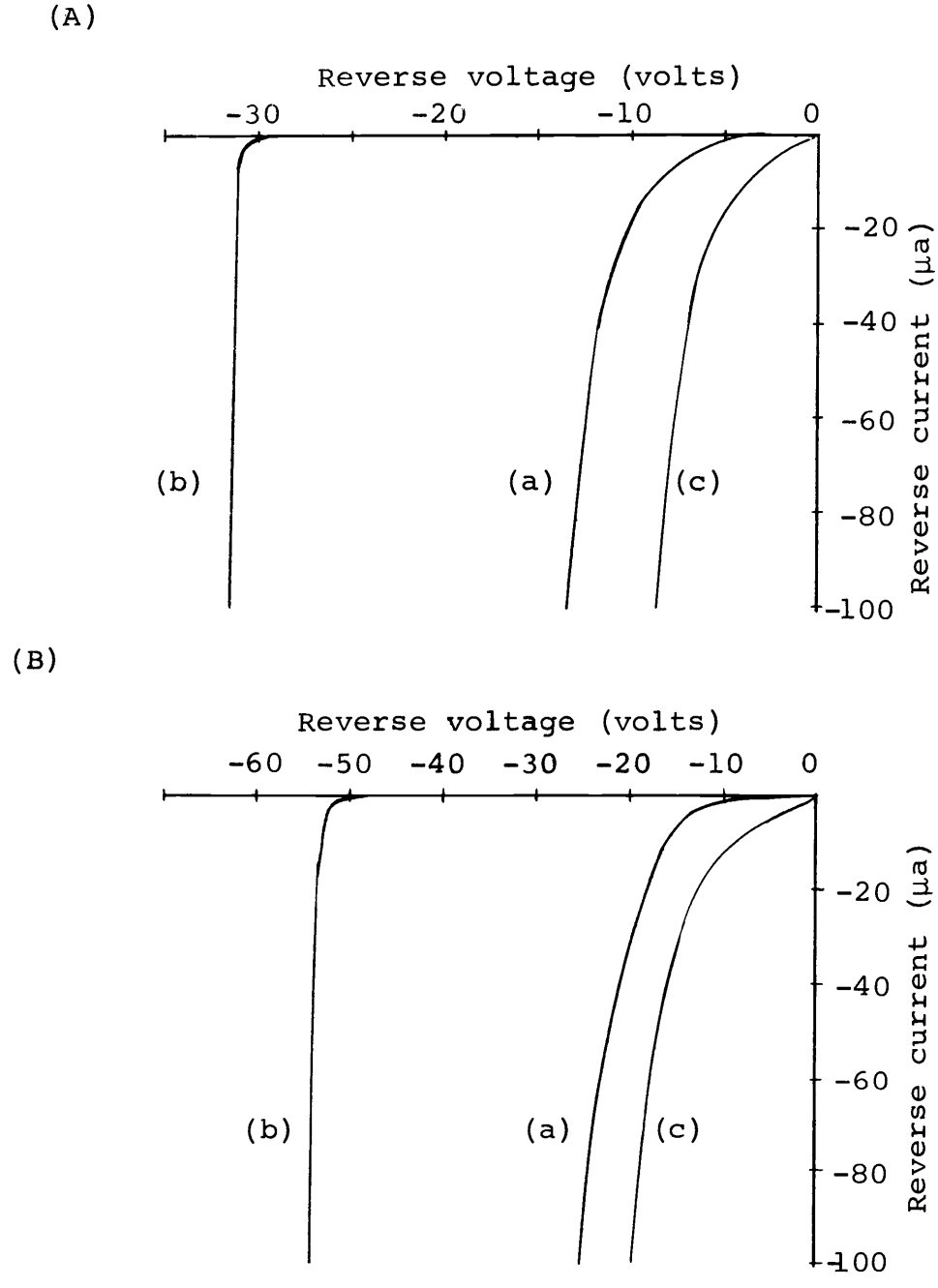


Figure 12. Reverse V-I characteristics of 1 ohm-cm (A) and 5 ohm-cm (B) substrates for p^+-n diodes.
Curve (a) initial measurement,
(b) after negative bias-temperature test,
(c) after positive bias-temperature test.

at room temperature gave the same effect as if positive stress were applied to the devices fabricated by a boron nitride powder.

It was also noticeable that under a negative stress the breakdown voltage increased to the value determined by the junction curvature in the cases using boron emulsion. As a result, in the devices fabricated by the boron emulsion, the effects of the mobile charges will be considered as if they were located at the silicon-silicon dioxide interface initially.

However, the basic mechanism is not known and these results can not be compared closely because of the different surface impurity concentration, which is higher by at least an order of magnitude for the boron emulsion as compared to the boron nitride source. But in order to get a stable device, the boron nitride system was preferred, and hence all experimental data were obtained from the devices fabricated by the boron nitride source.

IX. MEASUREMENTS OF THE BREAKDOWN VOLTAGE VERSUS THE EFFECTIVE GATE VOLTAGE

Figures 13-16 show the experimental measurements of the breakdown voltage as a function of effective gate voltage, $V_G - \Phi_{MS} + Qss/Cox$, for p^+-n diodes. Here the breakdown voltage was measured as a function of the gate potential applied with respect to the substrate.

Figures 13 and 14 show the breakdown voltage versus the effective gate voltage for 1 ohm-cm and n-type silicon with oxide thicknesses of 0.3 and 0.54 μm respectively.

For 5 ohm-cm and n-type silicon, Figures 15 and 16 show the measurements for oxide thicknesses of 0.3 and 0.54 μm respectively.

As discussed before, if the junction radius near the edges of the diffused p^+ region is sufficiently small, the p^+-n junction will break down first due to the junction curvature effect. When a negative gate bias is applied, the surface field tends to smooth out the field concentration near the junction edge. Thus the radius of curvature is effectively increased; hence this in turn increases the breakdown voltage.

Figure 17 shows the measured reverse V-I characteristics as a function of gate voltage for p^+-n rectangular diode with an oxide thickness of 0.3 μm and a 5 ohm-cm substrate.

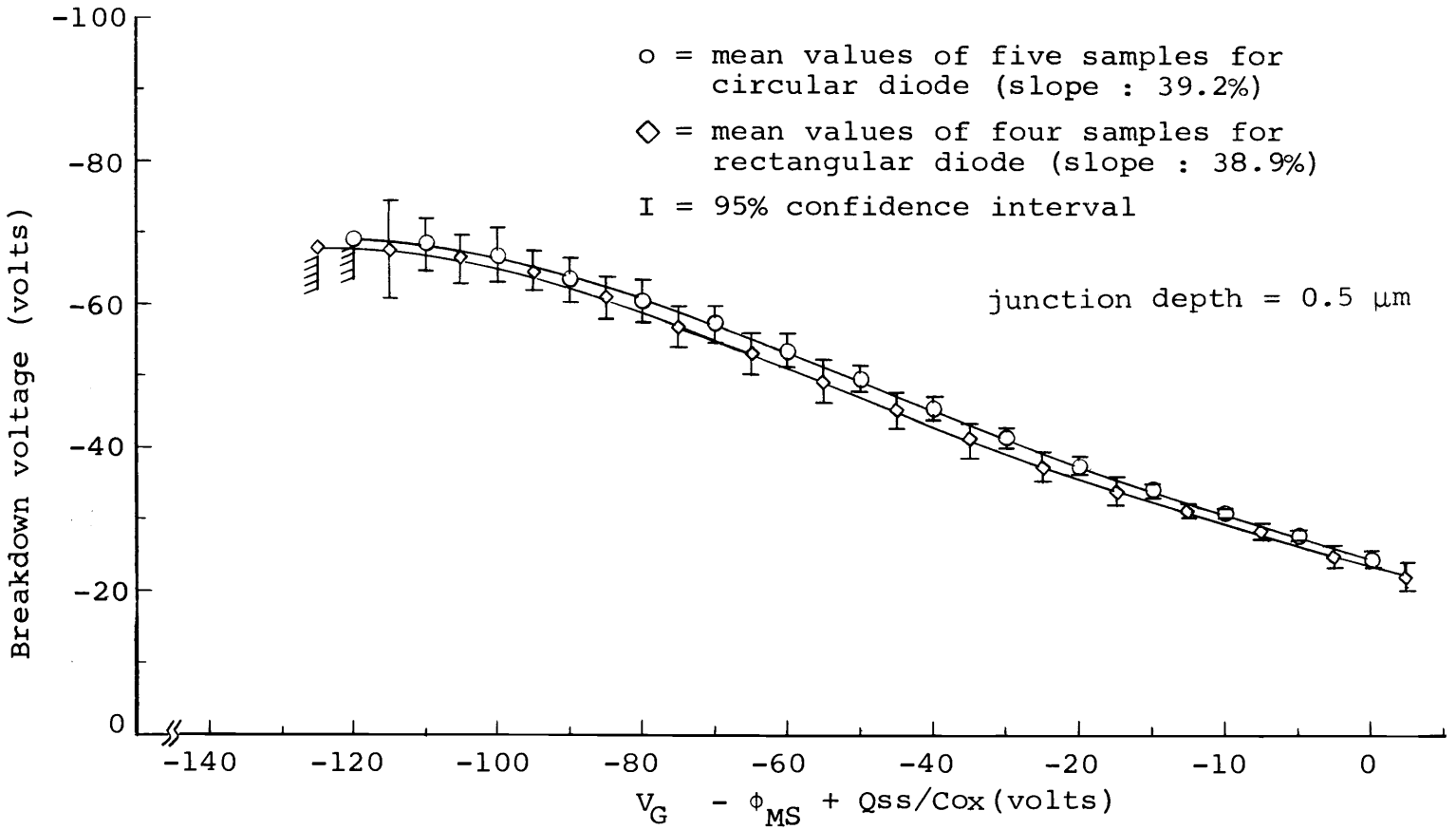


Figure 13. Breakdown voltage versus effective gate voltage for the circular and rectangular diodes of 1 ohm-cm substrate and oxide thickness 0.3 μm.
Cross-hatching shows onset of inversion of substrate surface or a large surface leakage current.

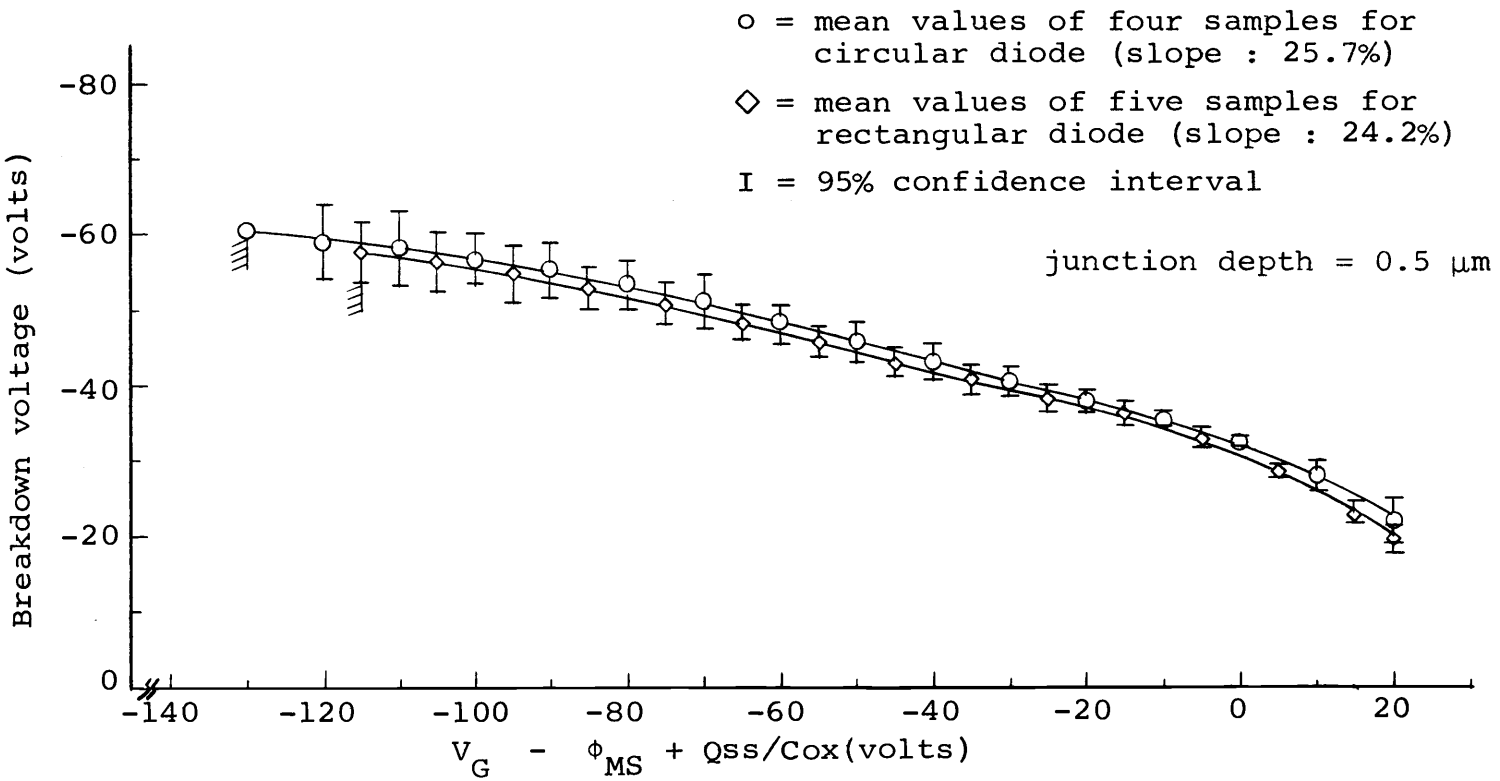


Figure 14. Breakdown voltage versus effective gate voltage for circular and rectangular diodes of 1 ohm-cm substrate and oxide thickness 0.54 μm.
Cross-hatching shows onset of inversion of substrate surface or a large surface leakage current.

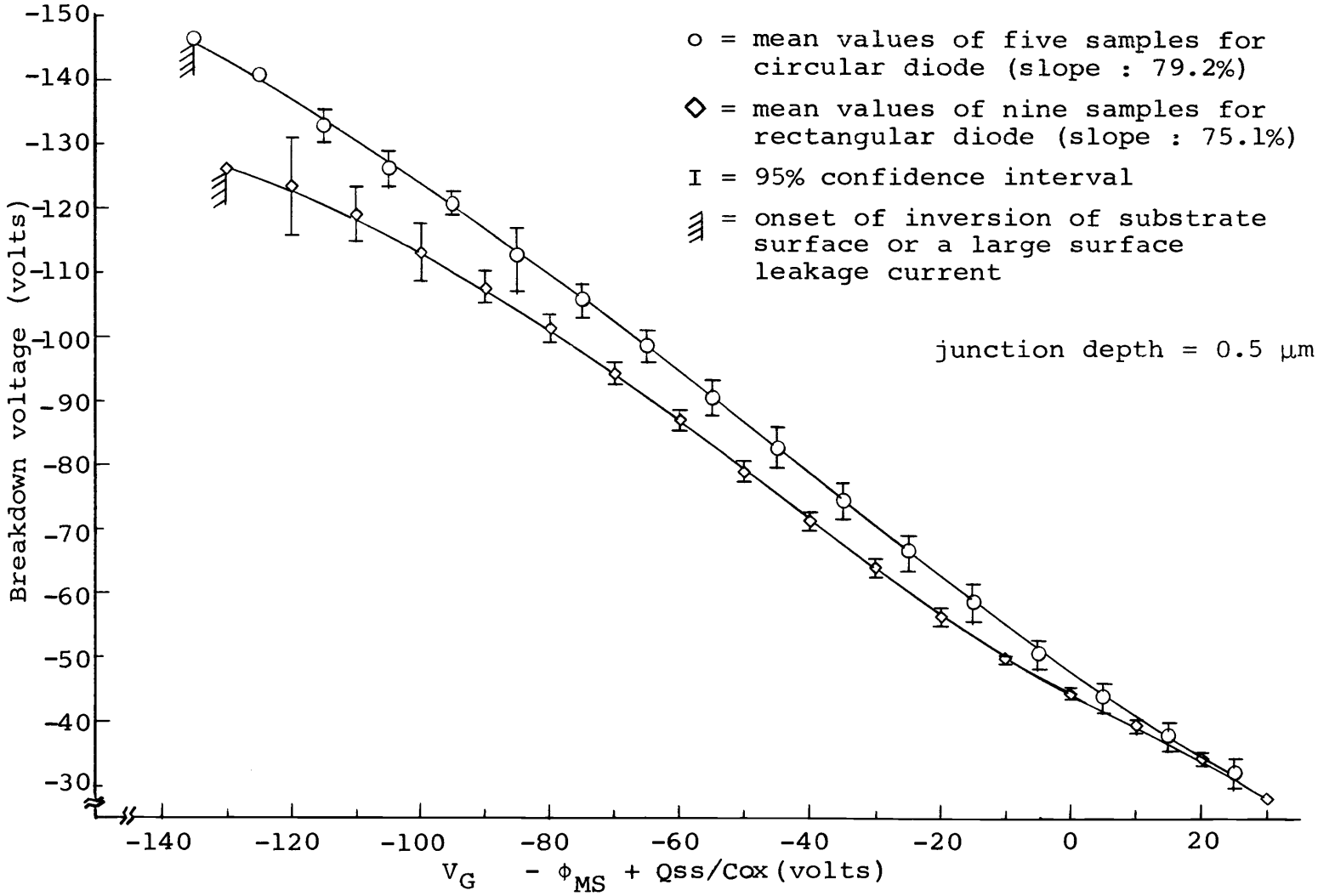


Figure 15. Breakdown voltage versus effective gate voltage for circular and rectangular diodes of 5 ohm-cm substrate and oxide thickness 0.3 μm.

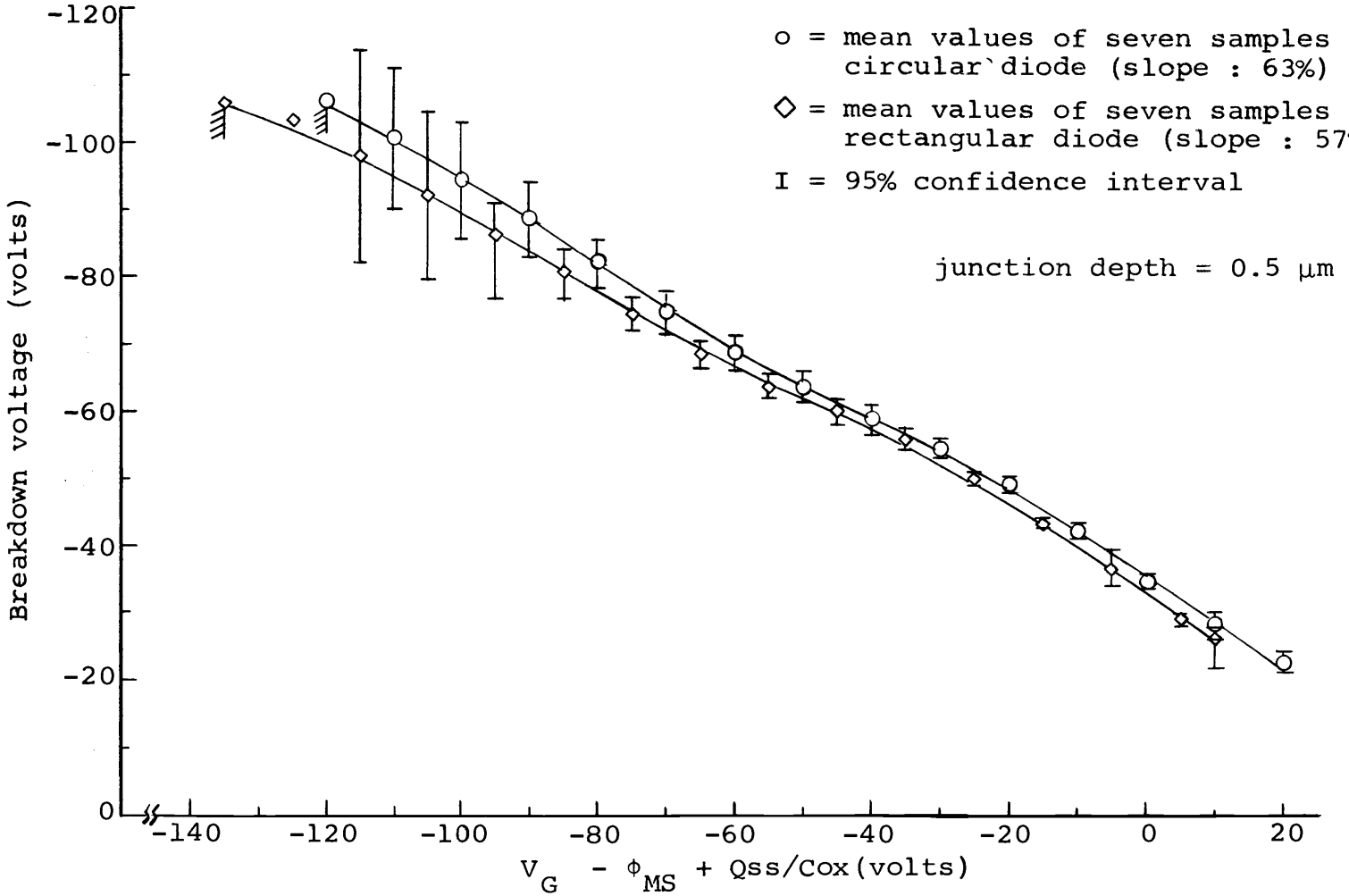
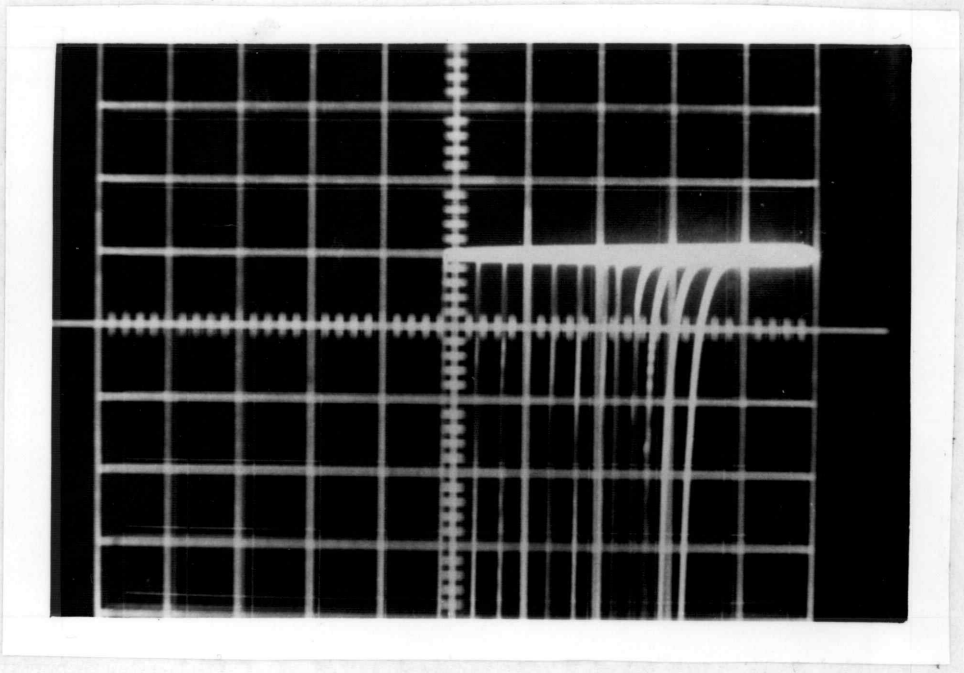


Figure 16. Breakdown voltage versus effective gate voltage for circular and rectangular diodes of 5 ohm-cm substrate and oxide thickness 0.54 μm. Cross-hatching shows onset of inversion of substrate surface or a large surface leakage current.



Horizontal scale : 20 volt/Div.
Vertical scale : 20 μa/Div.
Gate bias : -10 volt/step

t_{ox} = 0.3 μm, N_D = 10^{15} atoms/cm^3
Junction depth 0.5 μm

Figure 17. The reverse V-I characteristics as a function of gate bias for p^+-n rectangular diode.

The increments of breakdown voltage correspond to ten-volt steps of the gate potential, and the breakdown voltage was defined as the voltage at which the reverse current reached 20 μa.

Between the negative gate potential from 0 to 25 volts the incremental behavior of the reverse V-I characteristics is accounted for as the elimination of the oxide charge and work-function difference effects.

Beyond the gate potential of 25 volts, where surface was depleted, it was generally observed that the variation of the gate-to-substrate potential produced the changes in the breakdown voltage in a manner that was described by Equation 4 as a linear relationship between the breakdown voltage and gate potential.

At the extremes, as the gate-to-substrate potential was increased negatively or positively, the breakdown voltage tended toward saturation at a maximum or a minimum value.

The limitation of the breakdown voltage at a maximum value was determined by the onset of inversion of substrate surface. Cross-hatching in the figures shows this maximum value. Each point of Figures 13-16 represents the mean value of the samples, and the 95% confidence limits were calculated from the t-distribution by a computer.

Also, the slope of each figure, over a considerable range where the surface was depleted, was obtained by

linear curve fitting with a computer.

The experimental data of the measured samples are summarized in Table III (Appendix III).

Here the voltage enhancement was defined by the reverse breakdown voltage when the gate terminal is connected to the diffused area. All figures in Appendix III represent the average value of the samples.

Geometry Characteristics on the Junction Breakdown Voltage

Experimental data (from Figures 13 to 16) were obtained for p^+-n circular and rectangular diodes regarding the effect of junction curvature on avalanche breakdown for abrupt junctions. Theoretically, a cylindrical junction should have a higher breakdown voltage than that of a spherical junction.

A circular mask pattern was used in forming a cylindrical junction. However, the junctions formed at the corners of the rectangular mask should be considered as a near-cylindrical junction rather than spherical junctions, because the corners in the diffusion mask are seldom sharp in practice even though a high resolution positive photoresist is used.

In this project, the breakdown voltage of the circular diode was higher than that of the rectangular diode by approximately 3% for 1 ohm-cm and 6% for 5 ohm-cm.

Furthermore, the increase in breakdown voltage tended to be less rapid for the rectangular diodes where the surface was depleted.

Effect of Substrate Impurity Concentration

Figure 18 shows the breakdown voltage versus effective gate voltage for p^+-n diodes of various substrate impurity concentrations with an oxide thickness of 0.3 μm and a junction depth of 0.5 μm.

It is evident that the lower the substrate impurity concentration, the steeper the slope of the linear portion on the BV-V_G curve.

Effect of Oxide Thickness

The influence of various oxide thicknesses on the breakdown voltage versus effective gate-voltage curves is shown in Figure 19. The characteristic curves tended to increase with a slope more steep for the smaller oxide thickness.

From Figure 19, the intercepts of these characteristics at the zero effective gate voltage correspond to the constant terms in Equations 4 and 5 and these terms are also a function of oxide thickness.

Although the relationship between the breakdown voltage and oxide thickness was consistent with the empirical result as $BV = (t_{ox})^{0.2}$ (9:980), the characteristic curve

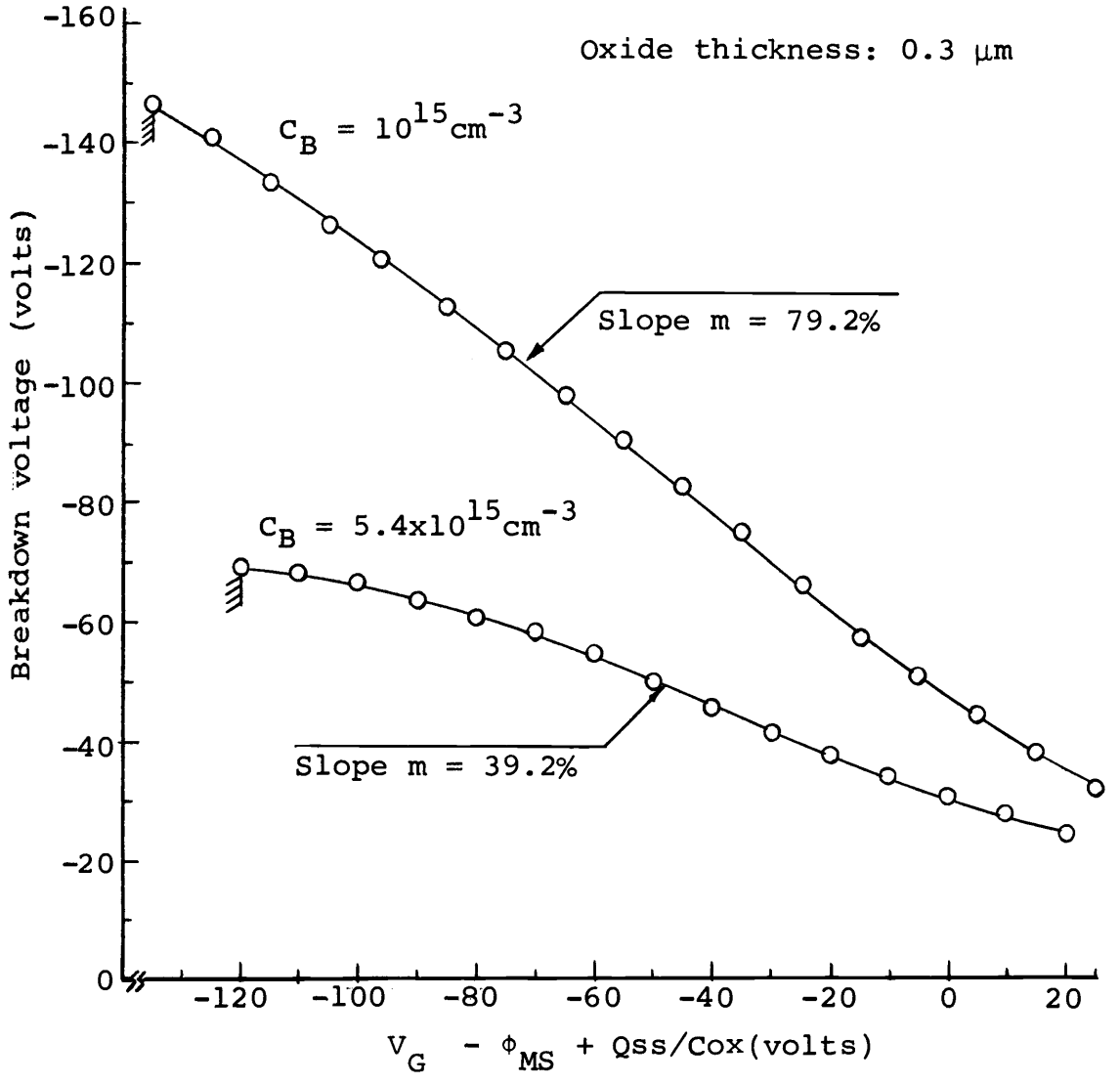


Figure 18. Breakdown voltage versus effective gate voltage for p+-n circular diodes of various substrate impurity concentrations: Cross-hatching shows onset of inversion of substrate surface.

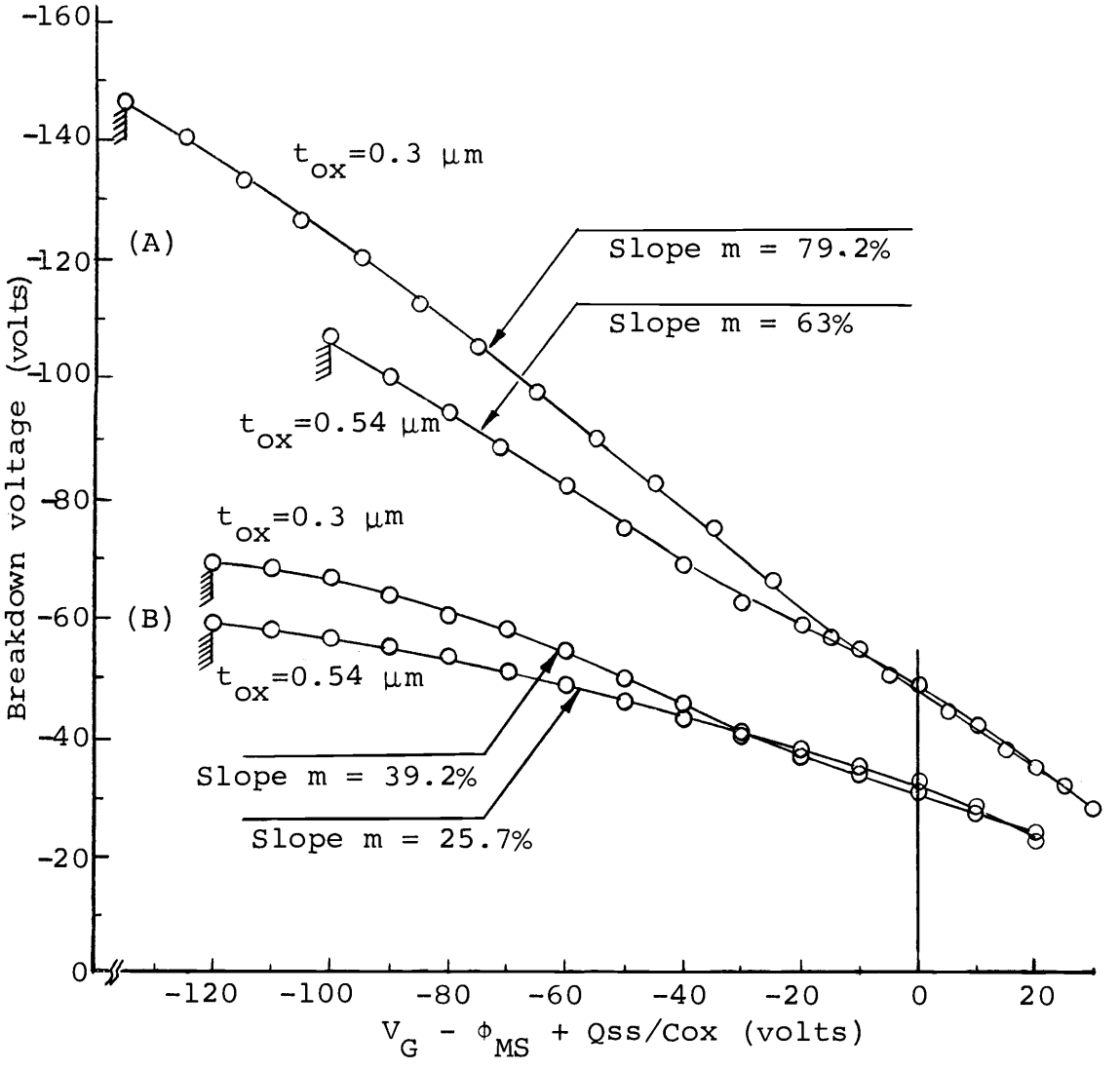


Figure 19. Breakdown voltage versus effective gate voltage for p^+-n circular diodes of various oxide thicknesses.

Curve (A) and (B) represent substrate impurity concentration $C_B = 10^{15}cm^{-3}$ and $5.4x10^{15}cm^{-3}$ respectively.

for the thick oxide sample tended toward saturation at a low breakdown voltage in this particular project.

Voltage Enhancement

When the gate terminal was connected to the diffused area and a reverse voltage was applied with respect to the substrate, the breakdown voltage increased significantly.

This increase in breakdown voltage is the same effect as a gate potential applied by an independent D.C supply. However, it will be useful for practical application in view of obtaining a higher breakdown voltage in planar diodes without an additional D.C supply.

The voltage enhancement can also be obtained by the intercept of the characteristic curve and a straight line, $BV = V_G$.

Figure 20(a) shows the characteristics of the breakdown voltage versus gate voltage with the substrate as a reference.

When the breakdown voltage is measured as a function of the gate potential applied with respect to the diffused p^+ region (b), the slope m' in the region A will be given by m/(1-m); and an intercept of characteristic curve at $V_G=0$ in Figure 20(b) will also be the voltage enhancement.

As shown in Figure 20, the measured voltage enhancement and the measured slope are in close agreement with the calculated values.

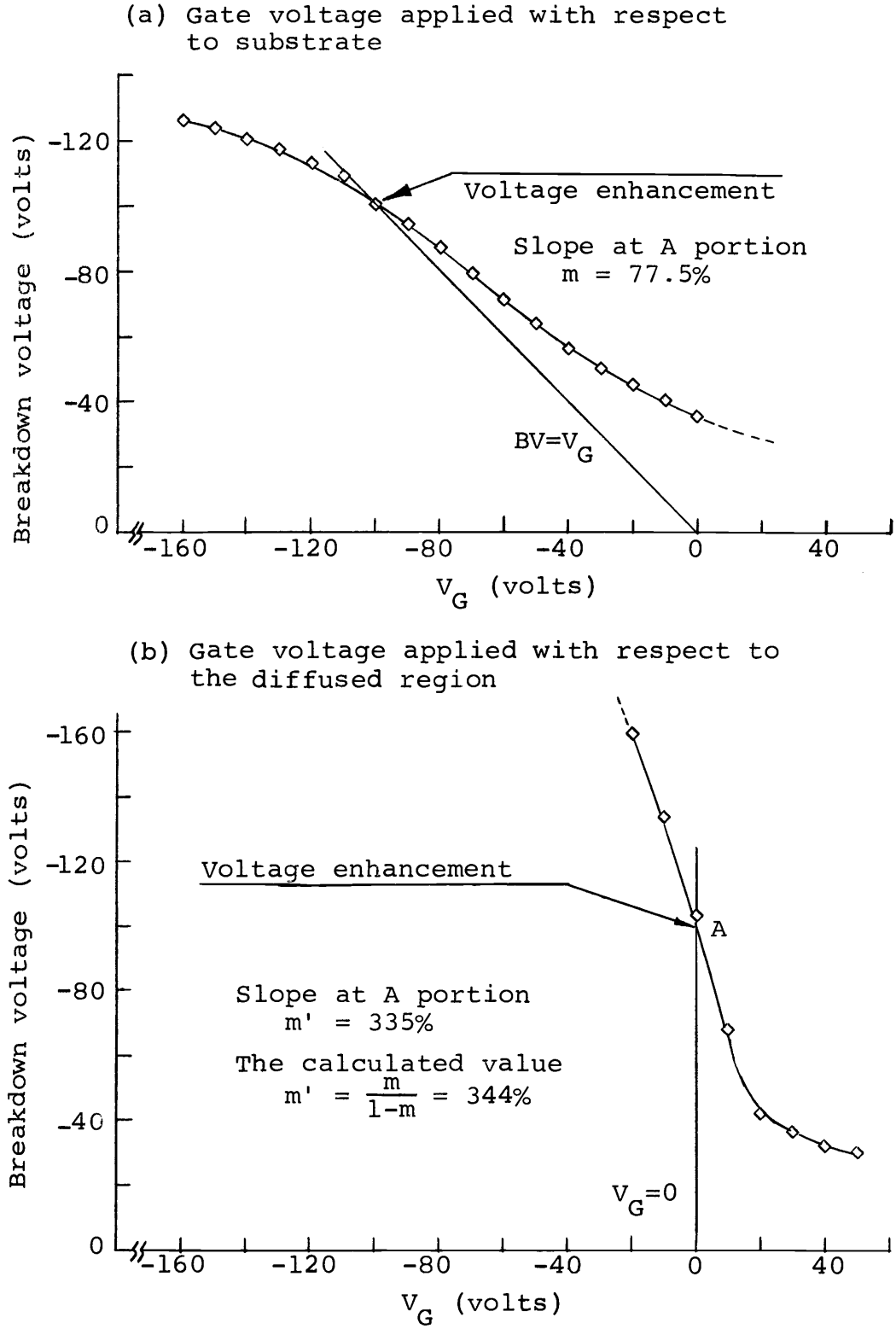


Figure 20. Breakdown voltage versus gate voltage for p^+-n rectangular diode of $N_D = 10^{15} cm^{-3}$ and $t_{ox} = 0.3$ μm.

X. SPACING EFFECT ON THE JUNCTION BREAKDOWN VOLTAGE

As a method to eliminate the limitation of junction breakdown voltage due to the curvature effect, the gate-controlled diodes with an extremely shallow junction have been investigated and resulted in the improvement of the junction breakdown voltage.

For the simple fabrication processes of a microwave transistor, it is necessary to cut out a small portion of the metal field plate which is placed over the collector junction periphery, as shown in Figure 21.

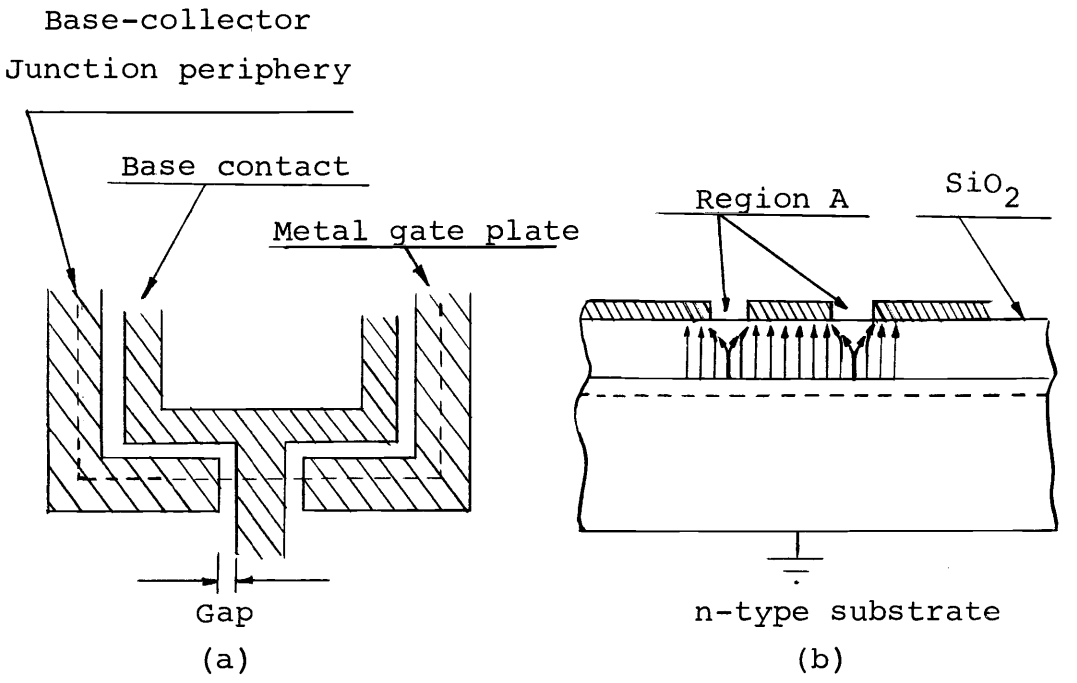


Figure 21. (a) Top view of the rectangular diode with a gap in the gate plate.
(b) Cross-sectional view and electric field lines.

In region A as shown in Figure 21(b), the effect of an external surface field on the junction breakdown will depend on the size of the gap. Thus, three different gaps of 12.7 μm, 6.35 μm and 3.175 μm were designed in this project for the rectangular diodes as shown in Figure 8.

In order to investigate the effect of the size of the gap, the breakdown voltage versus gate potential characteristics were measured for p^+-n rectangular diodes with both dry and wet measurements. A wet measurement was carried out after a conducting path was formed by placing a drop of water on the gaps between the gate metal and base contact lead.

Finally, these two measurements were compared with the data obtained for rectangular diodes with a completely surrounded gate.

Figures 22 and 23 show the breakdown voltage versus gate potential characteristics for the spacings of 12.7 μm and 6.35 μm respectively.

In the figures, curves (1) and (3) show the dry measurement for 5 ohm-cm and 1 ohm-cm respectively. Curves (2) and (4) are the wet measurements, which correspond to the dry measurements, and the dashed lines are the measurements of the rectangular diodes with the completely surrounded gate.

Figure 24 shows the measured characteristic curves for 1 ohm-cm with 3.175 μm spacing.

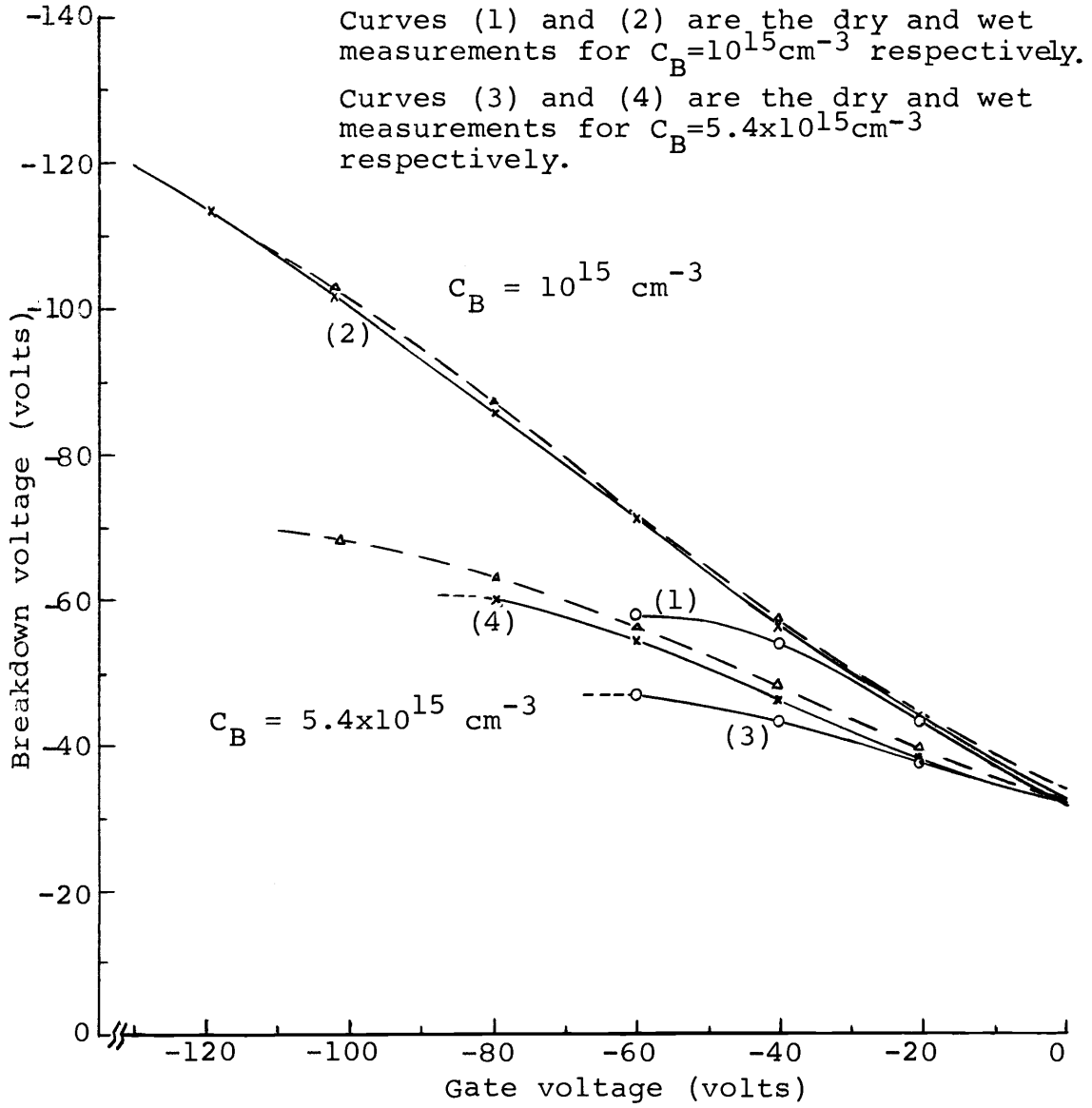


Figure 22. Breakdown voltage versus gate voltage for a gap of 12.7 μm.

Dashed lines are measurements of diodes with the gate metal surrounded completely at the junction edge.
Data points are the average of three samples.

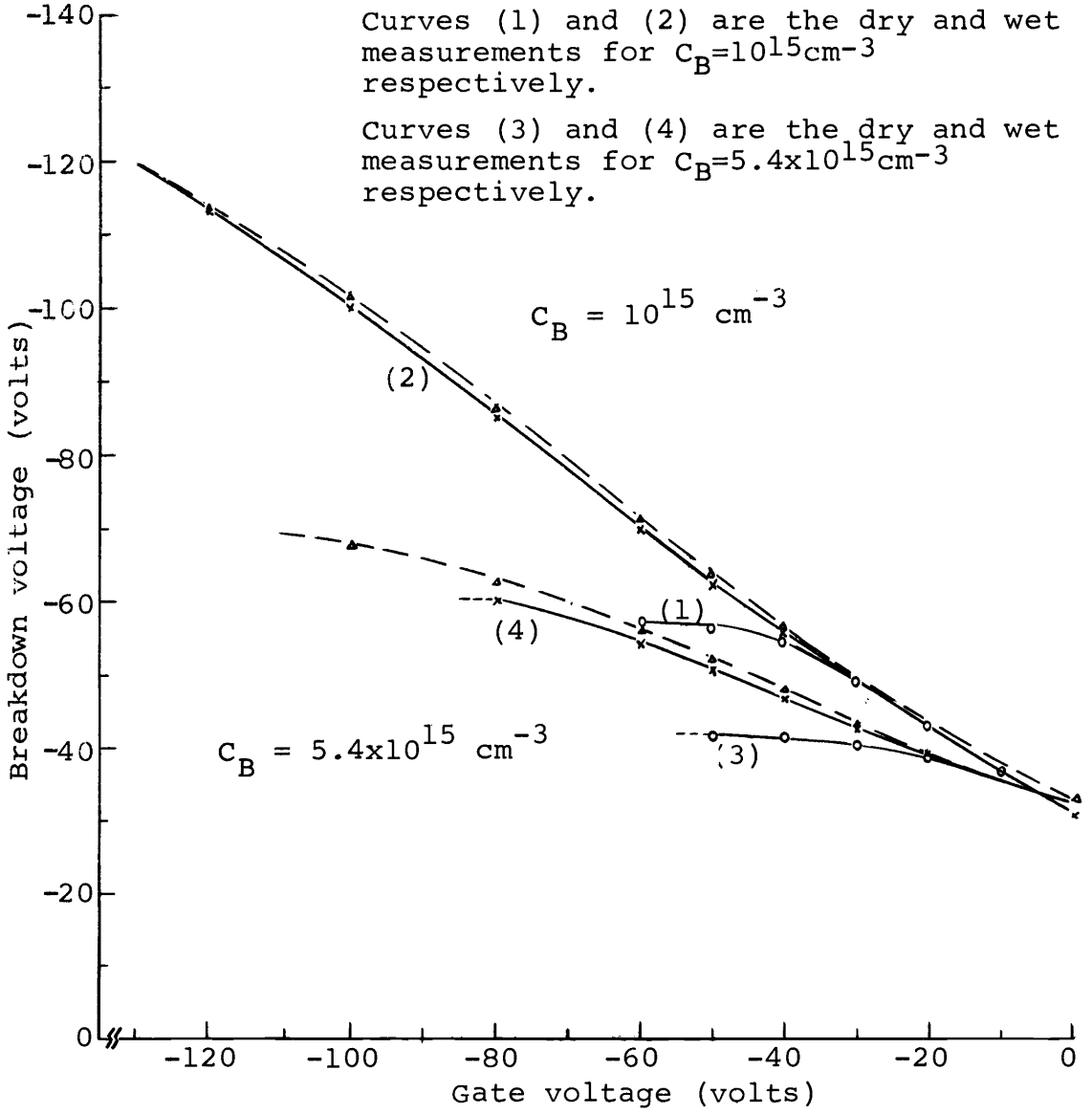


Figure 23. Breakdown voltage versus gate voltage for a gap of 6.35 μm.

Dashed lines are the measurements of diodes with the gate metal surrounded completely at the junction edge.
Data points are the average of three samples.

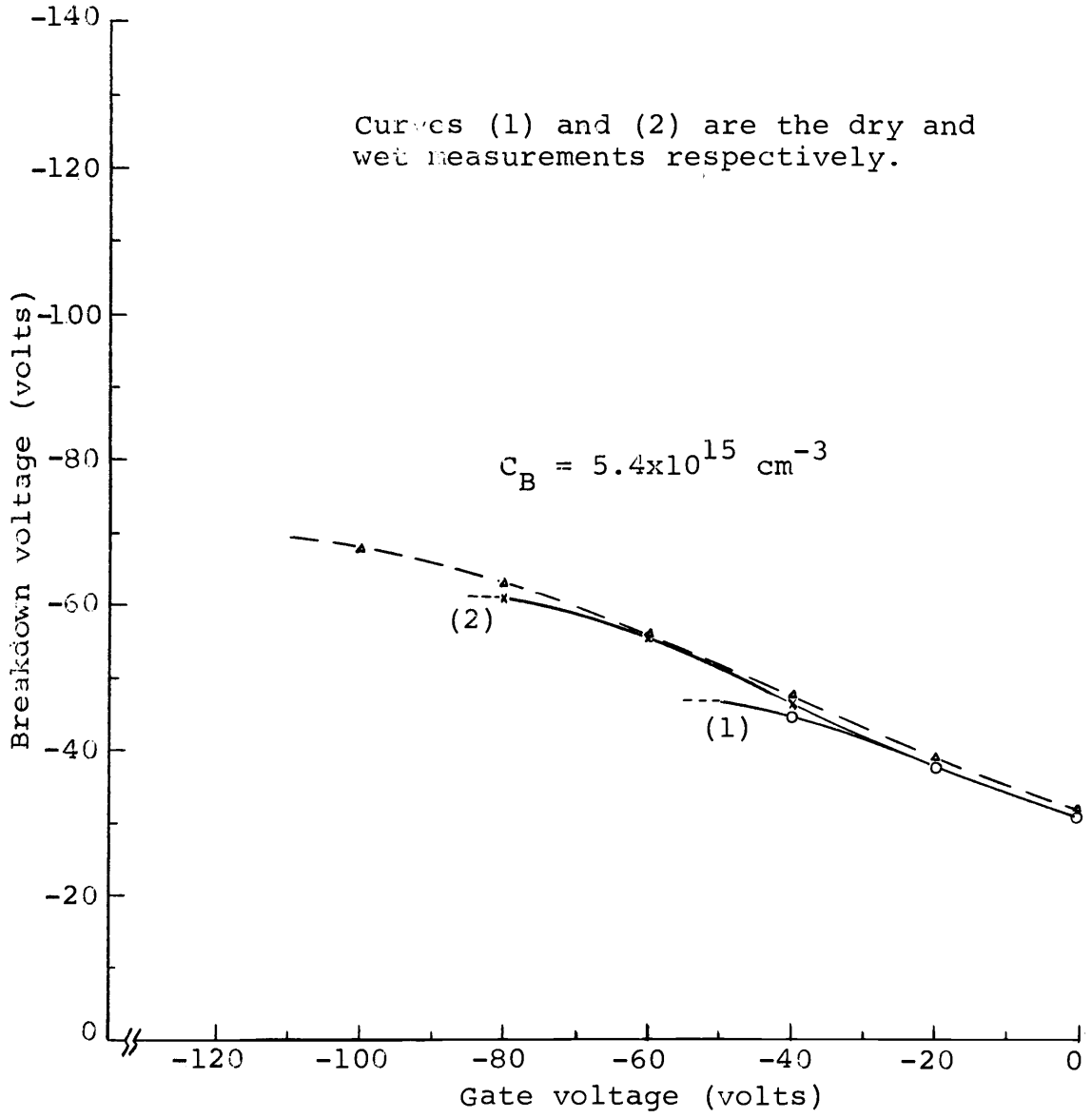


Figure 24. Breakdown voltage versus gate voltage for a gap of 3.175 μm.
Data points are the average of two samples.

Through the experimental measurements, it was readily shown that the breakdown voltage was limited to a low voltage when the external surface field was applied to a gate with a gap. The behavior of the breakdown voltage increasing was initially the same as that of rectangular diode with the completely surrounded gate. In this low gate potential region, the increase in breakdown voltage was considered as reducing the effect of mobile oxide charges at the n-type surface.

However, the characteristics of a dry measurement tended toward saturation at a low breakdown voltage, when the surface began to be depleted as the gate field increased. But the corresponding characteristics of a wet measurement gave results close to the measurements of rectangular diodes with the gate metal completely surrounded. As a result, when the gate metal was not completely around the junction periphery, the improved breakdown voltage was negligibly small at any spacing and any substrate impurity concentration.

XI. SUMMARY AND CONCLUSIONS

In order to improve the voltage capability of the diffused, shallow-collector junction of a microwave transistor, the effect of surface fields on the breakdown voltage was studied experimentally for p^+-n silicon diodes with a junction depth of 0.5 μm.

From the results of section IX, it was shown that the breakdown voltage could be increased over a wide range by the application of an external gate potential.

The results in this project were consistent with those investigated by Grove et al. (8).

However, in contrast to the results reported by de Graaf (3), it was found that the oxide thickness and substrate impurity concentration had an influence on the slope of the $BV-V_G$ curve. The slope m approaches unity for low substrate impurity concentrations and for small oxide thicknesses.

Regarding the effect of junction curvature on avalanche breakdown for the abrupt junctions, experimental data (from Figures 13 to 16) were obtained for p^+-n circular and rectangular diodes.

At the zero effective gate voltage, the breakdown voltage of circular diode was higher than that of rectangular diode by 3% for 1 ohm-cm and by 6% for 5 ohm-cm materials. Furthermore, when the surface was depleted,

the increase in breakdown voltage tended to be less rapid for the rectangular diode than for the circular diode.

Since the voltage enhancement was obtained from the curve of $BV-V_G$ by the intercept of the characteristic curve and the straight line, $BV = V_G$, the steeper slope of the characteristic curve resulted in the higher voltage enhancement.

From the results of section X, it was shown that the improved breakdown voltages were negligibly small at any substrate impurity concentration when the external surface field was applied to the gate metal which was not placed completely over the junction edge. Consequently, for application to a microwave transistor, it is necessary that multi-layer metal and dielectric depositions are included in order to separate the two layers of the gate and base contact metals (22).

In reducing the necessary gate voltage, the characteristics of the insulating layer was one of the most important factors. Since the voltage enhancement was obtained near the saturation region on the $BV-V_G$ curve, a high breakdown voltage could be obtained without an extra D.C supply.

Thus, for the high collector junction breakdown of the n-p-n microwave transistor, the most desirable model is proposed in this project by the physical structure in which the gate is connected to the diffused region of

the emitter or base.

As shown in Figure 25, the additional parasitic capacitances of the gate-to-collector (C_{gc}) and gate-to-base (C_{gb}) will be added to those of the intrinsic bipolar transistor.

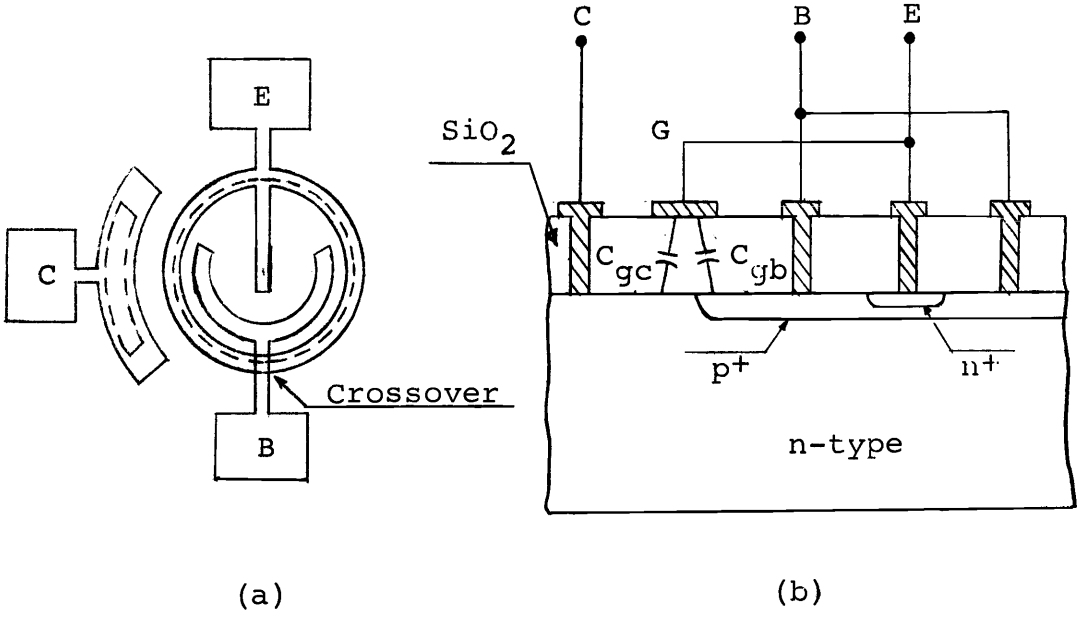


Figure 25. The physical structure of a high voltage microwave transistor (a) and the additional parasitic capacitances (b).

The effect of parasitic capacitances on frequency response will depend on the operational configurations as shown in Figure 26.

The capacitance of C_{gb} will have no effect if the gate is connected to the base. But when the gate is connected to the emitter, both capacitances of C_{gb} and C_{gc} will affect the frequency response.

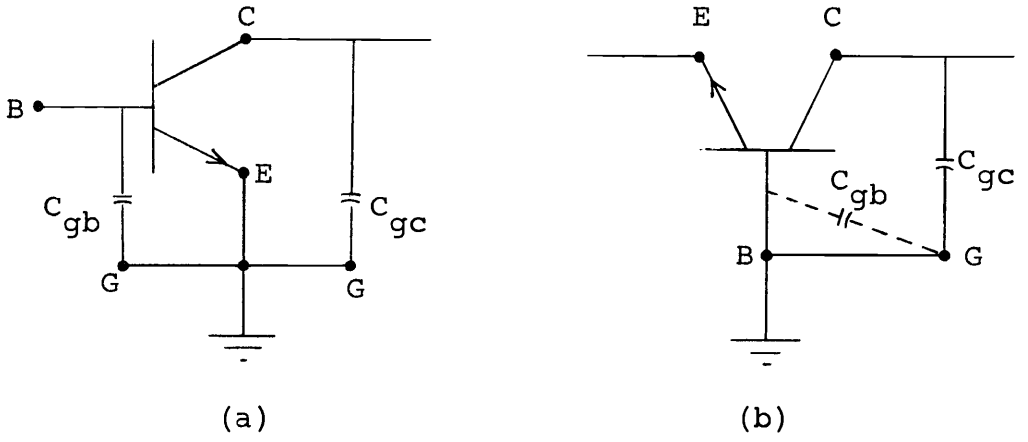


Figure 26. The effective parasitic capacitances of common configurations, common-emitter (a) and common-base (b).

Thus, although a higher breakdown voltage of the collector junction can be obtained by the above physical structure, a lower bandwidth will result. Also, a multi-layer metal and dielectric deposition is required as the additional process of device fabrication.

BIBLIOGRAPHY

1. Castrucci, P. P. and J. S. Logan. Electrode controls of SiO_2-passivated planar junctions. IBM Journal Res. and Dev. 8:396-399. 1964.

2. Cooke, H. F. Microwave transistor: Theory and design. Proceedings of the IEEE 59:1163-1181. 1971.

3. De Graaf, H. C. Gate-controlled surface breakdown in silicon p-n junctions. Philips Res. Repts. 25:21-32. 1970.

4. Goetzberger, A., B. McDonald et al. Avalanche effects in silicon p-n junctions. II. Structurally perfect junctions. Journal of Applied Physics 34:1591-1600. 1963.

5. Gregor, L. V. Passivation of semiconductor surfaces. Solid State Technology 14:37-43. April 1971.

6. Grove, A. S. Physics and technology of semiconductor devices. New York, John Wiley and Sons, 1967. 366 p.

7. Grove, A. S., B. E. Deal et al. Investigation of thermally oxidized silicon surfaces using metal-oxide-semiconductor structures. Solid-State Electronics 8:145-163. 1965.

8. Grove, A. S., O. Leistiko, Jr. et al. Effect of surface fields on the breakdown voltage of planar silicon p-n junctions. IEEE Transactions on Electron Devices 14:157-162. 1967.

9. Gurtler, R. W. Avalanche drift instability in planar p-n junctions. IEEE Transactions on Electron Devices 15:980-986. 1968.

10. Ihantola, H. K. Multiple-Guard-Ring (MGR) structure for planar p-n junction. Acta Polytech. Scandianavica. Ser. Ph 63:1-36. 1969.

11. Kennedy, D. P. and R. R. O'Brien. Avalanche breakdown calculations for a planar p-n junction. IBM Journal Res. and Dev. 10:213-219. 1966.

12. Kressel, H. A review of the effect of imperfections on the electrical breakdown of p-n junctions. RCA Review 28:175-207. 1967.

13. Leistiko, O. and A. S. Grove. Breakdown voltage of planar silicon junctions. Solid-State Electronics 9:847-852. 1966.

14. Looney, J. C. Private communication.

15. Revesz, A. G. and K. H. Zaininger. Si-SiO_2 solid-solid interface system. RCA Review 29:22-76. 1968.

16. Root, C. D., D. P. Lieb et al. Avalanche breakdown voltage of diffused silicon and germanium diodes. IRE Transactions on Electron Devices 7-8:257-262. 1960.

17. Schlegel, E. S., G. L. Schnable et al. Behavior of surface ions on semiconductor devices. IEEE Transactions on Electronic Devices 15:973-979. 1968.

18. Snow, E. H., A. S. Grove et al. Ion transport phenomena in insulating films. Journal of Applied Physics 36:1664-1673. 1965.

19. Speeney, D. V. and G. P. Carey. Experimental study of the effect of junction curvature on breakdown voltage in Si. Solid-State Electronics 9:831-845. 1966.

20. Sze, S. M. Physics of semiconductor devices. New York, John Wiley and Sons, 1969. 812 p.

21. Sze, S. M. and G. Gibbons. Effect of junction curvature on breakdown voltage in semiconductors. Solid-State Electronics 9:831-845. 1966.

22. Tolliver, D. L. and C. J. Santoro. Deposited oxide contours in multi-layer metal circuitry. Solid State Technology 14:32-36, April 1971.

23. Townsend, W. G. and A. J. Strachan. An investigation of lateral diffusion in silicon. Solid-State Electronics 14:551-556. 1971.

24. Wang, S. Solid state electronics. New York, McGraw-Hill Book Co., 1966. 778 p.

25. Zaininger, K. H. and F. P. Heiman. The C-V technique as an analytical tool. Solid State Technology 13: Part 1:49-56, May 1970. Part 2:46-55, June 1970.

APPENDIX

APPENDIX I

Calculation of the Planar Breakdown Voltage for a Cylindrical-abrupt Junction

The maximum field for the impurity concentration 10^{15} atoms/cm^3 with a junction depth of 0.5 μm is 5.3×10^5 volt/cm, from Figure b in Appendix II.

The corresponding depletion width (W) is given by Equation 3:

$$W = \frac{10^{16}}{N_B} (\epsilon/\epsilon_{si}) \frac{Em}{1.6 \times 10^5} = 10 \times \frac{5.3}{1.6} = 33 \ \mu m$$

From Equations 1 and 2, the planar breakdown voltage is given by:

$$VB_{planar} = VB_{plane} \times \left\{ \left[(n+1+R) R^n \right]^{1/(n+1)} - R \right\},$$

where $R = r_j/W$ and $n = 1$ for the cylindrical abrupt junction.

Thus the correction term is:

$$\left[(2 + \frac{0.5}{33}) \frac{0.5}{33} \right]^{1/2} - \frac{0.5}{33} = 0.159$$

$$VB_{planar} = 330 \times 0.159 = 52.5 \text{ volts}$$

In the same way, the planar breakdown voltage is calculated for the impurity concentration 5.4×10^{15}/cm^3.

The maximum field is 5.4×10^5 v/cm and the corresponding depletion width (W) is given by 6.2 μm.

And the correction term is:

$$\left[(2 + \frac{0.5}{6.2}) \ (\frac{0.5}{6.2}) \right]^{1/2} - (\frac{0.5}{6.2}) = 0.33$$

Therefore, the planar breakdown voltage is:

$$VB_{planar} = 96 \times 0.33 = 32 \text{ volts}$$

APPENDIX II

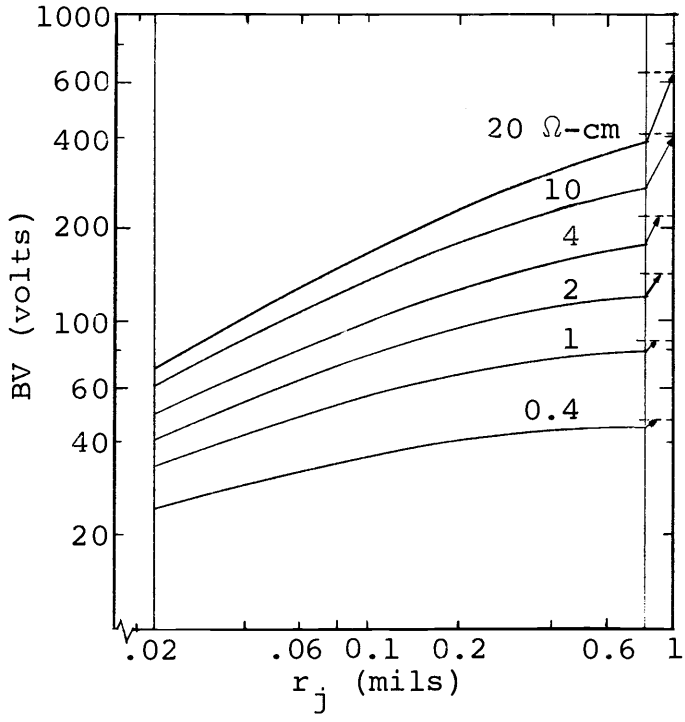


Figure a. Breakdown voltage vs. junction depth, r_j, for diffused p^+-n planar junctions for various values of substrate doping (Ref. 12).

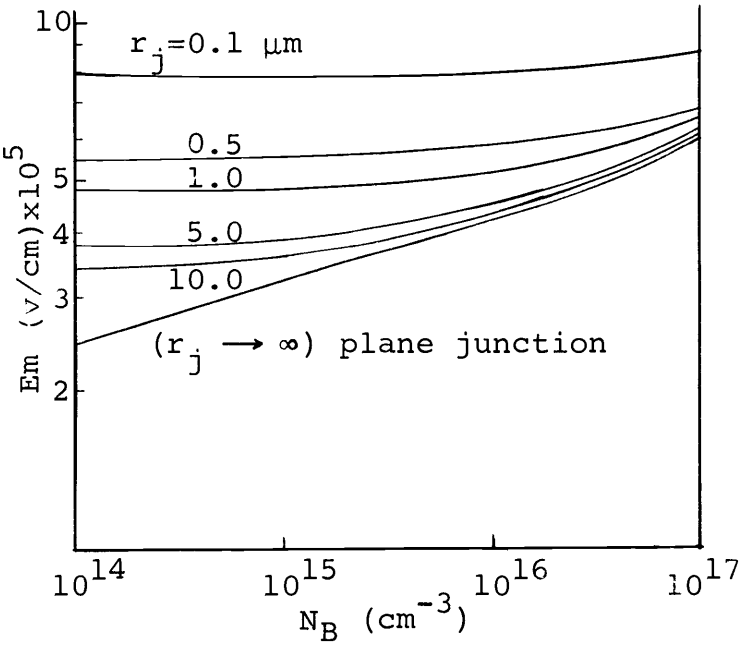


Figure b. Maximum field, Em, vs. substrate impurity concentration for different values of junction radius, r_j, for cylindrical-abrupt junctions in Si (Ref. 21).

APPENDIX III

TABLE I. SPECIAL ETCHING SOLUTION OF THE PYROLYTICALLY DEPOSITED SiO_2 (14)

4 : 1 = buffered HF* (70% concentration of HF) : ethylene-glycol (30%)

* Buffered HF:

1. Add HF to saturated NH_4F solution in the volume ratio of 4 : 1 (NH_4F : HF)
2. Saturated solution of NH_4F is about eight parts by weight of NH_4F to 15 parts by weight of deionized water.

TABLE II. THEORETICAL BREAKDOWN VOLTAGES OF THE PLANE (BV_{PLANE}) AND PLANAR (BV_{PLANAR})

Doping level	BV_{plane}	BV_{planar}
$C_B = 10^{15}$ cm^{-3}	330 volts	52.5 volts
$C_B = 5.4 \times 10^{15}$ cm^{-3}	96 volts	34 volts

TABLE III. EXPERIMENTAL SAMPLE DATA

1. 1 Ω-cm <111> -oriented n-type silicon

Device No.	Oxide Thickness	Surface State Density	$\lvert -\phi_{MS}+Qss/Cox \rvert$ (volt)	BV at $V_G-\phi_{MS}+Qss/Cox=0$	Slope m (%)	Voltage Enhancement (volt)	Diffusion Source
No. 1 (Fig.13)	0.3 μm	$3.2\times10^{11}cm^{-2}$	R.D : 5	30 volt	38.9	45.2	Boron Nitride Powder
			C.D : 5	31.1 "	39.2	48.2	
No. 2 (Fig. 14)	0.54 μm	$5.4\times10^{11}cm^{-2}$	R.D : 15	31 "	24.2	36	Boron Nitride Wafer
			C.D : 15	32.6 "	25.7	41	
2. 5 Ω-cm <100> -oriented n-type silicon							
No. 3 (Fig.15)	0.3 μm	$4.5\times10^{11}cm^{-2}$	R.D : 20	44.5 "	75.1	103	Boron Nitride Powder
			C.D : 25	47.1 "	79.2	123	
No. 4 (Fig. 16)	0.54 μm	"	R.D : 24	47 "	57	68.5	"
			C.D : 27	49.1 "	63	70.5	

R.D and C.D represent rectangular and circular diodes respectively.