AN ABSTRACT OF THE THESIS OF

David Kin-Poon Cheung (Name) for the M.S. (Degree)

in Electrical Engineering (Major) presented on Nov. 30, 1967. (Date)

Title: COMPATIBLE FIELD-EFFECT AND BIPOLAR TRANSISTORS

Abstract approved: [redacted]
Associate Professor James C. Looney

Four methods for the simultaneous fabrication of field-effect and bipolar transistors have been investigated. The basic process involves obtaining two different junction depths by a single diffusion. This was accomplished by the techniques of (1) partial masking, (2) two depositions, (3) etched channels, and (4) oxide depletion.

The first three methods were used for the fabrication of compatible field-effect and bipolar transistors. Each of the methods was evaluated on the basis of reproducibility, uniformity and predictability.

The field-effect transistor parameters obtained were comparable for all three methods. However, the two-deposition process was considered to be the best of the three because of its excellent reproducibility and the simplicity in its process steps.

COMPATIBLE FIELD-EFFECT AND BIPOLAR TRANSISTORS

by

David Kin-Poon Cheung

A THESIS

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Master of Science

June 1968

APPROVED:

[redacted]

Associate Professor of Department of
Electrical and Electronics Engineering

[redacted]

Head of Department of Electrical and
Electronics Engineering

[redacted]

Dean of Graduate School

Date thesis is presented Nov. 30, 1967

Typed by Erma McClanathan for David Kin-Poon Cheung.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

Figure

Figure

ACKNOWLEDGMENT

The author wishes to express his gratitude to Professor James C. Looney for his suggestions throughout the course of this thesis.

Also appreciation is expressed to Mr. Paul Cheung for his assistance in preparing the manuscript.

COMPATIBLE FIELD-EFFECT AND BIPOLAR TRANSISTORS

I. INTRODUCTION

It was the objective of this investigation to study the possibility of obtaining a junction field-effect transistor and a bipolar transistor in a compatible circuit by using diffusion techniques and various ways of controlling the initial surface concentration.

The design of this compatible field-effect transistor and bipolar transistor was such that the process of fabrication and the geometry of the bipolar transistor were used as the basis for the design of the field-effect transistor. In other words, if the additional steps for producing the field-effect transistor were deleted, the process would be the same as that used in a bipolar transistor production, and the result would be two bipolar transistors instead of a field-effect transistor and a bipolar transistor.

The two-gate field-effect transistor was designed to have approximately the same geometry as the bipolar transistor except that the channel thickness was to be smaller than the base region of the bipolar transistor and that its channel breakdown voltage was to be higher than the normal base-emitter breakdown voltage (see Section III). The gate 1 and gate 2 regions of the field-effect transistor had the same doping level,

junction depth, and thickness as the collector and the emitter regions of the bipolar transistor respectively. The channel width was determined by the surface concentration and the diffusion time of the channel diffusion cycle. The channel breakdown voltage was determined by its doping level. Since it was the same diffusion that yielded the channel and the base regions, something had to be done to the channel region of the field-effect transistor during its diffusion process so that it had a shallower junction depth and lighter doping level than the base region of the bipolar transistor.

The diffusion of boron into n-type single crystal silicon to obtain a p-type region has been studied extensively (20, 36, 38, 47). The present technique involved deposition of boron onto a masked substrate and thermal diffusion at an elevated temperature for a given time interval to obtain a single junction depth. However, to obtain two or more junction depths through one single diffusion process, as is required in the field-effect and bipolar transistor fabrication, involved more than merely deposition and diffusion. Four possibilities were studied in this thesis and three of them were found to yield good results.

The four different methods to arrive at two or more junction depths through one single diffusion process as

listed in this thesis are given below:

1. Partial oxide-masking
2. Two-deposition
3. Etched-channel
4. Oxide depletion

The first three methods have been investigated and they have been applied to the development of the compatible field-effect and bipolar transistors. The fourth method is more critical and has not been investigated experimentally.

The partial oxide-masking method was accomplished through partial masking of the channel region of the field-effect transistor by a thin layer of silicon dioxide during the deposition of boron. The result was that the surface concentration of the channel was smaller than the unmasked base region of the bipolar transistor. Diffusing for the same time interval, after the partially masked deposition for both the field-effect transistor and bipolar transistor, gave a smaller channel junction depth than the base junction depth and a correspondingly smaller average doping level in the channel region.

The two-deposition method involved two separate deposition processes to arrive at the difference in the surface concentration between the channel region of the field-effect transistor and the base region of the

bipolar transistor. The channel region was masked from the boron diffusion during the first deposition process which deposited the base region to a given surface concentration. Then it was unmasked and both of the regions were deposited a second time. The result was that the base region had a higher effective surface concentration (being deposited twice, besides the fact that the first deposition could be of a higher boron concentration) than the channel region which had been subjected to only one deposition. Diffusing for the same time interval after the second deposition was made, different junction depths and doping levels between the channel and the base regions were obtained.

In the case of the etched channel method, the channel region and the base regions were deposited at the same time and were diffused for the same time interval without any partial masking. This resulted in the same junction depth and average doping level in both regions after diffusion. The channel region was then selectively etched with silicon etch such that the channel region was indented. In this case, the difference between the channel depth and the base region was the depth of the channel region silicon being etched away.

The last method -- oxide depletion method -- has not been investigated. The suggested method was that

the base region and the channel region would be deposited at the same time with some oxygen introduced during the deposition cycle. Then the oxide layer at the channel region grown during deposition would be removed. A heavy oxidizing atmosphere would be introduced during diffusion such that the boron deposited on the surface would diffuse out of the channel region surface into the freshly grown oxide layer and the surrounding oxidizing gas, depleting it of the boron supply, while the boron saturated oxide layer at the base region would act as a buffer to decrease the diffusion of the dopant from the silicon surface out into the freshly grown oxide layer. After diffusion, a difference in the junction depth would be obtained.

After the channel diffusion, the gate 1 region (which has the same depth as the emitter of the bipolar transistor) and the emitter region were diffused on top of the channel or the base region. The samples were then metallized with an evaporated aluminum film alloyed onto the contact regions prepared from contact-hole photo-resist mask-etching steps.

II. THEORY AND OPERATION OF FIELD-EFFECT TRANSISTOR

In the presence of a reverse bias, a charge depletion region appears at the junction area of a p-n diode (31, 32, 36, 38, 39, 44, 47, 50). In case of a n^+-p step junction where one side is heavily doped while the other side of the junction is lightly doped (Fig. 1), this depletion layer thickness (X_m) is given by (35):

$$X_m = 10^4 \ (2\epsilon\varepsilon_0 V_t/qN)^{\frac{1}{2}} \text{ micron} \tag{1}$$

where N is the net impurity concentration (atom/cm^3) on the lightly doped side. For silicon,

$$X_m = (3.65) \ 10^{11} \ (V_t/N)^{\frac{1}{2}} \text{ micron} \tag{2}$$

The field-effect transistor operated by means of the pinching effect of this depletion layer. Two such junctions at each side of a semiconductor channel (Fig. 2) will have the effect of pinching off the channel current when the two depletion layers together extend to the full thickness of the channel. Therefore the pinch-off voltage V_p is given as (35):

$$V_p = (7.52) \ 10^{-16} \ X_c^2 \ N \text{ volts} \tag{3}$$

The source-drain current is given by the relationship (35)

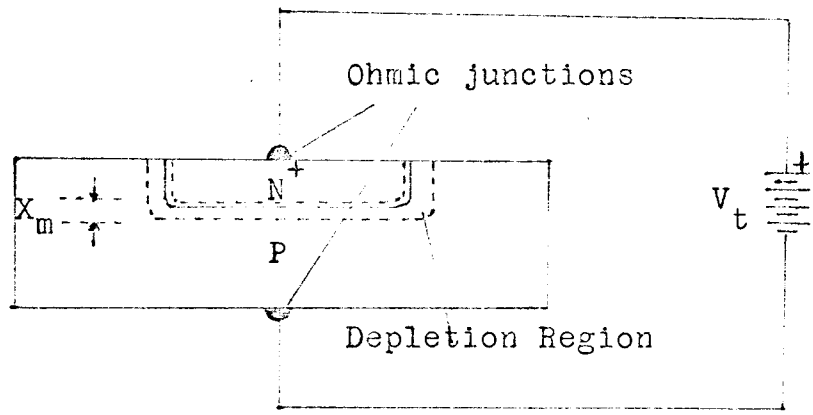


Fig. 1. Depletion Region of a reverse-biased N^+-P junction

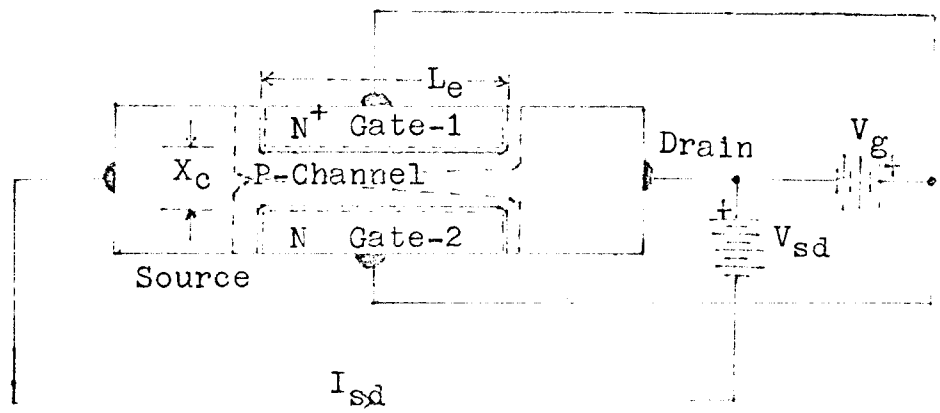


Fig. 2. Pinch off of a field-effect transistor channel

$$I_{sd} = \left[1 - 2/3\ (V_{sd}/V_p)^{1/2}\right] V_{sd} X_c W_c q U_c N/3L_e \text{ amps.} \quad (\text{at } V_g = 0) \qquad (4)$$

and the maximum transconductance (open channel conductance) by (35)

$$G_0 = X_c W_c q U_p N_c / L_e \qquad \text{mhos at } V_g = 0 \qquad (5)$$

The gate breakdown voltage of the field-effect transistor is a function of the highest doping level of its channel which occurs at the surface. The relationship between the highest doping level and the average doping level is quite complicated. Such a relationship is described in Appendix A-1.

III. THE DESIGN CONSIDERATIONS OF THE FIELD-EFFECT TRANSISTOR

The objective of the design of these compatible field-effect and bipolar transistors is that the process of fabrication and the geometry of the bipolar transistor are to be used as the basis for the parameters of the field-effect transistor (Figs. 3 and 4). In other words, if the additional steps for producing the field-effect transistor are deleted, the process will be the same as that used in a bipolar transistor production, and the result will be two bipolar transistors instead of a field-effect transistor and a bipolar transistor.

The two-gate field-effect transistor is designed to have approximately the same geometry as the bipolar transistor except for the depth of the channel region. The gate 1 and gate 2 regions of the field-effect transistor have the same doping level, junction depth and thickness as the collector region and the emitter region of the bipolar transistor respectively. (See Figs. 3 and 4).

If the channel region of the field-effect transistor has the same geometry (channel thickness) and doping level as the base region of the bipolar transistor -- in other words, if the base of the bipolar transistor is used as the channel for the field-effect transistor --

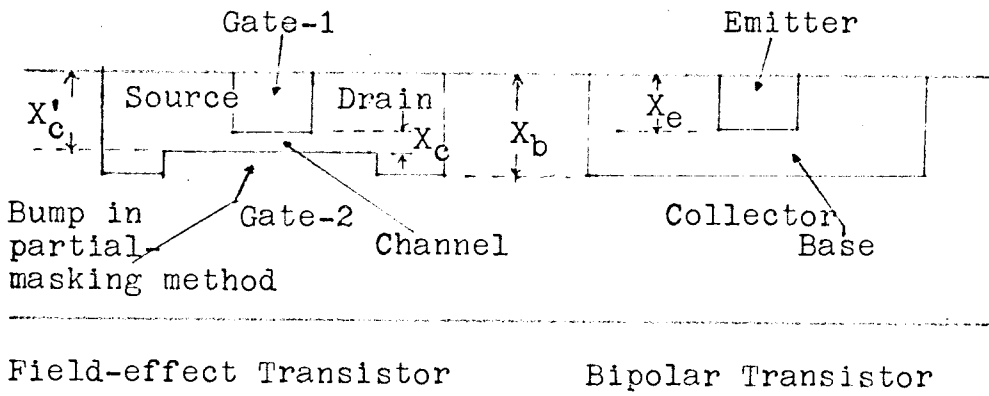


Fig. 3. Difference between a field-effect transistor and a bipolar transistor

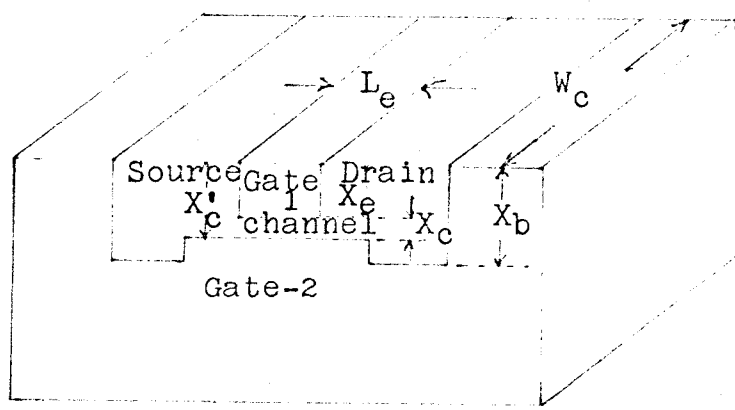


Fig. 4. Geometry of field-effect transistor

a voltage of five to six volts will be required to pinch off this channel. However, the breakdown voltage occurring near the surface where the doping level of the base is highest is about four volts (10^{19} at/cm^3). This means that the source to gate junction will breakdown at the surface before the channel even pinches off.

To decrease the pinch-off voltage, either the channel thickness, X_c, or its doping level, $\bar{N}_c$, must be decreased (4). The methods of partial-masking, two-deposition , and oxide-depletion are concerned mainly with decreasing the channel thickness. However, in the process of decreasing the channel thickness, its doping level is also decreased at the same time. The etched channel method deals with the decreasing of the surface doping level, but it has the additional effect of decreasing the channel thickness at the same time.

It will be shown that it is more efficient to decrease the pinch-off voltage by decreasing the channel thickness, X_c, than by decreasing the channel doping level, N_c, alone. Since the transconductance also varies with X_c and a higher transconductance means a better field-effect transistor, it is desirable to find the parameter which can yield the maximum ratio E of transconductance to the pinch-off voltage. Such a ratio is given as

$$E = g_o/V_p = C/X_c$$

$$\text{where } C = 8W_c\varepsilon\varepsilon_o\mu_p/L_e \qquad (6)$$

Decreasing X_c will, as is shown in the equation, increase the ratio (E) of the transconductance to pinch-off voltage, while decreasing the doping level will not yield a maximum in E. Therefore it is more desirable to decrease the pinch-off voltage by decreasing the channel thickness, X_c, than by decreasing the doping level, N_c, alone. All four processes as listed in this thesis are designed primarily to decrease the channel thickness, while the etched channel process has the additional feature of decreasing the surface doping level.

Since it is the same diffusion that diffuses the channel region and the base region simultaneously, parameters like diffusion time and temperature can not be used to influence the variation of the channel diffusion depth or its doping level. The surface concentration and the substrate geometry are the only parameters available for making the channel depth and its doping level different from the base region. Three of the four methods cited in this thesis have the effect of varying the channel surface concentration while leaving the base surface concentration unchanged during deposition. They are

1. partial masking,
2. two-depositions, and
3. oxide depletion.

The fourth method cited (etched-channel) actually used a variation of the substrate geometry at the channel region to arrive at the difference in diffusion depth and the doping level between the channel and the base regions. As a result, its geometry is different from the geometry obtained from the other three methods (Fig. 5).

These four methods are discussed in detail in a later section. The geometry of the bipolar transistor and the field-effect transistor produced from the four methods are given as reference in Fig. 5.

A Gaussian distribution type diffusion process is chosen for all the diffused regions such that a more even impurity concentration can be obtained. The Gaussian type of diffusion also improved the field-effect transistor characteristics by lowering the surface doping level at the source-drain region such that the source to gate junction breakdown voltage is much higher than that obtained from the complementary error distribution type of diffusion.

The relationships describing the surface concentration, impurity distribution, diffusion time, and

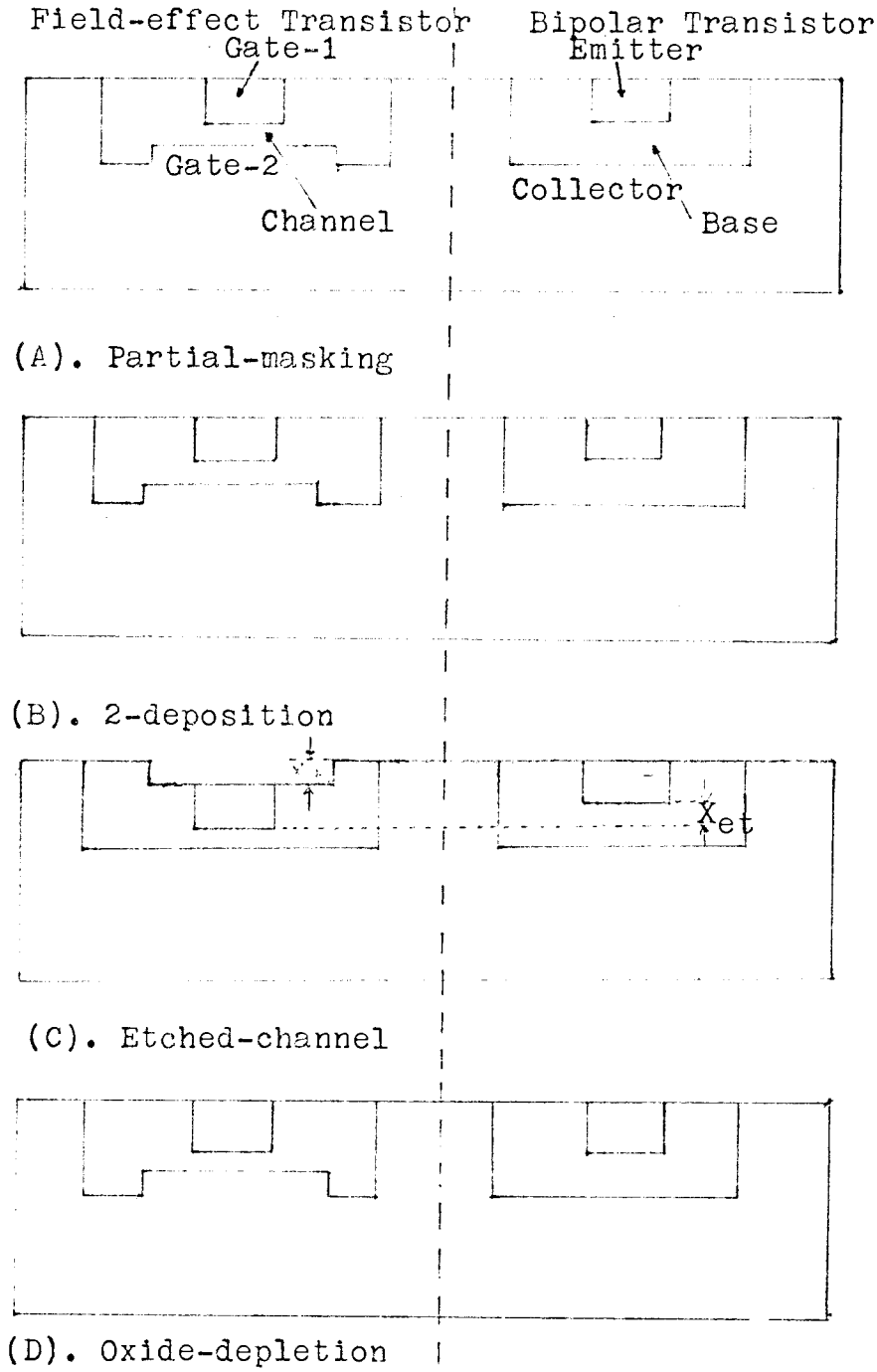


Fig. 5. Geometrical difference between the transistors obtained from: (A).Partial-masking, (B) Two-deposition, (C) Oxide-depletion methods.

junction depth are given in Appendix A-2 for reference.

IV. PARTIAL-MASKING METHOD

1. Partial-Masking

The first method develops from the fact that a thin silicon-dioxide layer offers the characteristic of partially masking the deposition of boron onto the silicon substrate (13, 23, 25, 45, 51). The resulting partially masked surface concentration is smaller than the unmasked surface concentration.

During diffusion, if both of the regions are diffused at the same temperature and for the same length of time, the region having a higher impurity surface concentration diffuses in deeper than the region with a lower surface concentration. Thus two different junction depths and doping levels will be obtained.

In the application to the compatible field-effect transistor and the bipolar transistor, the channel region is partially masked from the boron deposition. The surface concentration and hence the diffusion depth and the doping level of the channel region can be controlled from practically no deposition of impurity to no masking at all by the extent to which the channel region is masked.

In order to understand the mechanism of partially masking the boron diffusion by silicon-dioxide film, the

following sections of thermal growth and partial masking ability of silicon dioxide film are provided as a brief introduction.

2. Thermal Growth of Silicon Dioxide Film

Silicon dioxide film is usually formed by thermally oxidizing silicon at high temperature in a favorable oxidizing atmosphere such as dry oxygen, wet oxygen, or steam (12, 15, 16, 18, 19). The only stable oxide reported at high temperature was silicon dioxide. B. E. Deal and A. S. Grove have reported a quadratic form of oxide thickness as a function of time as given below:

$$2X_o/A = \left[1 + (t+T)4B/A^2\right]^{1/2} - 1 \qquad (7)$$

where X_o is the oxide thickness and (t) is the oxidation time. The constants are given in the literature (12).

3. Partial-Oxide Masking

In the deposition process, boron as an impurity is diffused from the high boron concentration gas through the oxide layer onto the silicon surface. The diffusion can be described by the complementary error distribution function with two boundaries, as discussed by Shiro Horiuchi and Jiro-Yamaguchi (23).

The minimum oxide thickness required to completely

mask the boron diffusion at a certain concentration, temperature, and diffusion time is called the mask-failure oxide thickness, and is used as the upper limit for the partial-masking oxide thickness. The plot of mask-failure oxide thickness obtained from Integrated Circuit Engineering (25) which is shown in Appendix A-4 is used as a reference in this investigation.

V. TWO-DEPOSITION METHOD

As mentioned in Section IV, the diffusion junction depth depends on the surface concentration, diffusion time, and diffusion temperature (5, 20, 26, 42, 44, 48, 52). The diffusion time and temperature have been chosen to give the desired base doping level and its junction depth. However, surface concentration can be used as the parameter for yielding a variable junction depth in the channel.

Assuming the average concentration of boron ($\overline{N_{so}}$) at the silicon surface has not reached its solid solubility concentration (52), the average surface concentration, $\overline{N_{so}}$, will increase with the deposition time. Neglecting the cooling down and heating up period, each successive deposition at the same temperature has the effect of increasing the total deposition time, resulting in the increase in the average surface concentration.

The average surface concentration can be described by the complementary error function (Appendix A-2).

$$N_{so}(X_{jo},t') = N_{bc}/\text{erfc } 2X_{jo}D^{-1/2}t'^{-1/2}$$

and

$$\overline{N_{so}(t')} = 1.13\ N_s X_{jo}^{-1}\ D^{1/2}\ t'^{1/2}$$

where N_{bc} is the background N-type doping level, (D) is

the diffusion constant of boron in silicon at the corresponding temperature and (t') is the corresponding deposition time. Now

$$Q_{so} = \overline{N_{so}} X_{jo} = 1.13\ N_s D^{1/2} t'^{1/2}$$

where Q_{so} is the sheet surface concentration for the Gaussian diffusion relationship:

$$N(x,t_d) = Q_{so} \pi^{-1/2} D^{-1/2} t_d^{-1/2} \exp\ (-X^2/4Dt_d)$$

$$= Q_{so} \pi^{-1/2} D^{-1/2} t_d^{-1/2} \exp\ (-M/4D)$$

and where $M = X^2/t_d$.

A smaller sheet surface concentration results in a smaller junction depth and it also decreases the gradient M/4D in the Gaussian diffusion relationship. In other words, diffusing for the same time interval, t_d, the junction depth arising from $Q_{so}(t_1+t_2)$ will be deeper than the junction depth obtained from $Q_{so}(t_2)$ if $t_1+t_2 > t_2$.

In the two-deposition process, the channel region of the field-effect transistor is masked from the first boron deposition by which the base region of the bipolar transistor is deposited to an average surface concentration $\overline{N_{so}}(t_1)$ for (t_1) minutes. Then the oxide masking the channel region is removed and the second deposition cycle is applied to both regions for (t_2) minutes. Thus

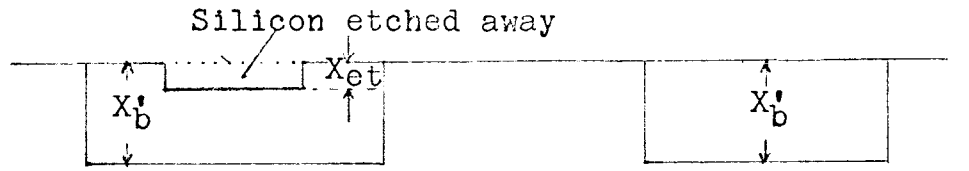
the base region will have an average surface concentration of $\overline{N_{so}}(t_1+t_2)$ from an effective deposition time of (t_1+t_2) minutes while the channel region, being subjected to the second deposition cycle only, will have an average surface concentration of $\overline{N_{so}}(t_2)$ from a deposition time of (t_2) minutes. After diffusion, the junction depth and the average doping level at the base region will exceed the channel junction depth and its doping level because it has a higher average surface concentration.

VI. ETCHED-CHANNEL METHOD

Not only can the surface concentration be used to vary the diffused junction profile, but the actual substrate configuration can also be used for the same purpose. The fact that the diffused junction profile follows the surface configuration is well known; usually this is undesirable. The surfaces of the samples to be diffused are polished flat and are kept from any dirt, oxide or contaminations. However, these are used in a controlled manner in this project to produce the desired results. In this case, the channel region is first deposited and diffused with the base region to the same depth and doping level. Then it is selectively etched down a depth of X_{et} microns. Since this channel region is lower than the base region, after diffusing in the gate region which has the same depth as the emitter region, the resulting channel will be thinner than the base region by a depth of X_{et} microns (Fig. 6).

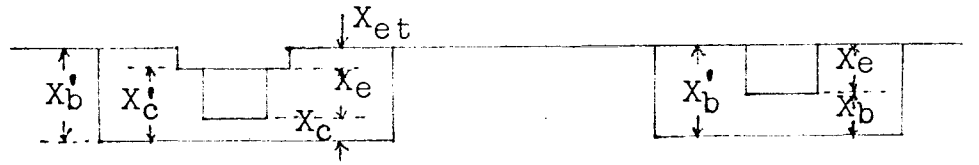
The effective average concentration in this channel region is lower than the base surface concentration, as is shown in Fig. 7.

The relationship of the average conductivity with the distance etched from the surface is described by the ratio (X'_c/X_j) and the corresponding surface concentration as given in Appendix A-1 (26). The surface



Field-effect transistor Bipolar transistor

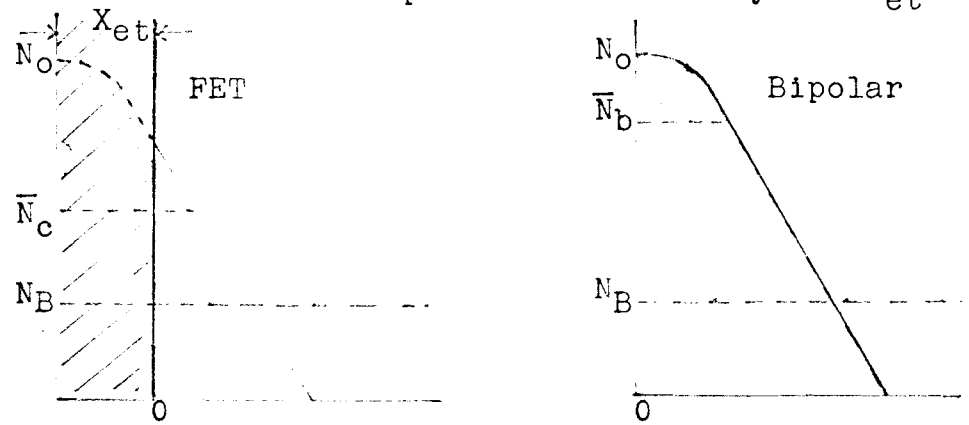
(A)



Field-effect transistor Bipolar transistor

(B)

Fig. 6. (A) Difference between field-effect transistor and bipolar transistor ---(Etched-channel)
(B) Gate-1 of FET is displaced from the emitter of the bipolar transistor by the X_{et}.



Distance from surface Distance from surface

(A) (B)

Fig. 7. Average concentration of (A)Channel of the field effect transistor and (B) Base of bipolar transistor.

concentration, N'_{so}, corresponding to the depth X'_c from the pre-etched surface, can be used to find the average conductivity of the etched channel region, and it can also be used to find the gate-to-source breakdown voltage (36, 35, 37, 38, 47).

VII. OXIDE-DEPLETION METHOD (3, 13, 22, 39)

B. E. Deal and E. H. Snow et al. (13) have discussed the effect of oxide depletion of P-type impurities in silicon. It has long been known that impurities redistribute during thermal oxidation of silicon. This phenomenon was studied in detail. Diffusion theory indicated that the impurity-redistribution characteristics should depend on three factors: the segregation coefficient of the impurity at the oxide-silicon interface; the ratio of diffusivities of the impurity in silicon and in the oxide; and the ratio of the oxidation rate constant to the impurity diffusivity in silicon. Four classes of redistribution were proposed, and verified experimentally. Examples are shown in Fig. 8.

Fig. 8a shows the case of dry oxygen oxidation of boron-doped silicon at 1100°C. Here the segregation coefficient of boron leads to incorporation of the boron in the oxide. As a result, boron is depleted at the silicon surface. The concentration of boron in the oxide close to the oxide-silicon interface is about three times that in the silicon surface region. If on the other hand the boron diffuses rapidly through the oxide, due to the addition of hydrogen to the ambient, the depletion at the surface is much greater, as

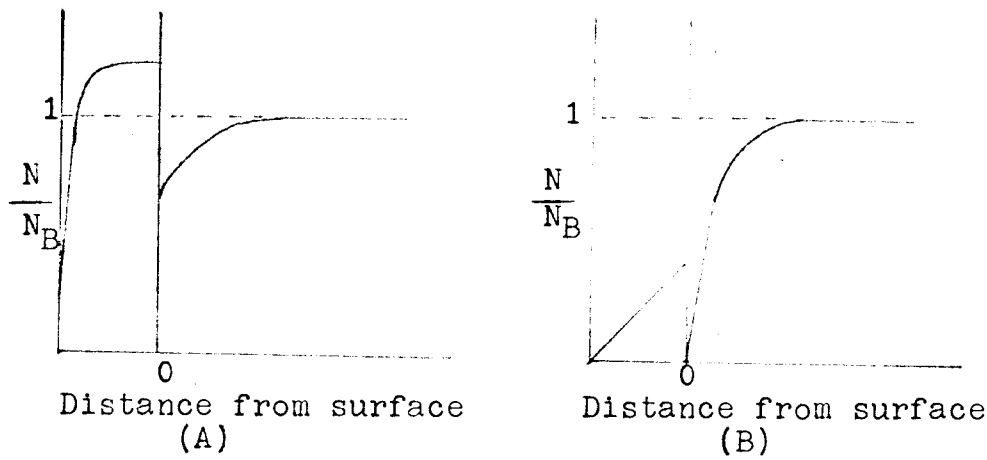


Fig. 8. Different cases of impurity redistribution in silicon due to thermal oxidation.
(A) Diffusion in oxide -- slow (boron)
(B) Diffusion in oxide -- fast (Boron with H_2 ambient).

indicated in Fig. 8b. All p-type impurities deplete at the surface during thermal oxidation of silicon. As oxidation temperature decreases, the redistribution effect increases. Similarly there is a greater effect for wet oxidation than for dry (13).

In application to the fabrication of the compatible field-effect and bipolar transistors, oxide-depletion can be used to decrease the surface concentration of boron at the surface of the channel region. The suggested process was to deposit the channel region of the field-effect transistor and the base region of the bipolar transistor simultaneously. Oxide growth during deposition would be preferable in that, after the deposition cycle, there would be enough oxide grown on both regions such that the oxide left on the base region could be used as a buffer to decrease the rate of growth of new oxide (during diffusion). The oxide in the channel region would be etched away. During diffusion, a steam-hydrogen oxidation atmosphere would be preferable since there is a greater redistribution effect for wet oxidation with hydrogen added to the ambient than for dry oxidation with only oxygen as the oxidizing agent, as discussed by B. E. Deal (13). During this oxidation-diffusion cycle, the boron concentration at the channel region would be reduced by the redistribution effect.

Hence, it would have a shallower junction than the base junction. To obtain variation in the junction depth, both regions could be diffused for t_1 hours after deposition before the oxide in the channel region was removed. After removal of the channel oxide, it could be further diffused in steam-hydrogen for t_2 hours. Thus the junction depth in the base region would be

$$X_b = \left[4D_1(t_1+t_2)\ln(N_{s1}/N)\right]^{1/2}$$

and the junction depth in the channel region would be

$$X_c = \left[4D_1t_1\ln(N_{s1}/N) + 4D_1t_2\ln(N'_{s2}(t_2)/N)\right]^{1/2}$$

where $N_{s2}(t_2)$ would be the relationship describing the impurity concentration at the oxide-depleted surface as a function of time at the diffusion temperature in steam-hydrogen oxidation atmosphere.

VIII. SUPPLEMENTARY EXPERIMENTAL METHODS AND RESULTS

1. Material Preparation (28, 38)

Slices were cut to the (111) crystallographic direction from 1.2 ohm-cm N-type single crystal silicon. One of the surfaces was lapped with 600 grit silicon carbide on a Beuhler polishing machine and then polished to a mirror finish with one micron alumina powder as a final abrasive. They were then degreased in hot acetone and chemically polished in diluted CP5. After soaking in hot sulfuric acid and rinsing in deionized water, each slice was carefully dried in dry nitrogen gas and stored in a dust free chamber. They were further treated with 48% hydrofluoric acid, rinsed in deionized water and dried in dry nitrogen gas before oxidation.

2. Deposition and Diffusion Evaluation

Several wafers previously prepared were cut into chips about 1 cm square and deposited with boron in batches of four chips at 950°C in dry nitrogen (3-1/2 cfh) for 1/2 hour, 1 hour, 1-1/2 hour, and 2 hour intervals. Borosilicate glass which was grown during deposition was removed from each of the chips and they were diffused at 1100°C in wet oxygen for 1 hour, 2 hour, 3 hour, 4 hour,

and 5 hour intervals. Junction depth was measured by 1° angle lapping; junction staining and measurement with calibrated Unitron micrometer under high power microscope as discussed in Appendix A-4.

The results were plotted as shown in Figs. 9-13 (each data point was obtained from the average of two to 12 experimental results). The junction depth varied with the square root of the diffusion time as predicted by the Gaussian distribution, with different slopes corresponding to different surface concentrations (Fig. 9) (Appendix A-2). Initial junction depths were extrapolated and were used to find the initial surface concentration N_{sc} (Figs. 9-10).

It was found that the initial surface concentration N_{sc} corresponding to the boron source concentration during deposition was about (1.27) 10^{20} at/cm^3. The deposition sheet concentration $\overline{Q_{jc}}$ was almost directly proportional to the square root of the time of deposition (Appendix A-2). The sheet concentration $\overline{Q_{jc}}$ for a complementary error distribution diffusion was given in Section V as

$$\overline{Q_{jc}} = 1.13\ N\ D^{1/2} t_1^{1/2}$$

The diffusion constant as calculated from the value of $\overline{Q_{jo}}$ (Figs. 11-12) was approximately (2.54) 10^{-14} cm^2/sec corresponding to 990°C as compared to a theoretical

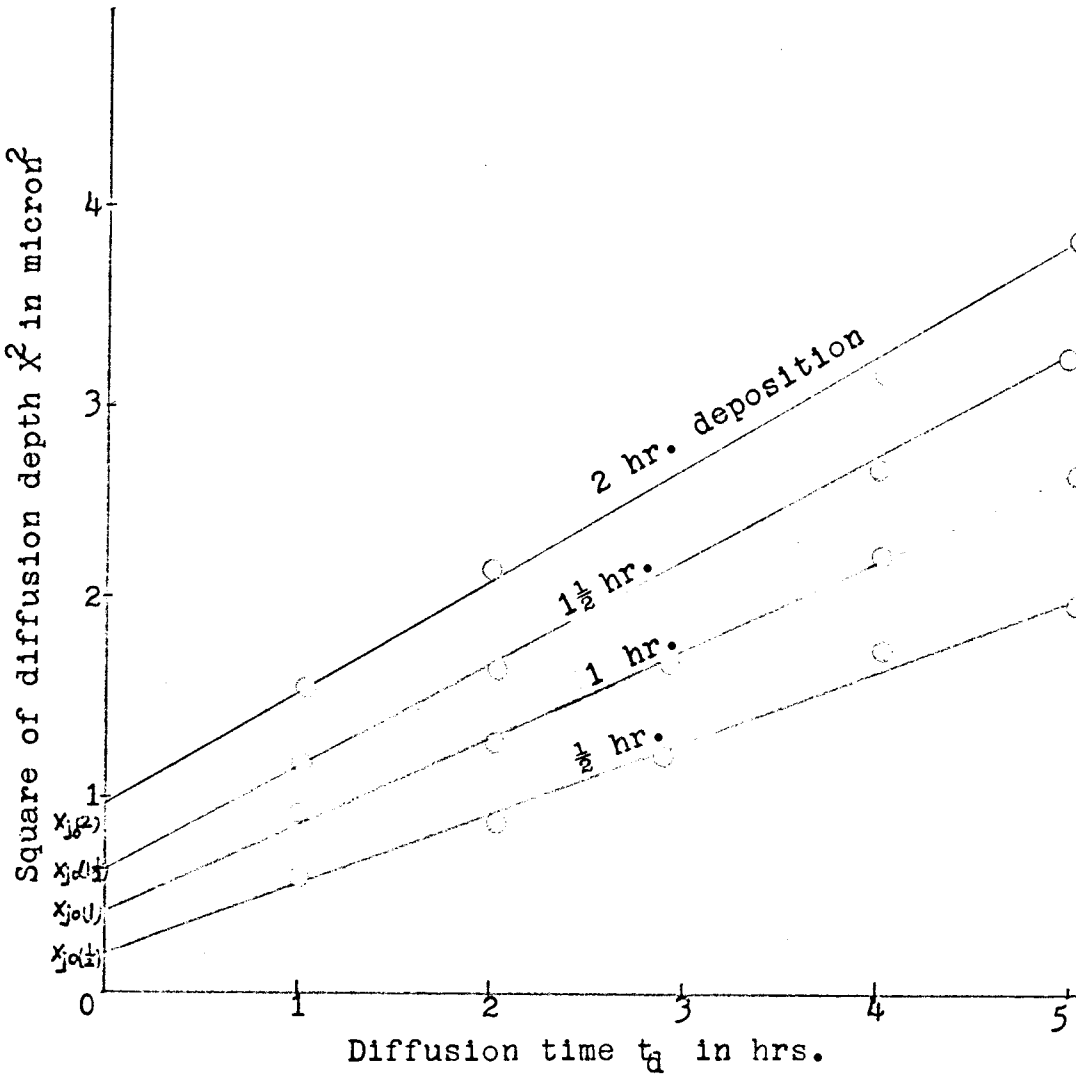


Fig. 9. Diffusion slopes of $\frac{1}{2}$; 1; $1\frac{1}{2}$; 2 hr. depositions @ 1100° C

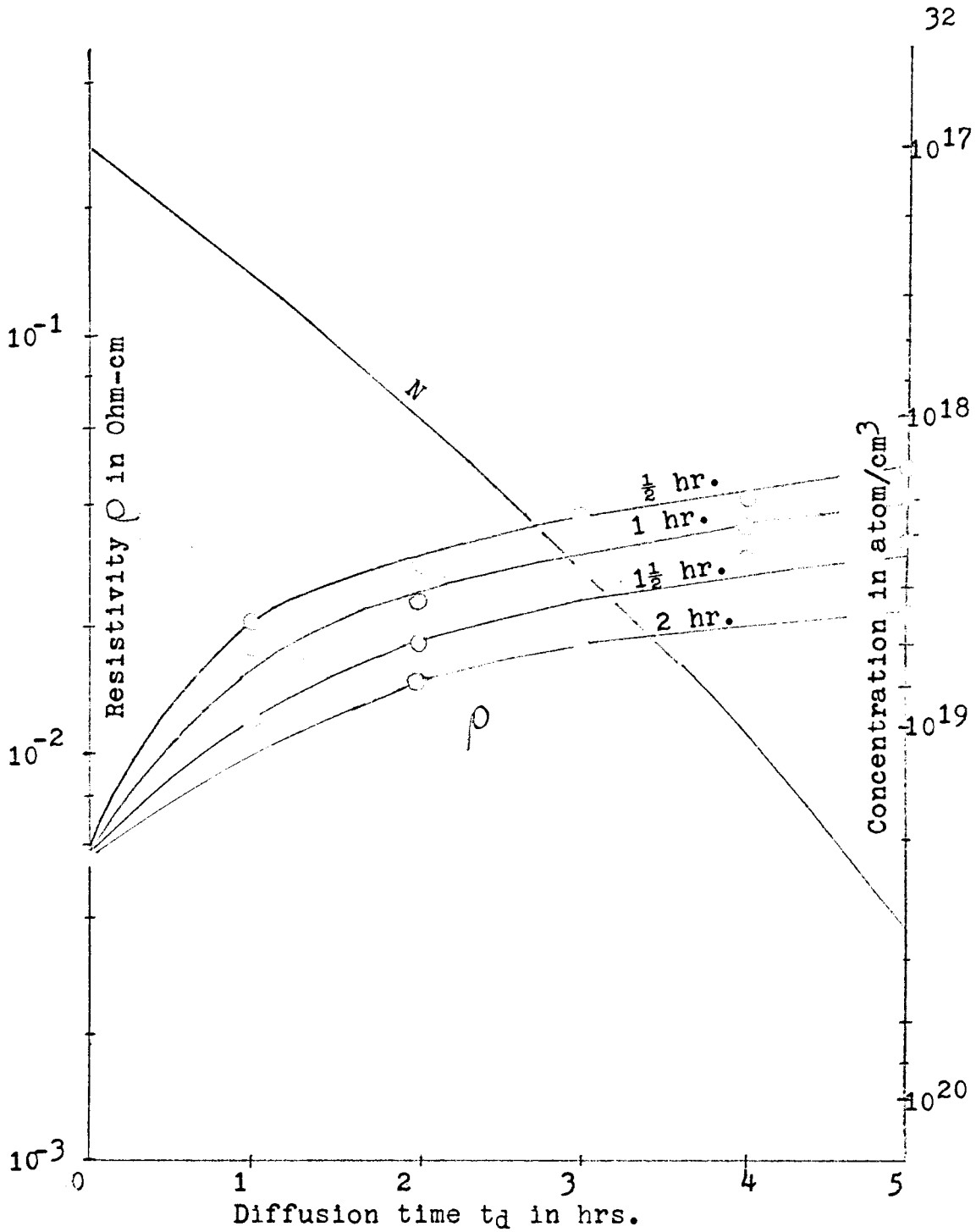


Fig. 10. Diffusion resistivity and average impurity concentration vs diffusion time @1100°C

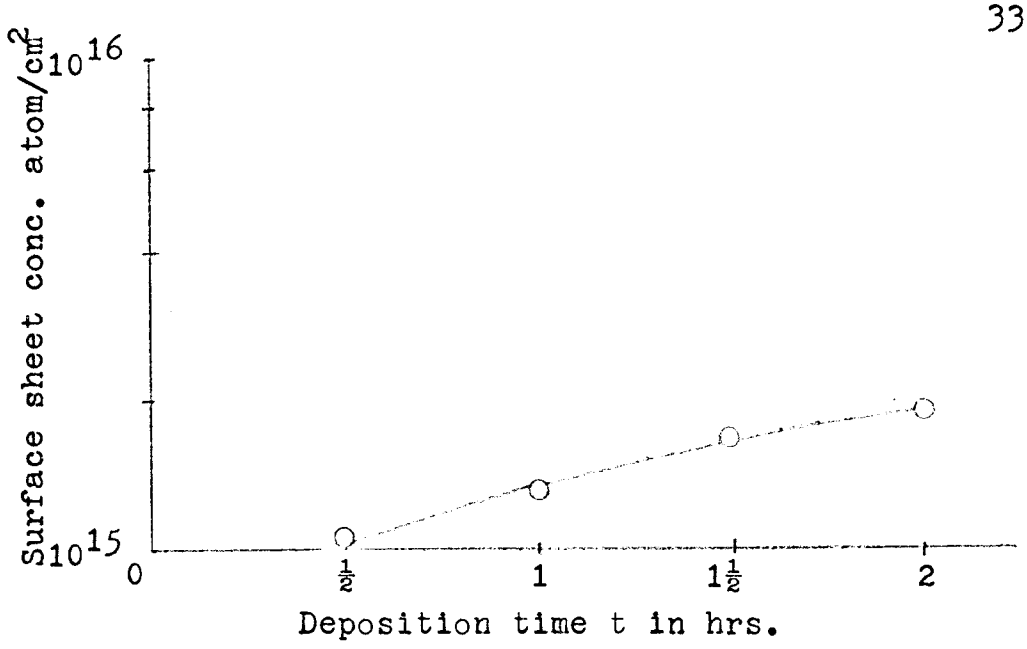


Fig. 11. Surface sheet concentration of deposition.

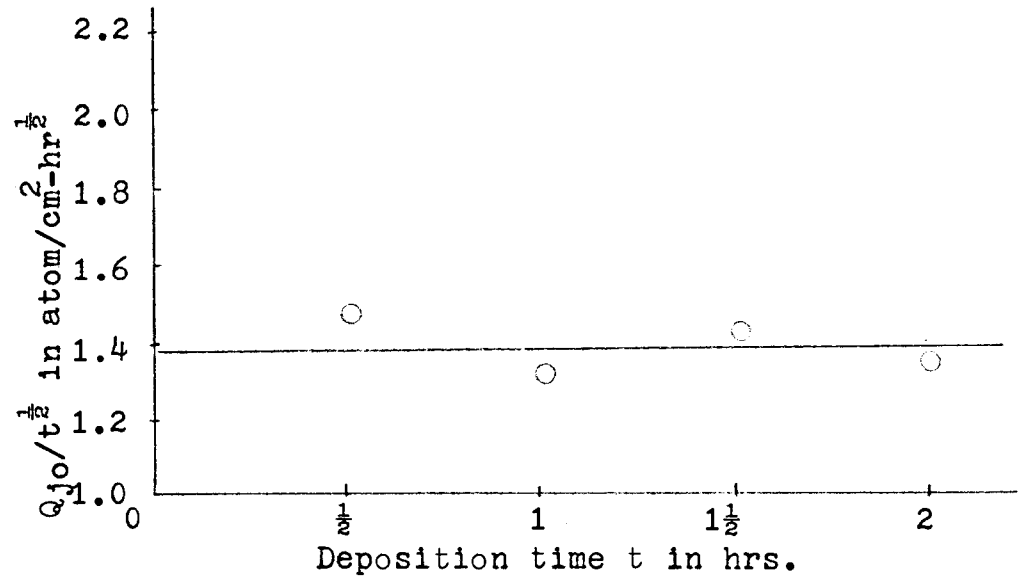


Fig. 12. Average $Q_{jo}/t^{\frac{1}{2}}$ curve.

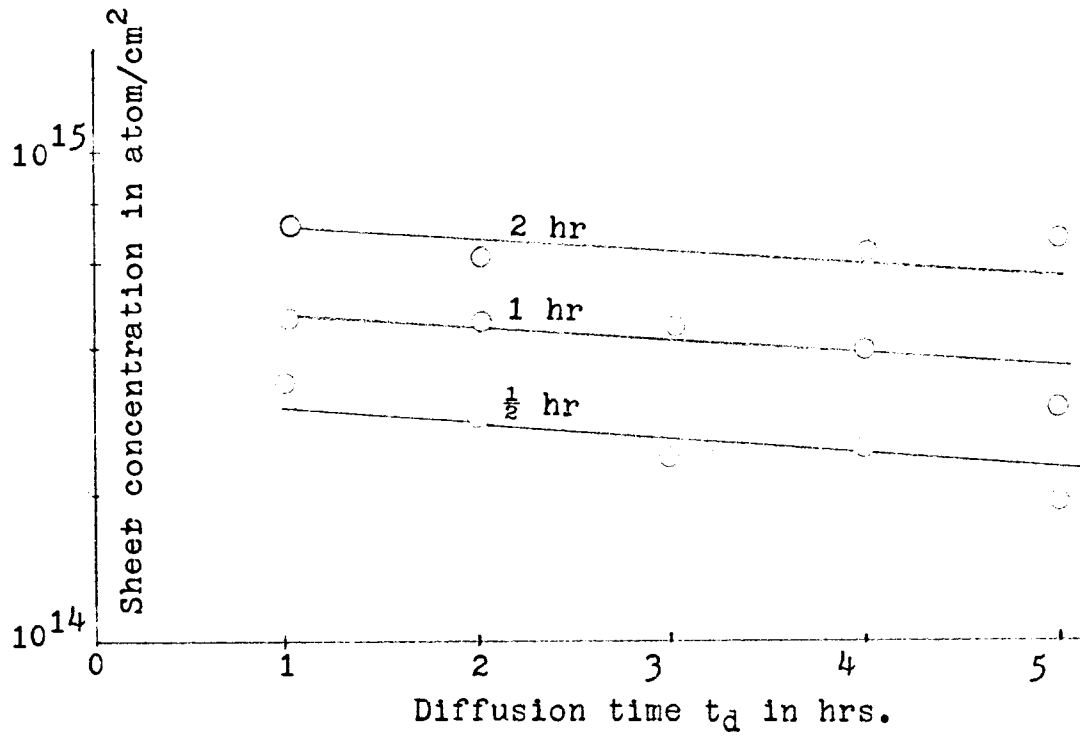
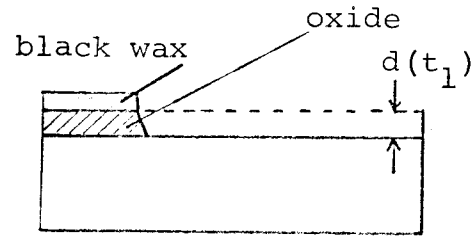


Fig. 13. Sheet concentration $\bar{Q}$ vs diffusion time t_d

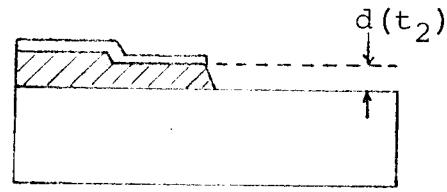
diffusion constant of (11) 10^{-15} cm^2/sec at 950°C (19). This suggested that the experimental boron concentration was lower than the theoretical source concentration of (2.13) 10^{20} at/cm^3 by a factor of 1.68, if the diffusion constant was (9) 10^{-15} cm^2/sec at 950°C.

3. Oxidation

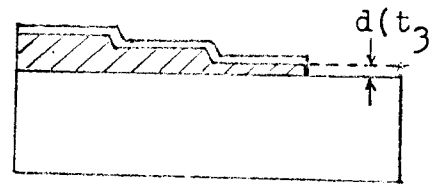
Slices previously prepared were oxidized sequentially by first oxidizing the whole wafer for t_1 minutes, then one-fourth of the wafer was masked with black wax and etched in buffered hydrofluoric acid (Appendix A-6). The black wax was removed and the oxide layer thickness was measured by a two-beam interferometer (7) (Fig. 14). The wafer was again oxidized for t_2 minutes and the second quarter of the wafer, in addition to the first quarter previously masked, was again covered with black wax and etched with buffered hydrofluoric acid. The process was repeated until three-fourths of the wafer was oxidized. The oxide thicknesses thus corresponded to oxidations of 0 min, t_3 min, t_3+t_2 min, $t_3+t_2+t_1$ min. To assure exact oxidation time, in the case of dry oxygen, dry argon gas was introduced into the furnace first until the system reached equilibrium temperature, then the argon gas was switched to oxygen for oxidation. Argon gas was again introduced after oxidation when the



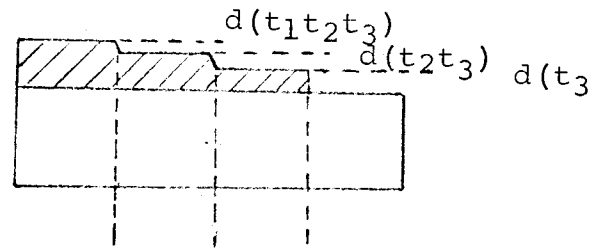
1) 1st quarter being masked and etched



2) 2nd treatment



3) 3rd treatment



4) Final configuration of oxide

Fig. 14. Sequential oxidation.

wafer was cooling down to room temperature.

The oxide thickness curve for dry oxygen at 940°C and 1100°C agreed with the data published by Evitts (15).

4. Partial Masking Evaluation

Several wafers oxidized as discussed in the oxidation section were deposited with boron at 943°C for one and one-half hours in an open-tube diffusion furnace with a flow of 3-1/2 cfh of dry nitrogen gas. After deposition, the borosilicate glass formed on the surface of the wafers in both the masked and unmasked regions was removed by first boiling in deionized water for half an hour and then etched in buffered hydrofluoric acid. They were then rinsed in deionized water and dried in dry nitrogen gas. The surface sheet resistance was measured by the four-point probe technique (48). These boron deposited samples were then diffused for five hours in a separate open tube furnace set at 1100°C with a gas flow of 0.4 cfh of wet oxygen. Both the deposition and the diffusion furnaces were automatically controlled with a Pt-Pt+ 13% Rhodium Thermocouple-controller to within $\pm$ 1°C. The diffused samples were then etched in buffered hydrofluoric acid to remove the oxide layer grown during diffusion. Their sheet resistances and junction depths were measured as done before to find their

average impurity concentration and the corresponding surface concentration. The results were plotted as shown in Figs. 15-16.

It was found that the values for the unmasked region (corresponding to an oxidation time of zero minutes and an oxide thickness of zero angstroms) was approximately the same as the values obtained in the deposition and diffusion experiment (see Section 2). The results in this section were therefore all normalized with respect to the values of one and one-half hours deposition with five hours diffusion as presented in Section 2.

It was also found that the experimental curves approached the predicted (25) total masking oxide thickness of 320 Å asymptotically (see Figs. 15-16).

5. Etching Rate of Silicon

Wafers of N-type 1.2 ohm-cm silicon previously prepared and diffused with boron were used to determine the etching rate of silicon in an etching solution of 20 parts HNO_3 to one part 48% HF to ten parts deionized water. Half of each wafer was masked with black wax and the oxide on the exposed half was etched away with buffered hydrofluoric acid. The wax was removed and the wafers were rinsed in acetone and dried. They were all dried in dry nitrogen gas at room temperature. They were

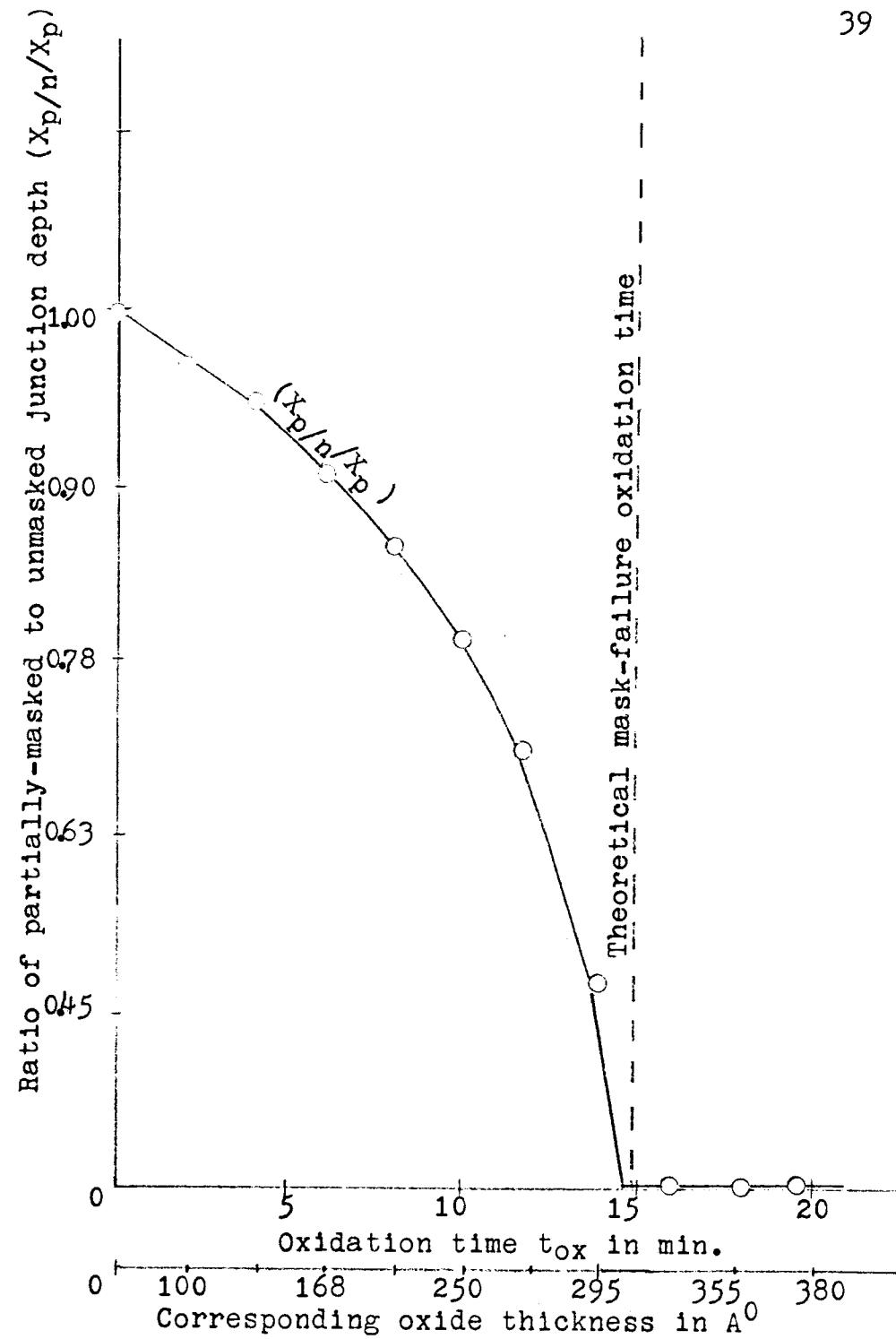


Fig. 15. Ratio of partially-masked to unmasked regions junction depth vs oxidation time and corresponding oxide thickness.

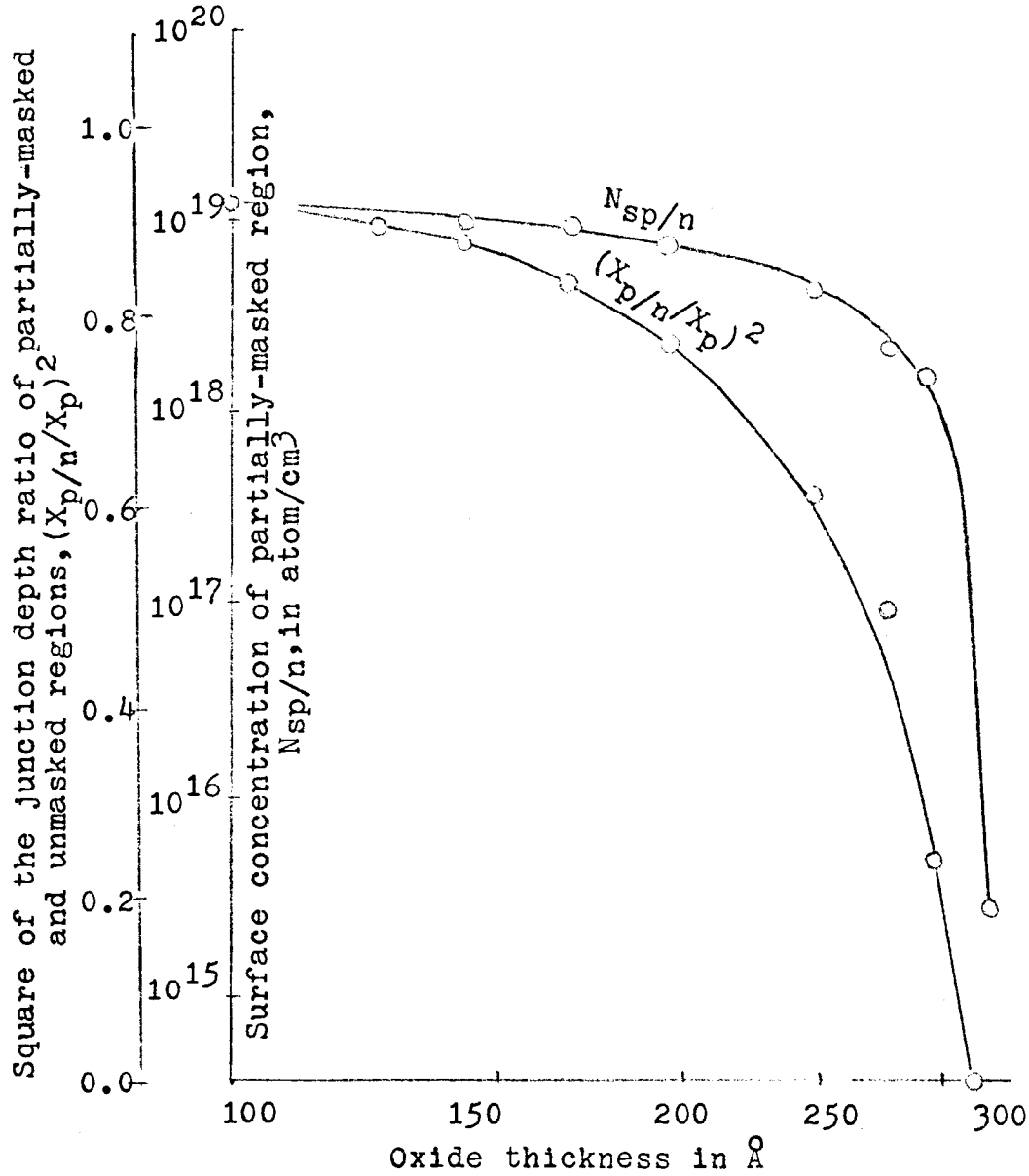


Fig. 16. a) Surface concentration of partially-masked region and b) square of the junction depth ratio of partially-masked and unmasked regions vs oxide thickness.

etched in the silicon-etch at room temperature for several seconds with ultrasonic agitation and rinsed immediately in water. The etched depth was measured with an interference fringe (wedge) method with sodium monochromatic light. The result was plotted as shown in Fig. 17.

It was found that the etching rate was constant and was approximately 0.8 microns/min (at room temperature and with ultrasonic agitation).

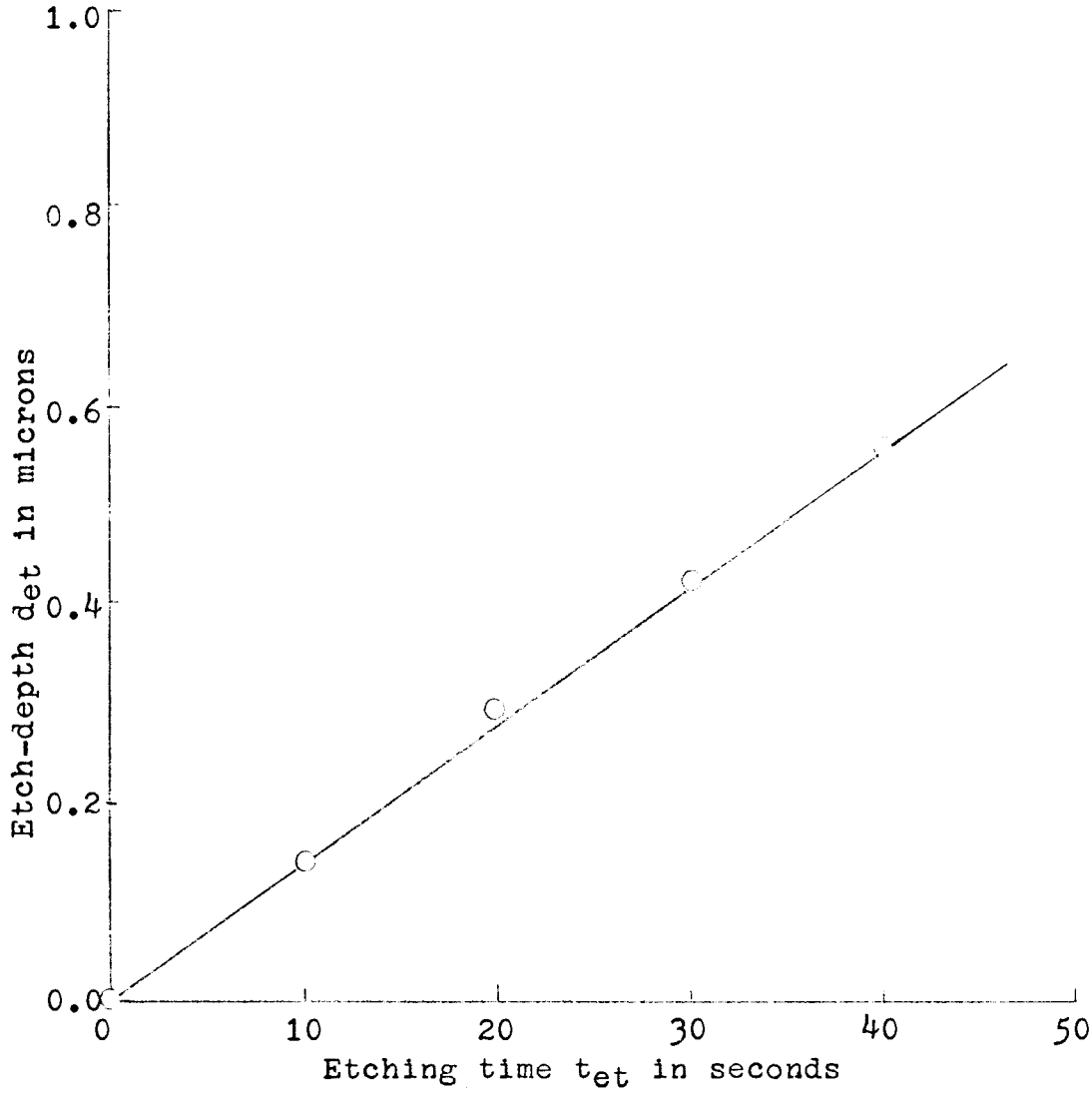


Fig. 17. Etching rate of silicon in 20 HNO_3:1 HF:10 H_2O

IX. EXPERIMENTAL FIELD-EFFECT TRANSISTOR FABRICATION METHODS AND RESULTS

1. Partial Masking Process

Wafers of 1.2 ohm-cm N-type single crystal silicon previously prepared were oxidized at 1100°C in air for 12 hours to obtain an oxide layer of 0.7 to 1 micron thickness. Base holes and channel holes were etched in buffered hydrofluoric acid using positive photoresist as a mask. A thin oxide layer was grown thermally on both regions in dry oxygen at 950°C for eight minutes. The oxide on the source-drain and the base regions of the transistors were etched away using a source-drain mask photo-resist step. Boron from a source of 40% B_2O_3 + 60% SiO_2 was deposited on the wafer at 950°C in dry nitrogen for one and one-half hours. After removing the borosilicate glass and five hours of diffusion, a junction depth ratio ($X_{p/n}$ / X_p) of 0.88 was obtained, with a base junction depth of 1.2 microns and a base region sheet resistance of 198 ohm/sq.

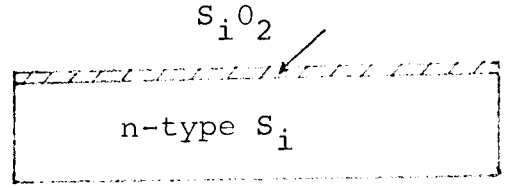
An emitter mask was used to etch the emitter and gate 1 holes in the oxide of the transistors which had grown during the boron diffusion. P_2N_5 was used as the phosphorus source in the emitter and the gate 1 regions deposition. The phosphorus deposition was 30 minutes at

950°C in dry nitrogen. The diffusion was 15 minutes at 1100°C in steam. The junction depth resulting from this N-type diffusion was 0.96 microns with a sheet resistance of 13.5 ohms/sq.

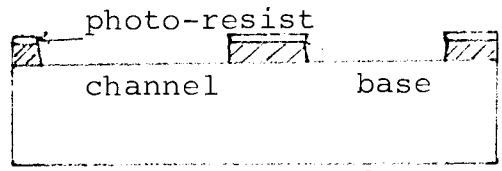
Contact holes were etched in the various regions and aluminum was vacuum evaporated on the surface. The metallization pattern was etched with a metallization mask photo-resist step in a solution of 80 parts H_3PO_4 to 16 parts water to five parts HNO_3 at 80°C. The aluminum left on the surface was alloyed into the silicon at 576°C in dry Argon gas to obtain ohmic contacts to the different regions.

The finished field-effect transistors were tested on a Model 1600 KGS100 Micromanipulator with a type 575 Tektronix Transistor Curve Tracer. Then several typical field-effect transistor samples were angle lapped, stained, and the junctions were measured by interference technique (Figs. 21-28).

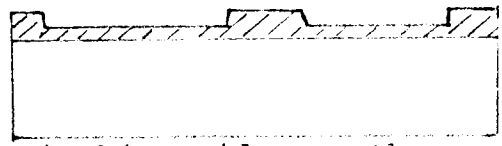
It was found that the average transconductance of the field-effect transistor obtained by this partial masking method was 350 micro-mhos with a breakdown voltage of 6.5 volts and a pinch-off voltage of 1.3 volts. The different junction depths and their impurity concentration obtained from resistivity measurements were given as shown in Tables I and II. Table III gives the steps involved in this process.



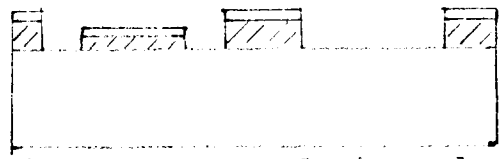
1) Thick oxide growth



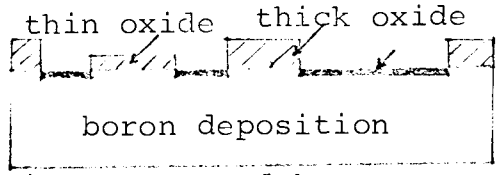
2) Etch channel and base oxide



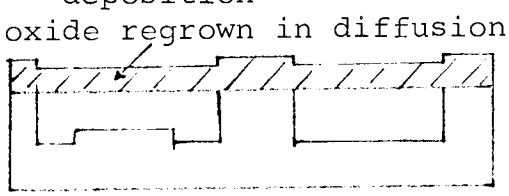
3) Thin oxide growth



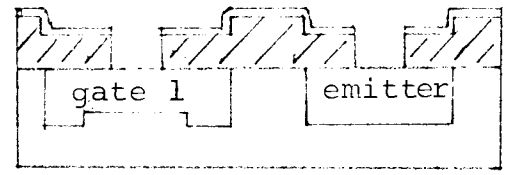
4) Etch source-drain and base oxide



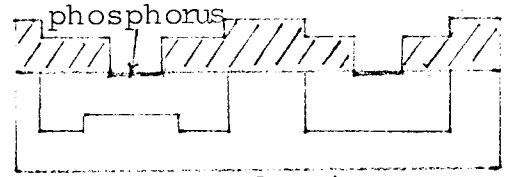
5) Channel and base deposition



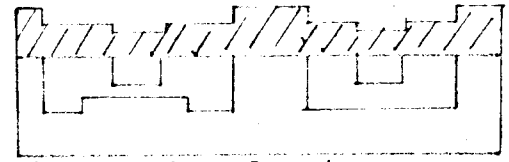
6) Channel and base diffusion



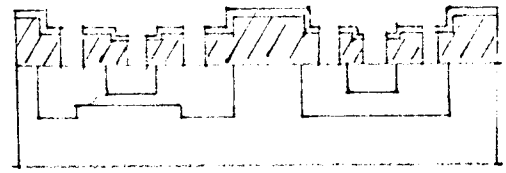
7) Etch gate 1 and emitter oxide



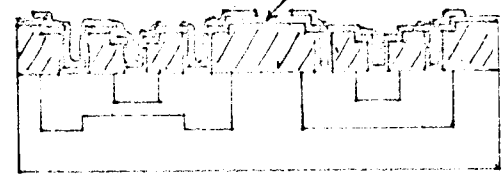
8) Gate 1 and emitter deposition



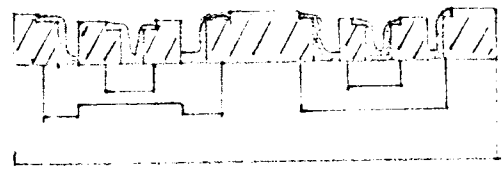
9) Gate 1 and emitter diffusion



10) Etch contact holes oxide aluminum



11) Metallization and aluminum etch



12) Alloy in

Fig. 18. Partial-masking method.

Table I. Field-effect and Bipolar Transistor Parameters (Partial-masking).

Parameters	Symbol	Unit	Experiment	Theo-retical
Transconductance @ Vg=0	G_o	micromho	320	369
Pinch-off current @ Vg=0	I_p	ma	0.205	0.259
Pinch-off voltage @ Vg=0	V_p	volts	1.30	2.01
Gate breakdown voltage	V_{Br}	volts	6.5	4.0
Channel resistance	R_c	ohms	3.3K	
Gate-1 or emitter depth	X_{g1}, X_e	micron	0.96	
Channel thickness	X_c	micron	0.096	
Channel depth	X'_c	micron	1.05	
Channel depth (pushing)	X'_c	micron	1.05	
S-D or Base depth	X_{SD}, X_b	micron	1.20	
Base sheet resistance	$\overline{R_{SD}}, \overline{R_{bs}}$	ohm/sq	198	
Channel sheet resistance	$\overline{R_{cs}}$	ohm/sq	252	
S-D sheet resistance	$\overline{R_{ss}}$	ohm/sq	198	
Gate 1 or emitter sheet resistance	$\overline{R_{gls}}, \overline{R_{es}}$	ohm/sq	13.5	

Table II. Field-effect and Bipolar Transistor Parameters (Partial-masking).

Parameters	Symbol	Unit	Values
Average base concentration	$\bar{N}_b$	at/cm^3	$(4)\cdot(10^{18})$
Average channel concentration @ $\frac{X}{X_c} = 0.909$	$\bar{N}_c$	at/cm^3	$(3.9)(10^{15})$
Average channel concentration ($\bar{R}_c$)	$\bar{N}_c'$	at/cm^3	$(8.6)(10^{16})$
Channel surface concentration	N_{cs}	at/cm^3	$(1.11)(10^{19})$
Average S-D concentration	$\bar{N}_{SD}$	at/cm^3	$(3.3)(10^{18})$
Average gate or emitter concentration	$\bar{N}_e$	at/cm^3	$(6.0)(10^{19})$
Channel surface concentration @ $V_{Br} = 6.5$ volts	N_{cs}	at/cm^3	$(4.6)(10^{17})$

Table III. Steps Involved in Partial-masking Process

1.	Material preparation	
2.	Thick oxide growth	Air at 1100°C 12 hr.
3.	Channel and base oxide mask photo-resist etching	Mask no. 2 base
4.	Thin oxide growth	950°C dry O_2, 8 min.
5.	S-D and base oxide mask photo-resist etching	Mask no. 1 S-D
6.	Channel and base deposition	950°C boron 3-1/2Cfh N_2, 1-1/2 hr.
7.	Channel and base diffusion	1100°C wet O_2, 5 hr.
8.	Gate 1 and emitter oxide mask photo-resist etching	Mask no. 3, emitter
9.	Gate 1 and emitter deposition	950°C P_2N_5, 3-1/2Cfh N_2, 30 min.
10.	Gate 1 and emitter diffusion	1100°C steam and O_2, 25 min.
11.	Contact holes oxide mask photo-resist etching	Mask no. 4 contact
12.	Aluminum metallization	150°C vacuum
13.	Metallization pattern mask photo-resist etching	Mask no. 5. Met.
14.	Ohmic contact alloying	575°C dry argon, 5 min.

2. Two-deposition Process

The silicon wafers were prepared as before. A thick oxide was again thermally grown on the surfaces. In this case, the source-drain holes of the field-effect transistors were first etched out and deposited with boron at 950°C in dry nitrogen at a flow rate of 3-1/2 cfh. before the bases of the bipolar transistors were deposited with boron. The borosilicate glass was removed as before. Then a base-hole mask was used to remove the oxide covering the channel region and the base region of the transistors (see Fig. 19). A second deposition was made and the borosilicate glass was again removed. The wafers were then diffused as was done in the partial-masking method at 1100°C in wet oxygen. Gate 1 and emitter regions were diffused in as before. Metallization and alloying were treated in the same way as described in Section IX-1. The results are shown in Figs. 22, 23, 27 and Tables IV and V. Table VI shows the steps involved in this process.

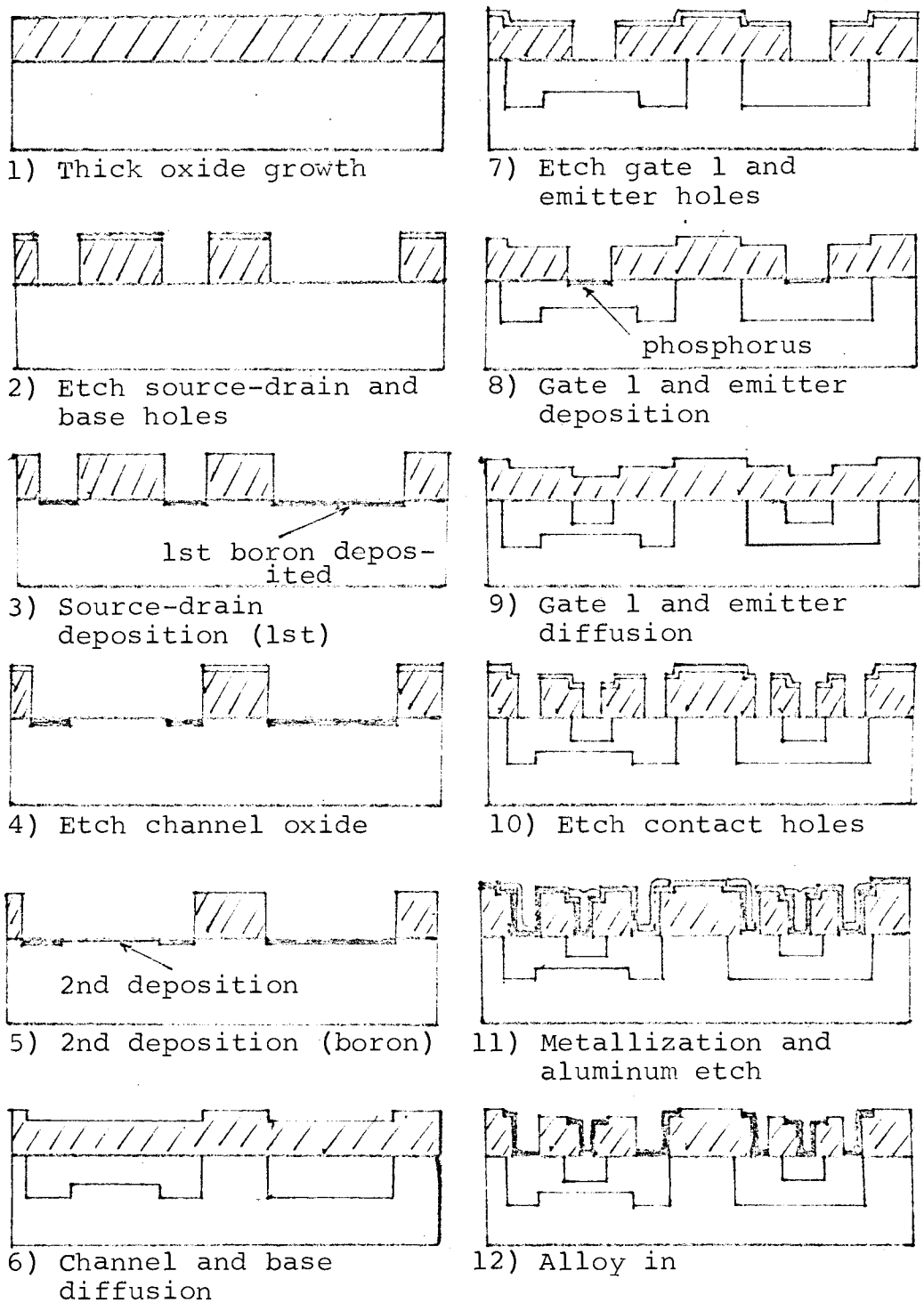


Fig. 19. Two-deposition method.

Table IV. Field-effect and Bipolar Transistor Parameters (Two-deposition).

Symbol	Unit	Exp.	Theor.
G_o	micro mho	275	215.5 @ $V_g = 0$
I_p	m.a.	0.09	0.0571 @ $V_g = 0$
V_p	volt.	1.10	0.796 @ $V_g = 0$
V_{Br}	volt.	6	4.2
R_c	ohm	5K	
X_{g_1}, X_e	micron	1.36	
X_c	micron	0.11	
X'_c	micron	1.62	
X'_c	micron	1.52	
X_{SD}, X_b	micron	1.60	
$\bar{R}_{bs}$	ohm/sq	205	
$\bar{R}_{cs}$	ohm/sq	300	
$\bar{R}_{ss}$	ohm/sq	205	
$\bar{R}_{g_1 s}, R_{es}$	ohm/sq	9.45	

Table V. Field-effect and Bipolar Transistor Parameters (Two-deposition).

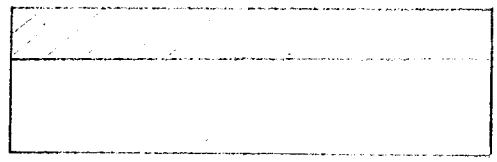
Symbol	Unit	
$\bar{N}_b$	at/cm^3	$(2.55)(10^{18})$
$\bar{N}_c$	"	$(3.07)(10^{15})$ @ $\frac{X}{X_c} = 0.922$
$\bar{N}'_c$	"	$(3.50)(10^{16})$
N_{cs}	"	$(5.60)(10^{18})$ @ X = 0
$\bar{N}_{SD}$	"	$(2.55)(10^{18})$
$\bar{N}_e$	"	$(7.00)(10^{19})$
N_{cs}	"	$(6.00)(10^{17})$ @ V_{Br} = 6 volt.

Table VI. Steps Involved in Two-deposition Process.

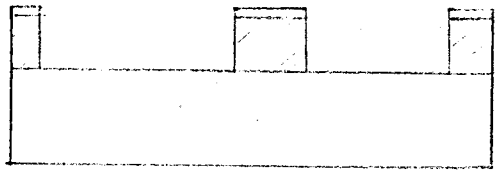
1.	Material preparation	
2.	Thick oxide growth	Air at 1100.C 12 hr.
3.	S-D and base mask photo-resist etching	Mask no. 1 S-D
4.	First deposition of S-D and Base	950°C boron, 3-1/2Cfh N_2, 1/2 hr.
5.	Channel and base oxide mask photo-resist etching	Mask no. 2 base
6.	Second deposition of channel and base	950°C boron, 3-1/2Cfh N_2, 1/2 hr.
7.	Diffusion of channel and base	1100°C wet O_2, 4 hr.
8.	Gate 1 and emitter oxide mask photo-resist etching	Mask no. 3 emitter
9.	Gate 1 and emitter deposition	950°C,P_2N_5, 3-1/2Cfh N_2, 35 min.
10.	Gate 1 and emitter diffusion	1100°C, steam and O_2, 25 min.
11.	Contact holes oxide mask photo-resist etching	Mask no. 4, contact
12.	Aluminum metallization	150°C, vacuum
13.	Metallization pattern mask photo-resist etching	Mask no. 5, Met.
14.	Ohmic contact alloying	575°C, dry argon, 5 min.

3. Etched-Channel Process

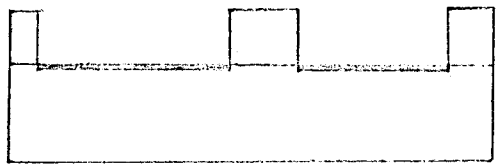
A thick oxide was again grown on the surface of the wafer. The base region and the channel region oxide was etched away by photo-resist masking. A one-hour deposition of boron was applied to the wafers, and they were diffused for three hours after removal of the borosilicate glass. A channel region mask was used to cut the oxide hole instead of the source-drain mask as in the partial-masking method. A silicon etchant of 20 parts HNO_3 to one part 48% hydrofluoric acid to ten parts of water was used to etch a dip in the channel region. The wafers were then diffused again for one more hour in steam to make the total diffusion time four hours. Steam was used to grow a thick oxide on the base region in a shorter time. Again the gate 1 and emitter regions and metal contacts were added, and the field-effect transistors were metallized and tested as before. The results obtained are shown in Figs. 24, 25, 28 and Tables VII and VIII. Steps involved in this process are given in Table IX.



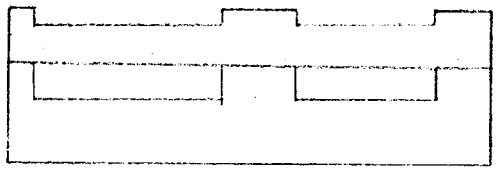
1) Thick oxide growth



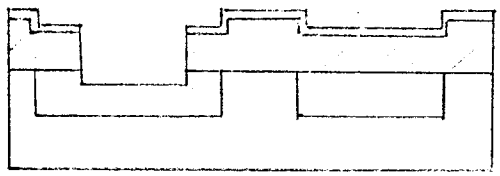
2) Etch channel and base holes



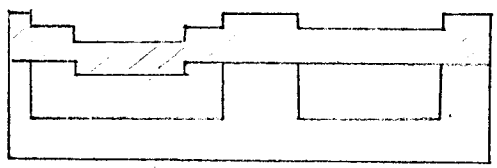
3) Channel and base deposition



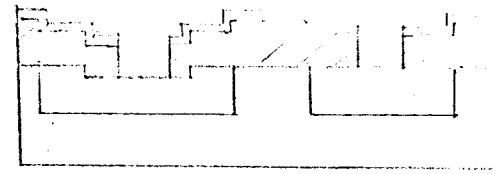
4) 1st channel and base diffusion



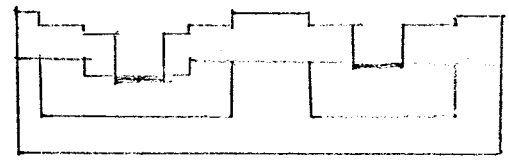
5) Etch channel silicon



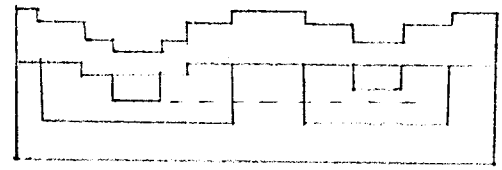
6) 2nd channel and base diffusion



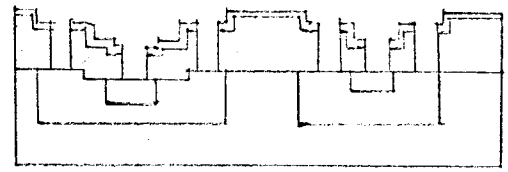
7) Etch gate-1 and emitter holes



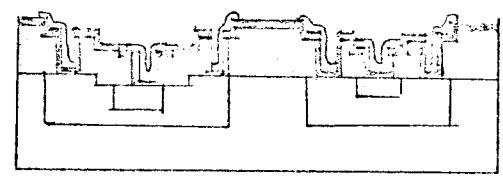
8) Gate-1 and emitter deposition



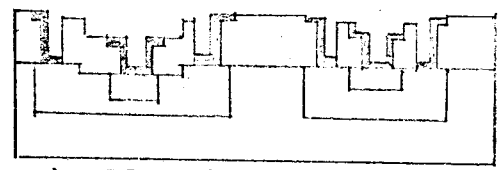
9) Gate-1 and emitter diffusion



10) Etch contact holes



11) Metallization and aluminum etch



12) Alloy in

Fig. 20. Etched-channel method.

Table VII. Field-effect and Bipolar Transistor Parameter (Etched-channel).

Symbol	Unit	Exp.	Theor.	
G_o	micro mho	400	385	@ $V_g = 0$
I_p	m.a.	0.72	0.776	@ $V_g = 0$
V_p	volt.	2.20	2.02	@ $V_g = 0$
V_{Br}	volt.	6.5	4.2	
R_c	ohm	2.97k		
X_{g_1}, X_e	micron	1.48		
X_c	micron	0.16		
X'_c	micron	1.48		
X'_c	micron	1.48		
X_{SD}, X_b	micron	1.19		
$\bar{R}_{bs}$	ohm/sq	205		
$\bar{R}_{cs}$	ohm/sq	305		
$\bar{R}_{ss}$	ohm/sq	205		
$\bar{R}_{g_1 s}, \bar{R}_{es}$	ohm/sq	9.46		

Table VIII. Field-effect and Bipolar Transistor Parameter (Etched-channel).

Symbol	Unit		
$\bar{N}_b$	at/cm^3	$(2.3)(10^{18})$	
$\bar{N}_c$	"	$(6.16)(10^{15})$	@ $\frac{X}{X_c} = 0.882$
$\bar{N}'_c$	"	$(4.3)(10^{16})$	
N_{cs}	"	$(6.55)(10^{18})$	@ X = 0
$\bar{N}_{SD}$	"	$(2.3)(10^{18})$	
$\bar{N}_e$	"	$(7)(10^{19})$	
N_{cs}	"	$(4.6)(10^{17})$	@ V_{Br} = 6.5 volt.

Table IX. Steps Involved in Etched-channel Process.

1.	Material preparation	
2.	Thick oxide growth	Air at 1100°C, 12 hr.
3.	Channel and base oxide mask photo-resist etching	Mask no. 2 base
4.	Channel and base deposition	950°C, boron, 3-1/2Cfh N_2, 1 hr.
5.	First channel and base diffusion	1100°C, wet O_2, 3-1/2 hr.
6.	Channel oxide mask photo-resist etching	Mask no. 6, channel
7.	Channel silicon etch	Silicon-etch, Rm. temp. 20 sec.
8.	Second channel and base diffusion	1100°C, steam and O_2, 1/2 hr.
9.	Gate 1 and emitter oxide mask photo-resist etching	Mask no. 3, emitter
10.	Gate 1 and emitter deposition	950°C, P_2N_5, 3-1/2Cfh N_2, 35 min.
11.	Gate 1 and emitter diffusion	1100°C, steam O_2, 27 min.
12.	Contact holes oxide mask photo-resist etching	Mask no. 4, contact
13.	Aluminum metallization	150°C, vacuum
14.	Metallization pattern mask photo-resist etching	Mask no. 5, Met.
15.	Ohmic contact alloying	575°C, dry argon, 5 min.

4. Resistivity Measurement

The resistivity of the different regions in all three processes were measured by the four-point probe techniques on test wafers which were sequentially masked such that each diffusion covered only half of the region formerly diffused.

X. COMPARISON OF THE FIELD-EFFECT TRANSISTOR PARAMETERS OF THE TRANSISTORS OBTAINED FROM THE THREE PROCESSES

The results obtained were comparable in all three processes, as shown in Table X. The range of transconductance G_o varied from 275 to 400 micro-mhos. The average transconductance G_o was about 300 micro-mhos for all three processes.

The efficiency E of the two-deposition process was the highest in this particular case, as was predicted by its smallest channel thickness X_c (0.11 micron) as compared to the other two (according to equation 6 in Section III, page 8). The mobility was estimated with the relationship as given from equation 6 (based on G_o, V_p, and X_c obtained experimentally), and was found to be around 330 cm^2/sec. This value of mobility agreed very well with the value obtained from the channel doping level based on R_c and X_c (see Appendix A-6 and Table X) (1, 9, 43).

The values of $\bar{N}_c$ and N_{cs} obtained from using the resistivity measurements and the method introduced by Irvin (26) differed from the values obtained from calculations using the channel resistance, channel thickness, and breakdown voltage by a factor of about 10. This difference may be because of impurity redistribution

during the gate 1 diffusion when some boron was pushed out of the diffusing gate 1 region into the channel, such that the resulting channel thickness and effective channel doping level was much higher than should be obtained during a normal single junction diffusion. Such an impurity-redistribution effect can be seen as a bulging out at the channel region in the vicinity of the gate 1 region as shown in the pictures in all three cases.

The concentration as obtained from R_c and X_c was in good agreement with the open channel transconductance, pinch off voltage, pinch-off current, and the mobility in all three cases (see Table X).

Table X. Comparison of Field-effect and Bipolar Transistor Parameters Obtained by Three Methods.

Symbol	Unit	P-M	Two-Dep.	Et.-Ch.
G_o	micro-mho	320	275	400 @ V_g=0
I_p	m.a.	0.205	0.09	0.72 @ V_g=0
V_p	volt.	1.3	1.1	2.2 @ V_g=0
V_{Br}	volt.	6.5	6.0	6.5 @ V_g=0
R_c	ohm	3.3k	5k	2.97k
X_{g_1},X_e	micron	0.96	1.36	1.32
X_c	micron	0.096	0.11	0.16
X'_c	micron	1.056	1.42	1.48
X'_c	micron	1.056	1.52	1.48 pushing effect
X_{SD},X_b	micron	1.20	1.60	1.48
$\bar{R}_{bs}$	ohm/sq	198	205	205
$\bar{R}_{cs}$	ohm/sq	252	300	305
$\bar{R}_{ss}$	ohm/sq	200	205	205
$\bar{R}_{g_1s}$,$\bar{R}_{es}$	ohm/sq	13.5	9.45	9.46
$\bar{N}_b$	at/cm^3	$(4)10^{18}$	$(2.55)10^{18}$	$(2.3)10^{18}$
$\bar{N}_o$	at/cm^3	$(3.9)10^{15}$	$(3.07)10^{15}$	$(6.16)10^{15}$
$\bar{N}'_c$	at/cm^3	$(8.6)10^{16}$	$(3.5)10^{16}$	$(4.3)10^{16}$ base on R_c,X_c
N_{cs}	at/cm^3	$(1.1)10^{19}$	$(5.6)10^{18}$	$(6.5)10^{18}$
$\bar{N}_{SD}$	at/cm^3	$(3.3)10^{18}$	$(1.7)10^{18}$	$(2.3)10^{18}$
$\bar{N}_e$	at/cm^3	$(6)10^{19}$	$(7)10^{19}$	$(7)10^{19}$
N_{cs}	at/cm^3	$(4.6)10^{17}$	$(6.00)10^{17}$	$(4.6)10^{17}$ base on V_{Br}
$\bar{N}_{g_2}$	at/cm^3	$(4.5)10^{15}$	$(4.5)10^{15}$	$(4.5)10^{15}$
E	10^{-6}/ohm-V	246	250	182
(E)(X_c)	cm/ohm-V	$(2.36)10^{-9}$	$(2.75)10^{-9}$	$(2.91)10^{-9}$
μ_p	cm^2/V-sec	278	323	342
μ_p	cm^2/V-sec	280	350	350 base on $\bar{N}'_c$

XI. COMPARISON OF THE THREE PROCESSES

As is shown in Table XI, both the partial-masking and the two-deposition processes involved 14 steps as compared to 15 steps in the etched-channel process. There was a total of five photo-resist mask-etching steps in all the three processes. A common set of photo-resist masks was used for the partial-masking and the two-deposition processes. In the case of the etched-channel process, a channel mask was used instead of the source-drain mask as was used in the other two processes. The first two methods produced field-effect transistors of the same geometry and similar doping levels when the junction depths were the same. In the etched-channel method, the bump in the gate 2 region was replaced by a dip on the surface of the channel. The gate 2 region in the etched-channel case was displaced (downward) by the distance of the dip on the channel surface (Fig. 25).

In comparing the difficulties in obtaining reproducible results, the two-deposition process excels the others in reproducibility because it does not involve any precise thin oxide growth or any etching-depth. Its deposition and diffusion processes can easily be reproduced, and are very straightforward.

In the partial-masking process, difficulties arose mainly from the problem of obtaining a uniform thin

Table XI. Collective Comparison of the Three Processes.

	Process required	P-M	Two-D	Et-Ch
1.	Material preparation	x	x	x
2.	Thick oxide growth	x	x	x
3.	Channel and base oxide mask photo-resist etching	x		x
4.	Thin oxide growth	x		
5.	S-D and base oxide mask photo-resist etching	x	x	
6.	First deposition of S-D and base		x	
7.	Channel and base oxide mask photo-resist etching		x	
8.	Second deposition of channel and base		x	
9.	Channel and base deposition	x		x
10.	First channel and base diffusion			x
11.	Channel and base oxide mask photo-resist etching			x
12.	Channel silicon etch			x
13.	Second channel and base diffusion			x
14.	Channel and base diffusion	x	x	
15.	Gate 1 and emitter oxide mask photo-resist etching	x	x	x
16.	Gate 1 and emitter deposition	x	x	x
17.	Gate 1 and emitter diffusion	x	x	x
18.	Contact holes oxide mask photo-resist etching	x	x	x
19.	Aluminum metallization	x	x	x
20.	Metallization pattern mask photo-resist etching	x	x	x
21.	Ohmic contact alloying	x	x	x
	Total number of steps involved	14	14	15

oxide in the absence of pin holes. Pin holes occurred wherever the surface was contaminated. Thus, surface cleanliness is very important in this process. In growing a thin oxide with dry oxygen gas, the period that the samples were in the furnace was very short (eight minutes). Any variation in the furnace temperature or the moisture content of the dry oxygen gas was reflected in the thickness of the oxide and therefore contributed to irreproducibility.

In the etched-channel process, the temperature and concentration of the silicon-etch solution was very important. Variation in temperature and variation in the amount of silicon being etched each time would cause variation in the resulting etched-channel depth unless it was compensated by the time for which the samples were etched. Therefore it would be advisable to change the etching solution often. Agitation during etching silicon prevented a uniform etching rate on the surface of the sample. It was found that the surface was rough after etching in hand-stirred agitation. The resulting junction profile after the emitter diffusion was not flat because the diffusion junction followed the profile of the surface. When ultrasonic agitation was applied, the resulting junction was reasonably smooth and flat.

XII. CONCLUSION

It was shown in this thesis that it was possible to obtain a compatible field-effect transistor and a bipolar transistor by the partial oxide masking method, the two-deposition method, and the etched-channel method. The flexibility and simplicity of these three methods were also demonstrated. A fourth method, the oxide-depletion process, was suggested but had not been studied experimentally. Capabilities of the above methods were not limited, however, to the fabrication of the compatible field-effect and bipolar transistors alone. Any circuit which required a variable junction depth alongside a fixed junction depth can be adapted with any of these three methods.

The best method was the two-deposition process. Its procedures were straightforward. Its deposition surface concentration could be well controlled. Its channel thickness and its channel resistivity was independent of the base. Its reproducibility was the best.

The reproducibility of the other two methods was good, although the growth of thin oxide in the partial-masking method was tricky; and the etching process in the etched-channel method had to be done with care. When the oxidation process of the thin oxide growth was under control, and when the samples were prevented from

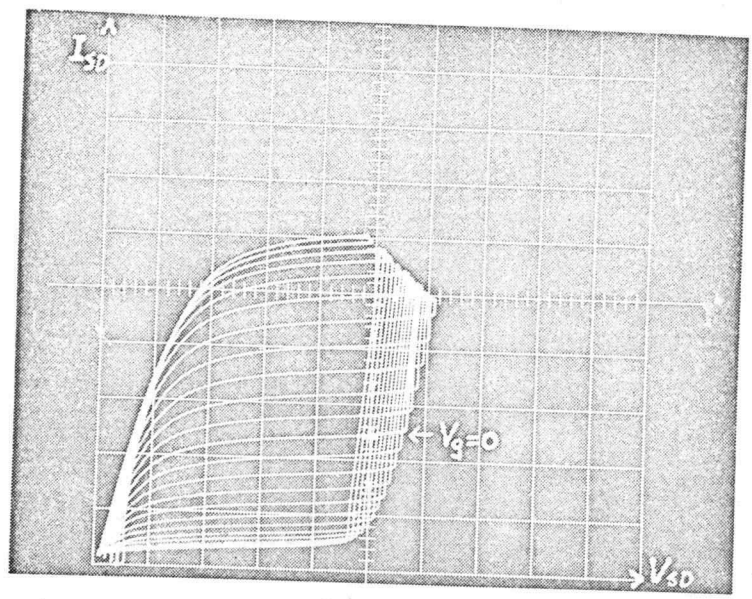
contamination by handling with great care, the yield of the partial-masking method was increased. Cleanliness and care in wafer handling was essential to all the processes described in this thesis. In the case of the etched-channel method, control on the strength of the etching solution, temperature, and agitation were the main factors affecting the reproducibility.

The field-effect transistors fabricated from all three methods in this investigation had similar characteristics. The impurity (boron) concentration at the source-drain region as measured from its resistivity was $(2.3)10^{18}$ to $(4.0)10^{18}$ at/cm^3. At the channel region, the impurity concentration (boron), as estimated from the channel resistance and its channel thickness, ranged from $(2.5)10^{16}$ to $(3.5)10^{16}$ at/cm^3, with the channel thickness ranging from 0.10 to 0.16 microns. The gate 1 impurity level (phosphorus) was about $(7)10^{19}$ at/cm^3, while the gate 2 region had an impurity level of $(4.5)10^{15}$ at/cm^3. The transconductance, pinch-off current and pinch-off voltage agreed very well with the theoretical calculations based on the channel resistance values measured experimentally. These values were used to estimate the hole-mobility of silicon and was shown to be about 340 cm^2/sec. and agreed with expected values.

An impurity redistribution effect was observed at

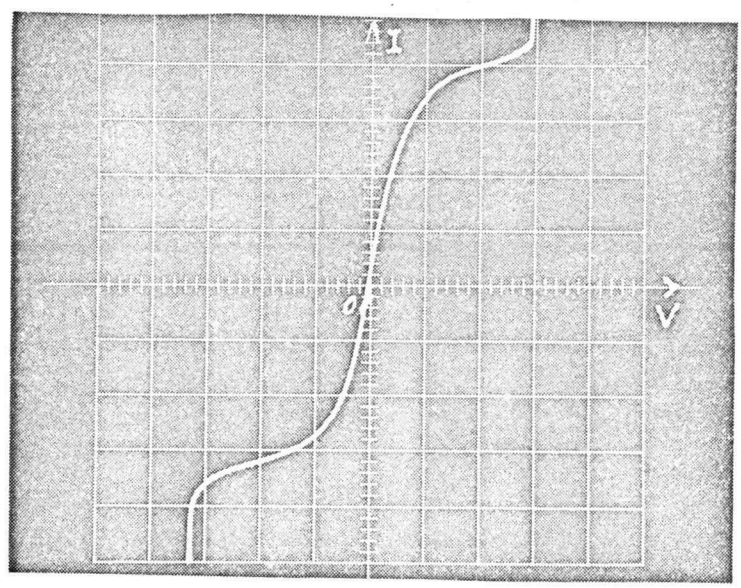
the vicinity of the gate 2 region represented by a thickening of the channel locally, and thereby greatly increased the average channel doping level $\bar{N}_c$. As a result, there was a difference between the values of channel doping level as obtained from Irvin's work (26) and the values as calculated from the channel resistance. The former values were found to be about ten times higher than the latter values.

The source-drain to gate 1 breakdown voltage was about 6.5 volts in this case. It may be desirable to increase this breakdown voltage by further decreasing the surface concentration during the channel region deposition. However, in increasing the breakdown voltage, the resistivity in the channel will be increased and the channel thickness will be reduced. This reduction in the channel thickness may not be desirable.



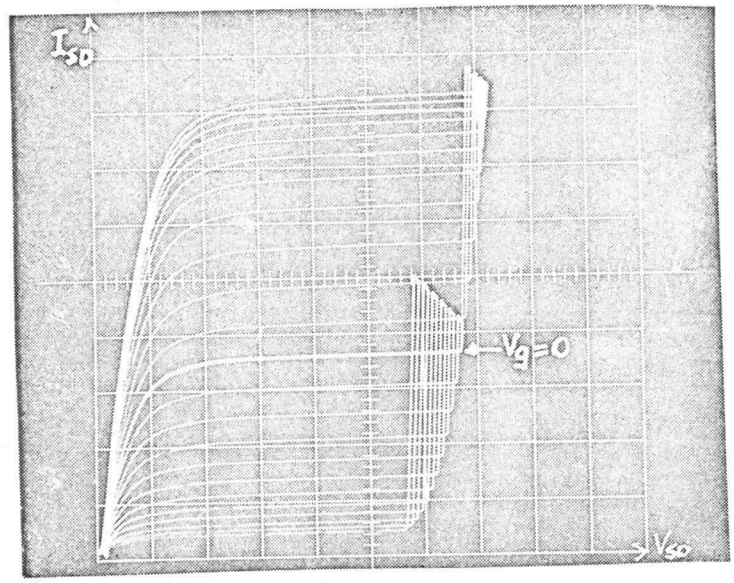
Vert. 0.1 ma/cm Hor. 1 V/cm Gate 0.1 V/step

Fig. 21. Field-effect transistor characteristic (I)
(Partial-masking type)



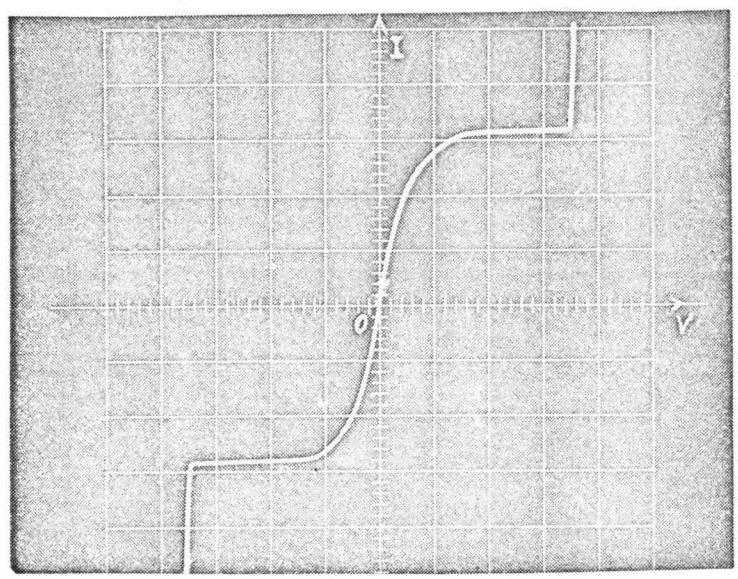
Vert. 0.1 ma/cm Hor. 2 V/cm (Open Gate)

Fig. 22. Field-effect transistor characteristic (II)
(Open Gate,Partial-masking type)



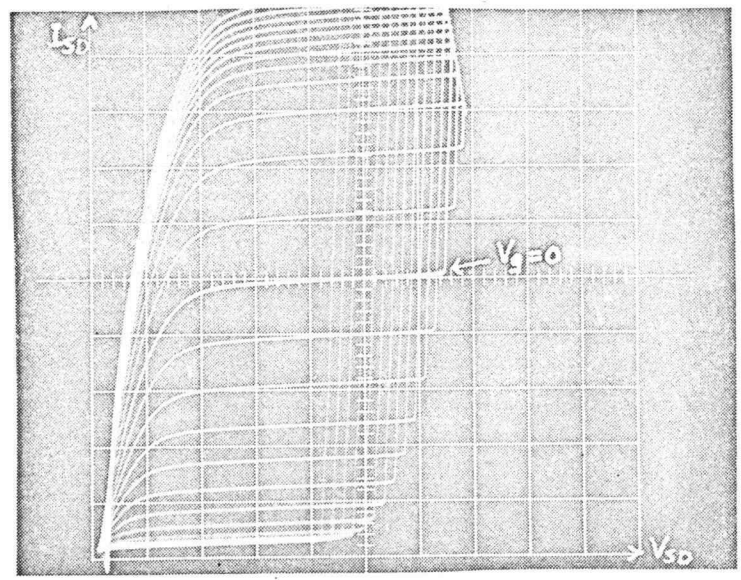
Vert. 0.05 ma/cm Hor. 1 V/cm Gate 0.1 V/step

Fig. 23. Field-effect transistor characteristic (I)
(Two-deposition type)



Vert. 0.1 ma/cm Hor. 2 V/cm (Open Gate)

Fig. 24. Field-effect transistor characteristic (II)
(Open Gate,Two-deposition type)



Vert. 0.05 ma/cm Hor. 1 V/cm Gate 0.2 v/step

Fig. 25. Field-effect transistor characteristic (I) (Etched-channel type)

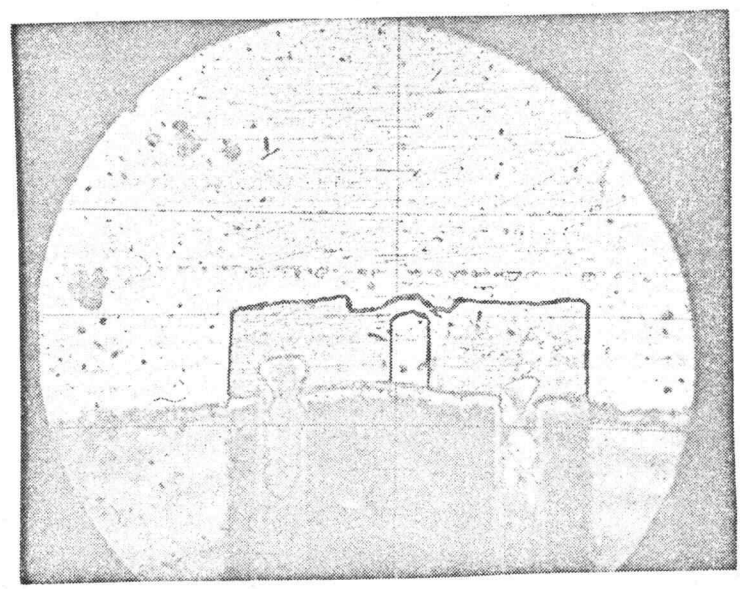


Fig. 26. Cross-sectional view of field-effect transistor (Partial-masking type) 400X

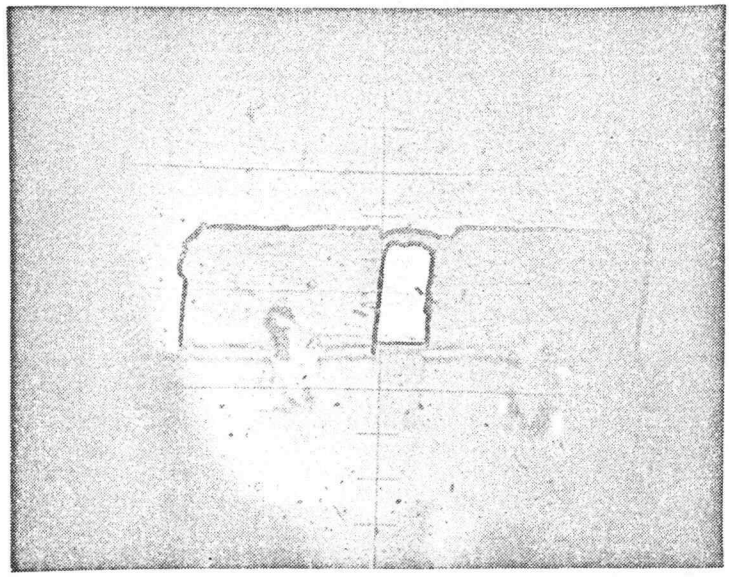


Fig. 27. Cross-sectional view of field-effect transistor (Two-deposition type) 400X

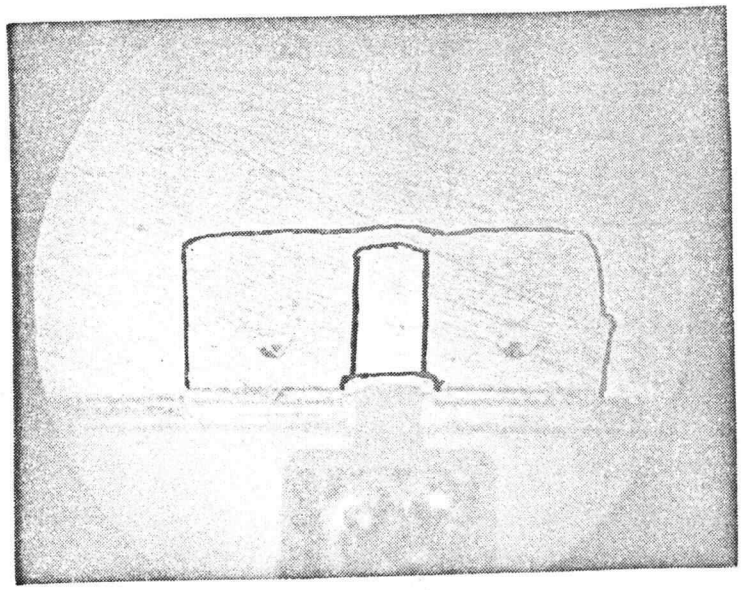


Fig.28. Cross-sectional view of field-effect transistor (Etched-channel type) 400X

BIBLIOGRAPHY

1. Adler, R. B. and R. L. Longini. Introduction to semiconductor physics. New York, Wiley, 1963. 247p.

2. Alley, Charles L. and K. W. Atwood. Electronic engineering. New York, Wiley, 1963. 646p.

3. Atalla, M. M. and E. Tannenbaum. Impurity redistribution and junction formation in silicon by thermal oxidation. Bell System Technical Journal 39:933-946. 1960.

4. Atalla, M. M., E. Tannenbaum and E. J. Scheibner. Stabilization of silicon surfaces by thermally grown oxides. Bell System Technical Journal 38:749-784. 1959.

5. Backenstoss, G. Evaluation of surface concentration of diffused layers in silicon. Bell System Technical Journal 37:699-709. 1958.

6. Barrer, R. M. Diffusion in and through solids. Cambridge, England, Cambridge University Press. 1951. 464p.

7. Bond, W. L. and F. M. Smits. The use of an interference microscope for measurement of extremely thin layers. Bell System Technical Journal 35:1209-1221. 1956.

8. Bosenberg, W. A. and J. A. Olmstead. Design and application of silicon unipolar transistors made by diffusion techniques. Paper prepared for a meeting of the Professional Technical Group on Electron Devices of the Institute of Radio Engineers, Washington, D.C. Oct. 1961.

9. Conwell, E. M. Properties of silicon and germanium; II. Proceedings of the Institute of Radio Engineers 46:1281-1300. 1958.

10. Dacey, G. C. and I. M. Ross. The field-effect transistor. Bell System Technical Journal 34:1149-1189. 1955.

11. Dacey, G. C. and I. M. Ross. Unipolar field-effect transistor. Proceedings of the Institute of Radio Engineers 41:970-979. 1953.

12. Deal, B. E. and A. S. Grove. General relationship for the thermal oxidation of silicon. Journal of Applied Physics 36:3770-3778. 1965.

13. Deal, B. E., E. H. Snow and A. S. Grove. Properties of the silicon dioxide-silicon system. Semiconductor Products and Solid State Technology 9(11):25-33. 1966.

14. Dunlap, W. C., Jr., H. V. Bohm and H. P. Mahon, Jr. Diffusion of impurities in silicon. (Abstract) Physical Review 96:822. 1954.

15. Evitts, H. C., H. W. Cooper and S. S. Flaschen. Rates of formation of thermal oxides of silicon. Journal of the Electrochemical Society 111:688-690. 1964.

16. Flint, P. S. The rates of oxidation of silicon. (Abstract) Journal of the Electrochemical Society 109:72C. 1962.

17. Frosch, C. J. Silicon diffusion technology. In: Transistor technology, ed. by F. J. Bioni. Vol. 3. New York, Van Nostrand, 1958. p. 90-99.

18. Frosch, C. J. and L. Derick. Surface protection and selective masking during diffusion in silicon. Journal of Electrochemical Society 104:547-552. 1957.

19. Fuller, C. R. and F. J. Strieter. Silicon oxidation. (Abstract) Journal of the Electrochemical Society 111:62C. 1964.

20. Fuller, C. S. Diffusion techniques. In: Transistor technology, ed. by F. J. Bioni. Vol. 3. New York, Van Nostrand, 1958. p. 64-89.

21. Fuller, C. S. and J. A. Ditzenberger. Diffusion of donors and acceptor elements in silicon. Journal of Applied Physics 27:544-553. 1956.

22. Halpern, J. and R. H. Redicker. Out-diffusion as a technique for the production of diodes and transistors. Proceedings of the Institute of Radio Engineers 46:1068-1076. 1958.

23. Horiuchi, Shiro and Jiro Yamaguchi. Diffusion of boron in silicon through oxide layer. Japanese Journal of Applied Physics 1:314-323. 1962.

24. Integrated circuits; edited version of a 1964 International Convention Symposium. IEEE Spectrum 1:62-101. June 1964.

25. Integrated Circuits Engineering Co. Unpublished chart on oxide thickness required for masking of a boron diffusion. Phoenix, Arizona.

26. Irvin, C. J. Resistivity of bulk silicon and of diffused layers in silicon. Bell System Technical Journal 41:387-410. 1962.

27. Javitz, A. E. and S. A. Halby. The materials of thin film devices. Electro-Technology 72(3):95-122. 1963.

28. Jensen, E. W. Polishing silicon wafers. Semiconductor Products and Solid State Technology 10(2):19-24. 1967.

29. Kerman, K. and M. Stelter. Coating of semiconductor substrates. Semiconductor Products and Solid State Technology 10(4):30-34. 1967.

30. Lauritzen, P. O. and O. Leistiko, Jr. Field-effect transistors as low-noise amplifiers. International Solid-state Circuits Conference, Digest of Technical Papers 5:62-63. 1962.

31. Lawrence, H. and R. M. Warner, Jr. Diffused junction depletion layer calculations. Bell System Technical Journal 39:389-404. 1960.

32. Levine, S. N. Principles of solid state microelectronics. New York, Holt, Rinehart and Winston, 1964. 211p.

33. Lin, H. C. et al. Advances in monolithic integrated circuits. Semiconductor Products and Solid State Technology 10(4):19-30. 1967.

34. Lindmayer, J. and C. Y. Wrigley. Fundamentals of semiconductor devices. New York, Van Nostrand, 1965. 486p.

35. McKay, K. G. Avalanche breakdown in silicon. Physical Review 94:877-884. 1954.

36. Mackintosh, I. M. The diffusion of phosphorus in silicon. Journal of the Electrochemical Society 109:392-401. 1962.

37. Miller, S. L. Ionization rates for holes and electrons in silicon. Physical Review 105:1246-1249. 1957.

38. Motorola Incorporated. Semiconductor Products Division. Integrated circuit: design principles and fabrication. New York, McGraw-Hill, 1965. 385p.

39. Phillips, A. B. Transistor engineering and introduction to integrated semiconductor circuits. New York, McGraw-Hill, 1962. 373p.

40. Prim, R. C. and W. Shockley. Joining solutions at the pinch off point in the "field-effect" transistor. Transactions of the Institute of Radio Engineers, Professional Group on Electron Devices, no. 4, p. 1-14. Dec. 1953.

41. RCA Receiving Tube Manual. Harrison, J. J., Radio Corporation of America. (Technical Series RC-22) 487p.

42. Reiss, H. and C. S. Fuller. Diffusion and precipitation in germanium and silicon. In: Semiconductors, ed. by N. B. Hannay. New York, Reinhold, 1959. p. 222-268. (American Chemical Society. Monograph 140)

43. Ryder, E. J. Mobility of holes and electrons in high electric fields. Physical Review 90:766-769. 1953.

44. Saby, J. S. and W. C. Dunlap, Jr. Impurity diffusion and space charge layers in "fused-impurity" p-n junctions. Physical Review 90:630-632. 1953.

45. Sah, C. T., H. Sello and D. A. Tremere. Diffusion of phosphorus in silicon oxide film. Journal of Physics and Chemistry of Solids 11:288-298. 1959.

46. Shive, J. W. The properties, physics and design of semiconductor devices. Princeton, N.J., Van Nostrand, 1959. 487p.

47. Shockley, W. The theory of p-n junctions in semiconductors and p-n junction transistors. Bell System Technical Journal 28:435-489. 1949.

48. Smits, F. M. Formation of junction structures by solid state diffusion. Proceedings of the Institute of Radio Engineers 46:1049-1061. 1958.

49. Smits, F. M. Measurement of sheet resistivities with the four point probe. Bell System Technical Journal 37:711-718. 1958.

50. Tannenbaum, M. and D. E. Thomas. Diffused emitter and base silicon transistors. Bell System Technical Journal 35:1-22. 1956.

51. Thurston, M. O., J. C. C. Tsai and K. D. Kang. Diffusion of impurities into silicon through an oxide layer. Columbus, Ohio, Ohio State University Research Foundation, 1961. 72 numb. leaves. (Report 896 - Final. U. S. Army Signal Supply Agency Contract DA-36-039-SC-83874)

52. Trumbore, F. A. Solid solubilities of impurity elements in germanium and silicon. Bell System Technical Journal 39:205-233. 1960.

APPENDIX I

Breakdown Voltage and Resistivity

The breakdown voltage (35, 36, 37, 38, 48) of the channel is determined by its doping level N_{cs} at the surface (highest), assuming the gate 1 region is doped heavier than the channel. The relationship is given in reference (38).

In general, V_{br} can be approximated by:

$$V_{br} = (5.65)\ 10^{-9}\ (N_c)^{0.657} \quad \ldots\ N_c \leq (2)10^{17}\ at/cm^3$$

$$V_{br} = (1.786)\ 10^{-3}\ (N_c)^{0.221}$$

$$(2)\ 10^{17} \leq N_c \leq 10^{19}\ at/cm^3$$

The relationship between the average doping level and the surface impurity concentration is discussed in reference 26. To find the surface impurity concentration, first, the average conductivity is calculated from the sheet resistance measurement.

$$\bar{\rho}_c = (4.5)\ 10^{-4}\ VX_c/I \qquad X_c \text{ in micron}$$

$$\bar{\delta}_c = 1/\bar{\rho}_c \qquad V \text{ in volts}$$

$$I \text{ in amp}$$

$$\rho \text{ in ohm-cm}$$

The average conductivity can be used to find the surface impurity concentration N_{cs} by referring to Irvin's resistivity plots (26) if the background concentration C_b is known. In this case C_b is $(4.5)\ 10^{15}\ at/cm^3$.

The concentration from $C_b = 10^{15}$ at/cm^3 is added on to the concentration from $C_b = 10^{16}$ at/cm^3 and the sum is multiplied by 0.45 to obtain the estimated concentration at (4.5) 10^{15} at/cm^3 background doping level.

From the value of N_{cs}, the average conductivity corresponding to the junction depth ratio (X_{gl}/X_c) was read from the graph. The reciprocal of conductivity (resistivity) can be used to find the average doping level of the channel from Irvin's plot of resistivity of p-type silicon at 300°K as a function of acceptor or donor concentration (26).

APPENDIX II

Diffusion Relationships

The gaussian distribution can be described by the relationship:

$$N(x,t) = Q \ln(-X^2/4Dt) \; / \; (\pi Dt)^{1/2}$$

where Q is the sheet concentration in at/cm^2

D is the diffusion constant in cm^2/sec

t is the diffusion time in hours.

$$Q = \overline{N(x_j,t)} X_j$$

where $\bar{N}$ is the average doping level

X is the distance in cm

X_j is the junction depth.

The complementary error function distribution is given as:

$$N(x,t) = N_s \; \text{erf} \; \; x/(4Dt)^{1/2}$$

The two distribution functions are plotted as shown in Fig. 8.

For the complementary error function distribution the total impurity concentration can be arrived at by integrating the error function complement and is given by:

$$Q = 1.13 \; N_s (Dt)^{1/2}$$

where $D = (4) \; 10^{-13}$ cm^2/sec at 950°C

and $D = (9) \; 10^{-14}$ cm^2/sec at 1100°C.

APPENDIX III

Junction Depth Evaluation

Since the diffused junction depth was very shallow (1.5 microns) a one degree angle delineation magnification was used. The sample was mounted on a block tilted at an initial angle of 1° and polished with 0.3 micron alumina powder to expose the diffused region. A drop of p-n junction stain consisting of 5 $CuSO_4$ (saturated) to 1 HF (48%) was applied to the exposed region under infrared irradiation. The n-region was stained to a copper color while the p-region remained dark.

A filar eye-piece equipped with a Unitron micrometer (calibrated with interference fringes from a two-beam interferometer) was used to measure the junction depths, using the relationship given below:

$$X_j = 17.5\ d/M$$

where d is the horizontal distance measured by the micrometer and M is the magnification of the filar eye-piece (calibrated with interferometer).

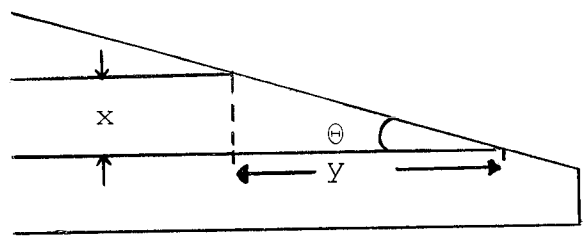


Fig. 30. Angle delineation magnification.

$x = y \tan \Theta^{\circ}$ For small angle $\tan \Theta^{\circ} \approx \pi\Theta^{\circ}/180^{\circ}$

$y = d/10^{-3}M$ where d in mm

y in micron

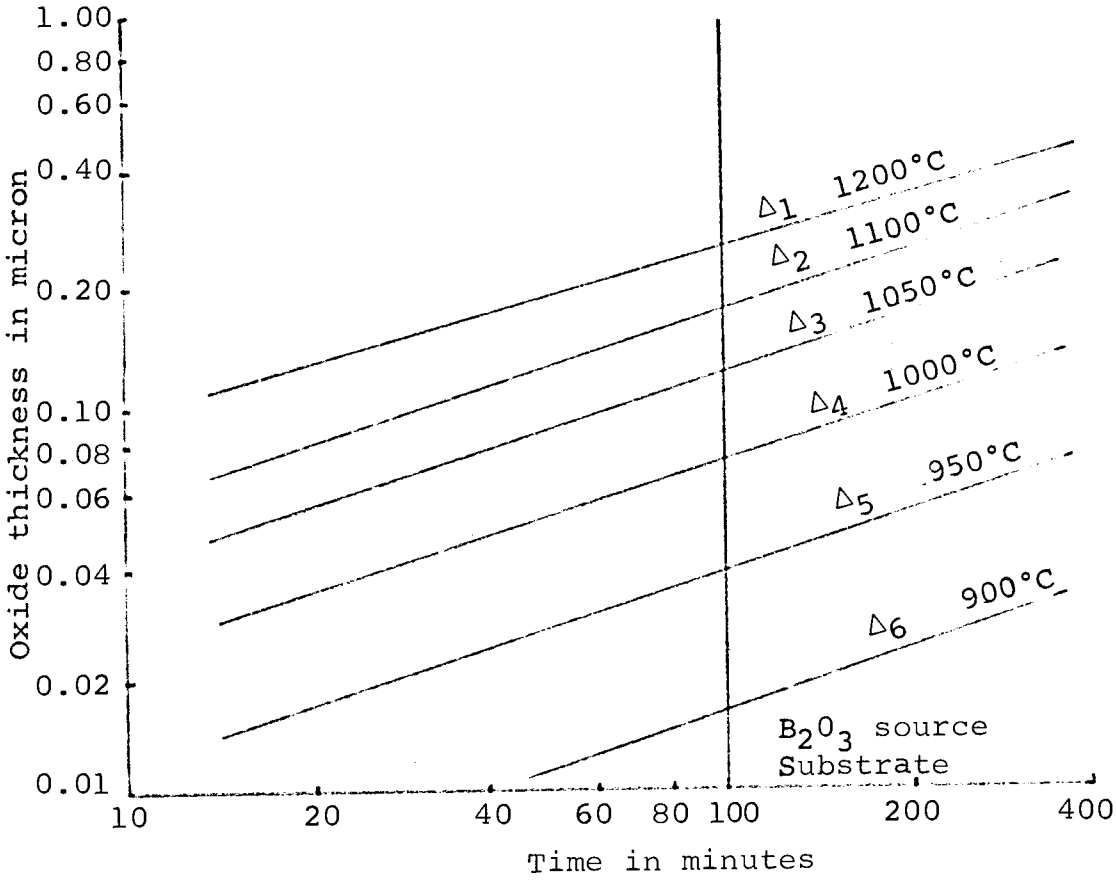
M = Magnification of eye-piece

$\Theta = 1^{\circ}$

$X = (\pi d)\ 10^{3}/180M$

$= 17.5\ d/M$ in micron

Appendix IV (25). Projection scheme on estimation of mask-failure oxide thickness of a boron diffusion.



Δ_1 = 0.37 cm/50°C
Δ_2 = 0.49 cm/50°C
Δ_3 = 0.80 cm/50°C
Δ_{12} = 0.12 cm/50°C
Δ_{23} = 0.31 cm/50°C
Δ_{34} = 0.33 cm/50°C

Δ_4 = 1.13 cm/50°C
Δ_5 = 1.47 cm/50°C
Δ_6 = 1.82 cm/50°C
Δ'_6 = 0.36 cm/10°C
Δ_{45} = 0.34 cm/50°C
Δ_{56} = 0.35 cm/50°C

Fig. 29. Projection scheme on estimation of mask-failure oxide thickness of a boron diffusion (from I.C.E.) (25).

APPENDIX V

Method and Sample Calculation of Field-effect Transistor Parameters

(1) Partial-masking Method:

W_c = 10 mils — G_o exp = 320μ mho

L = 1 mil — V_p exp = 1.3 volts @ $V_g = 0$

X_c = 0.096 micron — I_p exp = 0.205 ma

R_c = 33kΩ

X'_c = 1.056 micron

X_e = 0.96 micron

X_b = 1.20 micron

Using channel resistance and

$$\bar{\rho}_c = \frac{\bar{R}A}{l} = (3.3)\ 10^3\ (10)(0.096)/(1)\Omega\text{-cm} = 0.317\Omega\text{-cm}$$

$\bar{N}_c = 8.6 \times 10^{16}$

$\mu_p = 280\ cm^2/v\text{-sec}$ ... from the plot of carrier mobilities in silicon (1)

$G_o = q\mu_p \bar{N}_c\ X_c W_c/L = 369$ micromho

$V_p = q\bar{N}_c\ X_c^2/8\epsilon\epsilon_o = \bar{N}_c X_c^2\ (18.8)\ 10^{-16}$ volts

(X_c in micron)

$= 2.01$ volts

$I_p = G_o V_p/3 = 0.369 \times 2.01/3$ ma $= 0.259$ ma

Using resistivity measurement values:

$V/I_b = 44\ \Omega/sq$

$V/I_c = 56\ \Omega/sq$

$X_e/X'_c = 0.96/1.056 = 0.909$

$\bar{\rho}_b = (V/I_b)(4.5)(X_b)\ 10^{-4}\ \Omega\text{-cm} = (2.375)\ 10^{-2}\ \Omega\text{-cm}$

$\bar{\sigma}_b = 42.1$ mho/cm

Referring to silicon resistivity plot (26)

$\bar{N}_b = (4)\ 10^{18}$ at/cm^3

$N_{bs} = (1.4+1.2)(0.55)\ 10^{19}$ at/cm^3

$N_{bs} = (1.31)\ 10^{19}$ at/cm^3

$\bar{\rho}_c = (2.66)\ 10^{-2}\ \Omega\text{-cm}$

$\bar{\sigma}_c = 37.6$ mho/cm

$N_{cs} = (1.2+1.0)(0.55)\ 10^{19}$ at/cm^3 $= (1.11)\ 10^{19}$ at/cm^3

$\bar{N}_c = (3.3)\ 10^{18}$ at/cm^3

At $X_e/X'_c = 0.909$ $\quad \bar{\sigma}_{x/x_c} = (1.3)\ 10^{-1} \ldots 10^{15}$

$= (5)\ 10^{-1} \ldots 10^{16}$

$\bar{\rho}_{x/x_c} = 7.7 \ldots 10^{15}$ $\quad \bar{N}_{x/x_c} = (1.7)\ 10^{15} \ldots 10^{15}$

$= 2.0 \ldots 10^{16}$ $\quad = (7.0)\ 10^{15} \ldots 10^{16}$

$\bar{N}_{x/x_c} = (1.7+7.0)(0.45)\ 10^{15}$ at/cm^3 $= (3.9)\ 10^{15}$ at/cm^3

V_{Br} @ $N_{cs} = (1.11)\ 10^{19}$ at/cm^3 $\quad$ 4 volts (Fig. 31)

$\bar{\rho}_e = (1.297)\ 10^{-3}\ \Omega\text{-cm}$

$\bar{\sigma}_e = 771$ mho/cm

$\bar{N}_e = (6)\ 10^{19}$ at/cm^3

$\bar{N}_{es} = (2.1)\ 10^{20}$ at/cm^3 At $C_e = 10^{18}$ at/cm^3

The efficiency, E, can be found as

$E = G_o/V_p$ micro-mho/volt = 246 micro-mho/volt

$(E)(X_c) = C = 8W_c\epsilon\epsilon_o\mu_p/L_e = (8.51)\ 10^{-11}\ \mu_p$ mho-cm/volt

$C = (246)\ 10^{-6}\ (0.096)\ 10^{-4}$ mho-cm/volt = $(2.36)\ 10^{-9}$ mho-cm/volt

The estimated mobility is

$\mu_p = C/(8.51)\ 10^{-12}$ cm^2/v-sec = 278 cm^2/v-sec

$\mu_p = 280$ cm^2/v-sec from mobility plot (1)

($\bar{N}_c = (8.6)\ 10^{16}$ at/cm^3)

(2). Two-deposition Method:

$W_c = 10$ mils G_o exp = 275 micro-mho

$L = 1.0$ mil V_p exp = 1.10 volts

$X_c = 0.11$ micron I_p exp = 0.09 ma

$R_c = 5.0k\Omega$

$X'_c = 1.47$ micron

$X_e = 1.36$ micron

$X_b = 1.60$ micron

$\bar{\rho}_c = 0.55\ \Omega$-cm $\bar{N}_c = (3.5)\ 10^{16}$ at/cm^3 @ $R_c = 5k\Omega$

$\mu_p = 350$ cm^2/v-sec from Motorola (1)

$G_o = 215.5$ micro-mho

$V_p = 0.796$ volts

$I_p = 0.0571$ ma

Using resistivity measurement:

V/I_b = 45.5 Ω/sq

V/I_c = 66.6 Ω/sq

X_e/X'_c = 0.922

$\bar{\rho}_b$ = (3.28) 10^{-2} Ω-cm

$\bar{\partial}_b$ = 30.5 mho/cm

$\bar{N}_b$ = (2.55) 10^{18} at/cm^3

$\bar{\rho}_c$ = (4.26) 10^{-2} Ω-cm

$\bar{\partial}_c$ = 23.5 mho/cm

N_{cs} = (5.6) 10^{18} at/cm^3

$\bar{N}_c$ = (1.7) 10^{18} at/cm^3

$\bar{\partial}_{x/x_c}$ = (8) 10^{-2} ... 10^{15} = (4) 10^{-1} ... 10^{16} $\quad$ $\bar{\rho}_{x/x_c}$ = 12.5 ... 10^{15} = 2.5 ... 10^{16}

$\bar{N}_{x/x_c}$ = (3.07) 10^{15} at/cm^3

V_{Br} @ (5.6) 10^{18} at/cm^3 = 4.5 volts

$\bar{\rho}_e$ = (1.22) 10^{-3} Ω-cm

$\bar{\partial}_e$ = 818 mho/cm

$\bar{N}_e$ = (7) 10^{19} at/cm^3

$\bar{N}_{es}$ = (2.5) 10^{20} at/cm^3 $\quad$ at C_B = 10^{18} at/cm^3

E = 250 micro-mho/volt

C = (2.75) 10^{-9} mho-cm/volt

μ_p = 323 cm^2/v-sec $\quad$ μ_p (from Motorola (1)) = 350 cm^2/v-sec

(3). Etched-channel Method:

W_c = 10 mils G_o exp = 400 micro-mho

L = 1 mil V_p exp = 2.2 volts

X_c = 0.16 micron I_p exp = 0.72 ma

R_c = 2.97 kΩ

X_c' = 1.48 micron

X_e = 1.32 micron

X_b = 1.48 micron

Using channel resistance:

$\bar{\rho}_c$ = 0.475 Ω-cm $\bar{N}_e$ = (4.3) 10^{16} at/cm^3

μ_p = 350 cm^2/v-sec (from Motorola (1))

G_o = 385 micro-mho

V_p = 2.02 volt

I_p = 0.776 ma

Using resistivity:

V/I_b = 45.5 Ω/sq

V/I_c = 67.7 Ω/sq

X_e/X_c' = 0.892

$\bar{\rho}_b$ = (3.03) 10^{-2} Ω-cm

∂_o = 33 mho/cm

$\bar{N}_b$ = (2.3) 10^{18} at/cm^3

$\bar{\rho}_c$ = (4.02) 10^{-2} Ω-cm

$\bar{\partial}_c$ = 24.8 mho/cm

N_{cs} = (6.55) 10^{18} at/cm^3

$\bar{N}_c = (1.8)\ 10^{18}$ at/cm^3

$\bar{\delta}_{x/x_c} = (1.65)\ 10^{-1}$ mho/cm ... 10^{15}

$\bar{\rho}_{x/x_c} = 2.06\ \Omega$-cm ... 10^{15}

$= (7.00)\ 10^{-1}$ mho/cm ... 10^{16}

$\bar{\rho}_{x/x_c} = 1.43\ \Omega$-cm ... 10^{16}

$\bar{N}_{x/x_c} = (6.16)\ 10^{15}$ at/cm^3

$V_{Br} = 4.5$ volts @ $N_{cs} = (6.55)\ 10^{18}$ at/cm^3

$\bar{\rho}_e = (1.25)\ 10^{-3}\ \Omega$-cm

$\bar{\delta}_e = 889$ mho/cm

$\bar{N}_e = (7)\ 10^{19}$ at/cm^3

$N_{es} = (2.5)\ 10^{20}$ at/cm^3 at $C_B = 10^{18}$ at/cm^3

E - 182 micro-mho/volt

C = $(2.9)\ 10^{-9}$ mho-cm/volt

$\mu_p = 342$ cm^2/v-sec μ_p (from Motorola (1)) = 350 cm^2/v-sec

APPENDIX VI

Miscellaneous

1. Buffered hydrofluoric acid.....4 NH_4F(Sat) : 1 HF
2. Silicon-etch.....20 HNO_3 : 1 HF(48%) : 10 H_2O
3. Aluminum-etch.....80 H_3PO_4 : 16 H_2O : 5 HNO_3
   at 80°C
4. Boron source.....40% B_2O_3 + 60% SiO_2
5. Junction-stain.....5 $CuSO_4$(sat) : 1 HF(48%)
6. Photo-resist.....AZ1350 positive photo-resist
   from Shipley
7. Phosphorus-source.....P_2N_5