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Title A CONTROLLED NEGATIVE-RESISTANCE FOR REALIZATION OF CERTAIN NETWORK FUNCTIONS

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(Major professor)

A circuit which functions as a controlled negative-resistance is described and analyzed; the circuit contains two transistors, a breakdown diode, and five resistors connected in a stable feedback configuration. From the analysis a set of design equations is derived.

An experimental circuit is described and a comparison between measured performance and design objectives is presented.

Several network synthesis procedures are presented to provide background for experimental realizations using the controlled negative-resistance. The problem of biasing is examined for the synthesis techniques presented.

Two experimental realizations, one providing gain and one providing complex zeros of transmission, are described and performance is compared to theoretical specifications; in both cases the agreement is excellent.

A CONTROLLED NEGATIVE-RESISTANCE FOR REALIZATION OF CERTAIN NETWORK FUNCTIONS

by

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TABLE OF CONTENTS

LIST OF FIGURES

A CONTROLLED NEGATIVE-RESISTANCE FOR REALIZATION OF CERTAIN NETWORK FUNCTIONS

I. INTRODUCTION

Since the advent of the tunnel diode in 1958, several procedures of synthesizing networks using tunnel diodes have been developed. Tunnel-diode networks have several advantages over conventional resistance-capacitance (RC) networks; a tunnel-diode network can provide greater gain than can a pure RC network, and a tunnel diode and RC network in ladder form can realize transmission functions impossible to realize with an RC ladder without tunnel diodes.

Tunnel diodes, however, have characteristics which limit their usefulness as network elements; the magnitude of the negative-resistance is highly nonlinear, the capability of handling signals greater than a few hundred millivolts is greatly limited, there is limited choice of values of negative-resistance which can be provided, and the repeatability of negative-resistance values for diodes of the same type is generally poor.

The controlled negative-resistance to be described overcomes many of the limitations of tunnel diodes. The magnitude of the negative-resistance is quite linear over a large portion of the operating range, signal handling capability is the choice of the designer, and almost any value of negative resistance may be obtained with good repeatability.

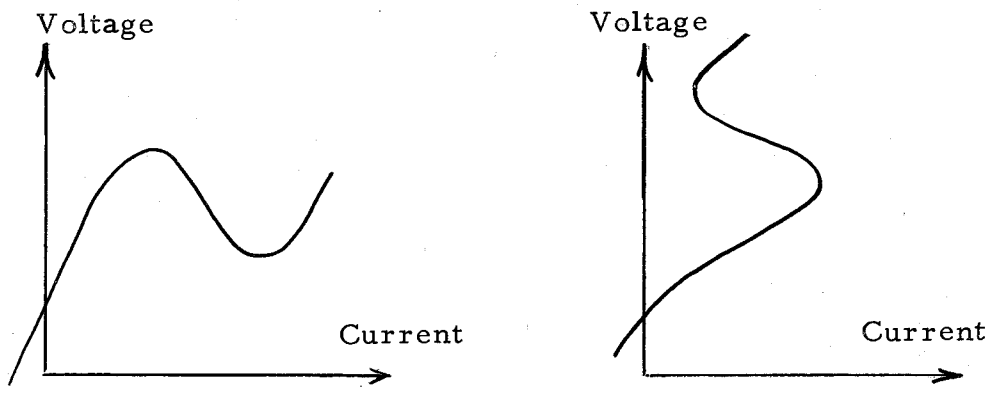
II. NEGATIVE-RESISTANCE DEVICES

Negative resistance is an electrical characteristic defined as either a decrease in current with increasing voltage if voltage is the independent variable or, conversely, a decrease in voltage with increasing current if current is the independent variable.

A number of electrical devices and circuits exhibit negative resistance. Some devices have been known for many years; examples are the electric arc (1, p. 492) and the dynatron (2, p. 5). Vacuum-tube negative-resistance circuits have been built for telephone repeater applications (1, p. 506; 7, p. 98). Advances in solid-state technology have produced a number of devices and numerous circuits exhibiting negative resistance; these include the tunnel diode (9, p. 1203), the unijunction transistor (3, p. 2), the four-layer diode (8, p. 9), negative-impedance converters (5, p. 726), and various other composite circuits (10, p. 326; 11, p. 25).

A negative resistance may be classified according to the shape of its characteristic curve. The two basic types are shown in Figure 2.1.

Figure 2.1(a), an N-type negative-resistance, is considered current controlled since voltage is a single-valued function of current. Figure 2.1(b), an S-type negative resistance, is considered voltage controlled since current is a single-valued function of voltage.



(a) N-Type (b) S-Type

Figure 2.1. Negative resistance types.

A positive-resistance, by definition, dissipates energy; conversely, a negative resistance supplies or converts energy. Since no physical device can supply an infinite quantity of energy, any negative-resistance must be bounded by two positive-resistance regions in a manner similar to the characteristic curves indicated in Figure 2.1.

In general, negative-resistances are not pure resistances but have some associated reactances. There is, at least, always some shunt capacitance which is inherant to all physical devices.

An example of limitations present in negative resistances is provided by the tunnel diode; a typical tunnel diode characteristic curve is indicated in Figure 2.2 and an equivalent circuit is given in Figure 2.3 (9, p. 1203).

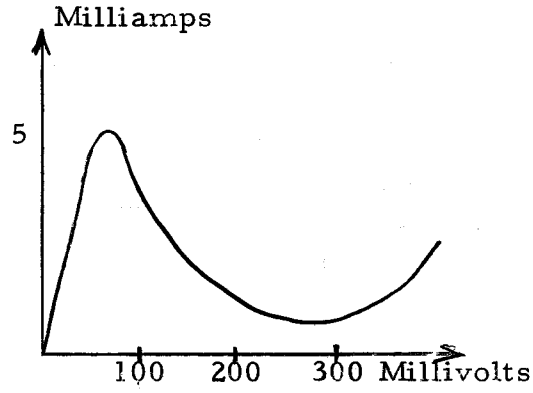


Figure 2.2. Typical tunnel diode characteristic curve.

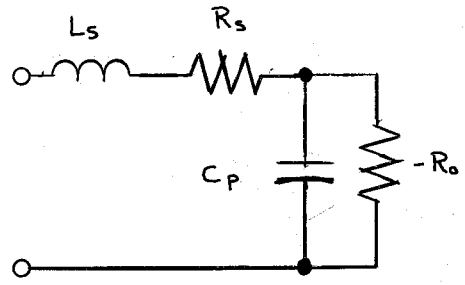


Figure 2.3. Tunnel diode equivalent circuit.

Negative resistances have many practical applications. Negative-impedance telephone repeaters have already been mentioned. Several network-synthesis methods have been developed using negative-impedance converters (4, p. 555-64; 15, p. 140-44). Tunnel diodes are used extensively as microwave oscillators, amplifiers, and converters, as logic elements, and as network synthesis elements (9, p. 1201-6; 6, p. 357-62; 13, p. 80-87; 14, p. 116-20).

III. A CONTROLLED NEGATIVE-RESISTANCE

3. 1 Basic Circuit Analysis

A simple analysis of the circuit in Figure 3. 1 will reveal three regions of operation as the voltage, V, increases from zero. These regions will be designated Regions I, II, and III in order of increasing voltage. In the following analysis, all voltages and currents are static unless otherwise indicated.

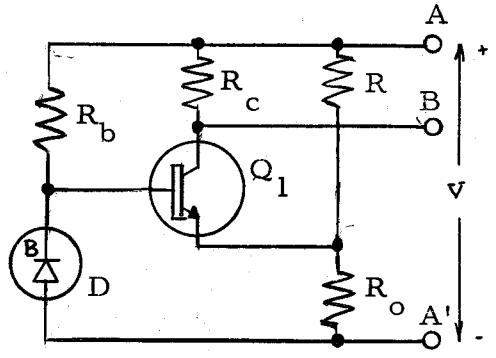


Figure 3. 1. A portion of the controlled negative resistance circuit.

Region I is characterized by the breakdown diode, D, in Figure 3. 1 not conducting. Using the simplified equivalent circuit for the transistor, Q_1, given in Figure 3. 2, the equivalent circuit of Figure 3. 1 which applies in Region I is given in Figure 3. 3. As V increases, the base current, I_{B1}, increases causing an increase in both the collector current, βI_{B1}, and the net input current, I. The lower limit of V for this region is at V = 0 and the upper limit occurs when the diode, D, breaks down.

Region II is characterized by conduction in the diode and all active elements. For these conditions the circuit in Figure 3. 1 has

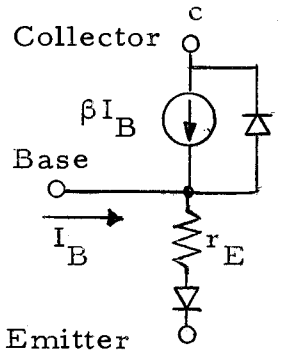


Figure 3.2. Simplified transistor equivalent circuit.

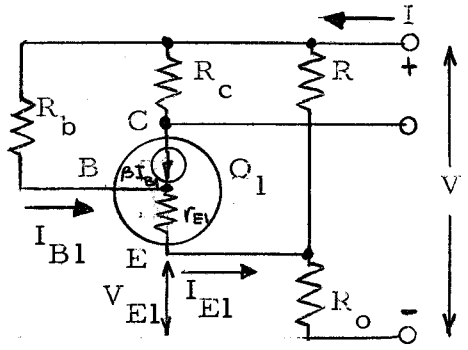


Figure 3.3. Region I equivalent of Figure 3.1.

the simple equivalent circuit shown in Figure 3.4. Referring to Figure 3.4 the base of Q_1 is kept at a constant voltage, V_D, by the conducting breakdown diode. The transistor tries, within gain limitations,

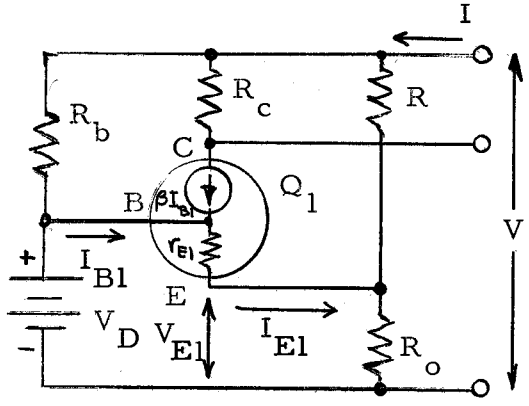


Figure 3.4. Region II equivalent of Figure 3.1.

to keep its emitter voltage, V_{E1}, constant since the base voltage is constant; a constant V_{E1} implies a constant current through R_0. But as V increases, the voltage drop across R, $V - V_{E1}$, increases, increasing the current through R. Since the current through R_0 is the sum of the current through R, and I_{E1}, the emitter current of Q_1, the emitter current must decrease if V_{E1} is to remain constant. The

upper boundary of this region occurs when I_{E1} decreases to zero and Q_1 becomes cut off.

Region III is characterized by conduction of the breakdown diode and the cutoff of all active elements. For these conditions, the circuit in Figure 3.1 has the simple equivalent shown in Figure 3.5. In this region the only current is through R_b and through the series combination of R and R_o.

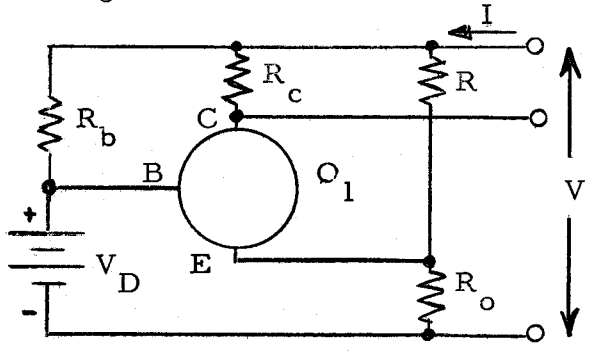


Figure 3.5. Region III equivalent of Figure 3.1.

Since the collector current of a transistor is approximately the emitter current and is proportional to the base current, the net result is that the collector current increases in Region I, decreases in Region II, and is zero in Region III. At the same time the input current, I, increases in Region I and in Region III, but remains almost constant in Region II.

A negative resistance results in Region II if the amplifier shown in Figure 3.6 is added to the circuit in Figure 3.1. In Figure 3.6 the input current, I', is the sum of I and of I_{E2}. I_{E2} is proportional

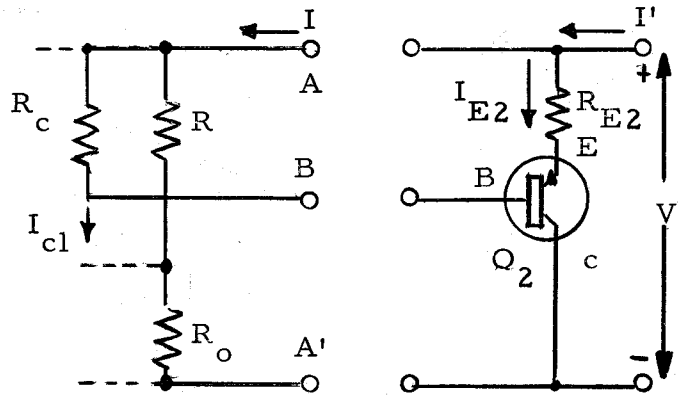


Figure 3.6. Current amplifier.

to the collector current of Q_1, I_{C1}, according to the values of R_C and R_E. If circuit values are chosen so that I_{E2} is a large portion of I', the I' will increase in Region I, decrease in Region II and increase again in Region III. The input current vs. voltage characteristics as indicated by this simplified analysis is shown in Figure 3.7 and the complete circuit is given in Figure 3.8.

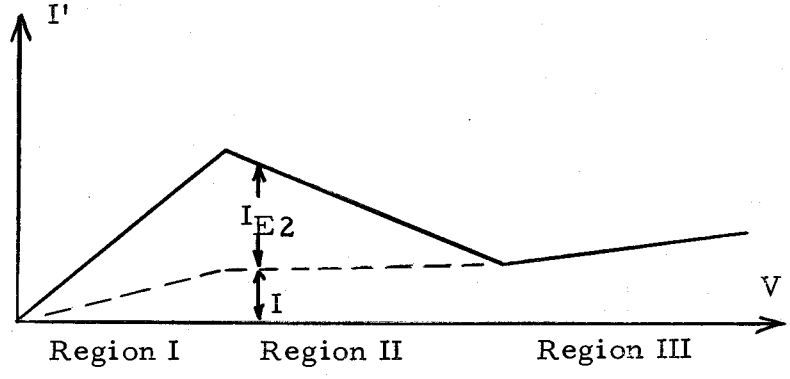


Figure 3.7. Input voltage-current characteristics.

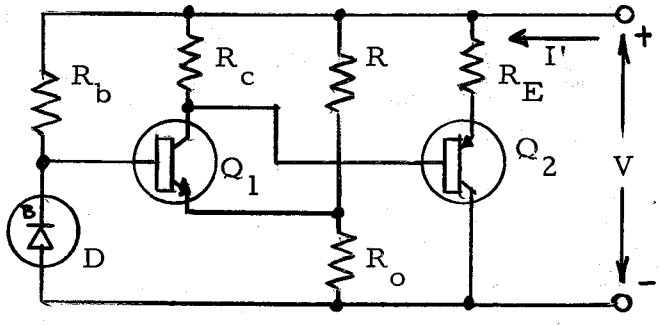


Figure 3.8. Controlled negative resistance circuit.

Control of the negative-resistance region is achieved by changing R_E. Since the value of R_E controls only the gain of the current amplifier, changing R_E will change the currents in Region I and II without changing the voltages which bound these regions.

3.2 Detailed Circuit Analysis

A more detailed analysis is necessary to explain some of the observed circuit characteristics and to provide accurate performance equations for design purposes. This analysis will be based on the large-signal equivalent circuits shown in Figure 3.9. Using these circuits, the equivalent circuit of Figure 3.8 is shown in Figure 3.10.

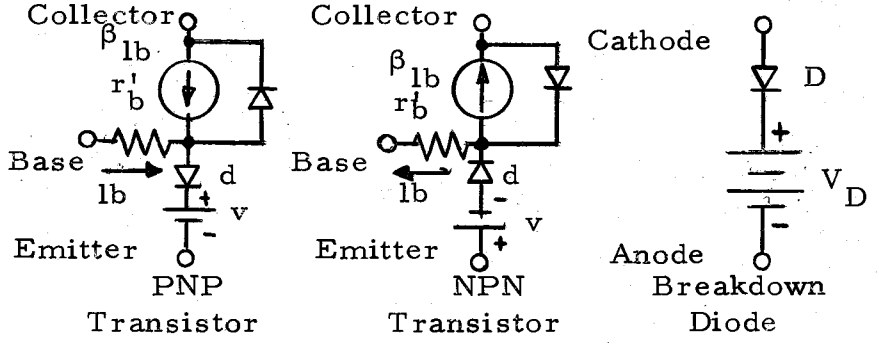


Figure 3.9. Component large-signal equivalent circuits.

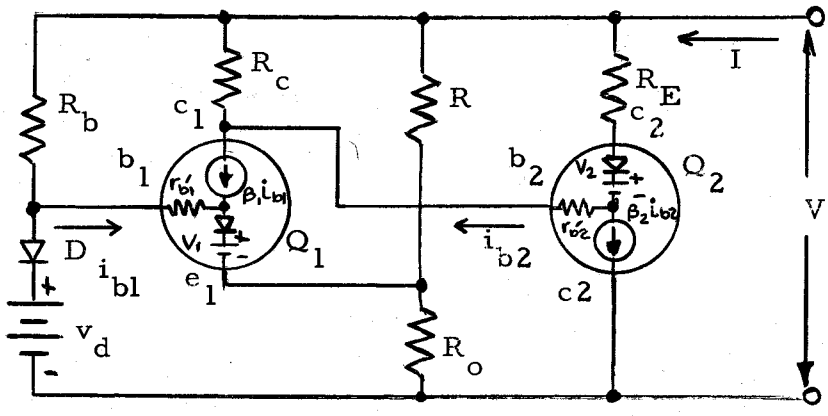


Figure 3.10. Large-signal equivalent circuit of Figure 3.8.

The following analysis will be divided into regions; the regions will be considered in the order of increasing terminal voltage and will be labeled sequentially with subscripted upper-case letters. The upper boundary of a region is labeled by upper-case letters in parenthesis. Subscripts in lower-case letters and/or numbers indicate circuit locations. Upper-case voltages and currents refer to the input terminals; lower-case, to internal circuit locations. Examples are: I_A is input current in Region A; V(C) is input voltage at upper limit of Region C; v_{b1} is the base voltage of Q_1. In addition, incremental resistance, dV/dI, will be designated R'.

Region A, which begins at V = 0, is defined by neither D, Q_1, nor Q_2 conducting; since Q_1 is not conducting, there is no voltage across R_c and Q_2 cannot conduct. Upper boundary for the region occurs when Q_1 conducts. Figure 3.11 shows the equivalent for this region; Q_1 is included to determine V(A).

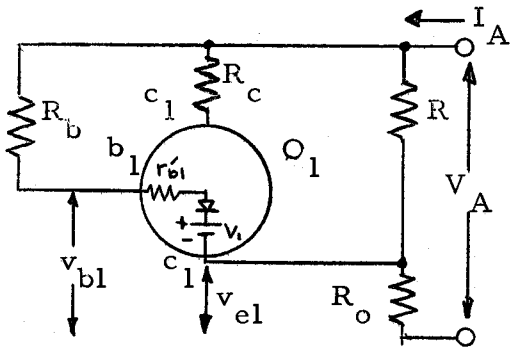


Figure 3.11. Region A equivalent of Figure 3.10.

The only current flowing is through R and R_o so that

$$I_A = V_A/(R + R_o) \qquad \text{(Eqn. 3.1)}$$

$$R'_A = (R + R_o) \qquad \text{(Eqn. 3.2)}$$

Q_1 will begin to conduct when $v_{bl} - v_{el} = v_1$. Since no current flows in R_b, $v_{bl} = V_A$, and $v_{el} = V_A R_o/(R + R_o)$. Then V(A) occurs when $V_A\left(1 - \frac{R_o}{R + R_o}\right) = v_1$, or

$$V(A) = v_1 \left(1 + \frac{R_o}{R}\right) \qquad \text{(Eqn. 3.3)}$$

Region B is defined by conduction of Q_1 but cut off of D and Q_2; after Q_1 begins to conduct, i_{c1} must increase until the voltage drop across R_c exceeds v_2 before Q_2 can conduct. Figure 3.12 shows the equivalent circuit for this region.

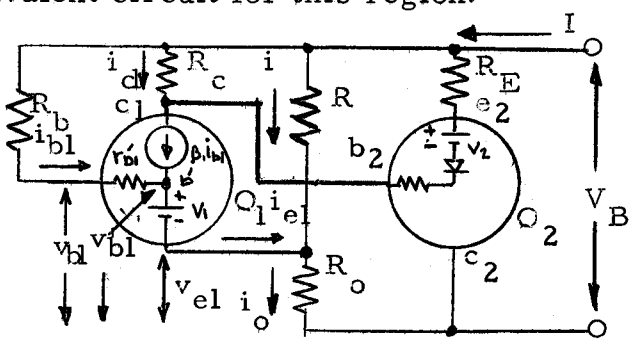


Figure 3.12. Region B equivalent of Figure 3.10.

The equations relating the currents and voltages in Figure 3. 12 are:

$$i_o = i_{b1}(\beta_1 + 1) + i \qquad I = i_o$$

$$v'_{b1} = v_1 + v_{e1} \qquad v_{e1} = i_o R_o$$

$$i = (V_B - v_{e1})/R \qquad (V_B - v'_{b1}) = i_{b1}(R_b + r'_{b1})$$

Solving these equations for I_B and R'_B gives:

$$I_B = \frac{V_B[R(\beta_1 + 1) + R_o + r'_{b1}] - v_1 R(\beta_1 + 1)}{R_o(R+R_o) + RR_o(\beta_1 + 1)} \quad \text{(Eqn. 3. 3)}$$

$$R_B = \frac{(R_b + r'_{b1})(R + R_o) + RR_o(\beta_1 + 1)}{R(\beta_1 + 1) + (R_b + r'_{b1})} \quad \text{(Eqn. 3. 4)}$$

V(B) occurs when $i_{b1}R_c = v_2$; substituting and solving for V(B) and I(B):

$$V(B) = v_1\left(1+\frac{R_o}{R}\right) + \frac{v_2}{R_c\beta_1}\left[(R_b + r'_{b1})\left(1+\frac{R_o}{R}\right) + R_o(\beta_1+1)\right] \quad \text{(Eqn. 3. 5)}$$

$$I(B) = \frac{v_1}{R} + \frac{v_2}{R\beta_1}\left[\beta_1 + 1 + \frac{R_b + r'_{b1}}{R}\right] \quad \text{(Eqn. 3. 6)}$$

Region C is defined by both Q_1 and Q_2 conducting but D not conducting; V(C) occurs when D starts to break down. The equivalent circuit is shown in Figure 3. 13.

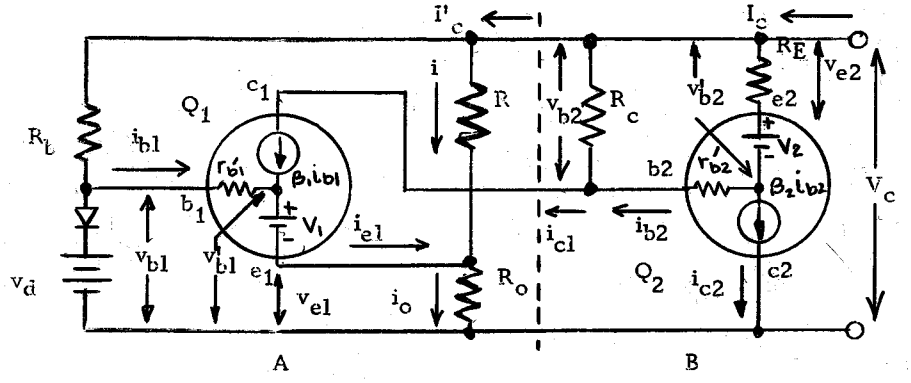


Figure 3. 13. Region C equivalent of Figure 3. 10.

The equations relating voltages and currents in Figure 3. 13a are:

$$I'_B = i + i_{b1} \qquad i_o = i + (\beta_1 + 1)i_{b1}$$

$$v'_{b1} = v_1 + v_{e1} \qquad v_{b1} = V - R_b i_{b1}$$

$$V - v_{e1} = iR \qquad v_{e1} = i_o R_o$$

$$v_{b1} - v'_{b1} = r'_{b1} i_b$$

and for Figure 3. 13b are:

$$I_B = I'_B + i_{c1} + \beta_2 i_{b2} \qquad v_{b2} = R_c (i_{c1} + i_{b2})$$

$$v_{b2} - v_{b2} = i_{b2} r'_{b2} \qquad v_{b2} = v_2 + R_E(\beta_2 + 1)i_{b2}$$

Solving the proceeding two sets of equations for I_C and R'_C gives:

$$I_C = \frac{V_C[R_b\gamma + r'_{b1} + R(\beta_1+1) + \beta_1\beta_2\gamma R] - v_1[(R+R_o)\beta_1\beta_2\gamma + R(\beta_1+1)]}{(R_b + r'_{b1})(R_o + R) + (\beta_1 + 1)RR_o}$$

$$- \frac{\gamma v_1 \beta_2}{R_c} \qquad \text{(Eqn. 3. 7)}$$

$$R'_C = \frac{(R_b + r'_{bl}) + (\beta_1 + 1)\, R}{\beta_1 \beta_2 R\gamma + R_b + r'_{bl} + (\beta_1 + 1)R} \qquad \text{(Eqn. 3.8)}$$

where:

$$\gamma = \frac{R_c}{(\beta_2 + 1)R_E + R_c + r'_{b2}} \qquad \text{(Eqn. 3.9)}$$

V(C) occurs when $v_{bl} = v_d$. Solving for V(C) and the corresponding current, I(C), gives:

$$V(C) = \frac{v_d[(R_b + r'_{bl})(R + R_o) + (\beta_1 + 1)RR_o] - v_1 R_b (R + R_o)}{r'_{bl}(R + R_o) + R_b R_o + RR_o(\beta_1 + 1)} \qquad \text{(Eqn. 3.10)}$$

$$I(C) = \frac{v_d[(R_b + r'_{bl}) + R(\beta_2\gamma + \beta_1 + 1)] - v_1[R_b + \beta_2\gamma(R + R_o) + (\beta_1 + 1)R]}{r_{bl}(R + R_o) + R_b R_o + R_o R(\beta_1 + 1)} - \frac{\beta_2 v_2 \gamma}{R_c}$$

(Eqn. 3.11)

These first three regions, Region A, B, and C, are equivalent to Region I of the simplified analysis.

Region D is defined by conduction of Q_1, Q_2, and D; V(D) occurs when Q_2 becomes cut off. Figure 3.14 shows the equivalent circuit which applies in this region.

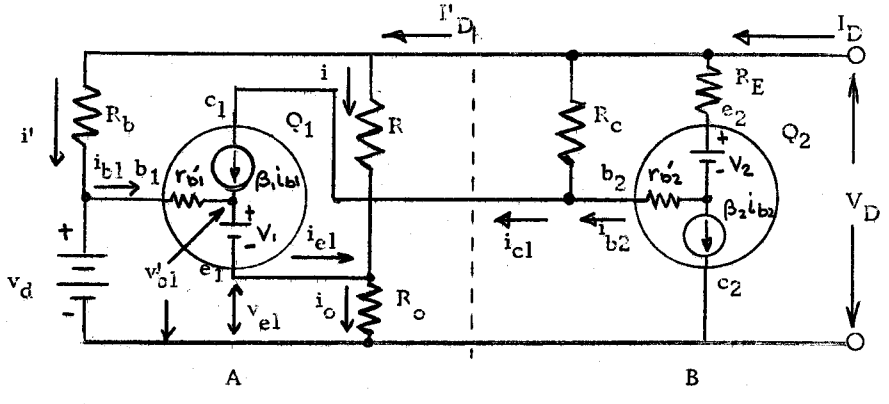


Figure 3.14. Region D equivalent of Figure 3.10.

The circuit equations for Figure 3.14b are identical to those given for Region C; for Figure 3.14a the equations are the same except that:

$$I' = i + i' \qquad \text{and} \qquad i' = \frac{V_D - v_d}{R}$$

Solving the new set of equations for I_D and R_D gives:

$$I_D = \frac{V_D[r'_{b1}(R+R_o+R_b) + RR_o(\beta_1+1) + R_oR_b(1-\beta_1\beta_2\gamma)]}{R_b[r'_{b1}(R+R_o) + RR_o(\beta_1+1)]}$$

$$- \frac{v_d[r'_{b1}(R+R_o) + RR_o(\beta+1) - \beta_1\beta_2\gamma R_b(R+R_o) - R_b(\beta_1 R - R)}{R_b[r'_{b1}(R+R_o) + RR_o(\beta_1+1)}$$

$$- \frac{v_1[(R+R_o)\beta_1\beta_2\gamma + R_b(\beta_1 R - R_o)}{r'_{b1}(R+R_o) + RR_o(\beta_1+1)} - \frac{\beta_2 v_2 \gamma}{R_c} \qquad \text{(Eqn. 3.12)}$$

$$R'_D = \frac{R_b[r'_{b1}(R+R_o) + RR_o(\beta_1+1)]}{r'_{b1}(R+R_o+R_b) + RR_o(\beta+1) + R_oR(1-\beta_1\beta_2\gamma)} \qquad \text{(Eqn. 3.13)}$$

where γ is given by Equation 3.9.

From the equivalent circuit, it can be seen that, with the diode conducting, the dynamic resistance, R'_D, would be composed of R_b in parallel with a second resistance. Using the notation $\|$ to indicate "in parallel with", R'_D may be written as:

$$R'_D = R_b \,\|\, -\frac{r'_{b1}(R+R_o) + RR_o(\beta_1+1)}{R_o(\beta_1\beta_2\gamma - 1) - r'_{b1}} \qquad \text{(Eqn. 3.13a)}$$

The upper boundary of the region occurs at V(D) where the collector current of Q_1 has dropped to $i_{b1} = \frac{V_2}{\beta_1 R_c}$ and Q_2 is cut off. Solving for V(D) and the corresponding current, I(D), gives:

$$V(D) = (v_d - v_1)\left(1+\frac{R}{R_o}\right) - \frac{v_2}{\beta_1 R_c}\left[R(\beta_1+1)+r'_{b1}\left(1+\frac{R}{R_o}\right)\right] \quad \text{(Eqn. 3.14)}$$

$$I(D) = \frac{1}{R_o R_b}\left\{v_d(R_b+R) - v_1(R+R_o+R_b) - \frac{v_2}{\beta_1 R_c}\left[r'_{b1}(R+R_o+R_b)\right.\right.$$

$$\left.\left. + R_o(R_b+R(\beta_1+1))\right]\right\} \quad \text{(Eqn. 3.15)}$$

Region E is defined by conduction of D and Q_1 but Q_2 cutoff. The upper limit of V occurs when Q_1 is cut off. Figure 3.15 shows the equivalent circuit for this region. The circuit equations for Figure

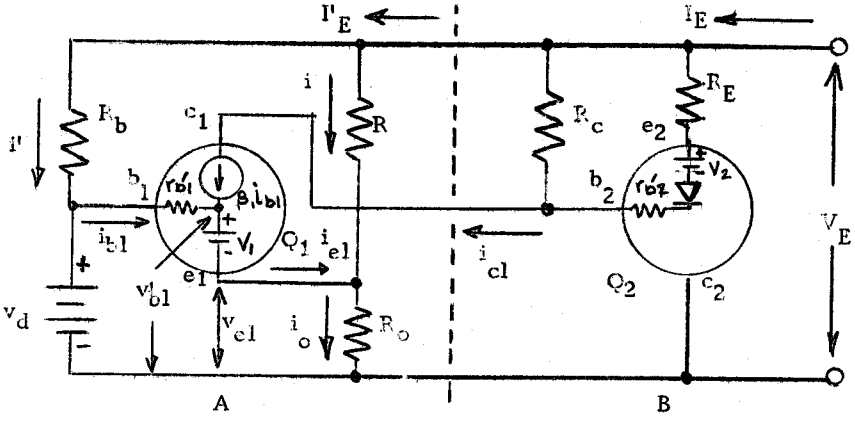


Figure 3.15. Region E equivalent of Figure 3.10.

3.15a are identical to those for Region D; those for Figure 3.15b are the same, also, except that

$$i_{b2} = 0 \qquad I = I' + i_{cl}$$

Solving the appropriate equations for I_E and R'_E gives:

$$I_E = \frac{V_E\left[r'_{b1}(R+R_o+R_b)+R_o R_b+R_o(\beta_1+1)R\right] - v_1 R_b(\beta_1 R - R_o)}{R_b\left[r'_{b1}(R+R_o)+(\beta_1+1)RR_o\right]}$$

$$- \frac{v_d[r'_{bl}(R+R_o)+RR_o(\beta_1+1)-\beta_1 RR_b + R_bR_o]}{R_b[r'_{bl}(R+R_o)+(\beta_1+1)RR_o]} \qquad \text{(Eqn. 3.16)}$$

$$R'_E = \frac{R_b[r'_{bl}(R+R_o)+(\beta_1+1)RR_o]}{r'_{bl}(R+R_o+R_b)+R_oR_b+RR_o(\beta_1+1)} \qquad \text{(Eqn. 3.17)}$$

Again, expecting R'_E to be composed of R_b in parallel with another resistance, R'_E can be written as:

$$R'_E = R_b \frac{r'_{bl}(R+R_o)+RR_o(\beta_1+1)}{r'_{bl}+R_o} \qquad \text{(Eqn. 3.17a)}$$

V(E), the upper boundary of the region occurs when the base current of Q_1 drops to zero and Q_1 is cut off. Solving for V(E) and the corresponding current, I(E), gives:

$$V(E) = (v_d - v_1)\left(1+\frac{R}{R_o}\right) \qquad \text{(Eqn. 3.18)}$$

$$I(E) = (v_d - V_1)\frac{R+R_b}{R_oR_b} - v_1\frac{1}{R_b} \qquad \text{(Eqn. 3.19)}$$

Region F is defined by conduction of D and cutoff of both Q_1 and Q_2; there is no upper bound except as restricted by component breakdown or diode power dissipation. The equivalent circuit for the region is given by Figure 3.16. The equations relating the voltages and currents for Figure 3.16 are:

$$I = i + i' \qquad V = (R+R_o)i \qquad (V-v_d) = i'R_b$$

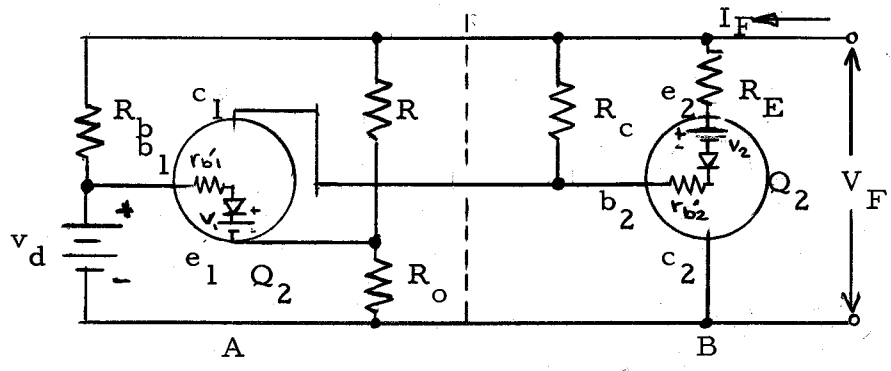


Figure 3.16. Region F equivalent of Figure 3.10.

Solving these equations for I_E and R'_E gives:

$$I_E = \frac{V - V_d}{R_b} + \frac{V_E}{R + R_o} \qquad \text{(Eqn. 3.20)}$$

$$R'_F = R_b \quad (R + R_o) \qquad \text{(Eqn. 3.21)}$$

There is no V(F) or I(F).

Region E and Region F are equivalent to Region III of the simplified analysis.

The results of this analysis may be represented by the input characteristic curve shown in Figure 3.17.

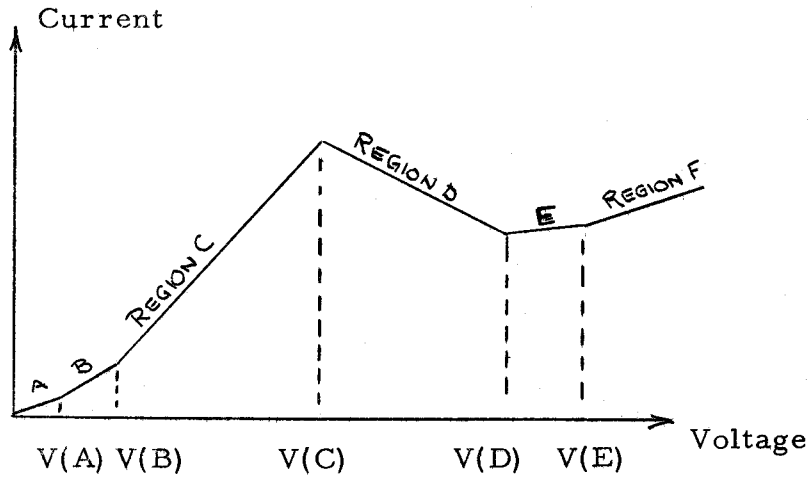


Figure 3. 17. Detailed input characteristic curve.

3. 3 Design Procedure

Usually the region of primary interest will be the negative-resistance region, Region D. Consequently, the circuit parameters would be determined from one of the following five sets of specifications:

$V(C),\ R'_D,\ V(D),\ I(D)$ or

$V(C),\ I(C),\ V(D),\ I(D)$ or

$V(C),\ I(C),\ V(D),\ R'_D$ or

$V(C),\ I(C),\ R'_D,\ I(D)$ or

$R'_D,\ I(C),\ V(D),\ I(D)$

These five sets, however, are all equivalent because the five parameters are all related by the expression

$$-R'_D = \frac{V(D) - V(C)}{I(C) - I(D)} \qquad \text{(Eqn. 3. 23)}$$

The most useful set of specifications from the design standpoint is V(C), R'_D, V(D), and I(D) because of the nature of the equations involved.

If it is assumed that r'_{b1} is small enough to be neglected, (its value is usually less than 1000Ω), and that β_1 and β_2 are large enough so that $(\beta+1)\approx\beta$, then Equations 3.10, 3.13a, 3.14, and 3.15 may be written approximately as:

$$V(C) \approx \frac{v_d[R_b(R+R_o)+\beta_1 RR_o] - v_1 R_b(R+R_o)}{RR + RR} \qquad \text{(Eqn. 3.10')}$$

$$R'_D \approx R_b \,\|\, -R\,\frac{\beta_1+1}{\beta_1\beta_2\gamma-1} \qquad \text{(Eqn. 3.13'a)}$$

$$V(D) \approx (v_d - v_1)\left(1+\frac{R}{R_o}\right) - v_2\,\frac{R}{R_c} \qquad \text{(Eqn. 3.14')}$$

$$I(D) \approx \frac{I}{R_o R_b}\left[v_d(R_b+R) - v_1(R+R_b+R_o) - v_2\,\frac{R_o}{\beta_1 R_c}(R_b+\beta_1 R)\right] \qquad \text{(Eqn. 3.15')}$$

To insure that transistor Q_1 never becomes saturated, the limitation, $R_b \geq \beta_1 R_c$, must be placed on R_c. If the equality is assumed, the solution of the preceeding four equations yields:

$$R_b = \frac{1}{I(D)}\left\{V(D)\left[\frac{V(D)-V_d}{V(D)-V(C)}\right] + \left[V(D) - v_d + v_1 - v_2\right]\left[\frac{V(C)-v_d}{V(D)-V(C)}\right]\right\} \qquad \text{(Eqn. 3.24)}$$

$$R_c = \frac{R_b}{\beta_1} \qquad \text{(Eqn. 3.25)}$$

$$R = R_c \frac{V(D) - V(C)}{V(C) - v_d - v_1} \qquad \text{(Eqn. 3.26)}$$

$$R_o = R_c \frac{[V(D) - V(C)][(v_d - v_1)]}{[V(C) - v_d][V(D) - v_d - v_2] + v_1[V(C) - v_d - v_2]} \qquad \text{(Eqn. 3.27)}$$

$$R_E = \frac{R_c}{\frac{R}{R_b}(1 + \frac{R_b}{R'_o}) + \frac{1}{\beta_1}} - \frac{R_c + r'_{b2}}{\beta_2} \qquad \text{(Eqn. 3.28)}$$

Using the design equations, Equations 3.24 through 3.28, the design procedure would follow the following steps:

Step 1: Choose the breakdown diode. Its breakdown voltage must be less than V(C) because V(C) is always greater than v_d. The diode should also have a sharply defined break down; otherwise, the transition at V(C) will be rounded instead of sharp.

Step 2: Choose the transistors, one NPN and one PNP. Their selection will determine v_1, v_2, β_1, β_2, r'_{b1}, and r'_{b2}. Guidelines for choosing Q_1 and Q_2 are:

(a). Breakdown voltage of Q_2 larger than V(D).

(b). Current rating of Q_2 at least $I(D) + \frac{V(D) - V(C)}{R'_D}$.

(c). Breakdown voltage of Q_1 at least $V(D) - v_d$.

Step 3: Using specifications and component parameters from preceeding step, determine component values from Equations 3.24 through 3.28.

Step 4: Minimum value of R_b is limited by maximum power

dissipation of the breakdown diode since the power dissipated, $P_d(D)$, at $V(D)$ is $\frac{v_d}{R_b}[V(D)-v_d]$. If the power is greater than the rated power of the diode, a larger R_b must be used; it is usually easiest to reduce $I(D)$ to make R_b larger. This completes the design procedure.

The magnitude of the negative resistance may easily be controlled by changing R_E since R_E effects only $I(C)$ (or R'_D).

IV. EXPERIMENTAL CONTROLLED NEGATIVE RESISTANCE

4.1 Design

The design procedure presented in Section III is illustrated by the realization of the following set of specifications:

A negative resistance of -2000Ω is to be produced. Break points are to be at 11 volts and 20 volts. It is to be biased midway between breakpoints at 5 milliamps.

The specifications should first be restated in standard form by determining I(D) which is 5 ma. - $\frac{5v.}{2K\Omega}$ or I(D) = 2.75 ma.

Step 1: Choose a 10.0 volt, 100 milliwatt zener diode.

Step 2: Choose a 2N706 for Q_1 and an ST8034 for Q_2. The first is an NPN transistor; the second, a PNP. The ST8034 is 600 mw, 25 volt silicon transistor with a beta of 90 at 10 volts and 7.5 ma.; the 2N706 is a silicon 300 mw, 20 volt transistor with a beta of 90 at 9 volts and 1 ma. There will be no problem on either power limitations or voltage breakdown for either transistor.

Step 3: Design equations give:

$$R_b = 50.0 \text{ K}$$

$$R_c = 556 \text{ ohms}$$

$$R = 12.5 \text{ K}$$

$$R_o = 5.13 \text{ K}$$

$$R_E = 69.4 \text{ ohms}$$

Step 4: There will be no problem with zener power dissipation since power dissipation at V(D) will be 2 mw.

4. 2 Performance

A circuit using the components listed in the preceeding section was constructed in the laboratory. Actual circuit values and circuit performance is tabulated in Table 4. 1 and typical characteristic curves for the circuit are shown in Figure 4. 1.

TABLE 4. 1. CIRCUIT DESIGN AND PERFORMANCE.

Quantity	Design Values	Realized Values
R_b	50. 0 K	50. 0 K, 1%
R_c	556	554 1%
R	12. 5 K	12. 5 K 1%
R_o	5. 13 K	5. 13 K 1%
R_E	69. 4	70. 0 Ω 1%
V_z	10. 0 v	10. 05 v
V(C)	11. 0 v	11. 0 v
V(D)	20. 0 v	20. 0 v
I(D)	2. 75 ma	2. 1 ma
R'_D	-2. 0 K	-2. 3 K

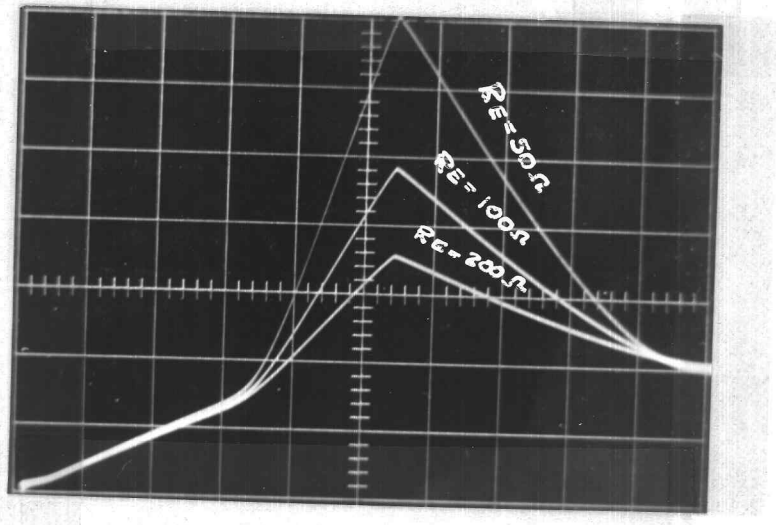


Figure 4. 1. Experimental characteristic curve.

The error in I(D) is due primarily to the assumption that r'_{b1} is zero; this assumption had to be made to obtain useful design equations and it is a reasonable assumption when significant base current flows, as, for example, at V(C). At V(C) with the circuit designed, r'_{b1} is about 500 Ω which is quite insignificant compared to R_b. But, as the base current decreases while changing V from V(C) to V(D), r_{b1} increases considerably, particularly as the base-emitter voltage approaches v_1.

A second major factor contributing to errors is the variation of β_1 and β_2; both are functions of the collector current and the collector-emitter voltages of the respective transistors. For example, in a typical 2N706, beta increases from 110 to 153 when the collector current is increased from 0. 1 to 1. 0 ma at a collector voltage of 4 v.

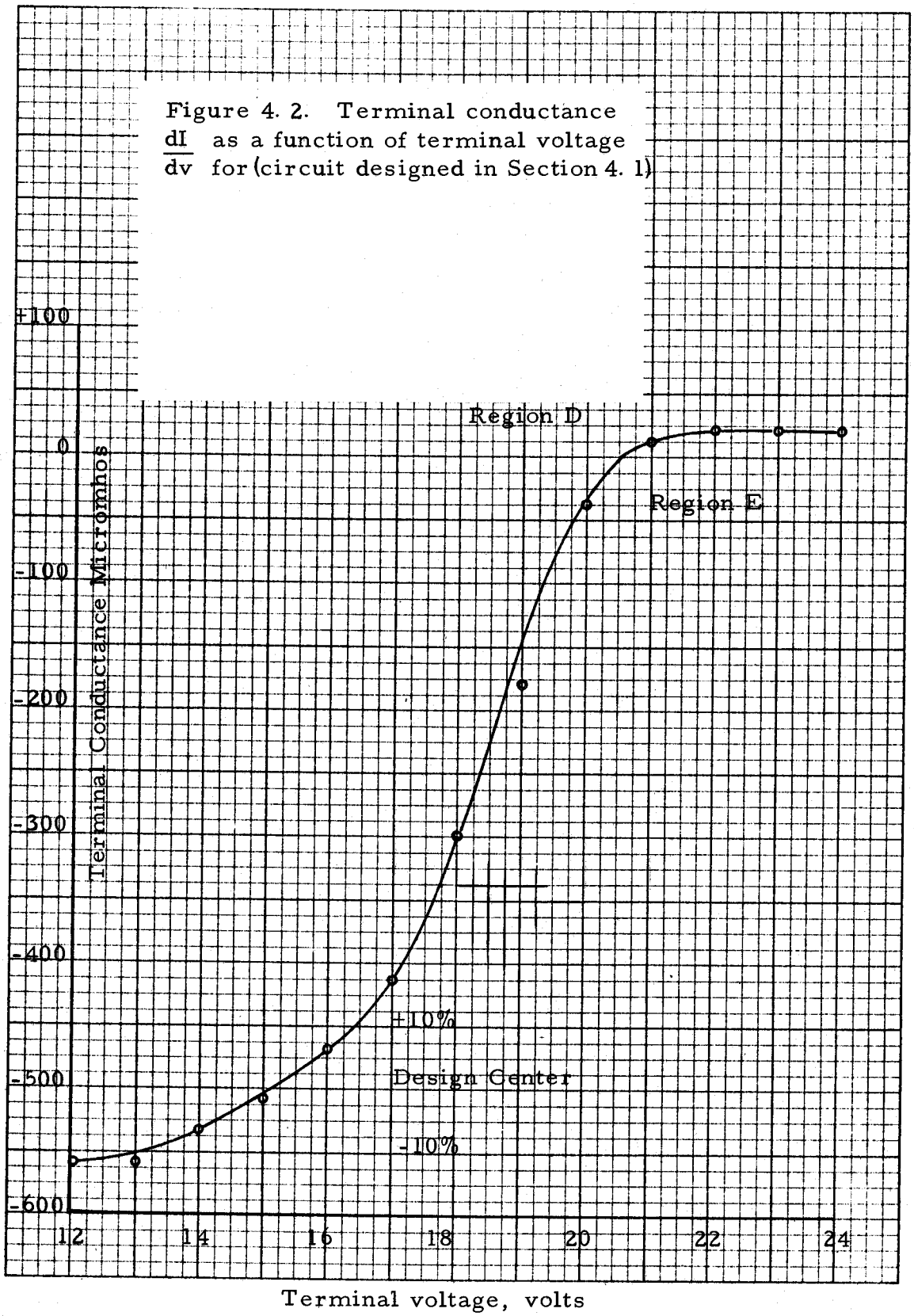
4. 3 Secondary Considerations

The linearity of R'_D (Equation 3. 13a) can be of major importance in network applications, particularly when large signals are to be handled. For the reasons indicated in the preceeding section, linearity is best near V(C). Decreases in both β_1 and β_2 and increases in both r'_{b1} and r'_{b2} contribute to nonlinearity at low currents. Linearity could undoubtedly be improved by a different choice of transistors. Figure 4. 2 shows the variation of $G'_D = (R'_D)^{-1}$ for the circuit designed in Section 4. 1.

The variation of R'_D with frequency is also a major consideration in network applications. Figure 4. 3 shows measured values of $G'_D = (R'_D)^{-1}$ and its associated susceptance, jB'_D, for a circuit similar to that designed in Section 4. 1; while the measured circuit was not absolutely identical, similar results could be expected.

Shunt capacitance may, or may not, be a problem in network applications. Most negative-resistance synthesis techniques take into account shunt capacitance. At frequencies below about 500 kc., the circuit measured in Figure 4. 3 has an equivalent shunt capacitance of approximately 100 pf. Usually the shunt capacitance required for network synthesis is greater by several orders of magnitude than that supplied by the circuit and shunt capacitance must be added. If the required shunt capacitance is less than that provided, it may be

Figure 4. 2. Terminal conductance $\frac{dI}{dv}$ as a function of terminal voltage for (circuit designed in Section 4. 1)



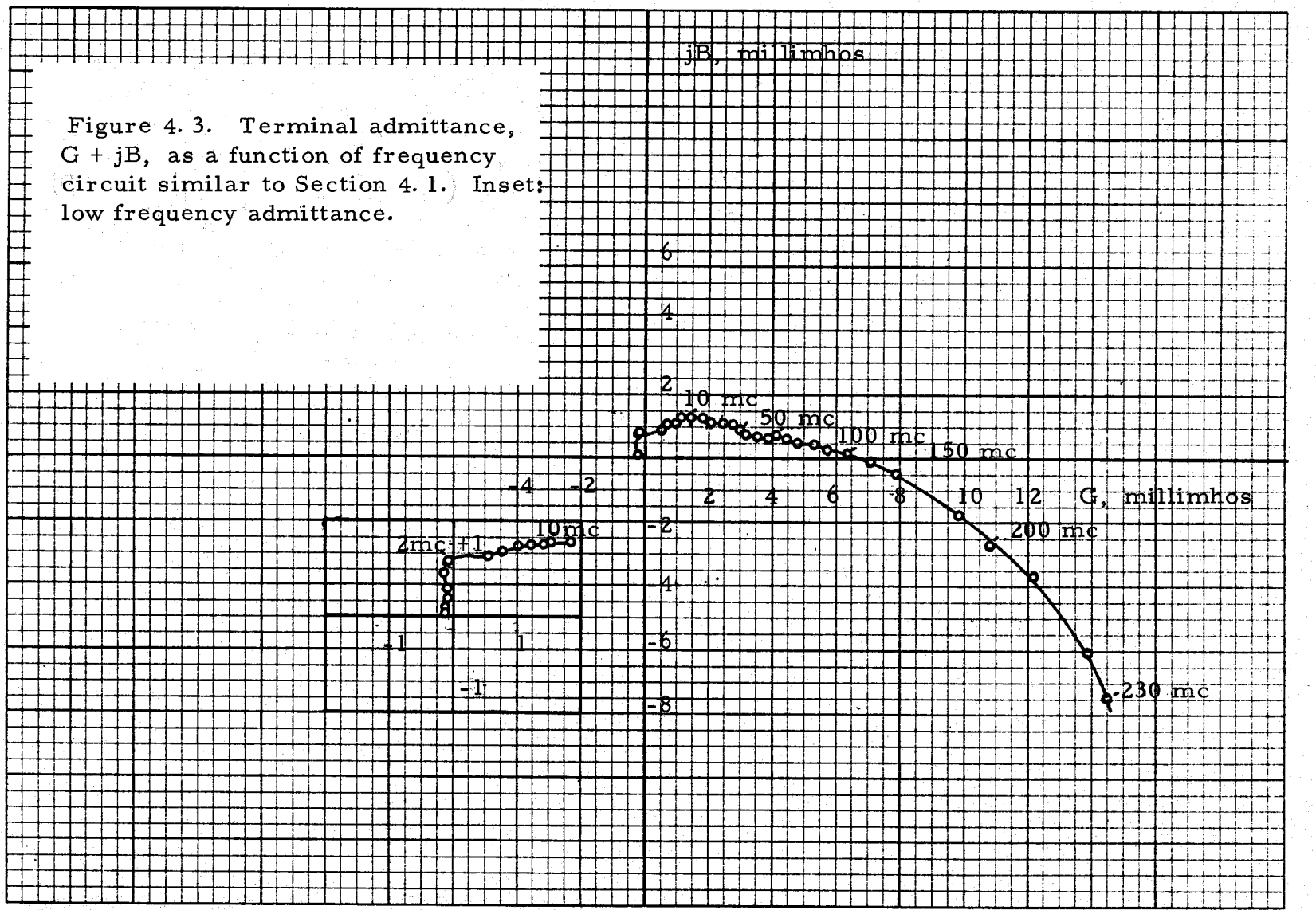


Figure 4. 3. Terminal admittance, G + jB, as a function of frequency circuit similar to Section 4. 1. Inset: low frequency admittance.

cancelled out, but only for a small frequency range, by shunting the resistor R, (see Figure 3.8, p.9), with a capacitance. That this will cancel the output capacity may be seen from Equation 3.13a:

$$R'_D = R_b - \frac{r'_{bl}(R+R_o)+RR_o(\beta_1+1)}{R_o(\beta_1\beta_2\gamma-1)-r'_{bl}}$$

which indicates that the circuit may also be considered as a negative impedance converter of the form given in Figure 4.4.

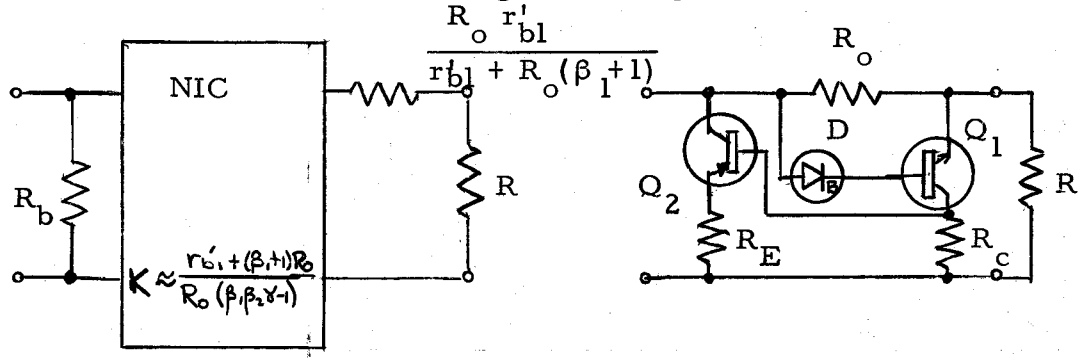


Figure 4.4a. Negative-impedance converter equivalent.

Figure 4.4b. A reorientation of Figure 3.8 to emphasize negative-impedance converter form

The compensation of the input capacitance will occur at only one frequency because of the "stray" resistance in series with R; although this undesired resistance cannot be removed by compensation as in many NIC's, it can be made small by making β_1 large.

Oscillation may occur in the upper part of Region C, particularly in breadboard circuits, where layout and lead lengths often are less

than ideal,especially if high frequency transistors are used. This condition may usually be prevented by placing a ferrite "suppressor" bead on either or both the collector and base leads of Q_2. Although the oscillation is usually too high to be seen on a curve tracer, it is revealed by a distortion of the traced curve with the distortion being effected by hand capacity near the circuit. Figure 4. 5a shows the distortion produced by such oscillation and Figure 4. 5b shows the curve after application of the suppressor beads.

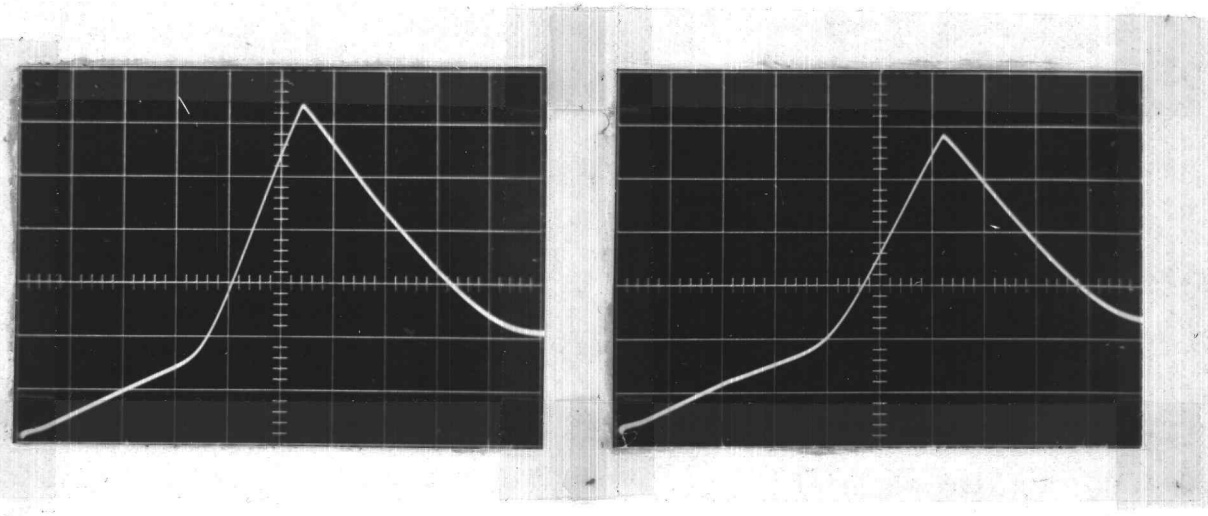


Figure 4. 5a. Effect of high frequency oscillation on the characteristic curve.

Figure 4. 5b. Same circuit as Figure 4. 3a with addition of suppressor beads.

V. NEGATIVE RESISTANCE SYNTHESIS TECHNIQUES

5. 1 Background

Synthesis with negative resistances gives several advantages over conventional passive network synthesis; higher gain constants may be realized than possible with transformerless networks, and pole-zero arrays impossible with passive synthesis may be realized with negative resistances.

A considerable number of negative-resistance synthesis techniques have been developed but most are either quite complex or require a large number of negative resistances. A paper by Losee and Mitra (6, p. 357-62) presents a set of realization techniques using simple adaptations of RC-ladder synthesis methods. Several of those techniques are outlined to provide a background for the experimental realizations presented in Chapter VI.

As previously indicated, all negative-resistance devices also exhibit a shunt capacitance; sometimes it is small enough to be neglected, but in RC-ladder synthesis it is an advantage.

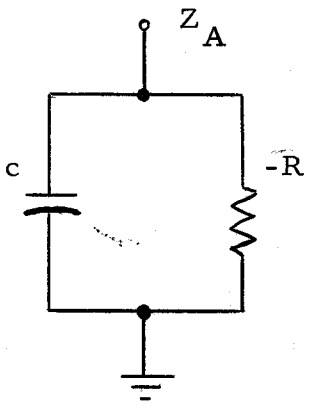


Figure 5. 1a. Negative resistance equivalent circuit.

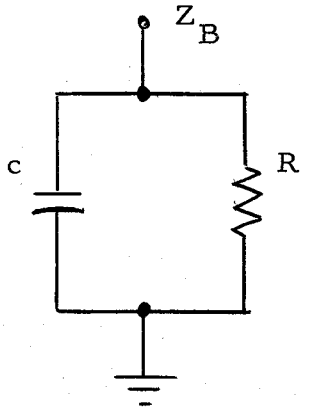


Figure 5. 1b. Passive parallel RC circuit.

The negative-resistance equivalent shown in Figure 5. 1a has an impedance, $Z_a(s)$, of:

$$Z_a(s) = \frac{1}{sC - \frac{1}{R}}$$

$$= \frac{1}{C} \frac{1}{s - \frac{1}{RC}} \qquad \text{(Eqn. 5. 1a)}$$

while the parallel RC circuit in Figure 5. 1b has an impedance, $Z_b(s)$, of:

$$Z_b(s) = \frac{1}{sC + \frac{1}{RC}}$$

$$= \frac{1}{C} \frac{1}{s + \frac{1}{RC}} \qquad \text{(Eqn. 5. 1b)}$$

The comparison of Equations 5. 1a and 5. 1b indicate that the circuit

of Figure 5. 1a can be used to realize positive real impedance poles in the same way parallel RC combinations are used to realize negative real impedance poles.

5. 2 Larger RC Ladder Gain Realizations

The use of a negative resistance to realize transfer functions usually realizable with passive RC-ladders gives larger gain factors than possible with the passive ladder; sometimes a net gain may even be realized. The procedure is outlined in the following steps and is illustrated in Figure 5. 2, page .

Step 1: Given an RC open-circuit voltage-transfer function, $G_{12}(s) = E_{out}/E_{in} = N(s)/P(s) = \prod_{i=1}^{m} (s + \sigma_i)/\prod_{j=1}^{n} (s + Z_j)$. Since G_{12} is an RC-transfer function, σ_i and Z_j are real, positive and $m \leq n$. The following procedure requires a transmission zero at infinity, making the condition on m and n a strict inequality, $m < n$.

Step 2: Using the relationship between open-circuit voltage-transfer functions and the "z" parameters of a network, $G_{12} = z_{12}/z_{11}$, form $z_{11} = P(s)/Q(s)$ and $z_{12} = N(s)/Q(s)$ with Q(s) of the form:

$$Q(s) = (s - a) \prod_{k=1}^{n-1} (s + p_k)$$

such that a and p_k are real positive and that $0 < z_1 < p_1 < z_2 < \ldots < z_n < \infty$. Note that the usual statement that "the critical frequency nearest the origin is a pole for RC impedances" must be modified for RC

impedances containing negative resistances to " the most positive critical frequency is a pole for $\pm$ RC impedances." The pole-zero configurations for z_{11} and z_{12} are shown in Figure 5. 2a.

Step 3: Subtract a 1Ω resistor from z_{11}. According to the assumed form for z_{11}, the leading coefficients of both P(s) and Q(s) are unity; thus, $z_{11}(\infty)$ is unity and removal of 1Ω from z_{11} shifts the highest zero of z_{11} to infinity. This operation is shown in Figure 5. 2b. The remainder impedance, z_o, is given by:

$$z_o = z_{11} - 1 = \frac{\prod_{j=1}^{n}(s + z_i)}{(s-a)\prod_{k=1}^{n}(s+p_k)} - 1$$

$$= \frac{\prod_{j=1}^{n}(s+z_i) - (s-a)\prod_{k=1}^{n-1}(s+p_k)}{(s-a)\prod_{k=1}^{n-1}(s+p_k)}$$

Step 4: Form $y_o = 1/z_o$ and shift the zero of y_o at a to the origin by removing $G_o = y_o(o)$;

$$G_o = \frac{1}{z_o(o)} = \frac{-a\prod_{k=1}^{n-1} p_k}{a\prod_{j=1}^{n} z_j + a\prod_{k=1}^{n-1} p_k}$$

Note that G_o is negative. The pole-zero plot for this step is shown in Figure 5. 2c. The remainder admittance, $y'_o = y_o - G_o$, is given by:

$$y'_o = \frac{(s-a)\prod_{k=1}^{n-1}(s+p_k)}{\prod_{j=1}^{n}(s+z_j)-(s-a)\prod_{k=1}^{n-1}(s+p_k)} - \frac{-a\prod_{k=1}^{n-1}p_k}{\prod_{j=1}^{n}z_j + a\prod_{k=1}^{n-1}p_k}$$

$$= \frac{(s-a)\prod_{k=1}^{n-1}(s+p_k)(\prod_{j=1}^{n}z_j) + a(\prod_{k=1}^{n-1}p_k)\prod_{j=1}^{n}(s+z_j)}{[\prod_{j=1}^{n}(s+z_j)-(s-a)\prod_{k=1}^{n-1}(s+p_k)][\prod_{j=1}^{n}z_j + a\prod_{k=1}^{n}p_k]}$$

Step 5: Remove the pole of y'_o at infinity to realize the shunt capacity associated with G_o. The need for this capacitance shunting G_o is the reason for requiring a transmission zero at infinity. Expanding both the numerator and denominator of y'_o in polynomial form, the coefficient of the term of the highest degree of the numerator, a_n, is

$$a_n = \prod_{j=1}^{n} z_j + a\prod_{k=1}^{n-1} p_k$$

and the coefficients of the two highest degree term of the demoninator, b_n and b_{n-1}, are:

$$b_n = \prod_{j=1}^{n} z_i + a\prod_{k=1}^{n-1} p_k - [\prod_{j=1}^{n} z_j + a\prod_{k=1}^{n-1} p_k] = 0$$

$$b_{n-1} = [\prod_{j=1}^{n} z_j + a\prod_{k=1}^{n-1} p_k][\sum_{y=1}^{n} z_j - \sum_{k=1}^{n-1} p_k + a]$$

Carrying out only the first step of the synthetic division of the numerator by the denominator of y'_o and calling the remainder $y_r(s)$:

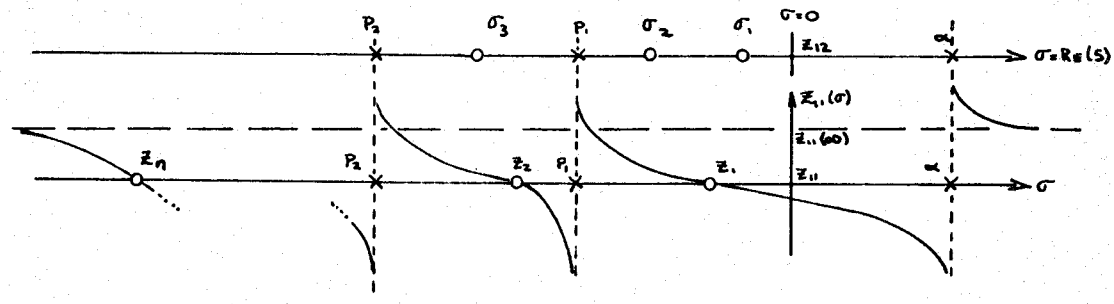


FIG. 5.2a. INITIAL POLE-ZERO CONFIGURATION FOR R-C TRANSFER WITH GAIN. SEE STEP 2. P.29

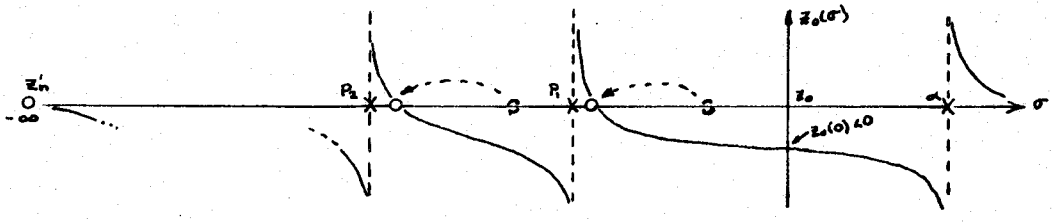


FIGURE 5.2b. REMOVAL OF 1Ω FROM Z_{11} TO FORM Z_0 WITH A ZERO AT INFINITY

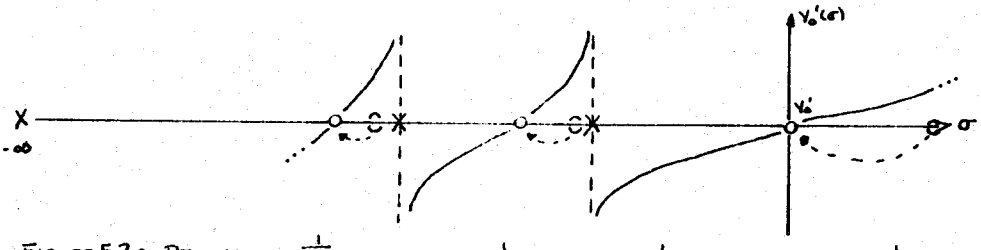


FIGURE 5.2c REMOVAL OF $\frac{1}{Z_0(0)}$ FROM $Y_0 = \frac{1}{Z_0}$ TO FORM Y_0' AND TO REALIZE $G_0 = \frac{1}{Z_0(0)}$

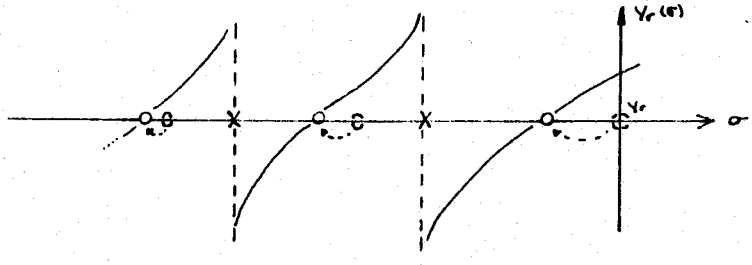


FIGURE 5.2d REMOVAL OF POLE AT INFINITY TO REALIZE G_∞

FIGURE 5.2 POLE-ZERO CONFIGURATIONS ILLUSTRATING PROCEDURE FOR REALIZING RC TRANSFER FUNCTIONS WITH GAIN

$$y'_o = \frac{s}{\sum_{j=1}^{n} z_j - \sum_{k=1}^{n-1} p_k + a} + y_r(s)$$

so that a shunt capacitance, $C_o = (\sum_{j=1}^{n} z_j - \sum_{k=1}^{n-1} p_k + a)^{-1}$, may be realized. This step is shown in Figure 5. 2d.

Step 6: Realize the remaining transmission zeros with conventional RC-ladder procedure. The remainder admittance, $y_r(s)$, is usually most easily determined numerically at this point from $y_r = y_o - G_o - sC_o$. The network form at this step is given in Figure 5. 3.

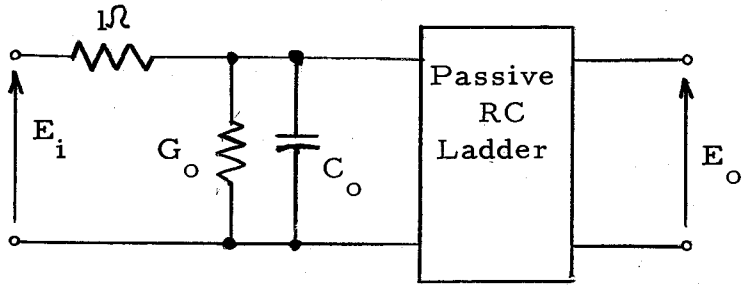


Figure 5. 3. Network form for realizing RC $G_{12} = \frac{E_o}{E_i}$ with gain.

5. 3 Nonminimum-phase RC Transfer Functions

Nonminimum-phase RC-transfer functions are characterized by having positive real zeros. Realization is directly analogous to standard RC-ladder techniques, and is best described by example:

Step 1: Given $G_{12} = E_o/E_i = \frac{(s+5)(s-1)}{(s+2)(s+4)}$

Step 2: Using the open-circuit transfer relationship or

$G_{12} = -y_{12}/y_{22}$, choose $-y_{12}$ and y_{22} with negative real poles interlaced with zeros of y_{22}:

$$y_{22} = \frac{(s+2)(s+4)}{(s+3)(s+6)}$$

$$-y_{12} = \frac{(s-1)(s+5)}{(s+3)(s+6)}$$

Pole-zero plots are given in Figure 5. 4.

Step 3: Shift the most positive zero of y_{22} to coincide with one of the positive zeros of $-y_{12}$, at σ_1. This is accomplished by removing $y_{22}(\sigma_1)$ from y_{22}; it should be noted that $y_{22}(\sigma_1)$ is greater than $y_{22}(o)$; removal of $y_{22}(o)$ will shift the zero to the origin but removal of a conductance greater than $y_{22}(o)$ is required to shift a zero to the positive real axis. In this case, the zero at $\sigma = -2$ is shifted to $\sigma = +1$ by removal of 15/28 mhos.

Step 4: Realize the positive transmission zero as a pole of $Z = [y_{22}(s) - y_{22}(\sigma)]^{-1}$ by removing a parallel combination of a negative resistance and a capacitance. In this example:

$$Z = \frac{(s+3)(s+6)}{(s-1)(s+\frac{46}{13})} = \frac{\frac{364}{59}}{(s-1)} + \frac{\frac{85 \cdot 124}{13 \cdot 33}}{(s+\frac{46}{13})}$$

The pole at s = 1 is then realized by a capacitor of 59/364 farads in parallel with a -364/59 ohm resistor.

Step 5: The procedure outlined in steps 3 and 4 is repeated for

each positive transmission zero; the remaining zeros are realized conventionally. Obviously this procedure requires one negative resistor for each positive zero. The resulting network form is given in Figure 5. 5.

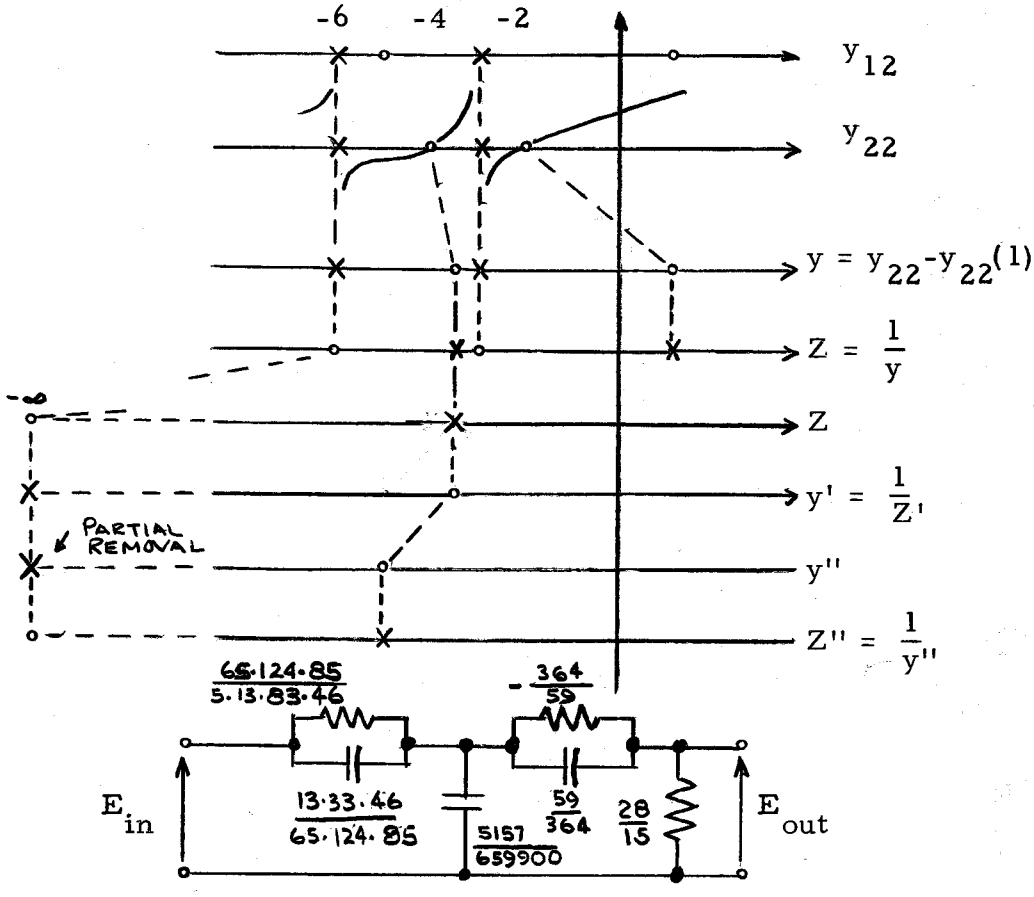


Figure 5. 4. Pole zero plot for example of section 5. 3.

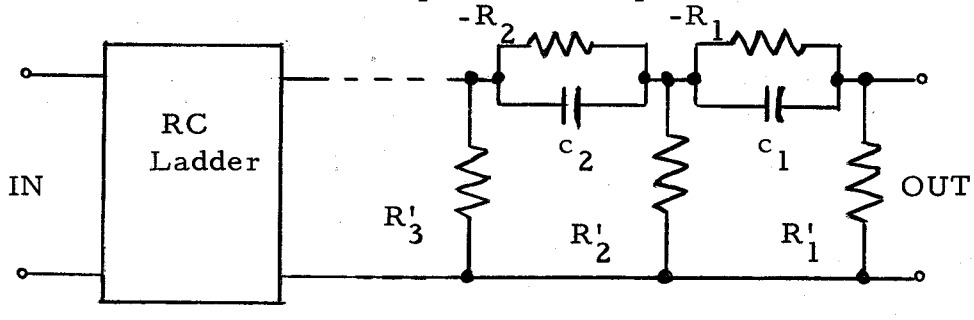


Figure 5. 5. General form for nonminimum-phase transfer.

5. 4 Arbitrary Zero of Transmission

Arbitrary zeros of transmission with negative real poles may be realized by two parallel two-ports of the form shown in Figure 5. 6.

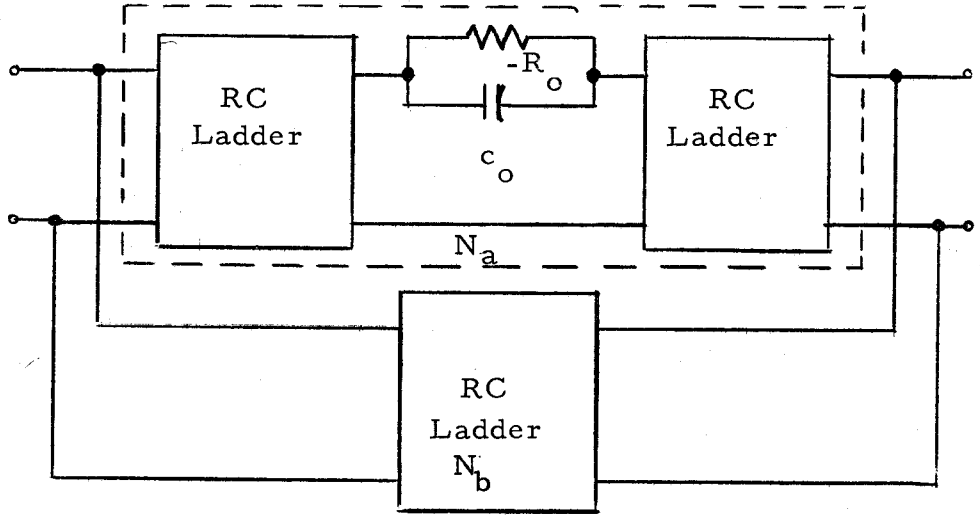


Figure 5. 6. Network form for arbitrary zero realization.

The technique is based in the fact that any arbitrary polynomial with a positive leading coefficient may be written as the sum of one polynomial with negative real zeros only and one polynomial with one positive real zero and all other zeros negative real (6, p. 361). Or, expressed algebraicly:

$$\sum_{n=1}^{k} a^n s^n = (s-\alpha) \prod_j (s+\sigma_j) + \prod_j (s+\sigma_i)\, a_k ; \alpha ; \sigma_i ; \sigma_j \text{ real positive}$$

(Eqn. 5. 2)

Since, for two parallel two-ports, N_a and N_b, with admittance parameters $[y^a]$ and $[y^b]$, the admittance $[Y]$ of the combined network, N, is the sum of the admittances of the parallel networks,

$[Y] = [y^a] + [y^b]$, the open-circuit voltage-transfer function of the network, N, may be written:

$$G_{12} = \frac{-Y_{12}}{Y_{22}} = \frac{-y^a_{12}\ -y^b_{12}}{y^a_{22} + y^b_{22}}$$

From the assumed configuration shown in Figure 5.6, $-y^a_{12}$ has one positive zero. Thus if G_{12} is specified with a denominator having only negative real zeros and with a numerator restricted only to having a positive leading coefficient, the numerator may be separated into two polynomials of the form given in Equation 5.2 and the terms may be associated with the admittance parameters of N_a and N_b. The procedure may be outlined as follows:

Step 1: Given - $G_{12} = H \frac{\sum^{k} a^n s^n}{(s+p_j)}$ with $a_k > 0$ and $p_j > 0$

Step 2: Separate the numerator of G_{12}:

$$G_{12} = H \frac{(s-\alpha)\prod(s+\sigma_j) + \prod(s+\sigma_i)}{\prod(s+p_j)}$$

Step 3: Associate terms with admittance parameters:

$$-y^a_{12} = \frac{(s-\alpha)\prod(s+z_j)}{Q(s)} \qquad -y^a_{12} = \frac{\prod(s+z_i)}{Q(s)}$$

$$y^d_{22} + y^b_{22} = \frac{1}{H}\frac{\prod(s+p_j)}{Q(s)}$$

If the coefficient, H, is chosen so that $\frac{1}{H}$ is two, then y^a_{22} and y^b_{22} may be easily identified as:

$$y_{22}^{a} = y_{22}^{b} = \frac{\prod(s+p_j)}{Q(s)}$$

Step 4: Actual synthesis of N_a follows the pattern outlined in Section 5.3; synthesis of N_b follows standard procedure.

5.5 Biasing

One factor seldom considered in the negative resistance synthesis problem is that of biasing.

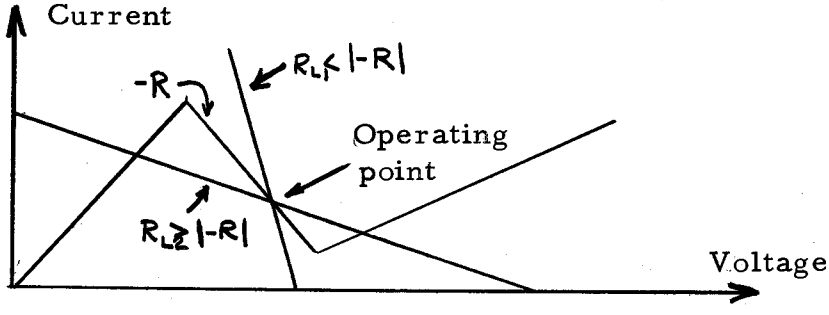


Figure 5.7. Biasing of a negative resistance.

To achieve stable bias for a negative-resistance device, the DC load-line must intersect the characteristic curve of the device only once and that intersection must be in the negative resistance region, as indicated by the line R_{L1} in Figure 5.7. Otherwise, the circuit will be stable in one of the two positive resistance regions, as indicated by the R_{L2} in Figure 5.7. The criterion of one intersection only in the negative resistance region can be met only when the effective load resistance is smaller in magnitude than the negative resistance; an equivalent condition is that the bias supply must "see" a

net negative resistance.

From a network synthesis standpoint it is desirable to be able to use a portion of the network for biasing although sometimes it is most convenient to add components for biasing. A simple example is provided by networks realized from the technique presented in Section 5.2. The DC driving-point impedance, $z_{11}(0)$, is negative as indicated in Figure 5.2a. Biasing may be provided by supplying bias current through a resistor of value less than $z_{11}(0)$ to the input terminals as shown in Figure 5.8.

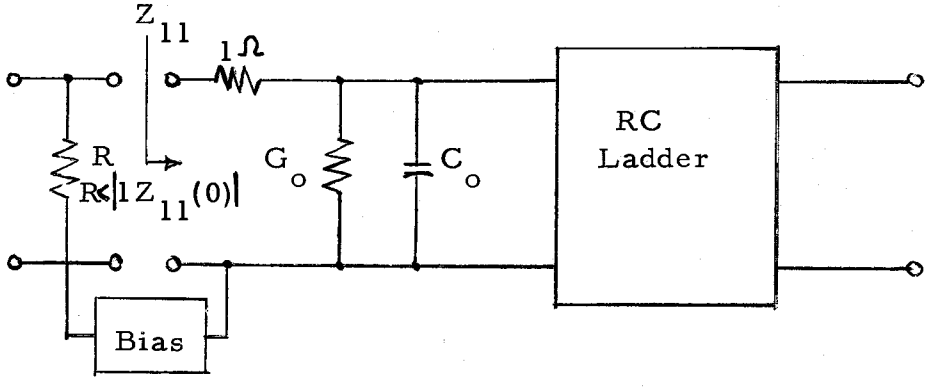


Figure 5.8. Bias scheme for Figure 5.3.

The ladder form of Figure 5.5 may be biased quite easily. Consider, first, synthesis of a ladder with one positive zero at $s = a$, $a > 0$, from a y_{22} partially diagrammed in Figure 5.9. Following the procedure previously outlined, the most positive zero is shifted to $s = a$ by removal of $y_{22}(a)$ which is greater than $y_{22}(0)$, leaving a $y_1(0)$ which is negative. After realizing the transmission zero as a pole with residue K_a, the network has the form shown in Figure 5.10.

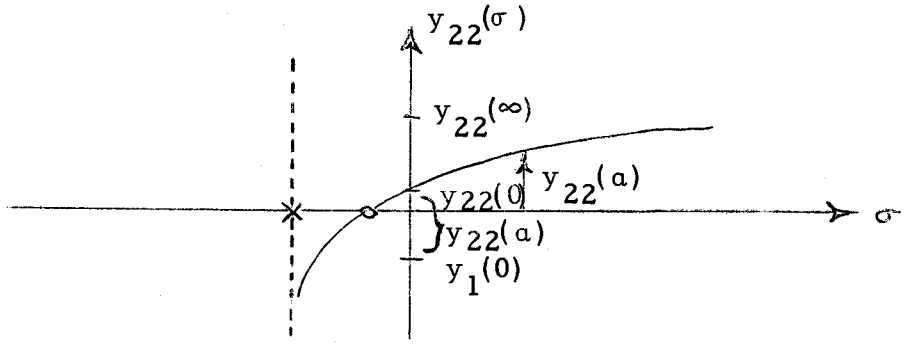


Figure 5.9. Illustration of first step to realize zero at s = a.

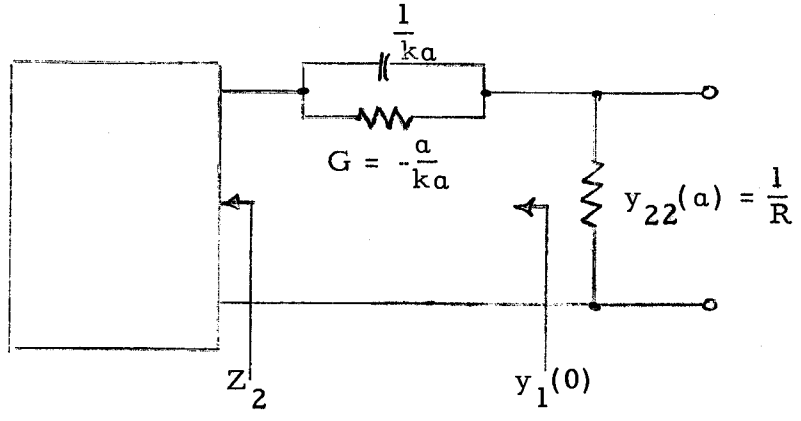


Figure 5.10. Network realization of transmission zero at s = a after first two steps.

Now, if the shunt arm $y_{22}(a)$ in Figure 5.10 is broken, the ladder may be examined for biasing possibilities. To allow biasing at this point, the resistance seen at the break must be negative, or, $\frac{1}{y_{22}(a)} + \frac{1}{y_1(0)}$. As indicated in Figure 5.9 which represents an arbitrary admittance function, $y_{22}(a) + y_1(0) > 0$ and $y_1(0) < 0$. Then manipulating the inequality:

$$y_{22}(a) > -y_1(0)$$

$$\frac{1}{y_{22}(a)} < -\frac{1}{y_1(0)} \qquad \text{since } -y_1(0) > 0$$

$$\frac{1}{y_{22}(a)} + \frac{1}{y_1(0)} < 0$$

Thus the resistance at the break is negative and bias may be applied at that point.

The procedure for biasing a ladder with a single positive transmission zero may be extended to ladders with more than one positive zero. The steps demonstrating this feasibility are shown in Figure 5.11. Figure 5.11a shows a ladder with an arbitrary number of arbitrary positive transmission zeros, recalling that after each realization of a positive zero, the remaining impedance is positive at $\sigma=0$. Figure 5.11b shows the network after breaking the first shunt leg and inserting the bias voltage. Figure 5.11c shows the result of combining the first shunt resistance and the first negative resistance; the result of this combination is negative as indicated in the preceeding paragraph. Figure 5.11d indicates the result of taking the Norton equivalent of the bias supply and the combination of the first two resistances. Figure 5.11e gives the result of finding the Thevenin equivalent of the bias source of Figure 5.11d. Since the driving-point impedance presented to the bias source does not change under successive Thevenin-Norton transformations, the driving-point impedance in Figure 5.11e is still negative and biasing is achieved. This procedure can be continued for all of the negative resistances in the network, indicating that each negative resistance may be biased through the network preceeding it.

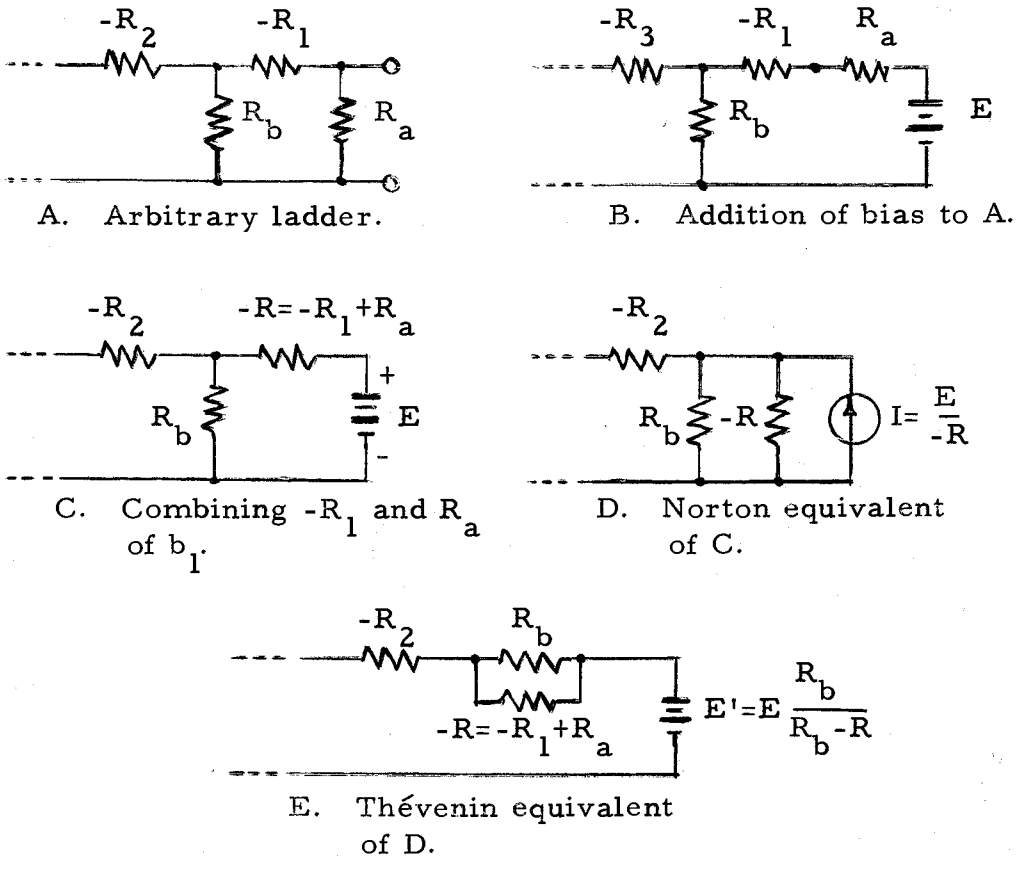


Figure 5. 11. Derivation of bias feasibility.

It should be noted that a considerable portion of the bias current will be lost in the shunt arms and that the DC voltage drop across each shunt arm is always larger than the voltage required to bias the next negative resistor. It is thus advantageous to design the negative resistances for as small a bias voltage as possible.

The network of Section 5. 4 may be biased in the same manner as the networks with positive real zeros since the portion of the network resulting from that technique is simply a ladder with one positive zero.

VI. EXPERIMENTAL NETWORK REALIZATIONS

6. 1. RC Ladder with Gain

Following the procedure outlined in Section 5. 2, a network with transfer poles at s = -1 and at s = -10 with no finite transfer zeros is desired. The synthesis proceeds in the following steps and is outlined in Figure 6. 1; the completed network is given in Figure 6. 2.

Step 1: Given -

$$G_{12}(s) = \frac{H}{(s+1)(s+10)} = \frac{N(s)}{P(s)}$$

All poles and zeros are real negative and the degree of the numerator is less than the degree of the denominator so that all criteria are met.

Step 2: Choose -

$$Q(s) = (s-2)(s+5)$$

then

$$z_{11}(s) = \frac{(s+1)(s+10)}{(s-2)(s+5)}$$

and

$$z_{12}(s) = \frac{H}{(s-2)(s+5)}$$

Step 3: Subtract one ohm from z_{11} -

$$z_{11} - 1 = 8\,\frac{(s+2)(s+5)}{(s-2)\,(s+5)}$$

Step 4: Remove $G_o = y_o(0)$ from $y_o = (z_{11} - 1)^{-1}$ -

$$y_o = \frac{1}{8} \frac{(s-2)(s+5)}{(s+2.5)}$$

and

$$G_o = \frac{1}{8} \frac{(-2)(5)}{(2.5)} = -\frac{1}{2}$$

Step 5: Remove $C_o = \left(\sum_{j=1}^{n} z_j - \sum_{k=1}^{n-1} p_k + a \right)^{-1}$ in parallel with G_o -

$$C_o = (1+10-5+2)^{-1} = \frac{1}{8}$$

Step 6: Determine $y_r = y_o - G_o - sC_o$ and continue remainder of synthesis as normal RC-ladder -

$$y_r = \frac{9}{16} \frac{s}{(s+2.5)}$$

$$z_r = \frac{1}{y_r} = \frac{16}{9} \left(1 + \frac{2.5}{s}\right)$$

The network resulting from the proceeding synthesis has a net gain of two at 2 = 0 as determined by the first two resistors in the network (Figure 6.2a). This gives a value of 20 for the gain constant, H, in Step 1; the maximum possible value of H for a passive ladder is 10.

Figure 6.3 shows a graphical comparison of the measured frequency response and the theoretical frequency response for the network shown in Figure 6.2b.

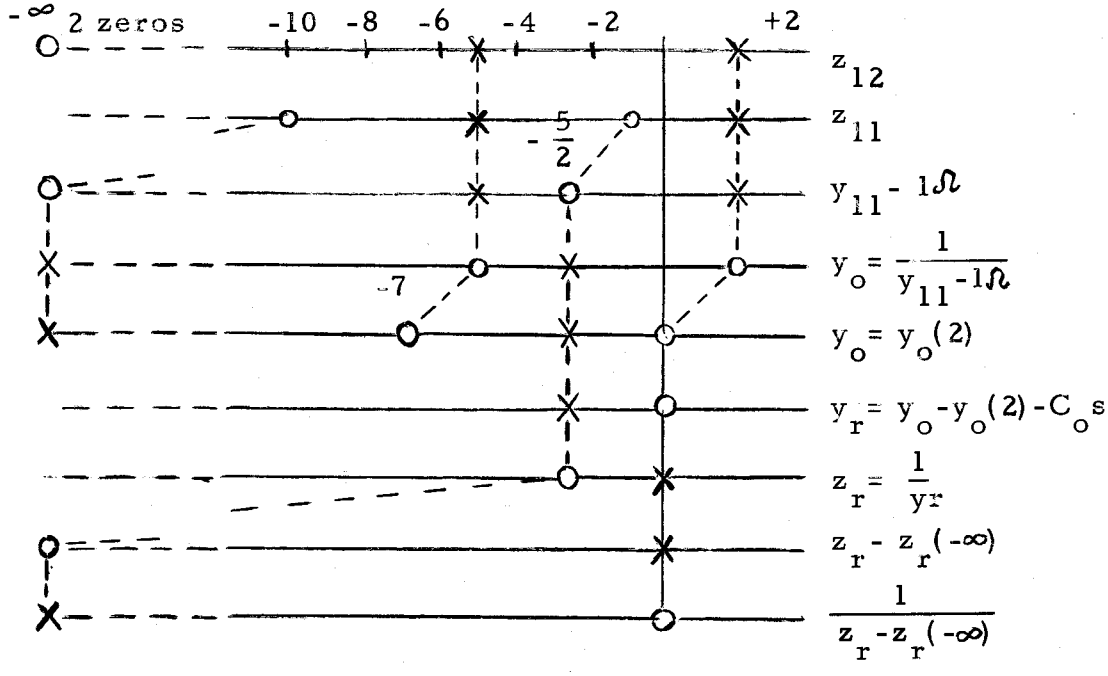
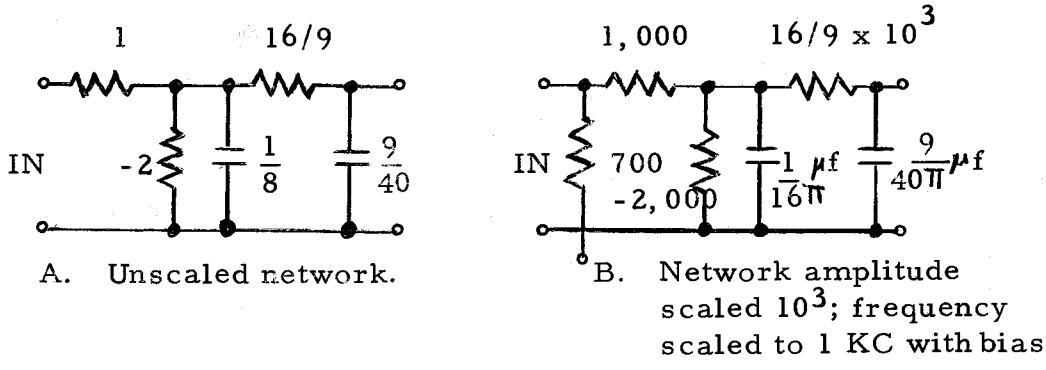


Figure 6. 1. Realization for $G_{12}(s) = \frac{H}{(s+1)(s+10)}$ with gain.



A. Unscaled network.

B. Network amplitude scaled 10^3; frequency scaled to 1 KC with bias.

Figure 6. 2. Network realized from Figure 6. 1.

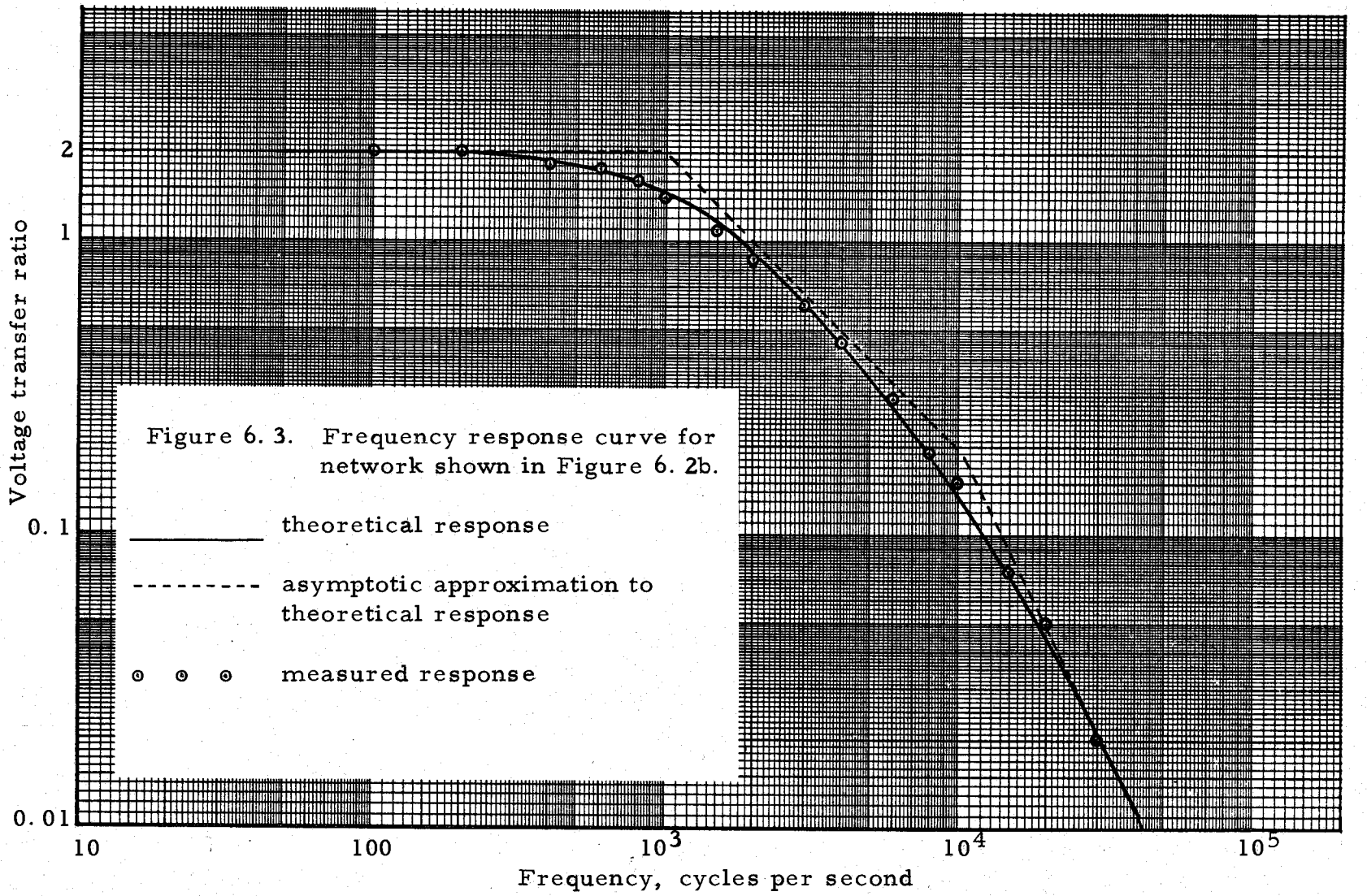


Figure 6.3. Frequency response curve for network shown in Figure 6.2b.

6. 2. Arbitrary Zeros of Transmission

Following the procedures outlined in Sections 5. 3 and 5. 4, a network with zeros at $s = \pm j1$ and any convenient RC poles is desired. The procedure is outlined in Figure 6. 4 and is detailed in the following steps.

Step 1: Given -

$$G_{12}(s) = \frac{(s^2 + 1)}{(s+\alpha)\ (s+\beta)}$$

Step 2: Separate the numerator of $G_{12}(s)$ into one term with only negative real zeros and one term with one positive real zero.

$$\begin{aligned} s^2 + 1 &= \frac{1}{2}s^2 + \frac{1}{2}s^2 - \frac{3}{2}s + \frac{3}{2}s + 1 \\ &= \frac{1}{2}s\,(s-3) + \frac{1}{2}(s^2 + 3s + 2) \\ &= \frac{1}{2}s\,(s-3) + \frac{1}{2}(s+2)(s+1) \end{aligned}$$

At this point, the poles of $G_{12}(s)$ may also be chosen. To easily identify the poles in the resulting response curve, they should be at least two octaves apart and two octaves away from the notch. Thus, a convenient denominator for $G_{12}(s)$ may be $(s+4)(s+16)$.

Step 3: Associate terms separated in G_{12} with admittance parameters and choose poles for those parameters. The identifications are:-

$$-y_{12}^{a} = \frac{s(s-3)}{Q(s)} \qquad -y_{12}^{b} = \frac{(s+2)(s+1)}{Q(s)}$$

$$y_{22}^{a} + y_{22}^{b} = 2\frac{(s+4)(s+16)}{Q(s)}$$

Q(s) must be chosen so that y_{22}^{a} and y_{22}^{b} are RC functions. It is convenient in this case to choose the two y_{22}'s equal. Thus, an appropriate Q(s) is (s+8)(s+20).

Step 4: Realization of Network B is a conventional RC-ladder procedure and is only outlined in Figure 6. 4a. Realization of Network A is outlined in Figure 6. 4b and proceeds as follows:

A. $-y_{12}^{a} = \frac{s(s-3)}{(s+8)(s+20)} \qquad y_{22}^{a} = \frac{(s+4)(s+16)}{(s+8)(s+20)}$

B. Remove $y_{22}(+3)$ from $y_{22}(s)$.

$$y_{22}(+3) = \frac{7}{11} \cdot \frac{19}{23} = \frac{133}{253}$$

$$y_{22} - y_{22}(3) = \frac{8(15s+212)(s-3)}{253(s+8)(s+16)} = y$$

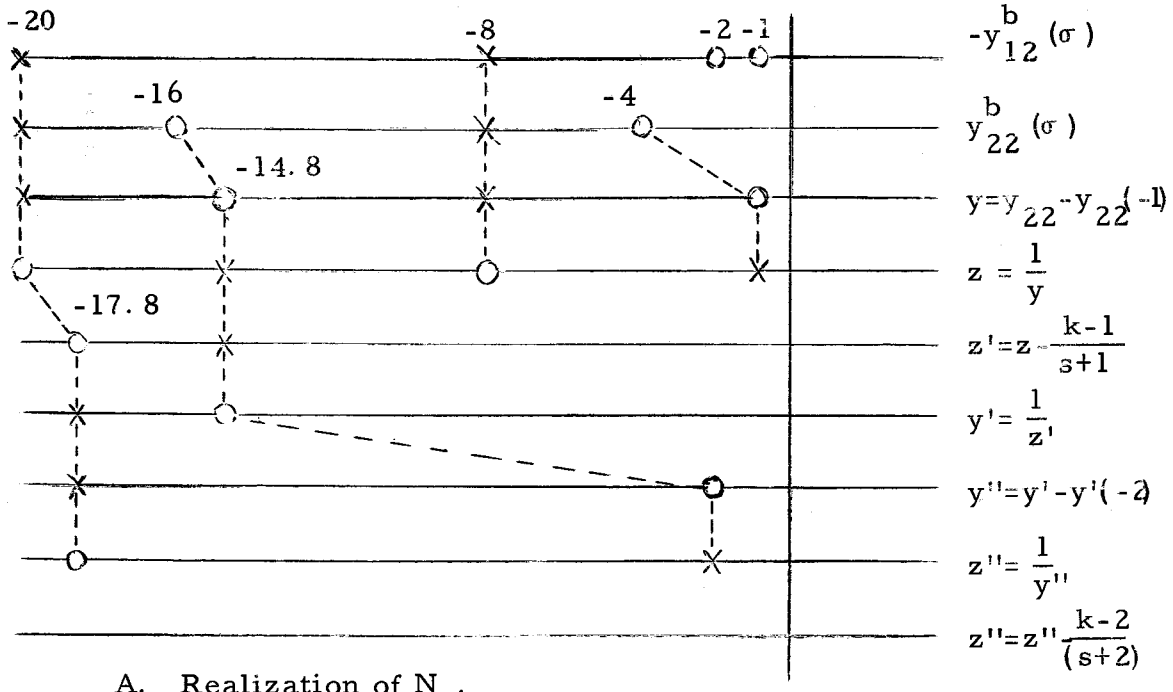
C. Realize the zero at s = +3 as a pole of $z = \frac{1}{y}$.

$$z = \frac{253}{8} \frac{(s+8)(s+16)}{(15s+212)(s-3)}$$

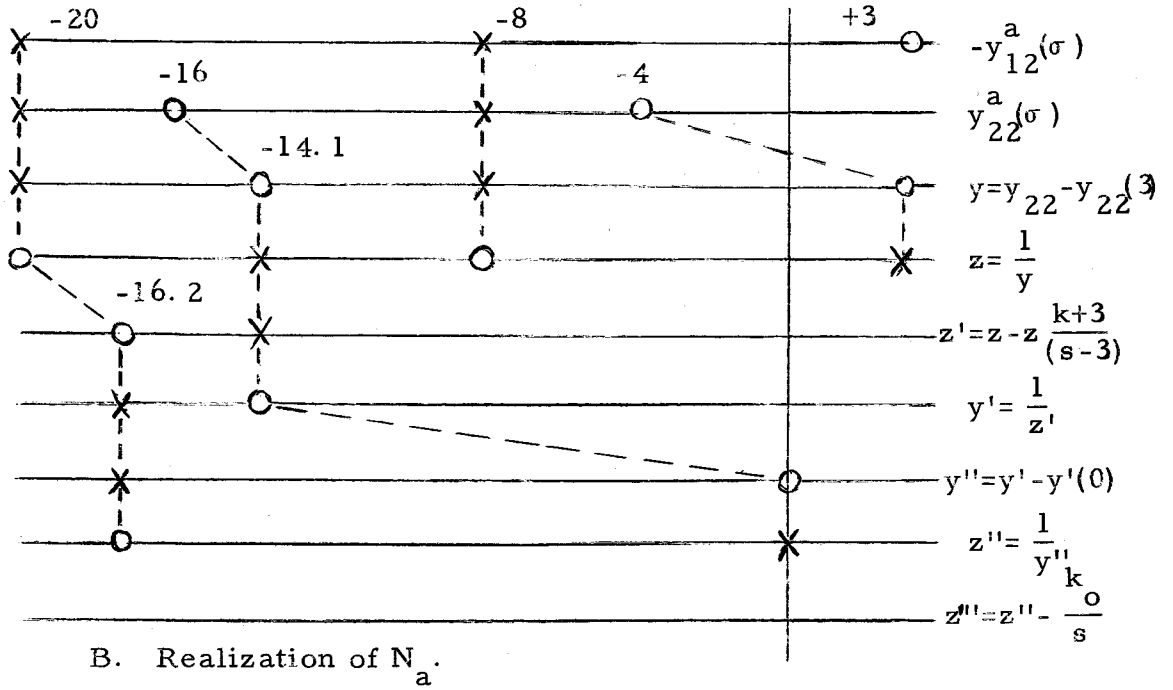
$$= \frac{253}{8} \frac{253}{257(s-3)} + \frac{(257s+4172)}{257(15s+212)}$$

$$z' = z - \frac{253}{8} \frac{253}{257(s-3)} = \frac{253}{257} \frac{257s+4172}{8(15s+212)} = \frac{1}{y'}$$

D. Shift zero of y' to s = 0 by removal of y' (0)



A. Realization of N_b.



B. Realization of N_a.

Figure 6.4. Illustration of realization for

$$G_{12}=\frac{s^2+1}{(s+4)(s+16)}.$$

$$y'(0) = \frac{257}{253} \cdot \frac{424}{1043}$$

$$y' - y'(0) = \frac{8096}{1043} \quad \frac{514}{253} \quad \frac{s}{(257\ s + 4172)} = y''$$

E. Realize the zero at s = 0 as a pole of $z'' = \frac{1}{y''}$

$$z'' = \frac{253}{514} \cdot \frac{1043}{8096} \quad \frac{257s + 4172}{s}$$

$$= \frac{253}{514} \cdot \frac{1043}{8096} \quad (257 + \frac{4172}{s})$$

At this point, the coefficients of realization for $-y_{12}^{a}$ and $-y_{12}^{b}$ must be examined since the result is obviously not valid unless the two $-y_{12}$'s are realized within the same factor. If they are not the transmission of the network with the higher coefficient must be reduced. For the two networks just realized, $k^{a} = 0.06134$ and $k^{b} = 0.0977$ so that attenuation must be added to N_b so that $k^{b} = k^{a}$; the attenuation required is k^{a}/k^{b}. The easiest point to insert the attenuation is to use the last resistance realized in N_b; it may be accomplished as shown in Figure 6.5 using a T-pad attenuator.

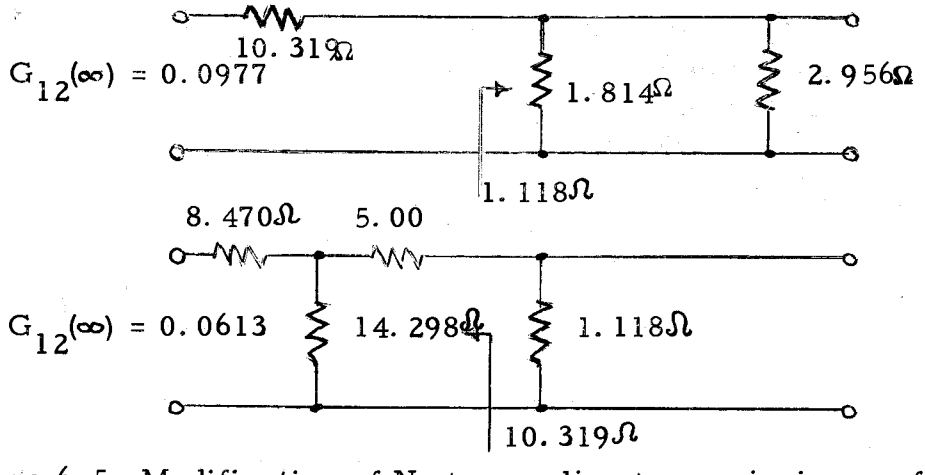


Figure 6.5. Modification of N_a to equalize transmission coefficients.

The resulting network from the preceeding realization after scaling s = j1 to s = j1000 cps and scaling impedance by 100 is shown in Figure 6.6; graphical comparison between computed and measured frequency response is shown in Figure 6.7.

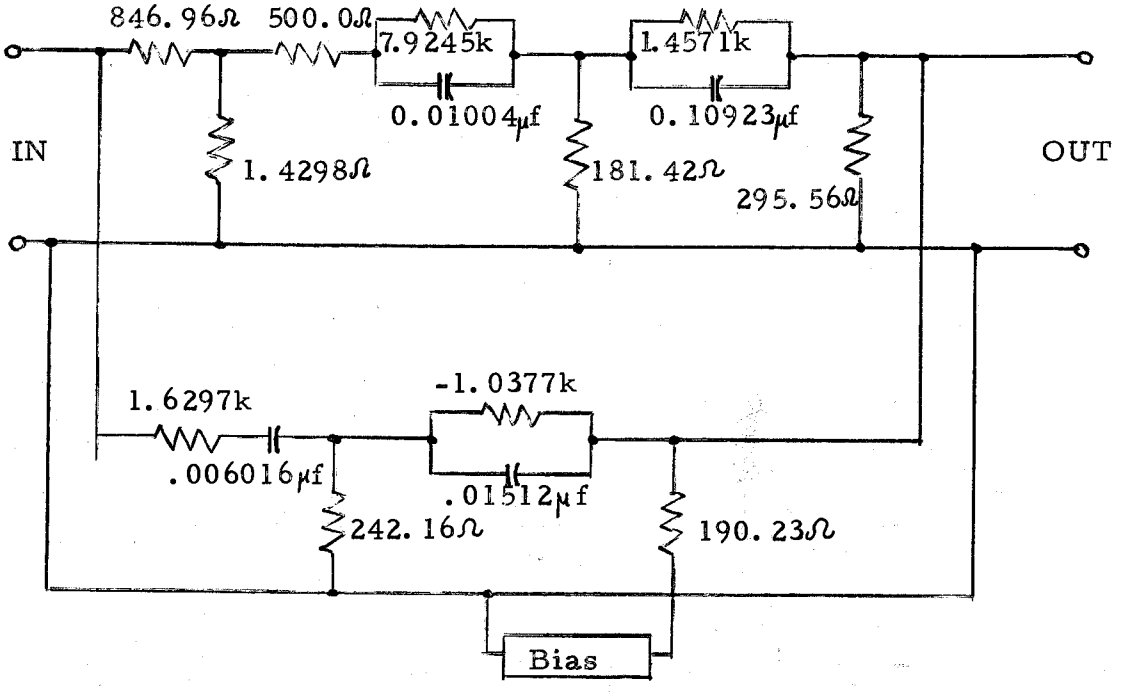


Figure 6.6. Network for realization of $G_{12} = \frac{(s^2+1)}{(s+4)(s+16)}$ scaled to 1 kc.

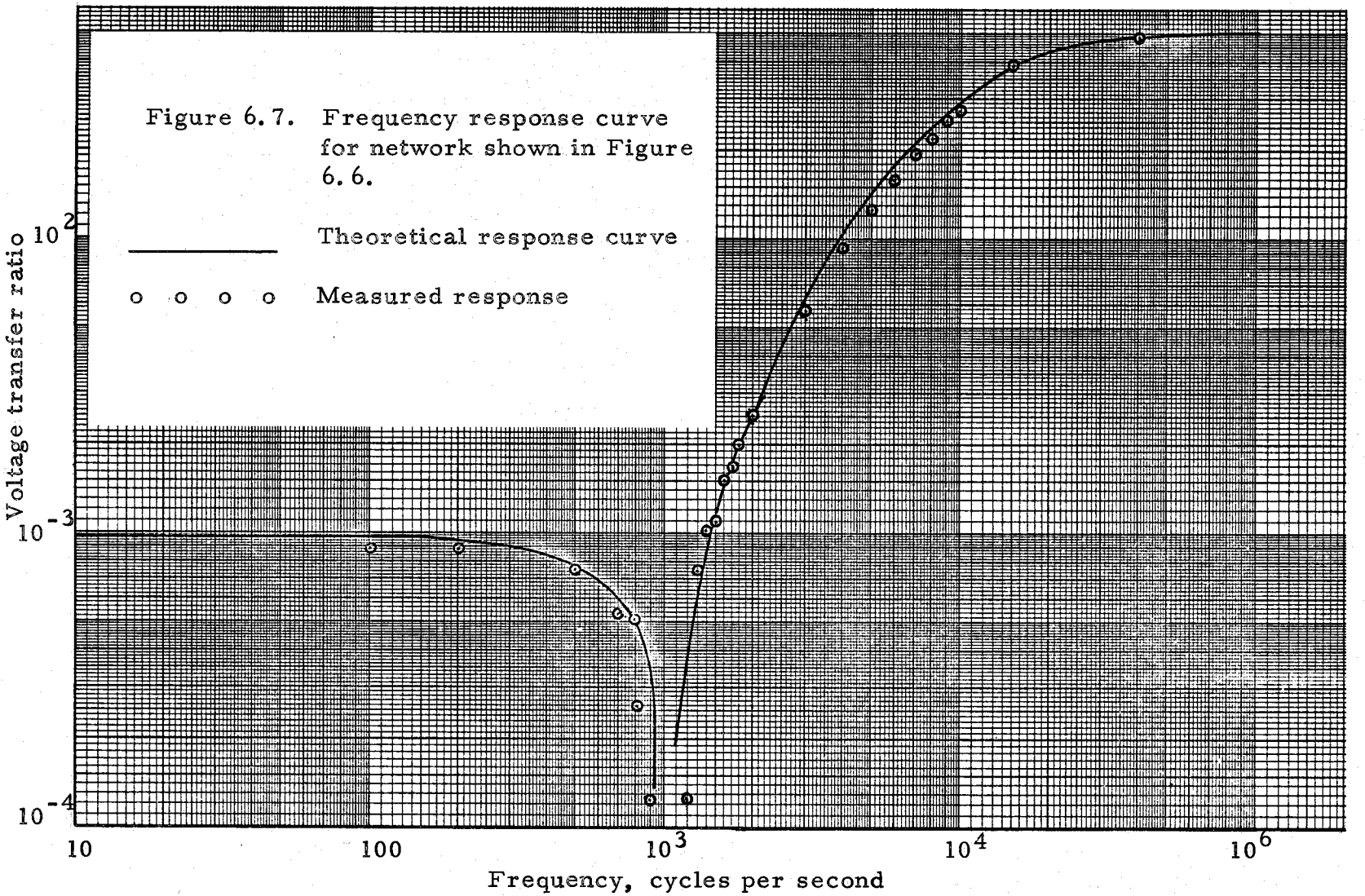


Figure 6.7. Frequency response curve for network shown in Figure 6.6.

——— Theoretical response curve

o o o o Measured response

SUMMARY AND CONCLUSIONS

The circuit of Figure 3. 8, page 9, exhibits five distinct regions of operation; the one of particular interest occurs after the zener diode begins to conduct and a negative resistance is generated at the terminals.

A set of design equations, Equations 3. 24 through 3. 28, is presented which allows the circuit component values to be determined from any set of specifications. Table 4. 1 compares a set of specified circuit parameters to parameters measured in a circuit designed to those specifications.

Several negative-resistance synthesis techniques proposed by Losee and Mitra (6, p. 357-62) are outlined for the purpose of demonstrating applications of the controlled negative resistance to actual problems in network synthesis; two such networks are actually realized and the measured frequency response is compared to the theoretical response.

The problem of including biasing within the network is discussed and it is demonstrated that biasing may always be included within a $\pm$ RC network without otherwise modifying the network.

The principal conclusion is that the device presented is a practical device for use in network synthesis where negative resistances are required. It's practicality arises from the ease of design, the

ability to handle large signals, and the ease with which the negative resistance may be controlled.

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APPENDIX

APPENDIX I

MEASUREMENT OF NEGATIVE RESISTANCES

The problem of measuring the magnitude of negative resistances presents several difficulties, particularly because of the bias requirements.

The simplest approach is to use a curve tracer; this proved to be most useful during experimental work on the negative resistance circuit where highly accurate measurements of negative resistance are not required. A curve tracer such as the Tektronix 575 or the circuit shown in Figure I. 1 proved adequate.

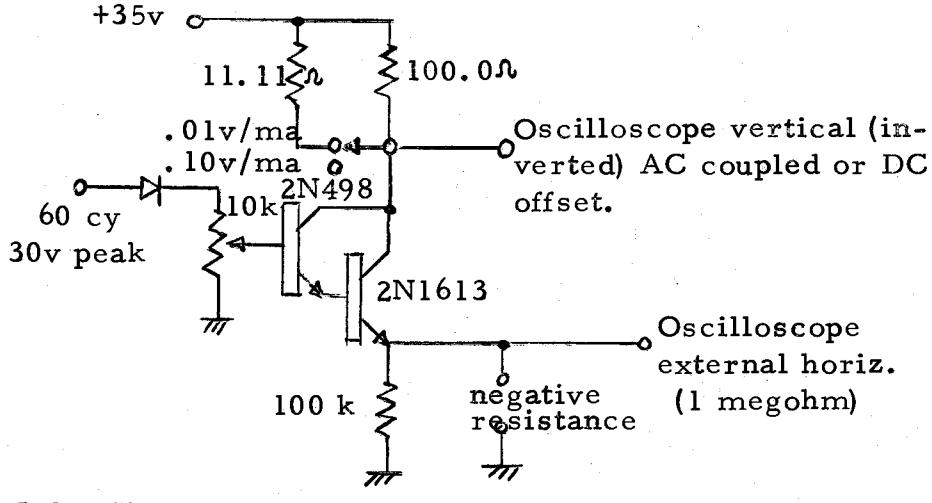

Figure I. 1. Simple curve tracer for two-terminal devices.

When greater accuracy is required, a different approach is required. One such approach is to modify the standard Wheatstone Bridge to accept bias as shown in Figure I. 2; two of the resistive arms

are replaced with equal capacitors to prevent bias current from circulating in the bridge. Stable biasing of the negative resistance is possible only if $r - R < 0$; fortunately, this condition presents a positive resistance to the bridge and it may be easily measured by nulling the bridge with R'. The method is not direct since the value of -R must be computed from the known value of r and the calibrated value of R'.

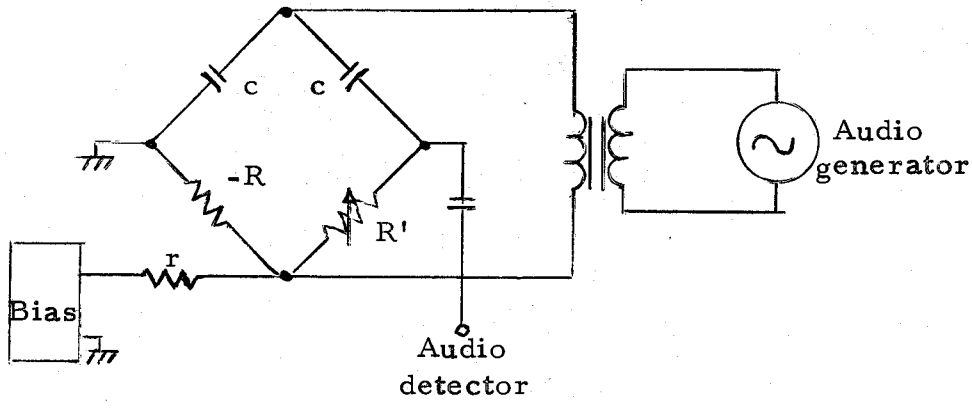

Figure I. 2. Bridge for measuring negative resistance.

Another approach used is a modification of a method suggested by Todd (12, p. 338). The principle is direct; when R' = -R , an infinite resistance occurs in the signal path and a null occurs. The circuit shown in Figure I. 3. The only difficulty with this technique is that DC current must flow through the calibrated resistor.

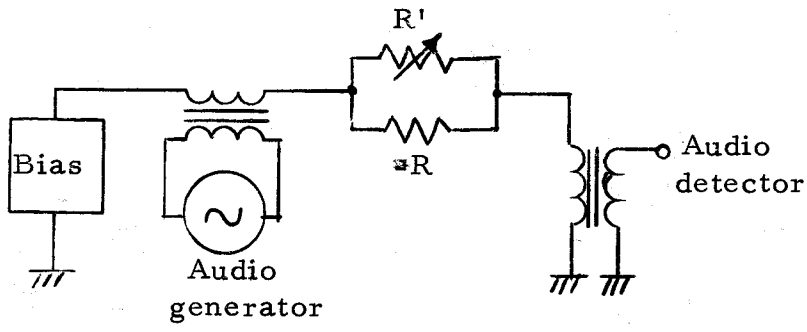

Figure I. 3. Circuit for measuring negative resistance.