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Title DESIGN OF HIGH-INPUT IMPEDANCE, WIDE-BAND TRANSISTORIZED AMPLIFIERS

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Conventional bi-polar transistors are inherently low input impedance devices. Transistor amplifiers have been designed which will present high input impedance, but the frequency response is limited to low frequencies, hundreds of kilocycles.

This thesis investigates both field effect transistors and positive feedback as applied to high input impedance wide band amplifier design. The field effect transistor, in the source-follower configuration, is shown to offer high input impedance, wide-band amplification, and low output impedance. Positive feedback is shown to increase considerably the input impedance without any danger of self-oscillations.

The generalized theory is presented using a model amplifier consisting of an input stage containing the field effect transistor, followed by two transistor stages. All the necessary criteria

are derived from this model.

An experimental amplifier was built and tested in the laboratory to check the validity of the theoretical analysis. The input impedance of this amplifier measured 20.7 MΩ of resistance shunted by 1.7 pf. of capacitance; the band-width extended from about 30 cps to about 10 Mc.

DESIGN OF HIGH-INPUT IMPEDANCE, WIDE-BAND TRANSISTORIZED AMPLIFIERS

by

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DESIGN OF HIGH-INPUT IMPEDANCE, WIDE-BAND TRANSISTORIZED AMPLIFIERS

I. INTRODUCTION

High input impedance is a very desirable amplifier characteristic in many applications. The conventional transistor, despite all its glamorous appeal, has proved to be ill-fitted for high input impedance amplifiers. Designers have devised ways and means of getting around this inherent transistor shortcoming, however, the results, as successful as they are, fall somewhat short of the achievements using vacuum tubes.

Wide band amplification and high input impedance are two conflicting characteristics in conventional transistors. Amplifiers can be designed which will attain one characteristic or the other, but not both simultaneously.

The advent of the Field Effect Transistor, usually abbreviated FET, has opened new vistas in high input impedance amplifier design.

In this thesis, the FET together with positive feedback is used in the development of a high input impedance wide band amplifier. It is shown that the FET facilitates the achievement of high input impedance without conflicting with wide band amplification. The earlier sections of this thesis contain the necessary

theory regarding both the FET and positive feedback; the last section describes an experimental amplifier which was built and tested in the laboratory. The input impedance of the experimental amplifier measured 20.7 megohms of resistance shunted by approximately 1.7 picofarads of capacitance, and the band width extended from about 30 cps. to about 10 Mc.

II. THE FIELD EFFECT TRANSISTOR AS A HIGH INPUT IMPEDANCE DEVICE

INSIDE THE FIELD EFFECT TRANSISTOR

It would be profitable to briefly mention the physics and structure of the field effect transistor (FET).

Figure 1 shows a simplified representation of a field effect transistor (FET). It consists of a P-type bar of silicon with two N-type regions situated on opposite sides of the bar.

Assuming a carrier density $P \gg N$, the conductivity of the P-type bar can be expressed as (8, p. 1)

$$G_o = \frac{(q\mu)\,(PWT)}{L} \qquad \text{(II-1)}$$

where: q = charge of electron

μ = electron mobility

P = hole density

W = width of the bar

T = thickness of the bar

L = length of the bar

Equation (II-1) shows that the conductivity can be varied by varying almost any parameter of Equation (II-1). However, practical limitations reduce the possibilities to either varying P, the hole density, or T, the thickness. In the case of the Field

Effect Transistor, as will be presently shown, the conductivity is modulated (or varied) by varying the conductive thickness.

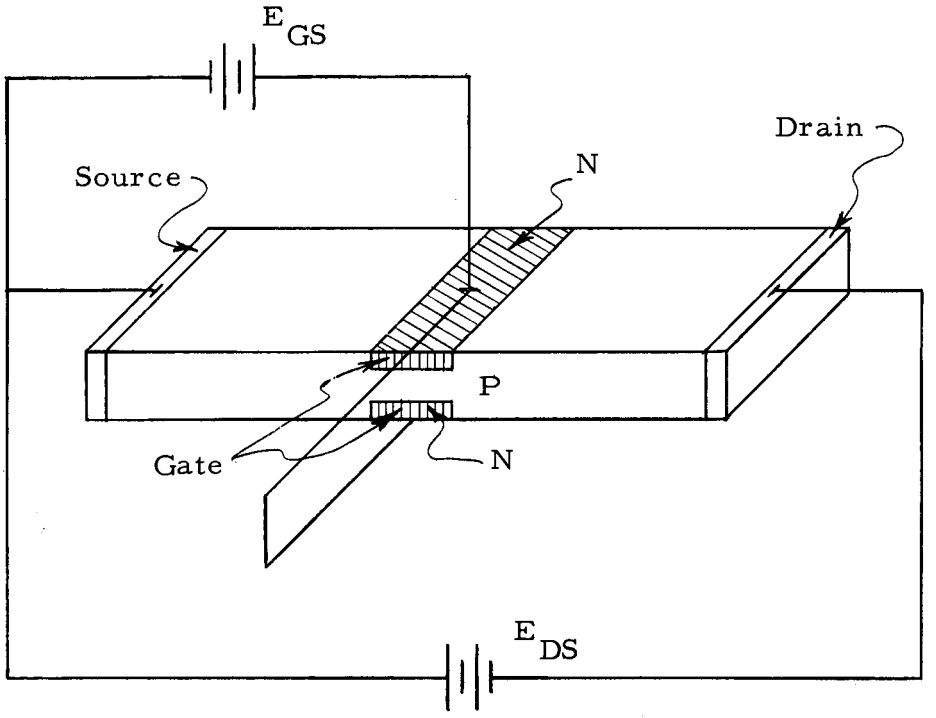

Figure 1. Elementary form of a FET.

The gate-source voltage indicated in Figure 1 effectively reverse-biases the P-N junction. Under this condition, a "space charge" region, also known as a depletion region, is created between the P and the N regions from which all free charge carriers have been removed. The width of the depletion regions is a function of both the impurity concentration and the junction potential.

Figure 2 shows that portions of Figure 1 consisting of the N-type regions and the P-type channel in between; it also depicts

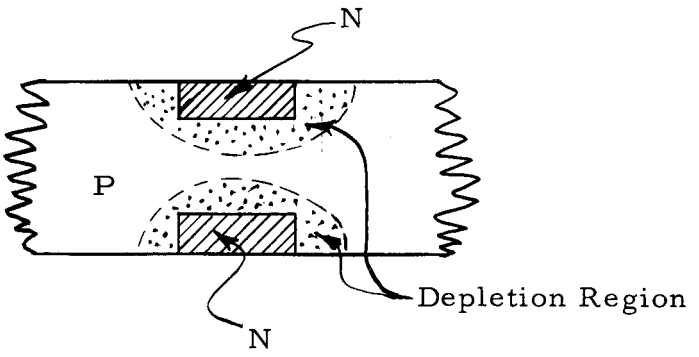

Figure 2. Variable thickness conductive channel in a FET.

the depletion regions created by the reverse bias. The width of the depletion region is increased by increasing the reverse-biasing voltage, and vice-versa. Thus, it is easily seen that the P-type channel width (available for conduction) is inversely proportional to the reverse-biasing voltage. Going back to Equation (II-1), then, it can be concluded that the conductivity of the P-type channel is inversely proportional to the reverse biasing voltage. This is the principle underlying the operation of the field effect transistor, the name being derived from the " effect" of the created "field" on the channel conductance.

Since a reverse bias between the gate and source is necessary for proper FET operation, the impedance presented by this P-N junction will be high. Therefore, the FET is inherently a high input impedance device.

The advantages offered by the FET over the conventional

bi-polar transistor can be summarized as follows (1, p. 69):

a. High input impedance.

b. Less sensitive to radiation damage, since the FET does not depend on minority carriers for its operation

c. Low noise, for the same reason as in b.

THE FIELD EFFECT TRANSISTOR AS AN ACTIVE DEVICE

Figure 3 shows the symbol representing a FET; the device is biased for "common source" operation. There are also other configurations similar to vacuum tubes or transistors. Figure 4

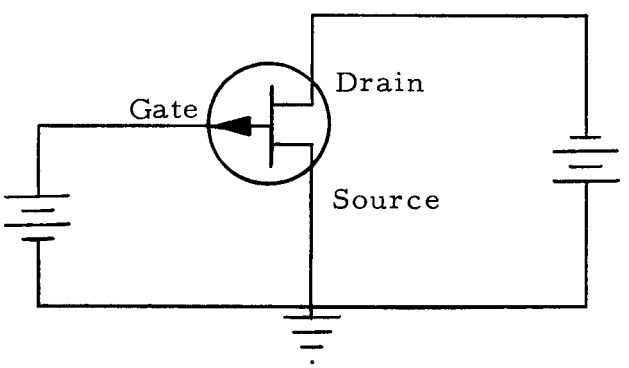

Figure 3. Symbolic representation of a P-channel FET.

shows the volt-ampere output characteristics for a typical FET. The curves of Figure 4 depict two distinct regions; the one

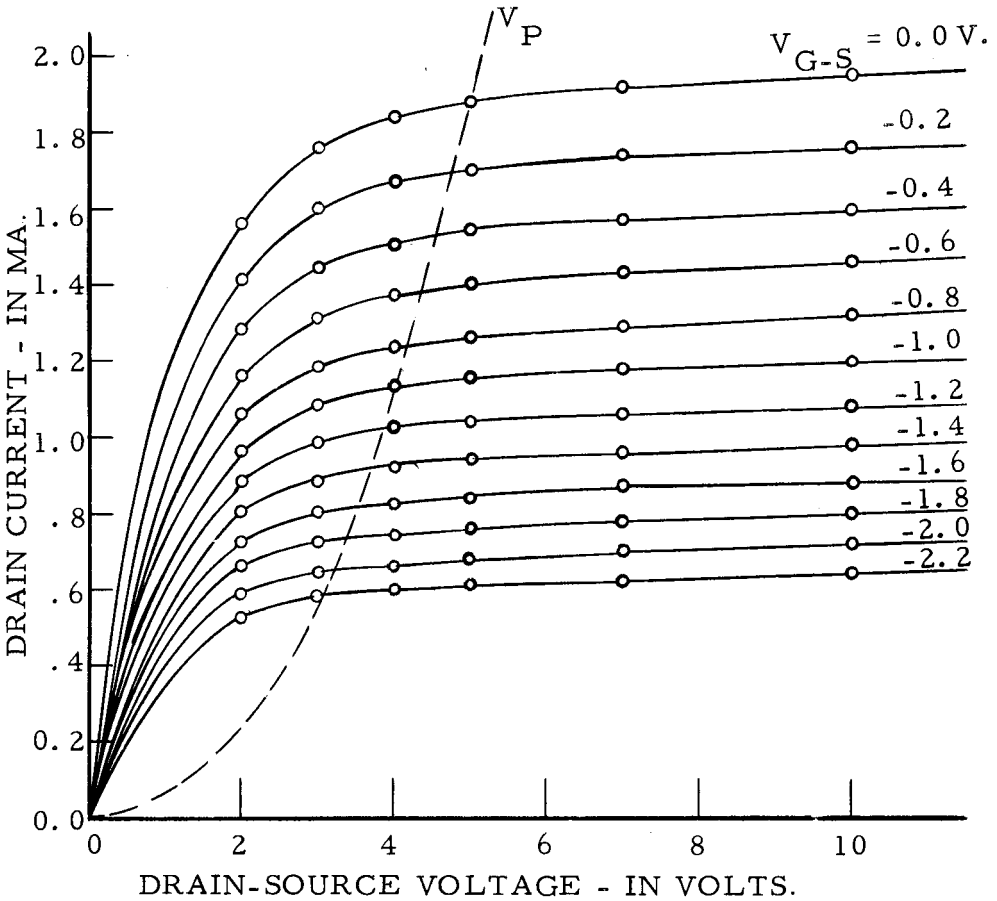

Figure 4. Volt-ampere output characteristics for TIX881 field effect transistor.

corresponding to low drain-source voltages is similar to the vacuum tube triode characteristics, and that corresponding to high voltages is similar to the vacuum tube pentode characteristics. The dotted line of Figure 4 indicates the separation between these two regions, and is normally called the "pinch-off" voltage (V_p).

FIELD EFFECT TRANSISTOR EQUIVALENT CIRCUIT

Analysis of circuits containing FETs can better be accomplished by dealing with an equivalent circuit. Figure 5 shows a FET equivalent circuit proposed by Texas Instruments Co. (8, p. 26). This equivalent circuit represents by lumped elements the physics and characteristics of the FET. Referring back to Figures 1 and 2, the branches R_3C_3 and R_4C_4 represent the depletion regions between the gate and the source, and between the gate and the drain. C_3 and C_4 represent the depletion layer capacitance, whereas R_3 and R_4 account for the reverse leakage current through the depletion region. Resistances R_1 and R_2 represent the ohmic contact and bulk resistance from the gate to the source and to the drain respectively; likewise R_6 and R_5 represent the bulk resistance and ohmic contacts at the drain and source terminals respectively. r_D is the differential P-type channel resistance in the pinch-off region, see above. The current generator represents the control of the gate-source voltage on the

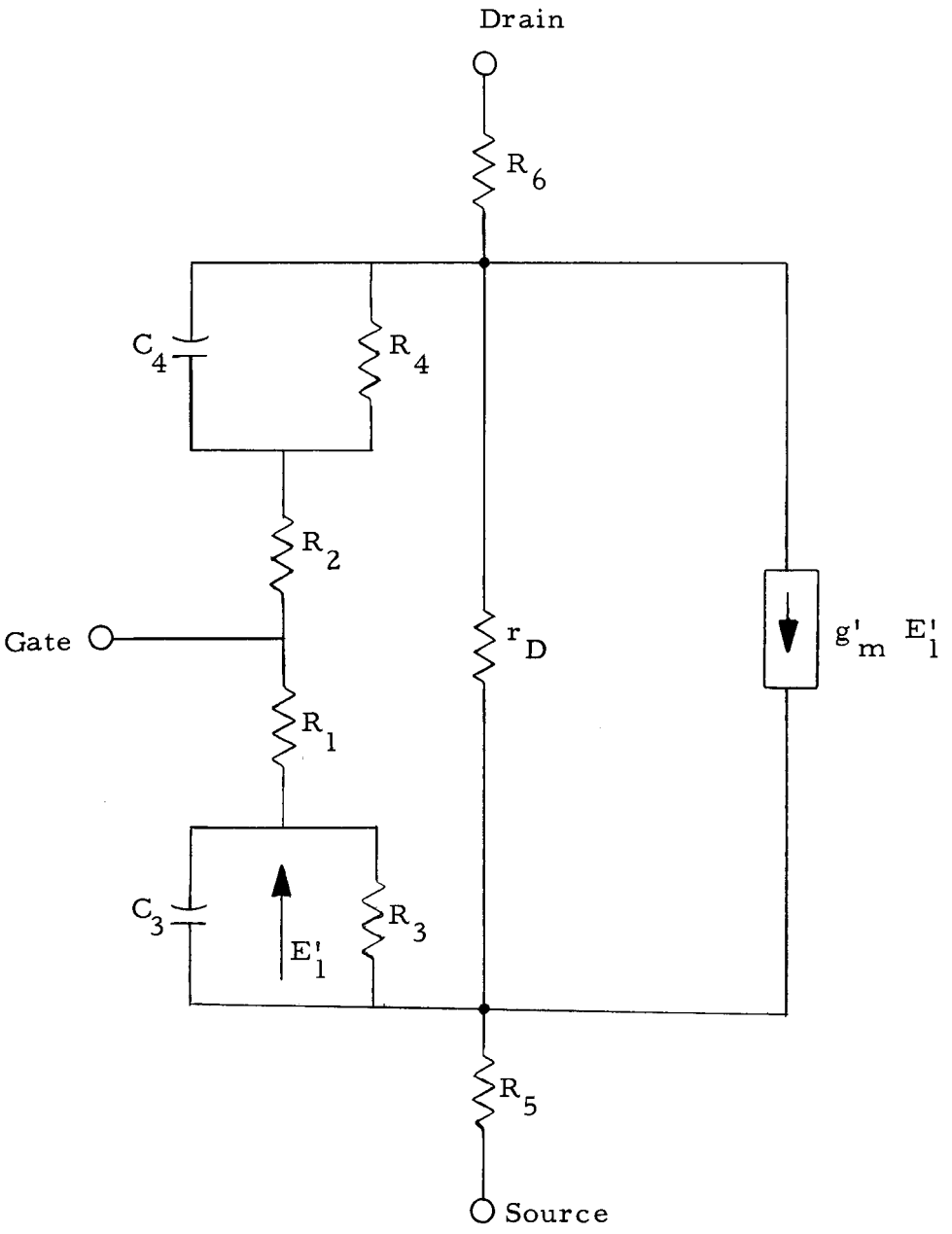

Figure 5. Field Effect Transistor equivalent circuit.

drain current, the controlling voltage being that across the capacitor C_3 (depletion region capacitance). There exists large differences among the magnitude of the resistances shown in the equivalent circuit, the order being as follows

$$R_3,\ R_4 \gg r_D \gg R_1,\ R_2,\ R_5,\ R_6$$

and approximately

$$R_3,\ R_4 \simeq \text{several megohms}$$

$$R_1 + R_5 \simeq \text{hundreds of ohms}$$

$$R_2 + R_6 \simeq \text{hundreds of ohms}$$

The equivalent circuit of Figure 5 has been found to be a good representation of the FET from d-c to around 100 Mc (8, p. 6). Although this equivalent circuit is quite complete, it is very complex and unyielding for analysis. Figure 6 shows another equivalent circuit frequently found in current literature, and which is much simpler. Because of the large difference among the magnitude of the resistances shown in Figure 5, it would be justifiable to eliminate resistances R_1, R_2, R_6 and R_5. To further show that the circuit of Figure 6 is a simplification of Figure 5, notice the following relations

$$g_o = \frac{1}{r_D}$$

$$g_{gs} = \frac{1}{R_3}$$

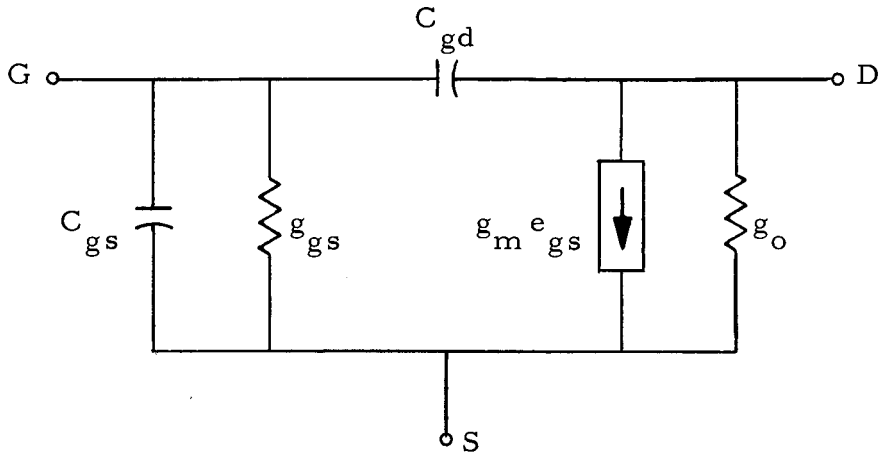

Figure 6. Simplified Field Effect Transistor equivalent circuit.

$$C_{gd} = C_4$$

$$C_{gs} = C_3$$

$$g_m = g'_m \quad \text{(since } R_1 \text{ is negligible)}$$

$$e_{gs} = E'_1$$

also, R_4 has been completely dropped out. The circuit of Figure 6 is a good approximation for most practical applications. However, for the purposes of this thesis it will be necessary to include R_4, since this resistance enters into the complete characterization of the input impedance. Therefore, the circuit of Figure 7 is the one which will be used in all succeeding work.

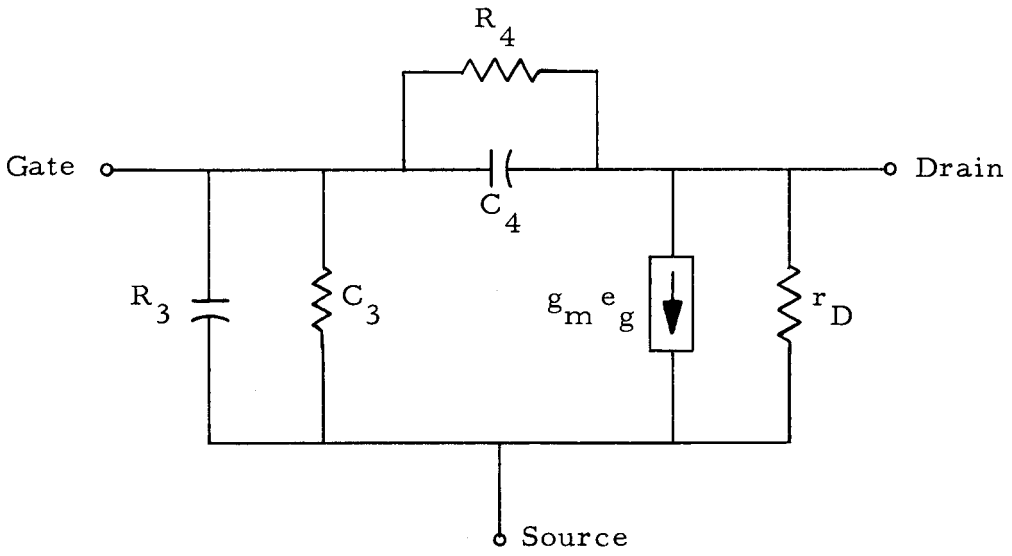

Figure 7. Simplified Field Effect Transistor equivalent circuit to be used in this thesis.

All the above presentation considered a P-channel FET. There is a counterpart N-channel type field effect transistor. In fact this type of FET was used in the experimental work of this thesis. The symbolic representation of the N-channel FET is shown in Figure 8.

III. THE SOURCE-FOLLOWER CONFIGURATION

Of the many possible configurations offered by the FET, the source follower configuration provides the highest input impedance. Besides, this configuration as will be presently shown, also offers the advantages of wide band width and low output impedance. These are all desirable characteristics in the design of high input impedance wide band amplifiers.

VOLTAGE AMPLIFICATION

Figure 8 shows a practical source follower circuit. In this circuit it is assumed that both C_1 and C_2 are very large, such that the impedances presented by these capacitors are negligible for all frequencies of interest. Using the FET equivalent circuit derived earlier, it is now possible to draw an equivalent a-c circuit for the source follower; this is shown in Figure 9. In order to simplify the analysis, the circuit of Figure 9 can be redrawn as shown in Figure 10. Notice that (in Figure 9) node (A) is effectively connected to ground. The branch R_4C_4 has been placed at the input for purposes which will be evident later on.

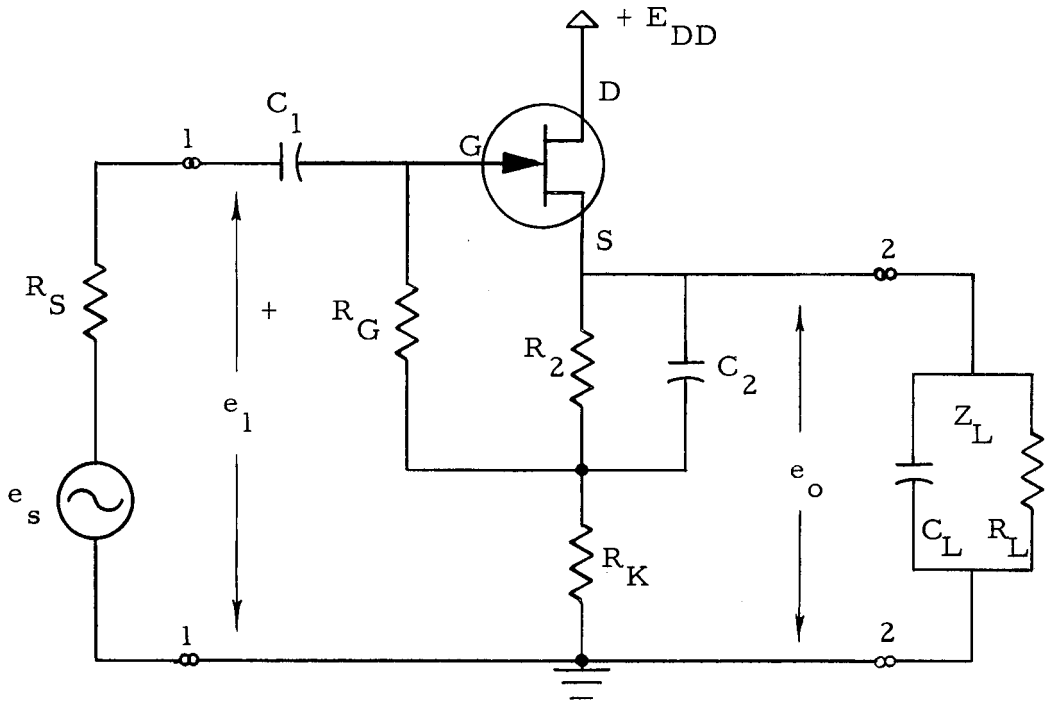

Figure 8. The source follower configuration.

Since here it is desired to investigate the amplification provided by the source follower, voltage amplification will be defined as

$$A_v = \frac{e_o}{e_1}$$

This truly describes the potentialities of the source follower alone independent of signal source output resistance.

Now, writing the nodal equation for node (B) of Figure 10

$$i_g = (i_K + i_D + i_L) - g_m e_g \qquad \text{(III-1)}$$

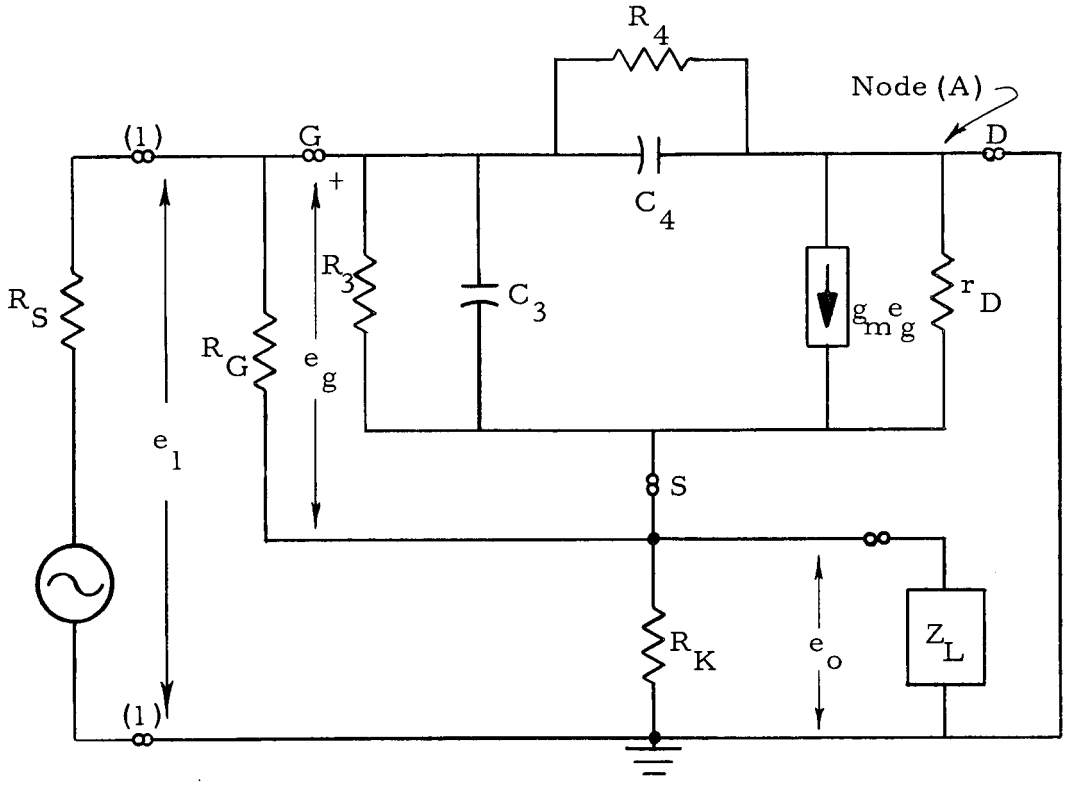

Figure 9. Source follower equivalent circuit.

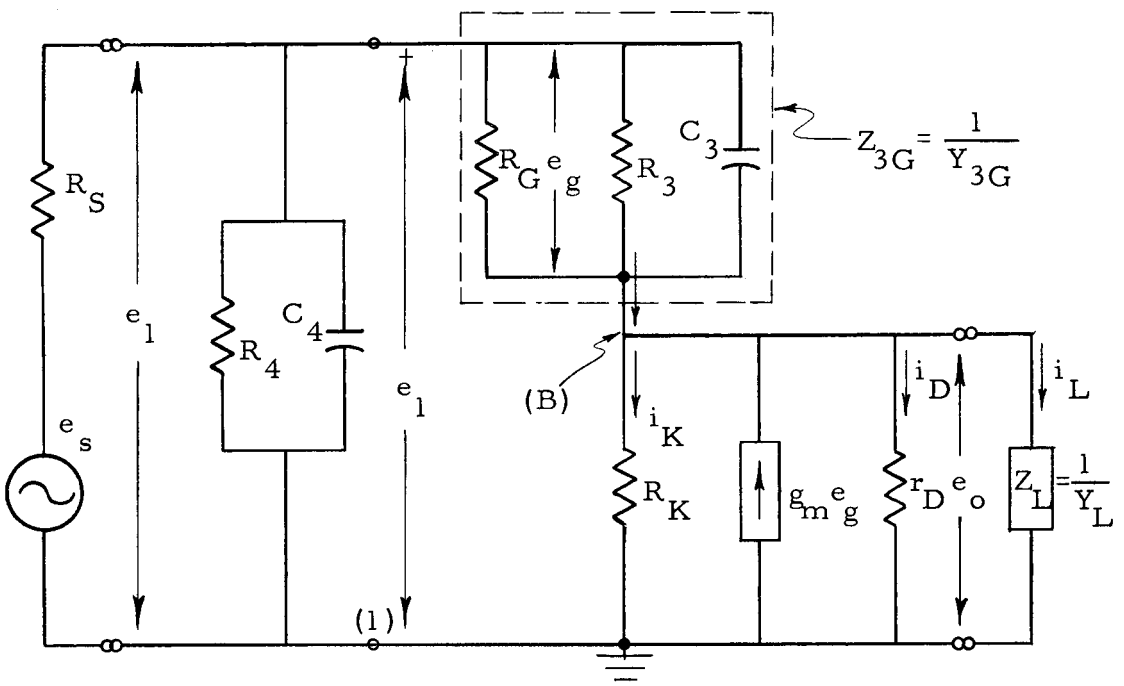

Figure 10. Source follower equivalent circuit rearranged.

but $$i_g = (e_1 - e_o)\ Y_{3G} \tag{III-2}$$

$$i_K + i_D + i_L = e_o Y_K + e_o Y_D + e_o Y_L = e_o (Y_K + Y_D + Y_L)$$

calling $$Y_{eq} = Y_K + Y_D + Y_L \tag{III-3}$$

$$i_K + i_D + i_L = e_o\ Y_{eq} \tag{III-4}$$

also $$e_g = e_1 - e_o \tag{III-5}$$

Substituting (III-2), (III-4), and (III-5) in (III-1)

$$(e_1 - e_o)\ Y_{3G} = e_o Y_{eq} - g_m\ (e_1 - e_o)$$

from which it is easily found,

$$A_v = \frac{e_o}{e_1} = \frac{1}{1 + \dfrac{Y_{eq}}{g_m + Y_{3G}}} \tag{III-6}$$

In general, the load Z_L (Y_L) can be assumed to consist of a resistance R_L (G_L) shunted by a capacitance C_L. Now, by substituting the expressions for Y_{eq} and Y_{3G} from Equation (III-3) and Figure 10 respectively into Equation (III-6) it is obtained, in Laplace transform notation

$$A_v = \frac{1}{1 + \dfrac{(G_K + G_D + G_L) + sC_L}{(g_m + G_G + G_3) + sC_3}} \tag{III-7}$$

Normally,

$$g_m \gg G_G + G_3$$

$$(G_K + G_L) \gg G_D$$

So that Equation (III-7) reduces to,

$$A_v = \frac{1}{1 + \frac{C_L}{C_3} \frac{\frac{G_K + G_L}{C_L} + s}{\frac{g_m}{C_3} + s}} \qquad \text{(III-8)}$$

At low frequencies, Equation III-8 reduces to

$$A_v = \frac{1}{1 + \frac{G_K + G_L}{g_m}} \qquad \text{(III-9)}$$

For large values of g_m (5000 micromhos or better) such that

$$g_m \gg (G_K + G_L) \qquad \text{(III-10)}$$

the voltage amplification becomes

$$A_v \simeq 1 \qquad \text{(III-11)}$$

To analyze the frequency response of A_v, the voltage amplification, assume $C_L \simeq C_3$. Further assume that near unity amplification is desired; Equation III-10 must hold. Under these conditions, the relation between the corner frequencies of

of Equation (III-8) is

$$\frac{G_K + G_L}{C_L} \ll \frac{g_m}{C_3} \qquad \text{(III-12)}$$

which indicates that the frequency response of the source follower voltage amplification is determined by G_K, G_L, and C_L. For an example assume $G_K + G_L = 5 \times 10^{-4}$ mhos and $C_L = 10$ pf ; this gives a corner frequency of approximately 10 Mc. This result shows that the source follower is suitable for wide band amplification.

INPUT IMPEDANCE

Figure 11 is essentially the circuit of Figure 10, repeated for convenience and also to indicate the symbols to be used in determining the input impedance.

From Figure 11 it is easily seen that the input impedance Z_{in}, is simply the parallel combination of Z_4 and Z_1. That is

$$Z_{in} = \frac{Z_1 Z_4}{Z_1 + Z_4} \qquad \text{(III-13}$$

The impedance Z_4 can be traced back to the equivalent circuit of the FET. See Figure 9, page 15. As indicated previously, R_4 represents the leakage current of the reverse biased junction and is several megohms in value. Therefore, at low frequencies Z_4 is in the megohms region.

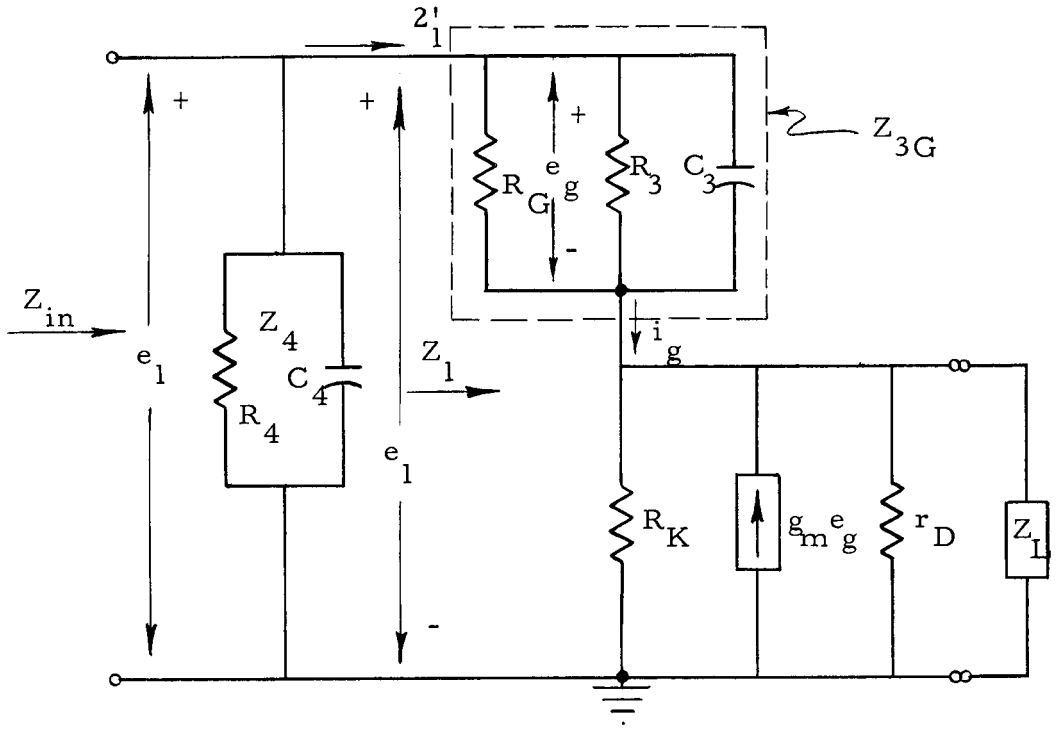

Figure 11. Source follower equivalent circuit.

On the other hand, the impedance Z_1 represents the input impedance to the source follower portion which is responsible for the voltage amplification. This impedance is, then

$$Z_1 = \frac{e_1}{i_1} = \frac{e_1}{i_g} \qquad \text{(III-14)}$$

From Figure 11

$$i_g = \frac{e_1 - e_o}{Z_{3G}} \qquad \text{(III-15)}$$

But, from Equation (III- 6)

$$e_o = A_v e_1 \qquad \text{(III-16)}$$

Substituting Equation (III-16) in Equation (III-15) and solving for e_1/i_g

$$Z_1 = \frac{e_1}{i_g} = \frac{Z_{3G}}{1 - A_v} \qquad \text{(III-17)}$$

In this expression Z_{3G} represents, at low frequencies, the parallel combination of R_3 and R_G. See Figure 11. R_3 is similar to R_4, mentioned earlier, and is several megohms in resistance. R_G is the complementary resistance needed to properly bias the gate-to-source junction; it also prevents the gate from floating. R_G can be made high in resistance, several megohms. Therefore, the impedance Z_{3G}, at low frequencies can be made quite high.

In previous discussion it was pointed out that A_v is less than unity, but under certain circumstances can be made quite close to unity (see page 17).

From the above argument, and considering Equation (III-17), one concludes that:

a. Z_1 is larger than Z_{3G}, since the quantity $(1-A_v)$ is always less than unity, the closer A_v is to unity the larger the value of Z_1.

b. Since Z_{3G} is in the megohms range, Z_1 will also be in the megohm region.

Substituting Z_1 and Z_4 from Equation (III-17) and Figure 11 respectively into Equation (III-13), and converting everything to admittances, it is found

$$Y_{in} = Y_4 + (1 - A_v) Y_{3G} \tag{III-18}$$

or substituting the components of Y_4 and Y_{3G} and simplifying (in Laplace transform notation)

$$Y_{in} = \left[\frac{(1 - A_v)}{R_{3G}} + \frac{1}{R_4}\right] + \left[(1-A_v)C_3 + C_4\right] s \tag{III-19}$$

For low frequencies, the input impedance is, from Equation (III-19)

$$Z_{in} = \frac{R_4 R_{3G}}{(1-A_v)R_4 + R_{3G}} = \frac{R_4 \dfrac{R_{3G}}{(1-A_v)}}{R_4 + \dfrac{R_{3G}}{(1-A_v)}} \tag{III-20}$$

and will be of the order of several megohms besides it is larger than the parallel combination of R_4 and R_{3G}, since the factor $(1-A_v)$ is less than unity.

Because of capacitors C_3 and C_4, the input admittance will increase for increasing frequencies. See Equation (III-19). Therefore, the input impedance will decrease for increasing frequencies; at very high frequencies the input impedance will be determined almost exclusively by capacitors C_3 and C_4.

From the above it can be seen that the source follower configuration does improve the input impedance; resistor R_{3G} is increased by the factor $(1-A_v)^{-1}$ which is larger than unity, and capacitor C_3 is decreased by the factor $(1-A_v)$ which is less than unity.

In Part IV it will be shown that positive feedback can be advantageously used to neutralize the detrimental effect of capacitances C_3 and C_4 on the input impedance.

OUTPUT IMPEDANCE

The output impedance will necessarily involve the signal source impedance. In order to facilitate the analysis, turn back to Figure 10 (p. 15) and notice that it is possible to substitute a Thevenin equivalent for the circuit to the left of point (1)-(1). The modified circuit appears in Figure 12.

The output impedance will be found following the definition

$$Z_o = \frac{\text{Open-circuit output voltage}}{\text{Short-circuit output current}} = \frac{e_{osc}}{i_{osc}} \qquad \text{(III-21)}$$

To find i_{osc}, simply consider the output being short circuited. Under these conditions

$$i_{osc} = g_m e_g + i_{g_{sc}} \qquad \text{(III-22)}$$

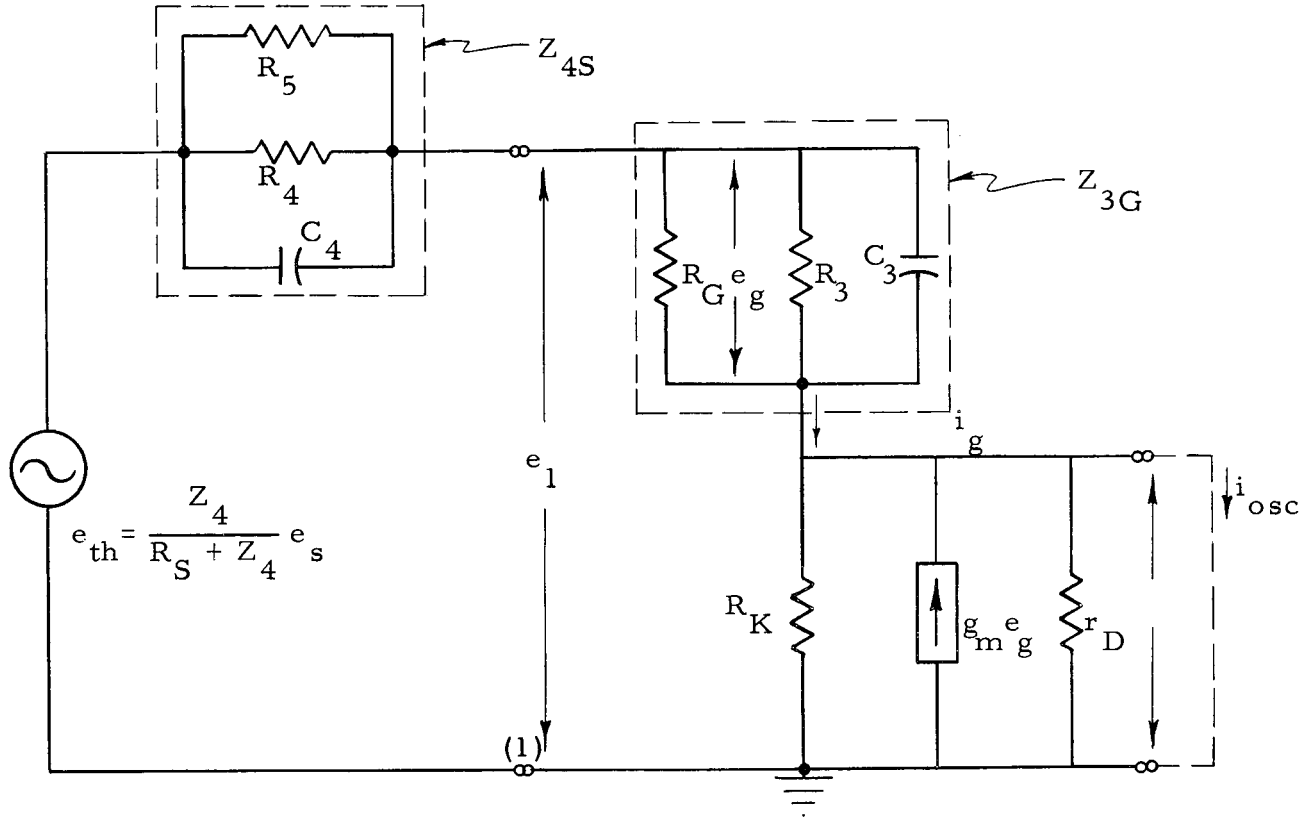

Figure 12. Modified equivalent circuit for the source follower.

but $e_g = e_{1_{sc}}$

$$i_{g_{sc}} = e_g Y_{3G} = e_{1_{sc}} Y_{3G}$$

then

$$i_{osc} = e_{1_{sc}} (g_m + Y_{3G}) \qquad \text{(III-23)}$$

From Figure 12

$$e_{1_{sc}} = \frac{Z_{3G}}{Z_{4S} + Z_{3G}} \; e_{th}$$

and

$$i_{osc} = \frac{Z_{3G}}{Z_{4S} + Z_{3G}} \; (g_m + Y_{3G}) \; e_{th} \qquad \text{(III-24)}$$

The open-circuit output voltage can be found as

$$e_{o_{oc}} = e_{1_{oc}} A_v' \qquad \text{(III-25)}$$

Where A_v' is similar to A_v of Equation (III-6) except for having $Z_L = \infty$, that is the load is not connected. Again, from Figure 12

$$e_{i_{oc}} = \frac{Z_1'}{Z_{4S} + Z_1'} \; e_{th} \qquad \text{(III-26)}$$

where once more Z_1' is similar to Z_1 of Equation (III-17), except for having A_v' instead of A_v in the expression. Substituting (III-26) in (III-25)

$$e_{o_{oc}} = \frac{Z_1'}{Z_{4S} + Z_1'} \; A_v' e_{th} \qquad \text{(III-27)}$$

Now, substituting from Equation (III-6)

$$A_v' = \frac{1}{1 + \frac{y_{eq}'}{g_m + Y_{3G}}} \qquad \text{(III-28)}$$

and from Equation (III-17)

$$Z_1' = \frac{Z_{3G}}{(1 - A_v'}$$

where Y_{eq}' again indicates $Z_L = \infty$ or $Y_L = 0$, Equation (III-27) reduces to

$$e_{o_{oc}} = \frac{Z_{3G}\,(g_m + Y_{3G})}{Y_{eq}'\,(Z_{4S} + Z_{3G}) + Z_{3G}\,(g_m + Y_{3G})}\, e_{th} \qquad \text{(III-29)}$$

Finally, substituting Equations (III-29) and (III-24) into Equation (III-21), and simplifying

$$Z_o = \frac{1}{Y_{eq}' + \frac{Z_{3G}}{Z_{4S} + Z_{3G}}\,(g_m + Y_{3G})} \qquad \text{(III-30)}$$

or

$$Z_o = \frac{1}{(Y_K + Y_D) + \frac{Z_{3G}}{Z_{4S} + Z_{3G}}\,(g_m + Y_{3G})} \qquad \text{(III-31)}$$

The effect of the signal source resistance, R_s, on the output inpudance is indicated by Z_{4S}, which is the parallel combination of Z_4 and R_s. For lower values of R_s such that

$$Z_{4S} \ll Z_{3G}$$

Equation (III-31) simply becomes

$$Z_o = \frac{1}{Y_K + Y_D + g_m + Y_{3G}} \qquad \text{(III-32)}$$

which if it is further assumed that

$$g_m > Y_K + Y_D + Y_{3G}$$

reduces to

$$Z_o \simeq \frac{1}{g_m} \qquad \text{(III-33)}$$

This again points out the necessity of obtaining FETs with large g_m in order to obtain low output impedance.

From Equation (III-31) it is observed that the output impedance will increase for increasing values of signal source resistance, R_s. For the case, although very unlikely,

$$R_s \gg Z_4$$

Equation (III-31) reduces to

$$Z_o = \frac{1}{(Y_K + Y_D) + \frac{Z_{3G}}{Z_4 + Z_{3G}} (g_m + Y_{3G})} \qquad \text{(III-34)}$$

This is the maximum value that the output impedance may acquire.

The above discussion has shown that the source follower indeed provides a low output impedance. It has been further shown that although this output impedance is function of the signal source resistance, R_s, it does have a maximum limit as indicated by Equation (III-34).

IV. POSITIVE FEEDBACK AND HIGH INPUT IMPEDANCE

It has already been mentioned that although the source follower possesses desirable characteristics for the design of high-input impedance wide band amplifiers, the capacitance in shunt at the input is certainly detrimental for high input impedance at higher frequencies. In this section it will be shown that positive feedback can be used to advantage in order to minimize (ideally eliminate) the effects of this shunt capacitance; it will be further shown that positive feedback can be used to obtain even higher impedances -- higher shunt resistive component at the input. Another aspect to be considered is the amplifier stability, being that positive feedback is used; it will be shown that by proper design, good stability can be assured.

To proceed with the presentation, it will be assumed that the source follower discussed previously is followed by two stages of amplification, each stage providing 180° of phase shift, or a total of 360° of phase shift for all frequencies of interest; thus, the output voltage will be in phase with the input voltage and positive feedback is now feasible. These two additional stages serve the purpose of isolating the signal to be fed back, besides they provide amplification to compensate for the less than unity

voltage amplification obtained from the source follower; the overall gain is assumed greater than unity. Figure 13 shows a block diagram of the composite amplifier being described here.

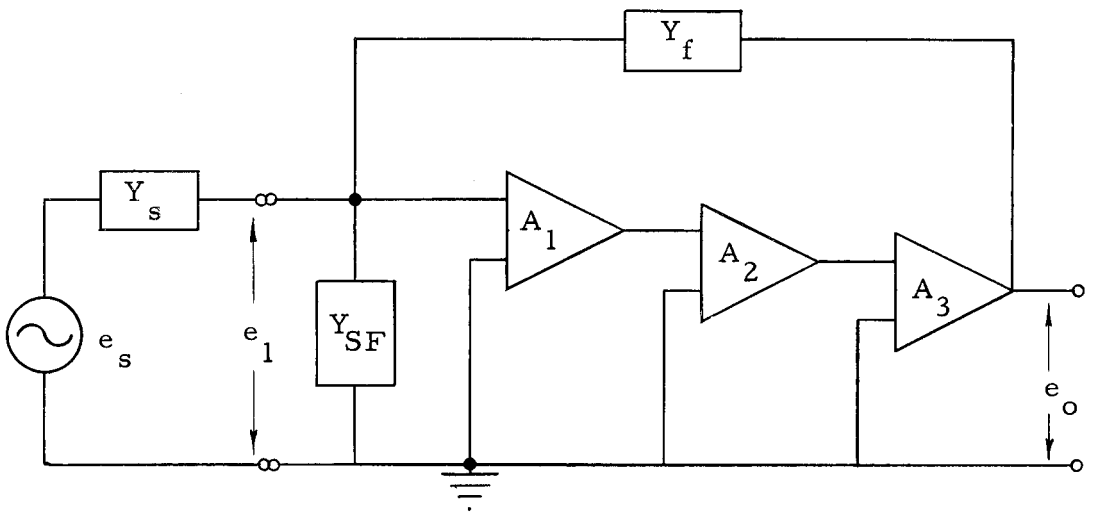

Figure 13. Three stage amplifier.

To simplify the diagram of Figure 13, all three stages of amplification can be combined into one, as is indicated in Figure 14. Further, the positive feedback is applied through a parallel R_fC_f circuit as shown in Figure 14.

From previous discussion (see Equation III-19) it is known that the input impedance of the source follower consists of a resistance and capacitance in parallel. This is indicated as an admittance Y_{SF} in Figure 13. For convenience in future analysis this admittance Y_{SF} will be decomposed into three parts as is shown in Figure 14. The signal source impedance is for

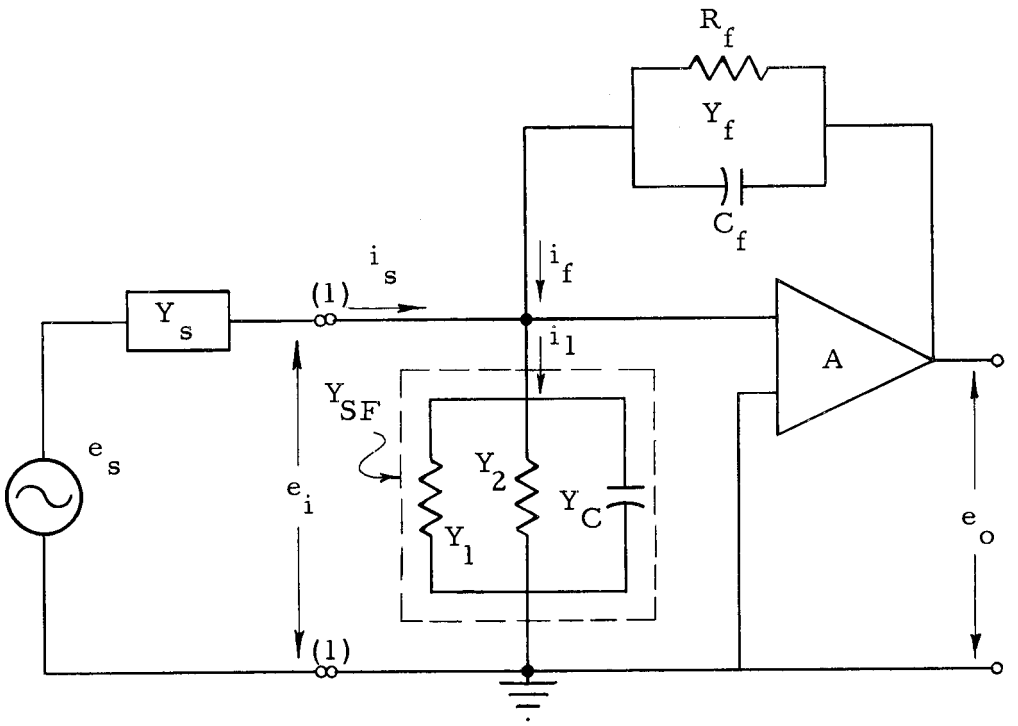

Figure 14. Amplifier with positive feedback.

convenience represented by an admittance Y_S.

INCREASING THE INPUT IMPEDANCE WITH POSITIVE FEEDBACK

The input impedance to be determined corresponds to that seen to the right of point (1)-(1) in Figure 14. For convenience it will be better to deal with admittances.

By adding the currents at the input node the total input admittance, denoted Y_{in}, can be found as follows:

$$i_s = i_i - i_f \tag{IV-1}$$

but

$$i_i = e_i Y_{SF} \tag{IV-2}$$

$$i_f = (e_o - e_i)\, Y_f \tag{IV-3}$$

then,

$$i_s = e_i Y_{SF} - e_o Y_f + e_i Y_f$$

since

$$e_o = A\, e_i$$

$$i_s = e_i\, (Y_{SF} - A Y_f + Y_f)$$

Finally,

$$Y_{in} = \frac{i_s}{e_i} = Y_{SF} - Y_f\,(A-1) \tag{IV-4}$$

Substituting for Y_{SF} and Y_f from Figure 14

$$Y_{in} = Y_1 + [Y_2 + Y_C - Y_{R_f}(A-1) - Y_{C_f}(A-1)] \tag{IV-5}$$

Since the voltage amplification was assumed to be larger than unity, the quantity (A-1) will be positive. Therefore, every term appearing inside the brackets in Equation (IV-5) is positive; this simply is an algebraic sumation of conductances and capacitive susceptances. Now, for any given value of A, it is always possible to choose R_f and C_f such that

$$Y_2 = Y_{R_f}\,(A-1) \tag{IV-6}$$

$$Y_C = Y_{C_f}\,(A-1) \tag{IV-7}$$

For these values of R_f and C_f, such that Equations (IV-6) and (IV-7) hold, the quantity in brackets in Equation (IV-5) vanishes and the input admittance simply reduces to

$$Y_{in} = Y_1 \qquad \text{(IV-8)}$$

where, it should be remembered, Y_1 is a pure conductance.

Thus, it is shown that the appropriate application of positive feedback theoretically eliminates the effects of the input shunt capacitance; what is more, it allows elimination of part of the input shunt resistance. The net result is that the input admittance can be made pure conductance and arbitrarily small; or equivalently the input impedance can be made very high and theoretically free from the shunt capacitance.

VOLTAGE AMPLIFICATION AND STABILITY CONSIDERATIONS

The amplifier voltage amplification denoted by "A" in Figure 14 can be shown to be unaffected by the positive feedback. In the following derivation this amplification, "A", will be considered to remain constant and greater than unity for all frequencies of interests.

The voltage amplification to be dealt with here is that one accounting for the transformation of e_s into e_o; this will certainly

involve all the parameters of Figure 14, and obviously the feedback comes into play. The voltage amplification to be desired then, is

$$A_f = \frac{e_o}{e_s} \tag{IV-9}$$

Again, by adding the currents at the input node,

$$i_s = i_i - i_f$$

$$(e_s - e_i)\, Y_S = e_i Y_{SF} - (e_o - e_i)\, Y_f \tag{IV-10}$$

but

$$e_i = \frac{e_o}{A} \tag{IV-11}$$

then

$$e_s Y_S - e_o \frac{Y_S}{A} = \frac{e_o}{A} (Y_{SF} + Y_f) - e_o Y_f$$

After simplification this becomes

$$A_f = \frac{e_o}{e_s} = \frac{Y_S\, A}{Y_S + Y_{SF} - Y_f(A-1)} \tag{IV-12}$$

Observing this expression, and remembering feedback theory, it can be concluded that for the case when

$$Y_f(A-1) = (Y_S + Y_{SF}) \tag{IV-13}$$

The denominator vanishes, and A_f becomes infinite. This corresponds to the unstable state, and oscillations will occur. Nyquist's criterion could also be applied here in the form that

for stable operation, the relation

$$Y_f\ (A-1) \ < \ (Y_S + Y_{SF}) \qquad \text{(IV-14)}$$

should hold for all frequencies.

The above discussion of stability was very generalized. To take into account other requirements that the amplifier must meet simultaneously, substitute Y_{SF} and Y_f from Figure 14 (page 30)

$$A_f = \frac{Y_S \quad A}{Y_S + Y_1 + [\,Y_2 + Y_C - Y_{R_f}(A-1) - Y_{C_f}(A-1)]} \qquad \text{(IV-15)}$$

The quantity in brackets is the same as the one encountered in relation with the input impedance, see Equation (IV-5), page 31, and as mentioned before, this quantity should be made equal to zero in order to achieve high input impedance.

It follows then, that if the amplifier is designed for high input impedance, with (ideally) no shunt capacitance, the voltage amplification simply reduces to

$$A_f = \frac{Y_S}{Y_S + Y_1} \quad A \qquad \text{(IV-16)}$$

In this expression all the parameters are positive quantities, and therefore there is no danger of oscillations.

It would be of interest to compare the amplification with feedback, as given by Equation (IV-16), and the similar

amplification in the absence of feedback. This latter amplification can be found from Figure 14, as

$$A_T = \frac{Y_S}{Y_S + Y_{SF}} \quad A \qquad \text{(IV-17)}$$

Since $Y_{SF} > Y_1$, the amplification with feedback is larger than the one without feedback.

In conclusion, the use of positive feedback for increasing the input impedance and eliminating the shunt input capacitance simultaneously yields a very stable amplifier.

V. AN EXPERIMENTAL HIGH INPUT IMPEDANCE WIDE BAND TRANSISTORIZED AMPLIFIER

This section is devoted to the description and discussion of an amplifier which was breadboarded and tested in the laboratory. This amplifier was assembled more to test the validity of the theory and criteria presented in previous sections than to demonstrate the practical aspects of amplifier design. It would be appropriate to mention at the onset that the components used, and this is especially true of the transistors used, are the ones immediately available rather than the choice of a sound judgement. The design was essentially made around the available FET, which happened to be an experimental unit made by Texas Instruments.

The amplifier built consists of three stages; a source follower input stage followed by two transistor (conventional transistors) stages. No theoretical discussion will be attempted for this particular amplifier since it would be essentially a repetition of the generalized theory presented earlier. However, use of the equations previously derived will be made whenever the occasion arises.

THE INPUT STAGE

Figure 15 shows a diagram of the source follower used

as the input stage, along with the value of each component. The FET used was a TI x 881, an experimental unit made by Texas Instruments. The drain source output characteristics are shown in Figure 4, page 7 .

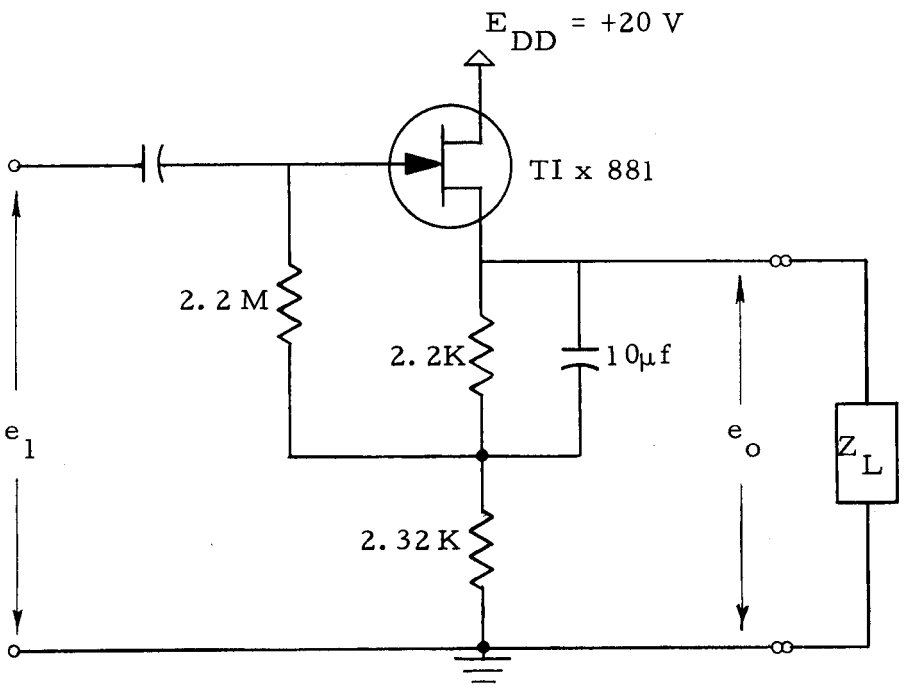

Figure 15. The source-follower input stage.

From the curves in this figure one can approximately compute (see FET equivalent circuit, page 12).

$$r_D = \left.\frac{\Delta e_D}{\Delta i_D}\right|_{E_{g\text{-}s}=-0.4\ V} = \frac{3}{03x0^{-3}} = 100\ K\ ohms \quad (V\text{-}1)$$

$$g_m = \left.\frac{\Delta i_D}{\Delta e_g}\right|_{E_{D\text{-}s}=10\ V} = \frac{.16x10^{-3}}{.2} = 800\ \mu mhos \quad (V\text{-}2)$$

From the characteristics of Figure 4 it is seen that for linear operations this FET should have a drain-source bias of over 10 volts. This voltage serves no vital functional purpose, and being rather high makes this FET rather incompatible for use with conventional transistors which usually are operated at low voltages. Notice that the source follower of Figure 15 requires a d-c supply of 20 volts, which is rather high for transistor circuits. Thus, in the interest of better compatibility with conventional transistors it would be desirable to have FETs with low pinch off voltage (refer to page 8).

Computation of the input impedance and voltage amplification requires a knowledge of the load, Z_L. In this case the load was the input impedance of the next stage, and it would be better to briefly discuss the following stage before performing any computations.

THE SECOND AND THIRD STAGES

It should be remembered that the purpose of the second and third stages is to isolate the signal to be fedback, and to provide amplification such that the overall amplification of the whole amplifier is larger than one.

These amplifying stages have to be designed for wide band

amplification, to be compatible with the ultimate goal. Furthermore, since the voltage amplification of the first stage is a function of the load, these amplifying stages must present a relatively high input impedance; that is high with respect to R_K of Figure 10 (page 15) as can be deduced from Equations (III-3) and (III-6). The two requirements mentioned here are nicely met by a common-emitter amplifier with emitter degeneration. The two stages were designed identically the same and are as shown in Figure 16.

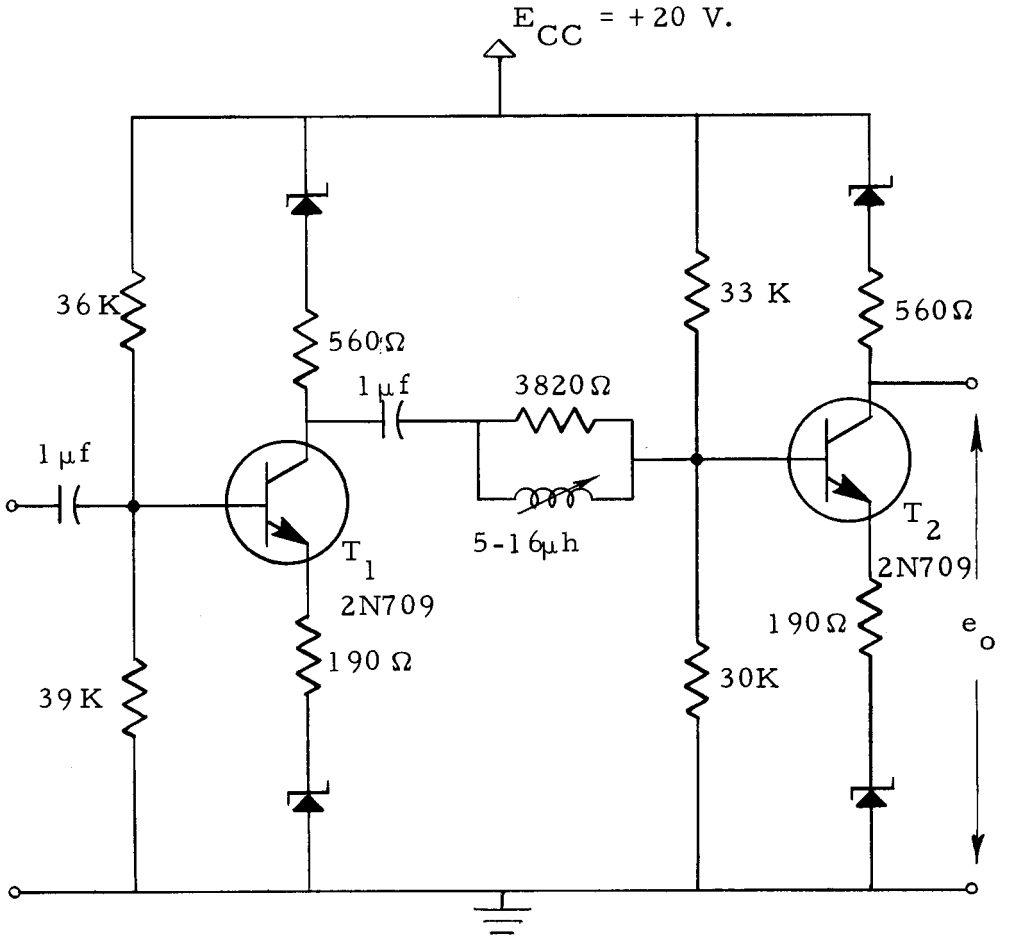

Figure 16. Second and third amplifier stages.

The four zener diodes shown in the diagram were necessary to make the transistors compatible with 20 d-c supply required by the FET. The transistors used were Fairchild's 2N709; these transistors are switching transistors, but were the only high frequency transistors available. The disadvantage of the 2N709 is the low collector-emitter breakdown voltage -- in the neighborhood of three to four volts. The variable inductor shown was used for series peaking in order to improve the frequency response. The low frequency β's were measured at

$$\beta_1 = 60 \qquad (V-3)$$

$$\beta_2 = 160 \qquad (V-4)$$

VOLTAGE AMPLIFICATION FREQUENCY RESPONSE

Figure 17 shows a complete diagram of the experimental amplifier built and tested.

The voltage amplification provided by the amplifier is

$$A = \frac{e_o}{e_1} \qquad (V-5)$$

This voltage ratio is independent of whether the feedback branch is connected or not; it is also independent of the signal source resistance, R_S. Figure 18 shows a graph of the voltage amplification vs. frequency. If the minus three db's points are

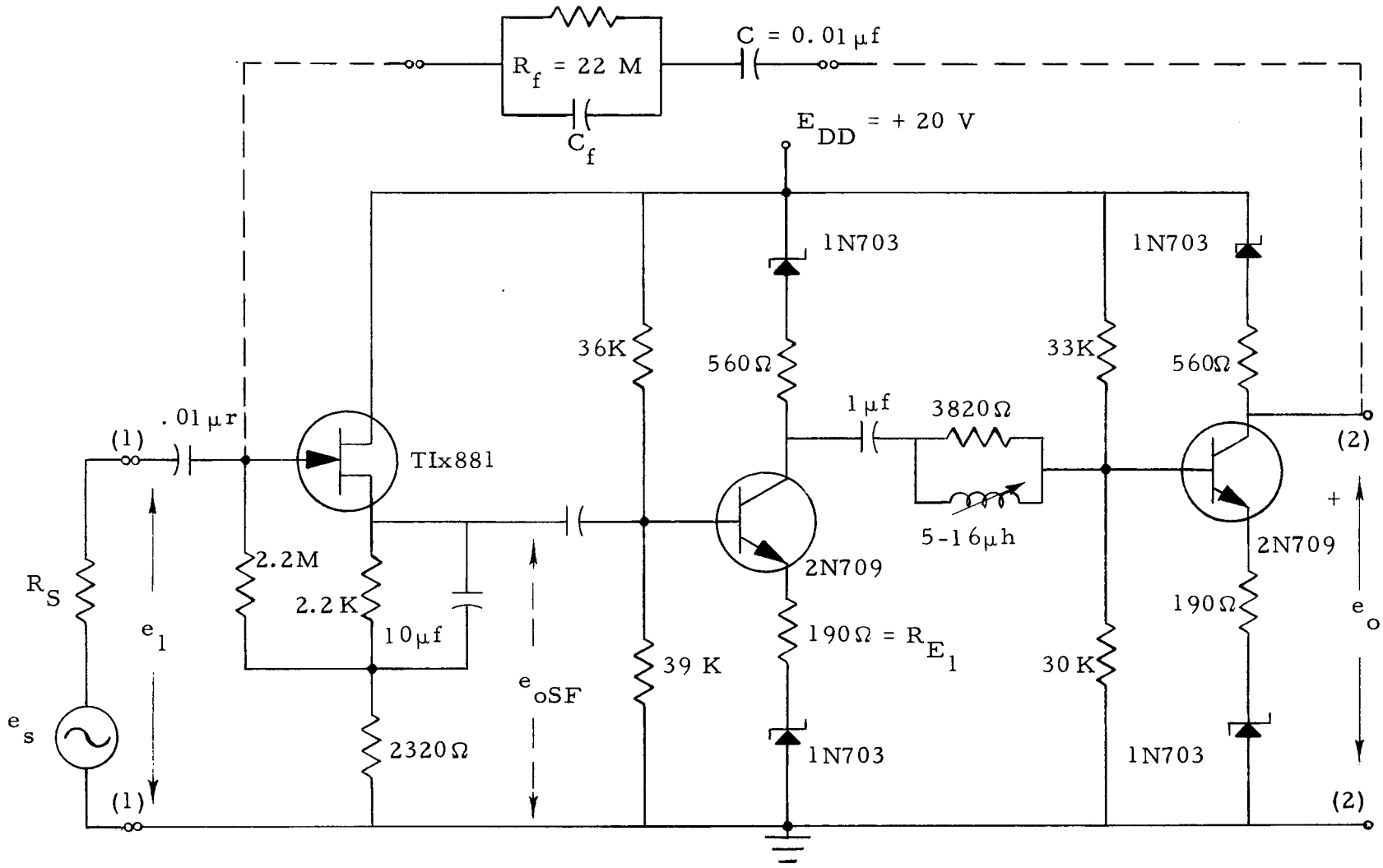

Figure 17. Complete diagram of the experimental amplifier.

taken as the limits, then the amplifier has a band width extending from 30 cps to about 10 Mc. Figure 18 also shows the voltage amplification frequency response for the source follower. This voltage amplification was measured in the circuit of Figure 17 as

$$A_{SF} = \frac{e_{oSF}}{e_1} \qquad (V-6)$$

It can be seen from Figure 18 that the bandwidth is limited by the two transistorized stages rather than by the source follower; this simply suggests that if a better amplifying stage could be obtained the overall response would be better. The measured overall voltage gain was found to be

$$A = 4.58 \qquad (V-7)$$

As it will be shown further on, it is not necessary to have this much voltage gain. Therefore, one immediate solution to improving the frequency response would be trading gain for bandwidth.

When computing the theoretical voltage amplification of the source follower, notice that the input impedance of the second stage, at low frequencies and disregarding the base biasing network is $Z_{in_1} \simeq \beta_1 R_{E_1} = (60)(190) = 11.4\,K\Omega$

Taking the base biasing network into account

$$Z_{in_{1T}} \simeq 7.1\,K\Omega \qquad (V-8)$$

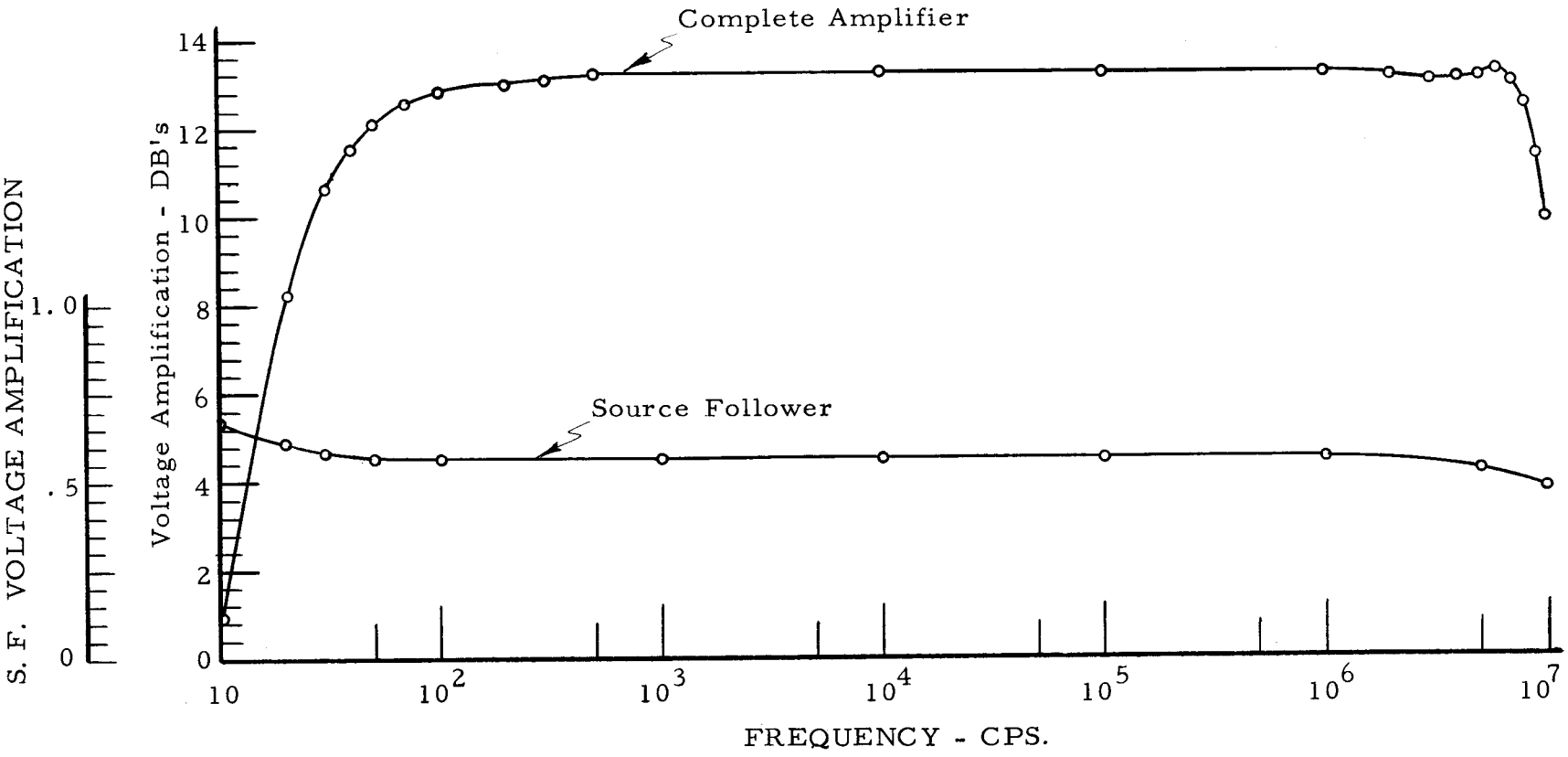

Figure 18. Voltage amplification frequency response.

By substituting this value and the values given by Equations (V-1) and (V-2), and the values shown in Figure 17 into Equation (III-6) it is possible to evaluate the source follower voltage amplification at low frequencies. Assuming $R_G << R_3$ in Figure 12, the approximate value is

$$A_{SF} = 0.58 \qquad (V-9)$$

which agrees reasonably well with the measured value (Figure 18) of

$$A_{SF} = 0.56 \qquad (V-10)$$

INPUT IMPEDANCE MEASURING TECHNIQUE

The measurement of the input impedance requires special care, because high impedances are involved. The technique here used can be better described by referring to Figure 19 where the amplifier (between points (1)-(1) to (2)-(2) in Figure 17) has been divided into an input impedance Z_{in} and an ideal amplifier (infinite input impedance) with a voltage amplification "A". This representation is valid whether the feedback is present or not, the only difference being Z_{in}.

Since the voltage amplification "A" is known for all frequencies of interest from the graph of Figure 18, it is possible to

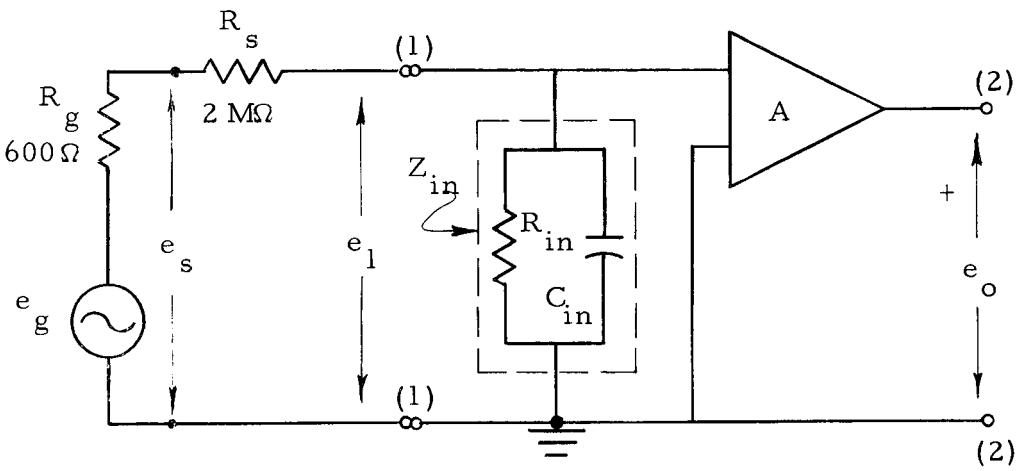

Figure 19. Circuit arrangement for measuring the input impedance.

determine e_1 in Figure 19 by simply measuring e_o. This procedure enables taking the measurement across a relatively low impedance as is the output of the amplifier; therefore, the input impedance of the measuring instrument introduces very negligible error, which would not be true if e_1 were measured directly.

Determining Z_{in} effectively reduces to determining R_{in} and C_{in}. This can be done as follows. For the voltage divider consisting of R_S and Z_{in} one can write

$$e_1 = \frac{Z_{in}}{R_S + Z_{in}} \quad e_S \tag{V-11}$$

Using Laplace transformation

$$Z_{in} = \frac{R_{in} \dfrac{1}{sC_{in}}}{R_{in} \dfrac{1}{sC_{in}}} = \frac{R_{in}}{R_{in} C_{in} s + 1} \tag{V-12}$$

Substituting this into Equation (V-11) and simplifying, the following ratio is found

$$\frac{e_1}{e_S} = \frac{\frac{1}{R_S C_{in}}}{s + \frac{1}{\frac{R_S R_{in}}{R_S + R_{in}} C_{in}}} \qquad (V-13)$$

For sinusoidal voltages, this can easily be shown to become

$$\frac{e_1}{e_S} = \frac{\frac{1}{R_S C_{in}}}{jW + \frac{1}{\frac{R_S R_{in}}{R_S + R_{in}} C_{in}}} \qquad (V-14)$$

From either Equation (V-13) or (V-14) it is seen that at low frequencies (below the corner frequency), the ratio simply becomes

$$\frac{e_1}{e_S} = \frac{\frac{1}{R_S C_{in}}}{\frac{1}{\frac{R_S R_{in}}{R_S + R_{in}} C_{in}}} = \frac{R_{in}}{R_S + R_{in}} \qquad (V-15)$$

or solving for R_{in}

$$R_{in} = \frac{R_S}{\frac{e_S}{e_1} - 1} \qquad (V-16)$$

At low frequencies e_S and e_1 are in phase and by

measuring their magnitudes and knowning the value of R_S it is easy to compute the value of R_{in}.

The quantity of Equation (V-14) is complex and can be fully characterized by a magnitude and an angle. However, it is also possible to deal only with the magnitudes, thus

$$\frac{|e_1|}{|e_S|} = \frac{\frac{1}{R_S C_{in}}}{\left| jW + \frac{1}{\frac{R_S R_{in}}{R_S + R_{in}} C_{in}} \right|} \qquad \text{(V-17)}$$

By simply measuring the magnitude of e_1 and e_S for different frequencies it is possible to obtain a plot of the magnitude of Equation (V-17) with frequency. This yields a graph similar to the Bode diagram. In this diagram one could easily recognize the corner frequency at which the magnitude has dropped to 0.707 of its magnitude at lower frequencies. From Equation (V-17) it is also seen that at the corner frequency, W_o,

$$W_o = \frac{1}{\frac{R_S R_{in}}{R_S + R_{in}} C_{in}} \qquad \text{(V-18)}$$

from which

$$C_{in} = \frac{1}{\frac{R_S R_{in}}{R_S + R_{in}} W_o} \qquad \text{(V-19)}$$

This expression gives the input capacitance function of the corner frequency, W_o, and the parallel combination of R_S and R_{in}.

INPUT IMPEDANCE FREQUENCY CHARACTERISTICS

Figure 20 shows curves corresponding to Equation (V-17) determined experimentally; this includes both for the amplifier without feedback and with feedback. There are also additional curves for the case of different values of capacitance, C_f in Figure 17, used in the feedback circuit. These curves, it should be emphasized, do not represent in themselves Z_{in} vs. frequency; however they do contain a qualitative indication of Z_{in}. As mentioned above, and since the same value of R_S was used throughout, their curves, at the lower frequencies, are closely associated to R_{in} (see Equation V-16), and the corner frequency is associated with C_{in} (see Equation V-19). From these curves, qualitatively, the higher the value of R_{in} the greater the magnitude of these curves at the low frequencies, and the lower C_{in} the higher the corner frequency.

For the case of no feedback, from the corresponding curve of Figure 20 and Equations (V-17) and (V-19), it was

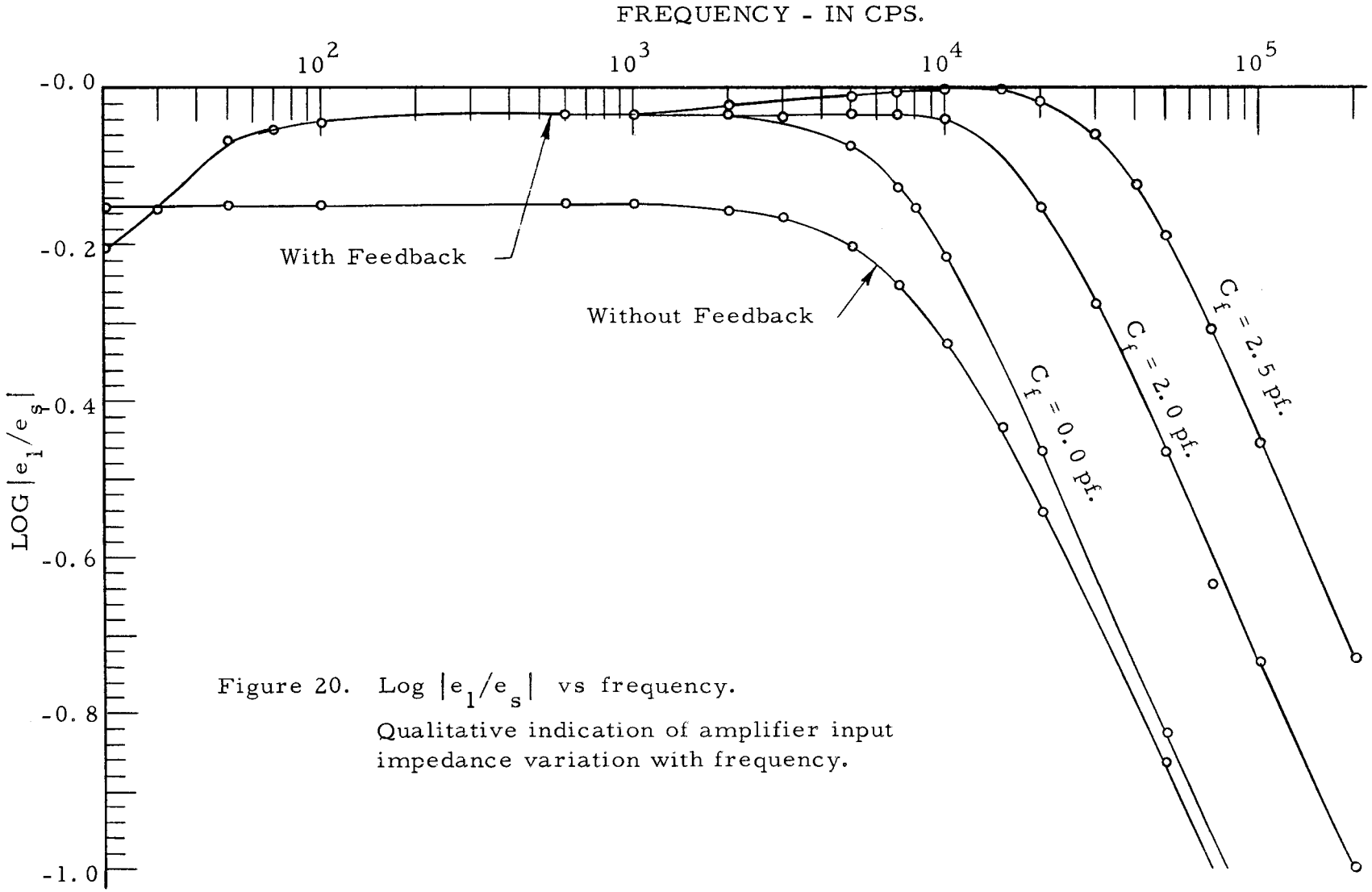

Figure 20. Log $|e_1/e_s|$ vs frequency.

Qualitative indication of amplifier input impedance variation with frequency.

found

$$R_{in} = 4.8\ M\Omega \qquad (V-20)$$

$$C_{in} = 12.6\ pf \qquad (V-21)$$

Similarly when feedback was applied the following results were obtained (see corresponding curves in Figure 20).

R_f	C_f	R_{in}	C_{in}	
22 MΩ	0 pf.	20.7 MΩ	9.36 pf.	(V-22)
22 MΩ	2 pf.	20.7 MΩ	3.83 pf.	(V-23)
22 MΩ	2.5 pf.	20.7 MΩ	1.7 pf.	(V-24)

From the above results the improvement in input impedance is quite evident.

Although only one value of resistance was used in the feedback branch, three different values of capacitance, C_f, were used. The curves of Figure 20 depict the influence of this C_f on the input inpedance vs. frequency. For $C_f = 2$ pf, the curve shows a flat portion and then decays gradually at higher frequencies as would be expected of circuits containing R and C in parallel. The curve corresponding to $C_f = 2.5 \pm 0.25$ pf, however, shows a little hump at around the corner frequency. This response is associated with overcompensation, that is the value of C_f is larger than required, or referring to Equation (IV-7) it is such

that

$$Y_{C_f} \ (A-1) > Y_C \qquad (V-25)$$

The value of the input resistance with positive feedback applied, R_{in-f}, can also be found theoretically. This requires a knowledge of the voltage gain, A, the feedback resistance, R_f, and the input resistance without feedback, R_{in}. From earlier discussion it should be remembered that the positive feedback essentially produces a negative resistance in shunt with R_{in}. The value of this negative resistance is, from Equation (IV-6),

$$-\frac{R_f}{A-1} = -\frac{22\times10^6}{4.58-1} = -6.15 \text{ M}\Omega \qquad (V-26)$$

When this negative resistance is combined in parallel with R_{in} there results

$$R_{in-f} = \frac{(4.8\times10^6)(-6.15\times10^6)}{4.8\times10^6 - 6.15\times10^6} = 21.8 \text{ M}\Omega \qquad (V-27)$$

which would be the value of the input resistance with positive feedback. This theoretical result compares quite well with the measured value of 20.7 MΩ.

By reversing the above process it would be possible to estimate the required value of R_f for any predetermined value of input resistance. Thus, positive feedback provides a flexible

and easy way of obtaining any desired input resistance.

Theoretically, as it was mentioned earlier, the input capacitance, C_{in}, could be completely eliminated. In practice this is not quite true; there is always some stray capacitance present. Positive feedback, nevertheless, as demonstrated by the experimental results, is of definite help in minimizing this input capacitance. The amplifier tested was simply assembled in a bread-board, and no extra special care was given to proper component layout. In any amplifier constructed properly, it can confidently be stated that the input capacitance can be reduced to fractions of one picofarad.

Going back to Equation (IV-6), which essentially represents the resistance to be subtracted from the input resistance,

$$R_2 = \frac{R_f}{(A-1)} \tag{V-28}$$

solving for R_f

$$R_f = R_2 (A-1) \tag{V-29}$$

For high input impedance R_2 will be in the megaohm region, and R_f will be (A-1) times higher. For high values of voltage amplification Equation (V-29) could give rather impractically high values of R_f. From this consideration, it would be better to have low values of voltage amplification. Since the only requirement is

for the voltage amplification to be larger than unity, values between two and three seem to be adequate.

VI. CONCLUSION

In this thesis it has been shown that the Field Effect Transistor, FET, is inherently a high input impedance device. It was further shown that the FET used in the source-follower configuration provides high input impedance, wideband voltage amplification, and low output impedance. These were found to be desirable characteristics in the development of high input impedance wideband amplifiers. Next, the theory of positive feedback as applied to high input impedance amplifiers was presented; it was shown that this type of feedback can be advantageously used for increasing the input impedance. Under proper design, it was found, the possibility of oscillations can be completely eliminated. Positive feedback was also shown to have no effect on the voltage amplification of the amplifier itself; however, when the signal source internal resistance is considered in the overall amplification, positive feedback was found to keep the overall amplification higher because of the increased amplifier input impedance.

The experimental amplifier, built and tested in the laboratory, was found to have a bandwidth of from 30 cps to around 10 Mc if the minus three db points are taken as the limits. The

input impedance obtained is indicated in the following table

	No Feedback	With Feedback
R_{in}	4.8 MΩ	20.7 MΩ
C_{in}	12.6 pf.	1.7 pf

SOME CLOSING REMARKS

It was the aim of this thesis to develop the necessary criteria for the design of high input impedance wide band amplifiers; this much has been successfully accomplished. However, there still remains two other important areas to be investigated before the above described experimental amplifier can be confidently used, and these areas are: stability with temperature variations, and the noise level.

As already pointed out, the experimental amplifier was assembled using whatever component was available and no special regard was given to temperature stability or noise level. For the case of conventional transistors, there are well established criteria for the design of highly stable low noise amplifiers. These criteria could undoubtedly be applied to the amplifier described in this thesis, assuming there is a flexible choice of components. As for the input stage containing the FET this much can be stated: First, the FET inherently has a lower noise level

than conventional transistors (see page 6); and second, the temperature variations are similar to that of conventional transistors suggesting that similar criteria could be applied.

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