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John F. Wager

Amorphous oxide semiconductors (AOSs) are of great current interest for thin-film transistor (TFT) channel layer applications. In particular, indium gallium zinc oxide (IGZO) is under intense development for commercial applications because of its demonstrated high performance at low processing temperatures. The objective of the research presented in this thesis is to provide detailed assessments of device stability, temperature dependence, and related phenomena for IGZO-based TFTs processed at temperatures between 200 °C and 300 °C. TFTs tested exhibit an almost rigid shift in $\log_{10}(I_D) - V_{GS}$ transfer curves in which the turn-on voltage, V_{ON}, moves to a more positive gate voltage with increasing stress time during constant-voltage bias-stress testing of IGZO TFTs. TFT stability is improved as the post-deposition annealing temperature increases over the temperature range of 200 – 300 ºC. The turn-on voltage shift induced by constant-voltage bias-stressing is at least partially reversible; V_{ON} tends to recover towards its initial value of V_{ON} if the TFT is left unbiased in the dark for a prolonged period of time and better recovery is observed for a longer recovery period. V_{ON} for a TFT can be set equal to zero after bias-stress testing if the

TFT electrodes are grounded and the TFT is maintained in the dark for a prolonged period of time. Attempts to accelerate the recovery process by application of a negative gate bias at elevated temperature (i.e., 100 ºC) were unsuccessful, resulting in severely degraded subthreshold swing. An almost rigid $\log_{10}(I_D)$ $-V_{GS}$ transfer curve shift to a lower (more negative) V_{ON} with increasing temperature is observed in the range of –50 °C to +50 °C, except for a TFT with an initial V_{ON} equal to zero, in which case the $\log_{10}(I_D)$ – V_{GS} transfer curve is temperature-independent. A more detailed temperature-dependence assessment, however, indicates that the $\log_{10}(I_D)$ – V_{GS} transfer curve shift is not exactly rigid since the mobility is found to increase slightly with increasing temperature. A noticeable anomaly is observed in certain $\log_{10}(I_D)$ – V_{GS} transfer curves, especially when obtained at elevated temperature (e.g., 30 and 50 ºC), in which I_D decreases precipitously near zero volts in the positive gate voltage sweep. This anomaly is attributed to a gate-voltage-step-involved detrapping and subsequent retrapping of electrons in the accumulation channel and/or channel/gate insulator interface. In fact, all IGZO TFT stability and temperature-dependence trends are attributed to channel interface and/or channel bulk trapping/detrapping.

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Ken Hoshino, Author

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STABILITY AND TEMPERATURE-DEPENDENCE ASSESSMENT OF IGZO TFTS

1 Introduction

Ever since the first transistor was introduced, almost all circuits based on semiconductor technology have been made progressively smaller and smaller, following Moore's law [1]. The gate lengths of a transistor implemented in current state-of-the-art integrated circuits are now as small as 45 nm. Such integrated circuits are based on the use of single crystal silicon and are designed to make the entire circuit as small as possible, thereby shrinking the die size and keeping the cost low.

Recently, other circuit integration technologies have emerged, in which, to some extent, an opposite design strategy is employed; namely, to cover as large of an area as possible with circuit functionality. The most well-known examples of this type of technology are flat-panel displays and solar cells. These technologies require relatively low process temperatures since the substrate is usually glass or a clear plastic, such as polyethylene terephthalate (PET), instead of the conventionally-used silicon substrate. Thus, the cost structure and development paradigm of silicon integrated circuit technology and large-area electronics are dramatically different.

The first large-area electronics material to be commercialized was hydrogenated amorphous silicon (a-Si:H) introduced by Spear and LeComber [2]. However, a-Si:H inherently possesses several drawbacks. The two most critical are its low carrier mobility, ~1 $cm^2V^{-1}s^{-1}$ [3], and its relatively poor stability. A low mobility limits the drive current capability and frequency performance of a thin-film transistor (TFT). The poor stability of a-Si:H TFTs constains their utility for many electronics

applications. Nonetheless, a-Si:H TFTs are used extensively as high dynamic range, voltage-controlled switches in active-matrix liquid-crystal displays (AMLCDs), which is a multi-billion dollar industry today.

In 1996, Kawazoe *et al.* at the Tokyo Institute of Technology reported on a novel inorganic oxide family of materials involving the use of multi-component combinations of heavy-metal cations [4]. These materials will be referred to in this thesis as amorphous oxide semiconductors (AOSs). Besides the visible transparency of many of the materials in this class, one of the most attractive characteristics of AOSs is their relatively high mobility. Their mobility is roughly ten times larger than that of a-Si:H, even though these materials possess an amorphous microstructure. Many of these AOSs have been used as transparent thin-film transistors (TTFTs). Some TTFT-based integrated circuits have already been reported [5][6].

Although AOS-based TTFTs have the potential to replace a-Si:H TFTs from a mobility point-of-view, little work has been devoted to the stability assessment of these devices, comparing to a-Si:H TFTs. The purpose of this thesis is to investigate the stability and temperature dependence of indium gallium zinc oxide (IGZO)-based TTFTs, extending the work initiated by Hung [7].

This thesis consists of the following topics: Chapter 2 provides background information related to TFT materials, structure, modeling, and assessment. Chapter 3 overviews device preparation and fabrication techniques employed. Chapter 4 and 5 supply stability test results and temperature dependence assessments, respectively. Chapter 6 provides physical insight of non-ideal phenomena observed in Chapter 4

and 5. Chapter 7 presents conclusions and proposes recommendations for future research.

2 LITERATURE REVIEW

2.1 Thin-Film Transistor Types

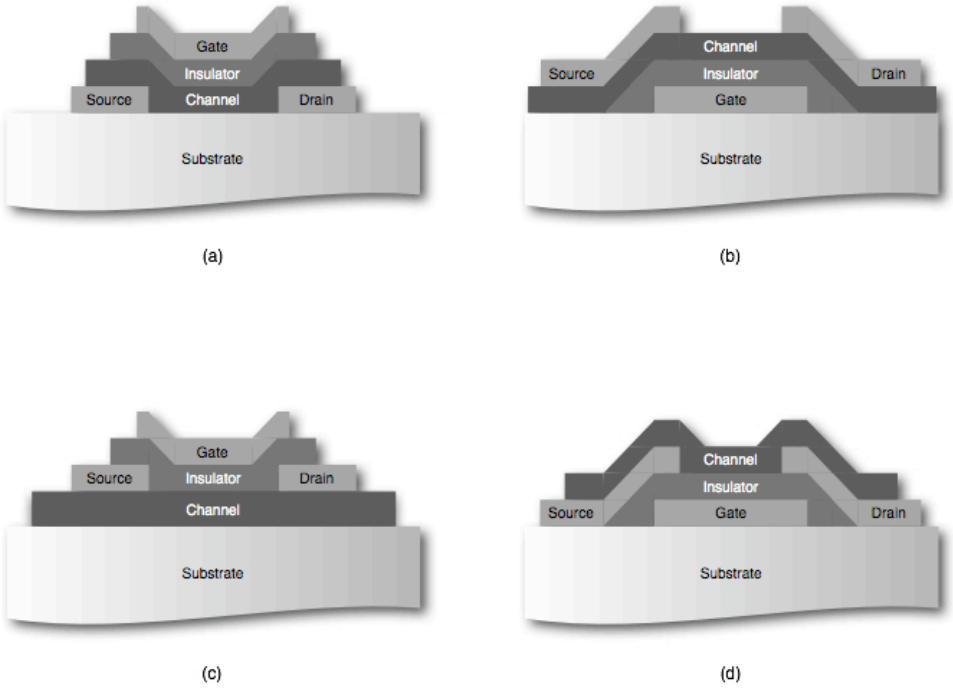


Figure 2.1: Thin-film transistor configurations: (a) staggered top-gate, (b) staggered bottom-gate, (c) coplanar top-gate, and (d) coplanar bottom-gate.

Four different configurations exist for thin-film transistors (TFTs), as depicted in Fig. 2.1: a) staggered top-gate, b) staggered bottom-gate, c) coplanar top-gate, and d) coplanar bottom-gate. This classification is defined by the gate electrode location and the relative position of the source / drain and the gate terminals. If the gate is on the channel layer, the device is in a top-gate configuration. In contrast, if the gate is below the channel layer, it is in a bottom-gate configuration. When the source / drain terminals are on the opposite side of the gate terminal across the channel layer, the device is in a staggered configuration. Likewise, if the source / drain terminals are on

the same side of the channel layer as the gate terminal, the configuration is in a coplanar arrangement.

There are four arrangement combinations of these two different gate locations and two different relative locations of the gate and the source/drain terminals, shown in Fig. 2.1. This notation was originally devised by Weimer [8], according to Tickle [9]. Advantages and disadvantages associated with fabricating different structural types are somewhat dependent upon the substrate type and TFT materials used and are not considered any further in this thesis.

TFTs may also be classified from an electrical characteristic point-of-view as either enhancement-mode or depletion-mode. The criterion for this distinction involves the gate voltage required to turn on the device and induce conduction current. If the device conducts current even when no voltage is applied to the gate terminal (normally-on), the device is called a depletion-mode device. In contrast, if the device does not conduct current when zero voltage is applied to the gate electrode, the device is called an enhancement-mode device. In other words, for an n-channel device, if the required applied gate voltage to turn the TFT on is positive, the device is an enhancement-mode device. On the other hand, if the required applied gate voltage is negative, the device is classified as depletion-mode. In practical applications, an enhancement-mode transistor is preferred for several reasons: lower power consumption (no gate voltage is necessary to turn off the device) and simpler circuit configuration (no extra circuits are required to turn off the device).

2.2 MIS Transistor Models and Operation

There are two different types of metal-insulator-semiconductor (MIS) devices which utilize different current conduction mechanisms. One exploits the creation of an inversion layer which electrically bridges the source and drain, giving rise to a drain current. A MOSFET is an example of this type. The other device type utilizes an accumulation layer to establish drain current. A TFT belongs to this class. Thus, it is not surprising that there are some differences between the device physics operation of a MOSFET and a TFT.

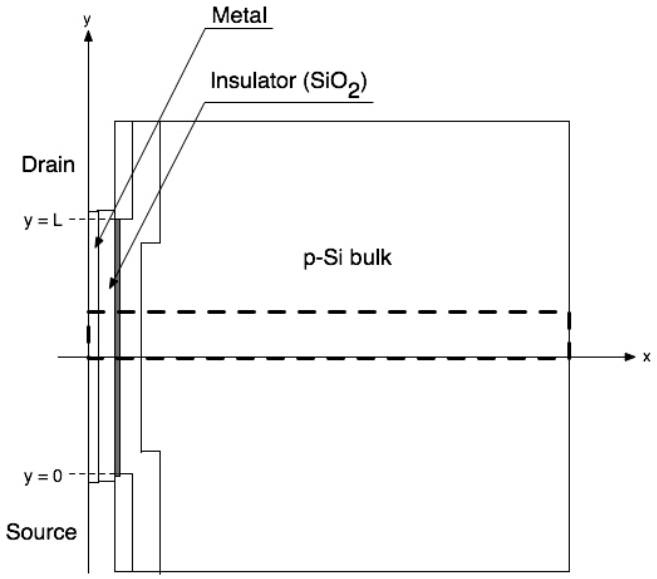
In the following subsections, a MOSFET model is presented and then refined so that it is applicable to TFTs.

2.2.1 Inversion-mode MOSFET Operation

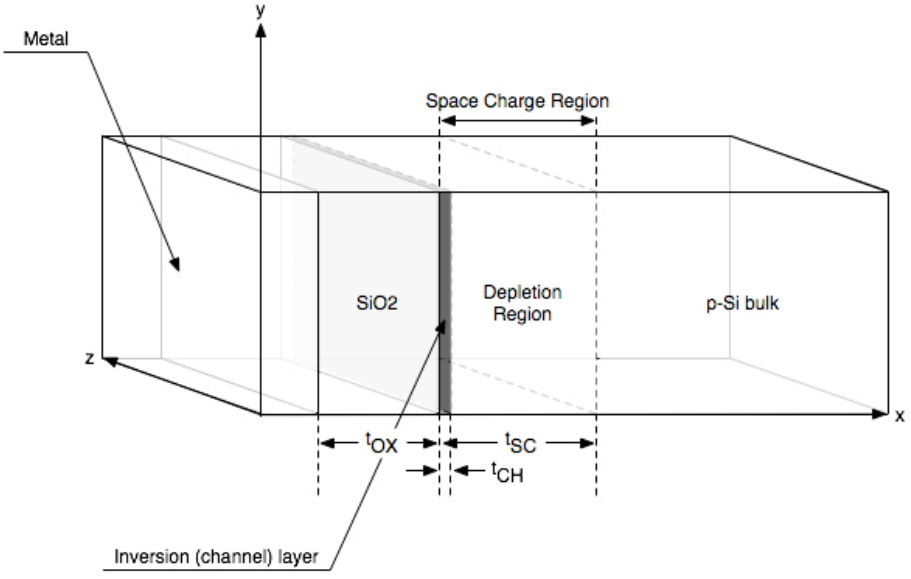
A simplified, long-channel MOSFET model, the conductivity modulation model [10], is presented in this subsection. A more accurate long-channel MOSFET model, the Pao-Sah model, which incorporates diffusion current as well as drift current [11], is also available but is not discussed because of its additional complexity [12].

Several modeling assumptions should be mentioned. First, the gradual channel approximation (GCA) constitutes the fundamental assumption for both the long-channel MOSFET and TFT model derivations. The GCA was originally introduced by Shockley in 1952 in a derivation of a junction field-effect transistor (JFET) model [13]. The GCA asserts the change in the electric field along the channel is much weaker than that normal to the channel. This is approximately equivalent to making the channel length, L, much larger than the oxide thickness, t_{OX}. Additionally, the

GCA implies that the two-dimensional electric field problem in the channel may be separated into two one-dimensional problems.



(a)



(b)

Figure 2.2: A simplified illustration of a long-channel MOSFET. (a) A cross-sectional view and (b) an enlarged view of the region identified with a dashed line in (a).

The second assumption, proposed by Brews [14], asserts that the inversion layer thickness, t_{CH}, is infinitesimally small ($t_{CH} \sim 0$). Because of this assumption, Brew's model is often referred to as the charge-sheet model. The basic idea of this model was originally introduced by Loeb *et al.* [15] in the context of a numerical mesh computation to calculate the electric field distribution in the inversion layer. Practically speaking, the charge sheet model assumes that there is no potential drop across the inversion layer along x-axis. In addition, the channel is assumed to never pinch-off at the drain, even after the gate-drain potential difference becomes less than the threshold voltage, V_T, i.e., the potential drop from the drain to the source is "pinned" at $V_{DS} = V_{GS} - V_T$ when the gate-drain voltage, V_{DG}, becomes less than V_T. Although clearly the gradual channel approximation is violated near the region close to the drain, the charge-sheet model well-describes the drain current dependence on the gate and drain potentials.

The third assumption is called the depletion approximation and includes two simplifications: 1) no carriers exist inside the depletion region, and 2) no charge exists outside the depletion region. This assumption simplifies the charge distribution to that of a step junction.

Now the MOSFET model may be derived. The following derivation mostly follows Sah [10]. The semiconductor is p-type and the source terminal is presumed to be grounded. With the drain potential, V_D, kept below the gate level minus the threshold level (i.e., $V_{DS} < V_{GS} - V_T$), an inversion layer is created underneath the gate insulator when the gate voltage exceeds the threshold level. This inversion layer

bridges the drain and the source, creating a path for current. The current density along the y-axis is given as

$$J_N(x,y,z) = q\mu_N(x,y,z)n(x,y,z)\xi(x,y,z) + qD_N(x,y,z)\nabla n(x,y,z), \tag{2.1}$$

where q is the elementary charge, $\mu_N(x,y,z)$ is the surface mobility in the channel which is smaller than that in the bulk, $n(x,y,z)$ is the electron density, $\xi(x,y,z)$ is the electric field, and $D_N(x,y,z)$ is the diffusion constant.

Assuming that the device channel width, W, is much larger than the length, L, so that fringing effects are negligible and all functions are independent of the z-axis,

$$J_N(x,y) = -q\mu_N(x,y)n(x,y)\xi_y(x,y) + qD_N(x,y)\frac{\partial}{\partial y}n(x,y), \tag{2.2}$$

where $\xi_y(x,y)$ is the electric field along the channel. Since the barrier at the source pn junction is lowered by the channel creation, the drain current is regulated only by the electric field between the source and drain when the gate-channel voltage is greater than the threshold voltage, V_T. This means that the dominant current mechanism is drift, leading to

$$J_N(x,y) \cong -q\mu_N(x,y)n(x,y)\xi_y(x,y). \tag{2.3}$$

Applying the GCA and integrating this current density expression over the cross section of the channel with the assumption that all current conduction occurs in the channel,

$$I_D = \int_0^W \int_0^{t_{CH}} J_N(x,y)dxdz \cong -W\int_0^{t_{CH}} \mu_N(x,y)qn(x,y)\xi_y(x,y)dx. \tag{2.4}$$

Assuming that the electric field is small enough that linear transport may be assumed,

$$I_D \cong -W\mu_{EFF}\int_0^{t_{CH}} qn(x,y)\xi_y(x,y)dx, \tag{2.5}$$

where μ_{EFF} is the effective mobility, as discussed in the next subsection. Also applying the charge-sheet model to this expression, the electric field inside the insulator can be presumed to be uniform along x-axis because of its infinitesimal thickness. Thus, the electric field is independent of x, and the expression becomes

$$I_D \cong -W\mu_{EFF}\int_0^{t_{CH}} qn(x,y)\xi_y(y)dx = -W\mu_{EFF}\left(-\frac{dV}{dy}\right)\int_0^{t_{CH}} qn(x,y)dx. \tag{2.6}$$

The integration term represents the total charge induced in the channel, which is approximated as

$$\int_0^{t_{CH}} qn(x,y)dx \cong \int_0^{\infty} q\left[n(x,y)-N_B\right]dx = C_{OX}\left[V_{GS}-V_T-V(y)\right], \tag{2.7}$$

where n is the electron concentration, N_B is the electron concentration in equilibrium, and V(y) is the channel potential as a function of the distance along the channel, y. Substituting Eq. 2.7 into Eq. 2.6,

$$I_D = W\mu_{EFF}\left(\frac{dV}{dy}\right)C_{OX}\left[V_{GS}-V_T-V(y)\right]. \tag{2.8}$$

Integrating along the channel,

$$\int_0^L I_D dy = \int_0^L W\mu_{EFF}\left(\frac{dV}{dy}\right)C_{OX}\left[V_{GS}-V_T-V(y)\right]dy = W\mu_{EFF}C_{OX}\int_{V_S}^{V_D} V_{GS}-V_T-V(y)dV$$

$$\Leftrightarrow LI_D = W\mu_{EFF}C_{OX}\left\{\left[V_{GS}-V_T\right]\left[V_D-V_S\right]-\frac{1}{2}\left[V_D{}^2-V_S{}^2\right]\right\} \tag{2.9}$$

Since the source is assumed to be grounded, this equation is equal to

$$I_D = \frac{W\mu_{EFF}C_{OX}}{L}\left\{[V_{GS} - V_T]V_{DS} - \frac{1}{2}{V_{DS}}^2\right\}, \tag{2.10}$$

where V_{DS} is the drain potential with respect to the source. This is the simplified drain current model for a long-channel MOSFET when $V_{DS} < V_{GS} - V_T$. Since an inversion layer exists from the drain to the source, this operational regime is referred to as pre-saturation.

When the drain voltage increases beyond that of the gate overvoltage ($V_{DS} > V_{GS} - V_T$), the inversion layer close to the drain becomes depleted, causing the drain current to saturate. For this reason, this operational region is dubbed saturation. However, as mentioned previously in the context of the charge sheet model, it is assumed that the channel never actually pinches off. In other words, the voltage drop between drain and source stays constant at $V_{DS} = V_{GS} - V_T$ no matter how small the gate-drain voltage difference. The situation is often referred to as 'pinch-off' and is defined by the condition that $V_{DS} = V_{DSAT} = V_{GS} - V_T$. Thus, the drain current is approximated by substitution of V_{DS} with $V_{GS} - V_T$ in Eq. 2.10, leading to

$$I_D \cong \frac{W\mu_{EFF}C_{OX}}{L}\left\{[V_{GS} - V_T][V_{GS} - V_T] - \frac{1}{2}[V_{GS} - V_T]^2\right\}$$

$$= \frac{W\mu_{EFF}C_{OX}}{2L}[V_{GS} - V_T]^2. \tag{2.11}$$

This expression represents the long-channel MOSFET model in the saturation regime.

In reality, when the gate voltage is less than the threshold voltage, a small amount of drain current may flow. This occurs because of electron injection into the

weakly inverted channel. This type of injection-limited, subthreshold current is modeled as diffusion currents. Starting from the drift-diffusion model which is used in the previous derivation,

$$J_N(x,y) = -q\mu_N(x,y)n(x,y)\xi_y(x,y) + qD_N(x,y)\frac{\partial}{\partial y}n(x,y) \quad , \tag{2.2}$$

Since conduction is assumed to be dominated by diffusion,

$$J_N(x,y) \cong qD_N(x,y)\frac{\partial}{\partial y}n(x,y). \tag{2.12}$$

Assuming that the diffusion coefficient is independent of the direction and integrating Eq. 2.12 over the cross section of the channel,

$$I_D \cong WD_N \frac{\partial}{\partial y}\int_0^{t_{CH}} qn(x,y)dx,$$

$$\cong WD_N \frac{\partial}{\partial y}\int_0^{\infty} q\left[n(x,y) - N_B\right]dx. \tag{2.13}$$

Integrating both sides along the channel,

$$\int_0^L I_D dy = \int_0^L WD_N \frac{\partial}{\partial y}Q_N(y)dy$$

$$\Leftrightarrow LI_D = WD_N\left[Q_N(y=L) - Q_N(y=0)\right], \tag{2.14}$$

where $Q_N(y=L)$ and $Q_N(y=0)$ are, respectively, the total charge density at the drain and at the source, which are equal to

$$Q_N(y=0) \approx Q_{N0}\exp\left\{\frac{q}{k_BT}\left[V_{GS} - V_{FB} - \frac{Q_{SC}}{C_{OX}}\right]\right\} \text{ and} \tag{2.15}$$

Operating regime and range	Drain current expression	Conduction mechanism
Subthreshold $V_{FB}+\frac{Q_{SC}}{C_{OX}}<V_{GS}<V_T$	$I_D=\frac{W}{L}D_N Q_{N0}\exp\left\{\frac{q}{k_BT}\left[V_{GS}-V_{FB}-\frac{Q_{SC}}{C_{OX}}\right]\right\}\left\{1-\exp\left[-\frac{qV_{DS}}{k_BT}\right]\right\}$	Diffusion
Pre-saturation $V_{GS}>V_T$ $V_{DS}<V_{GS}-V_T$	$I_D\cong\frac{W\mu_{EFF}C_{OX}}{L}\left\{[V_{GS}-V_T]V_{DS}-\frac{1}{2}{V_{DS}}^2\right\}$	Drift
Post-saturation $V_{GS}>V_T$ $V_{DS}>V_{GS}-V_T$	$I_D\cong\frac{W\mu_{EFF}C_{OX}}{2L}[V_{GS}-V_T]^2$	Drift

Table 2.1: Summary of drain current operation for a long-channel MOSFET.

$$Q_N(y=L)\approx Q_{N0}\exp\left\{\frac{q}{k_BT}\left[V_{GD}-V_{FB}-\frac{Q_{SC}}{C_{OX}}\right]\right\}, \tag{2.16}$$

where Q_{N0} is a constant, V_{FB} is the flat-band voltage, Q_{SC} is the charge density of the space charge region which consists of both depletion and inversion charges, and C_{OX} is the insulator capacitance density [10]. Substituting Eqs. 2.15 and 2.16 into Eq. 2.14,

$$LI_D=WD_N\left[Q_{N0}\exp\left\{\frac{q}{k_BT}\left[V_{GD}-V_{FB}-\frac{Q_{SC}}{C_{OX}}\right]\right\}-Q_{N0}\exp\left\{\frac{q}{k_BT}\left[V_{GS}-V_{FB}-\frac{Q_{SC}}{C_{OX}}\right]\right\}\right]$$

$$\Leftrightarrow I_D=\frac{W}{L}D_N Q_{N0}\exp\left\{\frac{q}{k_BT}\left[V_{GS}-V_{FB}-\frac{Q_{SC}}{C_{OX}}\right]\right\}\left\{1-\exp\left[-\frac{qV_{DS}}{k_BT}\right]\right\}. \tag{2.17}$$

This expression describes subthreshold drain current for a long-channel MOSFET under the condition of $V_{FB}+\frac{Q_{SC}}{C_{OX}}<V_{GS}<V_T$. The most important aspect of Eq. 2.17 is that subthreshold current depends exponentially on V_{GS}.

Table 2.1 is a summary of drain-current operation for a long-channel MOSFET. Three regimes of operation – subthreshold, pre-saturation, and post-saturation – are distinguished by the threshold voltage, V_T, and the pinch-off voltage, $V_{DSAT} = V_{GS} - V_T$. Note also that subthreshold is dominated by diffusion current, whereas pre-saturation and post-saturation involve drift current.

2.2.2 Differences Between Inversion- and Accumulation–mode Models

The operation and modeling of MOSFETs and TFTs are quite similar in many respects. However, MOSFETs are inversion-mode while TFTs are accumulation-mode devices. Two fundamental MOSFET parameters – threshold voltage and mobility – are considered in this section from a MOSFET perspective. Then, their applicability, or lack thereof, with regard to TFTs is discussed.

First, consider threshold voltage in a silicon MOSFET with a SiO_2 gate dielectric. The most common definition of threshold voltage for a MOSFET, V_T, is that it is the gate voltage at which the surface potential, ψ_s, reaches twice the bulk potential, $2\psi_B$. A more complete prescription for the threshold voltage also includes a flatband correction which accounts for charge in the insulator and at the insulator/semiconductor interface and also the depletion charge in the semiconductor space charge region. Then, assuming that the substrate is n-type and uniformly doped, the threshold voltage may be expressed as

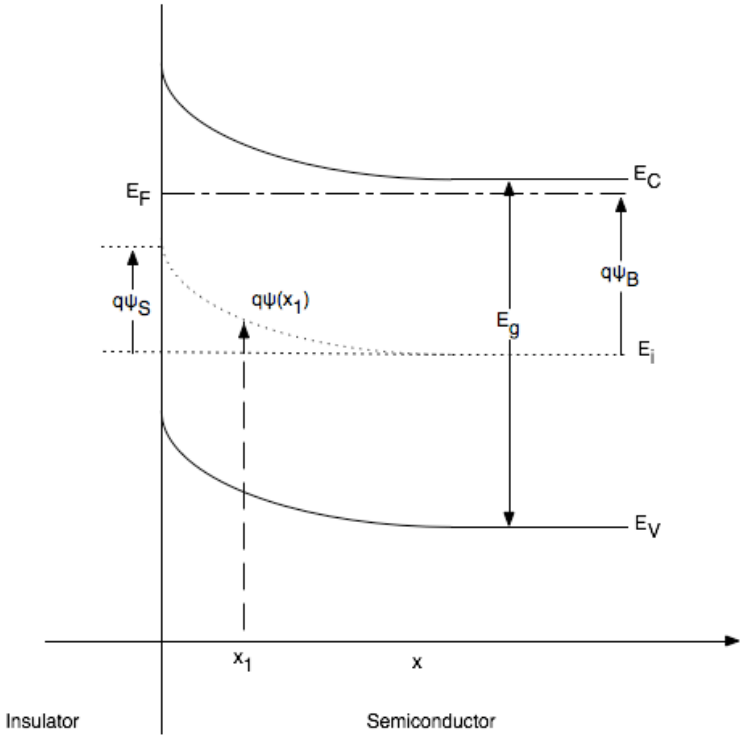


Figure 2.3: Energy band diagram and definition of parameters for an n-type semiconductor. Notice that both the surface potential, ψ_S, and bulk potential, ψ_B, possess signs defining their polarity. In this case, the sign of both ψ_S and ψ_B are negative.

$$V_T = V_{FB} + 2\psi_B + \frac{Q_{SC}}{C_{OX}}, \tag{2.18}$$

where V_{FB} is the flat-band voltage, Q_{SC} is the charge density of the space charge region, and C_{OX} is the insulator capacitance density. Q_{SC} is expressed as $Q_{SC} = \sqrt{2\varepsilon_{Si} q N_D \psi_B}$, where N_D is the donor dopant concentration of n-type substrate and ε_{Si} is the permittivity of silicon. The physics underlying this definition of the threshold voltage is established in the following discussion [16].

The charge induced at the SiO_2/Si interface is assessed using Possion's equation,

$$\frac{d^2\psi}{dx^2} = -\frac{d\xi}{dx} = -\frac{q}{\varepsilon_{si}}\left(p(x) - n(x) + N_D^+ - N_A^-\right), \tag{2.19}$$

where ψ is the potential, ξ is the electric field which is equal to $-\frac{d\psi}{dx}$, $p(x)$ is hole concentration, $n(x)$ is electron concentration, N_D^+ is the ionized donor density concentration, and N_A^- is the ionized acceptor concentration.

Assuming that the silicon bulk is lightly doped so that the Fermi distribution function can be approximated by the Boltzmann distribution and using the charge neutrality relation, expressions for the MOS capacitor of an n-type substrate are as follows,

$$n(x) = N_D \exp\left(\frac{q\psi}{k_B T}\right), \tag{2.20}$$

$$p(x) = \frac{n_i^2}{N_D} \exp\left(-\frac{q\psi}{k_B T}\right), \tag{2.21}$$

$$N_D^+(x) - N_A^-(x) = N_D - \frac{n_i^2}{N_D}. \tag{2.22}$$

Substituting in Eqs. 2.20, 2.21, and 2.22 into Eq. 2.19 leads to

$$\frac{d^2\psi}{dx^2} = -\frac{d\xi}{dx} = -\frac{q}{\varepsilon_{si}}\left(\frac{n_i^2}{N_D}\left(\exp\left(-\frac{q\psi}{k_B T}\right) - 1\right) - N_D\left(\exp\left(\frac{q\psi}{k_B T}\right) - 1\right)\right). \tag{2.23}$$

Eq. 2.23 can be solved for the electric field, multiplying both sides by $\frac{d\psi}{dx}(=\xi)$ and integrating in terms of the potential, ψ, from the bulk potential level, which is $\psi(\infty) = 0$, to the surface potential, $\psi(0) = \psi_S$. From Gauss's law, the total charge induced in the silicon channel, Q_S, is obtained as follows:

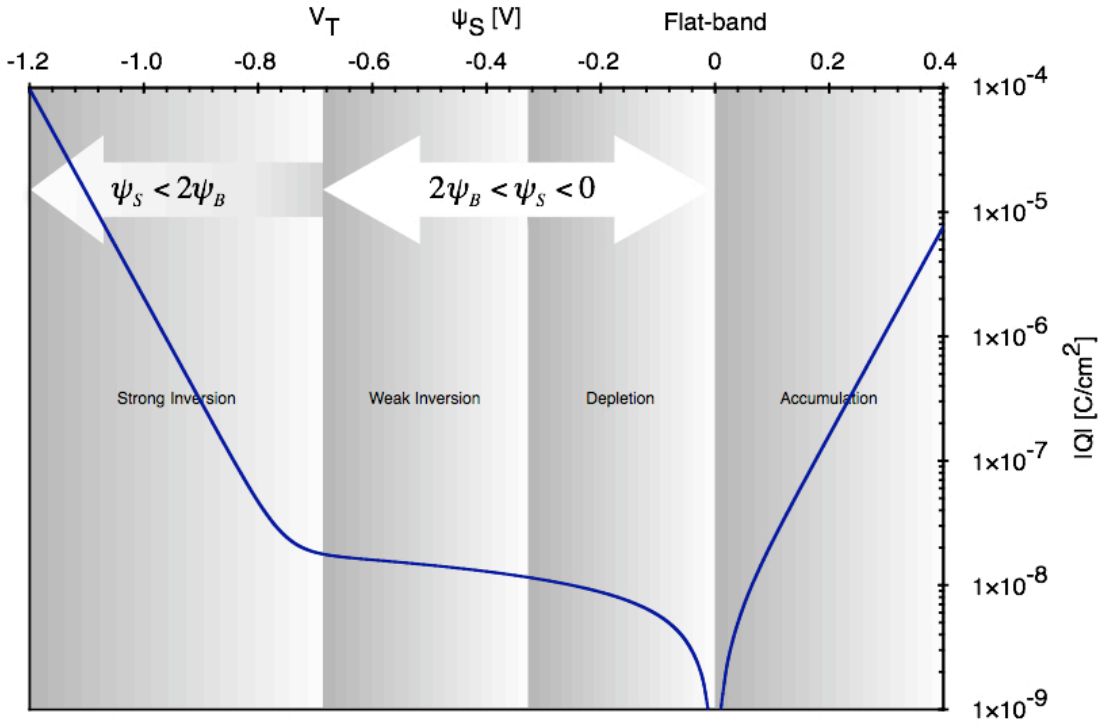


Figure 2.4: The surface potential and the total charge inside the channel of a MOS capacitor and an n-type substrate and a dopant density of 4×10^{15} cm^{-3}. Note that there is no weak accumulation regime, which implies that the MOSFET threshold voltage definition is not appropriate for TFT operation.

$$Q_S = -\varepsilon_{Si}\xi_S = \pm\sqrt{2\varepsilon_{Si}k_BTN_D\left[\left(\frac{n_i}{N_D}\right)^2\left(\exp\left(-\frac{q\psi_S}{k_BT}\right)+\frac{q\psi_S}{k_BT}-1\right)+\left(\exp\left(\frac{q\psi_S}{k_BT}\right)-\frac{q\psi_S}{k_BT}-1\right)\right]}. \tag{2.24}$$

A numerical calculation of Eq. 2.24 for a MOS capacitor with an n-type substrate is plotted in Fig. 2.4. Each regime of operation indicated in Fig. 2.4 – accumulation, depletion, weak inversion, and strong inversion – is dominated by different terms within the square bracket of Eq. 2.24: 1) When $\psi_S > 0$, the exponential term in the second parenthesis, $\exp\left(\frac{q\psi_S}{k_BT}\right)$, dominates. This defines the accumulation regime. 2) When $\psi_B < \psi_S < 0$, the $\frac{q\psi_S}{k_BT}$ term in the second bracket dominates. This

operational region is labeled depletion regime. 3) When $2\psi_B < \psi_S < \psi_B$, the exponential term in the first parenthesis, $\sim\left(\frac{n_i}{N_D}\right)^2 \exp\left(-\frac{q\psi_S}{k_B T}\right)$, becomes appreciable compared to $-\frac{q\psi_S}{k_B T} - 1$ in the second parenthesis, so that the total charge in the channel is established by $\left(\frac{n_i}{N_D}\right)^2 \exp\left(-\frac{q\psi_S}{k_B T}\right) - \frac{q\psi_S}{k_B T} - 1$. This regime of operation is denoted weak inversion. 4) When $2\psi_B > \psi_S$, $\left(\frac{n_i}{N_D}\right)^2 \exp\left(-\frac{q\psi_S}{k_B T}\right)$ dominates and strong inversion occurs.

From this analysis, the boundary between strong and weak inversion can be established in terms of the surface potential as [16]

$$\left(\frac{n_i}{N_D}\right)^2 \exp\left(-\frac{q\psi_S}{k_B T}\right) \sim 1, \tag{2.25}$$

$$\Leftrightarrow \psi_S \sim 2\frac{k_B T}{q} \ln\left(\frac{N_D}{n_i}\right) = 2\psi_B, \tag{2.26}$$

This is the fundamental reason why twice the bulk potential is chosen as a definition of the MOSFET threshold voltage.

Now notice that it is also clear from Fig. 2.4 that accumulation begins abruptly at flat-band. This abrupt onset of carrier accumulation just beyond flat-band is distinctly different from the $2\psi_B$ potential required for a MOSFET as, in this case, the interface transitions between depletion towards inversion. This difference between the onset of inversion and accumulation requires an assessment of the applicability of the

threshold voltage in the context of TFT. This leads to a physics-based reformulation of the threshold voltage for a TFT, as presented in Section 2.2.3.

A second MOSFET parameter which requires some reassessment when used in the context of a TFT is the mobility.

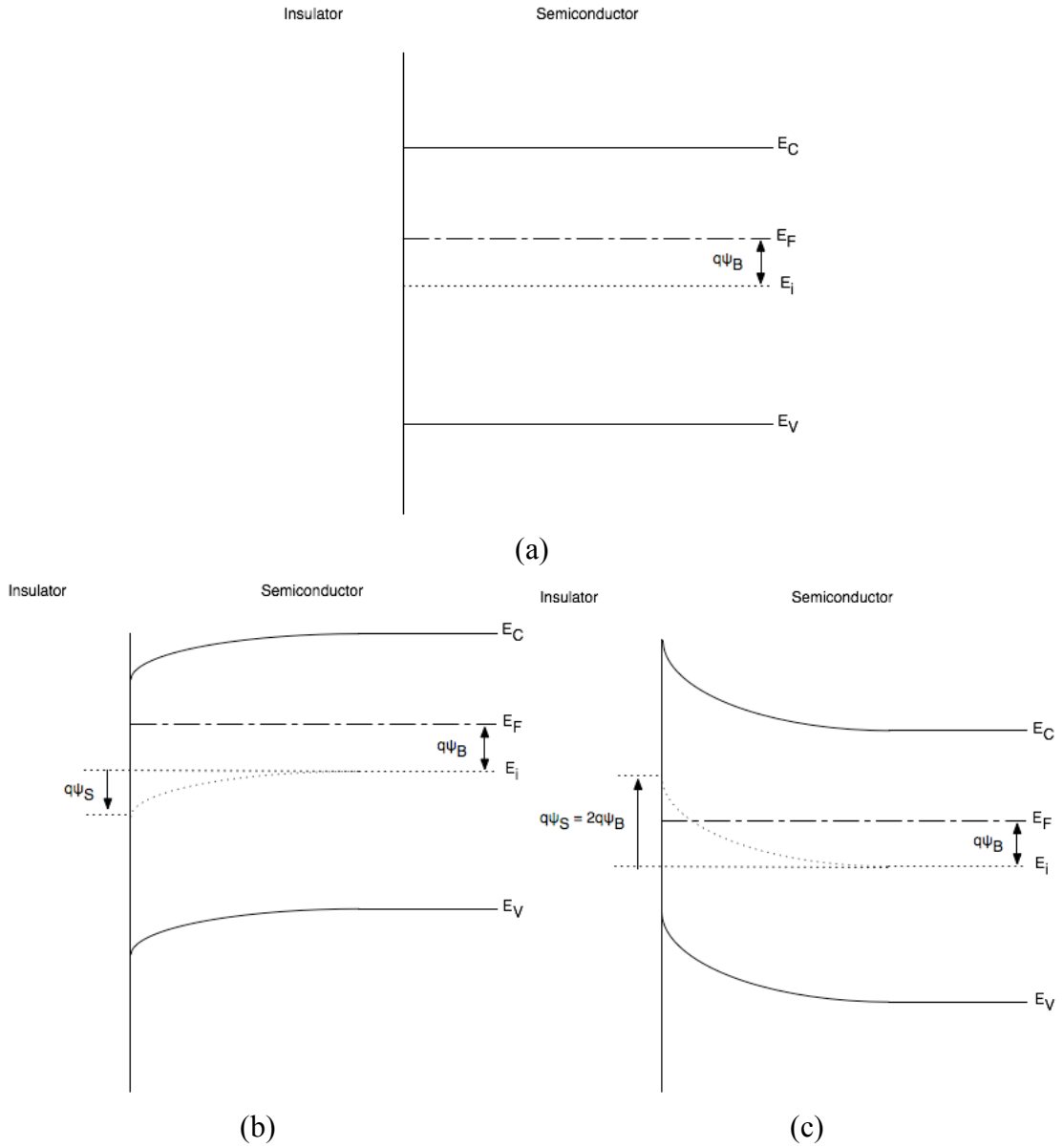


Figure 2.5: Energy band diagrams for an n-type semiconductor representing (a) flat-band, (b) accumulation, and (c) inversion. Notice that the surface potential does not have to be greater than twice the bulk potential in order to reach accumulation.

The effective mobility represents the induced carrier mobility averaged over all the induced mobile carriers in the inversion layer. Mathematically, μ_{EFF} is the constant that makes the following two equations equal;

$$I_D \cong -W\int_0^{t_{CH}} \mu_N(x,y)qn(x,y)\xi_y(x,y)dx \text{ and} \tag{2.4}$$

$$I_D \cong -W\mu_{EFF}\int_0^{t_{CH}} qn(x,y)\xi_y(x,y)dx. \tag{2.5}$$

In a simplified expression,

$$\mu_{EFF} = \frac{\int_0^{t_{CH}} q\mu_N(x,y)n(x,y)dx}{\int_0^{t_{CH}} qn(x,y)dx}. \tag{2.27}$$

Notice that the numerator of this expression represents the sheet conductance and the denominator corresponds to the total induced charge density. Therefore, the effective mobility is a ratio between the channel sheet conductance and the induced channel charge density. However, this expression does not provide a useful value of μ_{EFF} since its direct assessment is difficult. A more practical expression for μ_{EFF} can be derived from Eq. 2.10,

$$I_D = \frac{W\mu_{EFF}C_{OX}}{L}\left\{[V_{GS}-V_T]V_{DS} - \frac{1}{2}{V_{DS}}^2\right\}. \tag{2.10}$$

Dividing both sides of Eq. 2.10 by V_{DS} and assuming the drain current to be linear near $V_{DS} = 0$, which involves taking the limit with $V_{DS} \rightarrow 0$, leads to

$$\lim_{V_{DS}\to 0}\frac{I_D}{V_{DS}} = \lim_{V_{DS}\to 0}\frac{W\mu_{EFF}C_{OX}}{L}\left\{[V_{GS}-V_T] - \frac{1}{2}V_{DS}\right\}$$

$$\Leftrightarrow G_{CH} = \frac{W\mu_{EFF}C_{OX}}{L}[V_{GS}-V_T]\Big|_{V_{DS}\to 0} \tag{2.28}$$

where G_{CH} is defined as the channel conductance. Therefore, solving for the mobility gives

$$\mu_{EFF}(V_{GS}) = \left. \frac{G_{CH}(V_{GS})}{\frac{W}{L} C_{OX}[V_{GS} - V_T]} \right|_{V_{DS} \to 0} . \tag{2.29}$$

In this form, the effective mobility, μ_{EFF}, is easily measured. Note that the effective mobility explicitly depends on the gate-source voltage.

A second type of mobility which is often used in device characterization is the field-effect mobility, μ_{FE}. μ_{FE} was originally defined by Bardeen *et al.* to measure the effect of the surface potential on the mobility of induced carriers at the oxide/semiconductor interface of a germanium-based MOS capacitor [17]. Mathematically,

$$\mu_{FE} = \frac{d\sigma_{SQ}}{dQ}, \tag{2.30}$$

where σ_{SQ} is the channel sheet conductance and Q is the total charge density induced in the gate material, which is positive. Replacing the sheet conductance and the total charge density by equivalent integral expressions and using the chain rule, Eq. 2.30 can be reformulated as follows,

$$\mu_{FE} = \frac{\frac{\partial}{\partial V_{GS}} \int_0^{t_{CH}} q\mu_N n(x,y) dx}{\frac{\partial}{\partial V_{GS}} \int_0^{t_{CH}} qn(x,y) dx} . \tag{2.31}$$

Equation 2.31 for μ_{FE} is the counterpart expression to Eq. 2.27 for μ_{EFF}. Thus, Eq. 2.31 reveals that μ_{FE} is the ratio between the incremental channel sheet conductance

and the incremental induced channel sheet charge density. Comparing Eq. 2.27 to Eq. 2.29, leads to identification of

$$\int_0^{t_{CH}} q\mu_N n(x,y)dx \approx \frac{G_{CH}(V_{GS})}{\frac{W}{L}} = \sigma_{SQ}, \tag{2.32}$$

and also of

$$\int_0^{t_{CH}} qn(x,y)dx \approx C_{OX}\left[V_{GS} - V_T\right]. \tag{2.33}$$

Using Eqs. 2.32 and 2.33 in Eq. 2.31 allows the field-effect mobility to be re-expressed as,

$$\mu_{FE}(V_{GS}) \cong \left.\frac{\frac{\partial G_{CH}(V_{GS})}{\partial V_{GS}}}{\frac{W}{L}C_{OX}}\right|_{V_{DS}\to 0}. \tag{2.34}$$

This expression is the one developed by Hoffman [18], as discussed further in Section 2.2.3, and is slightly different from the one normally used,

$$\mu_{FE} \cong \left.\frac{g_m}{\frac{W}{L}C_{OX}V_{DS}}\right|_{V_{DS}\to 0}. \tag{2.35}$$

Note that since $g_m = \frac{\partial I_D}{\partial V_{GS}}$, Eqs. 2.34 and 2.35 imply that $\frac{\partial G_{CH}(V_{GS})}{\partial V_{GS}} \approx \frac{g_m}{V_{DS}}$.

A point of divergence between MOSFETs and TFTs with respect to this development involves the induced charge approximation used in Eq. 2.7,

$$\int_0^{t_{CH}} qn(x,y)dx \cong \int_0^{\infty} q\left[n(x,y) - N_B\right]dx = C_{OX}\left[V_{GS} - V_T - V(y)\right]. \tag{2.7}$$

Use of the threshold voltage, V_T, in Eq. 2.7 is based on the fact that an appreciable concentration of inversion electrons is induced only after V_{GS} exceeds V_T, which, from Fig. 2.4, means that the MOSFET is in strong inversion. However, as explained previously, for TFTs, there is no corresponding situation of weak and strong accumulation. Thus, some refinement of the induced carrier expression is required in order to modify MOSFET expressions so that they are appropriate for TFTs.

2.2.3 Accumulation-mode Device Operation – The Hoffman Model

In the physics-based treatment of accumulation-mode TFTs, Hoffman starts from the same assumptions as those for MOSFET models: 1) the GCA, 2) the charge-sheet model, and 3) the depletion approximation. The only difference is an additional assumption; there is no subthreshold current, i.e. drift is assumed to be the only TFT current mechanism. This assumption is appropriate since the charge accumulation starts immediately after the surface potential exceeds flatband, as shown in Fig. 2.4.

To develop TFT models based on these assumptions, he introduced three new device physics parameters: average mobility, μ_{AVG}, incremental mobility, μ_{INC}, and turn-on voltage, V_{ON} [19].

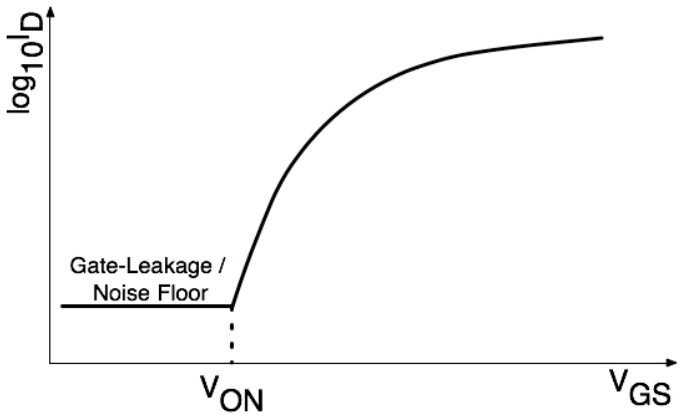


Figure 2.6: Location of the turn-on voltage, V_{ON}, as assessed from a $\log_{10}(I_D)$-V_{GS} transfer curve.

Turn-on voltage, V_{ON}, for an accumulation-mode TFT is analogous to threshold voltage, V_T, for an inversion-mode MOSFET, but physically correlates to a flatband voltage condition. As discussed previously in Section 2.2.2, V_T corresponds physically to the onset of an appreciable density of inversion carriers as distinguished with respect to a background depletion charge density. In contrast, V_{ON} corresponds to an onset of charge accumulation whose identification is not obscured by the presence of a depletion charge background since this accumulation charge onset corresponds to flatband, where there is a negligible background charge density. Operationally, V_{ON} is estimated as the gate voltage corresponding to the onset of drain current on a $\log_{10}(I_D)$-V_{GS} transfer curve, as shown in Fig. 2.6.

Derivation of Hoffman's model follows almost the same approach as that used for MOSFETs, except for the following differences. The major difference involves the expression for the total charge of induced carriers, Eq. 2.7,

$$\int_0^{t_{CH}} qn(x,y)dx \cong \int_0^{\infty} q\left[n(x,y) - N_B\right]dx = C_{OX}\left[V_{GS} - V_T - V(y)\right]. \tag{2.7}$$

Since, as explained previously, carriers begin to be induced immediately after the gate voltage surpasses the flat-band voltage, Eq. 2.7 is modified to

$$\int_0^{t_{CH}} qn(x,y)dx \cong \int_0^{\infty} q\left[n(x,y) - N_B\right]dx = C_{OX}\left[V_{GS} - V_{ON} - V(y)\right]. \tag{2.36}$$

Notice that the essential difference between Eq. 2.7 and Eq. 2.36 is that V_{ON} replaces V_T. Another trivial difference is that t_{CH} now refers to the thickness of the accumulation layer rather than the inversion layer. Therefore, the only important difference between the final MOSFET and TFT drain current equations is that V_{ON} replaces V_T.

Inserting Eq. 2.36 into Eq. 2.6, and integrating along the channel in a manner directly analogous to Eq. 2.9 results in

$$I_D = \frac{W\mu_{AVG}C_{OX}}{L}\left\{\left[V_{GS} - V_{ON}\right]V_{DS} - \frac{1}{2}V_{DS}^{\ 2}\right\}:$$

pre-saturation region ($V_{DS} < V_{GS} - V_{ON}$) and (2.37)

$$I_D = \frac{W\mu_{AVG}C_{OX}}{2L}\left[V_{GS} - V_{ON}\right]^2:$$

post-saturation region ($V_{DS} > V_{GS} - V_{ON}$). (2.38)

Note in Eqs. 2.39 and 2.40 that the average mobility, μ_{AVG}, replaces the effective mobility, μ_{EFF}, in Hoffman's formulations.

All of the drain current expressions in the different operating regimes are summarized in Table 2.2. Notice that no explicit TFT subthreshold current counterpart to that of a MOSFET is given in Table 2.2. Rather, in Hoffman's model the function $\mu_{AVG}(V_{GS})$ accounts for what is normally defined at subthreshold current.

The fundamental definition of the average mobility for a TFT is identical to that of the effective mobility of a MOSFET,

$$\mu_{AVG}(V_{GS}) = \frac{\int_0^{t_{CH}} q\mu_N(x,y)n(x,y)dx}{\int_0^{t_{CH}} qn(x,y)dx}, \tag{2.39}$$

where t_{CH} now represents the accumulation layer thickness. As discussed in Subsection 2.2.1, μ_{AVG} corresponds to the ratio between the sheet conductance of the channel and the total induced channel charge density. A more empirical expression for μ_{AVG} is derived in the same manner as μ_{EFF},

$$\mu_{AVG}(V_{GS}) = \left.\frac{G_{CH}(V_{GS})}{\frac{W}{L}C_{INS}[V_{GS}-V_{ON}]}\right|_{V_{DS}\to 0}, \tag{2.40}$$

Operating regime and range	**Drain current expression**	**Conduction mechanism**
Subthreshold (Not defined)	-	-
Pre-saturation $V_{GS} > V_{ON}$ $V_{DS} > V_{GS} - V_{ON}$	$I_D = \mu_{AVG}(V_{GS})C_{INS}\frac{W}{L}\{[V_{GS}-V_{ON}]V_{DS} - \frac{1}{2}V_{DS}^2\}$	Drift
Post-saturation $V_{GS} > V_{ON}$ $V_{DS} < V_{GS} - V_{ON}$	$I_D = \frac{1}{2}\mu_{AVG}(V_{GS})C_{INS}\frac{W}{L}[V_{GS}-V_{ON}]^2$	Drift

Table 2.2: A summary of operating regimes and ranges, conduction current expressions, and assumed conduction mechanisms, according to Hoffman's model. This table serves as a comparison between TFTs and MOSFETs, as summarized in Table 2.1.

where $G_{CH} = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{DS}=0} \approx \left.\frac{I_D}{V_{DS}}\right|_{V_{DS}\to 0}$. According to Hoffman's development, the counterpart of the field-effect mobility, μ_{FE}, is the incremental mobility, μ_{INC}, whose fundamental definition is identical to that of μ_{FE},

$$\mu_{INC}(V_{GS}) \cong \frac{\frac{\partial}{\partial V_{GS}}\int_0^{t_{CH}} q\mu_N n(x,y)dx}{\frac{\partial}{\partial V_{GS}}\int_0^{t_{CH}} qn(x,y)dx}. \tag{2.41}$$

The numerator of Eq. 2.41 represents a derivative with respect to V_{GS} of the channel sheet conductance and the denominator is equal to a derivative with respect to V_{GS} of the total channel sheet charge density. In a same manner as μ_{FE}, a practical expression for μ_{INC} is derived as

$$\mu_{INC}(V_{GS}) = \left.\frac{\frac{\partial G_{CH}(V_{GS})}{\partial V_{GS}}}{\frac{W}{L}C_{INS}}\right|_{V_{DS}\to 0} \approx \left.\frac{\frac{\Delta G_{CH}(V_{GS})}{\Delta V_{GS}}}{\frac{W}{L}C_{INS}}\right|_{V_{DS}\to 0}. \tag{2.42}$$

μ_{AVG} represents the average mobility of all of the carriers induced into the channel, including both mobile and trapped carriers. In contrast, μ_{INC} corresponds to the mobility of carriers induced incrementally into the channel as the gate voltage incrementally increases.

A comparison between these Hoffman's mobilities and commonly used formulations employed for MOSFETs is presented in Table 2.3. The only noticeable difference between μ_{AVG} and μ_{EFF} is the replacement of V_T with V_{ON}. The TFT threshold voltage may be estimated empirically by linearly extrapolating a $I_D^{1/2}$ vs.

V_{GS} plot to the V_{GS} intercept (for a device operating in saturation), as shown in Fig. 2.7 [20].

A significant limitation of μ_{EFF} compared to μ_{AVG} is evident from an assessment of Fig. 2.8. As evident from this figure, μ_{EFF} is only defined for $V_{GS} > V_T$. In fact, since a singularity exists at $V_{GS} = V_T$, it is not possible to accurately evaluate μ_{EFF} until V_{GS} is appreciably larger than V_T, in order to avoid mathematical problems associated with this singularity at $V_{GS} = V_T$. In contrast, μ_{AVG} is unambiguously defined over the relevant range of V_{GS}, i.e., $V_{GS} > V_{ON}$.

In summary, the accumulation-mode TFT model differs from the conventional MOSFET model primarily in the replacement of V_T with V_{ON} and μ_{EFF} with μ_{AVG}. A consequence of replacing V_T with V_{ON} is that TFT subthreshold current is implicitly taken into account by $\mu_{AVG}(V_{GS})$ over the range of $V_{ON} \leq V_{GS} \leq V_T$, rather than explicitly given by an expression such as Eq. 2.17 for a MOSFET. This equation is applicable to injection-limited transport, whereas recent research suggests that subthreshold current in AOS-based TFTs of primally interest to this thesis research operate under bulk-limited transport conditions within the framework of space-charge-limited current [21].

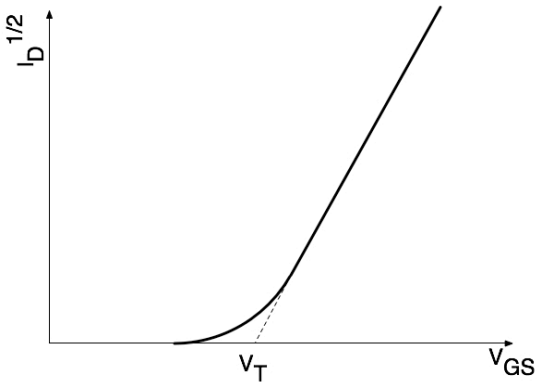


Figure 2.7: A plot of $I_D^{1/2}$ – V_{GS} for a TFT operating in saturaion. Threshold voltage V_T is estimated by extrapolating the linear part of the curve to the V_{GS} axis.

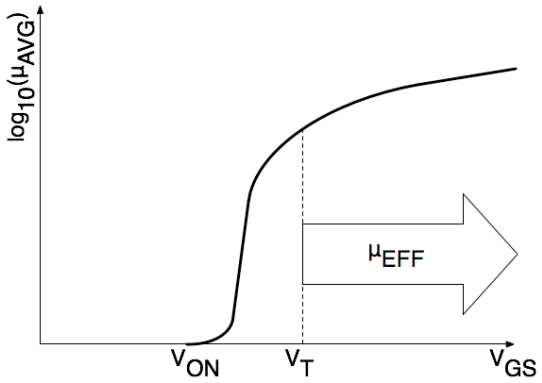


Figure 2.8: A plot of $\log_{10}(\mu_{AVG})$ versus V_{GS}, illustrating that μ_{AVG} is defined over the relevant range of V_{GS}, i.e., $V_{GS} > V_{ON}$ whereas μ_{EFF} is defined only for $V_{GS} > V_T$.

Conventional mobility		**Mobility defined by Hoffman**	
Name	Definition	Name	Definition
Field effect Mobility	$\mu_{FE}(V_{GS}) = \left.\frac{g_m(V_{GS})}{\frac{W}{L}C_{INS}V_{DS}}\right\|_{V_{DS}\to 0}$	Incrementa l Mobility	$\mu_{INC}(V_{GS}) = \left.\frac{\frac{\partial G_{CH}(V_{GS})}{\partial V_{GS}}}{\frac{W}{L}C_{INS}}\right\|_{V_{DS}\to 0}$
Effective Mobility	$\mu_{EFF}(V_{GS}) = \left.\frac{G_{CH}(V_{GS})}{\frac{W}{L}C_{INS}[V_{GS}-V_T]}\right\|_{V_{DS}\to 0}$	Average Mobility	$\mu_{AVG}(V_{GS}) = \left.\frac{G_{CH}(V_{GS})}{\frac{W}{L}C_{INS}[V_{GS}-V_{ON}]}\right\|_{V_{DS}\to 0}$

Table 2.3: A comparison of conventional mobilities and mobilities defined by Hoffman [79].

2.3 Transparent Thin-Film Transistor Channel Materials

As explained briefly in the introduction, oxide semiconductors with novel metal cations were reported by Kawazoe *et al.* in 1996 [4]. This class of oxides will be subsequently referred to in this thesis as amorphous oxide semiconductors (AOSs).

There are several potential channel material candidates for transparent thin-film transistor applications which have been reported up to now, including polycrystalline zinc oxide [22][23], amorphous zinc indium oxide (ZIO) [24], amorphous zinc tin oxide (ZTO) [25], and amorphous indium gallium zinc oxide (IGZO) [26][27][28]. Several other amorphous oxide materials are included in Table 2.4. AOSs possess certain structural and electrical properties not found in a-Si:H, such as a structure-independent mobility and a normal Hall coefficient sign. Because the research presented in this thesis focuses on IGZO-based TFTs, a detailed discussion of these characteristics is provided in the following subsections, based exclusively on IGZO.

2.3.1 Structure Independence of the Mobility

The first commercially produced amorphous semiconductor was hydrogenated amorphous silicon (a-Si:H), as mentioned in the introduction. One primary problem associated with a-Si:H is its low mobility (~1 cm^2/V-s).

In 1996, Kawazoe *et al.* at the Tokyo Institute of Technology proposed a procedure for realizing high-mobility amorphous oxide semiconductors (AOS) [4]. A rough sketch of the reason why this class of materials maintains a relatively high mobility even with an amorphous microstructure is provided below.

Material	Mobility [$cm^2V^{-1}s^{-1}$]	Band gap [eV]	Reference
In_2O_3	36	~3.3	[29]
CdO-GeO_2	12	~3.1	[30]
In_2O_3-ZnO (IZO)	~50	~3.5	[31]
In_2O_3-GaO_2-ZnO (IGZO)	12-20	2.8-3.0	[32]
a-Si:H (process temp. @ 150°C)	1.1	-	[33]
Organic (pentacene)	1.5	-	[34]

Table 2.4: The approximate mobility and bandgap of several types of amorphous conductive materials.

Electron conductivity is proportional to a product of the mobility and the carrier density,

$$\sigma \propto n\mu, \tag{2.43}$$

where n is the carrier density and μ is the mobility. Therefore, to make the conductivity higher, increasing the carrier density and/or the mobility is required. For TFT channel applications, mobility is of primary concern since a well-designed TFT channel layer has a very low carrier concentration. Thus, mobility will be the focus of the subsequent discussion.

The mobility is inversely proportional to the carrier effective mass, m^*, and directly proportional to the mean time between scattering events, $\langle \tau \rangle$,

$$\mu = \frac{q\langle \tau \rangle}{m^*}, \tag{2.44}$$

where q is the electron charge [35]. This relation indicates that a material with a smaller carrier effective mass has a larger mobility.

The energy band structure of an idealized, one-dimensional lattice in k-space near the Γ point is approximately given by

$$E = H_{nn} + 2H_{mn}\cos(ka) \approx H_{nn} + 2H_{mn} - H_{mn}(ka)^2, \tag{2.45}$$

where a is the lattice constant, and H_{mn} is the Hamiltonian matrix element, which is expressed as $H_{mn} = \int \phi^*(x_m) H \phi(x_m) dx$ and represents the magnitude of the interaction between two orbitals from different atoms, where φ is the electron orbital [36].

Since the effective mass of the electron is described as

$$m^* = \frac{\hbar^2}{\frac{d^2E}{dk^2}}, \tag{2.46}$$

plugging the idealized, one-dimensional model, Eq. 2.45, into Eq. 2.46, leads to

$$m^* \approx -\frac{\hbar^2}{2H_{mn}a^2}. \tag{2.47}$$

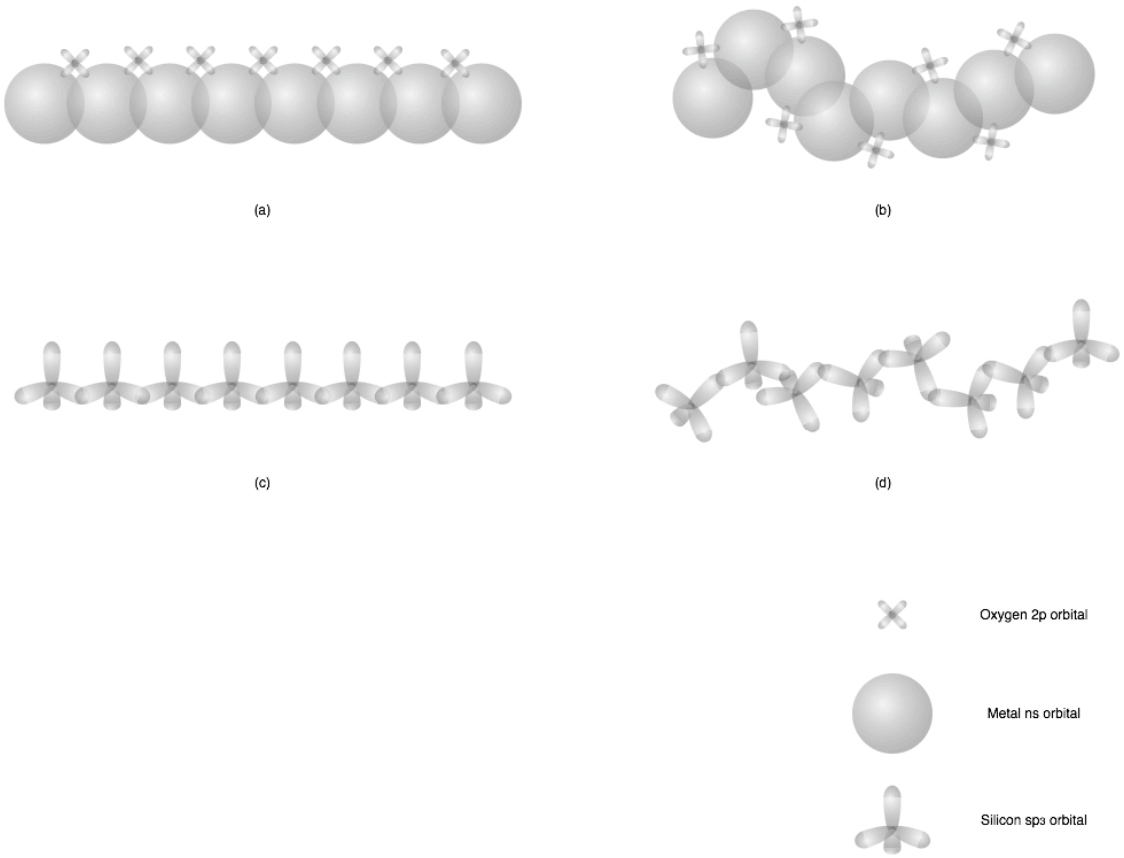


Figure 2.9: Atomic bonding configurations: a) crystalline structure of an amorphous oxide semiconductor (AOS) constructed using a multicomponent combination of heavy metal cations, b) crystalline structure of silicon, c) amorphous structure of AOS, and d) amorphous structure of silicon.

Because H_{mn} in the denominator of Eq. 2.47 represents the magnitude of the interaction between two overlapping orbitals of different atoms, Eq. 2.47 indicates that a larger interaction between orbitals results in a smaller effective mass, which, via Eq. 2.44, implies a larger mobility [36].

Because of the highly directional atomic structure of sp^3 orbitals, a large orbital overlap requires an ordered microstructure in a covalent material, so that amorphous covalent materials, such as a-Si:H, are characterized by low mobilities. In contrast, the ionic bonding structure of an AOS with an outer shell electronic configuration of $(n-1)d^{10}ns^0$, where $n \geq 5$, consists of large radii s-orbital cations, which are spherically

symmetric and possess low directionality [37]. Thus, even in an amorphous microstructure, the extent of the electronic overlap of an AOS remains almost unaltered compared to that of a crystalline microstructure, as illustrated in Fig. 2.9 [38].

Additionally, an AOS can be fabricated via a low substrate temperature process, such as sputtering or pulsed-laser deposition (PLD), while the fabrication process temperature used for a-Si:H is at least 250 °C and its electrical properties are degraded as the deposition temperature decreases [39]. Along with the directional insensitivity of the constituent ionic species, this low-temperature process makes it possible for AOSs to employ a low-temperature plastic substrate, such as PET (polyethylene terephthalate), to realize flexible devices, instead of traditional high-temperature substrates, almost all of which are rigid, such as glass. Devices created upon these pliable substrates open the possibility of new applications. One of the most promising applications of this class is electronic or e-paper [40], which has the potential of replacing traditional paper. Although several organic materials, such as pentacene, thiophene oligomers, and regioregular polythiophene, have been explored as TFT channel layer candidates, they all suffer from having a low mobility [41].

2.3.2 Percolation Conduction Model

Another characteristic of this AOS material class is that the sign of the Hall coefficient matches that of Seebeck coefficient [42], while the Hall coefficient of almost all other amorphous semiconductors exhibits a different sign from that of its Seebeck coefficient, presumably because of the short length of the carrier mean free path, which invalidates assumptions made in the solution of the Boltzmann transport

equation [43]. a-Si:H is an extreme case, since its Hall coefficient changes from negative to positive when the carrier type changes from p-type to n-type [44]. Having a normal sign of the Hall coefficient indicates that the length of the electron mean free path in an AOS is much longer than that observed in n-type a-Si:H and, therefore, hints that the dominant conduction mechanism is not quantum mechanical hopping via a band-tail states, which is sometimes referred to as variable range hopping (VRH). However, the $T^{-1/4}$ temperature dependence of the conductivity in single crystal IGZO for non-degenerate doping appears to be strong evidence for electron transport via VRH [45].

Nomura *et al.* resolve this apparent contradiction by employing a percolation mechanism, which has been studied in mathematical fields such as fractal geometry [46] and is known to yield the same $T^{-1/4}$ temperature dependence of the conductivity [45], for electron transport in IGZO. According to this model, quantum mechanical hopping is excluded as a conduction mechanism because of the relatively long average distance between monoenergetic states (see Fig. 2.10). When the Fermi level is below that of the highest energy barriers, which are associated with the random distribution of Ga^{3+} and Zn^{2+} ions in a single crystal structure $InGaO_3(ZnO)_5$, electron conduction is exclusively dominated by the percolation mechanism, in which electrons trickle through between the valley of potential energy barriers as shown in Fig. 2.11, and the conductivity temperature dependence goes as $T^{-1/4}$, characteristic of disorder. However, once the Fermi level is elevated above these conduction band potential energy peaks, the carrier density is high enough to fill all of the valleys in the tail states and electron transport is dominated by a temperature-independent, degenerate

mechanism. Energy band and density of state pictures for this model are shown in Fig. 2.12 [45]. Takagi *et al.*, also confirm that percolation transport dominates in amorphous IGZO, but that in this case disorder arises from the randomness of the amorphous microstructure in addition to Ga^{3+} and Zn^{2+} cation disorder [47].

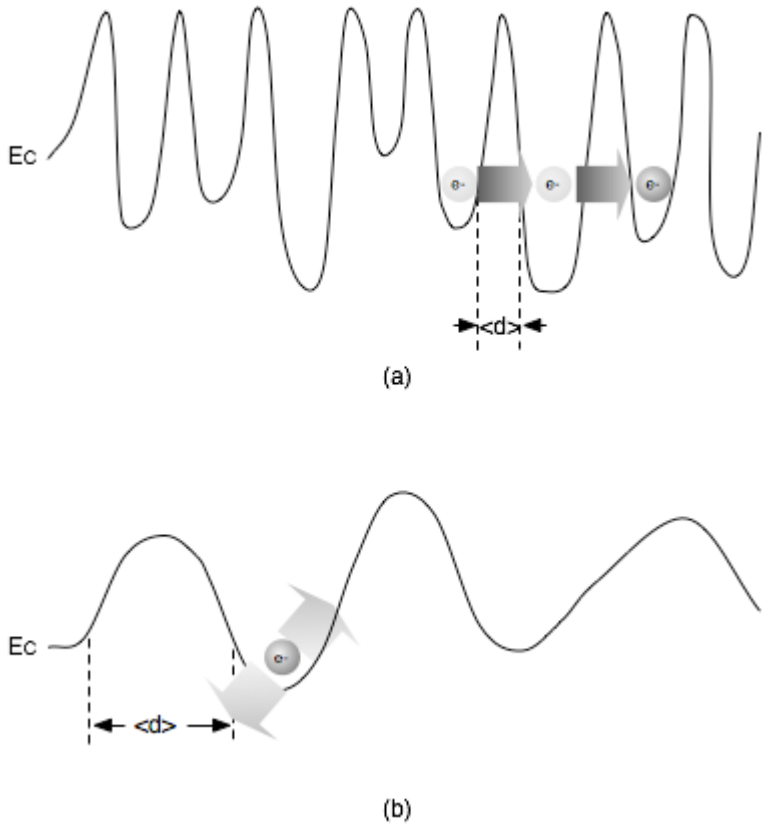
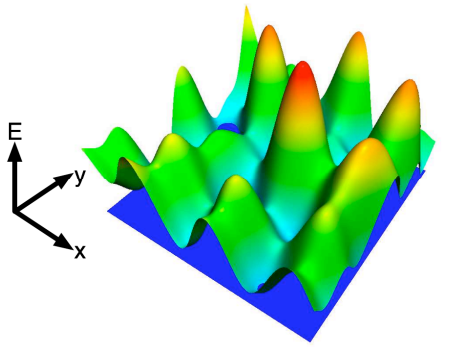
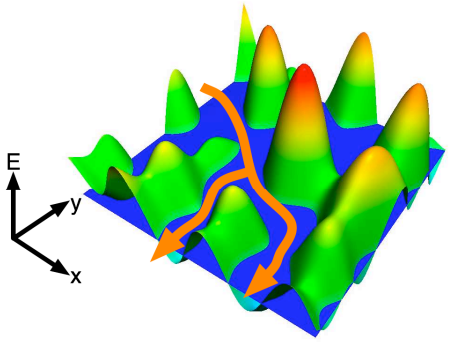


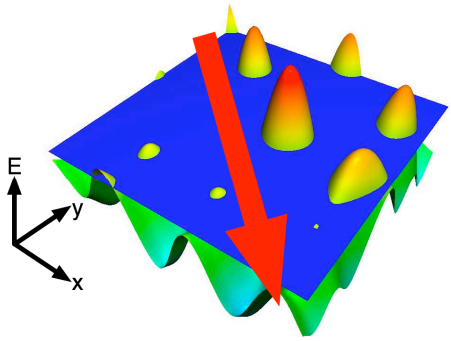
Figure 2.10: Energy-band diagram illustrating both hopping and percolation conduction mechanisms: a) hopping conduction, or variable range hopping (VRH), occurs when the average distance between the closest trapping sites, <d>, is small enough for electrons to quantum mechanically tunnel through the energy potential barrier. However, b) if <d> is large, tunneling does not occur. Rather, electron transport is via percolation, a process in which electrons trickle through valleys defined by potential energy barriers of variable height with a Gaussian distribution, which means that the electron moves in a direction perpendicular to this page as explicitly shown in Figure 2.11.



(a)



(b)



(c)

Figure 2.11: The conduction model suggested by Nomura, *et al.* [37], is shown. The bumpy surface represents the conduction band edge and the flat layer represents the Fermi level. The model is simplified by assuming that the temperature is close to 0 K. (a) When the Fermi level is low, there are not enough electrons induced above the conduction band edge. (b) As the Fermi level increases, connections between small pools of electrons are formed so that electrons trickle through potential valleys (percolation conduction). (c) When the Fermi level is high enough, almost all potential barriers are immersed under the Fermi level so that electrons move almost unhindered (degenerate conduction).

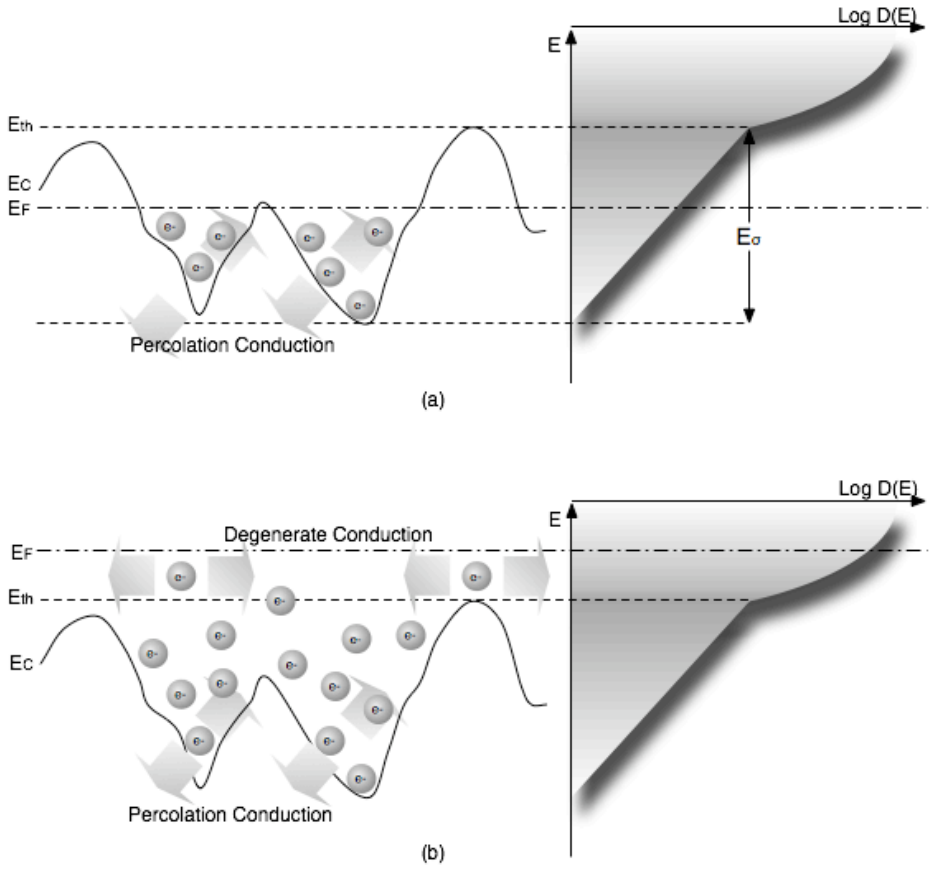


Figure 2.12: Energy-band picture of the electron conduction mechanism in single crystal IGZO as proposed by Nomura, *et al.* [45] Conduction band potential barriers and associated band-tail states arise as a consequence of a random distribution of Ga^{+3} and Zn^{+2} ions in crystalline $InGaO_3(ZnO)_5$. (a) When the Fermi level is below E_{th}, the electron conduction mechanism is dominated by percolation. (b) Once the Fermi level becomes higher than E_{th}, electron transport is not inhibited by potential energy barriers such that the conduction mechanism is characterized by temperature-independent, degenerate conduction. Three-dimensional model is provided in Fig. 2.11.

2.3.3 Physical Configuration of IGZO

IGZO is a composite of In_2O_3, Ga_2O_3 and ZnO. The base constituent, In_2O_3, exhibits a high Hall mobility of ~34 $cm^2V^{-1}s^{-1}$. However, In_2O_3 invariably possesses a high electron density due to its tendency to form oxygen vacancies [48]. To suppress oxygen vacancy creation, the addition of an oxide with a strong metal-oxygen bond is required. Ga_2O_3 is selected for this purpose. The third component of IGZO, ZnO, is

characterized by a small atomic distance between Zn atoms, which helps the IGZO conduction band to spread out in energy, which leads to an increase in the electron mobility [48]. In addition, including an aliovalent cation with different ionic radii, such as ZnO, enhances amorphization [48]. As a result, IGZO exhibits a wide range of controllable carrier concentration although the carrier density itself is not as high as the original In_2O_3. Also, all of those constituents are environmentally benign.

Single crystal IGZO has a layered structure, consisting of alternate stacking of InO_2 and $GaO(ZnO)^+$ layers [49]. The distance of the closest atoms in amorphous IGZO is similar to its crystalline counterpart, although InO_6 and InO_5 are more dispersed than in the crystal and close to what is expected for a random cation distribution. In 5s orbitals of these components constitute the bottom of the conduction band. Also Nomura *et al.*, calculate the a-IGZO band structure and found that the effective mass is small, about 0.2 m_e. From this result, Nomura *et al.*, conclude that no localized states exist at the conduction band minimum, unlike a-Si:H [50].

2.4 Previously Reported Long-term Instability Problems

Several types of device instability phenomena have been reported previously. Crystalline Si MOSFETs at an early stage of development suffered from a variety of instability problems. a-Si:H TFTs exhbit an instability involving a threshold voltage shift. A brief summary of both types of instability is provided below.

2.4.1 Crystalline Silicon-based MOSFET Instability Problems

The flat-band voltage of a MOSFET is given by

$$V_{FB} = \phi_{MS} - \sum_i \frac{\gamma_i Q_i}{C_{INS}}, \tag{2.48}$$

where V_{FB} is the flat-band voltage, ϕ_{MS} is the work function difference between the silicon and gate metal, C_{INS} is the insulator capacitance density, Q_i is a total charge density brought by the i^{th} contribution to charge density within the insulator, and γ_i is a normalized insulator charge centroid, which is defined as

$$\gamma_i = \frac{\int_0^{t_{OX}} x\rho_i(x)dx}{t_{OX}\int_0^{t_{OX}} \rho_i(x)dx}, \tag{2.49}$$

where t_{OX} is the insulator thickness, x is the distance from the gate /SiO_2 interface, and $\rho_i(x)$ is the i^{th} contribution to the charge distribution inside the insulator.

Four types of non-ideal charge are known to exist at the SiO_2/Si interface or within the insulator [51]. These include 1) oxide trapped charge, 2) fixed oxide charge, 3) interface state charge, and 4) mobile ion charge. These non-idealities are summarized in Fig. 2.13.

Most Si MOSFET instabilities originate from some type of charge rearrangements or generation at or near the insulator-semiconductor interface. Examples of possible instability mechanisms include 1) interface state generation, 2) electron/hole capture/release by traps within the insulator, and 3) mobile ion migration within the insulator.

The deviation of the flat-band voltage from Eq. 2.48 caused by a single type of charge generation, recombination, or rearrangement is expressed mathematically,

$$\Delta V_{FB} = -\frac{1}{C_{INS}}\left[\gamma_i \Delta Q_i + \Delta\gamma_i Q_i\right], \tag{2.50}$$

An alternative way to express an instability-induced change in the flat-band voltage, which explicitly emphasizes its time dependence, is to differentiate Eq. 2.48 with respect to time, again assuming that one type of charge generation, recombination, or rearrangement dominates, yielding,

$$\frac{dV_{FB}(t)}{dt} = -\frac{1}{C_{INS}}\left[\frac{d\gamma_i(t)}{dt}Q_i(t) + \gamma_i(t)\frac{dQ_i(t)}{dt}\right]. \tag{2.51}$$

Thus, according to Eqs. 2.50 and 2.51, there are four ways to minimize instabilities: 1) reduce the total amount of charge, 2) locate the charge close to the gate /SiO_2 interface, 3) immobilize the charge, and/or 4) suppress charge generation and/or recombination. Notice that 1 and 4 involve modifications of $Q_i(t)$, whereas 2 and 3 are directed at $\gamma_i(t)$.

Next, individual types of non-ideal charge are considered with respect to MOSFET instabilities.

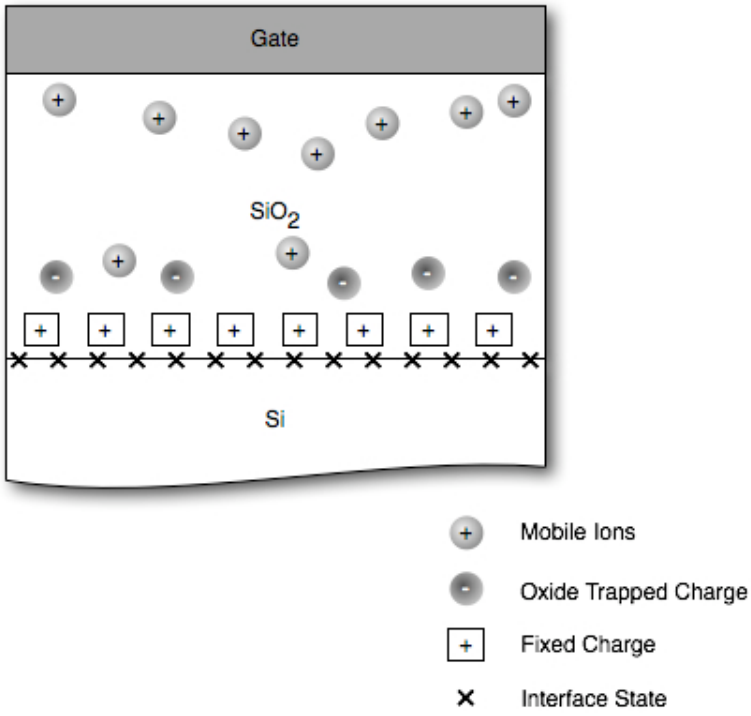


Figure 2.13: The four types of non-ideal charge which exist at the SiO_2-Si interface or within the insulator.

2.4.1.1 Interface State Generation

Si/SiO_2 interface states, which are sometimes called "fast" states, are disturbances of the crystalline Si lattice continuity, i.e., dangling bonds or bond angle misalignment. Dangling bonds are related to deep interface states which are located close to mid-gap, while states involving bond angle misalignment give rise to relatively shallow traps, often called band-tail states [52]. Interface states are energetically distributed throughout the bandgap, as shown in Fig. 2.14.

There are two basic types of electronic state associated with an energy level within the bandgap. An acceptor-like state is neutral if empty and is negatively charged after it captures an electron. In contrast, a donor-like state is neutral when occupied by an electron and is positive after it releases the electron. Acceptor-like

interface states are located in the upper portion of the bandgap, while donor-like states are present in the lower portion of the bandgap. The boundary energy between acceptor- and donor-like states is called the charge neutrality level (CNL). Interface charge is neutral when the Fermi level is aligned with CNL. As evident from Eqs. 2.50 and 2.51, an increase in the interface state density lends to a shift in the flat-band voltage. Additionally, an increase in the interface state density can degrade the subthreshold swing, as shown in Fig. 2.15 and as explained by Schroder [20] and Sah [10].

To minimize the density of deep interface states, an annealing process in an ambient such as 100% H_2 or 4% H_2 in forming gas is performed as a final process step to fill dangling bonds with H atoms [53].

However, Si-H or Si-OH bonds created thereby are relatively weak, and therefore easily broken by various stresses, such as Fowler-Nordheim tunneling [63] or avalanche electron injection [54], which leads to changes in the interface state density and concomitant degradation.

Water-related traps can also give rise to MOSFET instabilities. Feigl *et al.* found indiffused water in SiO_2 enhances both the density of traps in SiO_2 and the capture cross section of interface states [55]. Observing that interface state generation takes place after filling of traps inside SiO_2 and is related to the density of injected electrons, they suggested that interface creation is a three-step process involving 1) precursor generation in the SiO_2, 2) transport of precursors to the Si/SiO_2 interface, and 3)interface state creation. Batyrev *et al*. use computer simulation [56] to delineate how water molecules incorporated in the SiO_2 amorphous network evolve and

generate H^+ ions, which diffuse to the Si/SiO_2 interface and create Si dangling bonds [57]. First, the water molecule is integrated as an interstitial into the SiO_2. After it is incorporated into the Si-O-Si network and creates two silanol groups, it emits H^+, thereby absorbing a hole. Aided by the applied electric field, H^+ ions reach the Si/SiO_2 interface and react with Si-H bonds [58]. As a result, positively charged Si dangling bonds are generated at the Si/SiO_2 interface, and function as donor-like interface states.

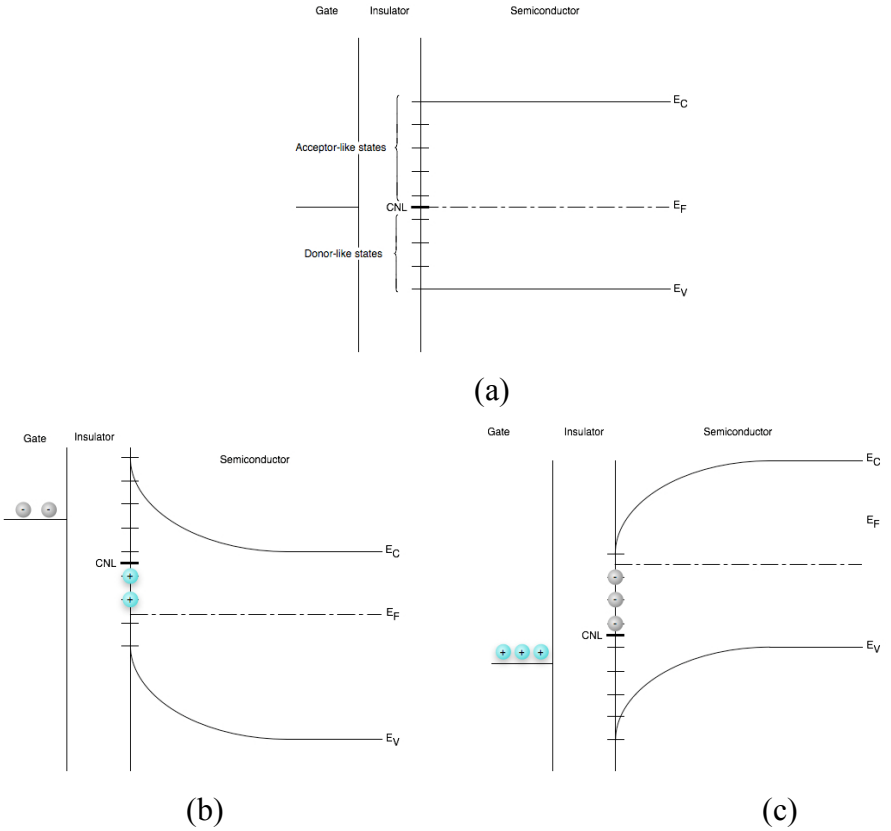


Figure 2.14: Interface states and the charge neutrality level. (a) Interface states located at above CNL are acceptor-like and those located below CNL are donor-like. (b) When a negative voltage is applied to the gate, the Fermi level relatively moves downward, so that some of the donor-like interface states lose electrons and the interface becomes positively charged. (c) In the contrast, when a positive voltage is applied to the gate, the Fermi level near the SiO_2/Si interface moves upward, so that electrons occupy some of the acceptor-like states such that the interface becomes negatively charged.

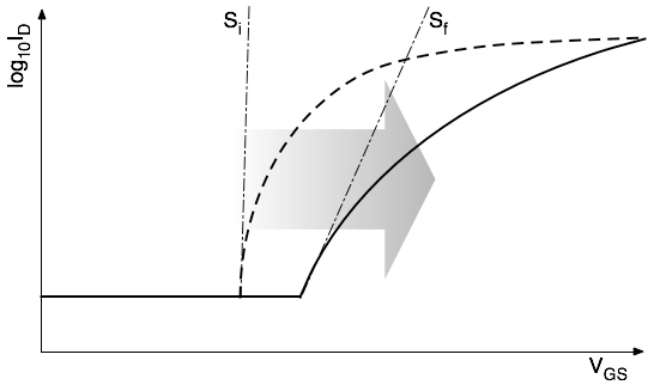


Figure 2.15: Degradation of the subthreshold swing caused by interface state creation. S_i = initial (undegraded) subthreshold swing and S_f = final (degraded) subthreshold swing.

SiO_2/Si interface state generation is also reported for the long-term gate stress of MOSFETs with a boron-doped (p-type) polysilicon gate [59][60]. This type of interface state generation becomes more severe when the sample is annealed in H_2. An increase in the number of the interfaces traps is observed at its peak of the distribution, which is located at an energy of 0.7 eV above the valence band edge. Ushizaka *et al.* hypothesized that this degradation is brought about by ionized hydrogen migrating to the Si/SiO_2 interface and the build donor-like interface states, in the same manner as that discussed previously for water-diffused SiO_2. This degradation can be alleviated by annealing in a N_2 ambient [60][61]. This type of degradation is not observed when a phosphorous-doped (n-type) polysilicon gate is used.

The interface state density is also increased by irradiation of photons having an energy larger than the Si bandgap [62]. Although arising from different mechanisms, interface state generation by various mechanisms appears to have much in common as

pointed out by Lopez-Villanueva *et al.* [63], indicating that the underlying physics involving H^+ creation and incorporation at the SiO_2/Si interface is the same.

2.4.1.2 Insulator Trapped Charge

Insulator trapped charge refers to traps inside the SiO_2 which are attributed to defects in the SiO_2 amorphous structure, such as oxygen vacancies. These types of traps are electrically neutral when empty and become negatively or positively charged with the capture of an electron or hole, respectively [51]. Because of the high potential barrier of carriers in silicon with respect to SiO_2, which is estimated to be ~3.1 eV for electrons and ~4.9 eV for holes, insulator trapped charge states may not be filled unless there is either a high electric field high enough to induce the tunneling/avalanche carrier injection or radiation/illumination is present which can introduce carriers into the SiO_2 layer. Therefore, under device operation using a relatively small gate field in the dark, this mechanism may be excluded from the possible instability mechanisms.

Insulator trapped charge effects the flatband voltage, and results in a threshold voltage shift as described mathematically by Eqs. 2.50 and 2.51, causing a rigid shift in a $\log_{10}I_D - V_{GS}$ plot. The direction of the threshold voltage shift depends on which type of carrier is trapped. The threshold voltage moves to a more positive voltage if electrons are trapped, while it moves to a more negative voltage if holes are captured. In contrast to the interface state generation, the subthreshold slope if not effected by charges in the insulator trapped charge density.

Insulator trapped charge within SiO_2 was first investigated by Williams in 1965, using a MOS capacitor structure [64]. He found traps within the bandgap of SiO_2 located ~2 eV below the conduction band minimum of SiO_2 with a density of $2.9\times10^{14}\ cm^{-3}$ and a capture cross-section of $1.3\times10^{-12}\ cm^{2}$. He briefly mentioned the possibility that these traps may not be located at a specified discrete energy level, but could be distributed in energy below this level.

Nicollian *et al.* measured a water-related acceptor-like trap located ~ 0.3 eV below the SiO_2 conduction band minimum with a capture cross-section of $1.5\times10^{-17}\ cm^{2}$ and with a maximum density of $\sim 6.0\times10^{18}\ cm^{-3}$ [65]. However, it is possible that this capture cross-section may actually be underestimated because of the intense electric field employed for avalanche injection, since the capture-cross section shrinks with increasing electric field [16]. Feigl *et al.* also concluded that post-metallization annealing is effective in reducing the density of traps with a capture cross-section of $\sim 10^{-17}$ cm^2. Extended post-oxidation annealing at a temperature of 1000 °C in dry N_2 for 16 hours reduces the density of the traps with a cross-section of $\sigma_C = \sim 10^{-18}$ cm^2 [55]. Other reports of insulator-trapped charge are summarized in Fig. 7-8 of Ref. 53 by Wolf.

2.4.1.3 Mobile Ion Charge

Thermally-grown SiO_2 has an amorphous structure, although, like most amorphous materials, it does exhibit a significant degree of short-range order [52]. It also possesses a rather open network which allows a mobile ion to move with a high

mobility. Historically, Na^+, Li^+ and K^+ ions were reported to migrate through a crystalline SiO_2 at a temperature lower than 250°C as early as 1888 [35].

Mobile ions are often initially located at the gate-metal/SiO_2 interface [52], where their effect is minimal since the normalized charge centroid factor is zero. However, displacement of this charge due to the application of an electric field leads to a threshold voltage shift as indicated in Eq. 2.51. For example, movement of positive ions away from the gate/SiO_2 interface due to the application of a positive gate voltage leads to a negative threshold voltage shift. In contrast, the threshold voltage is almost unchanged if a negative is applied. The subthreshold swing is not affected by the movement of mobile ion.

It is clear whether the threshold voltage shift is caused by oxide trapped charge or mobile ion charge because of the asymmetric nature and different polarity voltage threshold shift trends. The threshold voltage shift caused by oxide trapped charge exhibits a positive threshold voltage shift when the gate voltage is positive, while a negative gate voltage leads to the opposite result.

Several processing procedures are employed to minimize the effects of mobile ion charge.

The first processing procedure employed is to reduce the mobile ion concentration in the insulator by avoiding thermal evaporation using a tungsten filament for metallization and, instead, using electron beam evaporation. The tungsten filament is a probable source of mobile ion contamination [52].

A second processing procedure is to immobilize ions by gettering. The most common ion contaminant is Na^+ which moves to the Si/SiO_2 interface with application

of a positive voltage to the gate. To minimize this problem, phosphorous is introduced and diffused into the SiO_2 in order to create a thin phosphosilicate glass film on top of the SiO_2 layer, in which Na^+ ions are trapped and immobilized [52]. Since, according to Eq. 2.48, charge localized near to the gate/SiO_2 interface has a minimal effect on the MOSFET flat-band voltage shift, MOSFETs processed using a phosphosilicate glass film exhibit more stable characteristics [52]. This method, however, introduces another instability problem which is called dipolar polarization [52]. This mechanism is associated with the molecular structure of the phosphosilicate glass, which contains numerous permanent electric dipoles. These dipoles respond to the applied electric field more slowly than the SiO_2 network itself, giving rise to a dipolar polarization instability mechanism [52].

The last processing procedure considered is to introduce chlorine into the insulator to neutralize the positive ion charge and to also reduce the amount of mobile charge incorporated into the insulator. The incorporated chlorine is located close to the Si/SiO_2 interface [52], in an electrically neutral form. If a positive voltage is applied to the gate for an extended period of time, positive ions such as Na^+ move towards the Si/SiO_2 interface and are trapped by the chlorine. However, it is possible for these Na^+ ions to be de-trapped. Therefore, the use of chlorine is usually limited to that of a pre-clean process of the oxidation furnace chamber so that Na is not incorporated into the SiO_2 in the first place [52].

2.4.2 Hydrogenated Amorphous Silicon (a-Si:H) TFT Instabilities

Hydrogenated amorphous silicon (a-Si:H) TFTs are known to exhibit electrical instability, especially with regard to a threshold voltage shift [66]. Two mechanisms are thought to be associated with this instability: 1) carrier injection and capture by traps inside the a-SiN_X:H gate insulator and 2) dangling bond creation inside the a-Si:H [67]. These two mechanisms can concurrently contribute to the threshold voltage shift.

A variety of experiments have been designed and performed to understand the dominant threshold voltage shift mechanism. An effective and revealing instability assessment procedure involves measuring the transfer curve shift as a function of aging time using ambipolar TFTs [67]. An ambipolar TFT is a standard a-Si:H TFT except that it does not have n^+ source/drain contact layers so that both types of carriers, i.e. electrons and holes, can contribute to the flow of conduction current in the channel. Hole (p-type) and electron (n-type) conduction can be investigated by merely changing the polarity of the applied gate voltage. In the measurement, contact resistance problems are minimized by using unusually large dimensions [67].

Using ambipolar TFTs, it is possible to tell which instability mechanism is involved by observing the movement of the two $\log_{10}(I_D) - V_{GS}$ transfer curves (one involving electron transport and the other due to hole transport) in the following manner. 1) If the directions of movement of the n- and p-type transfer curves are opposite to one another, dangling bond creation inside the a-Si:H is the dominant cause of the threshold voltage shift. Alternatively, 2) if the directions of movement of

the n- and p-type transfer curves are the same, carrier injection and capture by traps in the a-SiN_X:H insulator is dominant. This carrier injection and trapping in the insulator mechanism is also witnessed as an instability mechanism in Si MOSFETs.

From the studies by many researchers, it was concluded in the early 1990s that the dominant a-Si:H TFT instability mechanism is charge injection followed by trapping in the gate insulator [67]. Based on this conclusion, Libsch and Kanicki formulated a dynamic model to describe empirical threshold voltage shift data [68]. The formulation is

$$\left|\Delta V_T\right| = \left|\Delta V_0\right|\left\{1-\exp\left\{-\left[\frac{t}{\tau}\right]^{\beta}\right\}\right\}, \tag{2.52}$$

where β is a constant, τ is a time constant which may be expressed as $\tau = \tau_0 \exp\left[\frac{E_\tau}{k_B T}\right]$, and $\left|\Delta V_0\right|$ is the potential difference across the insulator which is approximated as $\left|V_{GS} - V_{T0}\right|$, where V_{T0} is the initial threshold voltage, E_τ is an effective potential barrier for carriers to enter the insulator which is expressed in $E_\tau = \frac{E_A}{\beta}$, where E_A is a thermal activation energy. This model suggests that carriers injected into band-tail states of the a-SiN_X:H insulator near the a-Si:H/a-SiN_X:H interface may possibly be re-emitted to other states which are located deeper in the insulator. The extent of this charge redistribution increases as the stress time/field/temperature increases, which leads to the time-dependent exponential term in Eq. 2.52. This model offers a relatively good description of threshold voltage shifts under D.C. biasing [67].

3 EXPERIMENTAL TECHNIQUES

3.1 Thin-Film Transistor Preparation

The techniques employed in this research to deposit thin films onto a substrate are sputtering, when electrodes are made using indium tin oxide (ITO), and thermal evaporation, when aluminum electrodes are used. A brief description of these two process technologies is given in the following subsections.

3.1.1 Sputtering

There are several ways to deposit thin films onto a substrate, but the most widely-employed semiconductor-based techniques are chemical vapor deposition (CVD) and physical vapor deposition (PVD). Sputtering and thermal evaporation, the primary major methods used to make TTFTs in the research described herein, are categorized as PVD. The basic procedures of PVD process are: 1) vaporizing target materials via a physical process, 2) transporting the vaporized materials across the gap between the target and the substrate, and 3) forming a thin film on the surface of the substrate. In the remainder of this subsection, sputtering is discussed.

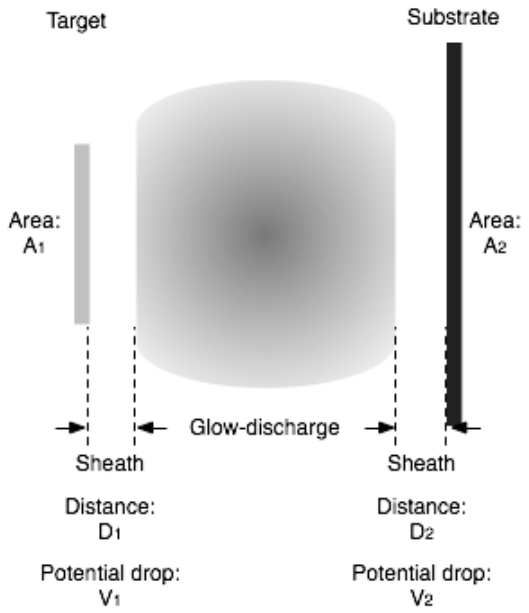


Figure 3.1: Plasma discharge architecture typical of that used for sputter deposition.

Sputtering is a dominant technology employed in modern integrated circuit manufacturing, mainly because of controllability over the parameters of the deposited film, such as the thickness and the stoichiometry [53]. Sputtering tends to yield poor step coverage compared to CVD. This is because atoms deposited by CVD move freely on the surface and incorporate into the film at stable, low-energy atomic sites. In contrast, PVD-deposited species tend to immediately stick to the surface upon which they land [69].

There are two primary reasons why PVD is preferred to CVD for TFT fabrication: 1) CVD usually requires a higher process temperature than sputtering. Since it is desirable that transparent oxide materials be deposited onto a low-temperature substrate such as plastic, a low process temperature is preferred. 2) CVD equipment is usually more elaborate than that used for sputtering [70].

Sputtering is a process in which atoms, ions, and clusters thereof are ejected from the surface of a target as a consequence of accelerated ion bombardment and deposited onto the surface of the substrate, thereby resulting in the deposition of a thin film. The glow-discharge created between a target and a substrate is a central feature of sputtering. This glow discharge consists of plasma with an equal number of working gas ions and electrons. Typically, argon (Ar) is chosen as the working gas because of its relatively reasonable price and availability. Inside the glow-discharge bulk, Ar atoms are ionized and excited as a result of their interaction with energetic electrons. Excited Ar atoms relax, emitting photons, which causes the plasma to glow with a characteristic color. Ar ions inside the glow discharge move by diffusion and are not energetic enough to ionize or dissociate other gas species, since the electric field that exists inside the glow-discharge plasma bulk is relatively weak. However, once the Ar ion reaches the edge of the plasma and enters into the region between the edge of the glow discharge and the target, which is called the sheath, the ion is accelerated by a strong electric field present in the sheath and impinges upon the surface of the target. Consequently, target atoms, ions, and clusters thereof are ejected from the target surface typically with an energy of ~10-40 eV, which is too energetic to settle on the surface of the substrate [53]. However, because their mean free path is usually less than the spacing between the target and the substrate, the collision that the sputtered species may experience reduce their energy to ~1-2 eV [53].

These collisions not only reduce the kinetic energy of the sputtered atoms but also cause atoms with smaller atomic mass than Ar to be dispersed more severely. For the work described herein, the element with the least mass is oxygen, which is about

16, and almost half of that of Ar, while gallium (Ga) has almost double the mass and In has approximately three times the mass of Ar. Thus, from these considerations, it is possible that the stoichiometry of the deposited film is altered from that of the target [28][71]. The atomic mass for each constituent is tabulated below.

Up to now, DC sputtering has been implicitly assumed in this discussion. However, when an insulating target, which is exclusively employed in the fabrication of the AOS channel layers studied in this thesis, is used, the glow-discharge cannot be sustained once the substrate that is connected to an electrode which is covered with a layer of the insulating channel material. Hence, RF sputtering instead of DC is employed for this study.

RF sputtering is different from its DC counterpart in the way in which the potential difference is applied: RF sputtering uses an AC voltage, while DC sputtering uses a DC voltage. The reason why RF is applied for the name instead of AC is that the actual AC signal frequency used is 13.56 MHz, to confine unwanted radio frequency broadcasting.

Ion bombardment of the target requires a DC electric field strong enough to accelerate ions from the glowing discharge to dislodge constituent species from the target. Although the applied voltage is AC, a DC potential difference builds up at the sheath after several cycles of the applied AC voltage. This is brought about by the fact that negative charge accumulates on the electrode surface because the mass of an electron is much smaller than that of an ion and, therefore, more electrons are attracted to the electrode surface than ions in the same period of time. This phenomenon is

called self-bias, and the self-bias voltage level is almost at the same magnitude as the AC voltage, as depicted in Fig. 3.2.

The reason why ion bombardment occurs preferentially on the target side rather than the substrate side can be explained as follows [53]: The current flux of ions flowing through the sheath can be expressed using the Child-Langmuir equation,

$$J = \frac{K}{m^{\frac{1}{2}}} \frac{V^{\frac{3}{2}}}{D^2}, \tag{3.1}$$

Element	Atomic mass [72]	Work function [73]	Vapor pressure [Pa]
Ar	39.948	-	-
O	15.9994	-	-
In	114.818	4.08	1.42×10^{17} @ 156.76°C
Zn	65.39	4.30	19.2 @ 419.73°C
Ga	69.723	4.25	9.31×10^{-36} @ 29.9°C
Sn	118.710	4.35	5.78×10^{-21} @ 232.06°C

Table 3.1: The atomic mass, work function, and vapor pressure of atomic constituents employed in the sputter deposition of several types of AOS.

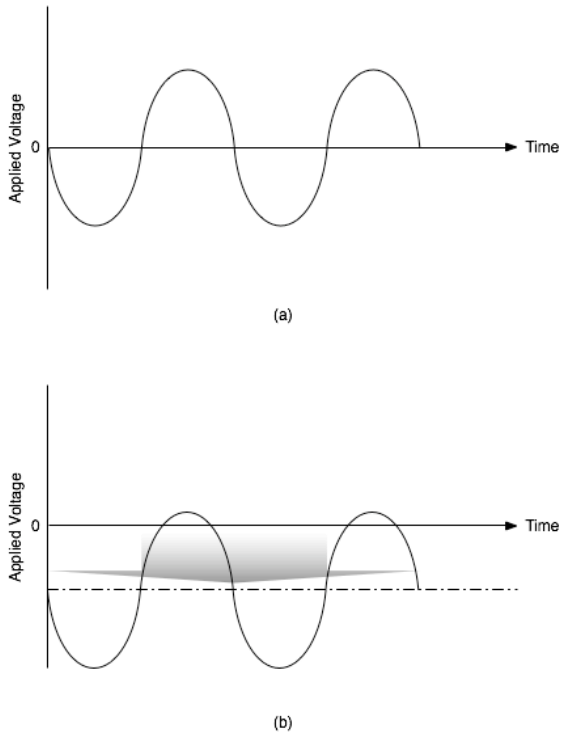


Figure 3.2: DC level shift of the applied AC voltage: a) the initial AC signal of the applied voltage signal, which is sustained for the first few cycles. b) The steady-state substrate potential, illustrating the self-bias voltage.

where V is the potential difference across the sheath, D is the distance across the sheath, m is the mass of the ion, and K is a constant. Setting up two equations, one for each sheath, namely one for the space between the glow discharge and the target, the other for the discharge and the substrate, and recognizing that the current densities through both sheaths are equal and that the constants K and the ion mass are common, one can derive the following equation,

$$\left(\frac{V_1}{V_2}\right)^{3/2} = \left(\frac{D_1}{D_2}\right)^2. \tag{3.2}$$

Modeling the sheath as a capacitor, and realizing that the two capacitors representing each sheath are in series,

$$C_1 V_1 = C_2 V_2, \text{ or} \tag{3.3}$$

$$\frac{V_1}{V_2} = \frac{C_2}{C_1}. \tag{3.4}$$

Using the basic formula for a capacitor, $C = \varepsilon \frac{A}{D}$, where A is the area of the electrodes, with the permittivity ε common for both sheaths, one can modify Eq. 3.4 as follows:

$$\frac{D_1}{D_2} = \frac{A_1}{A_2}\frac{V_1}{V_2}. \tag{3.5}$$

Then plugging Eq. 3.5 to Eq. 3.2 yields

$$\frac{V_1}{V_2} = \left(\frac{A_2}{A_1}\right)^4. \tag{3.6}$$

Theoretically, this equation means that the smaller the area of the electrode, the stronger the electric field close to the electrode. The stronger electric field close to the electrode leads to higher energy ion bombardment, which results in more pronounced sputtering. Although the exponent of four has never been confirmed experimentally, the principle that the smaller area electrode possesses a larger sheath potential is still valid [53]. Thus, the size of the electrode on which the target is attached is minimized to maximize the sputtering flux. On the other hand, the electrode on the substrate side is made as large as possible, usually the whole inner surface of the chamber is connected, in order to minimize unwanted ion-bombardment onto the substrate [53].

The sputtering system used for this thesis research is a customized magnetron sputtering system developed and constructed by Chiang and Tasker [74]. The chamber is a stainless steel vacuum chamber made by Nor-Cal Product, Inc. with a load lock. A McAllister DPRF-450 rotary platform is employed for the substrate

tilting and a Solar Products QH series resistive coil heater for the substrate heating. The system also equips two 3-inch Mighty Mak L300A01L, three 2-inch L200A01L sputter guns manufactured by US Inc. with a RNI OEM-25A 2500W RF power supply unit. The pumping system for the load lock consists of a Leybold DryVac 50B oil-free mechanical pump and a RuVac pump in series for rough pumping. The main chamber has a Varian TV1001 Navigator turbo-molecular pump with another DryVac 50B for backing up. The sputtering system is computer-controlled by a personal computer with a graphical user interface via an Adlink PCI-7248 digital input/output board.

TFT channel layers are created using the ambient gas pressure of 5 mTorr. The background pressure is 1×10^{-7} Torr. The RF power employed is 100 W or 75 W and the spacing between the target and the wafer is 4 inches. The IGZO 3-inch ceramic target is provided by Cerac Inc., and the stoichiometry is In:Ga:Zn:O=1:1:1:4. The deposition time used is 3.33 minutes and the channel thickness is approximately 80 nm. The deposition is accomplished with a shadow mask. Pre-sputtering is performed for 1 hour with a Ar/O_2 composition of 90/10 followed by 10 minutes in a pure Ar ambient.

3.1.2 Thermal Evaporation

Some of the samples tested have aluminum (Al) contacts instead of ITO contacts. For those samples, the Al electrodes are deposited by thermal evaporation. Thermal evaporation is a much simpler method than sputtering. It consists of three basic processes: 1) sublimation of the target material, 2) transport of sublimed species to the substrate, 3) deposition onto the surface of the substrate. Thermal deposition is

inexpensive and the deposition rate is high. In spite of these advantages, however, it is only applicable to the deposition of aluminum for TFT fabrication since each constituent of a compound material such as ITO or IGZO has a different vapor pressure (see Table 3.1). Because the constituent with high vapor pressure sublimes more rapidly than those with lower vapor pressures, an evaporated compound thin film typically has a poor stoichiometry [75].

The thermal deposition system used for Al evaporation is a Polaron model E6100, which has a basket-shaped resistive filament in a glass chamber. The base pressure of the system is 5×10^{-5} mbar, which is $\sim3.75\times10^{-2}$ mTorr.

3.1.3 Post Deposition Annealing

It is known and exploited in TFT fabrication that the carrier concentration of single crystal IGZO can be controlled by employing an annealing process after channel layer deposition [45]. Also, the channel mobilities of several types of AOS have been reported to be large only after annealing at several hundred degrees Celsius [76][77]. Vapor deposition of certain materials onto unheated substrates has been reported to cause the creation of minute voids, which are less than ~6 Å in diameter for a-Ge, for example [43]. Thus, it is possible that post-deposition annealing decreases the number of physical voids, traps, and/or defects within a channel layer [78], although the exact physical mechanism responsible for such an improvement has yet to be confirmed.

After deposition of the electrodes, samples are annealed in a furnace. The temperature-time profile of this post-deposition annealing process is shown in Fig. 3.3. Since there is no active cooling implemented in the annealing system used, the

temperature slope of the decreasing part of the profile is more gradual than two degrees per minute. The oven used for this process is a Burnstead Thermolyne 62700 furnace or a Neytech Qex vacuum furnace.

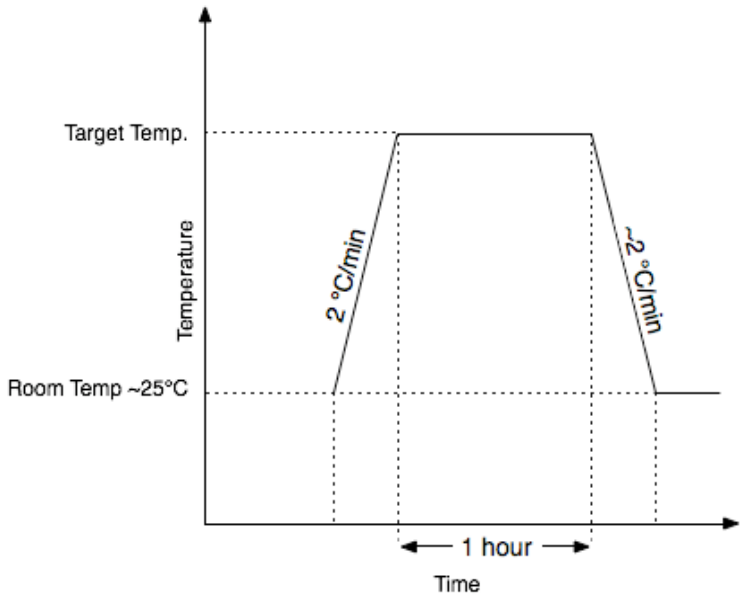


Figure 3.3 Temperature-time profile for the post-deposition annealing process.

3.2 Sample Preparation

Sample Group Name	Power [W]	Sputtering Ambient	Electrode	Annealing Temperature [°C]	Number of Die
June202007	100	Pure Ar	ITO	200	6
				250	6
				300	6
061202A	125	Ar: 96% O_2: 4%		100	1
				150	1
				200	1
				250	1
				300	1
				350	1
061206 A	75	Ar: 96% O_2: 4%		175	1
				250	1
				300	1
061206 B	100	Ar: 97% O_2: 3%		175	1
				250	1
				300	1
July132007 #1 (1, 3, 5)		Pure Ar		300	3
July132007 #1 (2, 4, 6)		Pure Ar	Al		3
July132007 #2		Pure Ar	ITO	250	3

Table 3.2: A summary of the process conditions used to fabricate IGZO TFTs, including the RF sputter power, working gas composition, the device structure, the electrode material, the annealing temperature, and the number of die. The total pressure is 5 mTorr.

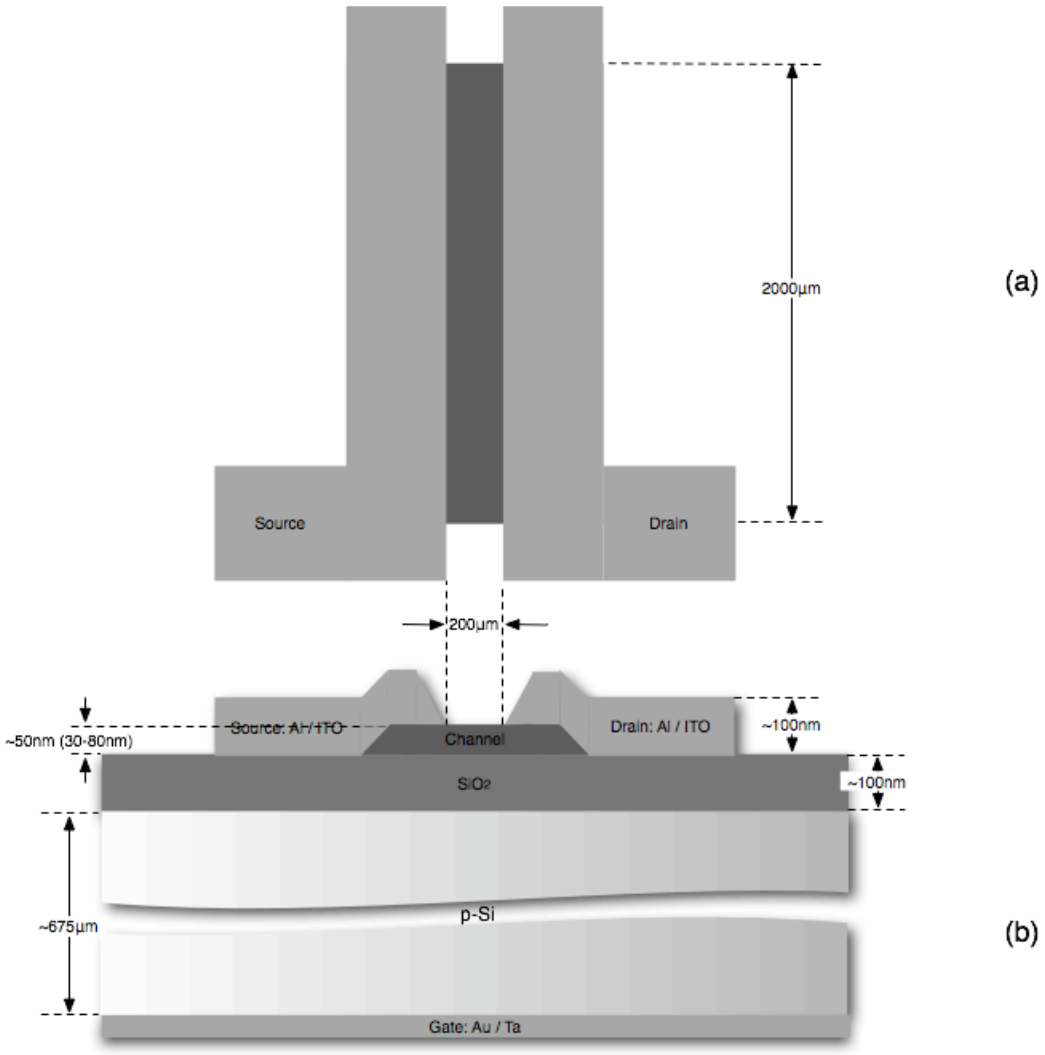


Figure 3.4: (a) Top down and (b) cross-sectional view of the TFT device structure.

Several different process conditions and materials are employed for sample fabrication. Each process condition might differ in the RF power, the working gas ratio, and/or the electrode which is either Al or ITO. Each sample group consists of three to six die that are processed at a different post-deposition annealing temperature, which ranges from 100 to 350 °C. Detailed fabrication information with the number of die and the annealing temperature for each sample group is provided in Table 3.2. Each die has six devices; three have the device size of 2000 µm / 200 µm (a 10/1 ratio) and the other three have 1000 µm / 200 µm (a 5/1 ratio). All samples are

fabricated on a p-type silicon wafer with a thermally-grown silicon dioxide layer provided by the Hewlett-Packard Development Company, L. P. The silicon wafer thickness is ~675 μm and the doping density is $\sim 3 \times 10^{16}$ m^{-3}. A detailed TFT device structure description is provided in Fig. 3.4.

3.3 Stability and TFT Temperature Assessment

Two different types of TFT electrical characterization experiments are conducted in this research project: 1) stability testing and 2) temperature-dependence assessment. Stability testing consists of constant-voltage bias-stress testing and two different types of recovery testing – zero-bias room temperature recovery testing and accelerated recovery testing. Details of each type of testing and an explanation of parameters employed to assess the data are provided in the following subsections.

3.3.1 Device Parameters

In this subsection, device parameters employed in this research are discussed in detail. From a $\log_{10}(I_D)$ - V_{GS} transfer curve plot, turn-on voltage, V_{ON}, subthreshold swing, S, drain current on-to-off ratio, $I_D^{ON\text{-}OFF}$, drain current hysteresis, H_{I_D}, and drain current hysteresis difference, ΔH_{I_D}, are extracted and assessed. An example of V_{ON}, S, and $I_D^{ON\text{-}OFF}$ parameter extraction is shown in Fig. 3.5. V_{ON} is defined as the voltage at which the positive transfer curve – a measurement sweep from V_{GS} = -20 V to 40 V – begins to increase with increasing V_{GS}. Subthreshold swing, S, is assessed as the inverse of the maximum slope of the positive sweep, when it is evaluated at V_{GS} slightly greater than V_{ON},

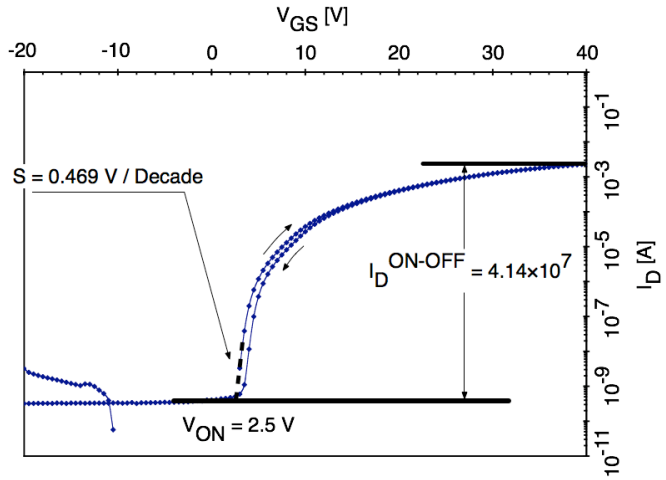


Figure 3.5: Parameter extraction from a $\log_{10}(I_D)$ - V_{GS} transfer curve measured at 50 °C with V_{DS} = 20 V for sample June202007-1 which is annealed at 300 °C. See Table 3.2 for more sample details. Note that the transfer curve exhibits a small amount of clockwise (CW) hysteresis.

$$S = \left(\frac{d \log_{10} I_D}{dV_{GS}} \Big|_{V_{GS} \approx V_{ON}} \right)^{-1}. \tag{3.7}$$

Drain current on-to-off ratio, $I_D^{ON\text{-}OFF}$, is defined as a ratio of the maximum to minimum current, namely,

$$I_D^{\,ON-OFF} = \frac{I_{ON}}{I_{OFF}}, \tag{3.8}$$

where I_{ON} is approximated as I_D at V_{GS} = 40 V and I_{OFF} is established by the gate leakage / noise floor at $V_{GS} < V_{ON}$.

The presence of hysteresis in double-swept transfer curves requires development of an evaluation methodology for its quantitative assessment. This is accomplished as follows. Figure 3.6 illustrates an idealized $\log_{10}(I_D) - V_{GS}$ transfer curve exhibiting clockwise (CW) hysteresis. As shown, two types of hysteresis may be specified. Gate voltage hysteresis, $H_{V_{GS}}$, is evaluated at a constant drain current as the maximum difference in gate voltages between the positive and negative sweep. This kind of

hysteresis has been discussed previously [79], and corresponds to a simple shift in the turn-on voltage for a well-behaved transfer curve with minimal hyteresis-induced distortion. Alternatively, drain current hysteresis, H_{I_D}, is defined as the maximum drain current difference between positive and negative sweeps at a constant gate voltage.

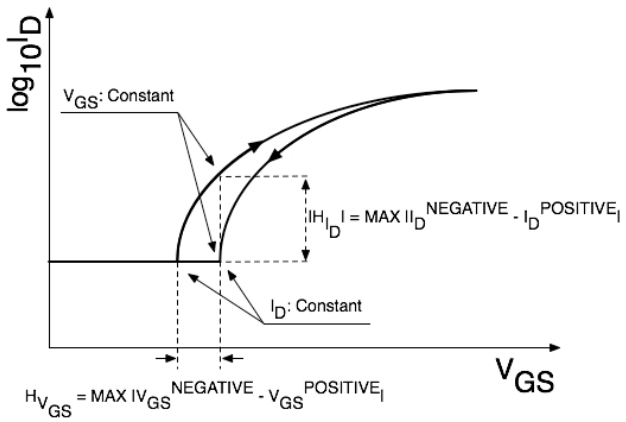
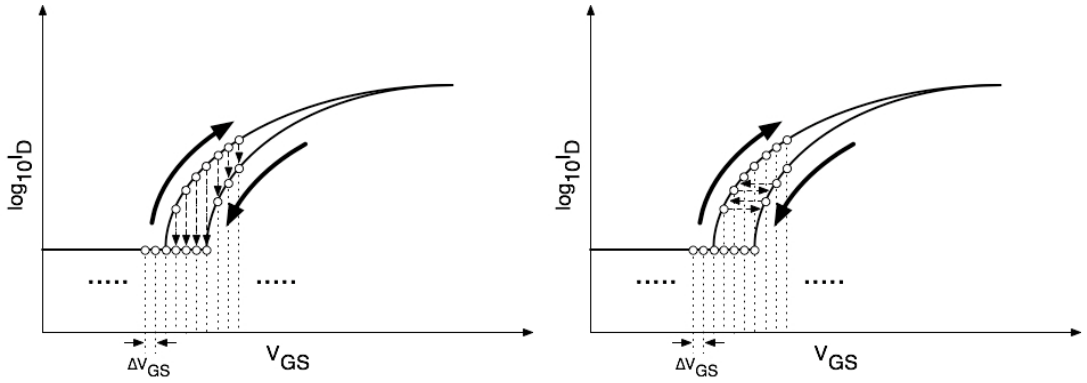


Figure 3.6: Definitions of gate voltage hysteresis, $H_{V_{GS}}$, and drain current hysteresis, H_{I_D}, for the case of clockwise hysteresis. Notice that the gate voltage hysteresis without distortion in the transfer curve is specified by the turn-on voltage shift.



(a) (b)

Figure 3.7: Transfer curves with discretized points at constant V_{GS} steps are indicated as open circles. (a) Demonstrates that drain current hysteresis, H_{I_D}, is easily assessed since it is obtained at constant V_{GS}. (b) Shows that evaluating the gate voltage hysteresis, $H_{V_{GS}}$, is problematic since V_{GS}'s at constant I_D are not available due to the data acquisition technique employed in this research.

H_{I_D} rather than $H_{V_{GS}}$ is employed in this research project for reasons associated with data acquisition and automated assessment, as discussed within the context of Fig. 3.7. As indicated in Fig. 3.7 (a), $I_D - V_{GS}$ data is acquired by incrementally changing V_{GS} while monitoring I_D so that functionally the data is presented in an $I_D(V_{GS})$ format. This $I_D(V_{GS})$ format is well-suited to H_{I_D} assessment. In contrast, Fig. 3.7 (b) highlights the basic problem associated with $H_{V_{GS}}$ evaluation, namely that it requires a $V_{GS}(I_D)$ data format. Since automated hysteresis evaluation is more convenient, H_{I_D} assessment was selected.

H_{I_D} may be expressed mathematically

$$H_{I_D} = \text{sgn}\left[\log_{10} I_D{}^{NEGATIVE} - \log_{10} I_D{}^{POSITIVE}\right] \max\left|\log_{10} I_D{}^{NEGATIVE} - \log_{10} I_D{}^{POSITIVE}\right|, \tag{3.9}$$

Parameter	**Sign**	
	Positive	**Negative**
H_{I_D}	Clockwise	Counterclockwise
ΔH_{I_D}	If hysteresis is *clockwise* in the pre-stressed state, hysteresis becomes *narrower* in the post-stressed state. If hysteresis is *counterclockwise* in the pre-stressed state, hysteresis becomes *wider* in the post-stressed state.	If hysteresis is *counterclockwise* in the pre-stressed state, hysteresis becomes *narrower* in the post-stressed state. If hysteresis is *clockwise* in the pre-stressed state, hysteresis becomes *wider* in the post-stressed state.

Table 3.3: A summary of a sign conventions associated with hysteresis assessment for drain current hysteresis, H_{I_D} and drain current hysteresis difference, ΔH_{I_D}.

where $I_D^{NEGATIVE}$ and $I_D^{POSITIVE}$ refer to drain currents, evaluated at a constant V_{GS}, for the negative and positive sweep directions, respectively, and sgn is a sign function defined by

$$\mathrm{sgn}(x) = \begin{cases} -1 & for \quad x < 0 \\ 0 & for \quad x = 0 \\ +1 & for \quad x > 0 \end{cases}. \tag{3.10}$$

This definition for H_{I_D} merits further discussion. The magnitude of H_{I_D} is determined by the $\max\left|\log_{10} I_D^{NEGATIVE} - \log_{10} I_D^{POSITIVE}\right|$ term, which, in words, is equivalent to the maximum difference in $I_D^{NEGATIVE}$ compared to $I_D^{POSITIVE}$. An absolute value of the $I_D^{NEGATIVE}$ - $I_D^{POSITIVE}$ difference is employed in order to decouple H_{I_D} magnitude and sign information. In fact, H_{I_D} sign information is explicitly taken into account through the inclusion of the $\mathrm{sgn}\left[\log_{10} I_D^{NEGATIVE} - \log_{10} I_D^{POSITIVE}\right]$ term. H_{I_D} is positive if hysteresis is clockwise (CW) and negative if counterclockwise (CCW), as shown in the first row of Table 3.3.

In addition to evaluating hysteresis for a single dual-sweep $\log_{10}(I_D) - V_{GS}$ transfer curve, it is desirable to assess the extent of hysteresis by comparing two sets of transfer curves obtained before and after subjecting a TFT to a bias-stress test. This gives rise to the drain current hysteresis difference defined as

$$\Delta H_{I_D} = H_{I_D}^{POST} - H_{I_D}^{PRE}, \tag{3.11}$$

where $H_{I_D}^{POST}$ and $H_{I_D}^{PRE}$ correspond respectively to drain current hysteresis after and before undertaking a bias-stress test.

Sign conventions associated with ΔH_{I_D} are rather complicated and are summarized in Table 3.3. As shown in the bottom portion of Table 3.3, positive ΔH_{I_D} means that hysteresis becomes wider (narrower) after stress testing if the hysteresis is CCW (CW) in the pre-stressed state. A negative ΔH_{I_D} corresponds to hysteresis becoming narrower (wider) after stressing if the hysteresis is CCW (CW) in the pre-stressed state.

3.3.2 Constant-Voltage Bias-Stress Testing

TFT device stability is assessed via constant-voltage DC testing over a period of 10^5 seconds at room temperature by monitoring the drain current at a constant V_{GS} and V_{DS}. Specifically, $V_{GS} = V_{DS} = 10$ V, 20 V, 30 V; $V_{GS} = 20$ V / $V_{DS} = 30$ V; and $V_{GS} = 30$ V / $V_{DS} = 10$ V. Acquired drain current data are plotted according to a semi-log scaled time function.

Before and after stability testing, transfer characteristics (I_D - V_{GS} and $\log_{10}(I_D)$ - V_{GS}) at $V_{DS} = 30$ V is measured and plotted.

3.3.3 No-Bias Room Temperature Recovery and Accelerated Recovery Procedures

After completing a constant-voltage bias-stress test, selected devices are subjected to a no-bias room temperature recovery procedure or an accelerated recovery procedure.

In the no-bias room temperature recovery procedure, devices are observed to return to their virgin electrical state when simply left for an extended period of time in

the dark with all three terminals open-circuited. The duration of recovery varies from 7 to 63 days.

The intent of the accelerated recovery procedure is to attempt to thermally reset the TFT back to its original unstressed state in a more controlled and accelerated fashion. Since a-Si:H TFTs are reported to recover to their original state after annealing at 200 °C for 30-60 minutes [80], a similar procedure was investigated for IGZO TFTs. Accelerated recovery conditions investigated are: (i) room temperature, 50 °C, 75 °C, 100 °C, or 150 °C, (ii) all terminals open-circuited, i.e., $V_G = V_D = V_S =$ open, $V_G = V_D = V_S = 0$ V, or $V_G = -10$ V & $V_D = V_S = 0$ V, and (iii) testing duration is 10^5 s.

3.3.4 TFT Temperature-Dependence Assessment

Temperature-dependence testing is carried out by measuring two transfer characteristics ($\log_{10}(I_D)$ - V_{GS}) using two different values of V_{DS}, namely, $V_{DS} = 30$ V and 1 V. From the $V_{DS} = 30$ V transfer characteristic, the turn-on voltage, V_{ON}, subthreshold swing, S, drain current on-to-off ratio $I_D^{ON\text{-}OFF}$, average mobility, $\mu_{AVG}(V_{GS})$, incremental mobility, $\mu_{INC}(V_{GS})$, are extracted

From the $V_{DS} = 1$ V transfer curve, the average and incremental mobilities as a function of gate-source voltage, $\mu_{AVG}(V_{GS})$ and $\mu_{INC}(V_{GS})$, are extracted. Assuming that $V_{DS} = 1$ V is small enough to apply Eq. 2.20 in Chapter 2.2.3, the average mobility is expressed as

$$\mu_{AVG}(V_{GS}) = \frac{G_{CH}(V_{GS})}{\frac{W}{L} C_{INS}[V_{GS} - V_{ON}]}, \tag{3.12}$$

where $G_{CH}(V_{GS}) = \frac{I_D(V_{GS})}{V_{DS}}$ is the channel conductance, C_{INS} is the insulator capacitance per unit area, which is ~34.5 nF / cm^2 for devices used in this study, and W and L are the channel width and length, respectively. An example of $\mu_{AVG}(V_{GS})$ is shown in Fig. 3.8. The incremental mobility, as discussed in Chapter 2.2.3, is evaluated as

$$\mu_{INC}(V_{GS}) = \frac{\frac{\partial G_{CH}(V_{GS})}{\partial V_{GS}}}{\frac{W}{L} C_{INS}}, \tag{3.13}$$

where the derivative $\frac{\partial G_{CH}(V_{GS})}{\partial V_{GS}}$ is estimated as $\frac{\Delta G_{CH}(V_{GS})}{\Delta V_{GS}}$, and where ΔG_{CH} corresponds to the change in channel conductance per measurement step ΔV_{GS}. An example of $\mu_{INC}(V_{GS})$ is shown in Fig. 3.8.

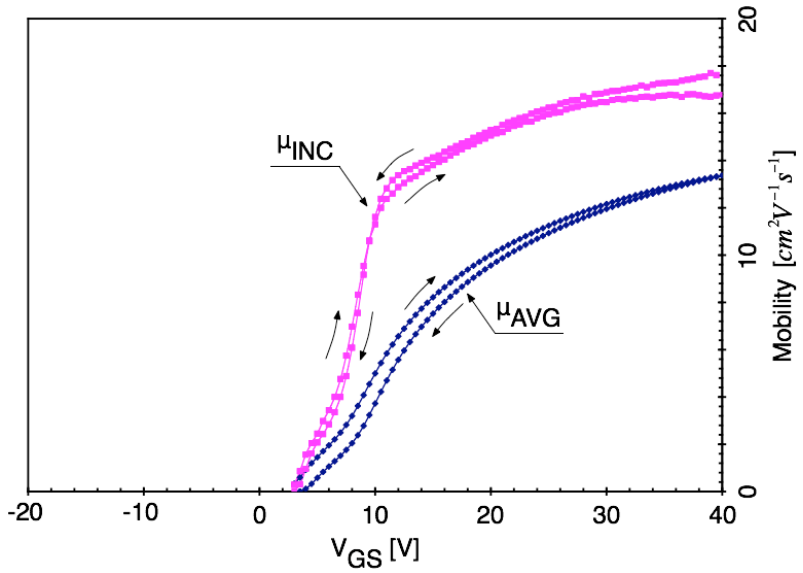


Figure 3.8: Average (μ_{AVG}) and incremental (μ_{INC}) mobilities extracted from a $\log_{10}(I_D)$-V_{GS} transfer curve measured at 50 °C and at V_{GS} = 1 V according to the procedure discussed in Subsection 3.3.4 for sample June202007 which is annealed at 300 °C. See Table 3.2 for more sample details.

For TFT temperature dependence assessment, two transfer curves and associated extraction of V_{ON}, S, I_D^{ON-OFF}, $\mu_{AVG}(V_{GS})$, $\mu_{INC}(V_{GS})$ are accomplished at each temperature step from -50 °C to 50 °C using a step of 20 °C.

3.3.5 Experimental Details

For the constant-voltage bias-stress testing, electrical measurements are accomplished using Agilent Technology semiconductor parameter analyzers, models SPC4155C or 4156C. The probe station used is a Micro Manipulator Co. Model 6000/6400 with Mode 110 micro-positioners and Kulicke and Soffa Manufacturing Company Model 200/201, with tungsten probes. The device under test (DUT) is maintained in the dark.

For tests which require temperature control, the TFT is placed inside a Sun Electric System EC-1A environmental chamber with all three terminals, i.e., the drain, gate, and source, connected to the semiconductor parameter analyzer (SPA), Agilent 4155C via tungsten probes.

For the accelerated recovery process, measurement commences approximately 10 minutes after the target temperature is reached, to allow for temperature stabilization. The temperature increase / decrease rate is regulated to two degrees per minute in order to minimize physical stress to the device. The heating process is carried out with an internal heater, while cooling is accomplished using liquid nitrogen, the flow of which is controlled by an internal computer. Unlike TFT post-deposition annealing, the cooling temperature slope is expected to be more accurate since an active system cooling is operative. The detailed temperature-time profile is depicted in Fig. 3.9.

For the temperature-dependence assessment, temperature control is initiated at the highest temperature in order to avoid condensation on the sample surface. Measurements at each step commence approximately 10 minutes after the target temperature is reached, in the same manner as for the accelerated recovery process. The temperature increase / decrease rate is also regulated to two degrees per minute. A detailed temperature-time profile is presented below in Fig. 3.10.

All equipments employed for testing are summarized in Table 3.4.

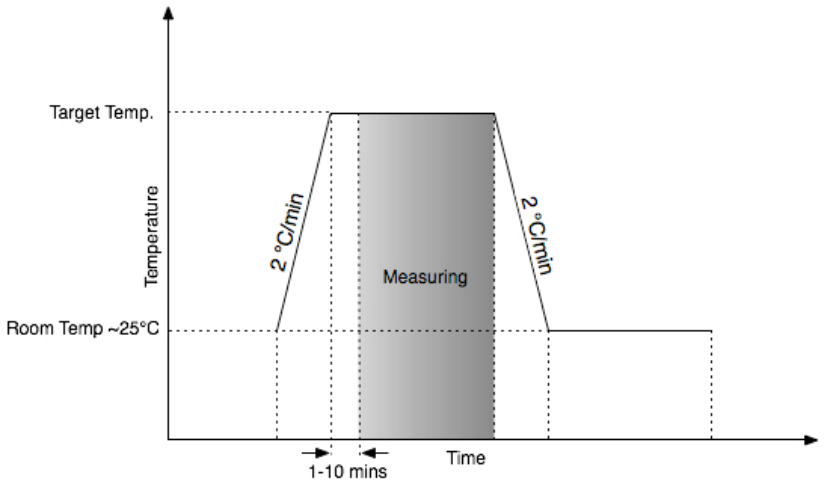


Figure 3.9: Temperature-time profile used for device resetting after the completion of a stability test. Electrical device testing at a given target temperature is performed approximately 1-10 minutes after the target temperature is reached.

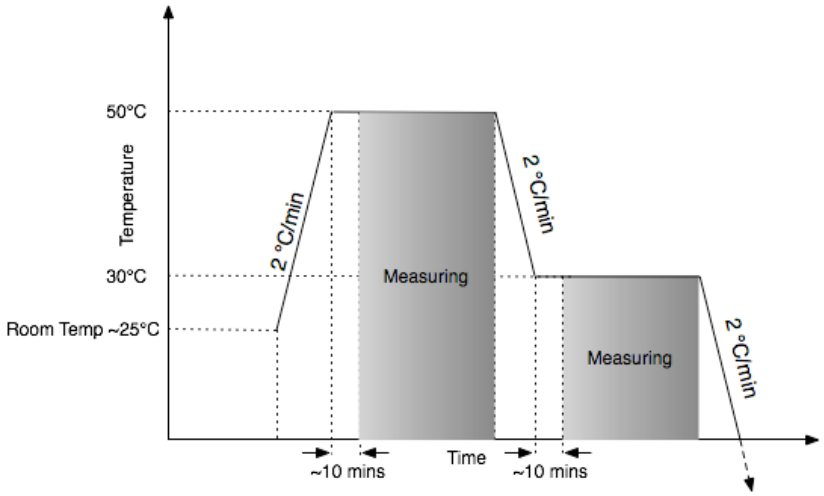


Figure 3.10: Temperature-time profile used for temperature dependence assessment. Electrical device testing at each temperature step is performed approximately 10 minutes after the target temperature is reached.

Make	Model Name	Category	Note
Sun Electric Systems	EC-1A	Environmental chamber	
Agilent Technology	SPC4155C	Semiconductor parameter analyzer	
Micro Manupulator Co.	Model 6000/6400	Probe station	
Kulicke and Soffa Manufacturing Company	Model 200/201	Micro positioner	Probe: tungsten
Agilent Technology	SPC 4146C	Semiconductor parameter analyzer	

Table 3.4: A summary of equipment used for TFT temperature-dependence assessment, constant-voltage bias stress testing, and the thermal resetting procedure.

4 STABILITY TESTING

In this chapter, several experiments related to TFT stability assessment are presented, including constant-voltage bias-stress testing and recovery tests. Constant-voltage bias-stress testing consists of two sets of measurements: (i) acquisition of transfer curves before and after stress testing and (ii) monitoring the drain current as a function of stress duration. Recovery testing includes: (i) a zero-bias room temperature recovery test in which no stress is applied to the device and (ii) a resetting test in which an elevated temperature and/or a voltage is applied to the TFT in order to aid its recovery.

In this chapter, only empirical results are presented. A discussion of stability mechanisms is deferred until Chapter 6.

4.1 Constant-Voltage Bias-Stress Testing

Constant-voltage bias-stress testing starts with measuring two $\log_{10}(I_D) - V_{GS}$ transfer curves – one with V_{DS} = 1 V and the other with V_{DS} = 30 V. Average mobility and incremental mobility are extracted from the former transfer curve and parameters such as turn-on voltage, V_{ON}, subthreshold swing, S, and drain current hysteresis, H_{I_D}, are acquired from the latter one. Each transfer curve is double-swept, i.e. applied V_{GS} increases from -20 V to 40 V then decreases back to -20 V without a pause in order to evaluate hysteresis.

After these pre-stress transfer curves are acquired, degradation of the drain current is observed over a period of 10^5 s under one of the following sets of constant voltage:

1. $V_{GS} = V_{DS} = 10$ V,
2. $V_{GS} = V_{DS} = 20$ V, or
3. $V_{GS} = V_{DS} = 30$ V.

The recorded drain current data is plotted as a function of stress time on a logarithmic time scale. A characteristic result is shown in Fig. 4.1, and exhibits a smooth continuous decrease in drain current, which is typical of most of the devices tested. In contrast, 5 samples out of the 32 tested are found to be noisy, for reasons which are not entirely clear. These noisy data sets will not be further considered.

The constant-voltage bias-stress measurement is completed with the acquisition of post-stress transfer curves and corresponding parameter extraction, which are identical in nature to the pre-stress transfer curves described previously. Transfer curves measured at $V_{DS} = 30$ V before and after constant-voltage bias stressing are plotted on the same figure in order to clarify the direction of the V_{ON} shift, as shown in Fig. 4.2. All the devices tested exhibit a positive V_{ON} shift. Fig. 4.2 also shows clockwise (CW) hysteresis, which is indicated by small arrows along the curves. CW hysteresis is consistently observed for all the TFTs tested.

The normalized decrease of the drain current due to constant-voltage bias-stress testing is calculated from the initial and final drain current points, according to $\frac{I_D(10^5 s) - I_D(0s)}{I_D(0s)} \times 100$. Then, this value is averaged over all the samples tested and

plotted as a function of annealing temperature, as shown in Fig. 4.3. As seen in this figure, TFTs exhibit less current degradation as the post-deposition annealing temperature increases. Invariably, TFTs with the best stability were annealed at 300 °C, the highest channel annealing temperature employed in this study.

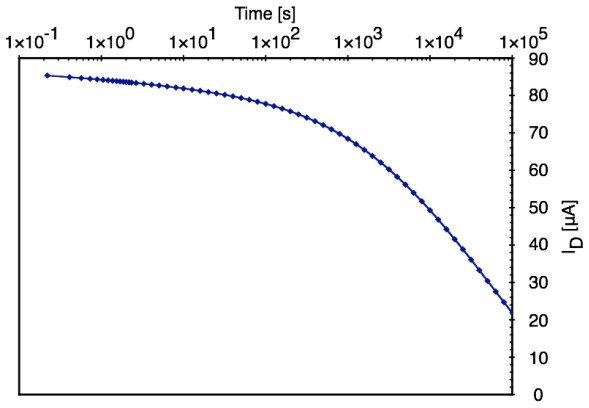


Figure 4.1: Drain current as a function of stress time on a logarithmic time scale over a period of 10^5 s for a constant voltage-bias stress-test experiment. The sample used is 061202 A350-5. The measurement is performed using an Agilent Technology semiconductor parameter analyzer under the following measurement conditions; the initial time interval is 10 ms, the number of sampling points is 10 points per decade, and the integration time is 16.7 ms.

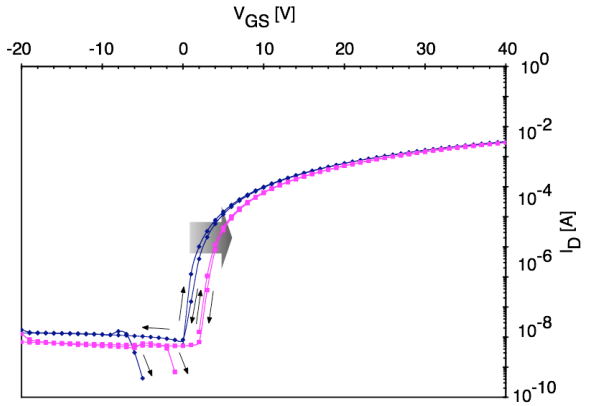


Figure 4.2: $Log_{10}(I_D) - V_{GS}$ transfer curves before and after constant-voltage bias-stress testing over a period of 10^5 s. The TFT employed is 061206 B175-1, which shows a positive rigid shift. The small arrows indicate the nature of hysteresis – clockwise (CW) in this case, while the large arrow specifies the direction of stress-induced change in the transfer curves. The measurement is performed using a semiconductor parameter analyzer 4155C or 4156C from Agilent Technology with integration time of 16.7 ms.

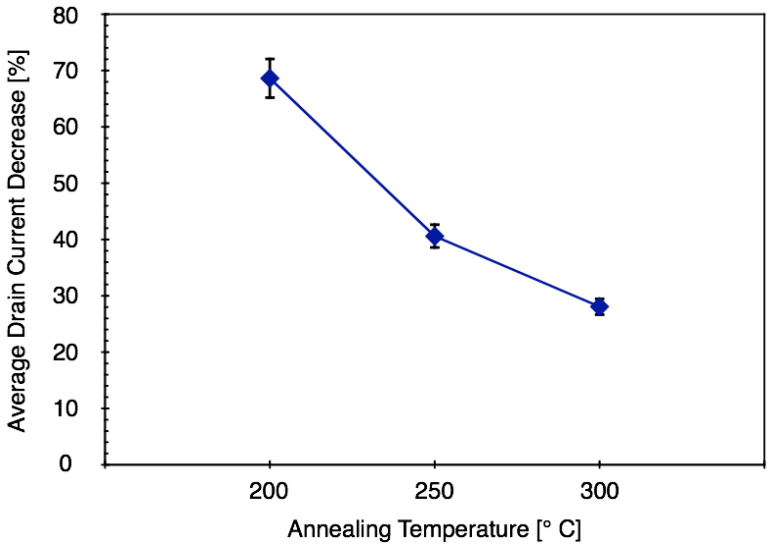
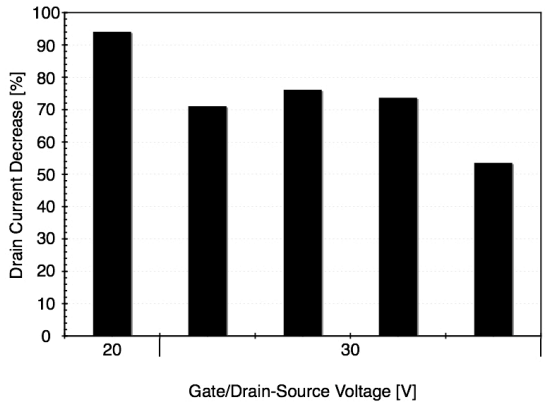
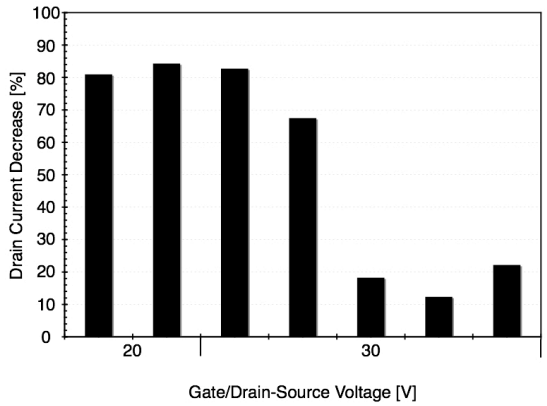


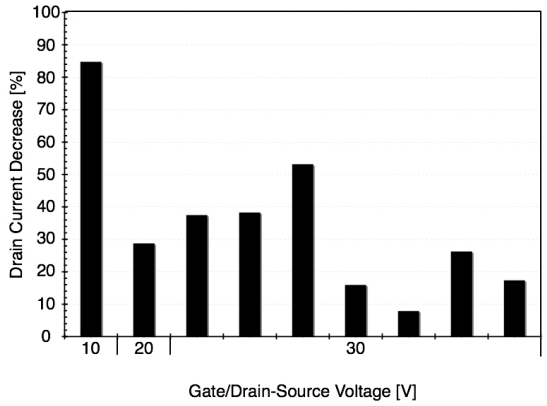
Figure 4.3: Drain current decrease, i.e. $\frac{I_D(10^5 s) - I_D(0s)}{I_D(0s)} \times 100$ associated with constant-voltage bias-stress testing as a function of post-deposition annealing temperature. Error bars are for a ±5 % fluctuation. This drain current decrease is an average over all of devices tested at a constant bias of $V_{GS} = V_{DS} = 30$ V (4 samples from June202007 1 for 200 °C, 5 samples from June202007 2 and July132007 2 for 250 °C, and 7 samples from June202007 3 and July132007 1 for 300 °C). Devices are selected so that all fabrication conditions are identical, except for the annealing temperature.



(a)



(b)



(c)

Figure 4.4: Drain current decrease, i.e. $\frac{I_D(10^5 s) - I_D(0s)}{I_D(0s)} \times 100$ associated with constant-voltage bias-stress testing as a function of gate/drain-source bias-stress voltages for samples annealed at (a) 200 °C, (b) 250 °C, and (c) 300 °C. Notice that a higher gate/drain-source voltage tends to result in less severe current degradation.

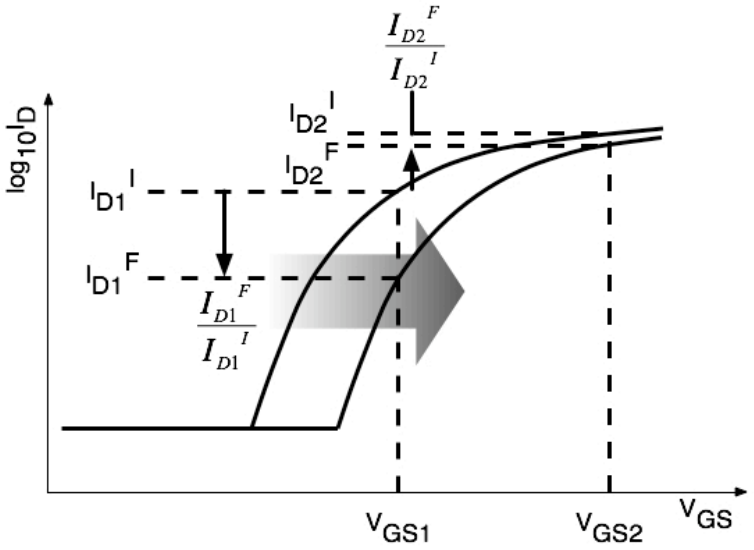


Figure 4.5: Transfer curves before and after constant-voltage bias-stress testing show that the drain current decay, i.e. $\frac{I_D{}^{I} - I_D{}^{F}}{I_D{}^{I}} \times 100$, tends to be larger at a smaller gate-source voltage.

Another noteworthy aspect of the drain current decrease during constant-voltage bias-stress testing is shown in Fig. 4.4, in which the amount of drain current decrease is presented as a function of the magnitude of the gate/drain-source voltage. Two main trends are evident from an assessment of Fig. 4.4. First, it is clear by comparing Fig. 4.4 (a), (b), and (c) which are associated with post-deposition channel annealing temperatures of 200, 250, and 300 °C, respectively, that the drain current degradation is less severe at a higher post-deposition annealing temperature. Second, for the TFTs at a constant post-deposition annealing temperature, TFTs tend to exhibit less drain current degradation when the gate/drain-source voltages are larger.

Since V_{GS} = V_{DS} for all the TFTs employed for Fig. 4.4, it is desirable to determine which terminal voltage is dominant in determing TFT stability. To investigate this question, two identical TFTs fabricated on the same die and next to each other are chosen and tested with different V_{GS} and V_{DS}; one with V_{GS} = 20 V and

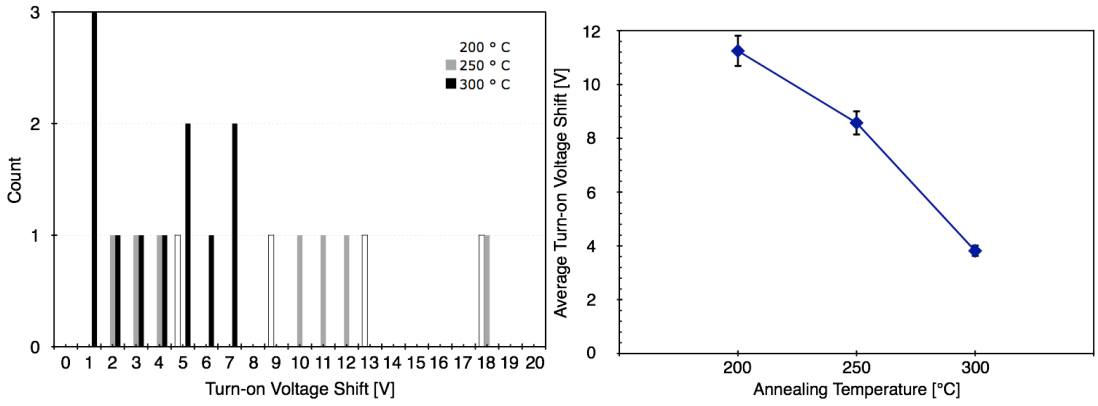
V_{DS} = 30 V (sample number: July132007 1-6-2) and the other one with V_{GS} = 30 V and V_{DS} = 10 V (sample number: July132007 1-6-3). Although both devices have almost identical electrical characteristics otherwise, the TFT biased at V_{GS} = 20 V exhibited 10 % more drain current decrease, suggesting that the gate voltage is the dominant factor in establishing drain current decrease. Refer to the Appendix for more details.

Fig. 4.5 may help to explain this trend in which less drain current degradation occurs at a larger gate/drain-source voltage. Expressing the drain current decrease as

$$\frac{I_D{}^I - I_D{}^F}{I_D{}^I} \times 100 = \left(1 - \frac{I_D{}^F}{I_D{}^I}\right) \times 100, \tag{4.1}$$

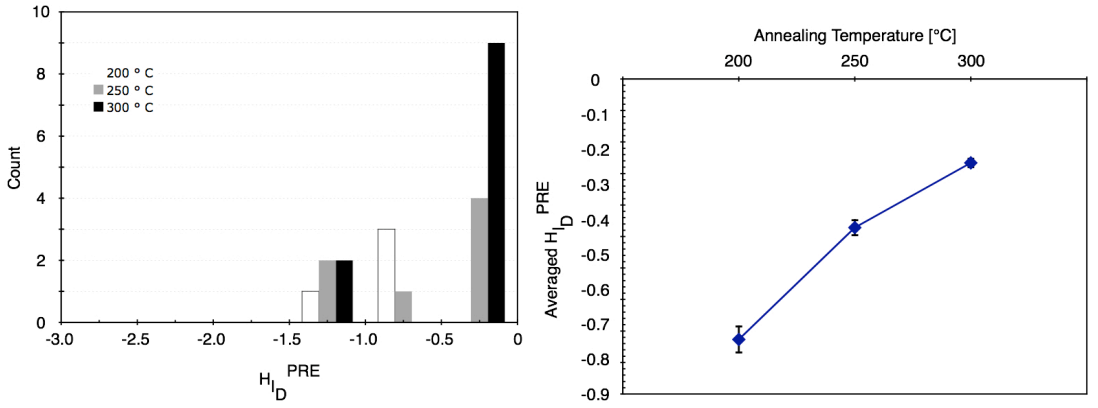
where $I_D{}^I$ is the drain current before stressing and $I_D{}^F$ is the drain current after stressing. Fig. 4.5 shows a rigid shift in the transfer curve to a more positive V_{ON} after constant-voltage bias-stress testing. This trend is typical of most of the IGZO-based TFTs tested. As evident from an assessment of Fig. 4.5, the drain current difference is larger when V_{GS} is small (V_{GS1}) and smaller when V_{GS} is larger (V_{GS2}).

As evident from an assessment of Figs. 4.6 - 4.9, there is a clear post-deposition annealing temperature dependence established for the turn-on voltage shift, drain current hysteresis, H_{I_D}, in the pre- and post-stressed states, and the drain current difference, ΔH_{I_D}.



(a) (b)

Figure 4.6: Effect of post-deposition annealing temperature on the turn-on voltage shift from the pre-stressed state to the post-stressed state. (a) Turn-on voltage shift distribution for various annealing temperatures. Devices exhibiting a turn-on voltage shift larger than 8 V are annealed at ≤ 250 °C. (b) Average turn-on voltage shift as a function of annealing temperature. Error bars are for a ±5 % fluctuation. The turn-on voltage shift decreases with increasing annealing temperature.



(a) (b)

Figure 4.7: Effect of post-deposition channel annealing temperature on drain current hysteresis in the pre-stressed state, $H_{I_D}{}^{PRE}$. (a) The H_{I_D} distribution of TFTs annealed at different temperatures. (b) H_{I_D} averaged over devices annealed at the same temperature is plotted as a function of annealing temperature. Error bars are for a ±5 % fluctuation. Both figures indicate that devices subjected to a higher annealing temperature tends to exhibit narrower hysteresis in the pre-stressed state.

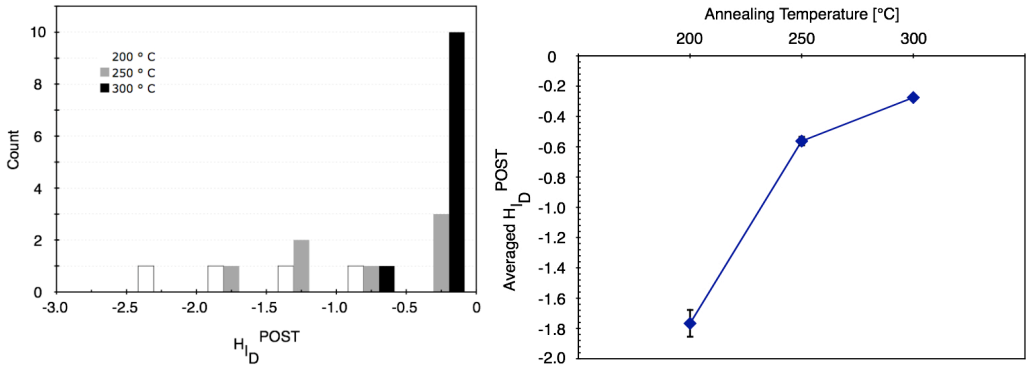
First, consider Fig. 4.6 (a) in which the distribution in the turn-on voltage shift after constant-voltage bias-stress testing is plotted as a function of turn-on voltage shift and post-deposition channel annealing temperature. All of the TFTs that exhibit a turn-on voltage shift larger than 8 V are post-deposition annealed at either 200 or

250 °C. The average turn-on voltage shift shown in Fig. 4.6 (b) clearly indicates that turn-on voltage stabilization is more effective at a higher post-deposition annealing temperature, at least up to 300 °C, the highest temperature employed for this particular purpose.

Fig. 4.7 illustrates the effect of post-deposition channel annealing temperature on H_{I_D} of pre-stressed TFTs. Hysteresis is always clockwise (CW) for all of the IGZO TFTs tested. Recall that the negative polarity of H_{I_D} identifies the hysteresis as clockwise. Thus, the H_{I_D} magnitude is of particular interest, with a smaller magnitude corresponding to a more stable TFT. The H_{I_D} distribution plot of Fig. 4.7 (a) reveals the general trend that less hysteresis tends to occur at a higher annealing temperature. This post-deposition channel annealing temperature trend is even more evident in Fig. 4.7 (b) which shows that the hysteresis magnitude monotonically decreases with increasing annealing temperature over the temperature regime explored. Note that Fig. 4.8 exhibits identical post-deposition channel annealing trends of drain current hysteresis for post-stressed TFTs as Fig. 4.7 does for pre-stressed TFTs.

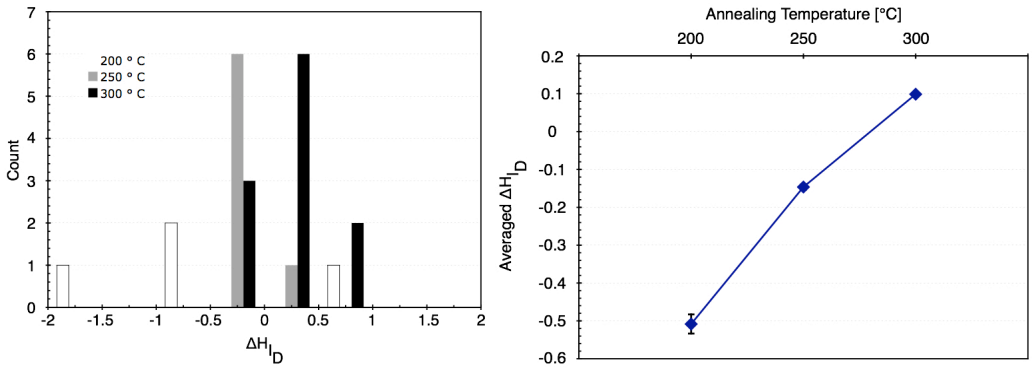
As shown in Fig. 4.9 (a), all of the TFTs annealed at 300 °C except for three exhibit a positive ΔH_{I_D}, corresponding to less hysteresis after stressing. Additionally, two of these three exceptions are so small that they can be considered to be within the range of experimental error. Figure 4.9 (b) indicates that there is a clear trend in which TFTs annealed at a higher temperature exhibit less ΔH_{I_D}. Notice from Fig. 4.9

(b) that the average TFT channel layer annealed at 300 °C exhibits less H_{I_D} after the constant-voltage bias-stress since ΔH_{I_D} is larger than 0.



(a) (b)

Figure 4.8: Effect of post-deposition annealing temperature on drain current hysteresis in the post-stressed state, $H_{I_D}{}^{POST}$. (a) The H_{I_D} distribution of TFTs annealed at different temperatures. (b) H_{I_D} averaged over devices annealed at the same temperature is plotted as a function of annealing temperature. Error bars are for a ±5 % fluctuation. Both figures indicate that devAces subjected to a higher annealing temperature tends to exhibit narrower hysteresis in the post-stressed state.



(a) (b)

Figure 4.9: Effect of post-deposition channel annealing temperature on the drain current hysteresis difference, ΔH_{I_D}. (a) ΔH_{I_D} distribution of samples annealed at different temperatures. (b) ΔH_{I_D} averaged over the devices annealed at the same temperature is plotted as a function of annealing temperature. Error bars show ±5 % of possible fluctuation. Notice in (a) that most of the TFTs annealed at 300 ° C exhibiting a positive ΔH_{I_D}, corresponding to narrower hysteresis after stressing. A clear trend that TFTs annealed at a higher temperature tend to show narrower hysteresis after the stress is noticeable in (b).

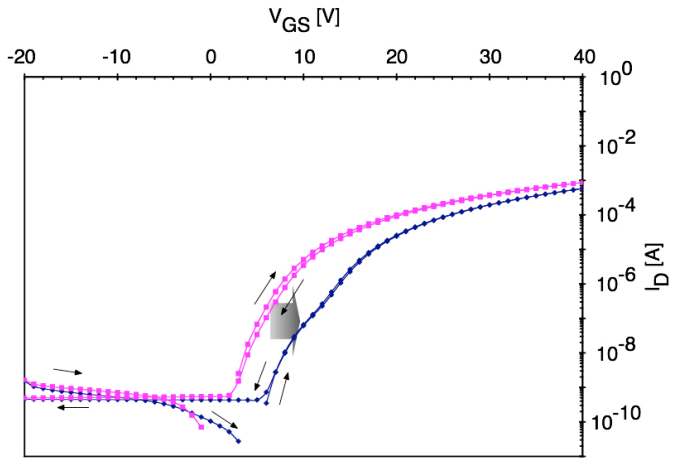


Figure 4.10: $Log_{10}(I_D) - V_{GS}$ transfer curves before and after constant-voltage bias-stress testing over a period of 10^5 s, which exhibits a kink in the subthreshold region after stressing. The small arrows indicate the nature of hysteresis – clockwise (CW) in this case, while the large arrows specify the direction of stress-induced change in the transfer curves. The measurement is performed using a semiconductor parameter analyzer 4155C or 4156C from Agilent Technology with integration time of 16.7 ms.

Most of the IGZO-based TFTs tested show a positive rigid shift of the transfer curve after the constant-voltage bias-stress test, as exemplified by Fig. 4.2. However, 4 TFTs out of 32 exhibit a kink in the subthreshold portion of the transfer curve after stressing, as presented in Fig. 4.10, and all of them are annealed at 300 °C. A kink is never found to be present in the transfer curve of an unstressed IGZO TFT. Rather, a kink appears only as a consequence of constant-voltage bias-stressing in a few of the TFTs tested. Wager *et al*. propose a possible mechanism for the kink, involving a high-density acceptor-like traps close to the conduction band edge [79]. Since the kink is not visible before stressing, it appears, according to this model, that acceptor-like traps are created as a consequence of bias stressing.

4.2 Recovery Tests

Two types of recovery test are performed. The first one is a no-bias room temperature recovery measurement in which no stress is applied to the device during

the recovery period. The second one is an accelerated recovery test in which an increase in temperature and/or applied voltages are employed in an attempt to accelerate the rate of recovery of the TFT back to its initial, pre-stressed state.

4.2.1 No-Bias Room Temperature Recovery

As pointed out by Brown *et al.* for solution-based organic TFTs [81], some bias-stress-induced aging is naturally recoverable, i.e., recovery occurs by simply leaving the TFT unstressed for an extended period of time. This is referred to herein as no-bias room temperature recovery.

Selected IGZO TFTs, all of which had been subjected to the constant-voltage bias-stress test as discussed in Subsection 4.1, are placed in the dark for an extended period of time without applying any stress or temperature control. Transfer curves for these TFTs are observed after various periods of recovery time, which ranges from 7 to 63 days, and are compared to pre-stressed and post-stressed transfer curves. Each set of transfer curves are plotted using a $\log_{10}(I_D) - V_{GS}$ format, as shown in Fig. 4.11, from which performance parameters such as V_{ON}, S, and H_{I_D} are extracted. These parameters in the post-recovery state are compared to those in the pre-stressed and post-stressed states to assess the degree of recovery from the post-stressed state and to the pre-stressed state.

Since each parameter has a device dependency, that is, samples exhibit different values from sample-to-sample in the initial, post-stress, and post-recovery state, minimizing the sample dependence is required in order to compare the degree of post-stress recovery between samples. All of the post-stress recovery parameters, which

involve V_{ON}, S, and H_{I_D} are redefined as differences in which the post-stressed state is subtracted from the post-recovery state.

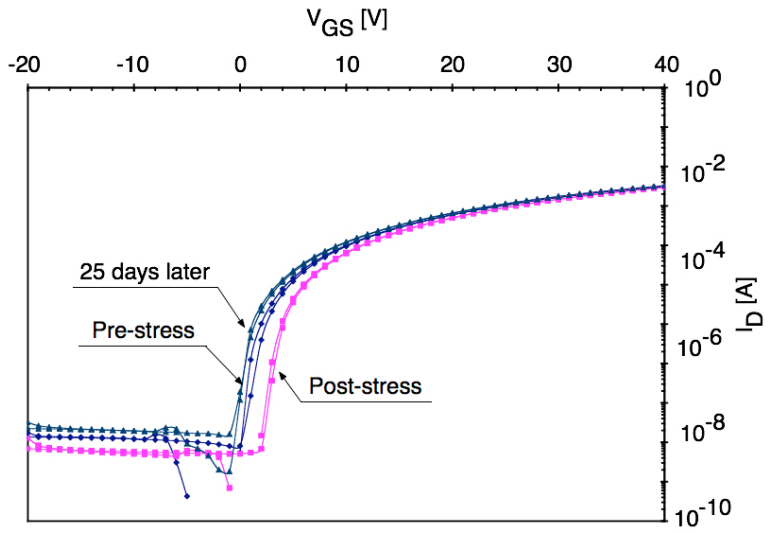


Figure 4.11: $I_D - V_{GS}$ transfer curves for pre-stress, post-stress, and 25 days after bias-stress testing are shown plotted on a logarithmic scale. The sample is 061206 B175-1, which is reused after the test shown in Figure 4.1. Detailed information for this sample is provided in Table 3.2.

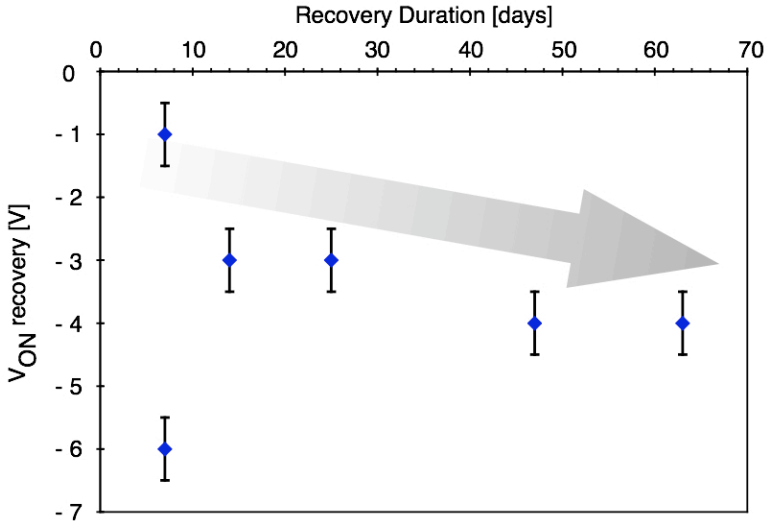


Figure 4.12: Post-stress recovery of the turn-on voltage. V_{ON} recovery = V_{ON} post-recovery – V_{ON} post-stress. Notice that if the TFT with -6 V of V_{ON} recovery is neglected, there is a trend in which the amount of V_{ON} recovery becomes larger when the recovery duration is extended. Error bars are for a ±0.5 V fluctuation due to the resolution employed in this measurement.

A recovery parameter of particular importance is V_{ON} which is plotted as a function of recovery time, as shown in Fig. 4.12. Notice that the sign of V_{ON} recovery is negative, which means V_{ON} moves toward the pre-stress value since all the samples exposed to constant-voltage bias-stress testing show a positive V_{ON} shift. As seen in this figure, V_{ON} recovers more as the recovery duration is extended except for the anomalous result of a TFT with V_{ON} recovery of -6 V at the recovery duration of 7 days. TFTs tested also show evidence of recovery in terms of S and H_{I_D} although these data are not shown in figure because the recovery time dependence was not established. Numerical recovery data for all three of these parameters are provided in the Appendix.

Pre-stress recovery parameters for V_{ON}, S, and H_{I_D} are obtained by subtracting a pre-stress value from a post-recovery value in order to evaluate the degree of the TFT recovery toward the pre-stressed state. Distributions of the degree of recovery in terms of these parameters are shown in Fig. 4.13. Since the pre-stress recovery parameter values become 0 when the post-recovery and pre-stress values are identical, the shape of distribution is expected to be symmetric across the origin if TFTs recover completely. Thus, the symmetric shape of the V_{ON} pre-stress recovery distribution shown in Fig. 4.13 (a) suggests that TFTs exhibit rather good room temperature recovery. However, the asymmetrical shapes of the S and H_{I_D} pre-stress recovery distributions indicated in Fig. 4.13 (a) and (b), respectively, reveal that these devices do not appear to fully recover.

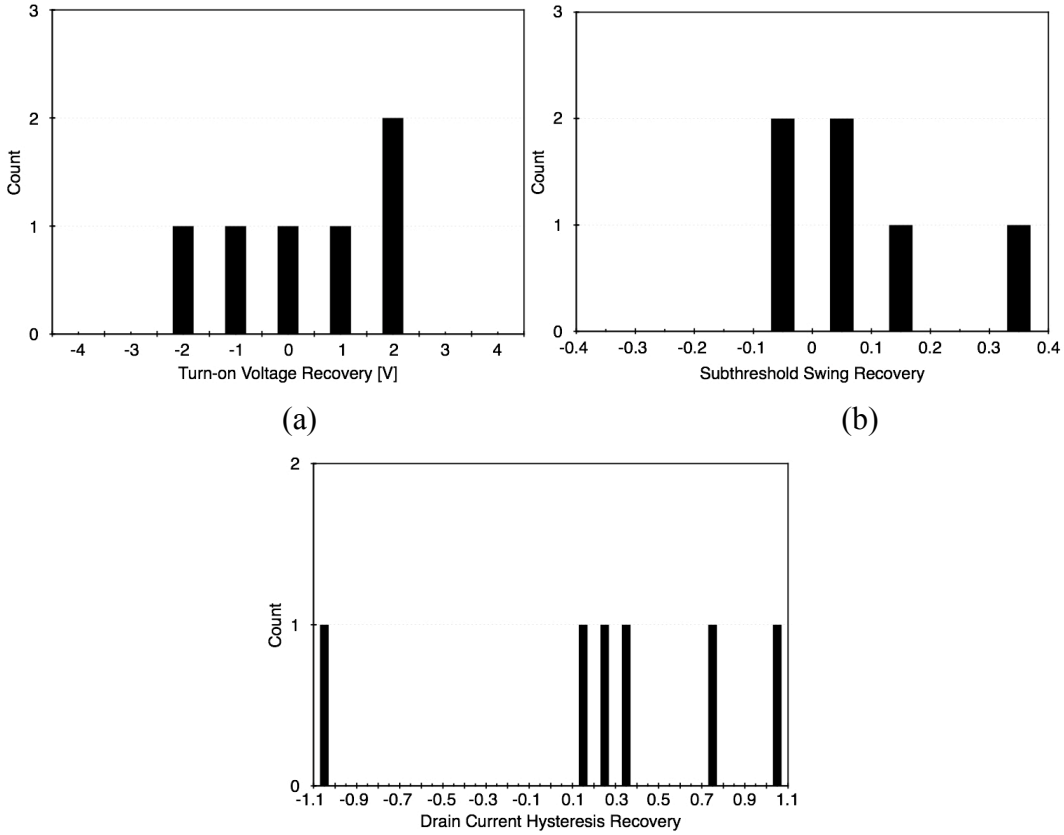


Figure 4.13: Distribution of pre-stress recovery with regard to (a) turn-on voltage, (b) subthreshold swing, and (c) drain current hysteresis. These pre-stress recovery parameters are defined as being equal to the post-recovery value minus the pre-stressed value. As seen from (b) and (c), TFTs do not fully recover from the post-stressed state since the distribution is uneven across 0, although they do appear to recover when only the turn-on voltage is observed, as shown in (a).

Considering all the results presented in this subsection, IGZO-based TFTs appear to have an ability to recover from the post-stressed state toward the pre-stressed state to some extent via no-bias room temperature recovery, although they also do not completely recover to the pre-stressed state even after two months.

4.2.2 Accelerated Recovery Testing

Since most of the stressed devices do not recover completely on their own as a consequence of no-bias room temperature recovery, as studied in Subsection 4.2.1, procedures for accelerated recovery are desirable.

The accelerated recovery procedure investigated in this subsection involves concurrent electrical and thermal stressing, while no stress is applied in no-bias room temperature recovery. An accelerated recovery experiment is accomplished as follows. (i) Perform a constant-voltage bias-stress test. (ii) Perform an accelerated recovery test. (iii) Perform a second constant-voltage bias-stress test. $Log_{10}(I_D) - V_{GS}$ transfer curves are measured for (a) before 1st stress, (b) after 1st stress, (c) before 2nd stress (post-recovery), and (d) after 2nd stress. Parameters such as V_{ON}, S, and H_{I_D} are extracted and compared for different stress conditions. Finally, I_D is monitored during each constant-voltage bias-stress test and is plotted on a semi-log scale. Numerical values of all extracted parameters are presented in Table 8.8 to Table 8.11.

<table>
<tr><th rowspan="2">Number</th><th colspan="3">Electrical stress [V]</th><th rowspan="2">Thermal stress [ºC]</th></tr>
<tr><th>V_G</th><th>V_S</th><th>V_D</th></tr>
<tr><td>1</td><td>0 V (grounded)</td><td>0 V (grounded)</td><td>0 V (grounded)</td><td rowspan="2">50</td></tr>
<tr><td>2</td><td>No stress (open)</td><td>No stress (open)</td><td>No stress (open)</td></tr>
<tr><td>3</td><td rowspan="3">0 V (grounded)</td><td rowspan="3">0 V (grounded)</td><td rowspan="3">0 V (grounded)</td><td>75</td></tr>
<tr><td>4</td><td rowspan="2">100</td></tr>
<tr><td>5</td><td>-10 V</td></tr>
<tr><td>6</td><td>No stress (open)</td><td>No stress (open)</td><td>No stress (open)</td><td>150</td></tr>
</table>

Table 4.1: Testing conditions employed for accelerated recovery testing. More detailed testing condition and TFT information are provided in Table 8.7 of the Appendix.

Fig. 4.14 displays $\log_{10}(I_D)$ – V_{GS} transfer curves corresponding to an accelerated recovery test for a TFT which exhibits excellent recovery. Constant-voltage bias-stress testing, for both the 1st and 2nd stresses, results in a nearly rigid displacement of the transfer curve to the right by 3 V from and initial V_{ON} of -1 V. Accelerated recovery for this device is almost ideal, as evident from the fact that pre-stress transfer curves almost lie on top of one another. Note that accelerated recovery is accomplished in what appears to be an optimal manner, i.e. all terminals are grounded while the TFT is subjected to an elevated temperature of 50 °C, in this case.

In contrast, the accelerated recovery test results shown in Fig. 4.15 illustrate a situation in which recovery was very unsuccessful. Notice that the 1st constant-voltage bias-stress measurement resulted in a nearly rigid shift in the transfer curve to the right by 4 V. This result is nearly identical to that presented for the ideal recovery case of Fig. 4.14.

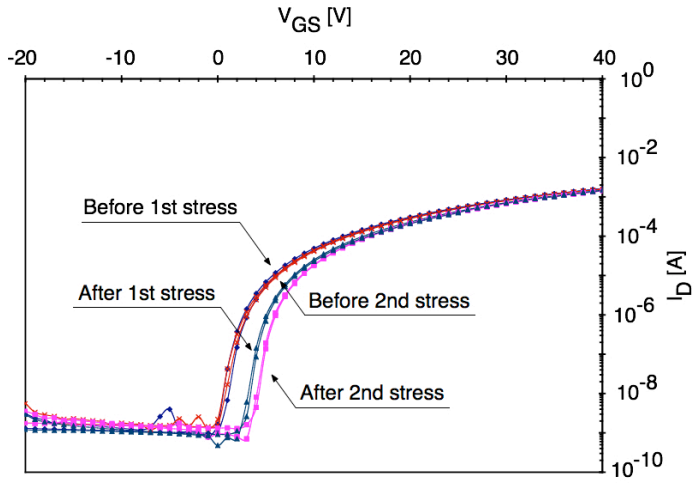


Figure 4.14: Drain current characteristics as a function of V_{GS} and time. $\text{Log}_{10}(I_D)$ – V_{GS} transfer curves before and after the 1st and 2nd constant-voltage bias-stress tests are shown. The TFT employed is 061206 B250-5. Accelerated recovery for this TFT is performed with all terminals grounded at a temperature of 50 °C. Detailed information for this TFT is provided in Table 3.2.

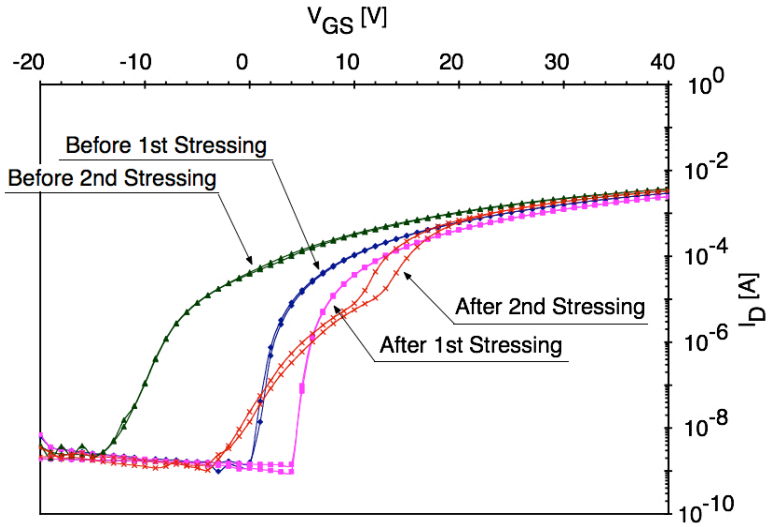


Figure 4.15: $Log_{10}(I_D)) - V_{GS}$ transfer curves before and after the 1st and 2nd constant-voltage bias-stress tests. The TFT employed is July132007 2-3-3. The stress applied in the constant-voltage bias-stress testing is $V_{DS} = V_{GS} = 30$ V. Accelerated recovery for this device is performed with the source and drain terminals grounded and the gate at -10 V using a temperature of 100 °C. Detailed information for this TFT is provided in Table 8.7.

The 'before 2nd stress' curve given in Fig. 4.15 is non-ideal in two ways. First, the turn-on voltage is strongly negative, $V_{ON} = -14$ V. This means that the TFT is depletion-mode, with a high concentration of electrons in the channel even in the absence of an applied gate voltage. Second, the subthreshold swing is degraded considerably from what it was prior to undergoing accelerated 'recovery,' i.e. S = 1.75 V/decade after 'recovery' and S = 0.69 V/decade prior to stressing. This degradation in S is attributed to the creation of interface traps [20]. Note that this extremely poor recovery is attributed to the use of an applied gate voltage of -10 V during accelerated recovery. In general, use of a negative, positive, or zero gate bias during elevated temperature recovery results in a V_{ON} shift towards negative, positive, or zero volts, respectively, as explained later in this subsection.

Returning once more to Fig. 4.15, the 'after 2nd stressing' transfer curve is extremely non-ideal. Compared to the post-recovery 'before 2nd stressing' curve, V_{ON} moves to the right under constant-voltage bias-stress testing, from V_{ON} = -14 V to -4 V. However, a positive voltage shift is the normal situation, although the magnitude of this shift for the TFT shown in Fig. 4.15 is quite large. A more significant trend is the formation of a kink after the 2nd constant-voltage bias-stress test. This kink is ascribed to a high-density acceptor-like discrete trap creation close to the conduction band edge, as discussed in Subsection 4.1. It is possible that these two types of created traps – one giving rise to the kink after the 2nd constant-voltage bias stress and the other associated with the subthreshold swing degradation after the accelerated recovery process – are associated with the same acceptor-like interface states. Finally, note that the 'after 2nd stressing' curve possesses an even more degraded subthreshold swing and more hysteresis than any of the other curves included in Fig. 4.15.

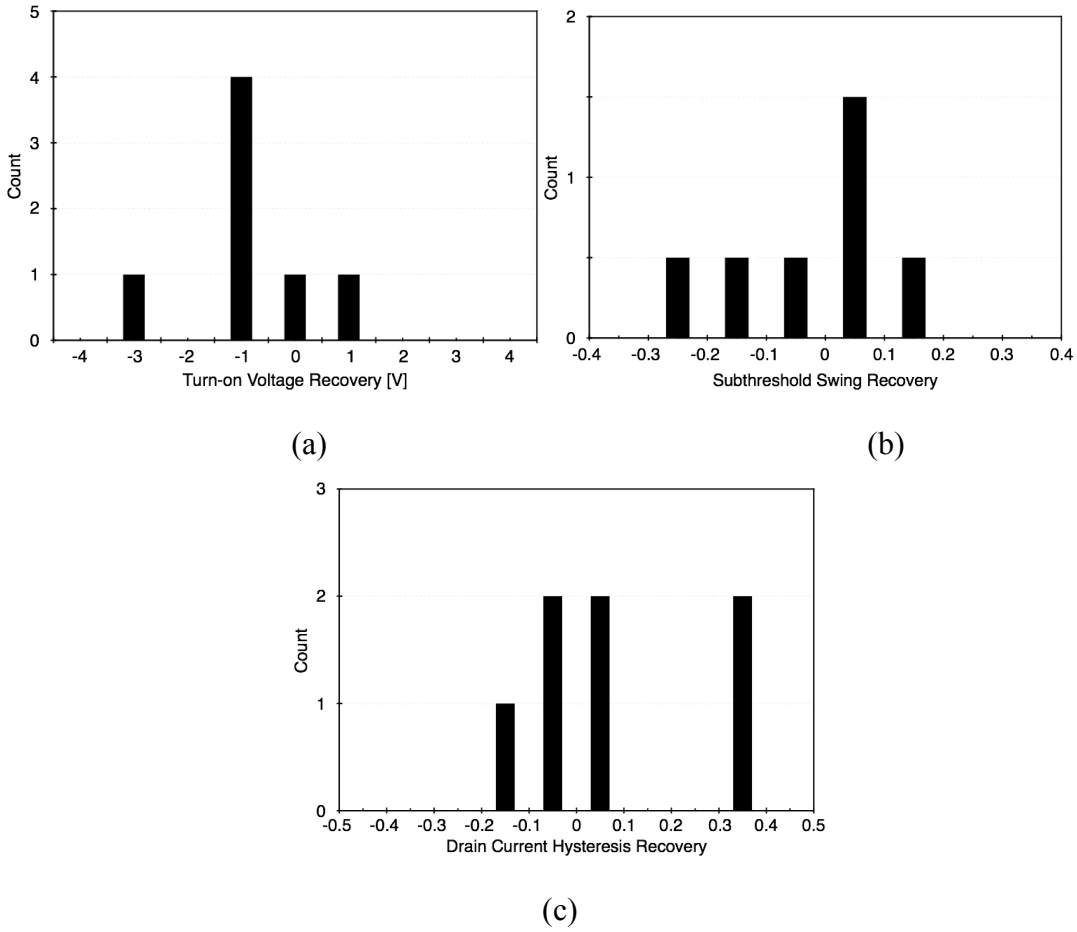


Figure 4.16: Distribution of the performance recovery to the pre-stressed state with regard to (a) turn-on voltage, (b) subthreshold swing, and (c) drain current hysteresis. The values are acquired as the post-recovery value minus the pre-stressed value. As seen in these figure, TFTs do not fully recover from the post-stressed state since the distribution is uneven across the origin. Accelerated recovery is accomplished at an elevated temperature with all terminals grounded.

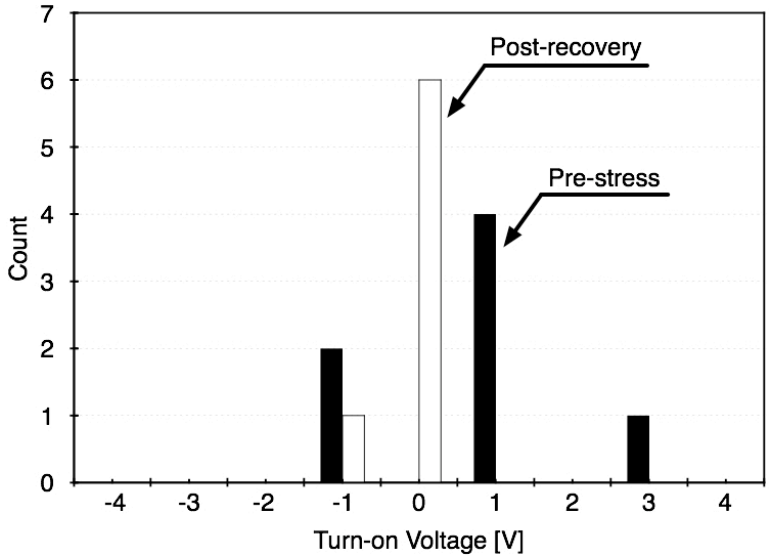


Figure 4.17: Distribution of IGZO-based TFTs with all terminals grounded with respect to the turn-on voltage. Black bars represent the turn-on voltage in the pre-stressed state and white ones represent that in the post-recovery state. Notice that devices distribute more close to 0 in the post-recovery state than in the pre-stressed state.

V_{ON}, S, and H_{I_D} after accelerated recovery are acquired and subtracted from their corresponding values in the pre-stressed state in order to evaluate the degree of TFT recovery toward the pre-stressed state. Distributions of the degree of recovery in terms of these parameters are shown in Fig. 4.16. V_{ON}, S, and H_{I_D} recovery values all cluster around zero but display asymmetrical distributions, suggesting that TFTs do not fully recover, even when an optional accelerated recovery procedure (i.e., all terminals grounded at an enhanced temperatures) is employed.

Fig. 4.17 shows an interesting comparison of distributions of V_{ON}'s for virgin (pre-stressed) TFTs compared to TFTs undergoing optimal accelerated recovery in which all terminals are grounded at an elevated temperature. Notice that the vast majority of TFTs recover to zero volts when the gate voltage is grounded. This observation is part of a more general trend in which V_{ON} after accelerated recovery

tends towards negative, positive, or zero bias if the applied gate bias during recovery is negative, positive, or zero, respectively. As seen in this figure, the turn-on voltage in the post-recovery state appears to become closer to 0 V than in the pre-stressed state for the TFTs with all the terminals, gate, drain, and source, grounded. The mechanism of this turn-on voltage shift is discussed in Chapter 6.

5 TFT TEMPERATURE-DEPENDENCE ASSESSMENT AND OFF CURRENT ANOMALY

This chapter focuses on empirical results related to the temperature-dependence of IGZO channel layer TFT electrical characteristics. Physical mechanisms responsible for IGZO TFT temperature dependent phenomena are discussed in Chapter 6.

5.1 Temperature-Dependence Assessment

In the temperature-dependence assessment procedure, two $\log_{10}(I_D)$ – V_{GS} transfer characteristics are measured, one at V_{DS} = 1 V, the other at V_{DS} = 20 or 30 V, at each temperature, i.e. -50, -30, -10, 10, 30, and 50 °C. Two sweeps are performed: a positive sweep, from -20 V to 40 V, followed by a negative sweep, from 40 V to -20 V. Positive and negative sweeps are obtained one after the other, without a pause between curves.

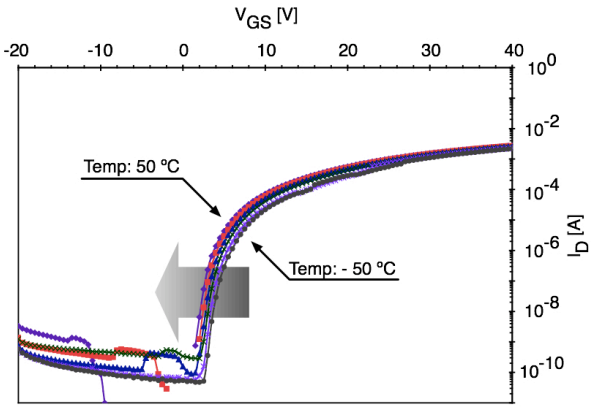


Figure 5.1: Superimposed positive sweeps of $\log_{10}(I_D)$ – V_{GS} transfer curves as a function of temperature at -50, -30, -10, 10, 30, and 50 °C. The arrow shows the direction of transfer curve displacement as temperature increases. Notice that an abrupt drain current decrease is observed near zero volts only at a temperature of 30 and 50 °C. The TFT employed is June202007 1-6-1.

Temperature dependence measurement details are as follows. A V_{GS} step size of 0.5 V or 1 V is used. I_D is acquired by integrating and averaging over a period of 16.7 ms at each step. The temperature dependence measurement starts at 50 °C and decreases to -50 °C in 20 °C steps in order to minimize measurement errors associated with condensation built up on the device. A 10-minute hold time at each temperature is used to ensure that a steady state is achieved before the measurement. From transfer curves measured at V_{DS} = 1 V, average and incremental mobilities are extracted, following the method explained in Section 3.3.4. Various parameters such as turn-on voltage, V_{ON}, subthreshold swing, S, and drain current on-to-off ratio, I_D^{ON-OFF}, are extracted from the transfer curves measured at V_{DS} = 20 / 30 V. Techniques for extracting these parameters are discussed in Subsection 3.3.1. Acquired parameters are plotted as a function of temperature in order to establish temperature-dependence trends. Details of the measurement are provided in Subsection 3.3.4.

Figure 5.1 shows positive sweep $\log_{10}(I_D)$ – V_{GS} transfer curves at each temperature, i.e., -50, -30, -10, 10, 30, and 50 °C, superimposed on one another. As clearly seen in this figure, transfer curves shift rather rigidly to the left towards more negative V_{GS}'s as the temperature increases. Also notice that there is an abrupt decrease in the drain current around V_{GS} = 0 V for the 30 and 50 °C curves, which are the highest temperatures of this study. This anomalous decrease in the drain current is more obvious at 50 °C than at 30 °C, indicative its temperature dependence.

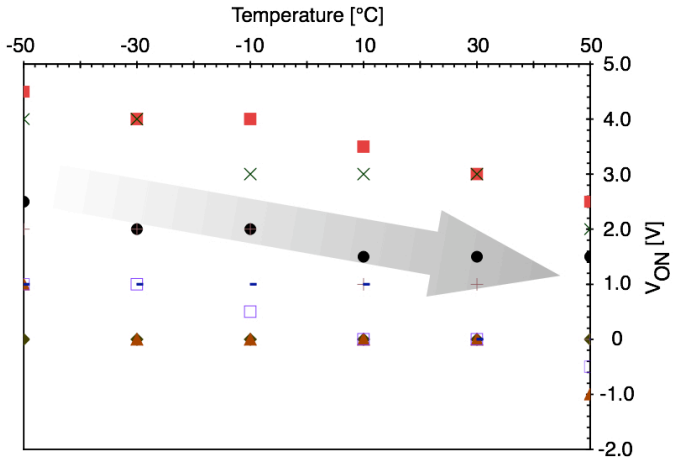
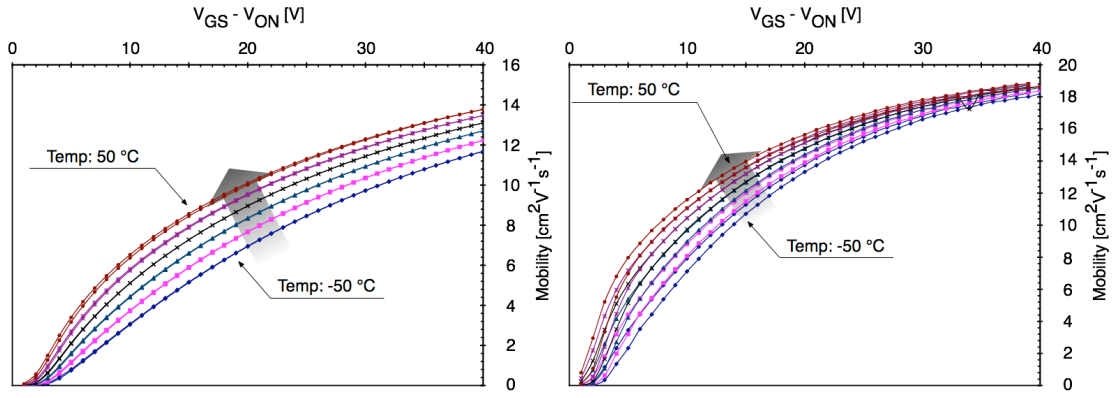


Figure 5.2: Temperature dependence of the turn-on voltage. Notice that the turn-on voltage of June132007 1-1-1(♦) shows no temperature dependence. The values of the turn-on voltage are extracted from the negative sweep, i.e. from V_{GS} = 40 V to -20 V, because of the current drop around V_{GS} = 0 V in the positive sweep, as shown in Fig. 5.4. The resolution of temperature is 20 °C, and that of the turn-on voltage is 0.5 V or 1 V. ♦: July132007 1-1-1, ■: July132007 1-4-1, ▲: July132007 1-4-2, ×: June202007 1-1-2, □: June202007 1-5-1, ●: July132007 1-6-1, +: June202007 2-1-3, and -: June202007 3-2-2.

Turn-on voltages extracted from $\log_{10}(I_D) - V_{GS}$ transfer curves at V_{DS} = 20 / 30 V are presented as a function of temperature in Fig. 5.2. With one exception, the clear trend is that V_{ON} decreases with increasing temperature between - 50 to + 50 °C. The behavior of the exception is notable. This device with V_{ON} equal to zero at room temperature exhibits a V_{ON} which is temperature-independent.

Figure 5.3 presents both average and incremental mobilities as a function of the overvoltage, i.e. $V_{GS} - V_{ON}$, and temperature. As clearly seen in the figure, both average and incremental mobilities exhibit a temperature dependence, i.e., both increase as the temperature increases. Even though the $\log_{10}(I_D) - V_{GS}$ transfer curves shown in Fig. 5.1 appear to shift rigidly toward more negative V_{ON}'s with increasing temperature, the mobility temperature dependence witnessed in Fig. 5.3 reveals this shift to be slightly non-rigid.



(a) (b)

Figure 5.3: Temperature dependency of (a) average and (b) incremental mobilities. The x-axis is normalized to $V_{GS} - V_{ON}$ to prevent the effect of turn-on voltage difference at a different temperature. The sample used is July132007 1-1-1. The arrow shows the direction of temperature increase.

Other notable observations with respect to this temperature dependence study are as follows: 1) No temperature dependence is observed for the subthreshold slope, S, or the drain current on-to-off current ratio, I_D^{ON-OFF}. 2) The temperature dependence of the drain current, $I_D(T)$, typically exhibits a better fit to an Arrhenius plot rather than a variable range-hopping (VRH) plot, which is expressed as a function of $T^{-1/4}$ [82]. However, for certain devices, $I_D(T)$ is equally well fit to either the Arrhenius or the VRH plot. The average activation energy obtained from Arrhenius plots of $I_D(T)$ when V_{GS} = 5 V is 0.15 eV, which corresponds to the Fermi level position with respect to the conduction band minimum of the channel layer [79]. To unambiguously establish drain current temperature trends for these types of device, a wider temperature range, especially in the lower temperature range, such as low as -200 °C is desirable. A summary of temperature measurements is provided in Table 5.1. In this table, a good Arrhenius fit is linear in $\frac{1}{T}$ while a good variable-range-hopping plot is linear in $\frac{1}{T^4}$.

Sample	V_{DS}	V_{ON}	I_D^{ON-OFF}	S	Temperature dependent? Mobility peak		I_D @ V_{GS} = 5 V	
					Average	Incremental	Arrhenius?	VRH?
July132007 1-1-1	20	No	No	No	Yes	Yes	Yes	No
July132007 1-4-1	20	Yes	No	No	Yes	?	Yes	Yes
July132007 1-4-2	30	Yes	No	No	Yes	Yes	Yes	Yes
June202007 1-1-2	30	Yes	No	No	?	?	Yes	No
June202007 1-5-1	20	Yes	No	No	Yes	?	Yes	No
June202007 1-6-1	20	Yes	No	No	N/A	N/A	Yes	No
June202007 2-1-3	30	Yes	No	No	Yes	Yes	Yes	No
June202007 3-2-2	30	Yes	No	No	Yes	No	Yes	No

Table 5.1: Summary of the IGZO TFT temperature-dependence assessment. A 'yes,' 'no,' or '?' entry in the first six columns is indicative of whether the respective parameter is temperature dependent over the temperature range - 50 to + 50 °C. A 'yes' or 'no' entry in the last two columns establishes whether the I_D temperature-dependence can be fit to an Arrhenius or variable-range hopping (VRH) model.

5.2 Off Current Direction Anomaly

Figure 5.4 displays positive and negative $\log_{10}(I_D)$-V_{GS} transfer curve sweeps for an IGZO TFT operated at an elevated temperature of 50 °C. The positive curve exhibits anomalous behavior in which I_D diverges off scale for a portion of the sweep voltage approaching zero volts. This anomalous behavior, when observed, is more noticeable at elevated temperatures and is usually not seen for room temperature measurements. Also notice that the positive and negative sweep curves are not identical and that the off current is on the order of 10^{-10} A, which is larger than the apparatus' minimum resolution by two orders of magnitude.

Further investigation of this anomalous drain current behavior reveals that it is correlated with anomalous current flow directions, as shown in Fig. 5.5. Figure 5.5 is quite complicated. Panels (a) and (b) are for a positive sweep, while panel (c) and (d) correspond to a negative sweep. Panels (a) and (c) plot positive currents (i.e., current flowing into the TFT), while panels (b) and (d) are for negative currents (i.e., current

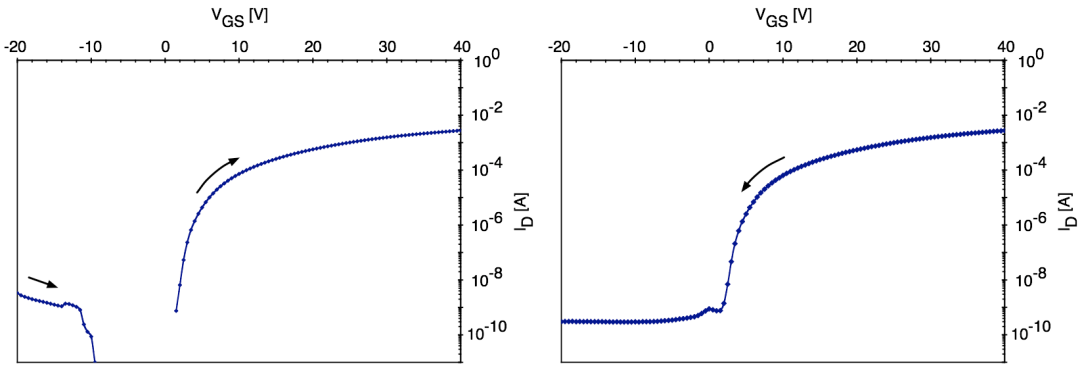


Figure 5.4: Separate plots of the $\log_{10}(I_D)$ – V_{GS} transfer characteristic at a temperature of 50 ° C: (a) a positive sweep (from V_{GS} = -20 V to 40 V) and (b) a negative sweep (from V_{GS} = 40 V to -20 V). The positive sweep is performed first, followed by the negative sweep without a pause between sweeps. The device shown is June202007 1-6-1.

flowing out of the TFT). The unshaded portion of each panel corresponds to a situation of normal current flow, so that shading is used to highlight the region of anomalous current flow. For each panel TFT insets are included in order to specify the direction of I_D and I_S current flow.

When a -20 V gate voltage step function is applied, current initially flows into the TFT through both the source and drain, as seen in Fig. 5.5 (a). In normal operation, drain and source currents should flow in the same direction such that these currents have opposite polarities. As the gate voltage increases from -20 V, the source current changes its direction at $V_{GS} \cong$ -10 V to that of its normal direction, as shown in Fig. 5.5 (b). However, the drain current also changes its direction to negative when $V_{GS} \cong$ -3 V so that both currents flow in the same direction once again, although both in an outward direction this time. When the gate voltage exceeds the turn-on voltage, both source and drain currents start to flow in the ideal direction, i.e., the drain current flows into the TFT and the source current flows out of the TFT. This condition is

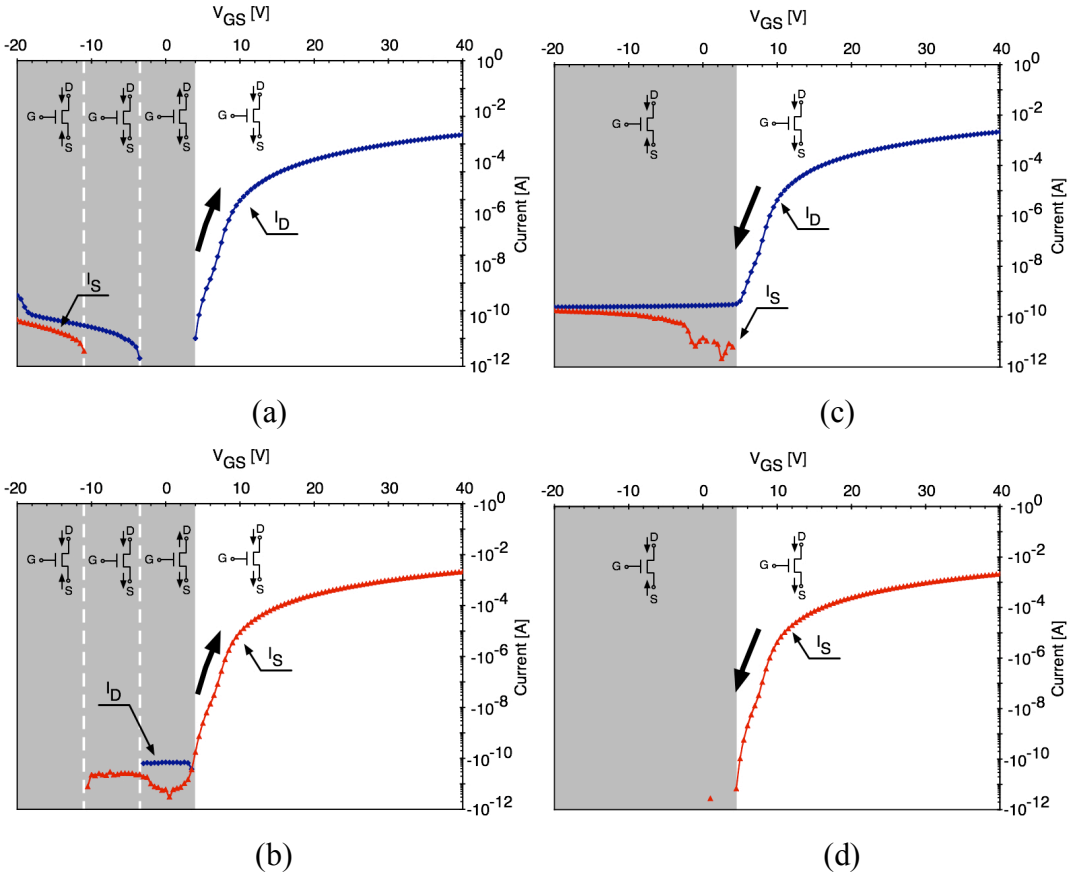


Figure 5.5: Source and drain currents flowing through an IGZO TFT for the case of (a) a positive sweep and a positive current, (b) a positive sweep and a negative current, (c) a negative sweep and a positive current, and (d) a negative sweep and a negative current. Positive current is defined as current going into the TFT, while negative current is defined as current flowing out of the TFT. Anomalous current flow occurs within the portion of the curve indicated in gray. The TFT insets included in each figure illustrate the direction of current flow. The sample is June202007 2-1-3, measured at 50 °C.

maintained until the gate voltage reaches the turn-on voltage in the negative sweep, as indicated in panel (c) and (d) of Fig. 5.5. When the gate voltage passes the turn-on voltage in the negative sweep, the source current direction becomes anomalous, as indicated in panel (c).

The anomalous drain/source current behavior illustrated in Fig. 5.4 and Fig. 5.5 probably appears to be very mysterious at this time. Since a specific physical

mechanism for this phenomena is proposed in Chapter 6, suffice it for now to say that this anomalous drain/source current is associated with trapping and detrapping of electrons in the channel as the channel is accumulated or depleted, respectively.

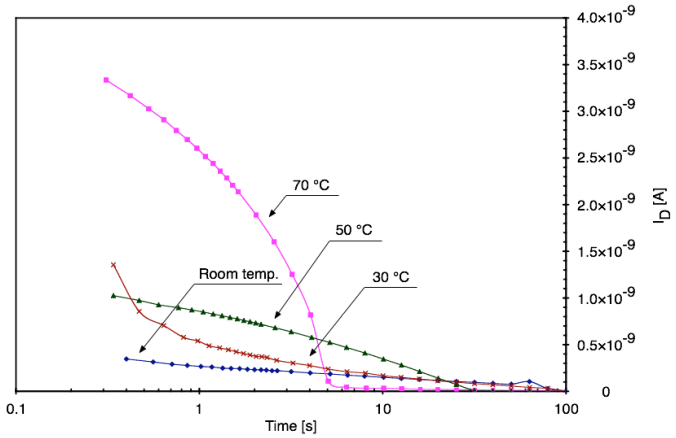


Figure 5.6: Transient response of the off current, I_{OFF}, at several different temperatures. The applied drain-source voltage is 20 V and gate-source voltage is -20 V. Both voltages are applied as a step function when t = 0 s. The sample is June202007 2-1-3.

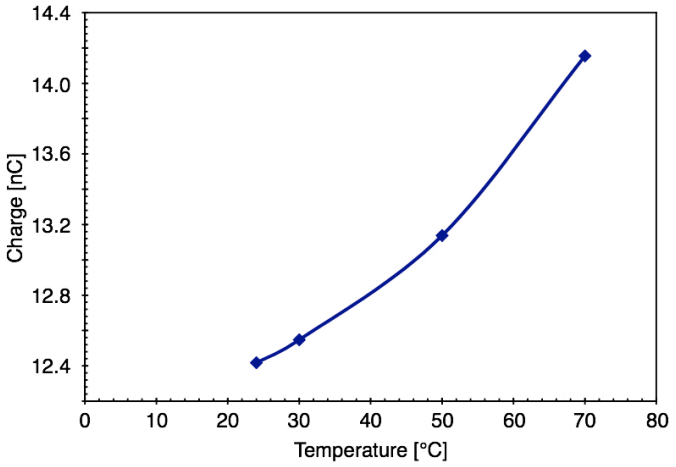


Figure 5.7: Temperature dependence of the charge released from traps inside the channel after applying a V_{GS} = -20 V voltage step (V_{DS} = 0). Charge is assessed by integrating the current flowing out of the source and drain over a period of 100 s after application of the gate voltage step. The sample measured is June202007 2-1-3.

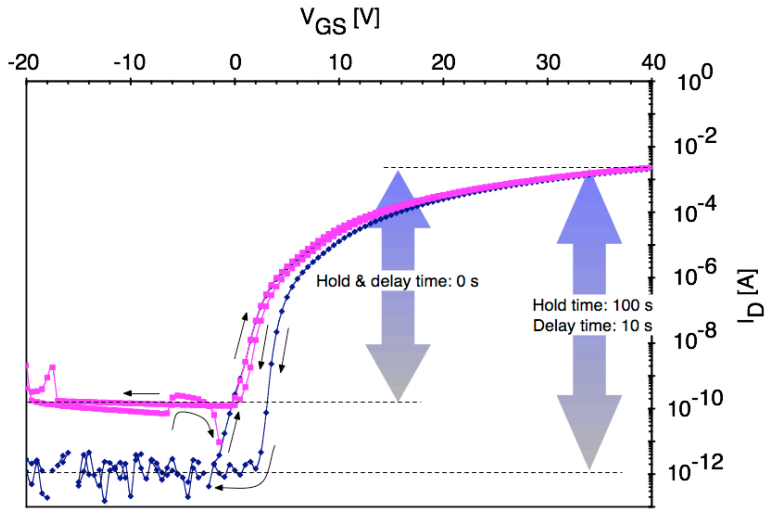


Figure 5.8: A comparison between $\log_{10}(I_D) - V_{GS}$ transfer curves acquired using (i) a hold time and delay time of 0 s and (ii) a hold time of 100 s and a delay time of 10 s. The drain current on-to-off ratio, I_D^{ON-OFF} is two orders of magnitude larger for (ii), but (ii) also exhibits more hysteresis. The sample is June202007 2-1-3 with V_{DS} = 20 V measured at room temperature.

Figure 5.6 presents the transient response of drain current to a V_{GS} = -20 V step function with V_{DS} = 20 V. As clearly seen in Fig. 5.6, especially from the response at a temperature of 70 °C, there is a drain current which starts flowing immediately after application of a -20 V gate-source step function and diminishes as time elapses. Such a current should not be observed for an ideal TFT since the gate-source voltage is well below that of the turn-on voltage, which is -2.5 V for this TFT. Several notable points regarding this drain current non-ideality shown in Fig. 5.6 are 1) current flows into the TFT, which equivalently means that electrons flow out of the TFT, 2) the duration in which this abnormal current flows is limited to a specific duration, e.g., 5 s for a temperature of 70 °C, and 3) this duration is clearly temperature dependent. The first observation noted above establishes that this abnormal current is associated with the electron (or negative charge) release from channel accumulation layer. A detailed explanation and a proposed mechanism for this behavior is presented in Chapter 6.

Figure 5.7 presents the total charge flowing out of the TFT due to detrapping as a function of temperature. This total charge is obtained by integrating the currents flowing through the source and drain of the TFT over a period of 100 s after application of a -20 V step function to the gate. It is clearly seen that the total charge increases as the temperature increases. Thus, detrapping is thermally enhanced. These trends are scrutinized further in Section 6.

Recognizing that a portion of the current behavior shown in Fig. 5.4 and Fig. 5.5 arises from temperature-dependent detrapping in the channel associated with the -20 V gate voltage step, it is clear that $\log_{10}(I_D) - V_{GS}$ transfer curves are not in steady-state when measured in this manner. One way to perform a transfer curve measurement so that it is closer to steady state is to introduce a hold time after application of the gate voltage step in which the – 20 V gate voltage is held constant for a fixed hold time prior to beginning the positive sweep. Another data acquisition modification which should ensure that the measurement is closer to steady state is to introduce a delay time between voltage steps, so that an I_D measurement does not occur until after the delay time period has elapsed.

Figure 5.8 shows a $\log_{10}(I_D) - V_{GS}$ transfer curve comparison between a data set acquired using zero hold and delay times and another data set obtained when the hold time is 100 s and the delay time is 10 s. Three important observations are available from an assessment of Fig. 5.8. First, the anomalous drain current behavior is eliminated when the hold and delay times are increased. Second, the off current decreases from ~ 10^{-10} A to 10^{-12} A when the hold and delay times are increased, thereby increasing the drain current on-to-off ratio from 1.8×10^{7} to 1.5×10^{9}. Lastly,

the turn-on voltage decreases from 0 V to -2.5 V, when the hold and delay times are increased. These two observations are related to trapping and detrapping of electrons in the channel, as discussed in more detail in Chapter 6.

6 PHYSICAL MECHANISMS FOR NON-IDEAL PHENOMENA

In this chapter, physical mechanisms for each non-ideal phenomenon observed in previous chapters are discussed.

6.1 Experimental Results Summary

In previous sections, several non-ideal phenomena are observed, which involve

1. V_{ON} shift during constant-voltage stress bias testing: An almost rigid shift in $\log_{10}(I_D) - V_{GS}$ transfer curves in which the turn-on voltage, V_{ON}, moves to a more positive gate voltage with increasing stress time in constant-voltage bias-stress testing of IGZO TFTs (Subsection 4.1).
2. Stability improvement with increasing post-deposition annealing temperature: An improvement of IGZO TFT stability with increasing post-deposition annealing temperature over the temperature range of 200 – 300 ºC; i.e., less V_{ON} shift and hysteresis in $\log_{10}(I_D) - V_{GS}$ transfer curves both in pre- and post-stressed states (Subsection 4.1).
3. Recoverable V_{ON} shift: An at least partially reversible turn-on voltage shift induced by constant-voltage bias-stressing. That is, V_{ON} tends to recover towards its initial value of V_{ON} if the TFT is left unbiased in the dark for a prolonged period of time. More complete recovery is observed as the recovery period increases (Subsection 4.2).

4. V_{ON} adjustable to 0 V: V_{ON} of a TFT can be set equal to zero volts after bias-stress testing, if the TFT electrodes are grounded and the TFT is maintained in the dark for a prolonged period of time (Subsection 4.2).

5. Failure of accelerated recovery: Attempts to accelerate recovery by application of a negative gate bias at an elevated temperature (i.e., 100 ºC) were unsuccessful. Accelerated recovery attempts led to a severely degraded subthreshold swing (Subsection 4.2).

6. Temperature dependence of V_{ON}: An almost rigid $\log_{10}(I_D)$ $-V_{GS}$ transfer curve shift to a lower (more negative) V_{ON} with increasing temperature, except for a TFT with an initial V_{ON} equal to zero, in which case the $\log_{10}(I_D) - V_{GS}$ transfer curve is temperature-independent. A more detailed assessment, however, indicates that the $\log_{10}(I_D) - V_{GS}$ transfer curve shift is not exactly rigid since the mobility is found to increase slightly with increasing sample temperature (Subsection 5.1).

7. Drain current anomaly: An anomaly in certain $\log_{10}(I_D) - V_{GS}$ transfer curves, especially when obtained at an elevated temperature (e.g., 30 or 50 ºC), in which I_D decreases precipitously near zero volts during the positive gate voltage sweep. This anomaly is attributed to detrapping due to the application of a -20 V gate voltage step at the initiation of a $\log_{10}(I_D) - V_{GS}$ transfer curve measurement (Subsection 5.2).

Although it might seem as if these results originate from different physical mechanisms, they are all believed to be related to trapping/detrapping phenomena. Different phenomena appear to arise from different types of trap.

6.2 Trapping Mechanisms

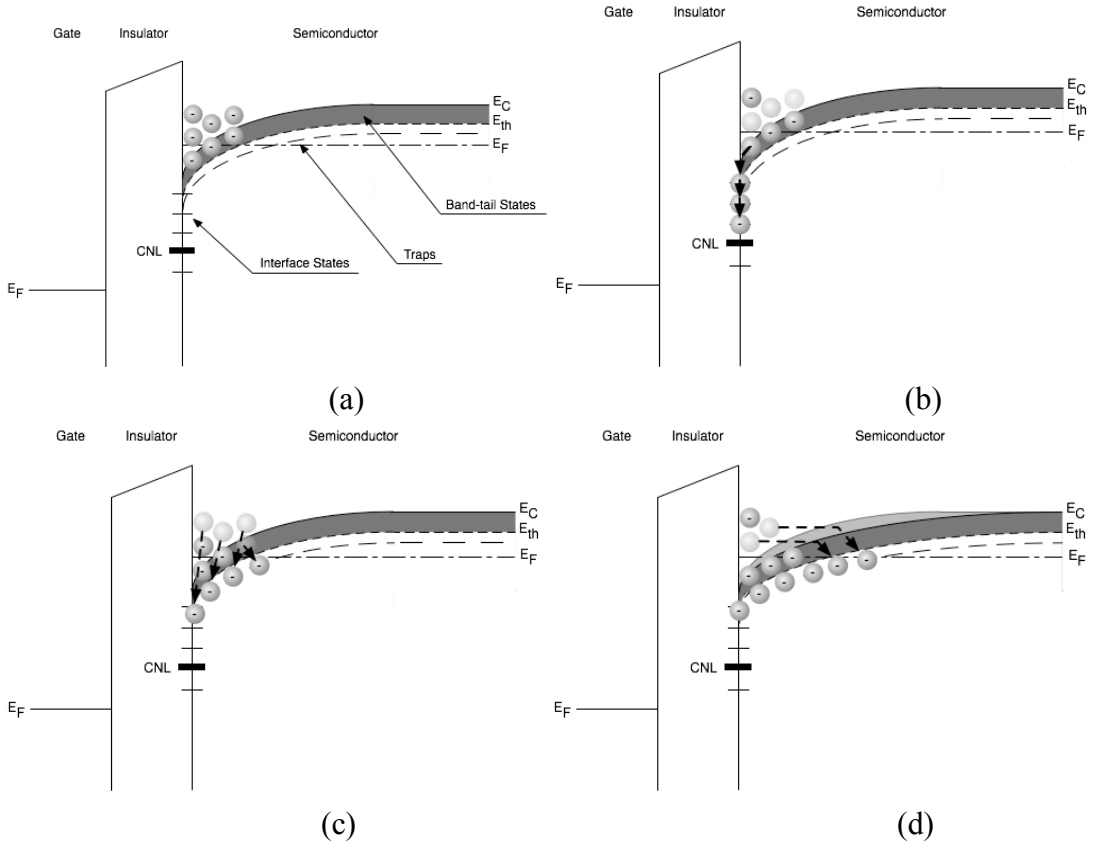


Figure 6.1: (a) Three possible trapping mechanisms involving interface states, 'bulk' semiconductor traps, and band-tail states. (b) Interface states which are located at the insulator/semiconductor interface capture electrons quickly. Interface states are acceptor-like when located above the charge neutrality level (CNL) and are donor-like when located below CNL. (c) 'Bulk' semiconductor trapping can occur throughout the channel layer. This trapping is rapid in the accumulation layer since many conduction band electrons are available for trap filling. However, this type of trapping may be slow in regions of the semiconductor which are depleted or which have a very small conduction band electron concentrations. (d) Band-tail state trapping is similar to 'bulk' semiconductor trapping since the time required for trapping depends upon the conduction band electron concentration.

In this subsection, several different trap types are discussed to facilitate understanding of the physical mechanisms associated with the non-ideal phenomena summarized above.

There are three different types of trap which may contribute to TFT non-ideal behavior: interface states, 'bulk' semiconductor traps, and band-tail states, as shown in Fig. 6.1 (a). Since the insulator employed is high-quality thermally-grown silicon dioxide provided by Hewlett-Packard, non-ideal factors in the insulator are believed to be negligible when compared to that of the IGZO layer. Thus, only trapping mechanisms involving the semiconductor layer or the insulator/semiconductor interface are considered. Since band-tail states are not believed to be a direct cause of the non-ideal phenomena observed in this research, they are not discussed any further in this subsection, although 'bulk' semiconductor traps may be perceived as a special case of band-tail states in amorphous IGZO.

6.3 Proposed Physical Mechanisms

In this subsection, physical mechanisms are proposed for each observed non-ideal phenomenon.

6.3.1 IGZO TFT instabilities

TFTs which underwent constant-voltage bias-stress testing for a period of 10^5 s show a rigid shift of the $\log_{10}(I_D) - V_{GS}$ transfer curve along V_{GS} axis. Since this process is reversible, it is attributed to electron trapping in conjunction with a charge centroid shift.

The capture time of a free electron into a trap may be expressed as

$$\tau_n = \frac{1}{v_{th}\sigma_n n_C}\exp\left[\frac{-q\psi(x)}{k_B T}\right], \tag{6.1}$$

where v_{th} is the thermal velocity (~1×10^7 cm/s at room temperature), σ_n is the capture cross section, n_C is the conduction electron density, and $\psi(x)$ is the potential at an arbitrary distance from the insulator/semiconductor interface.

τ_n is quite revealing with regard to physical mechanisms responsible for IGZO TFT instabilities and temperature-dependent phenomena. Table 6.1 is a compilation of room temperature trap capture times, based on the use of Eq. 6.1 and assuming a conduction band electron density, $n_C = 10^{15}$ cm^{-3}. Note that these estimates for τ_n are independent of whether the trap in question is an interface state, a 'bulk' semiconductor trap, or a band-tail state. Also notice that traps are distinguished as acceptor- or donor-like, depending on whether electron capture involves, respectively, neutral or coulombically attractive electrostatic interaction.

Table 6.1: Room temperature trap capture times, based on Eq. 6.1, assuming a conduction band electron density, $n_C = 10^{15}$ cm^{-3}.

σ_n [cm^2]	$q\phi(x)$ [eV]	τ_n [s]
10^{-15} (acceptor)	0 (flat-band)	10^{-7}
	+0.3 (accumulation)	10^{-12}
	-0.3 (weak depletion)	10^{-2}
	-0.6 (moderate depletion)	10^{3}
	-0.9 (strong depletion)	10^{8}
10^{-12} (donor)	0 (flat-band)	10^{-10}
	+0.3 (accumulation)	10^{-15}
	-0.3 (weak depletion)	10^{-5}
	-0.6 (moderate depletion)	10^{0}
	-0.9 (strong depletion)	10^{5}

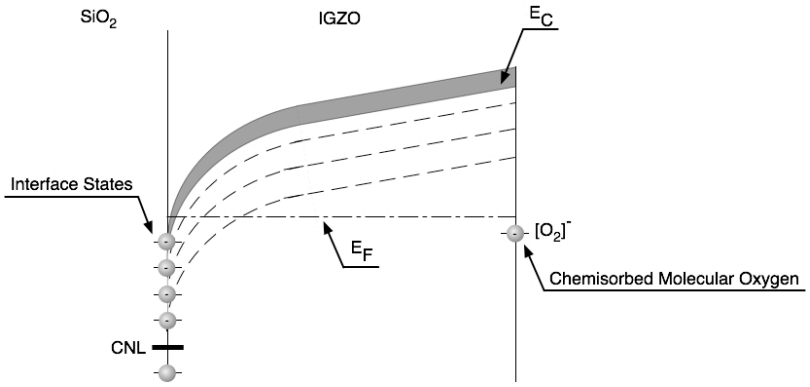


Figure 6.2: Energy band diagram of an IGZO-based TFT. Chemisorbed molecular oxygen depletes the full extent of the IGZO channel layer.

Table 6.1 indicates trapping to be very rapid under flat-band or accumulation conditions. Since a TFT operates in accumulation, electron trapping in the channel should occur very quickly, independent of whether this trapping involves interface states, 'bulk' semiconductor traps, or band-tail states. Recall that constant-voltage bias-stress measurements of IGZO TFTs demonstrate an operative instability mechanism for stress times of at least 10^5 s. Therefore, from Table 6.1, it appears as if this trapping occurs in regions of the TFT remote from the accumulation channel, where the semiconductor finds itself in moderate or strong depletion as illustrated in Fig. 6.2. The unpassivated front surface of the TFT appears to be a likely region in which very slow trapping would likely occur. Note that the IGZO channel layer is shown in Fig. 6.2 to be depleted across its entire thickness. This appears to be the case since the 'bulk' depletion width is calculated to be ~ 100 nm (assuming a conduction electron density of 10^{15} cm^{-3}, a potential difference of 0.1 V, and an IGZO relative dielectric constant of 11.5) while the physical width of the IGZO channel layer is 70 nm. Also notice that depletion of the IGZO channel layer is ascribed to this chemisorbed molecular oxygen [79].

Next, an explanation for why a positive turn-on voltage shift is observed after constant-voltage bias-stress testing is provided.

Figure 6.3 shows that there are two charge centroids in the semiconductor layer of an IGZO TFT, one for conduction band electrons and one for empty donor-like traps which are positively charged. According to Wager *et al.* [79], the turn-on voltage, V_{ON}, is given by

$$V_{ON} = \phi_{MS} - \sum_i \frac{\gamma_i^I Q_i}{C_G} - \sum_j Q_j \left(\frac{1}{C_G} + \frac{\gamma_j^S}{C_S} \right), \tag{6.2}$$

where ϕ_{MS} is the work function difference between a gate metal and a semiconductor, C_G is the insulator capacitance density, C_S is the channel capacitance density, and γ_i^I and γ_i^S are normalized charge centroid locations inside the insulator and channel, respectively, and are defined as follows:

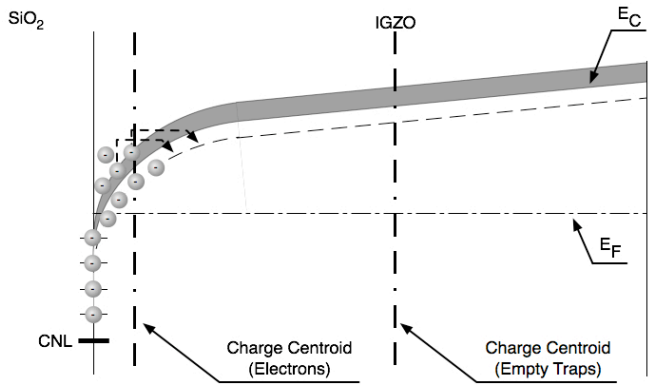


Figure 6.3: Charge centroids for conduction band electrons and empty donor-like traps. The charge centroid for conduction band electrons is located close to the insulator/semiconductor interface. Since 'bulk' semiconductor traps are assumed to be donor-like, they are positive when empty. Thus, a charge centroid for positively charged empty traps also exists.

$$\gamma_i^I = \frac{1}{t_G}\frac{\int_0^{t_G} x\rho_i(x)dx}{\int_0^{t_G}\rho_i(x)dx} = \frac{1}{t_G}\frac{\int_0^{t_G} x\rho_i(x)dx}{Q_i}, \tag{6.3}$$

$$\gamma_i^S = \frac{1}{h}\frac{\int_{t_G}^{t_G+h}(x-t_G)\rho_j(x)dx}{\int_{t_G}^{t_G+h}\rho_j(x)dx} = \frac{1}{h}\frac{\int_{t_G}^{t_G+h}(x-t_G)\rho_j(x)dx}{Q_j}, \tag{6.4}$$

where t_G is the insulator thickness, h is the channel thickness, and $\rho_i(x)$ and $\rho_j(x)$ are charge densities as a function of distance from the gate metal/insulator interface in the insulator and channel, respectively. The charge centroid in the insulator, γ_i^I, and in the channel, γ_i^S, ranges from 0 to 1; γ_i^I is 0 when all charge in the insulator is located at the gate/insulator interface and is 1 when it is present at the insulator/channel interface. Likewise, γ_i^S is 0 if all charge is at the insulator/channel interface and is 1 when all charge is located at the channel back surface.

Considering only two dominant charges in the channel, i.e., conduction band electrons (negative charge), Q_e^S, and empty donor-like traps (positive charge), Q_h^S, the V_{ON} shift may be expressed as

$$\begin{aligned}\Delta V_{ON} &= -\sum_j Q_{j2}\left(\frac{1}{C_G}+\frac{\gamma_{j2}^S}{C_S}\right)+\sum_k Q_{k1}\left(\frac{1}{C_G}+\frac{\gamma_{k1}^S}{C_S}\right)\\ &= -Q_{e2}^S\left[\frac{1}{C_G}+\frac{\gamma_{e2}^S}{C_S}\right]-Q_{h2}^S\left[\frac{1}{C_G}+\frac{\gamma_{h2}^S}{C_S}\right]+Q_{e1}^S\left[\frac{1}{C_G}+\frac{\gamma_{e1}^S}{C_S}\right]+Q_{h1}^S\left[\frac{1}{C_G}+\frac{\gamma_{h1}^S}{C_S}\right],\end{aligned} \tag{6.5}$$

where the subscript 1 and 2 refer to pre-stressed and post-stressed state, respectively. Assuming that charge centroid positions do not change before and after the stress, in other words, $\gamma_{e2}^S \approx \gamma_{e1}^S = \gamma_e^S$ and $\gamma_{h2}^S \approx \gamma_{h1}^S = \gamma_h^S$, Eq. 6.5 is reformulated to

$$\Delta V_{ON} \cong -\Delta Q_e^S\left[\frac{1}{C_G}+\frac{\gamma_e^S}{C_S}\right]-\Delta Q_h\left[\frac{1}{C_G}+\frac{\gamma_h^S}{C_S}\right]. \tag{6.6}$$

where $\Delta Q_e^S = Q_{e2}^S - Q_{e1}^S$ and $\Delta Q_h^S = Q_{h2}^S - Q_{h1}^S$. The overall sign of the first term of Eq. 6.6 is negative, due to the original negative sign, the negative sing associated with electron charge, and the negative sign of the ΔQ_e^S term since accumulation layer electrons are trapped. In contrast, the overall sign of the second term of Eq. 6.6 is positive since the original negative sign is cancelled by the negative sign of ΔQ_h^S since fewer traps are empty at the end of the bias stress duration. Since the turn-on voltage shift observed in this research is always positive, the second term in Eq. 6.6 appears to dominate the equation. Therefore,

$$\Delta V_{ON} \cong -\Delta Q_h\left[\frac{1}{C_G}+\frac{\gamma_h^S}{C_S}\right]. \tag{6.7}$$

Equation 6.7 constitutes a quantitative answer to the question: Why is the turn-on voltage shift positive for a constant-voltage bias-stress measurement of an IGZO TFT? In words, the answer to this question is that accumulation layer electrons are trapped in donor-like traps, appreciably decreasing the empty trap charge density within the IGZO layer. Employing practical values, including $\Delta V_{ON} = 5$ V, $C_G = 34.5\times10^{-9}$ F·cm^{-2}, $C_S = 1.46\times10^{-7}$ F·cm^{-2}, and $\gamma_h^S \approx 0.5$, the change in the number of empty traps is calculated to be 9.6×10^{11} cm^{-2}, compared to the number of electrons induced into the accumulation layer, 5.4×10^{12} cm^{-2} at V_{GS} = 30 V with V_{ON} = 5 V. Thus, when $\Delta V_{ON} = 5$ V, approximately 18 % of the accumulation layer electrons are trapped after 10^5 s.

In summary, the long time constants and positive turn-on voltage shifts witnessed in constant-voltage bias-stress measurements of IGZO-TFTs are both attributed to electron trapping into donor-like states located within the IGZO channel layer, away from the insulator/semiconductor interface.

6.3.2 Temperature Dependence

$Log_{10}(I_D) - V_{GS}$ transfer curves shift almost rigidly to lower V_{GS}'s as the temperature increases. More specifically, V_{ON} decreases while μ_{INC} and μ_{AVG} increase slightly as the temperature increases.

The V_{ON} temperature dependence mechanism is attributed to trap filling in the IGZO. According to the discrete donor trap model [79],

$$V_{ON} = -\frac{q}{C_G}\left(n_{CO} - p_{TO}\right), \tag{6.8}$$

where q is the electronic charge, C_G is the capacitance density of the insulator, n_{CO} is the equilibrium conduction band electron sheet density and p_{TO} is the empty donor-like trap equilibrium sheet density. Thus, according to this model, the turn-on voltage shift with respect to a change in temperature may be expressed as

$$\Delta V_{ON} = -\frac{q}{C_G}\left(\Delta n_{CO} - \Delta p_{TO}\right). \tag{6.9}$$

where ΔV_{ON} is negative when going from a lower to a higher temperature. This means, from Eq. 6.9, that n_{CO} (higher temperature) > n_{CO} (lower temperature) and p_{TO} (lower temperature) > p_{TO} (higher temperature). These two relations are always satisfied as long as the Fermi level is positioned below the trap energy. Additionally,

according to this model, the channel mobility is expected to increase with increasing temperature because fewer traps are empty, so that fewer electrons injected into the channel are trapped. Even if a more complicated trap distribution is assumed, the same basic arguments of a discrete trap model employed in this discussion are appropriate.

6.3.3 Drain Current Anomaly

During the positive sweep of a $\log_{10}(I_D) - V_{GS}$ transfer curve measurement, especially at an elevated temperature, the off current portion of the transfer curve sometimes exhibits an abrupt decrease around $V_{GS} = 0$, as discussed in Subsection 5.2. This drain current anomaly is the direct result of drain current which initially flows in a reverse direction due to detrapping.

Details of the proposed trapping/detrapping physical mechanism responsible for this drain current anomaly are illustrated in Fig. 6.4.

At zero bias, interface states, 'bulk' semiconductor traps, and band tail states are filled to their equilibrium occupancy, as indicated in an idealized manner in Fig. 6.4 (a). Initiation of the acquisition of a $\log_{10}(I_D) - V_{GS}$ transfer curve is accomplished by application of a large negative gate voltage, typically $V_{GS}(t = 0s) = -20$ V. This gate voltage depletes the semiconductor interface, leading to trap emission, as shown in Fig. 6.4 (b). Note that when trap emission is the dominant effect, the source current, I_S, direction is anomalous (see the transistor symbol shown in the gray portion of the $\log_{10}(I_D) - V_{GS}$ transfer curve of Fig. 6.4 (b)), since detrapped electrons are extracted at the source, rather than injected.

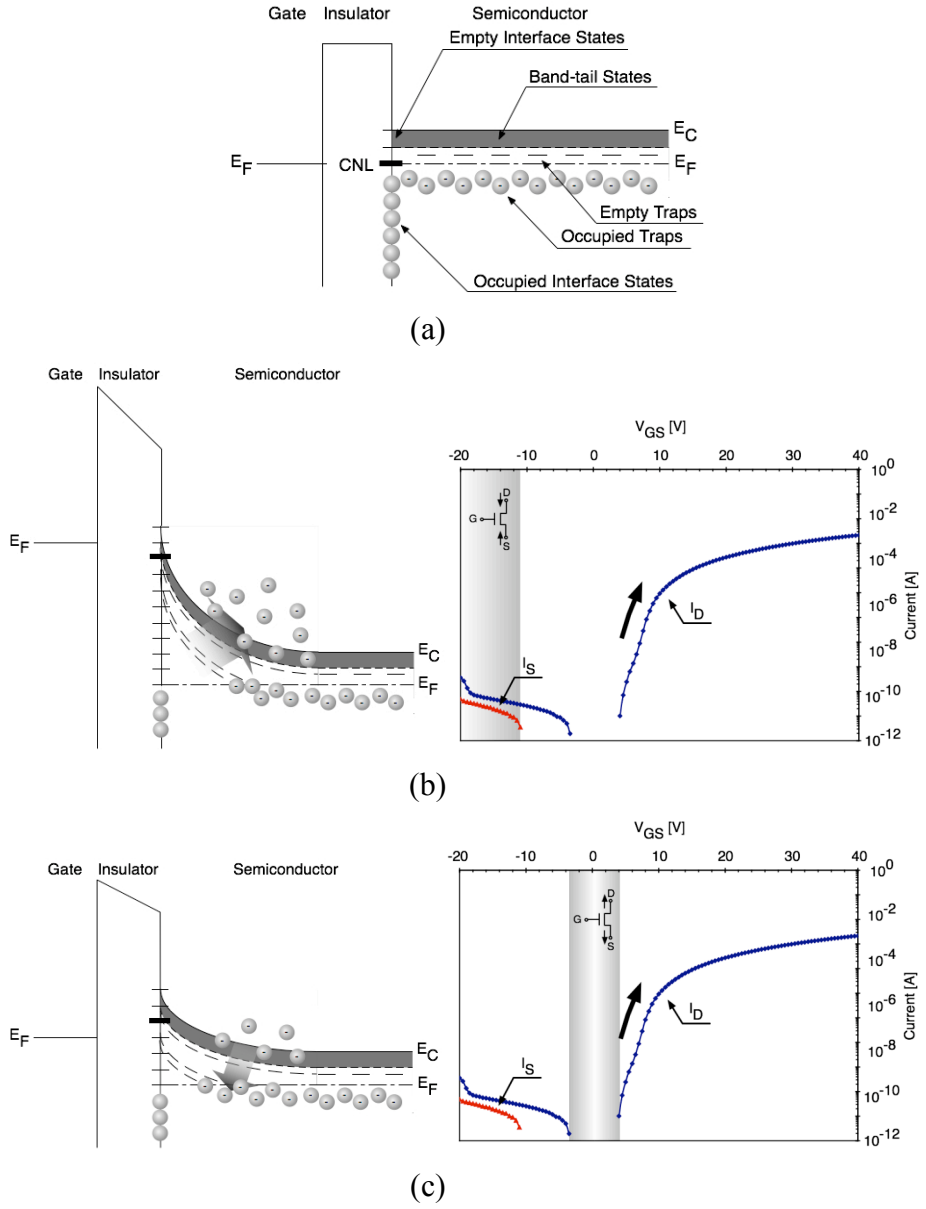


Figure 6.4: $Log_{10}(I_D) - V_{GS}$ transfer curve anomaly mechanism; (a) Idealized energy band diagram at zero bias. (b) When an abrupt large negative voltage, i.e., -20 V, is applied to the gate electrode, the channel layer interface strongly depletes so that electrons are released from traps and flow out of the TFT, contributing to drain and source currents. The trap emission rate decreases as the gate-source voltage increases and as time elapses. When the gate-source voltage reaches a certain level, i.e., ~ -11 V for this case, all of the electrons released from traps flow toward the drain terminal only, because of the drain-source 20 V voltage. (c) However, as the gate voltage increases, the channel layer interface becomes less depleted so that emptied traps start to capture electrons from the conduction band, reversing the direction of drain and source current flow.

As the gate voltage increases, the semiconductor electric field near the interface decreases so that the trap emission rate decreases, causing both I_S and I_D to decrease. This decrease in I_S and I_D is first gradual, but then precipitous. This precipitous decrease in I_S and I_D presumably occurs when regions of the channel near the source and drain, respectively, approach flat band.

Finally, as the gate voltage increases even further, to near zero volts, a situation arises in which trap filling occurs. This is shown in Fig. 6.4 (c). In this regime of operation, the polarities of I_S and I_D reverse, as shown by the transistor symbol included in the gray portion of the $\log_{10}(I_D) - V_{GS}$ transfer curve of Fig. 6.4 (c). Note that this regime only exists up to V_{ON}, after which normal drain current due to electron injection at the source and electron extraction at the drain are the dominant effects.

In summary, the drain current anomaly witnessed for certain IGZO TFTs during the positive sweep of a $\log_{10}(I_D) - V_{GS}$ transfer curve is ascribed to near-interface trap emission and subsequent trap filling. Since trap emission is a thermally activated process, this anomaly is more pronounced at elevated temperatures, as supported by Fig. 5.7. Note that this type of anomalous current flow only dominates when the TFT is in an off state in which $V_{GS} < V_{ON}$. An important consequence of this anomalous effect is that the measured drain current on-to-off ratio may be dramatically increased, by approximately two orders of magnitude, if a $\log_{10}(I_D) - V_{GS}$ transfer curve is acquired in a manner in which manifestation of this drain current anomaly is avoided, as presented in Fig. 5.8, by employing a less abrupt gate voltage. Another significant consequence of this anomaly is that deep depleting gate voltages should be avoided if IGZO TFT off current is to be minimized. This should be an easy constraint to meet

in normal circuit operation, as long as these devices are fully enhancement-mode, with $V_{ON} > 0$ V.

6.3.4 Stretched Exponential Law and Trapping Mechanism

With an appropriate reformulation, some examples of the drain current degradation phenomena discussed in Subsection 6.3.1 may be described using the following simple expression

$$I_D(t) = I_{D0} \exp\left[-\left(t/\tau\right)^{\beta}\right], \tag{6.10}$$

where I_{D0} is the initial drain current, β is a constant, which is sometimes called the Kohlrausch stretching exponent, and τ is a time constant. This expression is called a stretched exponential function, sometimes also referred to as a Kohlrausch-William-Watts (KWW) function and more commonly formulated as

$$\phi(t) = \exp\left[-\left(t/\tau\right)^{\beta}\right], \tag{6.11}$$

where $\phi(t) = \frac{I_D(t)}{I_{D0}}$. Various types of relaxation processes in many amorphous materials are known to be describable, using this expression [83][84][85]. The process to find the positive match between the empirical data and Eq. 6.10 is discussed in the Appendix.

The stretched exponential relationship can be employed to describe trapping when traps have an activation energy distribution

$$f(\Delta E)d\Delta E = \exp\left[-\frac{\Delta E}{k_B T_0}\right]\frac{d\Delta E}{k_B T_0}, \tag{6.12}$$

where f(ΔE)dΔE is an activation energy distribution, ΔE is the activation energy as measured from the conduction band edge, k_B is Boltzmann's constant, and T_0 is a characteristic temperature. This is similar to a band-tail state distribution, which can be expressed as

$$N(\Delta E) = N_0 \exp\left[-\frac{\Delta E}{k_B T_0}\right], \tag{6.13}$$

where N_0 is the density of states at the conduction band edge [86]. Following the method proposed by Bender and Shlesinger [87][88] based on the activation energy distribution expressed in Eq. 6.12, the probability density of an electron remaining at the same site for a time of t can be expressed as

$$\psi(t) \sim \frac{\beta\Gamma(\beta+1)}{\lambda_0{}^{\beta}} t^{-(1+\beta)}, \tag{6.14}$$

where $\beta = \frac{T}{T_0}$ and λ_0 are constants and Γ is a gamma function. This expression leads to the probability of conduction band electrons not being captured by a trap after a period of t, which is expressed in the form of a stretched exponential

$$\phi(t) = \exp\left[-const \bullet t^{\beta}\right], \tag{6.15}$$

as shown by Shlesinger and Motroll [89], following almost the same manner as Tachiya, only starting from a different expression [90]. When the mean duration of an electron moving to the next site, τ, is finite, Eq. 6.15 can be recast as [87]

$$\phi(t) = \exp\left[-\left(t/\tau\right)^{\beta}\right], \tag{6.11}$$

Therefore, the number of conduction electrons at a time t may be expressed as

$$n_C(t) = \phi(t) n_{C0}, \tag{6.16}$$

where n_{C0} is the initial number of conduction band electron at time 0. Since drift is thought to be the primary conduction mechanism of a TFT, as discussed in Subsection 2.2.3, the drain current density, J_D, may be expressed as

$$J_D(t) = q\mu_{EFF}(t) n \xi, \tag{6.17}$$

where q is the electronic charge, n is the number of mobile electrons, ξ is the electric field applied between the source and drain, and $\mu_{EFF}(t)$ is a time-dependent effective electron mobility, equal to

$$\mu_{EFF}(t) = \frac{n_C(t)}{n_T(t) + n_C(t)} \mu_n = \frac{n_C(t)}{n_{C0}} \mu_n = \phi(t) \mu_n, \tag{6.18}$$

where $n_T(t)$ is the concentration of trapped electrons, according to Tickle [9]. Combining Eq. 6.17 and 18, J_D is now expressed as

$$J_D(t) = \phi(t) q \mu_n n \xi. \tag{6.19}$$

When the initial drain current density is J_{D0},

$$\frac{J_D(t)}{J_{D0}} = \frac{I_{D0}(t)}{I_{D0}} = \phi(t) = \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right], \tag{6.20}$$

which is identical to the experimentally-deduced expression, Eq. 6.10. Thus, a Boltzmann distribution of traps, such as band-tail states as specified by Eq. 6.12, leads to a stretched exponential relationship for describing normalized drain current degradation, as given by Eq. 6.20.

A notable aspect of this formulation is that both β and τ have a physical meaning. β is related to the activation energy distribution via the characteristic

temperature T_0 and τ is related to the trap density. A larger τ and/or a larger β corresponds to a more stable TFT.

7 CONCLUSIONS AND RECOMMENDATION FOR FUTURE WORK

7.1 Conclusions

First, consider IGZO TFT instability assessment. Instability assessment is accomplished via constant-voltage bias-stress testing over a duration of 10^5 s. IGZO TFT instability is characterized by rigid shift in the $\log_{10}(I_D) - V_{GS}$ transfer curve to a more positive turn-on voltage. This turn-on voltage shift is found to be at least partially reversible. For example, if a TFT stressed is left for an extended period of time unbiased in the dark, it tends to return towards its initial turn-on voltage. IGZO TFT device stability improves with increasing post-deposition annealing temperature over the temperature range of 200 – 300 ºC. The IGZO TFT instability mechanism is ascribed to the filling of donor-like traps in the 'bulk' IGZO semiconductor and also to electron trapping at the SiO_2/IGZO interface.

Second, temperature dependent measurements are performed over a temperature range of -50 to +50 ºC. The main temperature effect is a decrease in the turn-on voltage with increasing temperature. No temperature dependence is observed for a IGZO TFT which has a turn-on voltage of zero. These temperature dependent trends are ascribed to donor-like traps.

Finally, an anomaly in certain $\log_{10}(I_D) - V_{GS}$ transfer curves, which is particularly pronounced at an elevated temperature of 30 or 50 ºC, is sometimes observed in which the drain current decreases precipitously near zero volts during the positive gate voltage sweep. This anomalous behavior is ascribed to trap emptying

subsequent to the application of a large, abrupt negative gate voltage which depletes the IGZO channel. The drain current on-to-off ratio is found to increase by up to two orders of magnitude if this anomalous behavior is circumvented using an extended hold time after applying the gate voltage step, so that the transfer curve measurement is accomplished in steady-state manner.

7.2 Recommendations for Future Work

There are still much work left to be accomplished with regard to the stability of amorphous semiconductor TFTs.

1. Long-term stability characteristics of IGZO TFTs under AC stressing: This is an alternate method employed, for example, in the assessment of AMLCDs [91]. AC bias-stress analysis may provide further insight into the TFT instability physics.

2. Assessment of 'bulk' traps, band-tail states, and interface states of IGZO TFTs: As presented in Chapter 6, all phenomena observed in this research are ascribed to trapping mechanisms. Direct measurement of trap properties is highly desirable.

3. Stretched exponential modeling: As discussed in Subsection 6.3.4, if traps follow a Boltzmann distribution, drain current degradation appears to be describable using a stretched exponential model. Experimental and theoretical work following this observation may lead to new insight into IGZO TFT instabilities.

4. Stability analysis of other types of amorphous oxide TFTs: Many other types of amorphous oxide semiconductor (e.g., zinc tin oxide, zinc indium oxide) are available for fabricating TFTs. Stability assessment of these types of TFT will establish their technological viability.

8 Appendix

8.1 Experimental Data

In the following subsections, complete sets of empirical results related to constant-voltage bias-stress testing, no bias room temperature recovery, and accelerated recovery are provided in the tabulated format. Columns are aligned so that the data acquired earlier in the testing process is on the left and that acquired later is on the right. The fabrication conditions of each sample are provided in Table 3.2 of Chapter 3.

8.1.1 Constant-Voltage Bias Stress Testing

Condition		Turn-on voltage [V]			Subthreshold swing		
Sample	**Stress [V]**	**Initial**	**Final**	**Shift**	**Initial**	**Final**	**Change**
061202 A250-1	$V_{DS} = V_{GS} = 30$	**+7**	+17	**+10**	**0.952**	0.659	-0.293
061202 A300-5	$V_{DS} = V_{GS} = 20$	**+7**	+15	**+8**	**1.35**	0.661	-0.693
061202 A350-5	$V_{DS} = V_{GS} = 10$	+2	+6	+4	**1.19**	**1.12**	-0.0693
061206 A175-2	$V_{DS} = V_{GS} = 10$	-1	+2	+3	0.491	0.481	-0.0100
061206 A250-2	$V_{DS} = V_{GS} = 10$				**N/A**		
061206 B175-1	$V_{DS} = V_{GS} = 30$	0	+2	+2	0.424	0.537	**+0.113**
061206 B250-5	$V_{DS} = V_{GS} = 20$	-1	+2	+3	**0.708**	0.661	-0.0471
061206 B300-3	$V_{DS} = V_{GS} = 30$				**N/A**		
061206 B300-4	$V_{DS} = V_{GS} = 10$	+1	+3	+2	0.659	0.537	-0.122
June202007 1-1-1	$V_{DS} = V_{GS} = 20$	**+4**	+13	**+9**	0.672	0.624	-0.0481
June202007 1-2-1	$V_{DS} = V_{GS} = 30$	+3	+16	**+13**	0.517	0.566	**+0.0493**
June202007 1-2-2	$V_{DS} = V_{GS} = 30$	+1	+19	**+18**	0.676	0.292	-0.385
June202007 1-4-1	$V_{DS} = V_{GS} = 30$	-2	+3	+5	0.507	**1.07**	**+0.561**
June202007 1-6-1	$V_{DS} = V_{GS} = 30$				**N/A**		
June202007 2-1-2	$V_{DS} = V_{GS} = 20$	+2	+14	**+12**	0.529	**0.852**	-0.323
June202007 2-2-1	$V_{DS} = V_{GS} = 30$	**+3**	+21	**+18**	**0.898**	0.540	-0.358
June202007 2-3-1	$V_{DS} = V_{GS} = 20$	+2	+13	**+11**	**0.865**	0.596	-0.269
June202007 2-3-2	$V_{DS} = V_{GS} = 30$	+1	+11	**+10**	0.689	**0.781**	**+0.0925**
June202007 3-1-1	$V_{DS} = V_{GS} = 10$	+1	+6	+5	0.674	0.559	-0.115
June202007 3-2-1	$V_{DS} = V_{GS} = 30$	+1	+8	+7	0.590	**0.709**	-0.119
June202007 3-3-1	$V_{DS} = V_{GS} = 30$	+1	+8	+7	**0.715**	0.525	-0.190
June202007 3-4-1	$V_{DS} = V_{GS} = 30$	+1	+7	+6	0.611	**0.855**	**+0.244**
July132007 1-2-2	$V_{DS} = V_{GS} = 30$	-1	0	+1	**0.804**	**1.176**	**+0.372**
July132007 1-3-2	$V_{DS} = V_{GS} = 20$	0	+4	+4	0.482	0.412	-0.0705
July132007 1-4-1	$V_{DS} = V_{GS} = 30$	+1	+4	+3	0.672	0.577	-0.0947
July132007 1-4-3	$V_{DS} = V_{GS} = 30$	+1	+3	+2	0.635	0.539	-0.0959
July132007 1-5-1	$V_{DS} = V_{GS} = 30$	0	+5	+5	0.684	0.622	-0.0622
July132007 1-6-2	$V_{DS} = 30, V_{GS} = 20$	-1	0	+1	**0.954**	**1.176**	**+0.222**
July132007 1-6-3	$V_{DS} = 10, V_{GS} = 30$	-1	0	+1	0.636	**1.071**	**+0.435**
July132007 2-1-2	$V_{DS} = V_{GS} = 30$	+1	+4	+3	0.491	0.607	**+0.116**
July132007 2-2-4	$V_{DS} = V_{GS} = 30$	0	+2	+2	0.449	0.435	-0.0141
July132007 2-3-3	$V_{DS} = V_{GS} = 30$	0	+4	+4	0.649	0.501	-0.148

Table 8.1: Summary of the turn-on voltage shift and transfer curve degradation before and after constant-voltage bias-stress testing. Provided information includes the sample name, stress condition, initial turn-on voltage (t = 0 s), final turn-on voltage value (t = 10^5 s), turn-on voltage shift, initial subthreshold swing (t = 0 s), final subthreshold swing (t = 10^5 s), and subthreshold swing change. The turn-on voltage shift is given as the final value subtracted from the initial turn-on voltage value. Subthreshold swing is defined as the minimum value of $\left(\frac{\partial V_G}{\partial \log_{10} I_D}\right)^{-1}$ at a gate voltage just beyond the turn-on voltage. Values greater than 4 V, 8 V, 0.7, and positive values are highlighted in the initial turn-on voltage, turn-on voltage shift, initial/final subthreshold swing, and subthreshold voltage swing change, respectively.

Condition		Hysteresis			Other degradation
Sample	Stress [V]	Initial	Final	Change	
061202 A250-1	$V_{DS} = V_{GS} = 30$	-0.442	-0.681	-0.239	
061202 A300-5	$V_{DS} = V_{GS} = 20$	-0.520	-0.313	**+0.208**	
061202 A350-5	$V_{DS} = V_{GS} = 10$	-0.307	**-0.0689**	**+0.238**	Kink
061206 A175-2	$V_{DS} = V_{GS} = 10$	-0.489	-0.507	-0.0181	
061206 A250-2	$V_{DS} = V_{GS} = 10$			**N/A**	
061206 B175-1	$V_{DS} = V_{GS} = 30$	-0.915	-0.470	**+0.446**	
061206 B250-5	$V_{DS} = V_{GS} = 20$	-0.795	**-0.368**	**+0.427**	
061206 B300-3	$V_{DS} = V_{GS} = 30$			**N/A**	
061206 B300-4	$V_{DS} = V_{GS} = 10$	**-0.182**	**-0.186**	**+0.00327**	
June202007 1-1-1	$V_{DS} = V_{GS} = 20$	-1.41	-0.624	**+0.764**	
June202007 1-2-1	$V_{DS} = V_{GS} = 30$	-0.802	-2.35	-1.55	
June202007 1-2-2	$V_{DS} = V_{GS} = 30$	-0.800	-1.37	-0.569	
June202007 1-4-1	$V_{DS} = V_{GS} = 30$	-0.879	-1.58	-0.699	
June202007 1-6-1	$V_{DS} = V_{GS} = 30$			**N/A**	
June202007 2-1-2	$V_{DS} = V_{GS} = 20$	-1.32	-1.57	-0.243	
June202007 2-2-1	$V_{DS} = V_{GS} = 30$	-1.04	-1.31	-0.268	
June202007 2-3-1	$V_{DS} = V_{GS} = 20$	-0.94	-1.26	-0.318	
June202007 2-3-2	$V_{DS} = V_{GS} = 30$	-0.391	-0.778	-0.386	
June202007 3-1-1	$V_{DS} = V_{GS} = 10$	-1.30	-0.301	**+0.999**	
June202007 3-2-1	$V_{DS} = V_{GS} = 30$	-0.456	-0.381	**+0.0754**	
June202007 3-3-1	$V_{DS} = V_{GS} = 30$	**-0.239**	-0.624	-0.385	
June202007 3-4-1	$V_{DS} = V_{GS} = 30$	-0.419	-0.326	**+0.0933**	Kink
July132007 1-2-2	$V_{DS} = V_{GS} = 30$	**-0.0723**	**-0.0732**	-0.000906	
July132007 1-3-2	$V_{DS} = V_{GS} = 20$	-1.13	**-0.202**	**+0.930**	
July132007 1-4-1	$V_{DS} = V_{GS} = 30$	**-0.233**	**-0.125**	**+0.108**	
July132007 1-4-3	$V_{DS} = V_{GS} = 30$	**-0.136**	**-0.143**	-0.00682	
July132007 1-5-1	$V_{DS} = V_{GS} = 30$	-0.309	**-0.254**	**+0.0547**	
July132007 1-6-2	$V_{DS} = 30, V_{GS} = 20$	-0.0915	-0.0677	**+0.0239**	Kink
July132007 1-6-3	$V_{DS} = 10, V_{GS} = 30$	**-0.173**	-0.0551	**+0.117**	Kink
July132007 2-1-2	$V_{DS} = V_{GS} = 30$	**-0.237**	-0.307	-0.0695	
July132007 2-2-4	$V_{DS} = V_{GS} = 30$	**-0.217**	-0.301	-0.0831	
July132007 2-3-3	$V_{DS} = V_{GS} = 30$	-0.475	**-0.118**	**+0.357**	

Table 8.2: Summary of the extent of hysteresis before and after constant-voltage bias-stress testing. Provided information includes the sample name, stress condition, initial hysteresis (t = 0 s), final hysteresis (t = 10^5 s), change in hysteresis, and comments related to transfer curve degradation. Hysteresis is given as the minimum difference in the drain current value when plotted on a log scale, i.e., $H_{I_D} = \mathrm{sgn}\left[\log_{10} I_D^{\,NEGATIVE} - \log_{10} I_D^{\,POSITIVE}\right] \max\left|\log_{10} I_D^{\,NEGATIVE} - \log_{10} I_D^{\,POSITIVE}\right|$. Since all the hysteresis appeared in this testing are clockwise, which implies the values are negative, a positive value in hysteresis change indicates that the hysteresis becomes narrower after stressing, while a negative hysteresis means that stress broadens the hysteresis loop. Highlighted numbers in the initial and final hysteresis columns indicate available a value larger than 0.3 V, while highlighted positive numbers in the hysteresis change column mean that hysteresis is reduced after stressing.

Condition		Drain current value [A]		Decrease [%]
Sample	Stress [V]	Initial	Final	
061202 A250-1	$V_{DS} = V_{GS} = 30$	**50.1514 µ**	0.0565085 µ	**99.8873**
061202 A300-5	$V_{DS} = V_{GS} = 20$	**28.4859 µ**	0.654104 µ	**97.7038**
061202 A350-5	$V_{DS} = V_{GS} = 10$	**86.8384 µ**	21.8763 µ	**74.808**
061206 A175-2	$V_{DS} = V_{GS} = 10$	111.866 µ	53.3672 µ	52.2936
061206 A250-2	$V_{DS} = V_{GS} = 10$	39.9847 µ	29.8872 µ	25.2534
061206 B175-1	$V_{DS} = V_{GS} = 30$	1.6405 m	1.42155 m	13.3465
061206 B250-5	$V_{DS} = V_{GS} = 20$	280.783 µ	208.633 µ	25.696
061206 B300-3	$V_{DS} = V_{GS} = 30$	1.52751 m	1.3287 m	13.0153
061206 B300-4	$V_{DS} = V_{GS} = 10$	30.9235 µ	19.7968 µ	35.9814
June202007 1-1-1	$V_{DS} = V_{GS} = 20$	**242.362 µ**	14.2909 µ	**94.1035**
June202007 1-2-1	$V_{DS} = V_{GS} = 30$	1.14361 m	0.33078 m	**71.0758**
June202007 1-2-2	$V_{DS} = V_{GS} = 30$	1.14087 m	0.271976 m	**76.1606**
June202007 1-4-1	$V_{DS} = V_{GS} = 30$	1.63624 m	0.430563 m	**73.6858**
June202007 1-6-1	$V_{DS} = V_{GS} = 30$	1.52427 m	0.70783 m	53.5627
June202007 2-1-2	$V_{DS} = V_{GS} = 20$	**290.977 µ**	45.5924 µ	**84.3313**
June202007 2-2-1	$V_{DS} = V_{GS} = 30$	0.715700 m*	0.123391 m	**82.759**
June202007 2-3-1	$V_{DS} = V_{GS} = 20$	**279.551 µ**	53.2294 µ	**80.959**
June202007 2-3-2	$V_{DS} = V_{GS} = 30$	0.909927 m	0.295883 m	67.4828
June202007 3-1-1	$V_{DS} = V_{GS} = 10$	**44.9098 µ**	6.82529 µ	**84.8022**
June202007 3-2-1	$V_{DS} = V_{GS} = 30$	1.16331 m	0.726776 m	37.5252
June202007 3-3-1	$V_{DS} = V_{GS} = 30$	1.40508 m	0.866902 m	38.3023
June202007 3-4-1	$V_{DS} = V_{GS} = 30$	1.32292 m	0.619134 m	53.1994
July132007 1-2-2	$V_{DS} = V_{GS} = 30$	1.75848 m	1.45354 m	17.3411
July132007 1-3-2	$V_{DS} = V_{GS} = 20$	0.462539 m	0.329499 m	28.763
July132007 1-4-1	$V_{DS} = V_{GS} = 30$	1.37258 m	1.15387 m*	15.9342
July132007 1-4-3	$V_{DS} = V_{GS} = 30$	1.35584 m	1.24872 m	7.90064
July132007 1-5-1	$V_{DS} = V_{GS} = 30$	1.21286 m	0.894667 m	26.2349
July132007 1-6-2	$V_{DS} = 30, V_{GS} = 20$	0.563192 m	0.4135130 m*	26.5769
July132007 1-6-3	$V_{DS} = 10, V_{GS} = 30$	0.90304 m	0.742374 m	17.7917
July132007 2-1-2	$V_{DS} = V_{GS} = 30$	1.49888 m	1.22536 m	18.2483
July132007 2-2-4	$V_{DS} = V_{GS} = 30$	0.916957m	0.803572 m	12.3654
July132007 2-3-3	$V_{DS} = V_{GS} = 30$	1.51708 m	1.181000 m	22.1531

Table 8.3: Summary of drain current shift for constant-voltage bias-stress testing experiments. Provided information includes the sample name, stress condition, initial drain current (t = 0 s), final drain current (t = 10^5 s), and percentage decrease of drain current (= ΔI_D / I_{D0}). Highlighted numbers in the initial drain current column are smaller than 500 µA and highlighted numbers in the drain current decrease column are larger than 70%. The asterisk shown in the cell represents the value is the minimum or maximum value recorded immediately before or after the initial or final plot, respectively.

8.1.2 No-Bias Room Temperature Recovery

Condition			Pre-stress recovery [V]			Post-stress recovery [V]		
Sample	Stress [V]	RxPrd [Days]	PreS	PostR	Δ	PostS	PostR	Δ
061202 A300-5	$V_{GS} = V_{DS} = 20$ V	7	+7	+9	+2	+15	+9	-6
061202 A350-5	$V_{GS} = V_{DS} = 10$ V	14	+2	+3	+1	+6	+3	-3
061206 A250-1	$V_{GS} = V_{DS} = 30$ V	63	+1	-1	-2	+3	-1	-4
061206 B175-1	$V_{GS} = V_{DS} = 30$ V	47	0	0	0	+4	0	-4
	$V_{GS} = V_{DS} = 10$ V	25	0	-1	-1	+2	-1	-3
061206 B250-5	$V_{GS} = V_{DS} = 20$ V	7	-1	+1	+2	+2	+1	-1

Table 8.4: A summary of turn-on voltage recovery. The column for pre-stress recovery represents the comparison of turn-on voltages between in the pre-stress state and in the post-relaxation state, showing how well the sample reproduces the pre-stress characteristic. The column for post-stress recovery represents the comparison of turn-on voltages between in the post-stress state and in the post-relaxation state, presenting how much the sample recovered from the post-stres state. Abbreviated terms such as RxPrd, PreS, PostR, and PostS stand for relaxation period, pre-stress, post-relaxation, and post-stress, respectively.

Sample	Condition: Stress [V]	RxPrd [Days]	Pre-stress recovery: PreS	Pre-stress recovery: PostR	Pre-stress recovery: Δ	Post-stress recovery: PostS	Post-stress recovery: PostR	Post-stress recovery: Δ
061202 A300-5	$V_{GS} = V_{DS} = 20$ V	7	1.35	1.35	0	0.661	1.35	+0.693
061202 A350-5	$V_{GS} = V_{DS} = 10$ V	14	1.19	1.58	+0.398	1.12	1.58	+0.468
061206 A250-1	$V_{GS} = V_{DS} = 30$ V	63	0.606	0.600	-0.00673	0.549	0.600	+0.0503
061206 B175-1	$V_{GS} = V_{DS} = 30$ V	47	0.521	0.424	-0.0969	0.482	0.424	-0.0579
	$V_{GS} = V_{DS} = 10$ V	25	0.424	0.551	+0.127	0.537	0.551	+0.0137
061206 B250-5	$V_{GS} = V_{DS} = 20$ V	7	0.708	0.740	+0.0325	0.661	0.740	+0.0796

Table 8.5: A summary of sub-threshold swing recovery. The column for pre-stress recovery represents the comparison of turn-on voltages between in the pre-stress state and in the post-relaxation state. The column for post-stress recovery represents the comparison of subthreshold swings between in the post-stress state and in the post-relaxation state. Subthreshold swing is provided as the minimum value of $\left(\frac{\partial V_G}{\partial \log_{10} I_D}\right)^{-1}$ at the gate voltage higher than the turn-on voltage. Abbreviated terms such as RxPrd, PreS, PostR, and PostS stand for relaxation period, pre-stress, post-relaxation, and post-stress, respectively.

Sample	Condition: Stress [V]	RxPrd [Days]	Pre-stress recovery: PreS	Pre-stress recovery: PostR	Pre-stress recovery: Δ	Post-stress recovery: PostS	Post-stress recovery: PostR	Post-stress recovery: Δ
061202 A300-5	$V_{GS} = V_{DS} = 20$ V	7	-0.520	-1.55	-1.03	-0.313	-1.55	-1.23
061202 A350-5	$V_{GS} = V_{DS} = 10$ V	14	-0.307	-0.206	+0.100	-0.0833	-0.206	-0.123
061206 A250-1	$V_{GS} = V_{DS} = 30$ V	63	-0.660	-0.390	+0.270	-0.375	-0.390	-0.0145
061206 B175-1	$V_{GS} = V_{DS} = 30$ V	47	-1.96	-0.915	+1.05	-0.553	-0.915	-0.362
	$V_{GS} = V_{DS} = 10$ V	25	-0.915	-0.193	+0.722	-0.172	-0.193	-0.0214
061206 B250-5	$V_{GS} = V_{DS} = 20$ V	7	-0.795	-0.460	+0.335	-0.368	-0.460	-0.0925

Table 8.6: A summary of hysteresis recovery. The column for pre-stress recovery represents the comparison of hystereses between in the pre-stress state and in the post-relaxation state. Notice that the hysteresis is given as the minimum difference in the drain current value in log scale, which is $H_{I_D} = \mathrm{sgn}\left[I_D^{\ NEGATIVE} - I_D^{\ POSITIVE}\right]\max\left|I_D^{\ NEGATIVE} - I_D^{\ POSITIVE}\right|$, not as a difference in time at the same drain current value due to the difficulty to obtain the data at the same current value. The negative sign of the difference of hysteresis implies that the hysteresis becomes narrower after the stress, while the positive sign means the hysteresis becomes wider after the stress. The column for post-stress recovery represents the comparison of turn-on voltages between in the post-stress state and in the post-relaxation state. Abbreviated terms such as RxPrd, PreS, PostR, and PostS stand for relaxation period, pre-stress, post-relaxation, and post-stress, respectively.

8.1.3 Accelerated Recovery

Sample	Conditions		
	1st stressing	Resetting	2nd stressing
061206 B250-5*	$V_{GS} = V_{DS} = 20$ V	$V_G = V_D = V_S = 0$ V Temp = 50 °C	$V_{GS} = V_{DS} = 20$ V
June202007 1-2-2	$V_{GS} = V_{DS} = 30$ V	$V_G = V_D = V_S = 0$ V Temp = 75 °C	$V_{GS} = V_{DS} = 30$ V
June202007 1-4-1	$V_{GS} = V_{DS} = 30$ V	$V_G = V_D = V_S =$: open, Temp = 150 °C	$V_{GS} = V_{DS} = 30$ V
June202007 2-2-1	$V_{GS} = V_{DS} = 30$ V	$V_G = V_D = V_S = 0$ V Temp = 100 °C	$V_{GS} = V_{DS} = 30$ V
June202007 2-3-2	$V_{GS} = V_{DS} = 30$ V	$V_G = V_D = V_S = 0$ V Temp = 50 °C	$V_{GS} = V_{DS} = 30$ V
July132007 1-2-2	$V_{GS} = V_{DS} = 30$ V	$V_G = V_D = V_S = 0$ V Temp = 50 °C	$V_{GS} = V_{DS} = 30$ V
July132007 1-3-2	$V_{GS} = V_{DS} = 20$ V	$V_G = V_D = V_S =$: open, Temp = 50 °C	$V_{GS} = V_{DS} = 20$ V
July132007 1-4-3	$V_{GS} = V_{DS} = 30$ V	$V_G = V_D = V_S = 0$ V Temp = 100 °C	$V_{GS} = V_{DS} = 30$ V
July132007 2-1-2	$V_{GS} = V_{DS} = 30$ V	$V_G = V_D = V_S = 0$ V Temp = 100 °C	$V_{GS} = V_{DS} = 30$ V
July132007 2-3-3	$V_{GS} = V_{DS} = 30$ V	$V_D = V_S = 0$ V, $V_G = -10$ V Temp = 100 °C	$V_{GS} = V_{DS} = 30$ V

Table 8.7: A summary of thermal resetting procedure conditions. The asterisk attached on the sample 061206 B250-5 represents the thermal resetting procedure is applied after the zero-bias room temperature recovery procedure, i.e. the sample is thermally reset a week after the first stress.

Condition		Pre-stress recovery [V]			Post-stress recovery [V]		
Sample	**Resetting Conditions**	**PreS**	**PostR**	**Δ**	**PostS**	**PostR**	**Δ**
061206 B250-5	$V_G = V_D = V_S = 0$ V Temp = 50 °C	-1	-1	0	+2	-1	**-3**
June202007 1-2-2	$V_G = V_D = V_S = 0$ V Temp = 75 °C	+1	0	-1	+19	0	**-19**
June202007 1-4-1	$V_G = V_D = V_S =$: open, Temp = 150 °C	-2	+2	+4	+3	+2	**-1**
June202007 2-2-1	$V_G = V_D = V_S = 0$ V Temp = 100 °C	+3	0	-3	+21	0	**-21**
June202007 2-3-2	$V_G = V_D = V_S = 0$ V Temp = 50 °C	+1	0	-1	+11	0	**-11**
July132007 1-2-2	$V_G = V_D = V_S = 0$ V Temp = 50 °C	-1	0	+1	0	0	**0**
July132007 1-3-2	$V_G = V_D = V_S =$: open, Temp = 50 °C	0	+2	+2	+4	+2	**-2**
July132007 1-4-3	$V_G = V_D = V_S = 0$ V Temp = 100 °C	+1	0	-1	+3	0	**-3**
July132007 2-1-2	$V_G = V_D = V_S = 0$ V Temp = 100 °C	+1	0	-1	+4	0	**-4**
July132007 2-3-3	$V_D = V_S = 0$ V, $V_G = -10$ V Temp = 100 °C	0	-14	-14	+4	-14	**-18**

Table 8.8: A summary of turn-on voltage recovery. The column for pre-stress recovery represents the comparison of turn-on voltages between in the pre-stress state and in the post-relaxation state. The column for post-stress recovery represents the comparison of turn-on voltages between in the post-stress state and in the post-relaxation state. PreS, PostR, and PostS stands for pre-stress, post-relaxation, and post-stress, respectively. Notice that July132007 2-3-3 which is stressed with $V_G = -10$ V shows a large negative turn-on voltage shift.

Condition		Pre-stress recovery [V]			Post-stress recovery [V]		
Sample	**Resetting Conditions**	**PreS**	**PostR**	**Δ**	**PostS**	**PostR**	**Δ**
061206 B250-5	$V_G = V_D = V_S = 0$ V Temp = 50 °C	0.708	0.779	+0.0717	0.661	0.779	+0.119
June202007 1-2-2	$V_G = V_D = V_S = 0$ V Temp = 75 °C	0.676	0.668	-0.00823	0.292	0.668	+0.376
June202007 1-4-1	$V_G = V_D = V_S$ =: open, Temp = 150 °C	0.507	0.486	-0.0201	1.07	0.486	-0.582
June202007 2-2-1	$V_G = V_D = V_S = 0$ V Temp = 100 °C	0.898	0.948	+0.0505	0.540	0.948	+0.408
June202007 2-3-2	$V_G = V_D = V_S = 0$ V Temp = 50 °C	0.689	0.825	+0.136	0.781	0.825	+0.0433
July132007 1-2-2	$V_G = V_D = V_S = 0$ V Temp = 50 °C	0.804	0.543	-0.260	1.18	0.543	-0.632
July132007 1-3-2	$V_G = V_D = V_S$ =: open, Temp = 50 °C	0.482	0.671	+0.189	0.412	0.671	+0.259
July132007 1-4-3	$V_G = V_D = V_S = 0$ V Temp = 100 °C	0.635	0.441	-0.194	0.539	0.441	-0.0983
July132007 2-1-2	$V_G = V_D = V_S = 0$ V Temp = 100 °C	0.491	0.525	+0.0341	0.607	0.525	-0.0822
July132007 2-3-3	$V_D = V_S = 0$ V, $V_G = -10$ V Temp = 100 °C	0.649	**1.75**	**+1.10**	0.501	**1.75**	**+1.25**

Table 8.9: A summary of sub-threshold swing recovery. Subthreshold swing is provided as the minimum value of $\left(\frac{\partial V_G}{\partial \log_{10} I_D}\right)^{-1}$ at the gate voltage higher than the turn-on voltage. The column for pre-stress recovery represents the comparison of turn-on voltages between in the pre-stress state and in the post-relaxation state. The column for post-stress recovery represents the comparison of subthreshold swings between in the post-stress state and in the post-relaxation state. PreS, PostR, and PostS stands for pre-stress, post-relaxation, and post-stress, respectively. Notice that July132007 2-3-3 which is stressed with $V_G = -10$ V shows severe degradation.

Condition		Pre-stress recovery			Post-stress recovery		
Sample	**Resetting Conditions**	**PreS**	**PostR**	**Δ**	**PostS**	**PostR**	**Δ**
061206 B250-5	$V_G = V_D = V_S = 0$ V Temp = 50 °C	-0.795	-0.399	+0.3 96	- 0.368	-0.399	- 0.031 7
June202007 1-2-2	$V_G = V_D = V_S = 0$ V Temp = 75 °C	-0.800	-0.820	- 0.02 03	-1.37	-0.820	+0.54 9
June202007 1-4-1	$V_G = V_D = V_S =$: open, Temp = 150 °C	-0.879	-0.736	+0.1 44	-1.58	-0.736	+0.84 3
June202007 2-2-1	$V_G = V_D = V_S = 0$ V Temp = 100 °C	-1.04	-0.691	+0.3 51	-1.31	-0.691	+0.61 9
June202007 2-3-2	$V_G = V_D = V_S = 0$ V Temp = 50 °C	-0.391	-0.514	- 0.12 3	- 0.778	-0.514	+0.26 3
July132007 1-2-2	$V_G = V_D = V_S = 0$ V Temp = 50 °C	- 0.072 3	- 0.0638	+0.0 0853	- 0.073 2	- 0.0638	+0.00 949
July132007 1-3-2	$V_G = V_D = V_S =$: open, Temp = 50 °C	-1.13	-0.296	+0.8 37	- 0.202	-0.296	- 0.093 2
July132007 1-4-3	$V_G = V_D = V_S = 0$ V Temp = 100 °C	-0.136	-0.122	+0.0 142	- 0.143	-0.122	+0.02 10
July132007 2-1-2	$V_G = V_D = V_S = 0$ V Temp = 100 °C	-0.237	-0.267	- 0.02 92	- 0.307	-0.267	+0.04 03
July132007 2-3-3	$V_D = V_S = 0$ V, $V_G = -10$ V Temp = 100 °C	-0.475	- 0.0233	+0.4 52	- 0.118	- 0.0233	+0.09 51

Table 8.10: A summary of hysteresis recovery. The column for pre-stress recovery represents the comparison of hystereses between in the pre-stress state and in the post-relaxation state. Notice that the hysteresis is given as the minimum difference in the drain current value in log scale, which is $H_{I_D} = \mathrm{sgn}\left[\log_{10} I_D^{\,NEGATIVE} - \log_{10} I_D^{\,POSITIVE}\right] \max\left|\log_{10} I_D^{\,NEGATIVE} - \log_{10} I_D^{\,POSITIVE}\right|$, not as a difference in time at the same drain current value due to the difficulty to obtain the data at the same current value. The negative sign of the difference of hysteresis implies that the hysteresis becomes narrower after the stress, while the positive sign means the hysteresis becomes wider after the stress. The column for post-stress recovery represents the comparison of turn-on voltages between in the post-stress state and in the post-relaxation state. PreS, PostR, and PostS stands for pre-stress, post-relaxation, and post-stress, respectively.

Condition		1st stress			2nd stress		
Sample	Stress [V]	Initial [mA]	Final [mA]	Decrease [%]	Initial [mA]	Final [mA]	Decrease [%]
061206 B250-5	$V_{GS} = V_{DS} = 20$ V	0.2808	0.2086	25.696	0.2765	0.2040	26.219
June202007 1-2-2	$V_{GS} = V_{DS} = 30$ V	1.1409	0.2720	76.161	1.2476	0.2831	77.305
June202007 1-4-1	$V_{GS} = V_{DS} = 30$ V	1.6362	0.4306	73.686	1.4114	0.6647	52.902
June202007 2-2-1	$V_{GS} = V_{DS} = 30$ V	0.7157*	0.1234	82.759	1.1148	0.4501	59.626
June202007 2-3-2	$V_{GS} = V_{DS} = 30$ V	0.9099	0.2959	67.483	0.9896	0.2544	74.295
July132007 1-2-2	$V_{GS} = V_{DS} = 30$ V	1.7585	1.4535	17.341	1.6624	1.4133	14.989
July132007 1-3-2	$V_{GS} = V_{DS} = 20$ V	0.4625	0.3295	28.763	0.4437	0.3047	31.333
July132007 1-4-3	$V_{GS} = V_{DS} = 30$ V	1.3558	1.2487	7.9006	1.2956	1.1068	14.578
July132007 2-1-2	$V_{GS} = V_{DS} = 30$ V	1.4989	1.2254	18.248	1.4206	1.0694	24.725
July132007 2-3-3	$V_{GS} = V_{DS} = 30$ V	1.5171	1.1810	22.153	2.1402	1.8138	15.250

Table 8.11: A summary of the first and second stress tests. The asterisk shown on the initial drain current value of June202007 2-2-1 implies that the drain current increased after the stress is applied and the value used is the maximum drain current value instead of the actual initial drain current value.

8.2 Application of a Stretched Exponential to Drain Current Degradation

As discussed in Subsection 6.3.4, drain current degradation as a function of time may be expressed in the stretched exponential format,

$$I_D(t) = I_{D0} \exp\left[-\left(t/\tau\right)^{\beta}\right], \tag{6.10}$$

where I_{D0} is the initial drain current value, β is a constant, which is sometimes called the Kohlrausch stretching exponent, and τ is a time constant. Equation 6.10 is recast by taking logarithm of both sides of this equation,

$$-\log_{10} I_D/I_{D0} = \left(t/\tau\right)^{\beta} \log_{10} e. \tag{8.1}$$

Once again taking the logarithm, Eq. 8.1 is reformulated into the following expression,

$$\log_{10}\left(-\log_{10} I_D/I_{D0}\right) = \beta \log_{10} t - \beta \log_{10} \tau + \log_{10}\left(\log_{10} e\right). \tag{8.2}$$

An example of constant-voltage bias-stress $I_D - \log_{10}(t)$ data is plotted in Fig. 8.1 (a) in conjunction with the same set of data replotted according to Eq. 8.1 in Fig. 8.1 (b) and according to Eq. 6.5 in Fig .8.1 (c). As clearly shown in Fig. 8.1 (c), some of the empirical data of constant-voltage bias-stress testing follow the stretched exponential rule.

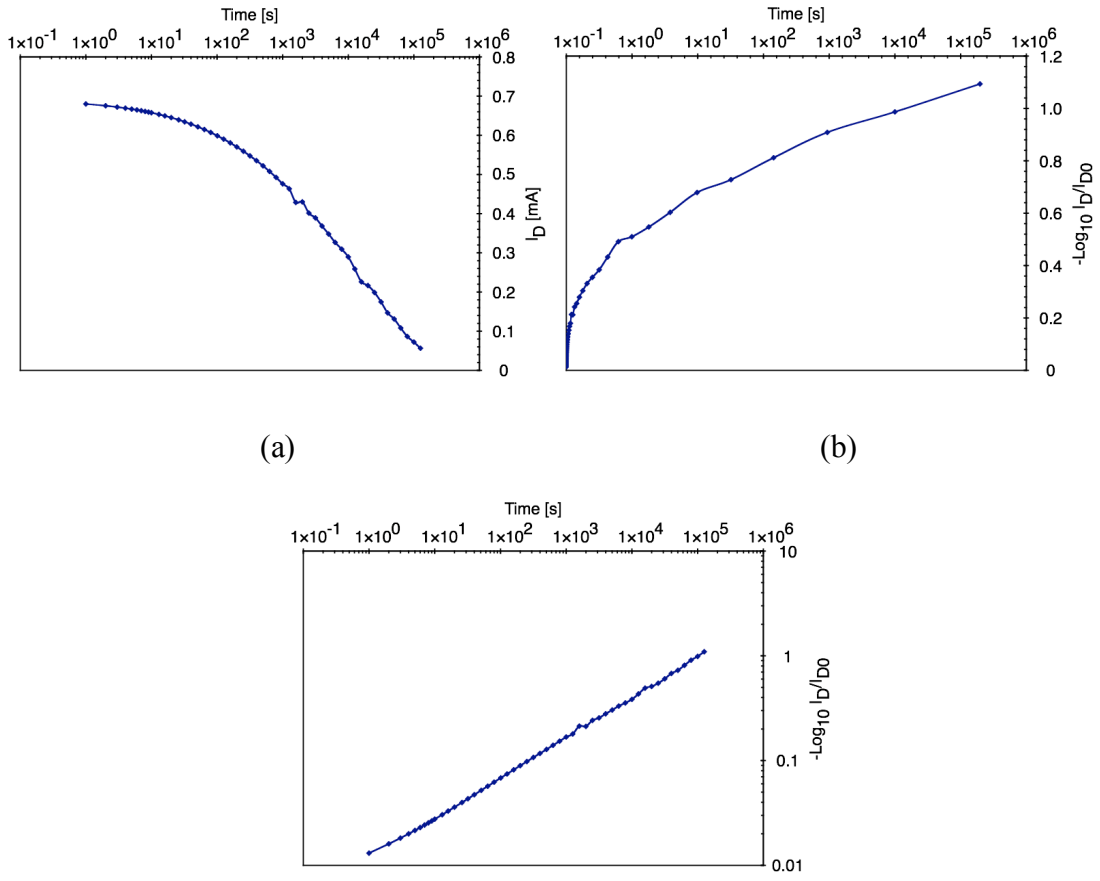


Figure 8.1: One set of constant-voltage bias-stress test data plotted in three different ways: (a) I_D – $\log_{10}(t)$, (b) $-\log_{10} I_D/I_{D0}$ – $\log_{10}(t)$ as per Eq. 8.1, and (c) $\log_{10}\left(-\log_{10} I_D/I_{D0}\right)$ – $\log_{10}(t)$ as per Eq. 8.1. If the data is consistent with Eq. 6.10, plot (c) should yield a straight line. The sample shown here is 061202 A350-1. Refer to Table 3.2 for detailed information regarding this sample.

Although majority of the TFTs tested exhibit a continuous characteristic on a stretched exponential plot, some of the data sets do not exhibit the simple, linear behavior displayed in Fig. 8.2 (c). For assessment purposes, these sets are classified into one of the following categories indicated in Fig. 8.2:

1. a straight line,
2. multiple straight lines,
3. a continuous wavy line, or

4. a noisy data set.

A summary of the distribution of drain current decay data sets according to this classification scheme is provided in Fig. 8.3. As shown in (a) of the figure, a majority of devices appear to be a single or a combination of several straight lines. A complete list of the stretched exponential plot types and corresponding device names is provided in Table 8.12.

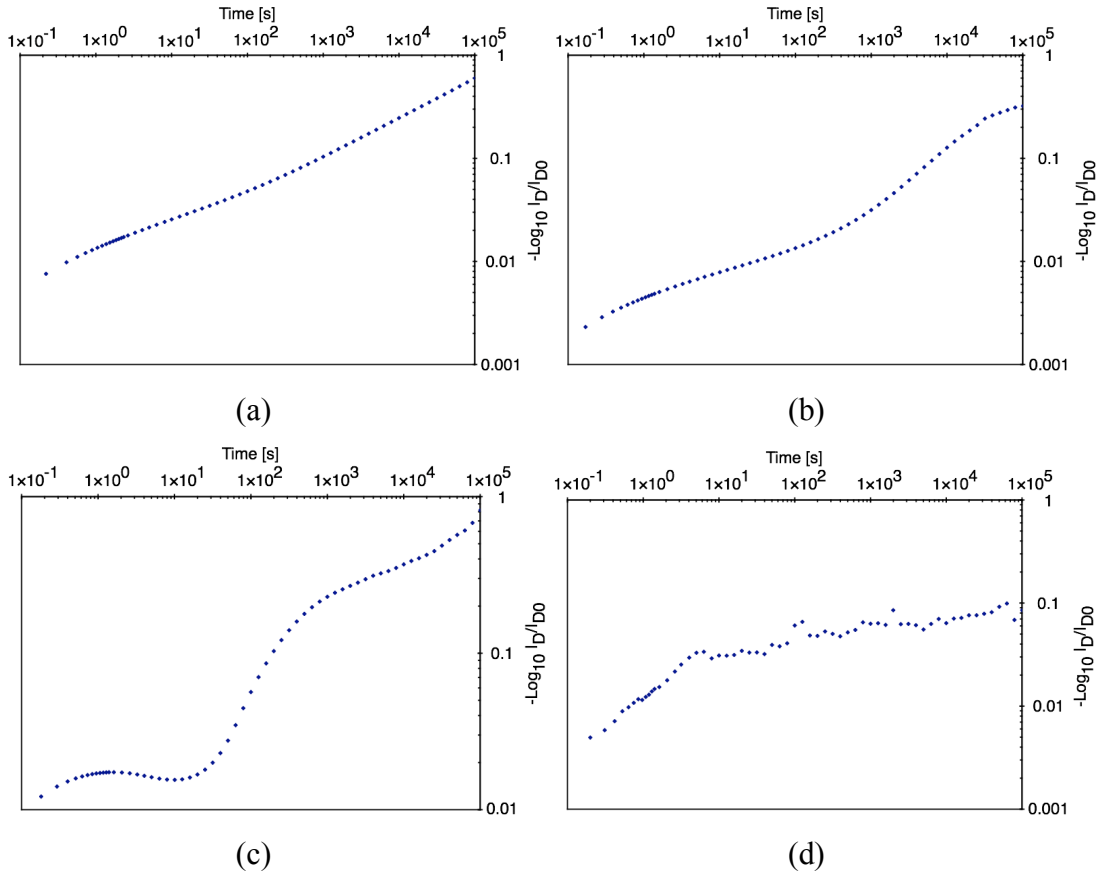
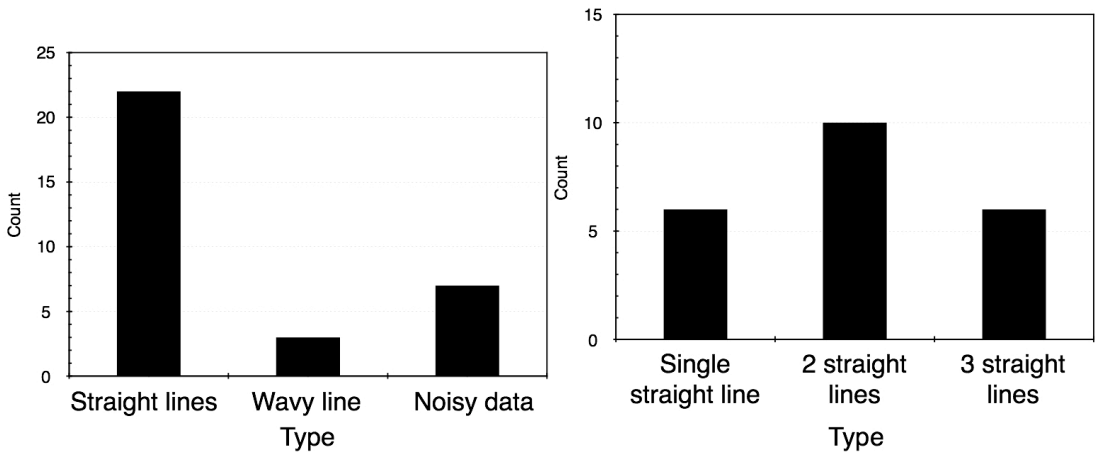


Figure 8.2: Four types of drain current trend monitored replotted using the stretched exponential format as specified by Eq. 8.2: (a) a straight line, (b) multiple straight lines, (c) a continuous wavy line, and (d) a noisy data set. The samples used for each plot are (a) 061202 A350-5, (b) 061206 A175-2, (c) June202007 3-1-1, and (d) July132007 1-6-3.



(a) (b)

Figure 8.3: Distribution of drain current decay trends when plotted using a stretched exponential format, Eq. 4.4. (a) Distribution according to the classification scheme introduced in Fig. 8.2. Most of the TFTs tested yield straight-line characteristics. (b) Distribution of TFTs displaying straight line drain current decay characteristics.

Condition		Type	Note
Sample	Stress [V]		
061202 A250-1	$V_{DS} = V_{GS} = 30$	2 straight lines	
061202 A300-5	$V_{DS} = V_{GS} = 20$	2 straight lines	
061202 A350-5	$V_{DS} = V_{GS} = 10$	2 straight lines	
061206 A175-2	$V_{DS} = V_{GS} = 10$	3 straight lines	
061206 A250-2	$V_{DS} = V_{GS} = 10$	2 straight lines	
061206 B175-1	$V_{DS} = V_{GS} = 30$	2 straight lines	
061206 B250-5	$V_{DS} = V_{GS} = 20$	3 straight lines	
061206 B300-3	$V_{DS} = V_{GS} = 30$	Single straight line	
061206 B300-4	$V_{DS} = V_{GS} = 10$	3 straight lines	
June202007 1-1-1	$V_{DS} = V_{GS} = 20$	2 straight lines	
June202007 1-2-1	$V_{DS} = V_{GS} = 30$	2 straight lines	
June202007 1-2-2	$V_{DS} = V_{GS} = 30$	2 straight lines	
June202007 1-4-1	$V_{DS} = V_{GS} = 30$	Noisy data	
June202007 1-6-1	$V_{DS} = V_{GS} = 30$	Noisy data	
June202007 2-1-2	$V_{DS} = V_{GS} = 20$	3 straight lines	
June202007 2-2-1	$V_{DS} = V_{GS} = 30$	Single straight line	
June202007 2-3-1	$V_{DS} = V_{GS} = 20$	2 straight lines	
June202007 2-3-2	$V_{DS} = V_{GS} = 30$	Single straight line	
June202007 3-1-1	$V_{DS} = V_{GS} = 10$	Wavy line	
June202007 3-2-1	$V_{DS} = V_{GS} = 30$	Noisy data	
June202007 3-3-1	$V_{DS} = V_{GS} = 30$	2 straight lines	
June202007 3-4-1	$V_{DS} = V_{GS} = 30$	Wavy line	
July132007 1-2-2	$V_{DS} = V_{GS} = 30$	Noisy data	
July132007 1-3-2	$V_{DS} = V_{GS} = 20$	3 straight lines	
July132007 1-4-1	$V_{DS} = V_{GS} = 30$	Noisy data	
July132007 1-4-3	$V_{DS} = V_{GS} = 30$	Single straight line	Increase in drain current
July132007 1-5-1	$V_{DS} = V_{GS} = 30$	3 straight lines	
July132007 1-6-2	$V_{DS} = 30, V_{GS} = 20$	Single straight line	
July132007 1-6-3	$V_{DS} = 10, V_{GS} = 30$	Noisy data	
July132007 2-1-2	$V_{DS} = V_{GS} = 30$	Noisy data	
July132007 2-2-4	$V_{DS} = V_{GS} = 30$	Single straight line	
July132007 2-3-3	$V_{DS} = V_{GS} = 30$	Wavy line	Increase in drain current

Table 8.12: Classification of the constant-voltage bias-stress testing data sets.

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