Solar cells that are based on an intimate metal-semiconductor (Schottky) contact generally produce lower efficiencies than $p-n$ junction solar cells. However, if a thin insulating layer (< 30 Å) is introduced between the metal and the semiconductor then the dominant current transport mechanism of thermionic emission is suppressed, and a large minority carrier tunneling current may flow between the metal and the semiconductor. The metal-insulator-semiconductor (MIS) structure can produce solar cells with higher efficiencies than traditional $p-n$ junction solar cells.

This thesis presents the theory, the fabrication techniques, and the experimental results for a minority carrier MIS structure as applied to a solar cell design that seeks to reduce cost by utilizing particulate silicon grains. The MIS contact investigated is aluminum/SiO$_2$/p-Si, where the p-Si is in the form of single crystal grains with diameters of 425-800 μm. The solar cell performance as a function of the insulator thickness and the semiconductor resistivity is compared to theory. Also, the performance of the particulate silicon solar cell is compared to a similarly processed MIS structure that is created on a polished silicon wafer. The best particulate solar cell yields 6% efficiency whereas the best wafer solar cell gives 10%.
A 6% Efficient MIS Particulate Silicon Solar Cell

by

Michael Greer

A THESIS

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Master of Science

Presented March 9, 1998
Commencement June 1998
I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

Michael Greer, Author
Acknowledgment

I would like to express special gratitude to Junlin Zhou of the Mechanical Engineering Department. He fabricated a portion of every particulate solar cell produced in this research, and he was always willing and able to help. Also, I am very thankful for the assistance of Prof. Subramanian. His expertise with experimental procedures necessary in this research led me in the right direction many times. Lastly, I would like to thank both my advisor Professor James A. Van Vechten for giving me the opportunity to work on this challenging project and Komatsu for funding it.
# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>I. Introduction</th>
<th>..........................................................</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>A. Motivation for Particulate Solar Cell Research</td>
<td>..........................................................</td>
<td>1</td>
</tr>
<tr>
<td>B. The Particulate Silicon Solar Cell Patent</td>
<td>....................................................................</td>
<td>2</td>
</tr>
<tr>
<td>II. Principles of Particulate Silicon Solar Cell Operation</td>
<td>....................................................................</td>
<td>4</td>
</tr>
<tr>
<td>A. The Intimate Metal-Semiconductor Contact (Schottky Contact)</td>
<td>..........................................................</td>
<td>4</td>
</tr>
<tr>
<td>B. The Minority Carrier Metal-Insulator-Semiconductor Tunnel Diode</td>
<td>..........................................................</td>
<td>16</td>
</tr>
<tr>
<td>III. Particulate Silicon Solar Cell Design and Construction</td>
<td>....................................................................</td>
<td>23</td>
</tr>
<tr>
<td>A. Material Selection</td>
<td>..........................................................</td>
<td>23</td>
</tr>
<tr>
<td>B. PSSC Construction</td>
<td>..........................................................</td>
<td>24</td>
</tr>
<tr>
<td>IV. Experimental Results</td>
<td>....................................................................</td>
<td>29</td>
</tr>
<tr>
<td>A. $I-V$ measurement: Efficiency, Fill Factor, Ideality Factor, Series and Shunt Resistance</td>
<td>..........................................................</td>
<td>29</td>
</tr>
<tr>
<td>B. $C-V$ measurement: Doping Concentration</td>
<td>..........................................................</td>
<td>39</td>
</tr>
<tr>
<td>C. Degradation</td>
<td>....................................................................</td>
<td>42</td>
</tr>
<tr>
<td>V. Proposed Modifications to the Particulate Silicon Solar Cell</td>
<td>....................................................................</td>
<td>44</td>
</tr>
<tr>
<td>A. Dielectric Improvement</td>
<td>....................................................................</td>
<td>44</td>
</tr>
<tr>
<td>B. Zinc-Oxide Transparent Conductor with a Nonplanar Approach</td>
<td>..........................................................</td>
<td>45</td>
</tr>
<tr>
<td>C. Semiconductor Resistivity</td>
<td>....................................................................</td>
<td>47</td>
</tr>
<tr>
<td>VI. Conclusions</td>
<td>....................................................................</td>
<td>50</td>
</tr>
<tr>
<td>Bibliography</td>
<td>....................................................................</td>
<td>51</td>
</tr>
<tr>
<td>Appendix</td>
<td>....................................................................</td>
<td>53</td>
</tr>
</tbody>
</table>
### LIST OF FIGURES

<table>
<thead>
<tr>
<th>Figure</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Postulated world consumption of fossil fuel</td>
<td>1</td>
</tr>
<tr>
<td>3. Zero bias energy band diagram for a metal- $p$-type semiconductor contact with $\phi_m &lt; \phi_s$</td>
<td>5</td>
</tr>
<tr>
<td>4. Voltage bias applied to a $p$-type Schottky contact</td>
<td>6</td>
</tr>
<tr>
<td>5. Absorption coefficient for silicon, GaAs, and germanium</td>
<td>12</td>
</tr>
<tr>
<td>6. Electron-hole pair generation rate versus distance from the semiconductor computed from Eqn (14)</td>
<td>13</td>
</tr>
<tr>
<td>7. Photocurrent mechanisms in a Schottky-barrier solar cell</td>
<td>14</td>
</tr>
<tr>
<td>8. Computed internal spectral response of a silicon $p$-$n$ junction with different surface recombination velocities, $S_s$</td>
<td>16</td>
</tr>
<tr>
<td>9. Possible charge transport mechanisms for a MIS tunnel diode under forward bias</td>
<td>18</td>
</tr>
<tr>
<td>10. Zero bias energy band diagram for the Al/SiO$_2$/p-Si structure</td>
<td>19</td>
</tr>
<tr>
<td>11. Pressing the silicon grains into the aluminum substrate</td>
<td>25</td>
</tr>
<tr>
<td>12. A finished particulate silicon solar cell</td>
<td>27</td>
</tr>
<tr>
<td>13. Witness wafer cell</td>
<td>27</td>
</tr>
<tr>
<td>14. NREL characterization of a 2 x 4 cm $p$-$n$ junction solar cell with an antireflection coating</td>
<td>30</td>
</tr>
<tr>
<td>15. Dark and illuminated measured current-voltage characteristics</td>
<td>31</td>
</tr>
<tr>
<td>16. Magnified view of the illuminated current-voltage characteristics given in Fig. 15</td>
<td>32</td>
</tr>
<tr>
<td>17. Ideality factor</td>
<td>34</td>
</tr>
<tr>
<td>18. First order representation of a series and parallel resistance</td>
<td>36</td>
</tr>
<tr>
<td>Figure</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>-------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>19.</td>
<td>Determination of $R_s$ using the illuminated $I-V$ characteristics</td>
</tr>
<tr>
<td>20.</td>
<td>Experimental characteristics of the Al/SiO$_2$/p-Si (minority carrier) structure</td>
</tr>
<tr>
<td>21.</td>
<td>The assumed space charge density $\rho$, the resulting electric field magnitude $</td>
</tr>
<tr>
<td>22.</td>
<td>Measured capacitance-voltage characteristic for the 3.8% efficient PSSC</td>
</tr>
<tr>
<td>23.</td>
<td>A representative example of the degraded dark current-voltage characteristic that occurs for the PSSC and the wafer witness a few days after fabrication</td>
</tr>
<tr>
<td>24.</td>
<td>The unplanarized PSSC with a thin dielectric layer</td>
</tr>
<tr>
<td>25.</td>
<td>A textured solar cell</td>
</tr>
</tbody>
</table>
A 6% Efficient MIS Particulate Silicon Solar Cell

I. Introduction

A. Motivation for Particulate Solar Cell Research

A maturing star feeds on successive elements of the periodic table. As the supply of a given "food" element becomes scarce, and hence energetically unfavorable, the star turns to the next element in the progression. The human consumption of fuels is following a similar pattern by cycling through the fuel varieties, wood, coal, natural gas, oil, etc., turning to the next in the sequence as the previous becomes unprofitable. Only 120 years ago the principal energy source in the United States was hay and wood [1].

The exhaustion of fossil fuels appears to be transpiring in a very short time when compared to all of human history [1]. As Fig. 1 illustrates, the expected ephemeral nature of fossil fuel availability dictates that efforts be made to develop renewable energy resources such as wind, hydroelectric, geothermal, nuclear fusion, fuel from wastes, biomass, and photovoltaic.

![Fig. 1 Postulated world consumption of fossil fuel. (from Fahrenbruch and Bube [1])](image-url)
Solar energy is the "engine" which has driven the production of most energy sources utilized by man throughout human history. Sunlight is converted to biomass which over time is converted to oil, peat, natural gas, and coal. In this sense our standard energy sources are already solar energy sources. However, from purely energetic considerations, these standard energy sources yield low overall conversion efficiencies of sunlight to electricity for the end user when compared to a common photovoltaic cell which is 15% efficient. Photovoltaics are also attractive because: they produce energy immediately, they are virtually pollution and maintenance free, and they are unlikely to be exhausted like fossil fuels. Photovoltaics have their limitations too: they require large array areas to produce substantial power, they are not suitable for all locations, the low voltage direct current collected from photovoltaic cells must be converted to high voltage AC to connect to the power grid, and foremost, photovoltaics are expensive.

The high cost of single crystal semiconductor material from which photovoltaics are traditionally fabricated has kept the price of photovoltaics high. The goal of this research is to produce a low cost silicon solar cell with an efficiency greater than 5% by using waste electronic grade silicon.

B. The Particulate Silicon Solar Cell Patent

The particulate silicon solar cell (PSSC) construction is based on patent number 5,415,700 authored by John Arthur, Robert Graupner, Tyrus Monson, James Van Vechten, and Ernest Wolff. As shown in Fig. 2, the patent cell consists of a metal substrate embedded with particulate silicon grains. A dielectric material is present between the grains to both stabilize the grains and to prevent a short circuit from occurring between the metal substrate and the transparent conducting top layer. The transparent conductor forms a Schottky contact with the silicon particles and acts as a topside conductive window. The transparent conductor is an oxide semiconductor (i.e., indium-tin-oxide or zinc-oxide) which can be made highly degenerate and may reach
resistivity values as low as $2 \times 10^{-4} \ \Omega\text{-cm}$. This high electrical conductivity facilitates effective lateral current collection in the top layer resulting in less need for intricate metal front contacts often found on $p$-$n$ junction cells.

![Diagram of solar cell layers](image_url)

**Fig. 2** Solar cell illustration excerpted from US Patent 5,415,700 (May 16, 1995).

The design is motivated by the need for inexpensive solar cells and the large amount of waste electronic grade silicon grains available to produce them. Annually, silicon wafer manufacturers generate 10,000 tons of waste silicon particulates as a product of slicing silicon boules to produce wafers. These waste grains vary in doping, resistivity, and grain size. Because they are single crystal, or very nearly so, they should produce a PSSC with an efficiency (based on the *active* cell area) which is close to that of an analogous wafer cell.
A. The Intimate Metal-Semiconductor Contact (Schottky Contact)

The structure in Fig. 2 is engineered so that the photovoltaic effect occurs at the interface between the silicon grains and so that the interface between the silicon grains and the metal substrate is essentially an ohmic contact with low resistance. The interface between the silicon grains and the transparent conductor is therefore a specific type of metal-semiconductor contact, and an understanding of the nature of this contact is important because it strongly determines the performance of the device.

As a metal and a semiconductor are brought together to form an atomically sharp junction in the absence of light and applied voltage, charge transfer will occur until the Fermi levels align at thermal equilibrium. The energy band diagrams for this process are shown in Fig. 3 for a p-type semiconductor. In this case, positive charge (i.e. holes) will transfer from the semiconductor to the metal and negative charge (i.e. electrons) will transfer from the metal to the semiconductor, thereby raising the electron energies in the bulk of the semiconductor and lowering those in the metal. As shown in Fig. 3, this is equivalent to $E_c$ and $E_v$ bending upwards such that $E_{Fm}$ and $E_{Fs}$ are coincident at the system Fermi level, $E_F$. As the positive charge leaves the semiconductor it deposits itself in a thin region (~10 Å) on the metal surface leaving behind fixed, uncompensated dopant ions in the semiconductor. The thickness of the region containing these negatively charged ionized is called the depletion region, $W$, and the metal-semiconductor contact is physically similar to a $n^+p$ junction.

In Fig. 3 the energy difference between the vacuum level and the Fermi level is called the work function. It is denoted as $q\phi_m$ ($\phi_m$ in volts) for the metal and for the semiconductor is given by $q\phi_s = q(\chi + V_n)$, where $q\chi$ is the electron affinity measured from the bottom of the conduction band $E_c$ to the vacuum level, and $qV_n$ is the energy difference between $E_c$ and $E_F$. The potential barrier, $(\phi_s - \phi_m) = V_o$, which retards hole
Fig. 3 Zero bias energy band diagram for a metal-\textit{p}-type semiconductor contact with $\phi_m < \phi_s$. (adapted from Streetman [2])

diffusion from the semiconductor to the metal is called the contact potential. For an ideal contact between a metal and a \textit{p}-type semiconductor the potential barrier height, $q\phi_B = E_s - q(\phi_m - \chi)$, represents the barrier that holes must surmount in going from the metal to the semiconductor.

Figure 3 illustrates the case where the metal-\textit{p}-type semiconductor work function relationship is $\phi_m < \phi_s$, which yields a rectifying contact. The effects on the band structure of voltage biasing a \textit{p}-type Schottky barrier with no illumination are shown in Fig. 4. A forward bias is achieved by applying a positive voltage to the semiconductor with respect to the metal. This applied voltage, $V_s$, counteracts the contact potential shown in Fig. 3b, unbends the energy bands $E_c$ and $E_v$, and allows
holes to diffuse more readily across the depletion region to the metal. In reverse bias, the applied voltage enhances the band bending and therefore also the barrier to the diffusion of holes from the semiconductor to the metal. However, note that the Schottky barrier height $q\phi_B$ for an ideal contact does not change with the applied bias, therefore, the probability that a hole in the metal may surmount $q\phi_B$ is independent of the applied voltage. As a result, the reverse saturation current, due to holes in the metal surmounting the barrier into the semiconductor, is also independent of applied voltage. The net result of these considerations is that the Schottky contact leads to a rectifying contact exhibiting strong current flow with forward bias and weak current flow with reverse bias.

\[ V_a \quad + \quad + \quad V_a \]

\[ E_F^p \text{ (thermionic theory)} \]
\[ E_F^m \]
\[ q\phi_B \]
\[ W \]

(a) forward bias \hspace{2cm} (b) reverse bias

**Fig. 4** Voltage bias applied to a $p$-type Schottky contact. No illumination. (adapted from Streetman [2])
It should be noted that the Schottky barrier diode operates by injecting *majority* carriers from the semiconductor to the metal for both $n$ and $p$ type semiconductor cases. While Schottky contacts formed with $p$-type and $n$-type semiconductor are analogous to $n^+p$ and $p^+n$ junctions, respectively, the current transport mechanisms by which carriers traverse the junction are quite different for the two devices.

In a $p$-type Schottky contact, holes in the semiconductor are transported from the semiconductor bulk to the metal-semiconductor interface where they may be emitted over the barrier into the metal. While moving through the interior of the semiconductor and the depletion region, the holes are governed by the physics of diffusion and drift. When the holes arrive at the metal-semiconductor interface their movement is governed by the rate at which they are emitted across the interface. The total current is determined by which process most strongly impedes the movement of holes, and two theories for the current flow have therefore developed. Bethe's theory of thermionic-emission [3] claims that the bottleneck lies with the transfer of carriers across the metal-semiconductor interface while the diffusion theory of Schottky [4] claims that diffusion in the semiconductor bulk is more important. Diffusion theory assumes that the quasi-Fermi level for the majority carrier is not constant throughout the depletion region (Fig. 4a) and this differs strikingly from the situation in a biased $p$-$n$ junction. Additionally, the diffusion theory yields an expression for the current-voltage relationship which is not of the form for an ideal rectifier because the reverse bias current does not saturate. Perhaps this is why thermionic emission is traditionally considered the dominant mode of current transport in an ideal Schottky contact. Of course, the true current transport is determined by a combination both mechanisms and a more complicated theory from Crowell and Sze [5] considers both the thermionic emission theory and the diffusion theory simultaneously.

In the thermionic emission theory, the drift and diffusion mechanisms are assumed to be negligible, and this assumption is illustrated in Fig. 4a, where the quasi-Fermi level for holes, $E_{Fp}$, is flat throughout the semiconductor. The electron and hole densities at the semiconductor surface are governed by,
where \( N_c \) and \( N_v \) are the effective density of states in the conduction band and valence band, respectively. Inspection of Fig. 4 shows that the majority carrier concentration, \( p_s \) in Eqn. (1), can be rewritten,

\[
p_s = N_v \exp\left(-q\phi_B - V_s\right)/kT) . \tag{2}
\]

Assuming that the semiconductor has spherical constant-energy surfaces, the holes will have an isotropic Maxwellian velocity distribution, and kinetic theory implies that the number of particles incident on the insulator is \( p_s \bar{v}/4 \), where \( \bar{v} \) is the average thermal velocity of holes in the semiconductor. The current density resulting from holes travelling from the semiconductor to the metal may be written immediately [6],

\[
J_{sm} = \frac{f q \bar{v}}{4} p_s = \frac{f q \bar{v}}{4} N_v \exp\left(-q\phi_B - V_s\right)/kT) . \tag{3}
\]

where \( f \) is the fraction of the holes that can tunnel from the semiconductor to the metal. Holes may also tunnel from the metal into the semiconductor with the same probability \( f \). However, this flow of holes is independent of bias because the barrier height remains unchanged for an ideal Schottky contact,

\[
J_{ms} = \frac{f q \bar{v}}{4} N_v \exp\left(-q\phi_B / kT\right) . \tag{4}
\]

The net current is then given by,

\[
J = J_{sm} - J_{ms} \tag{5}
\]
\[ J = \frac{f q \bar{v}}{4} N_v \exp(-q \phi_b / kT) \left[ \exp \left( \frac{qV}{kT} \right) - 1 \right]. \]

where \( \bar{v} = \left( \frac{8kT \pi m^*}{\pi m^*} \right)^{1/2} \) for a Maxwellian distribution of velocities and \( m^* \) is the transport effective mass for holes in the semiconductor. Equation (5) shows that at zero bias the net current given by \( J_{nm} - J_{ms} \) is indeed zero.

An implicit assumption in thermionic-emission theory is that \( f \) may be taken as unity which means that no holes traveling toward the metal-semiconductor interface are reflected. Although this seems like an extreme assumption, Monte Carlo calculations that assume an isotropic Maxwellian velocity distribution at the depletion region edge yield a current density very close to that predicted by using \( f = 1 \) in Eqn. (5) [7]. Therefore, with \( f = 1 \) and \( N_v = 2 \left( \frac{2\pi m^* q kT h^2}{\pi m^*} \right)^{3/2} \) Eqn. (5) becomes,

\[ J = A^* T^2 \exp(-q \phi_b / kT) \left[ \exp \left( \frac{qV}{kT} \right) - 1 \right], \]  

where \( A^* = 4\pi m^* q k^2 / h^3 \). Equation (6) is the current-voltage relationship according the thermionic emission theory. Although this derivation seems simplistic, Bethe's original derivation is founded on largely intuitive reasoning. A more mathematical version the thermionic-emission derivation may be found in Sze [8].

The current-voltage expression derived from the thermionic-emission theory assumes that the barrier height for \( p \)-type semiconductor is given by

\[ q \phi_b = E_g - q(\phi_m - \chi) \]  

and, hence, is independent of bias. However, for practical Schottky contacts this is not the case due to image force lowering and nonidealities such as the presence of an interfacial layer. Experimental results for covalent semiconductors like silicon clearly show that the Schottky barrier height is much less sensitive to \( \phi_m \) than the equation for the Schottky barrier height would imply. Bardeen has suggested that this is due to interface states that are present between the metal and the semiconductor. These interface states are specified by a neutrality level, \( \phi_b \), which is measured from the top of the valence band and usually falls in the semiconductor energy gap near \( E_F \). If the
neutrality level is above $E_F$ at zero bias then the surface states contain a net positive charge. Experimentally it is found that $\phi_b \approx E_g - \phi_0$ and that for silicon, GaAs, and GaP, $\phi_0 \approx 1/3 E_g$. Therefore, in practical devices $\phi_b$ is often “pinned” at $\sim 2/3 E_g$ by a high density of surface states.

The image force lowering is due to the force between an electron in the semiconductor and the positive charge induced in the metal. When an external electric field, $E$, is applied, this attractive force causes the total potential energy of the electron to be lowered by an amount $\Delta \phi = \sqrt{qE/4\pi \varepsilon_s}$, called the image force lowering, where $\varepsilon_s$ is the semiconductor static permittivity. The effect of the image force lowering is that the Schottky barrier height is lowered to an effective barrier height of $\Delta \phi_e = \phi_b - \Delta \phi$. Notice that $\Delta \phi_e$ varies with bias because $\Delta \phi$ depends on the applied electric field and hence the applied voltage bias (see [8] pp. 250).

To calculate the effect of image force lowering on the current-voltage characteristics, assume that $\partial \phi / \partial V$ is constant so that the effective barrier height becomes,

$$\phi_e = \phi_{b0} - (\Delta \phi_{bi})_0 + \beta V,$$

where $\phi_0$ is the zero bias barrier height and $(\Delta \phi_{bi})_0$ is the image force lowering at zero bias. Substituting $\phi_e$ for $\phi_b$ in the thermionic current-voltage expression (Eqn.6) gives [6],

$$J = A^* T^2 \exp\left[-q(\phi_{b0} - (\Delta \phi_{bi})_0 + \beta V)/kT\right] \cdot \exp(qV/kT)/kT - 1]$$

$$= J_0 \exp(-\beta qV/kT) \cdot \exp(qV/kT)/kT - 1],$$

where

$$J_0 = A^* T^2 \exp[-q(\phi_{b0} - (\Delta \phi_{bi})_0)/kT].$$
And by defining a new quantity, \( n \), called the ideality factor,

\[
\frac{1}{n} = 1 - \beta = 1 - \frac{\partial \phi_e}{\partial V},
\]

Eqn. (8) can be rewritten as,

\[
J = J_o \exp\left(\frac{qV}{nkT}\right) \cdot \left[1 - \exp\left(-\frac{qV}{kT}\right)\right].
\]  

The ideality factor is a measure of the variation of the effective barrier height with bias. If \( \partial \phi / \partial V \) is constant with bias then \( n \) is constant. In the ideal case that \( \partial \phi / \partial V \) is zero then \( n = 1 \). For an applied bias greater than \( 3kT/q \), Eqn. (11) reduces to,

\[
J = J_o \exp\left(\frac{qV}{nkT}\right).
\]

The generation rate of electron hole pairs in the semiconductor of a Schottky barrier solar cell may be deduced with some simple considerations beginning with the absorption of light in the semiconductor. Consider a beam of broadband light with intensity \( I_o(\lambda) \) (photons/cm\(^2\)-s-unit bandwidth) incident on a thick semiconductor. A photon of a given wavelength which has travelled without absorption a distance \( x \) into the semiconductor has no memory of the distance it has actually travelled. Subsequently, the probability that the photon will be absorbed in any \( dx \) is constant. Therefore, the decrease in the light intensity with \( x \), \( -dI(\lambda, x)/dx \), is proportional to the intensity remaining at \( x \) \[2\]. This yields,

\[
-\frac{dI(\lambda, x)}{dx} = \alpha I(\lambda, x) \quad \Rightarrow \quad I(\lambda, x) = I_o(1 - R) \exp(-\alpha x),
\]
where the proportionality constant, $\alpha$, is the absorption coefficient and $R$ is the reflection coefficient. As shown in Fig. 5, the absorption coefficient, $\alpha(\lambda)$, describes the magnitude of photon absorption at a given wavelength for a given material. The term $(1-R)$ in Eqn. (13) expresses that some fraction of the incident intensity $I_o(\lambda)$ is reflected away from the semiconductor surface.

Assuming that a large fraction of the absorbed photons generate electron-hole pairs, which is true for the semiconductors germanium and silicon, then the change in the photon intensity, $-d I(\lambda, x)/dx$, is the electron-hole pair generation rate, $G(\lambda, x)$. That is, the number of photons absorbed from the beginning to the end of a small interval $\Delta x$ is equal to the number of electron-hole pairs created. Or mathematically,

$$G(\lambda, x) = -\frac{dI(\lambda, x)}{dx} = \alpha(\lambda)I(\lambda, x) = \alpha(\lambda)I_o(1-R)\exp(-\alpha x). \quad (14)$$
For Eqns. (13) and (14) to be valid for a Schottky contact, the $(1 - R)$ reflection term should be replaced by $T(\lambda)$, the transmission coefficient of the Schottky contact metal.

Figure 6 gives a plot of $G(\lambda, x)$ which has been computed from Eqn. (14), and this illustrates two important points. First, since $G(\lambda, x)$ is closely related to $I(\lambda, x)$, it is clear that the light spectrum found at some distance within a semiconductor (for instance at the depletion region in a $p$-$n$ junction) can differ substantially from the spectrum at the surface. Second, the higher energy photons are absorbed near the semiconductor surface.

![Graph showing electron-hole pair generation rate versus distance from the semiconductor (silicon) computed from Eqn (14). The curve for $\lambda = 689$ nm corresponds to $h\nu = 1.8$ eV and $\alpha = 10^{3.5}$/cm. The curve for $\lambda = 540$ nm corresponds to $h\nu = 2.3$ eV and $\alpha = 10^{3.9}$/cm. For both wavelengths: $T = 0.80$ and $I_o = 1$ mW/cm$^2$.](image)

Fig. 6 Electron-hole pair generation rate versus distance from the semiconductor (silicon) computed from Eqn (14). The curve for $\lambda = 689$ nm corresponds to $h\nu = 1.8$ eV and $\alpha = 10^{3.5}$/cm. The curve for $\lambda = 540$ nm corresponds to $h\nu = 2.3$ eV and $\alpha = 10^{3.9}$/cm. For both wavelengths: $T = 0.80$ and $I_o = 1$ mW/cm$^2$.

If the Schottky contact metal is thin enough to readily pass light ($T(\lambda)$ large), then under illumination electron-hole pairs will be created which can be acted upon by the electric field in the depletion region to generate a photocurrent. Figure 7 illustrates the three photocurrent components for a $p$-type Schottky barrier solar cell under
illumination. Most long-wavelength light is absorbed in the bulk neutral region (process 3 in Fig. 7) producing electron-hole pairs. Only those electrons that are created within a diffusion length of the depletion region can diffuse to the junction and be collected. This is just as in a p-n junction solar cell. In fact, the expression for the photocurrent per unit bandwidth due to electron-hole pair production in the neutral region is similar to that for a p-n junction except that \((1 - R)\) is replaced by \(T(\lambda)\),

\[
J_n(\lambda) = qT(\lambda)I_0(\lambda)\left[\frac{\alpha L_n}{(\alpha L_n + 1)}\right]\exp(-\alpha x),
\]

where \(L_n\) is the diffusion length for electrons [8]. Electron-hole pairs are also created by short-wavelength light being absorbed in the depletion region (process 2 in Fig. 7). These electron-hole pairs are quickly separated by the high electric field in the depletion region, and therefore, they yield a higher collection efficiency than for the electron-hole pairs created in the bulk. The depletion region contribution to the photocurrent per unit bandwidth is equal to the number of photons absorbed per unit bandwidth in the depletion region, or,
Additionally, holes may be excited over the barrier (process 1 in Fig. 7) by incident photons with energy $h\nu > q\phi_B$. This process contributes less than 1% to the total photocurrent and will henceforth be ignored.

Notice that the total photocurrent, which is the sum of Eqn. (15) and (16), is due to light-generated minority carriers traversing the depletion region just as in a $p-n$ junction. Experimentally the photocurrent for the Schottky contact may be increased by increasing the transmission coefficient $T(\lambda)$ and/or the diffusion length $L_n$. In combination with an antireflection coating, rather high light transmission is attainable in practice for thin metal films; 90-95% transmission for 10-100 Å of gold and 85% transmission for 100 Å of aluminum [8], [9]. The current-voltage characteristics for an illuminated Schottky diode are given by adding the total photogenerated current, $J_p$, to the thermionic-emission dark current of Eqn. (11),

$$J = J_0 \exp\left(qV / nkT\right) \cdot \left[1 - \exp\left(- qV / kT\right)\right] - J_p . \hspace{1cm} (17)$$

Because the high electric field in the depletion region quickly separates the electron-hole pairs created there, the maximum photocurrent can be achieved by situating the depletion region in conjunction with the highest concentration of optically excited electron-hole pairs. As Eqn. (14) indicates, the highest light-generated electron-hole pair concentration occurs at the semiconductor surface ($x = 0$) for all wavelengths. For a standard $p-n$ junction solar cell the depletion region begins at approximately 4000-5000 Å from the semiconductor surface, whereas, for a Schottky barrier solar cell it begins at the semiconductor surface. While this benefits the spectral response of the Schottky barrier solar cell, the spectral response is also lowered for each photon energy due to the Schottky contact metal reflecting and absorbing light. Figure 8 illustrates the
computed ideal silicon $p$-$n$ junction solar cell spectral response, which is defined here as the total photocurrent at a given wavelength divided by $q I_o (\lambda)$.

Usually, a practical $p$-$n$ junction solar cell will have a spectral response corresponding to a surface recombination velocity of $S_p > 10^4$ in Fig. 8. In contrast, a practical Schottky barrier solar cell will exhibit a response suggesting a smaller $S_p$ and therefore a better short wavelength response. The larger surface recombination in the $p$-$n$ junction device is due in part to the crystal damage induced in the semiconductor during the ion implantation or high temperature diffusion necessary to produce the $p$-$n$ junction.

![Computed internal spectral response of a silicon $p$-$n$ junction with different surface recombination velocities, $S_p$. (from Sze [8])](image)

**Fig. 8** Computed internal spectral response of a silicon $p$-$n$ junction with different surface recombination velocities, $S_p$. (from Sze [8])

B. The Minority Carrier Metal-Insulator-Semiconductor Tunnel Diode

In practice, an atomically abrupt junction between a metal and a semiconductor like that in an ideal Schottky contact is seldom achieved. Ultra high vacuum techniques
are necessary to produce an intimate metal-semiconductor contact on silicon because a 10 Å SiO₂ interfacial layer will develop on silicon almost immediately upon cleaving in air. Under atmospheric conditions this natural oxide will grow to 20 Å in about 1 week.

The insulator thickness in a metal-insulator-semiconductor (MIS) contact determines whether the contact will operate as a Schottky contact, an MIS capacitor, or an MIS tunnel diode. If the insulator is less than 10 Å, carriers can tunnel through the layer easily, and the result is a Schottky contact. For a thick insulating layer (> 50 Å) the tunneling probability is extremely low, no current may be passed, and the structure represents a conventional MIS capacitor. For intermediate insulator thicknesses (10-50 Å) a third device called an MIS tunnel diode will result. The MIS tunnel diode is routinely called a Schottky barrier diode although an MIS tunnel diode operates by different current transport mechanisms than the Schottky barrier diode.

The dominant dark current in an MIS tunnel diode solar cell may be due to the movement of semiconductor minority or majority carriers across the insulator. MIS solar cells are therefore generally classified as either “majority carrier” or “minority carrier” devices. For both devices the photocurrent is due to minority carriers just as in Schottky and p-n junction diodes. Theoretical and experimental results [10],[11] indicate that, in general, the minority carrier devices yield higher efficiency solar cells. Additionally, several investigators have concluded [10], [12] that the Al/SiO₂/p-Si structure is an archetype minority carrier device. Because the PSSC consists of this basic structure and possesses an SiO₂ layer in the range 10-50 Å, it should operate as a minority carrier MIS tunnel diode. The following discussion will be limited to the minority carrier MIS case.

In Fig. 9, the energy band diagram for the minority carrier MIS structure is shown along with the possible current mechanisms that may exist: $J_{th}$ (thermionic emission), $J_s$ (charge exchange between the metal and semiconductor band edges via surface states), $J_{rg}$ (depletion layer recombination-generation), $J_{ot}$ (oxide trap tunneling current), $J_\alpha$ and $J_{vt}$ (tunneling currents). It is expected that in the forward bias regime
the two largest components of the total current would be $J_{th}$ and the tunneling currents $J_{el}$ and $J_{vt}$. However, experimental results [13] based on the temperature dependence of the current in minority carrier MIS devices indicates that the thermionic emission current is negligible. This can be explained in part by recalling that in a Schottky barrier diode $q\phi_B$ is pinned to $\sim 2/3 \ E_g$ by the surface states occurring at the interface between the thin native oxide and the semiconductor. This pinning results in $J_{th}$ values for traditional Si and GaAs Schottky barrier diodes that are too large for effective solar cell use, and it is therefore desirable to "free" $\phi_B$ and possibly lower $J_{th}$. In the MIS structure an oxide can be intentionally grown that will passivate the semiconductor surface and therefore allow $\phi_B$ to be determined by the metal work function instead of pinning by the surface states. Assuming that $J_{th}$ is therefore suppressed by the oxide layer and that $J_{rg}, J_s$, and $J_{el}$ are negligible, a qualitative analysis of the tunnel currents

Fig. 9 Possible charge transport mechanisms for a MIS tunnel diode under forward bias. (from Green et al. [10])
(\(J_{\alpha}, J_{\ell c}, J_{\sigma}, \text{ and } J_{\ell v}\)) alone is sufficient to explain the experimental \(I-V\) characteristics of the minority carrier MIS tunnel diode.

Figure 10 shows the energy band diagram for the Al/SiO\(_2\)/p-Si structure for which \(\phi_{mi} = 3.2\) eV. A low metal-to-insulator barrier height (\(\phi_{mi} < 3.6\) eV) leads to a minority carrier MIS device whereas a high metal-to-insulator (\(\phi_{mi} < 3.8\) eV) barrier height yields a majority carrier MIS device. The electron and hole densities at the surface of the \(p\)-type semiconductor may be expressed as,

\[
\begin{align*}
  n_s &= n_p \exp\left(\frac{q \psi_s}{kT}\right) \\
  p_s &= p_p \exp\left(-\frac{q \psi_s}{kT}\right),
\end{align*}
\]

(18)
where $\psi_s$ is the potential at the surface, $n_{po}$ and $p_{po}$ are the equilibrium surface densities of electrons and holes, respectively. The potential $\psi$ is defined as zero in the semiconductor bulk and is measured with respect to the intrinsic level, $E_i$, which is the energy at which the Fermi level would lie in the semiconductor bulk if the semiconductor were undoped [8]. If a $p$-type MIS structure at thermal equilibrium has a low metal-to-insulator barrier height ($\phi_{mi} < 3.6 \text{ eV}$), then the surface of the semiconductor is inverted at zero bias. As Fig. 10 illustrates, inversion occurs in the semiconductor when the intrinsic energy level, $E_i$, bends below the intrinsic energy level at zero bias. This band bending is equivalent to a large positive surface potential, $\psi_s$, and Eqn. (18) reveals that the electron concentration at the $p$-type semiconductor surface is enhanced.

If the bias is increased from zero to a moderate forward bias (metal negative) the Fermi level in the metal will rise with respect to the Fermi level in the semiconductor causing the bands to bend upwards near the semiconductor surface. According to Eqn. (18), as the forward bias increases, the semiconductor of Fig. 10 will go from inversion, through depletion of holes ($\psi_B > \psi_s > 0$), to accumulation of holes ($\psi_s < 0$). As the bands bend upwards toward accumulation, $\psi_s$ becomes more negative, the electron concentration at the surface will decrease according to Eqn. (18), and $J_e$ will likewise decrease to a negligible level. However, when $E_{fn}$ nears the conduction band edge at the surface, $J_e$ will increase quickly because the occupied states in the metal are now higher in energy than a large number of unoccupied states in the semiconductor. Concurrently, as $E_{fn}$ rises, carriers in the valence band see fewer empty states in the metal into which they can tunnel, and $J_{vt}$ will become insignificant. Because holes are accumulating at the surface as the forward bias increases, $J_{vt}$ will increase. For low $\phi_m$ values, $J_e$ is the dominant current over the entire forward bias range.

Under reverse bias (metal positive), $E_{fn}$ moves below $E_F$ in the bulk of the semiconductor resulting in a downward band bending that increases the inversion. As Eqn. (18) predicts, the electron concentration in the conduction band at the surface will increase with increasing reverse bias. As the occupation of states in the conduction band
increases with reverse bias, increasingly few electrons in the metal will possess energies greater than $E_o$, that are necessary to tunnel into the conduction band, and $J_{ct}$ will decrease quickly. It is obvious, however, that $J_{wc}$ should increase very rapidly under these conditions. The magnitude of $J_{wc}$ will depend strongly on the zero bias condition of the insulator-semiconductor interface.

The valence band tunnel currents under reverse bias are in general small except when the reverse bias is high enough to push $E_{fm}$ near or below the semiconductor valence band at the surface, $E_{vs}$. At this point, electrons in the valence band now see a large number of empty states in the metal. $J_{tv}$ will increase slowly as the positive voltage on the metal lowers $E_{fm}$ to within $kT$ of $E_{vs}$, but $J_{tv}$ will increase rapidly when $E_{fm} < E_{vs}$. The magnitude of $J_{tv}$ is determined by the number of these empty states in the metal and by the tunneling probability as a function of these states. For low $\phi_m$ values, $J_{wc}$ is the dominant current over the entire reverse bias range.

From the preceding observations it is clear that the dominant current for both reverse and moderate forward bias comes from minority carrier tunneling between the metal and the semiconductor conduction band for a p-type MIS contact with a low $\phi_{mi}$. These large electronic tunnel currents can pass in both directions through the oxide layer because the inversion layer ensures that few majority carriers are present at the insulator-semiconductor interface to communicate with the metal.

Ng and Card have developed closed form expressions for the current-voltage relationship and the open circuit voltage for both the minority and majority carrier MIS solar cell [12]. Their results for the p-type minority carrier MIS dark current and open circuit voltage are given by (from the Appendix),

$$J_{dark} = \frac{qD_n n_p 0}{L_n} \left[ \exp \left( \frac{qV}{kT} \right) - 1 \right]$$
Equations (19) and (20) are valid under the assumption that space-charge recombination is negligible and that the oxide layer \( d \) is thin enough that tunneling does not limit the dark current. It is somewhat remarkable that these expressions are identical to those for a \( n^+p \) junction solar cell.

Operating as solar cells, MIS tunnel diodes have been consistently shown to produce open circuit voltages that are larger than similarly constructed Schottky barrier solar cells and equal to \( p-n \) junction solar cells. It is also generally accepted that the short circuit current density in an MIS solar cell is somewhat larger than that in a \( p-n \) junction. Perhaps this is because the MIS structure has no “dead layer” like that present in diffused \( p-n \) junction devices, and therefore the long minority carrier lifetime inherent to pure, single crystal semiconductor materials is preserved. Additionally, the MIS structure is very suitable for a cost effective "flow-through" fabrication process and is compatible with an arbitrary semiconductor including polycrystalline material.
III. Particulate Silicon Solar Cell Design and Construction

A. Material Selection

Under the original patent design (Fig. 2), the materials to be used are zinc as the substrate, zinc-oxide as the transparent conductor, Macro Defect Free Cement (MDFC) as the dielectric material, and \( n \) or \( p \)-type silicon crystals. MDFC adheres well to silicon, can be made transparent if the voids are less than 1 \( \mu m \), and possesses a strength comparable to that of steel. Zinc-oxide was chosen over its most obvious competitor, indium-tin-oxide, because it yields equally transparent and conductive films at a much lower price, and zinc-oxide has been shown to produce a good Schottky contact with silicon [14].

In this research, the prime considerations in choosing the materials for the experimental PSSC are: cost, high temperature processing capability, long-term stability, and the available technology. Due to technical difficulties in producing the desired zinc-oxide film and the Macro Defect Free Cement, substitutions were made for these original design materials. The final experimental particulate cell in this report utilizes 2 mm thick aluminum sheeting for the substrate, 100 \( \AA \) of thermally evaporated aluminum as the transparent conductor, Crystalbond 509 (polyethylene phthalate) as the dielectric, and comminuted \( p \)-type silicon grains. The silicon grains are supplied by Wacker who creates them by crushing 15 Ohm-cm, \( p \)-type, single crystal boule fragments. These crystals arrive with a particle size distribution of 45-850 \( \mu m \) and are sieved by the OSU Mechanical Engineering Department into several smaller size ranges: 45-53; 53-75; 75-90; 90-106; 106-125; 125-180; 180-145; 425-850 \( \mu m \). Only the 425-850 \( \mu m \) particle size is used to produce the solar cells described here mainly because the larger grain size is easiest to process.

The proper choice of a dielectric is pivotal in lowering processing cost and increasing cell performance. The dielectric isolates the metal substrate from the conductive top-layer, and provides a smooth, level surface on which to deposit the
transparent conductor. It is desirable for the dielectric layer to be strong, clear, HNO₃ and HF resistant, mechanically polishable, and temperature resistant up to 550 C. Strength is needed in order to support the cell, especially for an optimized PSSC which would be as thin as possible to reduce material and hence costs. Furthermore, because the spray pyrolysis and sputtering methods used to deposit the transparent conductor heat the sample, the dielectric should exhibit little contraction upon cooling otherwise the thin transparent conductor will crack. The dielectric used in the PSSC (polyethylene phthalate) possesses only some of these desirable properties. It is clear, polishable, and strong, but it melts at ~100 C and is not chemical resistant.

Attempts were made to produce zinc-oxide films by sputtering and spray pyrolysis. Although reasonably low sheet resistance values for these films could be attained, both processes produce temperatures high enough to damage the polyethylene phthalate dielectric. In addition to being quicker, the evaporation of a thin aluminum layer does not harm the phthalate dielectric.

B. PSSC Construction

The first step in constructing a PSSC is to fuse the 425-850 μm silicon monocristalline grains to the aluminum substrate to make an ohmic contact. Because the grains may have been strained by the comminution process, they are first annealed at 1000 C and etched with CP4 (2HF: 15 HNO₃: 5 Acetic) to remove surface damage. After a cleaning with acetone/methanol/deionized water, between 12 and 18 silicon grains (425-850 μm) are placed on the 2 mm thick aluminum substrate. A heated press is then used to first heat the aluminum substrate and the silicon grains to 580 C for 10 minutes in air and then to press the silicon grains into the aluminum substrate using 4400 N (see Fig.11). If the local pressure or the net force delivered to an individual silicon grain during the press is too large, it will shatter. Two measures are taken to avoid this. First, the 10 minute preheat at 580 C is necessary to allow the aluminum substrate to soften slightly, reducing the amount of force necessary to embed the silicon
grains in the aluminum substrate. Second, the plate of the press that contacts the silicon grains is made of a compressible carbon fiber material so that the force delivered to an individual silicon grain is distributed over its entire top surface. The pressing is done at

4400 Newtons

compressible carbon plate

12-18 silicon grains aluminum substrate

Temperature = 580 C

Fig. 11 Pressing the silicon grains into the aluminum substrate.

580-590 C because this temperature is just above the silicon-aluminum eutectic temperature but significantly below the melting point of aluminum (660 C). Therefore, during the press, the aluminum substrate should remain solid while a small region under each silicon grain should melt. As the system cools, an aluminum rich regrowth region will occur on the underside of each silicon grain forming an ohmic contact.

The sample now undergoes a planarization process designed to flatten the grain top surfaces so that the grains may be continuously covered by the thin metal film applied later. The planarization is achieved by mounting the sample to the flat face of a metal pestle and then grinding the sample on a plane 600 grit surface. Approximately ½ the volume of the silicon grains is removed. The mechanical and metallurgical bond resulting from the pressing process is strong enough for ¾ of the silicon grains to remain
attached to the metal substrate during this planarization process. After this process, the sample is an array of irregularly spaced silicon grains with coplanar flat surfaces, as can be imagined if the dielectric and contact metal were removed from the finished PSSC of Fig. 12. While the planarized sample is still mounted to the metal pestle it is wet polished on a lapping wheel with a succession of polishing grits: 15 μm, 5 μm, 1 μm.

The planarized aluminum-silicon construction is now submersed in a CP4 silicon etch (2HF: 15 HNO₃: 5 Acetic) and is then cleaned with an acetone/methanol/deionized water. The etch removes silicon at the rate of 2-5 μm/min, and the sample is etched for 30 seconds to remove microscopic surface damage as well as residues from the polishing process. The chemical etch is critical to produce a silicon surface free of undesirable surface damage and likewise a good rectifying contact. In fact, all PSSCs created without a silicon etch possessed efficiencies less than 1%. After the etch, the silicon is exposed to air and this forms a SiO₂ layer approximately 11 Å thick.

Next the sample is subjected to a 15 min anneal at 480 C in flowing forming gas (10%H₂: 90% N₂). The anneal strengthens the silicon-aluminum alloy effecting a better ohmic contact. But most importantly, the anneal evaporates impurities present in the native oxide layer and conditions the SiO₂ layer so that it is free of pinholes or microcracks. After the anneal, the SiO₂ layer is very delicate and the device can be compromised by mechanical or thermal stresses.

Once the sample has been annealed, the polyethylene phthalate dielectric may be applied. At room temperature the dielectric can be easily pulverized into small grains. These phthalate grains are then manually placed between the embedded silicon grains, and the entire sample is heated until the phthalate becomes molten and fills the area between the silicon grains. If thinly applied, the molten phthalate flows to wet the vertical surfaces of the unpolished grains but leaves the planarized top surfaces uncovered. It is this desirable property of the phthalate that motivated its use.

The MIS contact is now produced by thermally evaporating a 80-100 Å aluminum film onto the area of the sample containing the polished silicon grains. The vacuum pressure is ~ 9 x 10⁻⁷ Torr and the film thickness is monitored in the vacuum
chamber during deposition. A low deposition rate (1-10 Å/sec) is used because it has been found that this increases film transmittance with no appreciable loss in conductivity [9]. A contact pad is then created by masking off the active solar cell region and evaporating 1 µm of aluminum as a strip along the periphery. Figure 12 shows the completed PSSC. No antireflection coating is deposited.

![Diagram of a finished particulate silicon solar cell](image)

**Fig. 12** A finished particulate silicon solar cell.

For every PSSC created, a witness solar cell is concurrently produced on a 8 Ω cm, *p*-type silicon wafer (Fig. 13). First, the wafer is etched if necessary and then cleaned. A back ohmic contact is formed by evaporating a 1 µm thick layer of 100 Å thick aluminum dots

![Diagram of a wafer witness cell](image)

**Fig. 13** Wafer witness cell.
aluminum onto the entire wafer back and then performing an anneal as described earlier. Next, a 80-100 Å thick, 3 mm diameter aluminum dot pattern is evaporated on the polished wafer face to form the MIS contact. The processes of annealing, chemical etching, cleaning, and evaporating the MIS contact metal are identical for a given PSSC and the accompanying witness wafer so that meaningful comparisons may be made.
IV. Experimental Results

A. \( I-V \) measurement: Efficiency, Fill Factor, Ideality Factor, Series and Shunt Resistance

The present development of the PSSC is at the sample level as opposed to the process level, which is to say that considerable variation exists among cells that are produced by the same processing steps. For this reason only basic characterization techniques such as \( I-V \) and \( C-V \) measurements have been employed.

The fill factor, efficiency, and ideality factor may all be attained from the \( I-V \) characteristic. The illuminated \( I-V \) characteristic is obtained for the PSSC and the wafer witness cell by shining a tungsten filament lamp on the cell from 14 inches and measuring the \( I-V \) response. The tungsten lamp emits like a black body source with a peak intensity at 720 nm and therefore does not adequately simulate AM1 (100 mW/cm\(^2\)) conditions under which solar cells are traditionally characterized. A calibrated solar cell may be used to calibrate the tungsten lamp since the short circuit current, \( I_{sc} \), for a silicon solar cell is linear with light intensity, \( P_{in} \). Therefore, a commercial \( p-n \) junction 2 x 4 cm silicon solar cell was purchased and sent to the National Renewable Energy Laboratory (NREL) to be calibrated at AM1. The NREL results are shown in Fig. 14. Notice that the spectral response in Fig. 14b is very similar to the calculated spectral response in Fig. 8 for a \( p-n \) junction solar cell with a large surface recombination velocity. A comparison of \( I_{sc} \) for the calibrated cell under 100 mW/cm\(^2\) (\( P_{in}^{AM1} \)) illumination and under the tungsten lamp intensity (\( P_{in}^{tungsten} \)) gives,

\[
\frac{I_{sc}^{AM1}}{P_{in}^{AM1}} = \frac{I_{sc}^{tungsten}}{P_{in}^{tungsten}} \quad \Rightarrow \quad P_{in}^{tungsten} = P_{in}^{AM1} \frac{I_{sc}^{tungsten}}{I_{sc}^{AM1}} = 33 \text{ mW/cm}^2 = 1/3 \times \text{AM1.} \quad (21)
\]

Figure 15 shows the dark and illuminated \( I-V \) characteristics for a PSSC and a wafer witness solar cell under the tungsten lamp intensity. The fill factor measures the
Fig. 14 NREL characterization of a 2 x 4 cm p-n junction solar cell with an antireflection coating. (a) current-voltage characteristic under illumination (100 mW/cm²). Fill factor = .749, efficiency = 12.4%, $V_\infty = .5729$ V, and $I_{sc} = .2300$ A. (b) Quantum efficiency.

"squareness" of $I$-$V$ curve and is given by the ratio of the two rectangle areas $V_m \times I_m$ and $V_\infty \times I_{sc}$,

$$FF = \frac{I_m \cdot V_m}{I_{sc} \cdot V_\infty},$$

(22)

where $V_m$ and $I_m$ are the voltage and current at the maximum power point, and $I_{sc}$ and $V_\infty$ are the short circuit current and the open circuit voltage. These quantities are illustrated more explicitly in Fig. 16 which gives a magnified 4th quadrant view of the illuminated $I$-$V$ characteristic in Fig. 15. The $I_m$, $V_m$ values, and hence the fill factor, are obtained by selecting the point on the illuminated $I$-$V$ curve which gave the largest $I \times V$ product. The fill factor values for the PSSC, wafer cell, and the calibrated p-n junction
Fig. 15 Dark and illuminated measured current-voltage characteristics. (a) particulate silicon solar cell. (b) wafer witness solar cell
Fig. 16 Magnified view of the illuminated current-voltage characteristics given in Fig. 15. (a) particulate silicon solar cell (see Fig. 15a); fill factor = .58, eff = 3.8%. (b) wintess wafer solar cell (see Fig. 15b); fill factor = .67, eff = 8.6%.
cell are .58, .67, and .749, respectively. In general, the wafer witness cells give fill factor values about 10% higher than similarly processed PSSCs.

The efficiency is given by,

$$\text{eff} = \frac{V_m \cdot I_m}{P_{in} \cdot A} = \frac{V_{oc} \cdot I_{sc} \cdot FF}{P_{in} \cdot A}$$

(23)

where $P_{in}$ is the light intensity incident on the cell, and $A$ is the total area of the cell. It should be mentioned that this research made no attempt to increase the packing density of silicon grains. It is conceivable that the ratio of the total planarized silicon grain area divided by the total cell area could be made greater than 0.7 with little additional effort. Therefore, the total cell area, $A$, for the PSSC is taken to be only the silicon grain area in the efficiency calculation. The $I$-$V$ characteristics in Fig. 16 yield $\text{eff} = 8.6\%$ for the wafer witness cell and $\text{eff} = 3.8\%$ for the PSSC. Typical wafer cell efficiencies are around 7% whereas typical PSSC efficiencies are about 4%. The highest PSSC cell efficiency is 6% and the calibrated $p$-$n$ junction cell yields 12%. Note that while the light generated current shown in Fig. 16 is less for the wafer witness cell, so is $A$, resulting in a higher efficiency for the wafer cell.

The ideality factor is given by,

$$n = \frac{q}{kT} \frac{dV}{d(\ln(I))} = \frac{q}{2.3kT} \frac{dV}{d(\log(I))}$$

(24)

Because the plot of $\log(I)$ vs $V$ for a real diode is not linear, $n$ is a function of applied voltage. $n$ usually varies between 1 and 2. From Fig. 17 it is found that the wafer witness cell gives $n = 1.8$ at .4 volts, and the PSSC cell gives $n = 2.1$ at .35 volts.

The efficiency and fill factor for a solar cell depend strongly on the series resistance, $R_s$, because a series resistance lowers the short circuit current and the maximum power delivered by the solar cell. It is desirable for a solar cell operating at one sun to possess $R_s/A < 1 \text{ Ohm/cm}^2$, where $A$ is the device area. The physical origins
Fig. 17 Ideality factor. Determined from the dark current-voltage characteristics of Fig. 15 and plotted here as log (I) v.s. V. Dashed lines indicate the slope used to determine the ideality factor, n. (a) the particulate silicon solar cell; n = 2.1. (b) wafer witness solar cell; n = 1.8.
of $R_s$ for a metal-semiconductor type solar cell include: 1) the resistance of the top metal contact pad, 2) the contact resistance and the spreading resistance of the back metallization (ohmic contact), 3) the bulk resistance of the semiconductor, and 4) the lateral resistance of the thin metal Schottky contact.

Although most methods used to extract $R_s$ are difficult to execute and the results difficult to interpret, two straightforward methods exist. In the first, an approximate value of $R_s$ may be found by examining the high voltage regime of the dark current-voltage characteristics. The series resistance dominates in this regime and the current-voltage characteristic yields a straight line of slope $1/R_s$ as shown in Fig. 18. The current-voltage curve indicates $R_s/A = 50 \, \Omega / .04 \, \text{cm}^2 = 2000 \, \Omega/ \text{cm}^2$ for the PSSC and $R_s/A = 45 \, \Omega / .01 \, \text{cm}^2 = 5000 \, \Omega/ \text{cm}^2$ for the wafer cell. These series resistance values are very large for solar cell purposes, and it is still not clear how PSSCs and wafer witness cells can possess such high $R_s$ values but still operate with efficiencies greater than 5%. PSSCs which obtained efficiencies greater than 5% usually exhibited $R_s/A < 500 \, \Omega/ \text{cm}^2$ derived according to the method shown in Fig. 18. The calibrated 2 x 4 cm p-n junction cell gives $R_s = 1 \, \Omega$ demonstrating that a high efficiency solar cell will have a low $R_s$.

The action of illuminating a solar cell may change $R_s$ from its dark value, and therefore, it is best to extract $R_s$ from data pertaining to the actual operating conditions of the solar cell. The second method for determining $R_s$ is graphical and consists of plotting the illuminated $I-V$ characteristics for multiple light intensities. A small fixed current increment, $\Delta I$, is chosen for each illuminated characteristic and the current is located that is $\Delta I$ above $I_{sc}$, or $I = I_{sc} + \Delta I$. As Fig. 19 illustrates, the resulting locus of these points forms a straight line with slope $1/R_s$. This method is free from limiting approximations, does not rely on the knowledge of other parameters such as $J_0$, $n$, or $R_p$ (the shunt or parallel resistance), and in general is considered to give good results. Figure 19 show that $R_s = 311 \, \Omega$ for the PSSC cell and $R_s = 290 \, \Omega$ for the wafer cell. Again it should be stressed that $R_s$ is the quantity that is clearly limiting higher fill factor and efficiency values for the PSSC and wafer cells.
Fig. 18 First order representation of a series and parallel resistance. (a) particulate silicon solar cell (area = 4 mm$^2$); $R_s \approx 50 \ \Omega$, $R_p > 5000 \ \Omega$. (b) wafer witness solar cell (area = 1 mm$^2$); $R_s \approx 45 \ \Omega$, $R_p \approx 4000 \ \Omega$. 

---

**Figures:**

(a) 

(b)
Fig. 19 Determination of $R_s$ using the illuminated $I$-$V$ characteristics. (a) wafer solar cell (area 1 mm$^2$); $R_s = 290$ Ω. (b) particulate silicon solar cell (area = 4 mm$^2$); $R_s = 311$ Ω
During the research little care was taken to control the thickness of the oxide layer but it is likely that the natural oxide layer present in these devices is in the range 11-16 Å. Other investigators have experimental results for the variation of the fill factor, open circuit voltage, short-circuit current, and efficiency versus oxide thickness (Fig. 20)

Fig. 20 Experimental characteristics of the Al/SiO₂/p-Si (minority carrier) structure. (a) $V_{\infty}, J_{\infty},$ and fill factor versus oxide thickness. (b) Conversion efficiency calculated from the characteristics of (a). (from Ng and Card [12])
for a similar Al/SiO₂/p-Si MIS configuration. The expressions presented earlier for \( V_\infty \) and \( J_\infty \) for the \( p \)-type silicon minority carrier MIS are independent of the oxide thickness because they are valid only when the oxide thickness does not hinder minority carrier tunneling. Figure 20a clearly shows that \( V_\infty \) is constant for all oxide thickness, and \( J_\infty \) is constant until 16 Å and decreases quickly thereafter. Above 16 Å, minority carrier tunneling through the oxide layer becomes important and the expression for \( J_\infty \) must contain an additional tunneling term (see Appendix). Fig. 20b indicates that the optimum SiO₂ thickness is around 11 Å because the efficiency falls off rapidly above this thickness.

B. \( C-V \) measurement: Doping Concentration

For a minority carrier MIS operating in the semiconductor limited regime the minority carrier Fermi level and the semiconductor energy bands are fixed in relation to \( E_{\text{fn}} \) [10]. As a result, the charge stored in the inversion region at the semiconductor-insulator interface undergoes only small changes with bias so that a change in applied reverse bias is accommodated primarily by a change in the depletion layer width.

Assuming that the free carrier density in the depletion region is small compared to the acceptor concentration (depletion approximation), Fig. 21 shows the change in the depletion layer space charge, electric field, and electrostatic potential as a reverse bias is applied.

By starting with Poissons equation,

\[
\frac{d^2 \psi}{dx^2} = -\frac{q}{\varepsilon} N_A \tag{25}
\]

and integrating twice as indicated in Fig. 21,

\[
-V_s = \psi_s - \psi_w = \frac{q}{\varepsilon} N_A \left( Wd_0 + \frac{W^2}{2} \right), \tag{26}
\]
a simple expression for the capacitance-voltage characteristic can be attained,

\[
W = \sqrt{d_0^2 - 2 \frac{\varepsilon V_a}{N_A} d_0}
\]  

(27)

\[
C = \frac{dQ}{dV} = -qAN_A \frac{dW}{dV}
\]  

(28)

\[
\frac{C}{A} = \left[ \frac{2}{\varepsilon qN_A} (V_c - V_a) \right]^{-\frac{1}{2}} \Rightarrow \frac{1}{C^2} = \frac{2}{q\varepsilon^2 A^2 N_A} (V_c - V_a).
\]  

(29)

Fig. 21 The assumed space charge density \( \rho \), the resulting electric field magnitude \( |E| \), and the electrostatic potential \( \psi \) as a function of distance into the semiconductor. \( \psi \) is obtained by integrating \( |E| \), and \( |E| \) is obtained by integrating \( \rho \). (from Green et al. [10]).
In Eqns. (25)-(29), $d_0$ is the zero bias depletion region width, $V_c = q\frac{N_A}{2\varepsilon}d_0^2$, $N_A$ is the impurity density, and $A$ is the diode area.

The $C-V$ measurement is made by superimposing a 10-20 mV 1MHz ac signal onto a dc bias. The ac voltage signal, $dV$, causes a small change in the depletion region width, $dW$, and therefore a small change in the amount of uncompensated charge, $dQ$ [15]. For a metal-semiconductor contact, the depletion region width lies almost entirely within the semiconductor. The capacitance as given by Eqn. (29) is measured for different dc bias voltages $V_s$. According to Eqn. (29), a plot of $1/C^2$ v.s. $V_s$ will yield $V_c$ from the voltage axis intercept and $N_A$ from the slope. If $N_A$ is indeed constant throughout the depletion region, then $1/C^2$ v.s. $V_s$ will be linear. Knowledge of the doping concentration value, $N_A$, is equivalent to knowing the resistivity of the semiconductor in the metal-semiconductor contact. This is especially important for this research because the resistivity value of the semiconductor material supplied by Wacker was not directly specified.

An experimental plot of $1/C^2$ v.s. $V_s$ for the 3.8 % efficient PSSC is given in Fig. 22. Figure 22 shows that the $1/C^2$ v.s. $V_s$ slope is nearly constant and this partially

\[
1/C^2 \quad (1/nF^2)
\]

\[
\begin{array}{c|c|c|c|c|c|c|c}
0 & 0.5 & 1 & 1.5 & 2 & 2.5 & 3 \\
0 & 0.5 & 1 & 1.5 & 2 & 2.5 & 3 \\
\end{array}
\]

**Fig. 22** Measured capacitance-voltage characteristic for the 3.8% efficient PSSC. The slope yields $N_A = 1.3 \times 10^{15} /\text{cm}^3$. (For $I-V$ characteristics see Fig. 15)
justifies the depletion approximation assumption. The $1/C^2$ capacitance expression in Eqn. (29) depends critically on an accurate determination of the diode area, $A$, because this expression contains the square of the diode area. Because a simple determination of the planarized silicon grain area for the PSSC has proven difficult, the $N_A$ value for the PSSC as determined from the $C-V$ measurement should be considered approximate. However, the experimental result, $N_A = 1.3 \times 10^{15}$ $/\text{cm}^3$, is equivalent to a silicon resistivity of 6 $\Omega$ cm and this value agrees reasonably well with a resistivity value of 15 $\Omega$ cm found independently from a four point probe resistivity measurement. The resistivity measurement was made on a bulk piece of single crystal silicon that came from the ingot used to produce the silicon grains.

C. Degradation

In general, the presence of the thin insulator layer present in MIS solar cells has caused their long-term stability to be questioned by many investigators. Indeed, both the PSSC and wafer cells of this research suffer from sudden degradation, and the scant amount of life-testing results from other investigators for the Al/SiO$_2$/p-Si structure are mixed. Figure 23 shows an example of the dark current-voltage characteristic that commonly develops after a PSSC or a wafer cell has undergone substantial mechanical and thermal stresses during testing. This current-voltage degradation occurs suddenly on the curve tracer screen, and it usually happens about 2-3 days after the cells have been fabricated. The upper curve of Fig. 23 passes through the positive current axis at zero voltage, and this suggests that a capacitive effect is present in the cell. As the cell is illuminated from the dark situation of Fig. 23, the lower curve in Fig. 23 will lose its rectangular character and the hysteresis will become more pronounced.

The degradation has been witnessed by other investigators and has been attributed to microcracks which develop in the $\sim 15 \text{ Å}$ SiO$_2$ layer [9]. Although the true failure mechanism is not understood, it is possible that these microcracks could allow intimate contact between the 100 Å aluminum layer and the semiconductor leading to
hysteresis and poor photoresponse [9]. Lien and Charlson have observed that a similar MIS solar cell also yields “leaky” $I-V$ characteristics if the SiO$_2$ layer is not made continuous by annealing. Other possible failure modes exist. Because aluminum reduces SiO$_2$, the interfacial layer may be compromised and this may allow a shunting current to flow that is composed of majority carriers [16]. It may also be that the thin aluminum layer is oxidizes in an atmospheric ambient or that the SiO$_2$ interfacial layer continues to grow by the diffusion of oxygen through the thin top metal layer. These last two modes could be circumvented by encapsulating the cell. Because the degradation in PSSC and wafer witness appears suddenly, it is most likely due to either a fault in the insulator layer or a shunting current resulting from a conductive path between the top metal layer and the metal substrate.
V. Proposed Modifications to the Particulate Silicon Solar Cell

A. Dielectric Improvement

There are several possible modifications to the current PSSC design that would lower the processing time and cost while increasing the cell performance. These modifications were not tested due to time constraints or technological limitations. The most important modification is the replacement of the present dielectric material, Crystalbond 509 (polyethylene phthalate), with a more suitable dielectric. Recall that the silicon grains are planarized and polished while embedded in the metal substrate, that is, before the phthalate is introduced. After the polishing, the phthalate (as a fine granular solid) is then meticulously added by hand between the silicon grains and melted at 100 C. Additional solid phthalate is added until the phthalate melt level is close to the top of the planarized silicon grains. Inspection of the grains under a microscope after the phthalate application indicates that the phthalate outgasses during melting because in some cases a residue is evident on the polished surface of the silicon grains.

A better overall approach would be to apply quickly a thick layer of molten dielectric material between and on top of the silicon grains before the planarization and polishing process. This allows the dielectric and silicon grains to be planarized together, thereby creating a more planar cell surface with less effort. Also, if a dielectric is present during the planarization and polishing processes the silicon grains will be further stabilized; approximately ¼ of the silicon grains pull away from the metal substrate during planarization if no dielectric is present.

Currently, the phthalate cannot be added before planarization because its presence is incompatible with the processing steps which follow the planarization/polishing. For example, polyethylene phthalate cannot withstand a silicon etch well (HNO₃ / HF / Acetic), and it is soluble in acetone and methanol. This incompatibility precludes the acetone/methanol/deionized water cleaning and the silicon etch which are necessary after the PSSC has been polished but before the top metal contact is deposited. Another problem is that polyethylene phthalate melts at a low
temperature (~100°C) and this precludes the use of high temperature processing
(~500°C), for instance, that necessary to apply indium-tin-oxide or zinc oxide by spray
pyrolysis. Although phthalate does have the desirable qualities of being clear, filling
voids when melted, and polishing well, an ideal dielectric material must also resist
chemical etchants and organic solvents and allow processing at elevated temperatures.

B. Zinc-Oxide Transparent Conductor with a Nonplanar Approach

According to the original patent design zinc oxide is to be used in the form of a
transparent conductor as the top-contact “metal”. Kobayashi et. al. have shown that the
MIS structure formed between zinc-oxide and p or n type silicon is adequate to produce
solar cells of at least 8% [14]. Also, theoretical calculations have shown that for a
silicon based MIS, the maximum obtainable AM1 efficiency is 21% if either aluminum or
zinc-oxide is used as the top contact metal [17]. There are several advantages to using a
zinc-oxide film instead of a thin metal film. First, the high band gap (~ 3 eV) of zinc-
oxide results in a film that can be made 85-90% transparent for wavelengths in the range
400-850 nm [18],[19]. Second, the index of refraction for zinc-oxide is 2.0, and this
allows a specific thickness of the material to serve as an antireflection coating [20]. For
these reasons a zinc-oxide film should exhibit better spectral response. And lastly,
because the zinc-oxide will be made at least 500 Å thick, it should provide the
nonplanarized PSSC with increased film continuity and a longer lifetime. High quality,
low cost films of zinc oxide may be quickly and cheaply produced by spray pyrolysis
[21], [18].

Preferably, the planarization/polishing step should be omitted because it is time
consuming, problematic, and limits the light absorbing capacity of a silicon grain by
lowering its surface area. The current development of the PSSC requires planarization
because thin metal films (< 200 Å) do not continuously cover surfaces that have any
jagged topography. Figure 24 shows an unplanarized, unpolished PSSC that has a thin
dielectric layer. This configuration maximizes the exposed surface area of the silicon
Fig. 24 The unplanarized PSSC with a thin dielectric layer. The silicon grains have been chemically etched before application of the thin dielectric.

grains. Due to shadowing, the structure of Fig. 24 can not be continuously covered by a thin film metallization technique although it is quite possible with a thick zinc oxide layer (> 3000 Å) deposited by spray pyrolysis. Because zinc-oxide is applied as a liquid in this process, by rotating the substrate of Fig. 24 during spraying, the spray mist should move sufficiently to bridge all of the crevices.

The structure of Fig. 24 is similar to a “textured” solar cell construction, illustrated in Fig. 25, which has pyramidal surfaces created by anisotropical etching of the <100> silicon surface to reveal the <111> planes. Figure 25a shows that light incident on a given pyramid will reflect to a neighboring pyramid thereby reducing reflection losses. For bare silicon, the surface reflectivity is lowered from 35% for flat surfaces, as in the planarized PSSC, to 20% for a textured surface [8]. And with an antireflection coating, a textured cell can reduce reflection to just a few percent, as Fig. 25b demonstrates. The textured cell also encourages light to penetrate the semiconductor along paths that are not perpendicular to the junction interface. This causes photogeneration to occur nearer the depletion region, resulting in a larger quantum efficiency. Textured cells can easily produce total conversion efficiencies of over 15% [8]. Although the PSSC of Fig. 24 is not a well defined array of pyramids, the effects mentioned above should extend to this structure although to a lesser degree.
Fig. 25 A textured solar cell. (a) pyramidal array lowers surface reflection by effectively increasing the active silicon area. (b) reflection loss v.s wavelength for a flat surface and a textured solar cell. (from Sze [8])

C. Semiconductor Resistivity

The optimal semiconductor resistivity for a solar cell is most easily found from experiment. In general, a low resistivity yields large open circuit voltages while a high resistivity preserves the high lifetimes necessary for a large short circuit current. Table 1 shows experimental evidence from several investigators of the Al/SiO₂/p-Si MIS solar cell which suggests that $V_\infty$ may be maximized by using a semiconductor with a resistivity of 1 Ω-cm or less. The expression for $V_\infty$ presented earlier in Eqn. (20),
Table 1: Open circuit voltage compared to substrate resistivity. Values are for the Al/SiO$_2$/p-Si MIS structure.

\[
V_{\infty} = \frac{kT}{q} \ln \left( \frac{L_n J_{sc}}{qD_n n_{p0}} \right),
\]

predicts that $V_{\infty}$ will increase with decreasing resistivity of the $p$-type substrate. This is because $n_{p0}$ falls as the acceptor doping concentration increases, or equivalently, as the resistivity of the semiconductor decreases. Even though $V_{\infty}$ depends on $n_{p0}$ through the slowly varying natural log, the experimentally observed dependence on resistivity shown in Table 1 is quite strong.

As stated earlier, the total series resistance for a solar cell should be kept less than 1 $\Omega$ for each square centimeter of device area. To attain a rough estimate of the resistance due to the semiconductor in an MIS contact, the simple formula, $R = \rho L / A$, may be used. For a 3 mm diameter dot of 15 $\Omega$-cm and of 1 $\Omega$-cm wafer material this
formula gives, 10.6 Ω and 1.06 Ω, respectively. This calculation and the preceding experimental results indicate that the 15 Ω-cm silicon resistivity currently used in the PSSC is too high. The wafer witness cells use 8 Ω-cm p-Si and this may partially account for their higher efficiency.
VI. Conclusions

Efficiencies of 4-6% obtained from the PSSC are encouraging when compared to the wafer witness efficiencies of 8-10%. By optimizing the oxide thickness, semiconductor resistivity, and chemical etching procedures, both the wafer witness solar cell and the PSSC could be improved. In addition, the 3-dimensional character of an unplanarized PSSC will maximize the active silicon grain area, and therefore, the unplanarized PSSC may produce a better photoresponse than the planarized PSSC. Clearly though, the most immediate improvement will come by lowering the series resistance.

The PSSC created in this research lends itself to large scale fabrication techniques, primarily because it could be made quickly in one “flow through” process. Unfortunately, the resistivity window for the $p$-type silicon is relatively small, and it is still uncertain how other grain sizes will perform. There may be only a small amount of waste silicon of the proper resistivity and grain size available, and it may require substantial expense to extract these specific grains.
Bibliography


Derivation of the Current-Voltage Characteristics for the Minority Carrier MIS Solar Cell. (from [12])

Nomenclature:

- $D_n$: Diffusion coefficient for electrons.
- $E_v$: Energy of the semiconductor valence band.
- $E_{FP}$: Quasi Fermi energy for holes.
- $E_{FM}$: Fermi energy of the metal.
- $k$: Boltzmann's constant.
- $L_p$: Diffusion length for holes.
- $n_i$: Intrinsic carrier concentration.
- $N_c$: Effective density of states in the semiconductor conduction band.
- $N_d$: Semiconductor donor concentration.
- $p(0)$: Hole concentration at the semiconductor surface.
- $p_{so}$: Hole concentration in the neutral region of the $n$-type semiconductor in equilibrium.
- $W$: Depletion width.
- $\alpha$: Absorption coefficient.
- $\chi_h$: Effective tunneling barrier for holes.
- $\varepsilon_s$, $\varepsilon_i$: Static permittivity of the semiconductor, insulator.
- $\phi_h$: Defined in figure below.
- $\mu_p$: Hole mobility.
- $\psi_s$: Semiconductor surface potential.

The following derivation is for an $n$-type semiconductor substrate although it extends to $p$-type by simply changing the appropriate parameters. From the figure below it is clear that the MIS solar cell is forward biased under illumination and that the minority carrier quasi Fermi level at the semiconductor surface, $E_{FP}(0)$, does not align exactly with the metal Fermi level due to difficulty in tunneling through the oxide.
Energy band diagram for an illuminated MIS solar cell. (from Ng and Card [12])

The basic strategy to find the illuminated minority carrier current is to first find the portion of the current due to drift and diffusion and then use the tunneling current as an additional condition to reach an explicit expression. So, assuming that the recombination current is negligible, the drift component of the minority-carrier current is given by,

\[ J_p = p \mu_p \frac{dE_{Fp}}{dx} \]  \hspace{1cm} (A1)

Substituting the equation,

\[ p = N_c \exp \left( - \frac{E_{Fp} - E_v}{kT} \right) \]  \hspace{1cm} (A2)

for \( p \) in Eqn. (A1) and the equation,
\[ E_v = -q\phi_h + \frac{q^2 N_d}{2\varepsilon_s} \left(x^2 - 2Wx\right) \]  
(A3)

for \( E_v \) in Eqn. (A2), and integrating from \( x = 0 \) to \( x = W \) gives,

\[ \exp\left( -\frac{E_{fp}(0)}{kT} \right) - \exp\left( -\frac{E_{fp}(W)}{kT} \right) = J_p \exp\left( -\frac{qV}{kT} \right) \frac{\pi\varepsilon_s N_d}{n_i^2} \sqrt{\frac{2q^2kT}{\psi_s}} \left( \text{erf} \left( \sqrt{\frac{q\psi_s}{kT}} \right) \right) \]  
(A4)

For the case of interest, \( q\psi_s \ll kT \) and the error function reduces to unity giving,

\[ \exp\left( -\frac{E_{fp}(0)}{kT} \right) - \exp\left( -\frac{E_{fp}(W)}{kT} \right) = MJ_p \exp\left( -\frac{qV}{kT} \right), \]  
(A5)

where

\[ M = \frac{1}{n_i^2 \mu_p} \sqrt{\frac{\pi\varepsilon_s N_d}{2q^2kT}}. \]  
(A6)

If most of the incident photon flux, \( I_0 \), is absorbed in the neutral region then the general solution for the continuity equation is,

\[ \Delta p = G \exp\left( -\frac{x'}{L_p} \right) + H \exp\left( -\frac{x'}{L_p} \right) - \frac{I_0}{1 - 1/\alpha^2 L_p^2} \exp(-\alpha x'). \]  
(A7)

In Eqn. (A7) the new coordinate \( x' \) is used where \( x'=0 \) at the depletion region edge (see Fig. A1), and the boundary conditions are taken to be,

\[ x' = \infty \quad \Delta p = 0 \]  
(A8)
\[ x' = 0 \quad \Delta p = p_{n0} \left[ \exp \left( -\frac{E_{FP}(W)}{kT} \right) \cdot \exp \left( -\frac{qV}{kT} \right) - 1 \right]. \quad (A9) \]

By substituting \( E_{FP}(W) \) from Eqn. (A5) into the boundary condition of Eqn. (A9), Eqn. (A7) becomes,

\[
\Delta p = \left[ \frac{I_0}{\alpha D_p} + p_{n0} \left( \exp \left( -\frac{E_{FP}(0)}{kT} \right) \cdot \exp \left( \frac{qV}{kT} \right) - MJ_p - 1 \right) \right] \cdot \exp \left( -\frac{x'}{L_p} \right) \\
- \frac{I_0}{(1-1/\alpha^2 L_p^2)} \exp(-\alpha x') \\
(A10)
\]

If Eqn. (A10) is used in the expression for the diffusion component of the hole current density,

\[
J_p = qD_p \frac{d\Delta p}{dx'} \bigg|_{x'=0} \
(A11)
\]

the hole current density becomes,

\[
J_p \left[ 1 + \frac{qMP_{n0} D_p}{L_p} \right] = \\
- qI_0 \left( 1 - \frac{1}{\alpha L_p} \right) + \frac{qP_{n0} D_p}{L_p} \left[ \exp \left( -\frac{E_{FP}(0)}{kT} \right) \cdot \exp \left( \frac{qV}{kT} \right) - 1 \right] \\
(A12)
\]

For practical devices, the values for \( \frac{qMP_{n0} D_p}{L_p} \) and \( \frac{1}{\alpha L_p} \) are much less than one.

Ignoring these terms gives,
\[ J_p = -qF_0 + \frac{qP_{\text{so}}D_p}{l_p} \left[ \exp\left( -\frac{E_{\text{fp}}(0)}{kT} \right) \cdot \exp\left( \frac{qV}{kT} \right) - 1 \right], \tag{A13} \]

where the total incident photon flux, \( \int I_0(\lambda) d\lambda \), is called \( F_0 \). This equation expresses that the minority carrier current is the maximum photocurrent minus a current that may be considered as a back-diffusion current resulting from the high hole concentration at the semiconductor surface.

Now, an expression derived by Card and Rhoderick \cite{24} for the hole tunneling current may be used to find \( E_{\text{fp}}(0) \) in Eqn. (A13). The expression is given by,

\[ J_p = \frac{4\pi m^*_h q(kT)^2}{\hbar^2 N_v} \cdot \exp\left(-\chi_h^{1/2} d\right) p(0) \left[ \exp\left( \frac{E_{\text{fp}}(0)}{kT} \right) - 1 \right] \]

\[ = Q \exp\left( \frac{qV_i}{kT} \right) \cdot \left[ 1 - \exp\left( -\frac{E_{\text{fp}}(0)}{kT} \right) \right], \tag{A14} \]

where \( p(0) \) is the hole concentration at the semiconductor surface, \( \chi_h \) is the effective tunneling barrier for holes, \( V_i \) is the voltage across the oxide layer, and

\[ Q = \frac{4\pi m^*_h q(kT)^2}{\hbar^2} \exp\left(-\frac{q\phi_0}{kT}\right) \exp\left(-\chi_h^{1/2} d\right). \tag{A15} \]

The total illuminated hole current, \( J_p \), may now be determined by solving Eqn. (A14) for \( E_{\text{fp}}(0) \),

\[ \exp\left( -\frac{E_{\text{fp}}(0)}{kT} \right) = 1 - \frac{J_p}{Q \exp\left( \frac{qV_i}{kT} \right)}, \tag{A16} \]

and inserting this into Eqn. (A13) to give,
where $V_s$ is the voltage across the semiconductor ($V = V_s + V_i$). For reverse bias and moderate forward biases, which are the biases of interest in solar cell operation, the minority carrier MIS tunnel diode is limited by current transport through the semiconductor (diffusion limited) [10]. Assuming that space-charge recombination is negligible and that the oxide layer thickness, $d$, is small enough that tunneling does not limit the dark current, then Eqn. (A17) yields a simplified dark current,

$$J_p = \frac{-qI_0 + \frac{qP_{n0}D_p}{L_p} \left[ \exp \left( \frac{qV}{kT} \right) - 1 \right]}{1 + \frac{qP_{n0}D_p}{QL_p} \exp \left( \frac{qV_s}{kT} \right)}$$  \hspace{1cm} (A17)

The open circuit voltage may be found by setting $J_{\text{dark}} = J_{\text{sc}}$,

$$V_\infty \equiv \frac{kT}{q} \ln \left( \frac{L_p J_{\text{sc}}}{qP_{n0}D_p} \right).$$  \hspace{1cm} (A19)

For the $p$-type minority carrier case the diffusion limited Card and Ng have also developed additional theory which incorporates the interfaces states.