AN ABSTRACT OF THE DISSERTATION OF

Hamidreza Maghami for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on May 20, 2019.

Title: Digital Friendly Continuous-Time Delta-Sigma Analog-to-Digital Converters

Abstract approved: _____

Terri S. Fiez Karti Mayaram

Conventional Delta-Sigma ($\Delta\Sigma$) analog-to-digital converters (ADCs) utilize operational transconductance amplifiers (OTAs) in their loop filter implementation followed by multi-bit voltage domain quantizers. As CMOS integrated circuit technology scales to smaller geometries, the minimum transistor length and the intrinsic gain of the transistors decrease. Moreover, with process scaling the voltage headroom decreases as well. Therefore, designing OTAs in advanced CMOS processes is becoming increasingly difficult. Additionally, multibit quantizers are becoming more difficult to design due to the decreased voltage headroom and the challenges of low offset and noise requirements.

In this thesis, alternative digital solutions are introduced to replace traditional analog blocks. In the proposed solutions, compressed voltage-domain processing is shifted to the time-domain which benefits from process scaling as the transistors

scale down in size and become faster.

First, a novel highly linear VCO-based 1-1 multi stage noise shaping (MASH) delta-sigma ADC structure is presented. The proposed architecture does not require any OTA-based analog integrators or integrating capacitors. Second-order noise shaping is achieved by using a VCO as an integrator in the feedback loop of the first stage and an open loop VCO quantizer in the second stage. A prototype was fabricated in a 65nm CMOS process and achieves 79.7 dB SNDR for a 2MHz signal bandwidth.

Second, a novel time-domain phase quantization noise extraction for a VCO-based quantizer is introduced. This technique is independent of the OSR and the input signal amplitude of the VCO-based quantizer making it attractive for higher bandwidth applications. Using this technique, a novel 0-1-1 MASH ADC is presented. The first stage is implemented using a 4-bit SAR ADC. The second and the third stages use a VCO-based quantizer (VCOQ). Behavioral simulation results confirm second-order noise shaping with a 75dB SNDR for an OSR of 20.

Digital Friendly Continuous-Time Delta-Sigma Analog-to-Digital Converters

by

Hamidreza Maghami

A DISSERTATION

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Doctor of Philosophy

Presented May 20, 2019
Commencement June 2019

Doctor of Philosophy dissertation of Hamidreza Maghami presented on May 20, 2019.

APPROVED:

Co-Major Professor, representing Electrical and Computer Engineering

---

Co-Major Professor, representing Electrical and Computer Engineering

---

Head of the School of Electrical Engineering and Computer Science

---

Dean of the Graduate School

I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Hamidreza Maghami, Author

ACKNOWLEDGEMENTS

First and foremost, I would like to express my gratitude and appreciation to my advisors Professor Terri Fiez and Professor Karti Mayaram to give me the opportunity to work under their supervision. Words cannot fully express my humble admiration and indebtedness toward them. Their abundant kindness and tremendous insights, guidence and motivations helped me immensely throughout the years on my journey. Professor Fiez and Professor Mayaram have thought me how to better communicate my ideas and always have been supportive when I faced difficulties by providing invaluable advices and encouragement. It has been my great honor and privilege to be supervised by them.

My sincere appreciation goes to my Ph.D. program committee members Professor Gabor Temes, Professor Un-Ku Moon and Professor Arun Natarajan for not only their valuable comments on my research but all the lessons I learned from them in the past years. Also, I'd like to thank Professor Sharmodeep Bhattacharyya for serving as my graduate council representative in multiple stages of my program.

I am grateful to my friend and OSU Alumni, Dr. Ramin Zanbaghi. He has been my mentor in the past few years. Without his guidance, this work would not have been anywhere close to its current form. In spite of his busy schedule, he always made himself available to discuss research related or personal issues. I am indebted to him for his help and friendship.

I must thank all the members of the EECS department who have helped me in every step of my way, weather the students of our research group, or other groups. I learned a lot from each and every one of them. Some of these students include Saeed Pourbagheri, Samira Zaliasl, Ankur Guha Roy, Ronghua Ni, Justin Goins, Hossein Mirzaei, Pedram Payandehnia, Siladytia Dey, Hui Zhang, Brian Miller, Kyle Gray, Ravi Teja, Yi Zhang, Tao He, Manjunath Kareppagoudr, Jason Muhlestein, Spencer Leuenberger, Hyuk Sun, Praveen Venkatachala, Ahmed El-Shater, Calvin Lee, Farshad Farhabakhshian, Jerry Leung, Zhiping Wang, Mohamed Megahed, Yu Sang Chun, Azmeen Rahman, Shaan Sengupta, Hyunkyu Ouh, Mahmoud Sadollahi, Manoj Johnson, Yanchao Wang, Robin Garg, Siddarth Mahendra, Bhagirath Thota, Kamala Sadagopan, Emanuel Caceres, Jyotindra Shakya and Subramanian T R. It was great to know you all. If I have not included someone in this list, it is unintentional.

It is a pleasure to thank my closest friends in Corvallis, Hossein Mirzaei, Pedram Payandehnia, Arash Azizi, Milad Ghayour and Ali Ahmed for the wonderful times we shared, specially the Saturday night dinners. In addition, I would like to thank all my friends in Crossfit Train 97333 who gave me the necessary distractions from my research and made my stay in Corvallis memorable.

Finally, my deep and sincere gratitude to my family for their continuous and unparalleled love, help and support. This work could not have been completed without the support and motivation I received from them, even though we have not seen each other for years. Love you all. I am forever indebted to my parents Fatemeh and Javad for their unconditional love and never ending support

and encouragement throughout my life. They have made me who I am today by their sacrifices and giving me the opportunities and experiences. They selflessly encouraged me to explore new directions in life and seek my own destiny. I am forever thankful to my only sister Hoda and brothers Mohammad-Hossein, Amin and Iman for the endless encouragement and love they have given me throughout my life and always being there for me as a friend. Also, I would like to extend my gratitude to my brother in law Mahdi Moein. His hardworking, optimistic, bright and confident attitude has always been my inspiration since we met. Finally, I would like to express my appreciation to other members of my family, specially my dear grandma, who always have been caring to me and keeping me in her prayers. If it was not for her prayers this work would never be where it is today.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF FIGURES

LIST OF FIGURES (Continued)

LIST OF FIGURES (Continued)

LIST OF TABLES

To my dearest Parents,

Fatemeh and Javad

for their unconditional love and sacrifice

Chapter 1: Introduction

All signals occurring in the real world are analog. A beautiful sound of a bird singing, the light which reflects on objects that helps us see things and the electromagnetic waves used in the communication between two people through cellphones are all analog. The analog signals are continuous in time and magnitude. On the other hand, the processors (computers) process information in the digital domain. Thus, they operate with discrete time and magnitude (digital) signals. Most of the signal processing is performed in the digital-domain using digital signal processors (DSPs). Figure 1.1 shows the egg model for electronic applications [1]. There has to be an interface block to connect the real world signals to the computers for processing. This block is called an analog-to-digital converter (ADC).

ADCs are the essential components of electronic devices which interact with the real world. A high-quality microphone picking up the sound in nature, photocells in a video camera and a seismographic sensor to detect any small vibration of earth, all require different ADCs with different requirements to convert the analog signals to digital. Figure 1.2 shows an example of an ADC application in a conventional receiver and how the ADC is incorporated. First, the signal is detected by an antenna and then it is amplified and filtered by the receiver front-end. After that, the desired signal is digitized by the ADC and the ADC output which is in the digital domain, is further processed in a DSP.

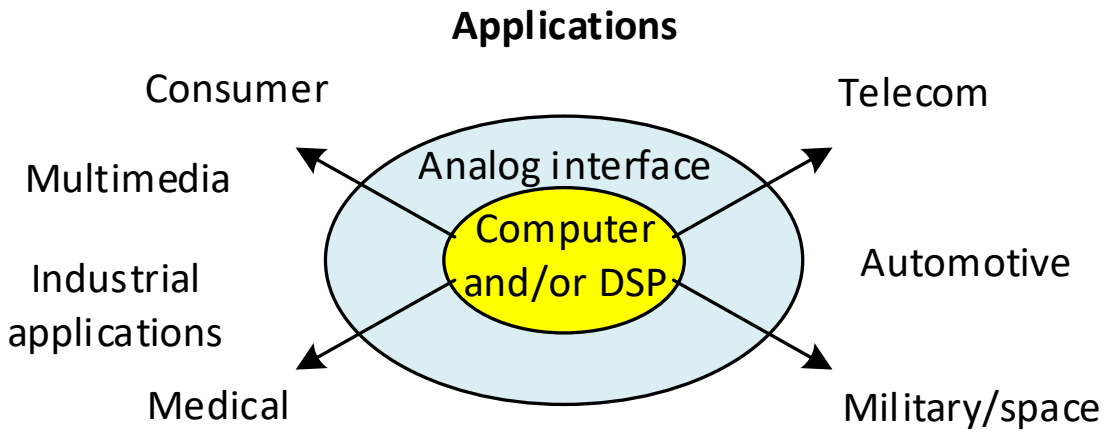


Figure 1.1: Egg model for electronic applications [1].

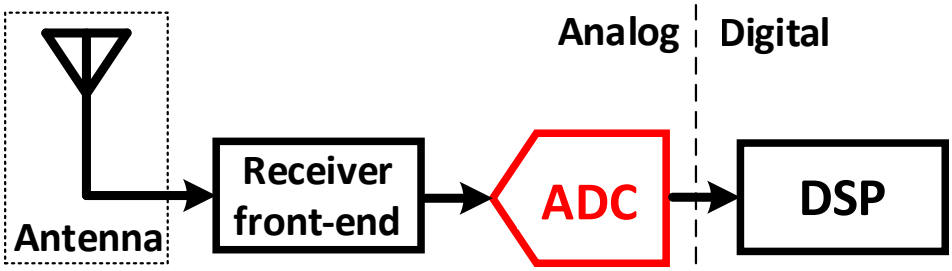
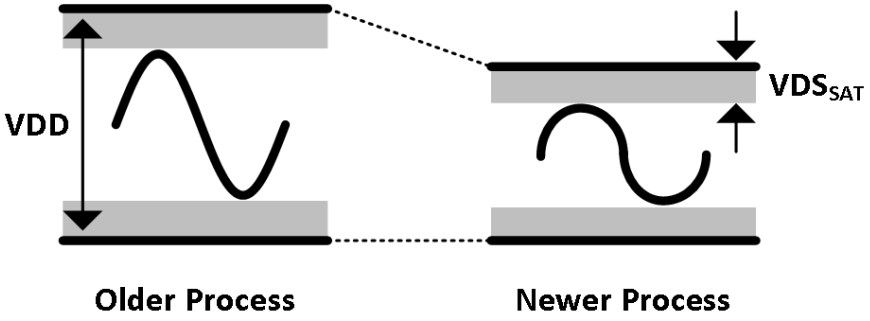


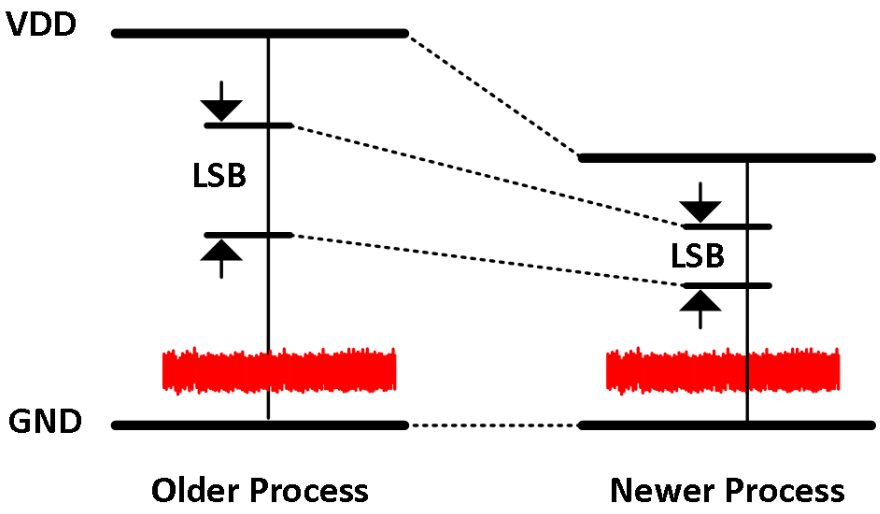
Figure 1.2: Block diagram of a simple receiver chain.

In order to reduce system cost, it is highly desirable to integrate analog and digital systems together onto a single chip. Digital circuitry is the technology driver since it represents the majority of the chip area and functionality. To achieve higher performance with reduced cost for digital systems, the transistor sizes are reduced from one generation to the next. This size reduction greatly benefits digital circuitry switching speed and reduces the area needed to achieve a particular function. Alternately, this scaling handicaps the analog circuit performance due to the reduction in the analog transistor intrinsic gain and voltage headroom. Figure 1.3 (a) shows the voltage headroom reduction in moving to a new process. As the supply voltage scales down as is the case in newer technologies, the maximum allowable signal swing decreases. This has a negative impact on analog circuits such as ADCs. As shown in Fig. 1.3 (b), as the supply voltage reduces, the least significant bit (LSB) voltage of the ADC scales down relatively to provide the same resolution, while the thermal noise remains the same. As a result, for a given signal-to-noise ratio and in a thermal noise limited scenario, the power consumption of the ADC has to be increased to reduce the thermal noise for a new technology node. In addition to this issue, conventional ADCs need high gain high bandwidth (BW) operational transconductance amplifiers (OTAs). Designing high performance OTAs is becoming more challenging in advanced technology nodes due to the reduced voltage headroom and reduced intrinsic gain of the transistors. Due to these issues, new ADC implementations are required that benefit from process scaling [2, 3].

One attractive alternative to conventional ADCs is time-domain ADCs. In



(a)



(b)

Figure 1.3: (a) Effect of process scaling on the maximum signal swing. (b) Effect of process scaling and thermal noise on the resolution of voltage domain ADCs.

these type of ADC, quantization is performed in the time-domain. As the transistor size reduces due to the process scaling, the time-domain resolution improves due to a reduced gate delay. Therefore, these ADCs take advantage of process scaling. Because of these advantages, time-domain ADCs have gained more attention recently [4].

1.1 Scope of this work

VCO-based quantizers (VCOQs) are a popular time-domain quantizer architecture. The simple digital friendly implementation of VCO-based quantizers makes them power and area efficient in advanced nano-meter CMOS processes [5]. Also these quantizers provide first order of noise shaping. While these are desirable characteristics, often the major performance limitation of VCO-based ADCs is the VCO nonlinearity.

The focus of this work is mainly on developing new techniques to enhance the precision of VCO-based ADCs without using OTAs or power hungry linearization methods. This precision enhancement is achieved by improving the linearity of VCO-based ADCs and also increasing the order of the noise shaping. To achieve this high precision OTA-less VCO-based ADCs, two novel methods are proposed. First, a highly linear VCO-based 1-1 MASH $\Delta\Sigma$ ADC structure is presented and measurement results are provided. Second, a novel time-dmain phase quantization noise extraction for a VCO-based quantizer is introduced. Using this technique a second order noise shaping SAR-VCO ADC is realized. Simulation results are

provided to validate the performance of the proposed ADC.

1.2 Thesis organization

The rest of the thesis is organized as follows. In Chapter 2 a 1-1 MASH OTA-less VCO-based ADC using single phase VCOs is presented. In-depth analysis of the effect of different non-idealities is provided in this chapter. In Chapter 3 a technique is introduced to extract the quantization noise of a multi-phase VCO. Using this technique, the implementation of the 1-1 MASH using multi-phase VCOs is described and then measurement results are provided from a fabricated prototype. In Chapter 4 another high precision quantization noise extraction technique is introduced. Using this technique a second order noise shaping SAR-VCO is realized and simulation results are provided. Finally, Chapter 5 provides a brief summary and concludes the paper.

Bibliography

[1] P. R. Gray, P. Hurst, R. G. Meyer, and S. Lewis, *Analysis and design of analog integrated circuits*. Wiley, 2001.

[2] A. Sanyal, S. Li, and N. Sun, "Low-power scaling-friendly ring oscillator based adc," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018, pp. 1–5.

[3] A. Babaie-Fishani and P. Rombouts, "A Mostly Digital VCO-Based CT-SDM With Third-Order Noise Shaping," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 8, pp. 2141–2153, Aug 2017.

[4] W. Yu, K. Kim, and S. Cho, "A 148 fs_{rms} integrated noise 4 MHz bandwidth second-order $\Delta\Sigma$ time-to-digital converter with gated switched-ring oscillator," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 8, pp. 2281–2289, 2014.

[5] M. Z. Straayer and M. H. Perrott, "A 12-bit, 10-MHz bandwidth, continuous-time $\Sigma\Delta$ ADC with a 5-bit, 950-MS/s VCO-based quantizer," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 4, pp. 805–814, 2008.

Chapter 2: A Highly Linear OTA-free VCO-based 1-1 MASH $\Delta\Sigma$ ADC

In this chapter, a new VCO-based 1-1 MASH delta-sigma ADC structure is presented. The proposed architecture does not require any OTA-based analog integrators or integrating capacitors. Second-order noise shaping is achieved by using a VCO as an integrator in the feedback loop of the first stage and an open loop VCO quantizer in the second stage. Simple digital circuitry extracts the phase quantization error of the first stage as a pulse signal that is applied to the second stage. The input of the first VCO is a very small amplitude signal and the input of the second VCO is a two-level PWM signal. Therefore, the VCO non-linearity does not limit the overall ADC performance, mitigating the need for power hungry linearization methods. The proposed idea was simulated at the transistor level and the results verify the analysis.

2.1 Introduction

Quantization noise shaping combined with oversampling in data converters enhances the signal-to-quantization-noise ($SQNR$) ratio in a particular frequency band. By pushing most of the quantization noise out of the signal band, oversampling data converters are able to achieve high resolution at reasonably high

conversion speeds [1]. Although noise shaping techniques have been applied to different types of analog-to-digital converters (ADCs) such as successive approximation register (SAR) ADCs [2, 3], integrating quantizer ADCs [4], etc., they are most commonly used in delta-sigma ($\Delta\Sigma$) modulators.

$\Delta\Sigma$ ADCs utilize oversampling and noise shaping to achieve high accuracy despite using inaccurate components. This feature combined with relaxed anti-aliasing requirements make $\Delta\Sigma$ ADCs an appropriate choice for various applications from ultra-low-power biomedical devices to ultra-wide-band communications applications [5].

Continuous-time (CT) $\Delta\Sigma$ ADCs have the advantage of inherent anti-aliasing filtering compared to discrete-time (DT) $\Delta\Sigma$ ADCs. Loop filter integrators in CT $\Delta\Sigma$ ADCs are usually implemented using active RC-integrators due to the linearity requirements [1]. However, with process scaling, the intrinsic gain of the transistor reduces, which makes it increasingly difficult to design high gain operational transconductance amplifiers (OTAs) in modern CMOS processes.

As the supply head-room reduces with process scaling, multibit quantizers are becoming more difficult to design due to the offset and noise requirements of the comparators. One attractive alternative is to use time domain quantizers such as time-to-digital converters (TDC) or VCO-based quantizers. TDCs and VCO-based quantizers benefit from process scaling due to the increased time resolution of the delay cells.

Moreover, the digital friendly nature of VCO-based $\Delta\Sigma$ ADCs makes them power and area efficient in advanced nano-meter CMOS processes [6]. While these

are desirable characteristics, often the major performance limitation of VCO-based ADCs is the VCO non-linearity. Several techniques have been introduced to mitigate the non-linearity issue. In [6] a VCO-based quantizer is implemented inside a closed loop. Here, the high in-band loop gain suppresses the VCO non-linearity. In order to achieve more than first-order noise shaping, however, this architecture needs OTAs which generally have higher power requirements as compared to VCOs and do not scale well with process scaling. In [7–9], two stage architectures were employed to cancel out the harmonic components due to the VCO non-linearity. Although these architectures solve the VCO non-linearity issue, the loop filter implementations employ OTAs. In [10–13] the VCO non-linearity is corrected by using a pulse width modulated (PWM) input signal. However, to achieve high linearity, a power hungry PWM generator is needed at the input. In [14–16] VCOs are used as a phase integrator followed by a quantizer. Therefore, the input signal to the VCO is reduced and VCO non-linearity is suppressed significantly. However, in [14], the order of the modulator is limited to one and [15,16] require OTAs to implement high order noise shaping. In [17] a higher order modulator using enhanced linearity VCOs is introduced. Although, no OTA is used, the linearity of the modulator is still limited to around 10.5 bits.

In this chapter, a novel highly linear VCO-based 1-1 MASH architecture is presented that does not require an OTA or a PWM generator. The first stage is a closed loop first-order VCO-based ADC. The quantization noise of the first stage is extracted in the time domain using simple digital circuitry. The extracted quantization noise, which is in PWM form, is fed to the second stage which is an open

loop VCO-based ADC. The proposed structure suppresses the VCO non-linearity without the added requirement of a PWM generator at the input. Moreover, since no OTA is used in this ADC, this architecture benefits from process scaling.

The organization of this chapter is as follows. In Section 2.2 the 1-1 MASH VCO-based $\Delta\Sigma$ ADC presented in [10, 11] is reviewed to provide a background for the proposed structure. This architecture needs a PWM generator at its input to suppress the VCO non-linearity. The proposed highly linear 1-1 MASH VCO-based $\Delta\Sigma$ ADC, which mitigates the use of a PWM generator is presented in Section 2.3. Section 2.4 provides design insight for the proposed architecture by examining the effect of different design parameters on the performance. In Section 2.5, the effects of non-idealities on the performance are analyzed. Next, a transistor level design example is demonstrated to verify the analysis in Section 2.6. Finally, Section 2.7 concludes the chapter.

2.2 Prior Art

Fig. 2.1 shows a 1-1 MASH VCO-based ADC architecture presented in [10, 11]. Both stages of the ADC are open loop VCO-based quantizers. The first stage quantizes the input voltage. A phase detector (PD) block shown in Fig. 2.1 generates a pulse signal which goes high (V_{DD}) at the positive edge of the sampling clock ($CLK_S(t)$) and goes low at the first positive edge of the VCO_1 output ($W_1(t)$) in that sampling period. This signal is shown as $E_{Q1}(t)$ in Fig. 2.2. In order to process the first stage quantization noise in the second stage, the generated pulse

signal switches on and off VCO_2. In this architecture, the input signal is required to be fed to VCO_2. In this way, the quantization error of the first stage will be available at the output of the second stage and can be removed in the final output by using simple digital filters. A more detailed explanation of the architecture is as follows.

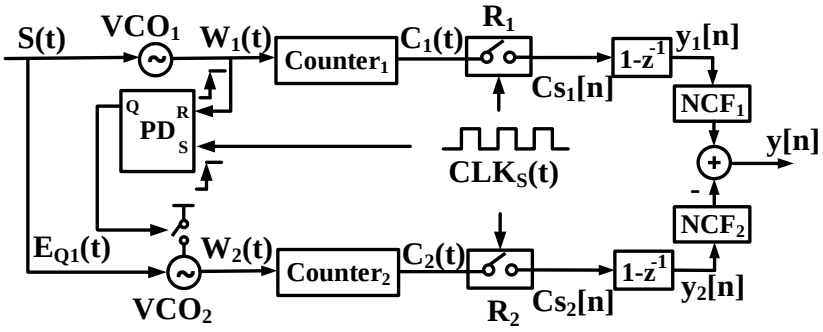


Figure 2.1: 1-1 MASH architecture based on open loop VCO-based ADCs [10].

The output of VCO_1 is a square wave signal $W_1(t)$, the frequency of which is a linear function of the VCO input signal $S(t)$. Equation (2.1) shows the relationship between VCO_1 output phase ($\phi_1(t)$) and its input voltage ($S(t)$). In this equation, K_{VCO1} and f_{fr1} are the voltage-to-frequency gain and the free-running frequency of VCO_1, respectively.

$$\phi_1(t) = \int_0^t (2\pi K_{VCO1} S(t) + 2\pi f_{fr1}) dt \tag{2.1}$$

$Counter_1$ output increases for each rising edge of $W_1(t)$ which is equal to a 2π radian phase change of the VCO output. The output of $Counter_1$ is sampled by register R_1 on the rising edge of CLK_S. Equation (2.2) describes the sampled

output of Counter$_1$, $Cs_1[n]$. In this equation ϕ_{q1} is the first stage quantization phase error. It is a function of both the input voltage and the time difference between the rising edge of $CLK_S(nTs)$ and the first rising edge of $W_1(t)$ ($t_{Q1}[n]$) in each sampling period as shown in Fig. 2.2.

$$\begin{aligned} Cs_1[n] =& \frac{\phi_1(nT_S) + \phi_{q1}(nT_S)}{2\pi} \\ &= \int_0^{nT_S} (K_{VCO1}S(t) + f_{fr1})\,dt \\ &+ \int_{nT_S}^{t_{Q1}[n]} (K_{VCO1}S(t) + f_{fr1})\,dt \end{aligned} \tag{2.2}$$

The sampled Counter$_1$ output is digitally differentiated ($Cs_1[n] - Cs_1[n-1]$) to generate the first stage output which is equal to:

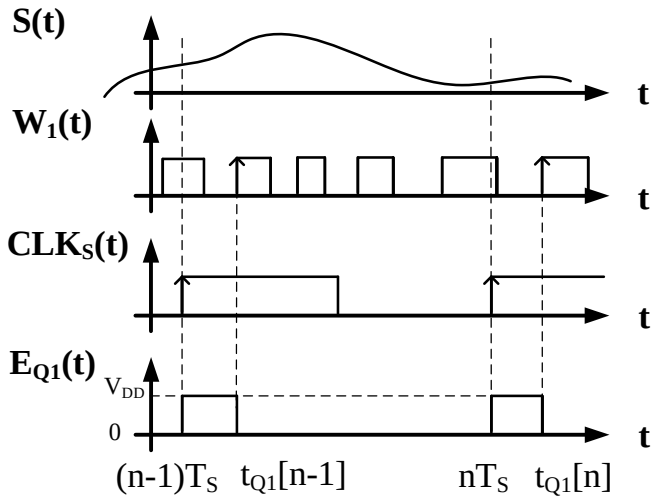


Figure 2.2: The timing diagram of the $E_{Q1}(t)$ pulse extraction [10].

$$y_1[n] = \int_{(n-1)T_S}^{nT_S} (K_{VCO1} S(t) + f_{fr1})\, dt + \frac{\phi_{q1}(nT_S) - \phi_{q1}((n-1)T_S)}{2\pi} \tag{2.3}$$

Assuming the sampling frequency is much higher than the input signal bandwidth (BW), the input signal can be assumed constant between two consecutive samples. Thus, using z-transforms the first stage output is:

$$Y_1(z) = \left(K_{VCO1} T_S z^{-1}\right) S(z) + f_{fr1} T_S + \left(1 - z^{-1}\right) \frac{\phi_{q1}(z)}{2\pi} \tag{2.4}$$

where $f_{fr1}T_S$ is an offset and can be easily removed in the digital domain. First-order noise shaping can be seen in the above equation.

In a MASH structure, the quantization noise of the first stage is processed by the second stage. The quantization noise in VCO-based ADCs is contained in the phase domain and it does not explicitly exist in this structure. As can be seen in (2.2), the phase quantization error of the first stage is the integral of the input signal between the rising edge of $CLK_S(nTs)$ and the first rising edge of $W_1(t)$ ($t_{Q1}[n]$). Fig. 2.2 shows this time difference as a pulse signal ($E_{Q1}(t)$) in the time domain. Since $E_{Q1}(t)$ is high (V_{DD}) only between kT_S and $t_Q[k]$ (k = 0,1,2, ...)

and zero elsewhere, $\phi_{q1}((n-1)Ts)$ can be written as:

$$\begin{aligned}\phi_{q1}\left((n-1)\,T_S\right) = \\ \int_{(n-1)T_S}^{t_{Q1}[n-1]} 2\pi\left(K_{VCO1}S(t)+f_{fr1}\right)dt \\ = 2\pi\int_{(n-1)T_S}^{nT_S}\frac{E_{Q1}\left(t\right)}{V_{DD}}\left(K_{VCO1}S(t)+f_{fr1}\right)dt\end{aligned} \tag{2.5}$$

In order to cancel ϕ_{q1} at the final output of the MASH structure, first ϕ_{q1} is generated at the second stage output. Then, by applying proper digital filtering to each stage output and subtracting the two signals from each other, ϕ_{q1} is canceled at the final output. Equation (2.5) shows that ϕ_{q1} is a function of both $E_{Q1}(t)$ and $S(t)$. To generate ϕ_{q1} at the second stage output, the input signal is applied to the VCO_2 input. A control switch is added to VCO_2 which turns it off (on) when $E_{Q1}(t)$ is low (high) as shown in Fig. 2.1. In this way the VCO_2 output phase changes only when $E_{Q1}(t)$ is high. The VCO_2 output phase holds its value when $E_{Q1}(t)$ is low. The VCO_2 output phase can be written:

$$\phi_2\left(t\right) = \int_0^t \frac{E_{Q1}\left(t\right)}{V_{DD}}\left(2\pi K_{VCO2}S(t)+2\pi f_{fr2}\right)dt \tag{2.6}$$

Similar to the first stage, the output of the second stage is calculated by digitally differentiating the sampled Counter_2 output ($Cs_2[n]-Cs_2[n-1]$) and is equal to:

$$\begin{aligned}y_2\left[n\right] = \int_{(n-1)T_S}^{nT_S}\frac{E_{Q1}\left(t\right)}{V_{DD}}\left(K_{VCO2}S(t)+f_{fr2}\right)dt \\ + \frac{\phi_{q2}\left(nT_S\right)-\phi_{q2}\left(\left(n-1\right)T_S\right)}{2\pi}\end{aligned} \tag{2.7}$$

Assuming both VCOs are perfectly matched, the first term of (2.7) matches (2.5). Thus, using z-transforms the second stage output is:

$$Y_2(z) = \left(z^{-1}\right)\frac{\phi_{q1}(z)}{2\pi} + \left(1 - z^{-1}\right)\frac{\phi_{q2}(z)}{2\pi} \tag{2.8}$$

Based on (2.4) and (2.8), to cancel ϕ_{q1}, simple digital filters are used as follow:

$$\begin{aligned} NCF_1(z) &= z^{-1} \\ NCF_2(z) &= \left(1 - z^{-1}\right) \end{aligned} \tag{2.9}$$

Therefore, the final output can be derived as:

$$Y(z) = z^{-2}\left(K_{VCO1}T_S\right)S(z) + \left(1 - z^{-1}\right)^2\frac{\phi_{q2}(z)}{2\pi} \tag{2.10}$$

In the architecture presented in [10, 11], second-order noise shaping has been achieved using two VCOs in a MASH structure. This architecture does not require OTAs and therefore has the benefits of scalability and reduced power. The frequency of VCO_1 changes proportional to the input voltage ($S(t)$). Thus, the width of the generated pulse ($E_{Q1}(t)$) is also a function of $S(t)$ and it does not explicitly correspond to ϕ_{q1}. In order to generate ϕ_{q1} at the output of the second stage, $S(t)$ also has to be applied to VCO_2. Since the input signal is directly fed to both the VCOs, the non-linearity of the VCOs still limits the overall ADC performance. In [10] a PWM generator is used at the input to generate a PWM signal. The linearity of the PWM generator is important and thus this block consumes

significant power [12]. Additionally, VCO_2 has to hold its phase perfectly when it is turned off which is challenging in practice due to circuit nonidealities, such as leakage current and charge redistribution.

In Section 2.3, a new 1-1 MASH VCO-based $\Delta\Sigma$ ADC is proposed. In this structure, the VCO non-linearity is inherently suppressed, and two VCOs are utilized to achieve second-order noise shaping. There is also no need for any OTA or a power hungry linearization method.

2.3 Proposed Structure

Fig. 2.3 shows the block diagram of the proposed VCO-based 1-1 MASH ADC. In this structure, the first stage is a closed-loop architecture with phase feedback and the second stage is an open-loop VCO-based ADC. VCO_1 in the first stage is used in the phase domain and operates as an integrator. Counter_1 works as an N-bit (2^N level) phase quantizer and its output is sampled by a register which generates the first stage output codes. The output of the first stage is fed back to the VCO_1 input using a DAC. Similar to Fig. 2.1, VCO_2 in the second stage is used in the frequency domain. However, in the proposed architecture, the input signal is not connected to the input of VCO_2, compared to the architecture reported in [10,11]. Here, a two level PWM signal generated in the first stage is applied to VCO_2. In this work, the PD block shown in Fig. 2.1 is replaced by a quantization phase detector (QPD) block. As shown in Fig. 2.4, the QPD block is made up of a flip-flop and an XOR gate which generates the pulse signal $E_{Q1}(t)$. Similar to Fig. 2.2,

$E_{Q1}(t)$ is high (V_{DD}) between the rising edge of $CLK_S(nT_S)$ and the first rising edge of $W_1(t)$ ($t_{Q1}[n]$) in each sampling period and zero elsewhere.

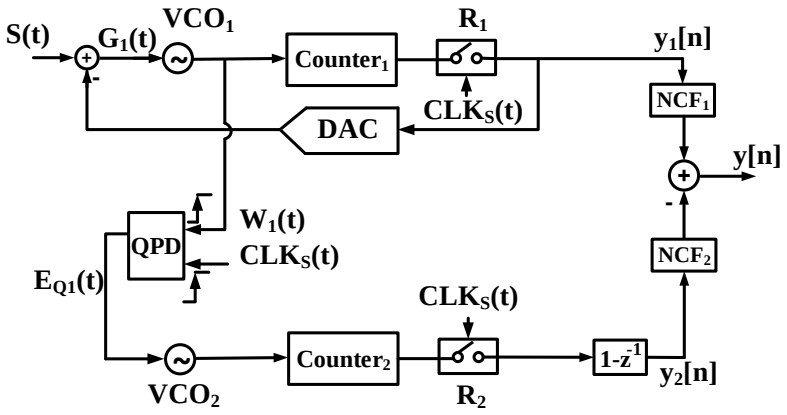


Figure 2.3: Proposed 1-1 MASH ADC structure [18].

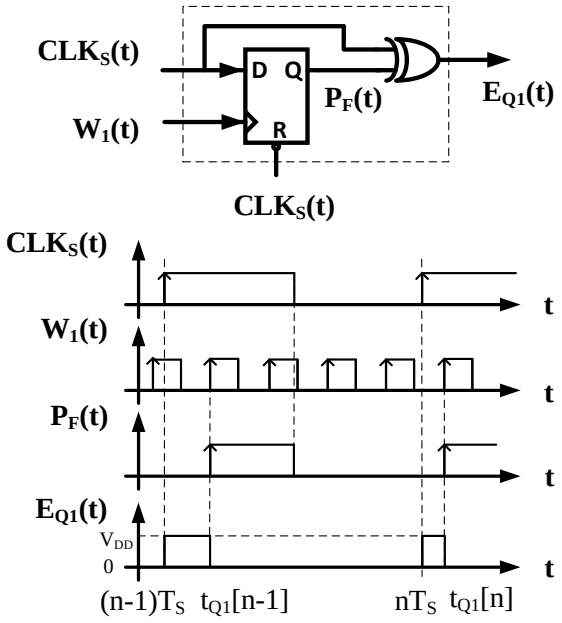


Figure 2.4: Block diagram and timing of QPD.

Compared to the architecture shown in Fig. 2.1, there is no first-order differentiator after Counter_1 and VCO_1 is used in a feedback loop. As shown below, the signal magnitude at the input of VCO_1 is small and this provides two benefits: 1) the linearity of the first stage is improved significantly, and 2) compared to the architectures in [10, 11], the quantization phase error of the first stage can be extracted in the time-domain as a two-level PWM signal. Therefore, the second stage is inherently linear. Also, there is no need for an additional PWM generator at the input.

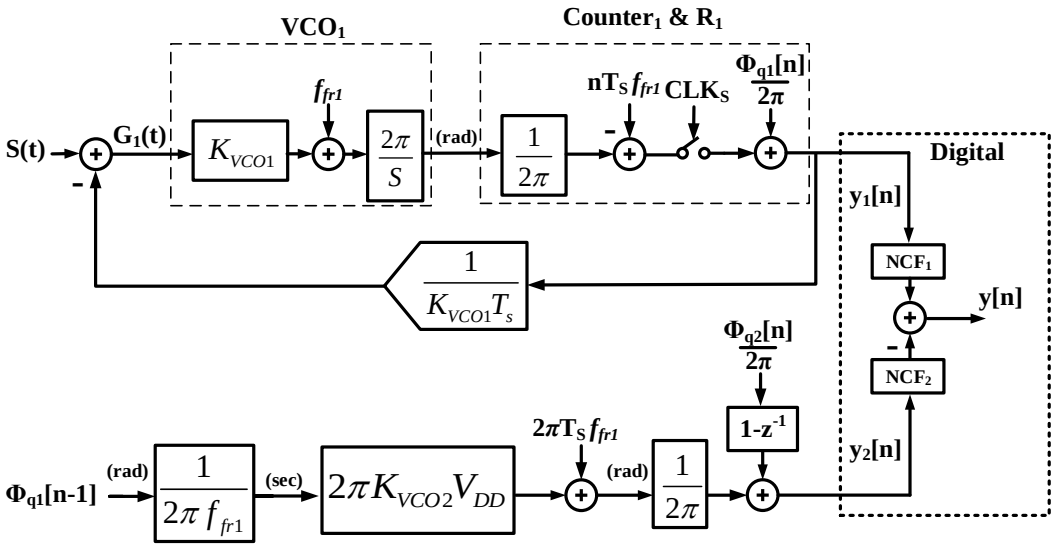


Figure 2.5: Linear model of the proposed 1-1 MASH.

A linear model of the proposed 1-1 MASH ADC is shown in Fig. 2.5. VCO_1 acts as a phase integrator. When the counter output unit increments, it indicates a phase change of 2π radians. The register samples the counter output at each rising edge of CLK_S. Therefore, $y_1[n]$ is proportional to the VCO_1 output phase

with some additional phase quantization noise. Due to the free running frequency of VCO_1, the sampled $\mathrm{Counter}_1$ output contains a ramp signal in the discrete time domain. To cancel the effect of the ramp signal in the linear model, $nT_S f_{fr1}$ is subtracted from the sampled $\mathrm{Counter}_1$ output. This issue is explained in more detail in Section 2.3.1.

Using the linear model shown in Fig. 2.5, the STF and NTF of the proposed 1-1 MASH can be calculated. The output of the first stage $Y_1(z)$ is:

$$Y_1(z) = \left(K_{VCO1} T_S z^{-1}\right) S(z) + \left(1 - z^{-1}\right) \frac{\phi_{q1}(z)}{2\pi} \tag{2.11}$$

Similar to (2.2), the quantization phase error (ϕ_{q1}) can be derived as a function of the VCO_1 input signal $G_1(t)$ as follows (refer to Figs. 2.3 and 2.4):

$$\begin{aligned} &\phi_{q1}\left((n-1)T_S\right) = \\ &\quad \int_{(n-1)T_S}^{t_{Q1}[n-1]} 2\pi \left(K_{VCO1} G_1(t) + f_{fr1}\right) dt \end{aligned} \tag{2.12}$$

Using (2.11), $G_1(z)$ can be calculated as:

$$\begin{aligned} G_1(z) = S(z) - \frac{Y_1(z)}{K_{VCO1} T_S} &= \left(1 - z^{-1}\right) S(z) \\ &\quad - \left(1 - z^{-1}\right) \frac{\phi_{q1}(z)}{2\pi \left(K_{VCO1} T_S\right)} \end{aligned} \tag{2.13}$$

In (2.12), $K_{VCO1} G_1(t)$ is negligible compared to f_{fr1} as explained next. As shown in (2.13), the first and the second terms of $G_1(z)$ are the first-order shaped input signal and the quantization noise, respectively. At a high enough oversam-

pling ratio (OSR), the signal magnitude at the VCO input is negligible. Since ϕ_{q1} has a value between zero and 2π radians, the maximum value of the second term is f_s/K_{VCO1}. Note that the value of f_{fr1} is chosen much higher than f_s in the design of a conventional counter based quantizer [19]. Therefore, f_{fr1} is much bigger than $K_{VCO1}G_1(t)$ and (2.12) can be simplified to:

$$\begin{aligned}\phi_{q1}\left(\left(n-1\right)T_S\right) \approx & \int_{(n-1)T_S}^{t_{Q1}[n-1]} 2\pi f_{fr1} dt \\ = & \frac{1}{V_{DD}} \int_{(n-1)T_S}^{nT_S} 2\pi f_{fr1} E_{Q1}(t) dt \\ = & 2\pi f_{fr1}\left(t_{Q1}\left[n-1\right] - \left(n-1\right)T_S\right)\end{aligned} \tag{2.14}$$

Equation (2.14) demonstrates that there is a linear relationship between the phase domain and time domain quantization noise. Therefore, the phase quantization error information can be extracted in the time domain as a pulse signal. The extracted quantization noise of the first stage ($E_{Q1}(t)$) is applied to the second stage which is implemented as an open loop VCO-based ADC. Since the input of this stage is in PWM form, the non-linearity of VCO_2 is no longer an issue. The phase output of VCO_2 and the second stage output code can be written as:

$$\phi_2\left(t\right) = \int_0^t 2\pi\left(K_{VCO2}E_{Q1}\left(t\right) + f_{fr2}\right)dt \tag{2.15}$$

$$\begin{aligned} y_2[n] = &\left(\int_{(n-1)T_S}^{nT_S} K_{VCO2}E_{Q1}(t)\,dt\right) \\ &+T_S f_{fr2} + \frac{\phi_{q2}(nT_S) - \phi_{q2}((n-1)T_S)}{2\pi} \end{aligned} \tag{2.16}$$

The first term of (2.16) matches (2.14) with a constant gain difference. Therefore, from (2.14) and (2.16) the following equation can be derived.

$$\begin{aligned} y_2[n] = &\frac{K_{VCO2}V_{DD}}{2\pi f_{fr1}}\phi_{q1}((n-1)T_S) \\ &+T_S f_{fr2} + \frac{\phi_{q2}(nT_S) - \phi_{q2}((n-1)T_S)}{2\pi} \end{aligned} \tag{2.17}$$

The term $T_S f_{fr2}$ is a constant value and can be easily removed in the digital domain. Therefore, $Y_2(z)$ is:

$$\begin{aligned} Y_2(z) = &\left(\frac{K_{VCO2}V_{DD}}{f_{fr1}}z^{-1}\right)\frac{\phi_{q1}(z)}{2\pi} \\ &+\left(1-z^{-1}\right)\frac{\phi_{q2}(z)}{2\pi} \end{aligned} \tag{2.18}$$

As shown in Fig. 2.5, to generate the MASH output code, $y[n]$, a simple set of digital filters are used as follows:

$$\begin{aligned} NCF_1(z) = &z^{-1} \\ NCF_2(z) = &\left(1-z^{-1}\right)\frac{f_{fr1}}{K_{VCO2}V_{DD}} \end{aligned} \tag{2.19}$$

Therefore, the final output is:

$$\begin{aligned} Y(z) =& NCF_1(z)\,Y_1(z) - NCF_2(z)\,Y_2(z) \\ =& z^{-2}\left(K_{VCO1}T_s\right)S(z) \\ &+\left(1-z^{-1}\right)^2\frac{f_{fr1}}{2\pi K_{VCO2}V_{DD}}\phi_{q2}(z) \end{aligned} \tag{2.20}$$

Equation (2.20) shows second order noise shaping. Considering the input signal is a sine wave, the maximum signal amplitude at the output (assuming N is large enough) is 2^{N-1}. Here N is the number of Counter$_1$ bits (2^N level quantizer). Therefore, the maximum signal power at the output is:

$$P_{sig-\max} = \left(\frac{2^{N-1}}{\sqrt{2}}\right)^2 = \frac{2^{2N}}{8} \tag{2.21}$$

Based on (2.20) the quantization noise power at the output can be calculated as:

$$\begin{aligned} P_{Q-noise} =& \\ &\int_{\frac{-f_S}{2OSR}}^{\frac{f_S}{2OSR}} \frac{\Delta^2}{12f_S}\left|\left(\frac{f_{fr1}}{2\pi K_{VCO2}V_{DD}}\right)\left(1-e^{-j\frac{2\pi f}{f_S}}\right)^2\right|^2 df \\ =&\left(\frac{f_{fr1}}{V_{DD}K_{VCO2}}\right)^2\frac{\pi^4}{60OSR^5} \end{aligned} \tag{2.22}$$

where, Δ is the LSB of ϕ_{q1} and is equal to 2π. Therefore, the peak signal-to-

quantization-noise ratio ($SQNR$) is

$$\begin{aligned} Peak\, SQNR &= 6 \cdot 02N - 11 \cdot 14 \\ &+50 \log (OSR) + 20 \log \left(\frac{V_{DD} K_{VCO2}}{f_{fr1}} \right) \end{aligned} \tag{2.23}$$

Choosing $f_{fr1} = V_{DD} K_{VCO2}$ results in the same $SQNR$ as a conventional second-order delta-sigma ADC with an N-bit quantizer [1].

2.3.1 Pseudo-differential implementation

In this sub-section, a pseudo-differential implementation of the proposed 1-1 MASH ADC is described. Fig. 2.6 shows the pseudo-differential architecture. In this architecture, two VCOs are arranged in a pseudo-differential manner in each stage. The output phase of the first stage is measured by comparing sampled Counter_{1P} and Counter_{1N} outputs. In this way, $\text{y}_1[n]$ represents the difference between the two VCO output phases.

Each of the positive and negative paths of the first stage act as a phase integrator followed by a quantizer. Therefore, two different quantization noise sources are in the first stage. As shown in Fig. 2.6, a pair of QPD blocks and a pseudo-differential second stage design are required to remove the first stage quantization noise at the output. As explained in the following, in the pseudo-differential structure, the free running frequency of the VCOs can be chosen arbitrarily.

In a standard VCO, the output phase is the integral of its frequency. The relation between the VCO_1 input voltage (node $G_1(t)$ shown in Fig. 2.3) and the

output phase is as below:

$$\phi_1(t) = \int_0^t (2\pi K_{VCO1} G_1(t) + 2\pi f_{fr1})\, dt \tag{2.24}$$

Counter_1 converts the phase information to an integer number. According to (2.24), even if $G_1(t)$ is zero, the output frequency of VCO_1 is f_{fr1} and the Counter_1 output increases as time goes by. Counter_1 changes counting direction whenever it reaches its range boundaries. Therefore, the sampled Counter_1 output of a single VCO does not convey phase information.

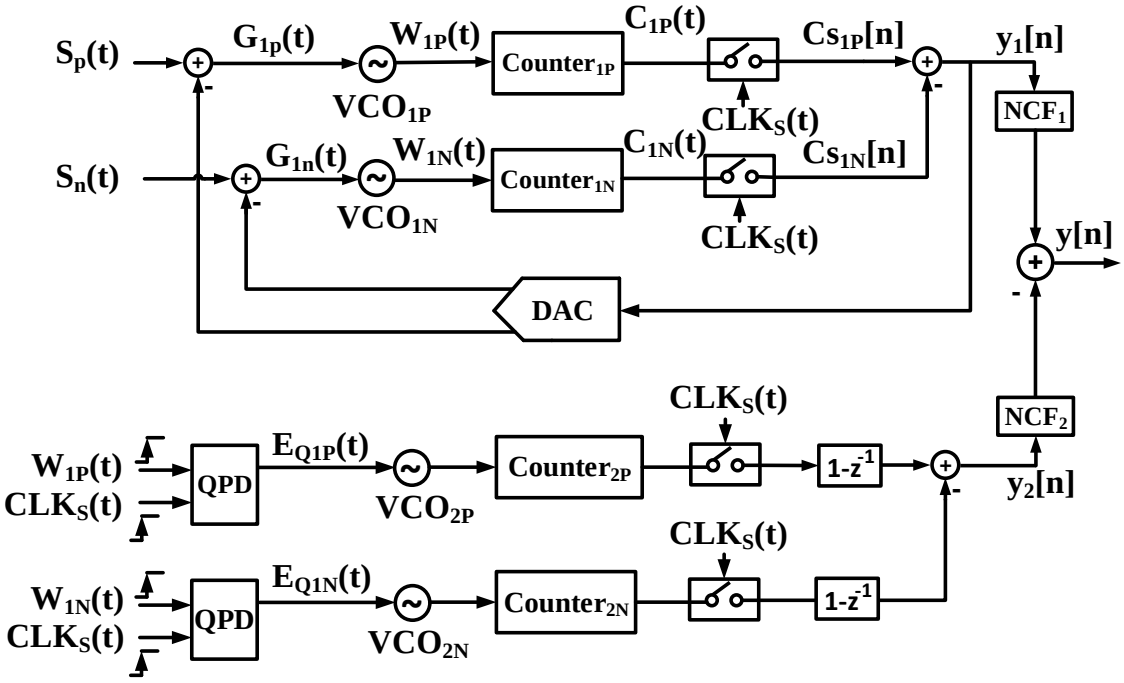


Figure 2.6: Pseudo-differential structure of the proposed 1-1 MASH.

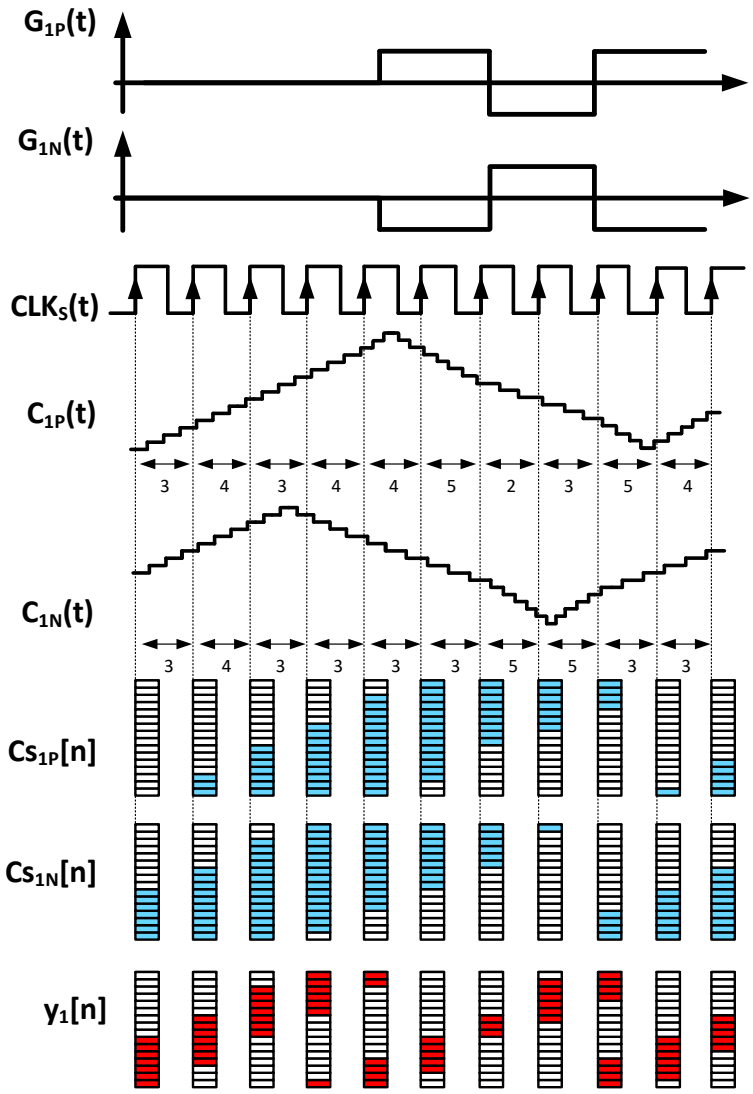


Figure 2.7: Example of phase extraction in the proposed pseudo-differential architecture.

However, this problem is solved in the pseudo-differential structure. The output phases of VCO_{1P} and VCO_{1N} shown in Fig. 2.6 are as follows:

$$\phi_{1P,N}(t) = \int_0^t \left(2\pi K_{VCO1P,N} G_{1P,N}(t) + 2\pi f_{fr1P,N}\right) dt \tag{2.25}$$

Similar to (2.2) $C_{S1P}[n]$ and $C_{S1N}[n]$ are:

$$\begin{aligned} Cs_{1P,N}[n] =& \frac{\phi_{1P,N}(nT_S) + \phi_{q1P,N}(nT_S)}{2\pi} \\ =& \int_0^{nT_S} \left(K_{VCO1P,N} G_{1P,N}(t) + f_{fr1P,N}\right) dt \\ &+ \frac{\phi_{q1P,N}(nT_S)}{2\pi} \end{aligned} \tag{2.26}$$

Assuming $K_{VCO1P} = K_{VCO1N} = K_{VCO1}$ and $f_{fr1P} = f_{fr1N} = f_{fr1}$, by taking the difference of $C_{S1P}[n]$ and $C_{S1N}[n]$, the first stage output is:

$$\begin{aligned} y_1[n] =& Cs_{1P}[n] - Cs_{1N}[n] \\ =& \int_0^{nT_S} K_{VCO1}\left(G_{1P}(t) - G_{1N}(t)\right) dt \\ &+ \frac{\phi_{q1P}(nT_S) - \phi_{q1N}(nT_S)}{2\pi} \end{aligned} \tag{2.27}$$

and f_{fr1} is completely removed at the first stage output. Note that, based on (2.13), $G_{1P}(t)$ and $G_{1N}(t)$ are the shaped input signal minus the shaped quantization noise. Fig. 2.7 shows an example of f_{fr1} cancelation in the first stage of the proposed pseudo-differential structure. In this example, a pair of 4 bit counters (16 level quantizer) is used. Also, f_{fr1} is assumed to be around $3.5\times f_S$. In the

real implementation, counters have limited output range and the counter output changes direction every time it reaches its highest and lowest counts. To account for this issue, the subtraction of Counter_{1P} and Counter_{1N} outputs is done by XORing the sampled counter outputs shown as $y_1[n]$ in Fig. 2.7. Since f_{fr1} is canceled at the output, it can be chosen arbitrarily.

In Fig. 2.7, $y_1[n]$ is the output code which corresponds to the DAC selection pattern. The middle point of $y_1[n]$, which is the DAC middle point, rotates at approximately $f_{fr1}/16$ in this example. This results in an inherent clock averaging (CLA) pattern in the proposed ADC [14]. A proper choice of f_{fr1} pushes the harmonics caused by DAC mismatch out of band. Thus, there is no need for an explicit dynamic element matching (DEM) technique [14].

In the proposed pseudo-differential structure, since VCO_{1P} and VCO_{1N} are identical, in the absence of mismatches, PVT variations affect the free running frequency of both VCOs in the same way. Therefore, the performance does not change. Also, due to the pseudo-differential structure, even order harmonics are canceled at the output. The behavioral model of the pseudo-differential architecture is simulated in Simulink/MATLAB. Fig. 2.8 shows the PSD of the pseudo-differential structure using the parameters in Table 2.1. Fig. 2.8 shows that the desired second-order noise shaping is achieved.

Table 2.1: Specifications of the proposed 1-1 MASH

Spec.	Value	Spec.	Value
$f_{fr1}(Hz)$	$16 \times f_S$	N	5
$K_{VCO1}(Hz/V)$	$30 \times f_S$	OSR	32
$K_{VCO2}(Hz/V)$	$16 \times f_S$	Input amp. (dBFS)	-0.6
$V_{DD}(V)$	1		

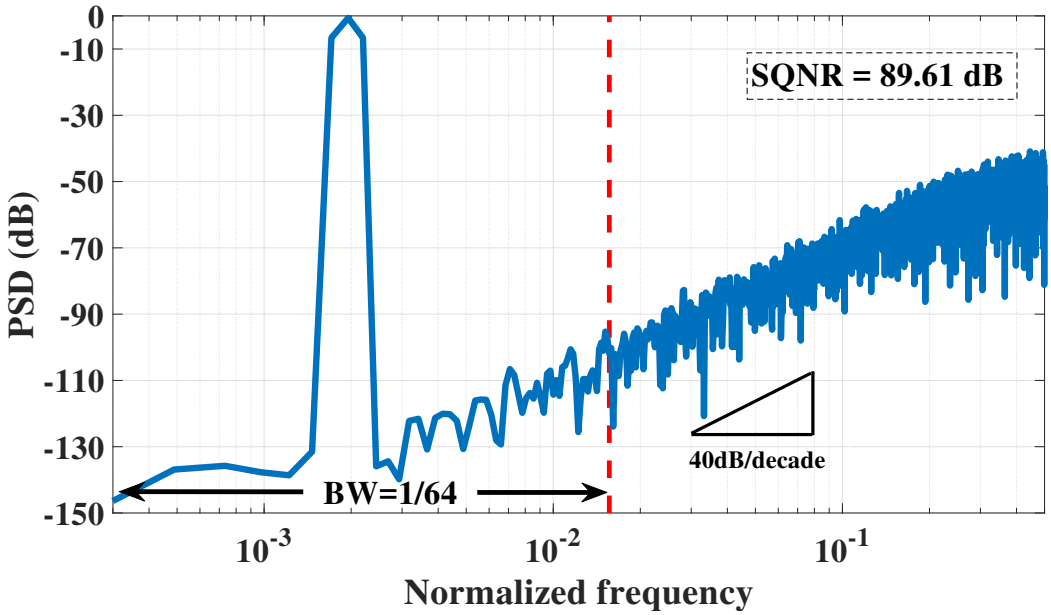


Figure 2.8: PSD of the proposed pseudo-differential 1-1 MASH.

In the next section, the performance of the proposed ADC is examined for different design parameters.

2.4 Performance Analysis with Design Parameters

In MASH ADC architectures an interstage gain can be used between different stages to enhance the $SQNR$. In the proposed scheme, there is an inherent interstage gain between the first stage and the second stage which can be used to improve the output $SQNR$. In this section, this technique is discussed and verified through comprehensive simulations.

2.4.1 SQNR enhancement

As shown in (2.23), the last term of the equation affects the $SQNR$. In the linear model shown in Fig. 2.5, $(V_{DD}K_{VCO2})/f_{fr1}$ acts as an inter-stage gain, which can be used to improve $SQNR$ for the two stage MASH structure. Fig. 2.9 shows the peak $SQNR$ versus $(V_{DD}K_{VCO2})/f_{fr1}$. In this simulation, f_{fr1} and V_{DD} are kept constant and K_{VCO2} has been swept. The ADC design parameters used in this simulation are shown in Table 2.2.

As can be inferred from Fig. 2.9, the peak $SQNR$ saturates for high K_{VCO2} values. This limitation on the maximum achievable $SQNR$ stems from an earlier approximation made from (2.12) to (2.14). This issue is investigated in more detail in the following section.

Table 2.2: Specifications of the proposed 1-1 MASH

Spec	**Value**	**Spec**	**Value**
$f_{fr1}(Hz)$	$16 \times f_S$	N	5
$K_{VCO1}(Hz/V)$	$(2^N - 2) \times f_S$	OSR	32
$f_{in}(Hz/V)$	BW	Input amp. (dBFS)	-0.6
$V_{DD}(V)$	1		

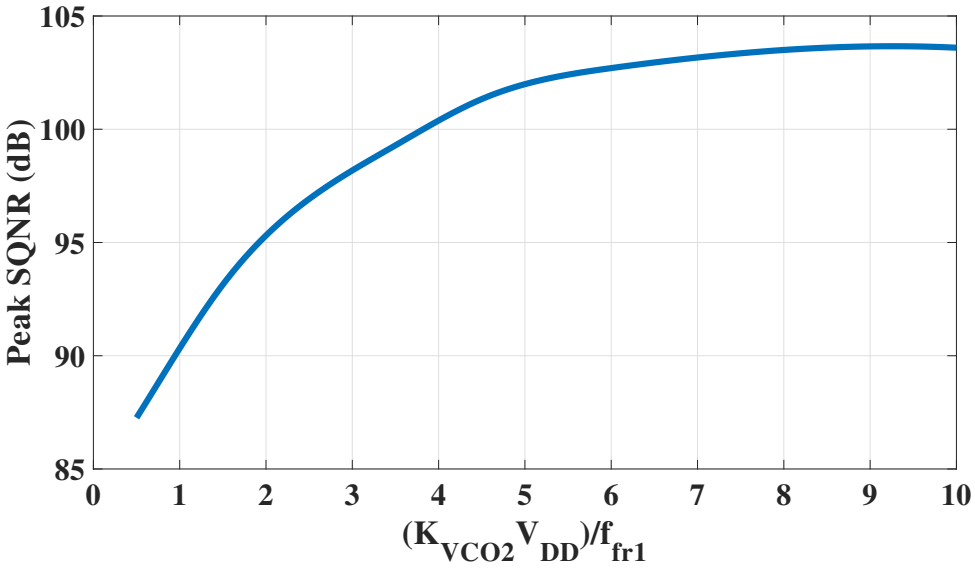


Figure 2.9: Peak $SQNR$ vs. $(V_{DD}K_{VCO2}/f_{fr1})$.

2.4.2 Estimation of phase domain quantization noise of the first stage in time domain

The quantization noise of the first stage is in the phase domain (2.12). As shown in (2.14), if the frequency variation of VCO_1 ($K_{VCO1}G_1(t)$) is small compared to f_{fr1}, the quantization noise can be extracted in the time domain. Because of this approximation, there is always some ϕ_{q1} leakage to the output. Assuming $\alpha\phi_{q1}$ is the error due to this approximation of ϕ_{q1} at the second stage input, $\alpha\phi_{q1}NCF_2$ is the error at the final output. Considering αNCF_2=$L(z)$, (2.20) can be modified to:

$$\begin{aligned} Y(z) = & z^{-2}\left(K_{VCO1}T_s\right)S(z) \\ & + \left(1-z^{-1}\right)^2\frac{f_{fr1}}{2\pi K_{VCO2}V_{DD}}\phi_{q2}(z) \\ & + L(z)\,\phi_{q1}(z) \end{aligned} \tag{2.28}$$

Since NCF_2 has a first-order noise shaping transfer function, the error in ϕ_{q1} extraction gets one order of noise shaping at the final output.

Based on (2.28), if $(V_{DD}K_{VCO2})/f_{fr1}$ is high enough, the peak $SQNR$ is limited to $L(z)\phi_{q1}(z)$ as shown in Fig. 2.9. To investigate the effect of $L(z)\phi_{q1}(z)$ on $SQNR$, $(V_{DD}K_{VCO2})/f_{fr1}$ is assumed to be high enough so that the effect of ϕ_{q2} can be neglected on the peak $SQNR$ in the following analysis. Hereafter, the peak $SQNR$ limited to $L(z)\phi_{q1}(z)$ is called the maximum achievable $SQNR$.

$L(z)$ is a function of the relative VCO_1 frequency variation with respect to f_{fr1}. In order to reduce $L(z)$, VCO_1 frequency variation with respect to f_{fr1} has to be

reduced. From (2.12) and (2.13) it can be seen that the frequency of VCO_1 is:

$$\begin{aligned} freq_{VCO1}(z) =& K_{VCO1}G_1(z) + f_{fr1} \\ =& \left(1 - z^{-1}\right) K_{VCO1}S(z) \\ &+ \left(1 - z^{-1}\right) \frac{f_s \phi_{q1}(z)}{2\pi} + f_{fr1} \end{aligned} \tag{2.29}$$

Equation (2.29) shows that the $freq_{VCO1}$ is a function of both the shaped input signal and the shaped quantization noise. Maximum $freq_{VCO1}$ variation happens when the first two terms of (2.29) have their maximum variation. The maximum amplitude of the first stage output ($y_1[n]$) is 2^{N-1}. Therefore, based on the transfer function in (2.11), the maximum value of $K_{VCO1}S(z)$ is approximately $2^{N-1}f_S$. The first term of (2.29) is a difference of two consecutive samples of the input signal multiplied by K_{VCO1}. Therefore, the maximum variation of the first term of (2.29) is:

$$\begin{aligned} &\Delta_{\max}\left(\left(1 - z^{-1}\right) K_{VCO1}S(z)\right) \\ &= Max\left(\left(1 - z^{-1}\right) K_{VCO1}S(z)\right) \\ &- Min\left(\left(1 - z^{-1}\right) K_{VCO1}S(z)\right) \\ &= \left|\left(1 - e^{-\frac{j\pi}{OSR}}\right)\right| 2^N f_S \end{aligned} \tag{2.30}$$

ϕ_{q1} has a value between 0 to 2π. As a result, the maximum difference of two consecutive samples of ϕ_{q1} is 2π. Thus, the maximum variation of the second term

in (2.29) is:

$$\Delta_{\max}\left(\left(1-z^{-1}\right)\frac{f_s\phi_{q1}\left(z\right)}{2\pi}\right)=f_S \tag{2.31}$$

Based on (2.30) and (2.31), the maximum $freq_{VCO1}$ variation normalized to f_{fr1} is:

$$\frac{\Delta_{\max}\left(freq_{VCO1}\right)}{f_{fr1}}=\left(\left|\left(1-e^{-\frac{j\pi}{OSR}}\right)\right|2^N+1\right)\frac{f_S}{f_{fr1}} \tag{2.32}$$

In the following sub-sections, the effects of N, OSR, and f_{fr1} on the maximum achievable SQNR are investigated through behavioral model simulations. The design parameters of the ADC used in these simulations are shown in Table 2.2. In these simulations the value of K_{VCO2} is chosen high enough to ensure that the maximum $SQNR$ is achieved for the parameters used.

2.4.2.1 Effect of N

The first stage is a first order delta-sigma modulator with an N-bit quantizer. The maximum peak-to-peak swing of the ADC output is 2^N. Therefore, increasing N, results in a higher maximum signal swing at the output. It is expected that the maximum achievable $SQNR$ increases by 6 dB with each increment of N. On the other hand, (2.32) shows that increasing N results in more $freq_{VCO1}$ variation with respect to f_{fr1}. Therefore, increasing N results in more ϕ_{q1} leakage ($L(z)$) to

the output. Hence, less than 6 dB improvement in maximum $SQNR$ is achieved. The maximum achievable $SQNR$ is simulated for the proposed scheme for different values of N in Fig. 2.10. As can be seen, since ϕ_{q1} leakage increases with increasing N, the maximum achievable $SQNR$ improvement is less than 6 dB for each increment of N.

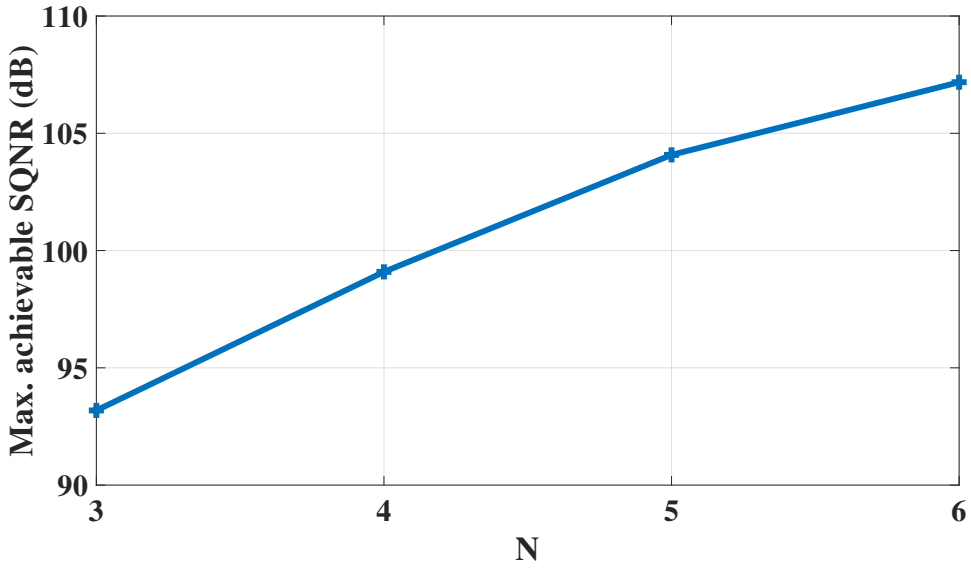


Figure 2.10: Maximum achievable $SQNR$ for different values of N.

2.4.2.2 Effect of OSR

By increasing OSR, the difference of the input signal between two consecutive samples becomes smaller. Therefore, the input voltage variation for VCO_1 due to the ADC input voltage is less. For a fixed value of N, this results in a smaller $freq_{VCO1}$ variation (Eq. (2.32)). As a result, a more accurate relation between

the time domain and the phase domain quantization noise is achieved. Therefore, the maximum achievable $SQNR$ increases by increasing OSR. The maximum achievable $SQNR$ is simulated for the proposed scheme for different values of OSR in Fig. 2.11. In this simulation f_{in} is kept at the edge of the BW. As can be seen in Fig. 2.11, the rate of maximum achievable $SQNR$ improvement is smaller for higher values of OSR. This is due to the fact that the maximum $freq_{VCO1}$ variation relative to f_{fr1} in (2.32) is due to the signal variation (the first term) and the quantization noise variation (the second term). Since the $freq_{VCO1}$ variation due to the quantization noise is not a function of OSR, for higher values of OSR, the second term in (2.32) becomes comparable to the first term. This limits the maximum achievable $SQNR$.

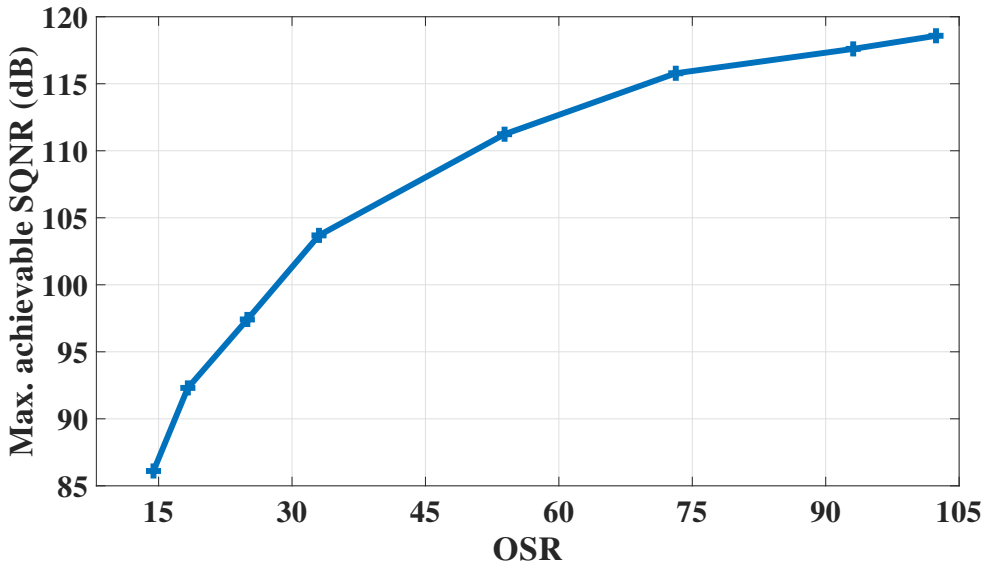


Figure 2.11: Maximum achievable $SQNR$ for different values of OSR.

2.4.2.3 Effect of f_{fr1}

As discussed in Section 2.3.1, f_{fr1} is removed at the pseudo-differential structure output and, therefore, its value can be chosen arbitrarily. Equation (2.12) shows that increasing f_{fr1} makes $K_{VCO1}G_1(t)$ negligible compared to f_{fr1}. Therefore, increasing f_{fr1} makes the relation between phase and time domain information (as shown in (2.14)) more linear. The maximum achievable $SQNR$ is simulated for the proposed scheme for different values of f_{fr1} in Fig. 2.12. Although the maximum achievable SQNR improves for higher f_{fr1}, as (2.23) suggests a higher value of K_{VCO2} is required to achieve a high $SQNR$. On the other hand, a higher f_{fr1} requires a faster VCO_1 and Counter_1 in the design. This increases the power consumption and the circuit implementation complexity.

Generally, for higher speed applications, the required $SQNR$ of the ADCs is less than lower speed applications. Therefore, depending on the required $SQNR$, f_{fr}/f_S can be chosen to reasonably meet the design requirements. Based on Fig. 2.12, even if f_{fr}/f_S is in the range of 2 to 4, a $SQNR$ of more than $80dB$ is still achievable using the parameters of Table 2.2.

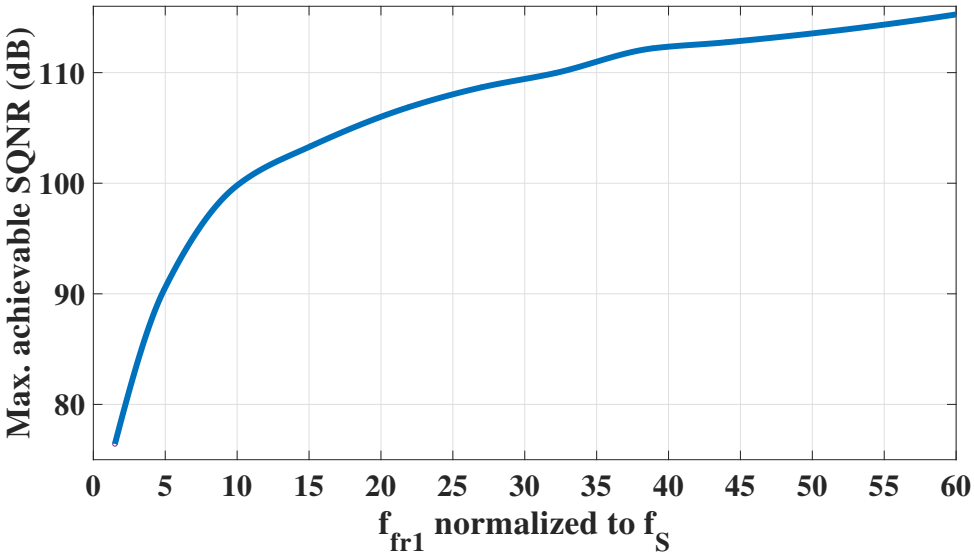


Figure 2.12: Maximum achievable $SQNR$ for different values of f_{fr1}.

2.5 Effect of Non-Idealities

In a real implementation, non-idealities degrade the performance of the ADC. In this section, some of the non-ideality factors and related solutions, listed in Table 2.3, are described. The effect of each non-ideality factor on the performance of the proposed scheme is explained and Simulink/MATLAB simulation results are presented. The ADC design parameters are the same as in Table 2.2.

Table 2.3: Non-idealities and related solutions

Non-ideality	**Solution**
VCO non-linearity	VCO_1 is in a feedback loop and a two level PWM signal drives VCO_2
Mismatch between analog and digital filters	Calibration
VCO mismatch	Low sensitivity
Missing narrow pulses in Q extraction path	Pulse width extension
Propagation delay in QPD block	Low sensitivity
Setup/hold times of the quantizer	Modified quantizer
Rise/fall times of the QPD	Low sensitivity

2.5.1 VCO non-linearity

The VCO non-linearity is the major bottleneck in designing VCO-based ADCs. To mitigate this issue, the first stage VCO is used as a phase integrator. Therefore, the signal variation at the input of the VCO is small. As a result, the non-linearity of VCO_1 is suppressed significantly [15]. The input of the second stage VCO is a two level PWM signal. Therefore, VCO_2 operates linearly as well [12].

In order to investigate the effect of the non-linearity on the proposed ADC, a non-linear V-to-F tuning characteristic (extracted from VCO transistor level simulations), is used for all the VCOs in the behavioral model. Fig. 2.13 shows the FFT of the output of a pseudo-differential stand-alone open loop VCO-based ADC, using the same V-to-F tuning characteristic. The signal to quantization noise and distortion ratio ($SNDR$) is limited to 38 dB in the standalone VCO-based topology.

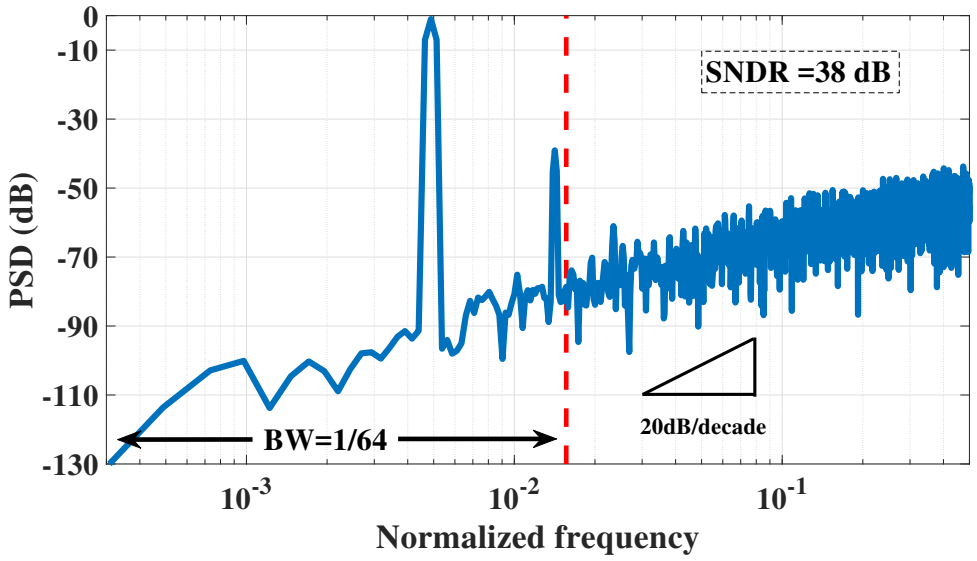


Figure 2.13: PSD of the output of a pseudo-differential open loop VCO-based ADC.

As shown in (2.13), in the proposed architecture, the input signal of VCO_1 ($G_1(t)$) contains a shaped input signal (the first term) and the shaped quantization noise (the second term). Assuming the OSR is high enough, the first term is small and the non-linearity introduced by the input signal is greatly suppressed. On the other hand, the magnitude of the shaped quantization noise can be large such that it limits the $SNDR$. Due to the non-linear characteristic of the VCO, high frequency components of the shaped quantization noise get modulated to the in-band frequency range and degrade the performance. Fig. 2.14 shows the maximum achievable $SNDR$ vs. N for two scenarios, with and without the VCO non-linearity. As can be observed in this figure, the degradation due to the VCO

non-linearity reduces significantly by increasing N.

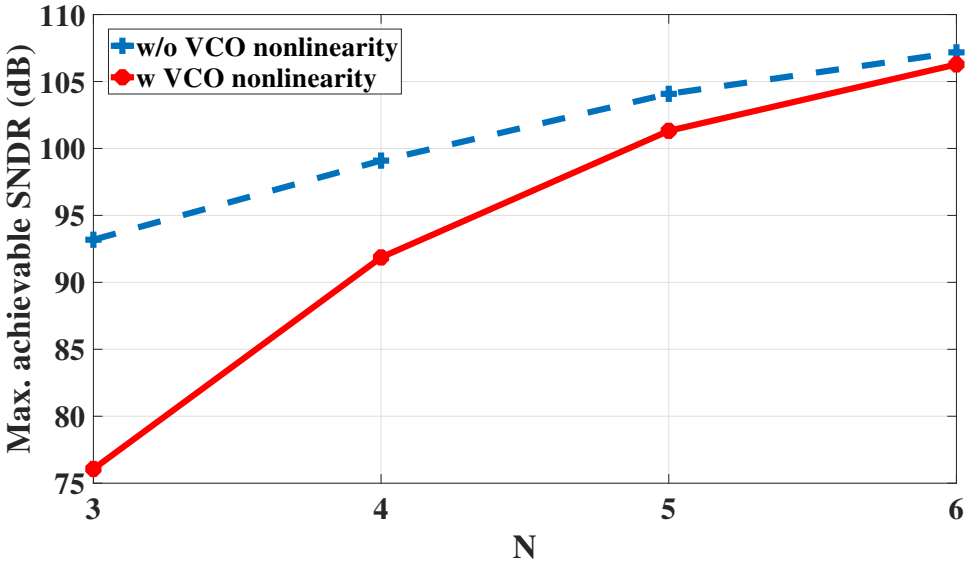


Figure 2.14: Maximum achievable $SNDR$ of the proposed ADC vs. N, with linear and non-linear VCO.

2.5.2 Mismatch between analog and digital filters

Mismatch between the analog and digital filters is a common issue for MASH structures [1]. This problem leads to quantization noise leakage to the output. Equation (2.19) shows NCF_2 is a function of f_{fr1} and $K_{VCO2}V_{DD}$. Fig. 2.15 shows the output $SQNR$ variation due to mismatch between $f_{fr1}/(K_{VCO2}V_{DD})$ in NCF_2 and its ideal analog value. As can be seen, in the presence of $\pm 10\%$ mismatch between the analog and digital filters, a $SQNR$ of more than 85 dB is achievable, using the parameters of Table 2.2.

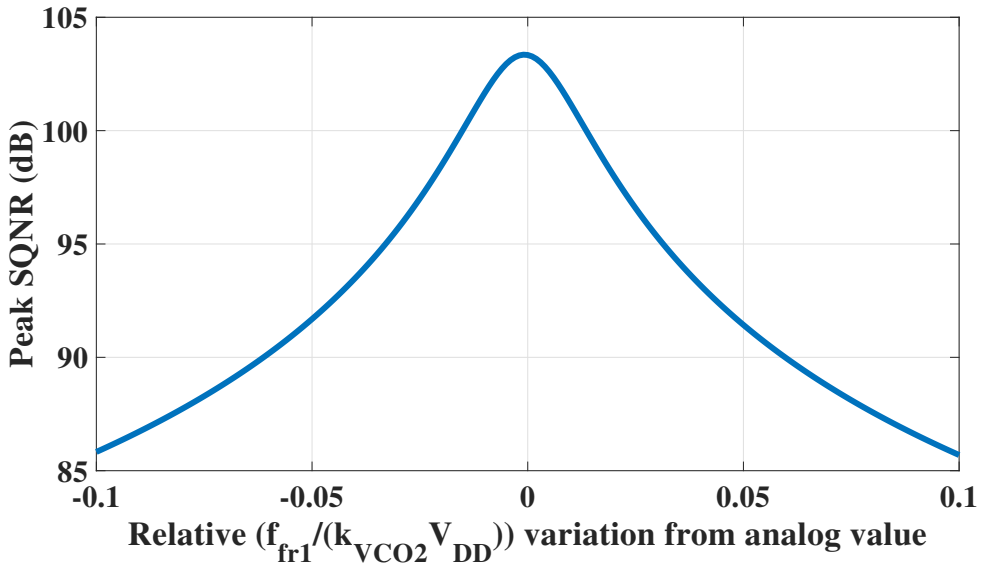


Figure 2.15: $SQNR$ vs. $f_{fr1}/(K_{VCO2}V_{DD})$ variation from its nominal value.

In order to reduce the analog and digital filtering mismatch, a simple calibration method can be used. The ratio of $f_{fr1}/(K_{VCO2}V_{DD})$ needs to be calculated precisely in the digital domain to match the analog value. In the beginning of the calibration, the first stage loop is broken and VCO_1 is connected to the AC ground (DC common-mode voltage). As shown in Fig. 2.16(a), a digital differentiator is used after $\mathrm{Counter}_1$ to extract the frequency information of VCO_1. $D_1(z)$ is as follows:

$$D_1(z) = f_{fr1}T_S + \left(1 - z^{-1}\right)\frac{\phi_{q1}(z)}{2\pi} \tag{2.33}$$

In (2.33) by averaging multiple samples of $D_1[n]$, the shaped quantization noise

is reduced and $f_{fr1}T_S$ can be extracted.

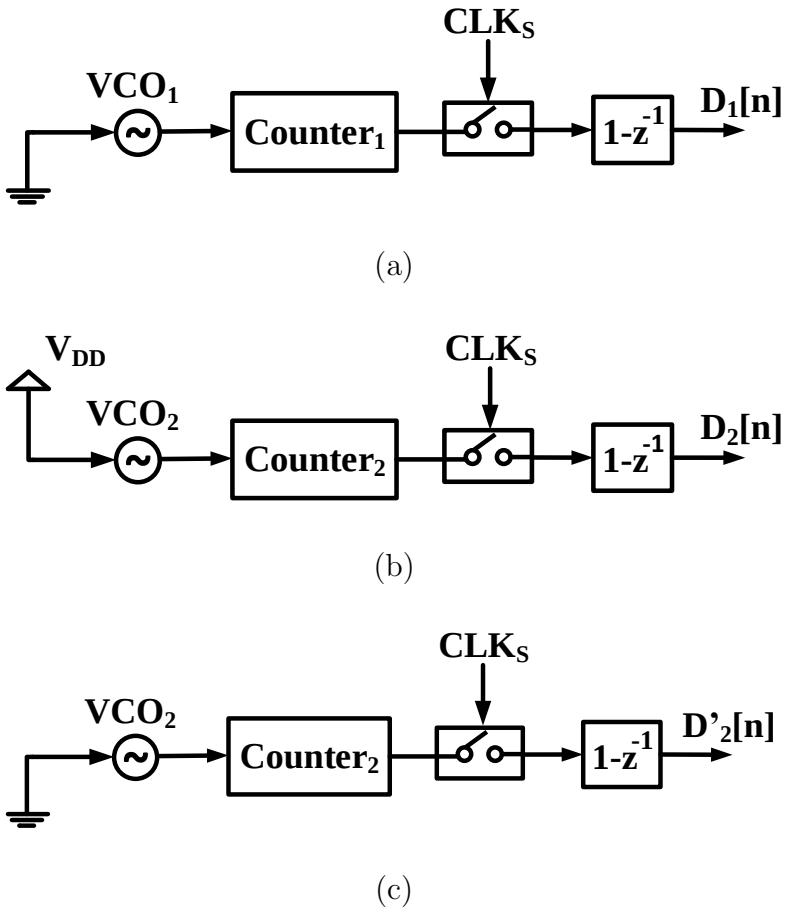


Figure 2.16: Proposed calibration method. (a) f_{fr1} extraction, (b) K_{VCO2} extraction - phase 1, (c) K_{VCO2} extraction - phase 2.

Next, extracting $K_{VCO2}V_{DD}T_S$ takes place in two different phases. First, VCO_2 is connected to V_{DD} as shown in Fig. 2.16(b) and the frequency information is

extracted as below:

$$\begin{aligned} D_2(z) =& K_{VCO2}V_{DD}T_S + f_{fr2}T_S \\ &+ \left(1 - z^{-1}\right)\frac{\phi_{q2}(z)}{2\pi} \end{aligned} \tag{2.34}$$

In the second phase, VCO_2 is connected to the ground as shown in Fig. 2.16(c). Equation (2.35) shows its frequency information.

$$D_2'(z) = f_{fr2}T_S + \left(1 - z^{-1}\right)\frac{\phi_{q2}(z)}{2\pi} \tag{2.35}$$

By averaging multiple samples of $D_2[n]$ and $D_2[n]$ as before and subtracting the averaged values, $K_{VCO2}V_{DD}T_S$ can be extracted. By knowing $f_{fr1}T_S$ and $K_{VCO2}V_{DD}T_S$ values, NCF_2 can be accurately calibrated in the digital domain and the $SQNR$ reduction can be corrected.

2.5.3 VCO mismatch

There are two types of mismatch with respect to the VCOs. The first type is the mismatch among different delay cells of a VCO. The second type is the mismatch between the two VCOs. Since in the proposed architecture only one delay element drives the counter, mismatch between delay cells does not degrade the performance. Although this mismatch can change K_{VCO} and f_{fr} of each VCO, this can be modeled as a mismatch between the different VCOs.

In the proposed pseudo-differential structure, the design specifications of the

first stage VCO and the second stage VCO dont need to be identical. Therefore, they can be designed independently.

The mismatch between f_{fr1P} and f_{fr1N} causes offset at the first stage output, which results in a dynamic range (DR) reduction.

Since, the input signal swing at the VCO_1s' inputs is small, the mismatch between K_{VCO1P} and K_{VCO1N} does not degrade the output $SQNR$. This is simulated in Fig. 2.17.

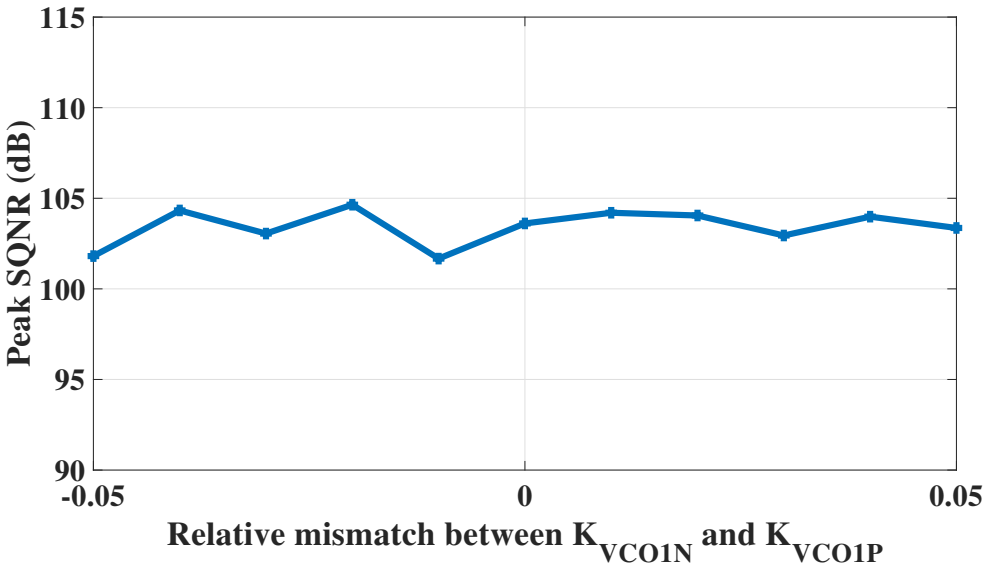


Figure 2.17: Effect of VCO mismatch on the pseudo-differential structure.

The second stage is a pair of open loop VCO quantizers operating in the frequency domain. Mismatch between f_{fr2P} and f_{fr2N} results in an offset in the second stage output. This offset can be avoided by measuring f_{fr2P} and f_{fr2N} in the calibration phase, similar to Fig. 2.16(b). Also, K_{VCO2P} and K_{VCO2N} can be

measured in the calibration phase and therefore their mismatch can be compensated in digital filters.

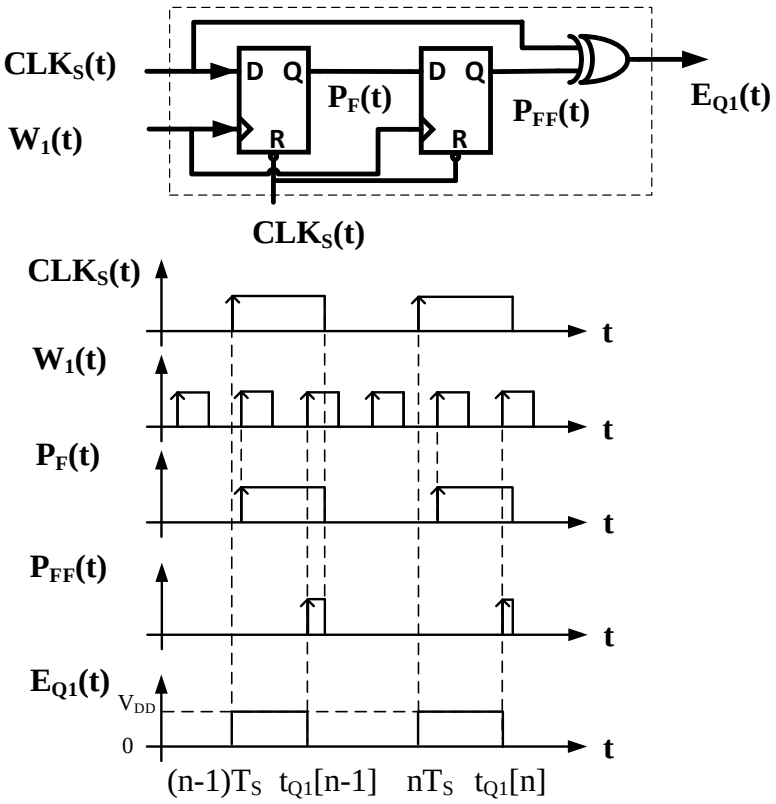


Figure 2.18: Pulse width extension in the QPD block.

2.5.4 Effect of narrow pulses in Q extraction path

As shown in (2.14) the pulse width of $E_{Q1}(t)$ (shown in Fig. 2.3) is a linear function of the phase quantization noise of the first stage. This pulse width can be very narrow and if it is smaller than the rise time of the QPD block, the pulse can

be missed. Also in practice, the second stage VCO does not switch immediately between two frequency states when a pulse is applied to its input. Therefore, if the pulse width is too small, VCO_2 is not able to reach its expected high frequency before the pulse goes down again. This will degrade the performance. To avoid this degradation due to missing pulses, a pulse extension technique is used [11]. In this technique, the pulse width is increased by one LSB, which is equal to 2π radians and $1/f_{fr1}$ seconds in the phase and time domain, respectively, as shown in Fig. 2.18. Since one LSB is added to all quantization noise samples, it acts as an offset and gets removed after the digital differentiator of the second stage. Therefore, it does not affect the performance of the ADC. Fig. 2.19 shows the PSD of the overall modulator with and without the pulse extension technique. In the behavioral simulation, the rise time of the XOR gate in the QPD blocks is assumed to be 3 percent of the sampling period. It can be inferred from Fig. 2.19 that the pulse extension technique improves the $SQNR$ by 20 dB.

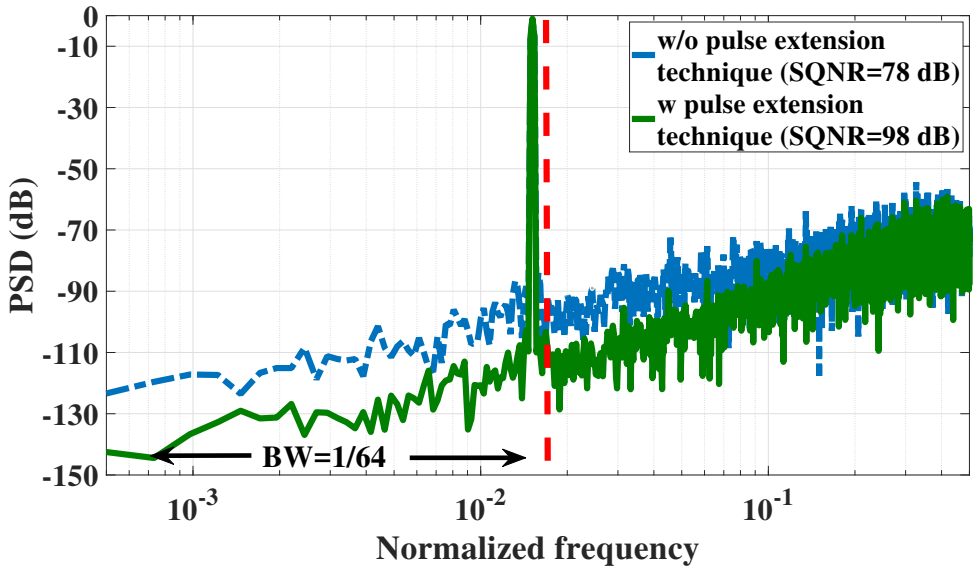


Figure 2.19: Effect of pulse width extension technique on the proposed 1-1 MASH ADC.

2.5.5 Effect of propagation delay in QPD block

As shown in Fig. 2.18 two flip-flops and an XOR gate are used in the QPD block. In practice, each of these blocks have a propagation delay. The effect of this propagation delay on the pulse width is shown in Fig. 2.20. In this figure, $T_{pd,FF}$ and $T_{pd,XOR}$ are the propagation delay of each flip-flop and XOR gates. A comparison of Fig. 2.18 and Fig. 2.20, shows that the propagation delay has the following effect on the generated pulse ($E_{Q1}(t)$). $E_{Q1}(t)$ signal gets shifted by $T_{pd,XOR}$ and its pulse width increases by $T_{pd,FF}$. Also, it generates an extra narrow pulse with a constant width of $T_{pd,FF}$ in each sampling period. Since all of these time shifts due

to the propagation delays are the same for all the samples, they act as an offset and can be removed after the digital differentiator. Therefore, the propagation delay has no effect on the performance.

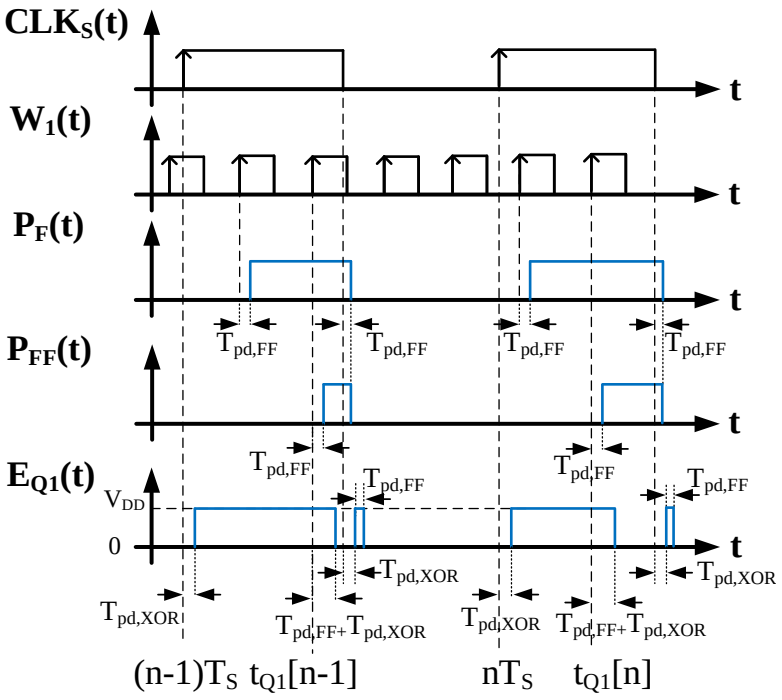


Figure 2.20: Effect of propagation delay on $E_{Q1}(t)$.

2.5.6 Effect of non-zero setup/hold times of the quantizer

Fig. 2.21 shows the first stage quantizer (Counter$_1$ and sampling flip-flops), QPD and their corresponding waveforms. A 3-bit quantizer is shown for simplicity while the real implementation is 5-bit. The counter is made of a chain of back-to-back connected flip-flops. The counter output changes by one unit at each rising edge

of the VCO_1 output (W_1(t)). The counter output is sampled by a set of flip-flops.

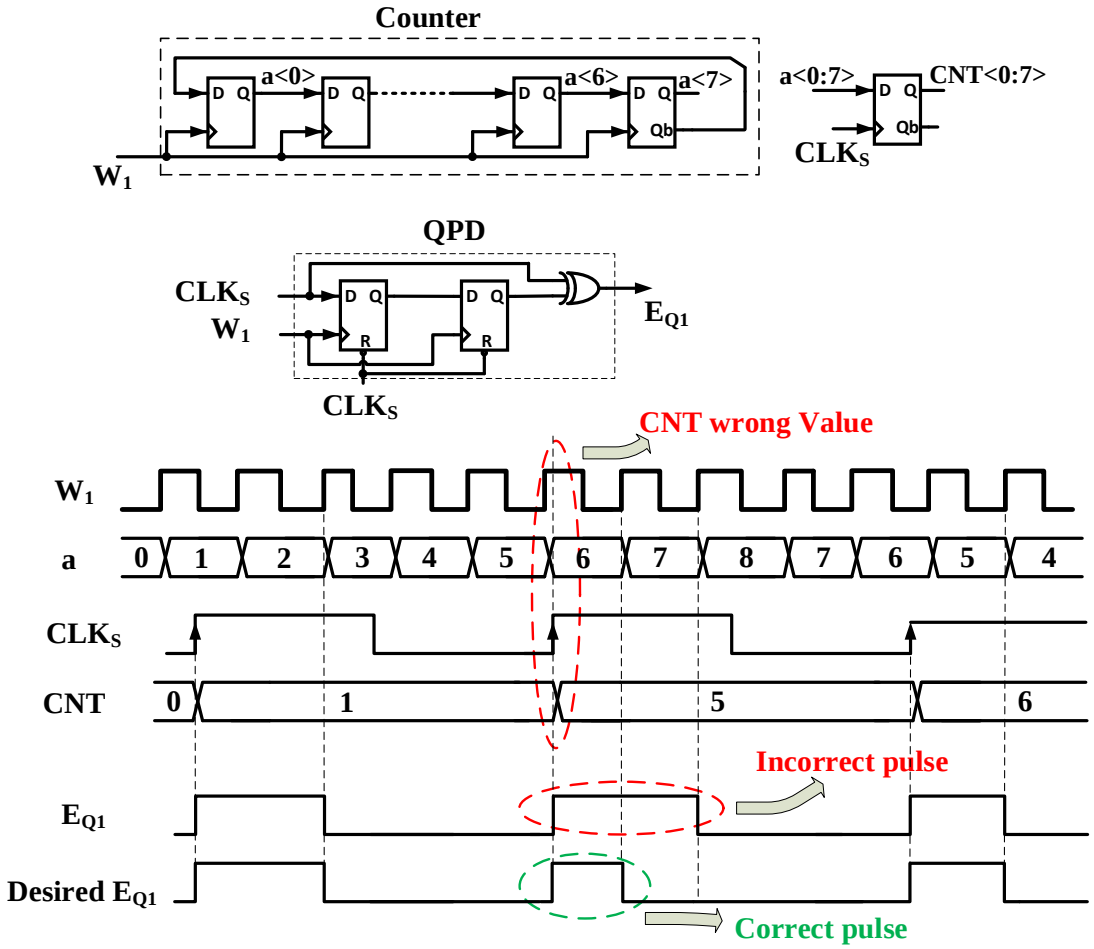


Figure 2.21: Effect of non-zero setup/hold times of the quantizer.

As can be seen in Fig. 2.21, if the rising edge of VCO_1 ($W_1(t)$) happens right before the rising edge of CLK_S, the sampled output might be an incorrect value by one unit (LSB). This can be a problem due to the fact that the QPD block works independent of the output digital value and does not incorporate the quantizer

incorrect decision in the ϕ_{Q1} extraction. Therefore, the $E_{Q1}(t)$ pulse width is one LSB more than what it should have been for some of the samples for which this error occurs. Since, the quantizer failed to detect the $W_1(t)$ rising edge, the quantizer assumes this rising edge happened right after the sampling instant. Therefore, the proper pulse should be the one as shown in Fig. 2.21 as Desired $E_{Q1}(t)$

This error adds one LSB for some of the codes (not all of them). Therefore, this error is not like an offset and will degrade the performance. Fig. 2.22 shows the proposed method to resolve this issue. As can be seen, a set of latches has been added between the counter and the sampling FFs. The latches are controlled by the CLK_{Setup} signal. They are transparent when CLK_{Setup} is high and they hold their values when CLK_{Setup} is low. CLK_{Setup} is also shown in Fig. 2.22. The above mentioned problem stems from the setup/hold times of the sampling FFs. CLK_{Setup} is low for some time before and after the sampling instant. This way, the data at the input of the sampling FFs remains constant and therefore, the setup/hold times of the FFs will not be violated. Signal AA in Fig. 2.22 shows the output of the latches. As can be seen, when the rising edge of $W_1(t)$ is close to the rising edge of the CLK_S, signal AA, shows a small time shift compared to signal a. In other words, for some VCO rising edges, a small amount of extra phase shift is added to avoid violating the setup/hold times of the FFs.

To be able to extract ϕ_{Q1}, the same delay has to be applied to $W_1(t)$ when going through the ϕ_{Q1} extraction path. This is shown in Fig. 2.22 as well. A FF and a latch are added in the path of the $W_1(t)$ signal. This combination copies the delay in the quantizer due to the counter and the latch. $WD_1(t)$ is the signal

used to extract ϕ_{Q1}. This signal is in phase with AA, and does not toggle close to the sampling instant. Therefore, the above mentioned issue does not exist in this scheme and the corresponding ϕ_{Q1} is extracted as shown in Fig. 2.22.

In Fig. 2.22, $WD_1(t)$ (and also toggling of AA) is the delayed version of the $W_1(t)$. For some of the rising edges of the $W_1(t)$ which are close to the sampling instant a small extra delay is intentionally added. This intentional added delay will make sure that quantizer decision and the QPD work consistently with each other. Using this technique ϕ_{Q1} is extracted and later canceled at the output of the proposed 1-1 MASH ADC. Any mismatch between the delay of the ϕ_{Q1} extraction path and the quantizer, as long as it is not too large to cause setup/hold times violations, will add the same error for all the codes and, therefore, will act as an offset. This offset will be removed after NCF_2 which contains a derivative function.

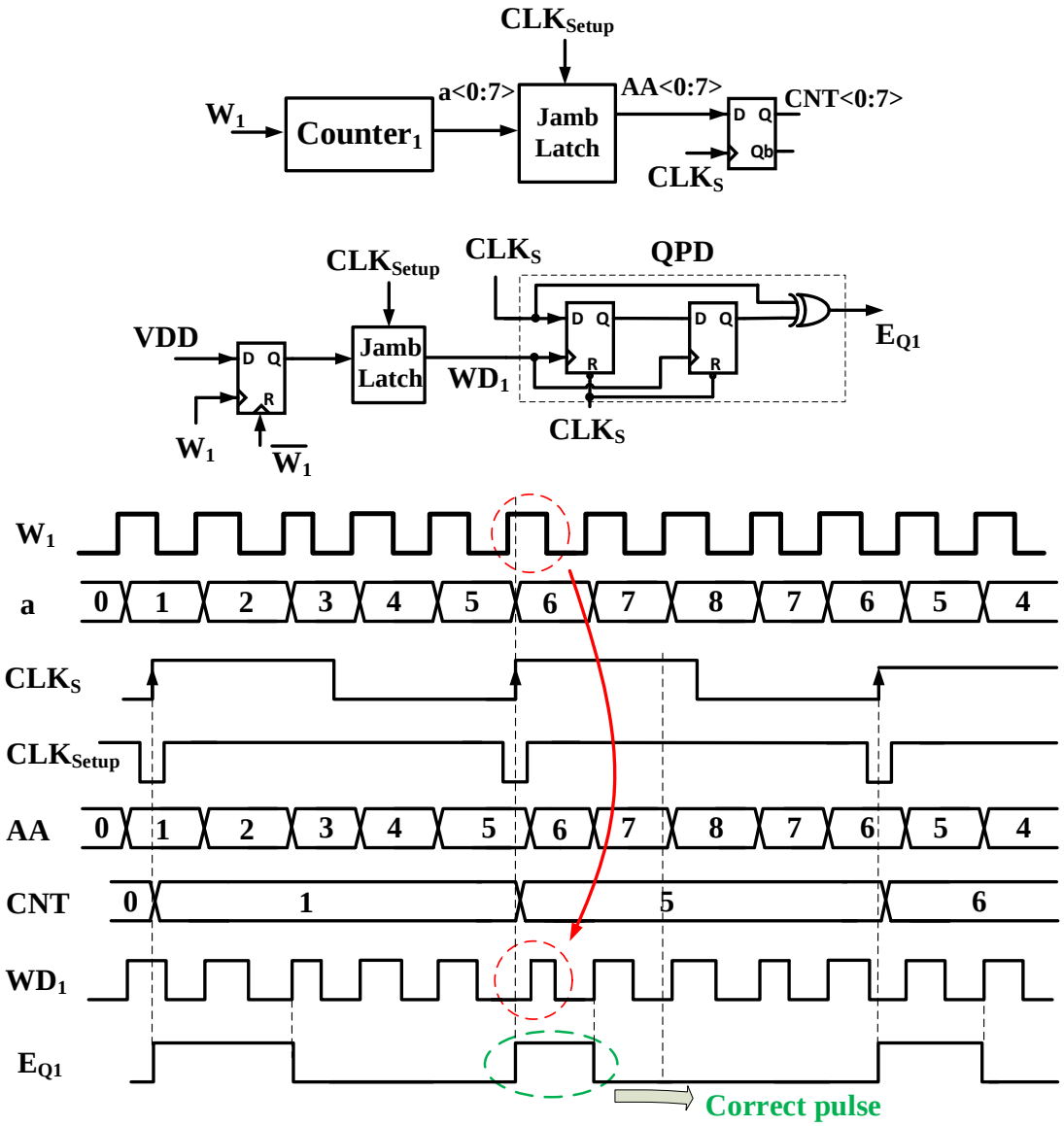


Figure 2.22: Proposed quantizer.

2.5.7 Effect of non-zero rise/fall times of QPD

Another timing non-ideality which has to be considered is the non-zero rise/fall times of the ϕ_{Q1} extraction path. As discussed in [20], this effect can be modeled as a low-pass filter in the ϕ_{Q1} extraction path. Fig. 2.23 shows the effect of non-zero rise/fall times of the QPD. In this figure, two $W_1(t)$ signals are considered in which one of them is t_0 time delayed compared with the other one. Also, f_{VCO1} is assumed to be fixed due to the first stage feedback.

As can be seen, even though there are slow rise/fall times in the $E_{Q1}(t)$ signal, the difference between the width of the two pulses is still t_0. From Fig. 2.23 it can be seen that both the pulses have exactly the same beginning. They both start with a small delay after the rising edge of CLK_S and they both experience the same rise time. The pulse width of one of them is t_0 longer assuming f_{VCO1} remains constant. Both the pulses experience the same fall time because they are using the same circuit. The only difference between the pulses would be the pulse width which is the same value as the Q-noise difference in both cases. Note that, due to the usage of the pulse extension technique, the limited rise/fall times wont affect the ϕ_{Q1} extraction if we design the one LSB size to be larger than the rise time to let the $E_{Q1}(t)$ settle to a high value before it has to go to a low value again. Using the pulse extension technique, all the samples experience the exact same added error due to the slow rise time. Also, since all the samples are using the same circuit in QPD, exactly the same error is added to the extracted pulses due to the slow fall time. Since these errors are the same for all the samples, they

act as an offset and, thus, they will be removed at the output of NCF_2 due to the derivative function.

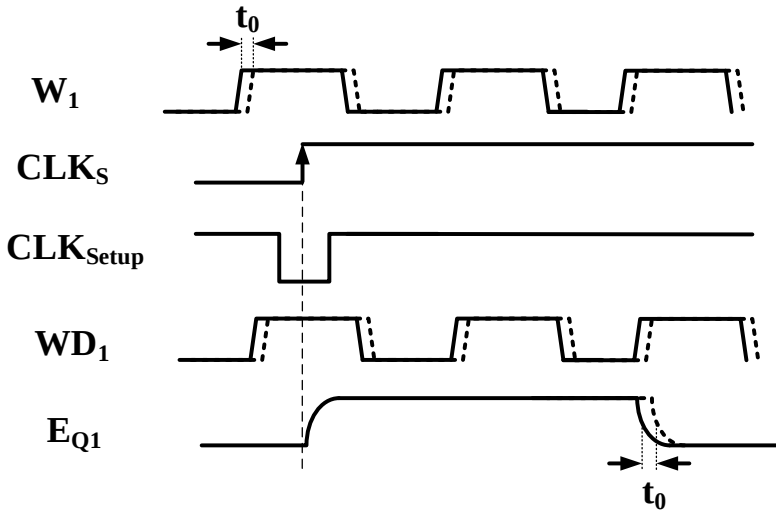


Figure 2.23: Effect of slow rise/fall times of QPD.

2.6 Design Example

The proposed ADC is implemented at the transistor level using a 65nm CMOS technology with a 1V supply. The target design specifications are shown in Table 2.4.

The simplified schematic of the proposed architecture is shown in Fig. 2.24. A single-ended structure is shown for simplicity, while the real implementation is pseudo-differential.

Table 2.4: Required specifications of the proposed PROPOSED 1-1 MASH

Spec	Value
BW	1 MHz
$SNDR$	$>$ 80 dB

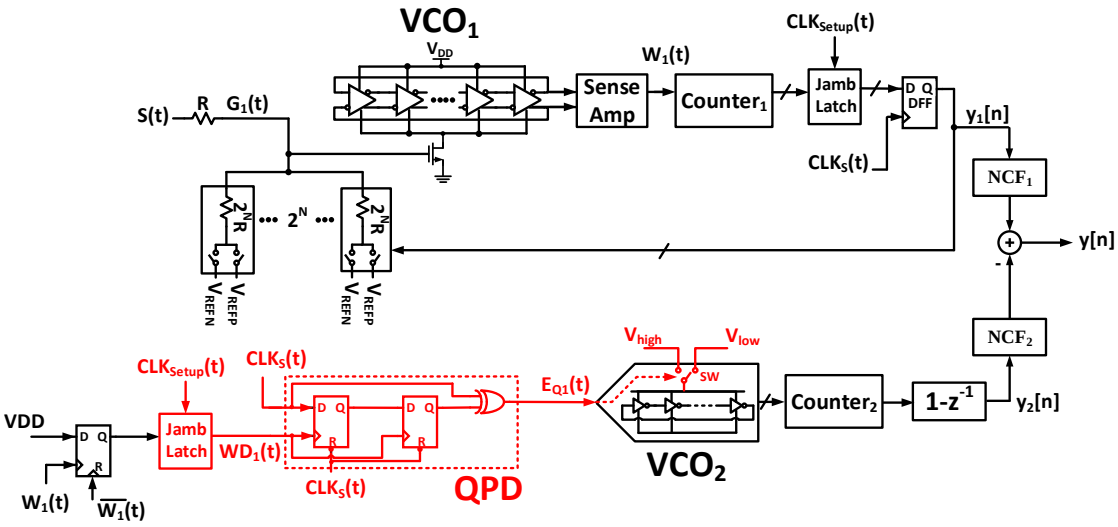


Figure 2.24: Simplified schematic of the proposed 1-1 MASH ADC.

The first stage DAC is implemented using a resistive DAC architecture. Since the input resistor is connected between the ADC input voltage and the VCO_1 input, which is operating as a virtual ground, the linearity of this resistor is critical. Thus, rnpoly resistive type is used for the input resistor. Unlike the input resistor, each of the DAC resistors are switched between two fixed voltages. Thus, the DAC resistors are inherently linear. In this design, smaller size resistors, rppolywo

resistive type, are used for the resistive DACs. The input resistor value is 5 $k\Omega$ and each DAC element size is 160 $k\Omega$.

10-stage VCOs are used in the first stage. Fig. 2.25 shows the schematic of the delay cells used in VCO_1. Each delay cell contains two cross-coupled inverter pairs and a voltage controlled tail current is shared between all the delay cells. The width of the inner pair is one fourth of the outer pair. The input common-mode voltage of VCO_1 is designed to be 500 mV. Since the overall performance of the proposed ADC is limited by the VCO_1 thermal noise, delay cells with large sizes have been used to lower VCO_1 phase noise.

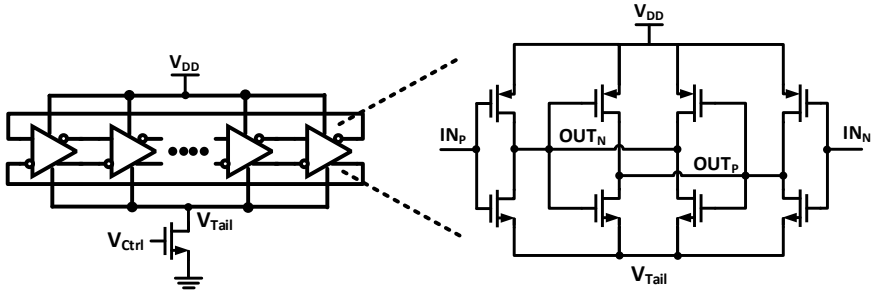


Figure 2.25: Delay cell used in the first stage VCO.

In this design, VCO_2 delay cells contain two cross-coupled inverter pairs without a tail current. The frequency of VCO_2 is controlled by changing its supply voltage. As can be seen in Fig. 2.24, in the real implementation, E_{Q1}(t) pulse is applied to a pair of switches which connect the VCO_2 supply either to V_{high} or V_{low}. Therefore, the VCO_2 frequency switches between values of f_{high} and f_{low}. V_{low} and V_{high} are designed to be 350 mV and 560 mV, respectively. Therefore, VCO_2 frequency switches between 42 MHz and 730 MHz.

The design parameters are shown in Table 2.5. As can be seen, f_{fr1} has been chosen to be around $4.5\times f_S$. Since, the pulse extension technique is used, the minimum and the maximum pulse width of $E_{Q1}(t)$ are $T_S/4.5$ and $2T_S/4.5$, respectively. Since, the sampling frequency is $56MHz$, the $E_{Q1}(t)$ pulse width varies between $4ns$ and $8ns$. This ensures that the digital circuitry operates at a speed comparable to the sampling clock.

Table 2.5: Design Parameters of the proposed 1-1 MASH

Spec	**value**	**Spec**	**Value**
$f_{fr1}(MHz)$	264	OSR	28
$K_{VCO1}(GHz/V)$	1.5	$V_{DD}(V)$	1
$f_{low}(MHz)$	42	$f_S(MHz)$	56
$f_{high}(MHz)$	730		

In order to show the low sensitivity of the proposed architecture to the timing error, in the following simulations the critical path has been post layout extracted while the rest of the circuits are at the transistor level. The critical path is highlighted in red in Fig. 2.24. Fig. 2.26 shows the transient response of the VCO_2 control voltage (supply). The rise time is about 135 ps. In order to show the immunity of the proposed architecture to the timing error, large delay cells (the same as VCO_1 without the tail current source) are used in VCO_2 and two T-gate switches control the VCO_2 supply voltage. This design is for a proof of concept,

as small size delay cells with low power consumption used in VCO_2 would make the design more power efficient.

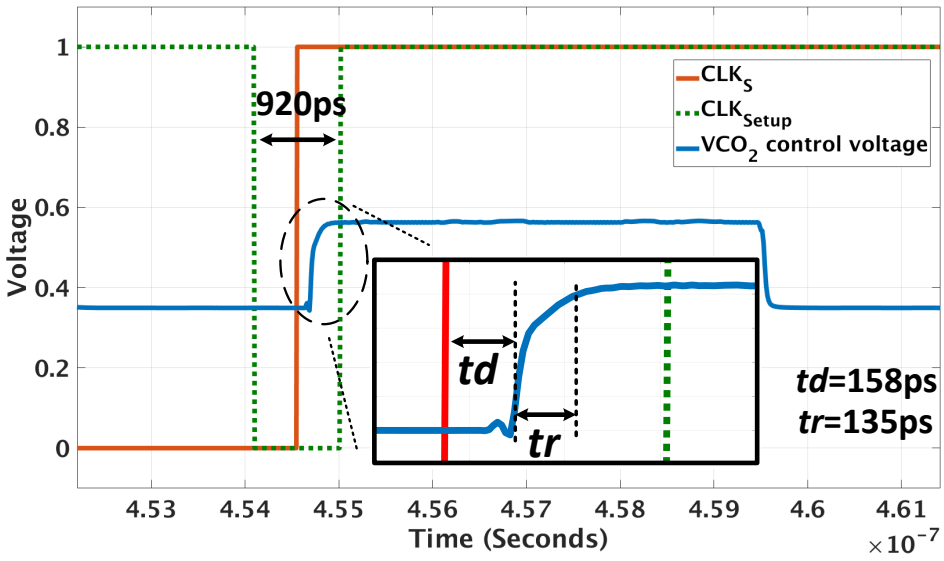
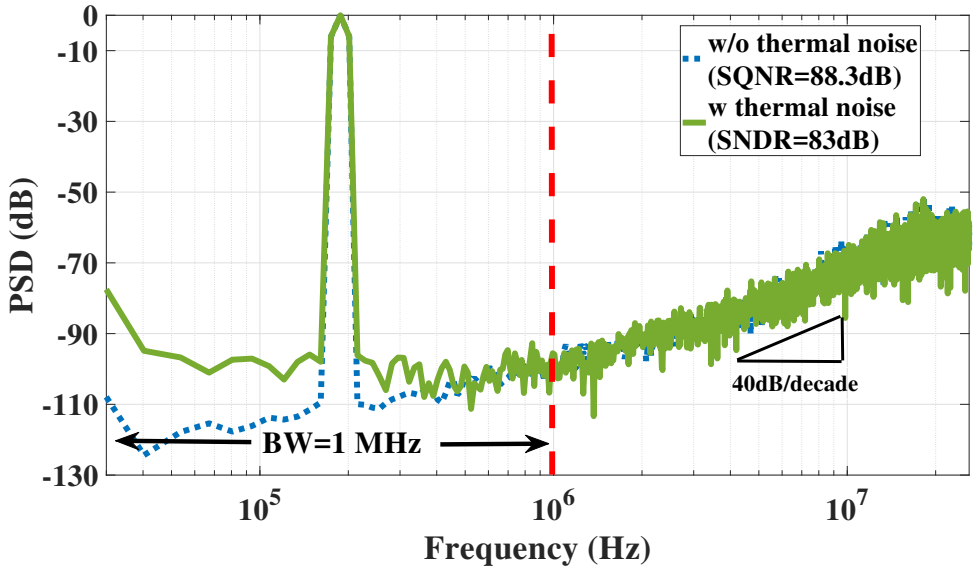
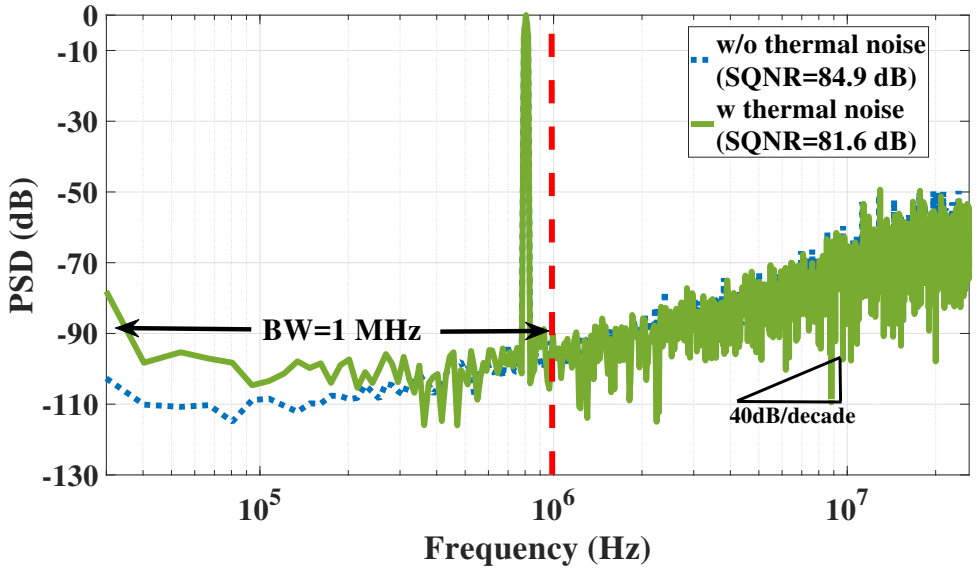


Figure 2.26: Transient response of the VCO_2 control voltage.

Fig. 2.27 shows the output spectrum of the proposed 1-1 MASH ADC for f_{in}=180 kHz and f_{in}=800 kHz, with and without thermal noise. In this simulation, the input signal to the ADC is a -1.3 $dBFS$ single tone sine wave. As discussed, a higher input frequency results in a higher f_{VCO1} variation. Therefore, the performance degrades as f_{in} gets closer to the BW. The 1-1 MASH output spectrum shows second-order noise shaping with $SQNR$ of 84.9 dB and $SNDR$ of 81.6 dB. The proposed ADC consumes 750 μW.



(a)



(b)

Figure 2.27: Spectrum of the proposed 1-1 MASH output. (a) f_{in}=180 kHz, (b) f_{in}=800 kHz.

Table 2.6: Performance Comparison

	[4]	[14]	[21]	[22]	**This work**
Process (nm)	180	130	90	40	65
Power (mW)	2.9	1.06	16	1.91	0.75
f_S (MHz)	50	300	600	65	56
BW (MHz)	1.04	2	10	1.92	1
$SNDR$ (dB)	78.2	65.8	78.3	79.6	81.6
FOM_S (dB)1	163.8	159	163	169.6	172
FOM_W ($fJ/step$)2	209.5	170	120	64	38

$$FOM_S = SNDR + 10 \times log_{10}(\text{BW/Power})$$

$$FOM_W = \text{Power}/((2\times\text{BW})\times 2^{ENOB})$$

Table 2.6 shows a comparison of the proposed ADC with other works with similar performance. Note that the reported performance of the proposed ADC is based on the post layout extraction and the transistor-level simulations. In this design, the front end blocks which are the input resistors, DAC and the VCO_1s are the main contributors of the thermal noise. The SNR due to the input resistors and DAC noise is 87 dB. Simulations show that the VCO_1s are the dominant source of the thermal noise and they limit the SNR to around 84 dB. Thermal noise due to the second stage will be shaped by one order and therefore has a minor effect on the overall SNR.

2.7 Conclusion

A new, inherently linear, VCO-based 1-1 MASH ADC is proposed. Simulation results verify the performance of this architecture. Using a 1-1 MASH structure, second-order noise shaping is achieved without the need for an OTA. Since the first stage is in a closed loop and the input of the second stage is a two level pulse signal, the overall ADC is inherently linear. Therefore, there is no need for power hungry linearization methods while using VCO quantizers.

Bibliography

[1] S. Pavan, R. Schreier, and G. C. Temes, *Understanding Delta-Sigma Data Converters*. John Wiley & Sons, 2017.

[2] J. A. Fredenburg and M. P. Flynn, "A 90-MS/s 11-MHz-bandwidth 62-dB SNDR noise-shaping SAR ADC," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 2898–2904, 2012.

[3] P. Payandehnia *et al.*, "Fully passive third-order noise shaping SAR ADC," *Electronics Letters*, vol. 53, no. 8, pp. 528–530, 2017.

[4] N. Maghari and U.-K. Moon, "A third-order DT $\Delta\Sigma$ modulator using noise-shaped bi-directional single-slope quantizer," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 12, pp. 2882–2891, 2011.

[5] M. José *et al.*, "Next-generation delta-sigma converters: trends and perspectives," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 5, no. 4, pp. 484–499, 2015.

[6] M. Z. Straayer and M. H. Perrott, "A 12-bit, 10-MHz bandwidth, continuous-time $\Sigma\Delta$ ADC with a 5-bit, 950-MS/s VCO-based quantizer," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 4, pp. 805–814, 2008.

[7] P. Zhu, X. Xing, and G. Gielen, "A 40 MHz-BW 35 fJ/step-FoM nonlinearity-cancelling two-step ADC with dual-input VCO-based quantizer," in *Proc. IEEE European Solid State Circuits Conference (ESSCIRC)*, 2014, pp. 63–66.

[8] S. Dey *et al.*, "A 50 MHz BW 76.1 dB DR Two-Stage Continuous-Time DeltaSigma Modulator With VCO Quantizer Nonlinearity Cancellation," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 3, pp. 799–813, March 2018.

[9] Y. Xu, S. Leuenberger, and U.-K. Moon, "Highly linear continuous-time MASH $\Delta\Sigma$ ADC with dual VCO-based quantizers," in *Proc. IEEE International Symposium on Circuits and Systems*. IEEE, 2015, pp. 2033–2036.

[10] L. Hernandez, "VCO based multi-stage noise shaping ADC," *Electronics Letters*, vol. 48, no. 4, pp. 206–208, 2012.

[11] W. Yu, K. Kim, and S. Cho, "A 148 fs_{rms} Integrated Noise 4 MHz Bandwidth Second-Order $\Delta\Sigma$ Time-to-Digital Converter With Gated Switched-Ring Oscillator," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 8, pp. 2281–2289, 2014.

[12] S. B. Rao, "Linearizing techniques for voltage controlled oscillator based analog to digital converters," Ph.D. dissertation, 2013.

[13] P. Gao *et al.*, "Design of an intrinsically-linear double-vco-based adc with $2^n d$-order noise shaping," in *2012 Design, Automation Test in Europe Conference Exhibition (DATE)*, March 2012, pp. 1215–1220.

[14] K. Lee, Y. Yoon, and N. Sun, "A Scaling-Friendly Low-Power Small-Area$\delta\sigma$ ADC with VCO-Based Integrator and Intrinsic Mismatch Shaping Capability," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 5, no. 4, pp. 561–573, Dec 2015.

[15] M. Park and M. H. Perrott, "A 78 dB SNDR 87 mW 20 MHz bandwidth continuous-time $\Delta\Sigma$ ADC with VCO-based integrator and quantizer implemented in 0.13 μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3344–3358, 2009.

[16] K. Reddy *et al.*, "A 54mW 1.2 GS/s 71.5 dB SNDR 50MHz BW VCO-based CT $\Delta\Sigma$ ADC using dual phase/frequency feedback in 65nm CMOS," in *Proc. IEEE Symp. VLSI Circuits Dig. Tech. Papers*, 2015, pp. C256–C257.

[17] A. Babaie-Fishani and P. Rombouts, "A Mostly Digital VCO-Based CT-SDM With Third-Order Noise Shaping," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 8, pp. 2141–2153, Aug 2017.

[18] H. Maghami *et al.*, "A highly linear OTA-free VCO-based 1-1 MASH $\Delta\Sigma$ ADC," in *Proc. IEEE International Symposium on Circuits and Systems*, 2017.

[19] P. Prabha *et al.*, "A highly digital VCO-based ADC architecture for current sensing applications," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 8, pp. 1785–1795, 2015.

[20] E. Gutierrez *et al.*, "A Pulse Frequency Modulation Interpretation of VCOs Enabling VCO-ADC Architectures With Extended Noise Shaping," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 2, pp. 444–457, Feb 2018.

[21] K. Reddy *et al.*, "A 16mW 78dB-SNDR 10MHz-BW CT-$\Delta\Sigma$ ADC using residue-cancelling VCO-based quantizer," in *2012 IEEE International Solid-State Circuits Conference*, Feb 2012, pp. 152–154.

[22] H. Tsai *et al.*, "A 1.2V 64fJ/conversion-step continuous-time $\Sigma\Delta$ modulator using asynchronous SAR quantizer and digital $\Sigma\Delta$ truncator," in *2012 IEEE Asian Solid State Circuits Conference (A-SSCC)*, Nov 2012, pp. 241–244.

Chapter 3: A 0.9V 79.7dB SNDR 2MHz-BW 1-1 MASH OTA-less VCO-based $\Delta\Sigma$ ADC with a Novel Phase Quantization Noise Extraction Technique

In this chapter a novel technique is introduced to extract the quantization noise of a multi-phase VCO-based quantizer (VCOQ) in the time domain as a PWM signal. Using this technique, a new highly linear VCO-based 1-1 MASH delta-sigma ADC structure is presented. This architecture does not require any OTA-based analog integrators or power hungry linearization methods. The first stage is a closed loop multi-phase VCO-based voltage-to-phase (V-to-P) converter and the second stage is an open loop multi-phase VCO-based voltage-to-frequency (V-to-F) converter. Using the proposed technique the phase quantization error of the first stage is extracted as a pulse signal and then fed to the second stage. The input of the first VCO is a very small amplitude signal and the input of the second VCO is a two-level PWM signal. Therefore, the VCO non-linearity does not limit the overall ADC performance, mitigating the need for power hungry linearization methods. The prototype achieves second order noise shaping with a DR/SFDR/SNR/SNDR of 82.7/88.7/80.3/79.7 dB for an input signal BW of 2 MHz. The fabricated design consumes 1.248 mW from a 0.9 V supply.

3.1 Introduction

As new technologies are developing in different fields of industry such as biomedical applications, additive manufacturing and microelectronics, the energy optimization is becoming more vital. Also due to an expansive growth in Internet-of-Things (IoT), more physical devices and everyday objects in consumer or industrial applications are getting connected. These devices can communicate and interact with others using sensors through internet, and they can be remotely monitored and controlled [1–7]. Therefore, there is an ever-increasing demand for high performance sensors with low power consumption. ADCs are important part of sensors. As a result low power high resolution ADCs are needed for these systems. Nyquist rate ADCs such as pipeline [8–11] or successive approximation register (SAR) [12, 13] require anti-aliasing filters [14–16] with high selectivity. These filters often add significant power and design overhead. Unlike Nyquist rate ADCs, oversampling ADCs, such as noise shaping SAR [17–19], integrating quantizer [20] and delta-sigma ADCs [21–23] relax the selectivity requirement of anti-aliasing filters significantly. Among different types of oversampling ADCs, delta-sigma ADCs are most commonly used.

Conventional $\Delta\Sigma$ ADCs utilize OTAs in their loop filter implementation followed by multi-bit voltage domain quantizers. With process scaling the intrinsic gain of the transistors as well as the voltage headroom decreases. This makes OTA design increasingly difficult in advanced CMOS processes [24]. Also, since the voltage headroom reduces, multi-bit voltage domain quantizers become more

difficult to design due to their noise and offset requirements.

Recently, there has been a focus on alternative digital solutions that replace traditional analog blocks. Time domain quantization methods, such as those using VCO-based quantizers are an attractive alternative. VCOs are implemented using simple inverters. Due to their highly digital nature, they benefit from technology scaling. As the transistor dimension reduces, the inverter delay decreases which results in a higher timing resolution of the VCO-based ADCs. Moreover, VCO-based ADCs feature inherent quantization noise shaping and guaranteed monotonicity. Despite these advantages, the VCO nonlinearity often limits the performance of these ADCs. Several techniques have been introduced to increase the order of noise shaping and mitigate the VCO nonlinearity.

In [25] a VCO-based quantizer (VCOQ) is placed in a closed loop and is used as a voltage-to-frequency (V-to-F) converter. The high in band gain of the filter preceeding the VCO-based quantizer, reduces the VCO nonlinearity. However, to provide more than first order noise shaping, this architecture requires OTAs. In [26] a residue cancellation architecture is used to reduce the effect of the VCO nonlinearity. A coarse flash ADC is used before the VCO to reduce the voltage swing at the input of the VCO. Since, the input voltage swing of the VCO is small, this method suppresses the VCO nonlinearity. To achieve more than first order noise shaping, this architecture also requires OTAs. To cancel the VCO nonlinearty, a two stage architecture were used in [23, 27]. In the loop filter of these architectures, OTAs were employed. In [28, 29] the input of the VCOs is a pulse width modulated (PWM) signal. Since, the VCOs operate at only two

frequencies, they are inherently linear. However, power hungry PWM generators are needed at the input to avoid a performance degradation. In [30–32], the VCO-based ADC is used as a voltage-to-phase (V-to-P) converter. Since the VCO acts as an integrator followed by a quantizer, its input signal swing reduces and, therefore, the VCO nonlinearity is mitigated. This architecture also uses OTAs to implement higher order noise shaping. A third order OTA-less modulator is introduced in [33]. Although linearity-enhanced VCOs are used, the linearity of the modulator is still limited to 10.5 bits.

In this chapter and [34], the highly linear OTA-less 1-1 MASH VCO-based ADC intreduced in the previous chapter is implemented using multi-phase VCOQs. The first stage is a closed loop VCO-based ADC where a multi-phase VCOQ is used as a V-to-P converter. A novel technique is introduced to extract the quantization noise of a multi-phase VCOQ in the time domain as a PWM signal. The PWM signal is then applied to the second stage which is an open loop multi-phase VCOQ used as a V-to-F converter. Since, the first stage is a closed loop V-to-P converter and the input of the second stage is a PWM signal, the VCO nonlinearity is mitigated in this architecture. The prototype achieves second order noise shaping with high linearity without using OTAs.

The rest of the chapter is organized as follows. The architecture of the 1-1 MASH VCO-based ADC is presented in Section 3.2. In Section 3.3, the novel quantization noise extraction of a multi-bit VCOQ is described. The implementation details and the effect of nonidealities are discussed in Section 3.4. Section 3.5 provides the measurement results and finally Section 3.6 concludes the chapter.

3.2 Architectural level analysis of OTA-less 1-1 MASH VCO-based ADC

Recently there has been a significant interest in VCO-based ADCs due to their inherent first-order noise shaping and simple digital friendly implementation. Despite these benefits often the VCO nonlinearity is the main concern in implementing VCO-based ADCs. In this section, first the basic concept of first order V-to-F and V-to-P converters are described. Then, the system level concept of the proposed architecture is provided. This architecture achieves second order noise shaping and mitigates the VCO nonlinearity without using power hungry linearization methods.

3.2.1 Open loop first order VCO-based V-to-F converter

A conceptual realization of an open loop first order VCO-based V-to-F converter is shown in Fig. 3.1 (a). The VCO consists of back-to-back connected delay cells. Compared to single-phase VCQs which only use the information of one VCO output tap, multi-phase VCOQs use multiple VCO output taps. In Fig. 3.1 the frequency of the VCO is controlled by $V_i(t)$ and the VCO output phase is defined as:

$$\phi(t) = \int_0^t (2\pi K_{VCO} V_i(t) + 2\pi f_{fr}) dt \tag{3.1}$$

where K_{VCO} and f_{fr} are the voltage-to-frequency gain and the free-running frequency of the VCO, respectively. Assuming N delay cells are used for the VCO

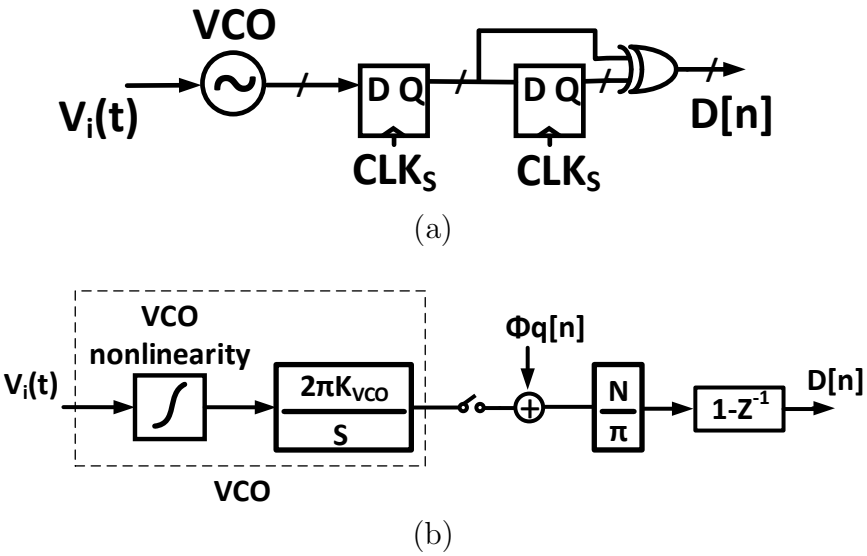


Figure 3.1: Open loop first order VCO-based V-to-F converter. (a) Conceptual realization. (b) Block diagram.

implementation, each π/N phase change of the VCO translates to one delay element output change. As can be seen in Fig. 3.1 (a) a set of registers is used to sample the VCO output taps. The current sampled values are then differentiated with the previous sampled values using a set of XOR gates. The XOR output represents the VCO output phase change between two sampling instances. Fig. 3.1 (b) shows the block diagram of the first-order V-to-F converter. Since the phase digitization occurs at the sampling of the VCO output taps, the quantization error (ϕ_q) which is in the phase domain is added after the VCO and before the differentiator ($1 - z^{-1}$). The output of VCOQ is:

$$D[n] = \int_{(n-1)T_S}^{nT_S} 2N\left(K_{VCO}V_i(t) + f_{fr}\right)dt + \frac{N}{\pi}[\phi_q(nT_S) - \phi_q((n-1)T_S)] \tag{3.2}$$

where T_S is the sampling clock period.

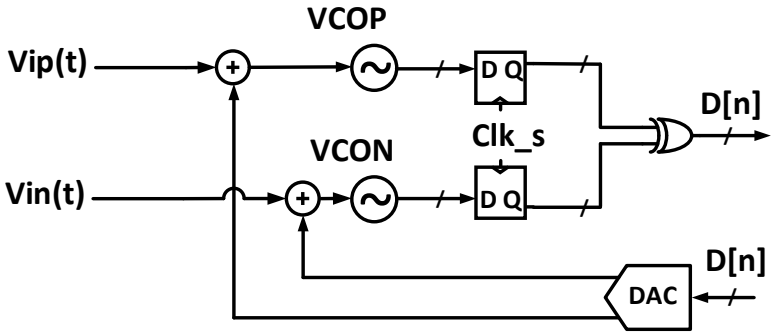
Assuming the input signal remains constant between two consecutive samples, using z-transforms the output is:

$$D(z) = \left(2NK_{VCO}T_S z^{-1}\right)V_i(z) + 2Nf_{fr}T_S + \frac{N}{\pi}\left(1 - z^{-1}\right)\phi_q(z) \tag{3.3}$$

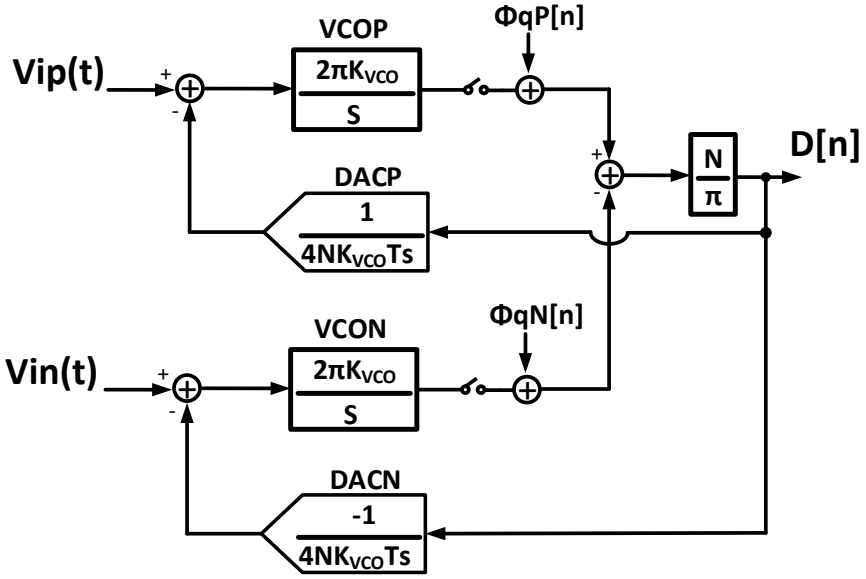
In this equation ϕ_q is the phase quantization noise and has a value between $[0, \frac{\pi}{N})$. This architecture provides first-order noise shaping but since the VCO nonlinearity is directly applied to the input signal, the performance of the ADC can be significantly degraded due to the nonlinear characteristic of the VCO.

3.2.2 Closed loop first-order VCO-based V-to-P converter

In conventional implementations of V-to-P converters [30, 31], the intrinsic DEM capability of a VCOQ is lost. Thererfore, an additional DEM block is required to address the DAC mismatch issue. In [32] a novel implementation of a closed loop $\Delta\Sigma$ ADC using a VCO-based integrator is introduced which provides an intrinsic DEM scheme of clocked averaging (CLA). This architecture is shown in Fig. 3.2



(a)



(b)

Figure 3.2: Closed loop first order VCO-based V-to-P converter. (a) Conceptual realization. (b) Block diagram.

(a). In this architecture two VCOs are used in a pseudo-differential manner. The output phase is measured by comparing the output phase of the two VCOs to each other. As shown in [32], in this architecture the free running frequency of the VCOs can be chosen freely and also this architecture does not need an explicit DEM block. Fig. 3.2 (b) shows the block diagram of the closed loop first order V-to-P converter. Since, the phase of each VCO is sampled before being compared using the XOR gates, two independent noise sources, $\phi_{qP,N}$ exist in the system. Fig. 3.2 (b) shows a first order CT $\Delta\Sigma$ and its output is:

$$\begin{aligned} D(z) = &\left(2NK_{VCO}T_S z^{-1}\right) V_{id}(z) \\ &+ \left(\frac{N}{\pi}\right)\left(1 - z^{-1}\right)\left(\phi_{qP}(z) - \phi_{qN}(z)\right) \end{aligned} \tag{3.4}$$

where V_{id} is the differential input signal.

3.2.3 Proposed multi-phase VCO-based 1-1 MASH ADC

Fig. 3.3 shows the conceptual block diagram of the proposed multi-phase VCO-based 1-1 MASH ADC. In this architecture, the first stage is a closed loop first order V-to-P converter and the second stage is an open loop V-to-F converter. The quantization noise of the first stage which is in the phase domain is extracted in the time domain as a PWM signal ($E_Q(t)$) using a quantization phase detector (QPD) block. The detailed implementation of the QPD is explained in Section 3.3. In this architecture since, VCO_1 is used as an integrator its input voltage variation

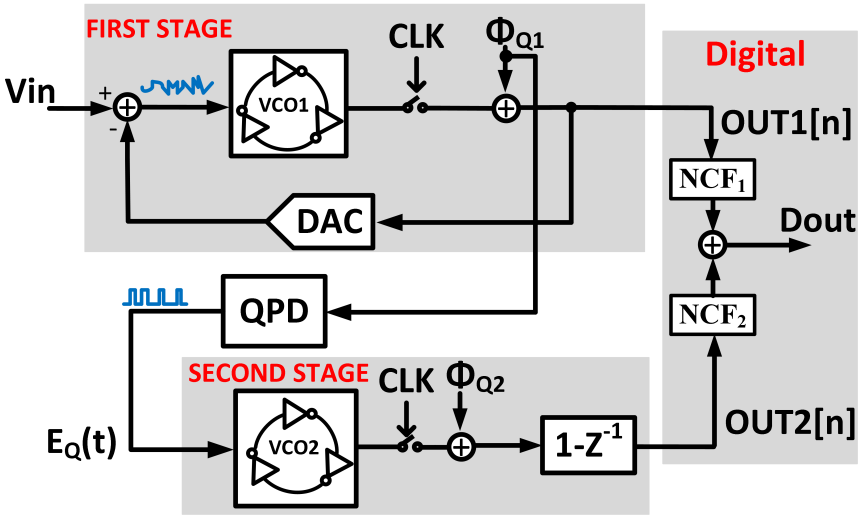


Figure 3.3: Block diagram of the proposed 1-1 MASH ADC.

is small and therefore the VCO_1 nonlinearity is suppressed. Also, since the input signal of VCO_2 is a two level PWM signal, VCO_2 operates at only two frequencies which makes the second stage VCO inherently linear.

Fig. 3.4 shows the VCO_2 frequency ($f_{VCO2}(t)$) change when the PWM signal of $E_Q(t)$ is applied to its input. $f_{VCO2}(t)$ switches between f_{High} and f_{Low} when $E_Q(t)$ changes from V_{Low} to V_{High}. Similar to (3.2), the output is:

$$D_2[n] = \int_{(n-1)T_S}^{nT_S} 2N f_{VCO2} dt + \frac{N}{\pi}[\phi_{q2}(nT_S) - \phi_{q2}((n-1)T_S)] \tag{3.5}$$

Assuming $E_Q(t)$ is always equal to V_{Low} at the sampling instances:

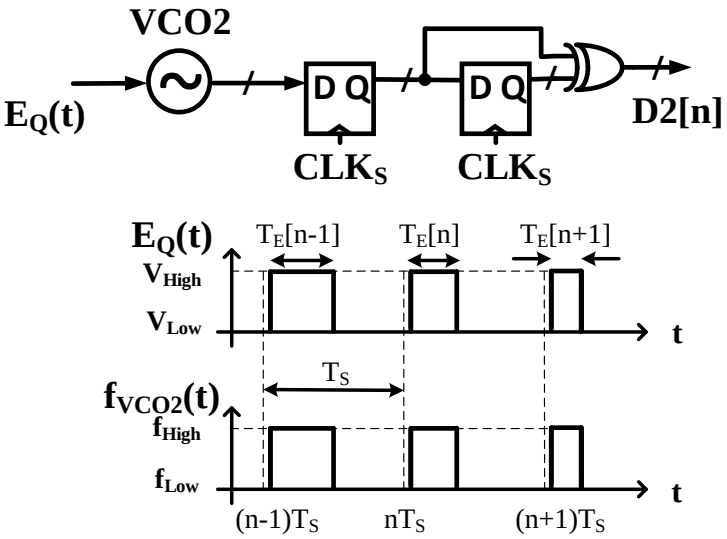


Figure 3.4: $f_{VCO2}(t)$ behavior when a PWM signal is applied to its input.

$$\begin{aligned} D_2[n] =& 2N\left(T_E[n] f_{High} + \left(T_S - T_E[n]\right) f_{Low}\right) \\ &+ \frac{N}{\pi}\left[\phi_{q2}\left(nT_S\right) - \phi_{q2}\left(\left(n-1\right)T_S\right)\right] \end{aligned} \tag{3.6}$$

where T_E is the pulse width of $E_Q(t)$.

Using z-transforms the output is:

$$\begin{aligned} D_2(z) =& 2N\left(f_{High} - f_{Low}\right) T_E(z) + 2NT_S f_{Low} \\ &+ \frac{N}{\pi}\left(1 - z^{-1}\right)\phi_{q2}(z) \end{aligned} \tag{3.7}$$

As can be seen, the time domain information (T_E) goes to the output with a

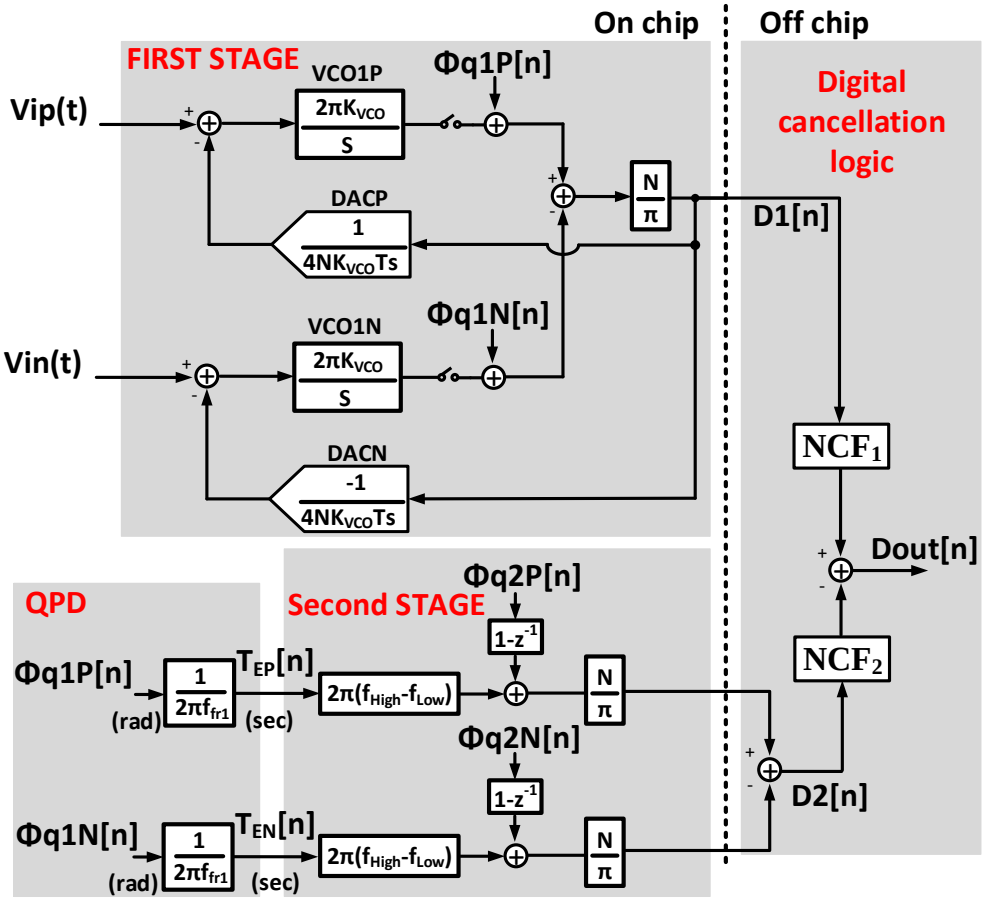


Figure 3.5: Linear model of the proposed 1-1 MASH ADC.

linear gain of $2N(f_{High} - f_{Low})$ and the quantization noise is first order shaped. In (3.7), $2NT_S f_{Low}$ is a constant value and can be removed in a pseudo differential architecture.

Fig. 3.5 shows the linear model block diagram of the 1-1 MASH ADC. As shown in Section 3.3 the QPD block converts the quantization error from the phase domain to the time domain with a gain of $1/(2\pi f_{fr1})$. Based on the linear model

of Fig. 3.5, the first stage output ($D_1[n]$) and the second stage output ($D_2[n]$) are:

$$\begin{cases} D_1(z) = \left(2NK_{VCO1}T_S z^{-1}\right) V_{id}(z) \\ \qquad\qquad + \dfrac{N}{\pi}\left(1-z^{-1}\right)\left(\phi_{q1P}(z) - \phi_{q1P}(z)\right) \\ D_2(z) = \dfrac{N}{\pi}\dfrac{(f_{High} - f_{Low})}{f_{fr1}} z^{-1}\left(\phi_{q1P}(z) - \phi_{q1P}(z)\right) \\ \qquad\qquad + \dfrac{N}{\pi}\left(1-z^{-1}\right)\left(\phi_{q2P}(z) - \phi_{q2N}(z)\right) \end{cases} \tag{3.8}$$

In order to cancel ϕ_{q1} and second order noise shape ϕ_{q2}, the following noise cancellation filters (NCFs) are required:

$$\begin{aligned} NCF_1(z) &= z^{-1} \\ NCF_2(z) &= \frac{f_{fr1}}{(f_{High} - f_{Low})}\left(1-z^{-1}\right) \end{aligned} \tag{3.9}$$

Therefore, the final output can be derived as:

$$\begin{aligned} &D_{OUT}(z) = \left(2NK_{VCO1}T_S z^{-2}\right) V_{id}(z) \\ &+ \frac{N}{\pi}\left(\frac{f_{fr1}}{f_{High} - f_{Low}}\right)\left(1-z^{-1}\right)^2\left(\phi_{q2P}(z) - \phi_{q2N}(z)\right) \end{aligned} \tag{3.10}$$

As seen in (3.10), the second stage quantization noise is second order shaped.

3.3 Proposed Quantization Noise Extraction Technique

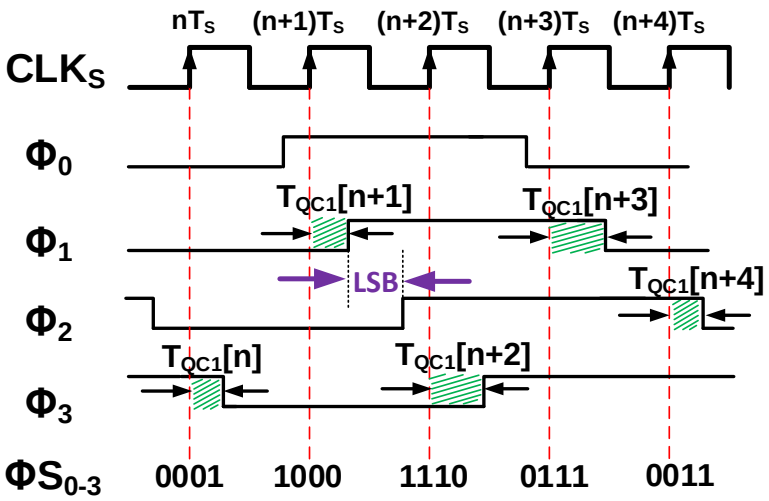
When VCOQ is operating as a V-to-P converter the quantization noise, which is in the phase domain (ϕ_q), is not explicitly available. In this section a novel method to extract ϕ_q in the time domain is presented.

Fig. 3.6 shows the output phases (ϕ_i) of one of the multi-phase VCOQs used in the first stage. In this figure $\phi_{S,i}$ is the sampled VCO output code. Fig. 3.6(a) and Fig. 3.6(b) show the timing and phase diagrams of ϕ_{q1}, respectively. For the sake of simplicity a 2-bit VCOQ is illustrated while the actual implementation utilizes a 5-bit VCOQ. ϕ_{qC1} is defined as $LSB - \phi_{q1}$ which is easier to extract in the time domain compared to ϕ_{q1}. ϕ_{qC1} is the amount of VCO phase change from the rising edge of CLK_S to the transition edge of one of the VCO output phase taps which toggles first after the rising edge of CLK_S in each sampling period. This time period is shown as T_{qC1} in Fig 3.6(a). ϕ_{qC1} (the shifted version of ϕ_{q1}) can be extracted in the time domain as described next.

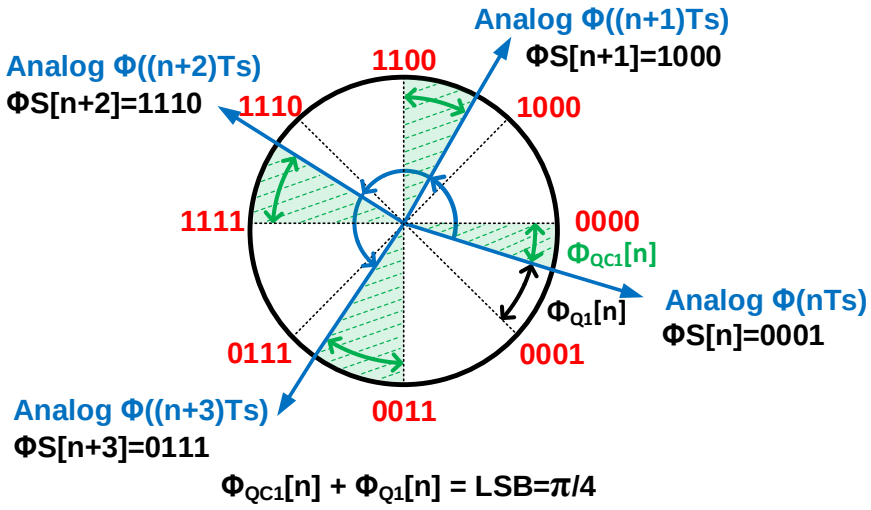
ϕ_{qC1} is defined as:

$$\phi_{qC1}[n-1] = \int_{T_{QC1}[n]} 2\pi f_{VCO1} dt \tag{3.11}$$

As (3.11) shows, ϕ_{qC1} is the integration of the VCO frequency over the time period of $T_{QC1}[n]$. Since VCO_1 is in a closed loop, the input signal variation of VCO_1 is small. Therefore, the VCO_1 frequency variation is also small, resulting in a linear relationship between ϕ_{qC1} and $T_{QC1}[n]$ as shown in (3.12).



(a)



(b)

Figure 3.6: VCO_1 output and phase quantization noise. (a) Timing diagram. (b) Phase diagram. [29].

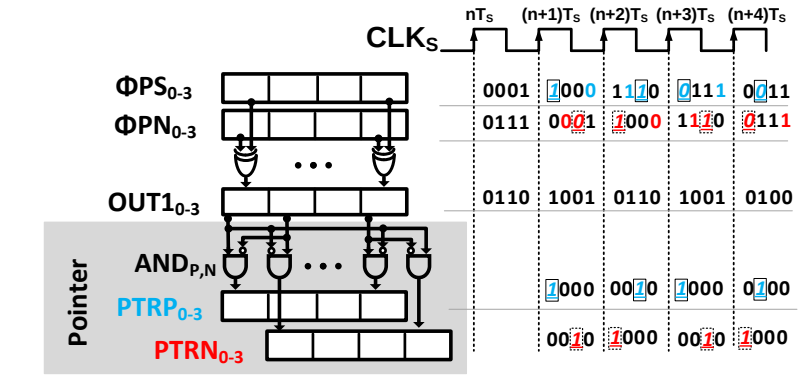
$$\phi_{qC1}[n-1] \approx 2\pi f_{fr1} T_{QC1}[n] \tag{3.12}$$

Since, there is a linear relation between ϕ_{qC1} and T_{QC1}, the quantization noise can be represented in the time domain. The accuracy of (3.12) depends on the variation of f_{VCO1}. The shaded areas in Fig. 3.6(a) show the representation of ϕ_{qC1} in the time domain (T_{QC1}). The LSB difference between ϕ_{q1} and ϕ_{qC1} does not affect the performance of the ADC since it is cancelled in the digital filter NCF_2.

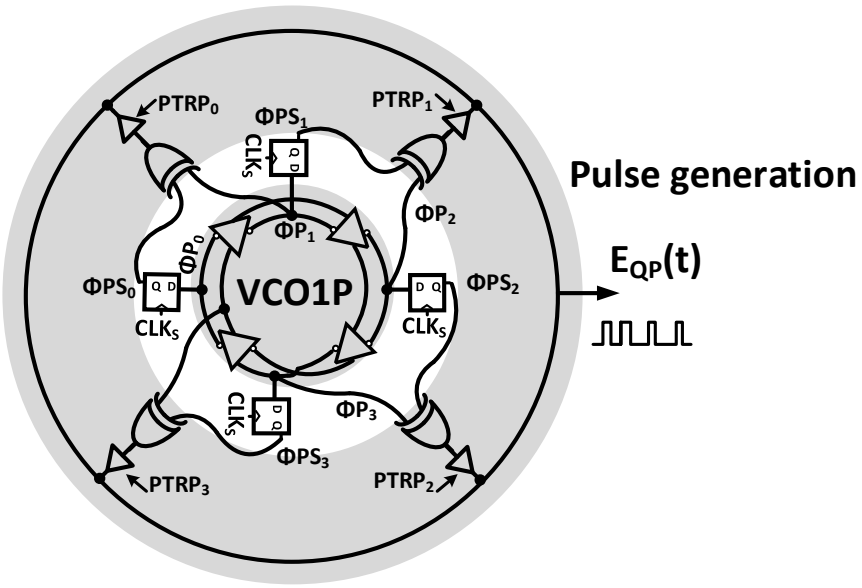
As shown in Fig. 3.6(a) only one of the VCO output taps carries a valid ϕ_{qC1} signal during each sampling period. Therefore, to extract ϕ_{qC1} in the time domain, requires first detecting the proper output phase tap carrying ϕ_{qC1}. Next, the PWM pulse corresponding to ϕ_{qC1} has to be generated.

To select the proper output phase tap of $\text{VCO}_{1P,N}$, two pointers ($\text{PTR}_{P,N}$) are used. The operation of the pointers is demonstrated in Fig. 3.7 (a). The pointers are implemented using two sets of AND gates ($\text{AND}_{P,0-3}$, $\text{AND}_{N,0-3}$). The inputs of the AND gates are connected to the first stage outputs. During each sampling period the output of a single AND gate in each set toggles high (indicating the phase tap that has the last transition in the previous sampling period).

After detecting the phase tap that has the last transition in the previous sampling period, the PWM pulse which represents ϕ_{qC1} in the time domain can be simply generated by using two sets of XOR gates followed by tri-state buffers. Fig. 3.7 (a) shows the PWM generation for VCO_{1P}. As shown in Fig. 3.7 (a), each sampled VCO phase tap is XORd with the next phase tap. These XOR



(a)



(b)

Figure 3.7: Phase quantization noise extraction in the time domain as a PWM signal. (a) Detecting the proper output phase tap carrying ϕ_{QC1}. (b) PWM pulse generation corresponding to ϕ_{QC1}.

gates generate different pulses at the output. Next, the pointer signal selects the one that carries ϕ_{qC1} through a tri-state buffer. In this way, the desired PWM pulse is generated. Both the pointers and the PWM generator blocks have been implemented using simple combinational logic with a similar design implemented for VCO_{1N}.

3.4 Circuit Details

The simplified schematic of the proposed 1-1 MASH $\Delta\Sigma$ modulator is shown in Fig. 3.8. The first stage is a first order CT $\Delta\Sigma$ modulator. It consists of two VCOs followed by a phase encoder. The digitized first stage output is fed back to the input of $\mathrm{VCO}_{1P,N}$ through a resistive DAC. The quantization noise of the first stage is extracted in the time domain by the QPD block which is implemented using combinational logic. The second stage consists of two open loop VCOs followed by frequency encoders. Next, the key building blocks of the modulator are described.

3.4.1 VCOs

32-stage (5-bit) VCOs are used in both the stages. Fig. 3.9 shows the delay cells used in the first stage VCOs. Each delay cell consists of four cross-coupled inverter pairs and a voltage controlled tail current sources. The width of the outer pair is designed to be four times more than the inner pair. The frequency of $\mathrm{VCO}_{1P,N}$ is adjusted by controlling the tail current. Since VCO_1 thermal noise is directly

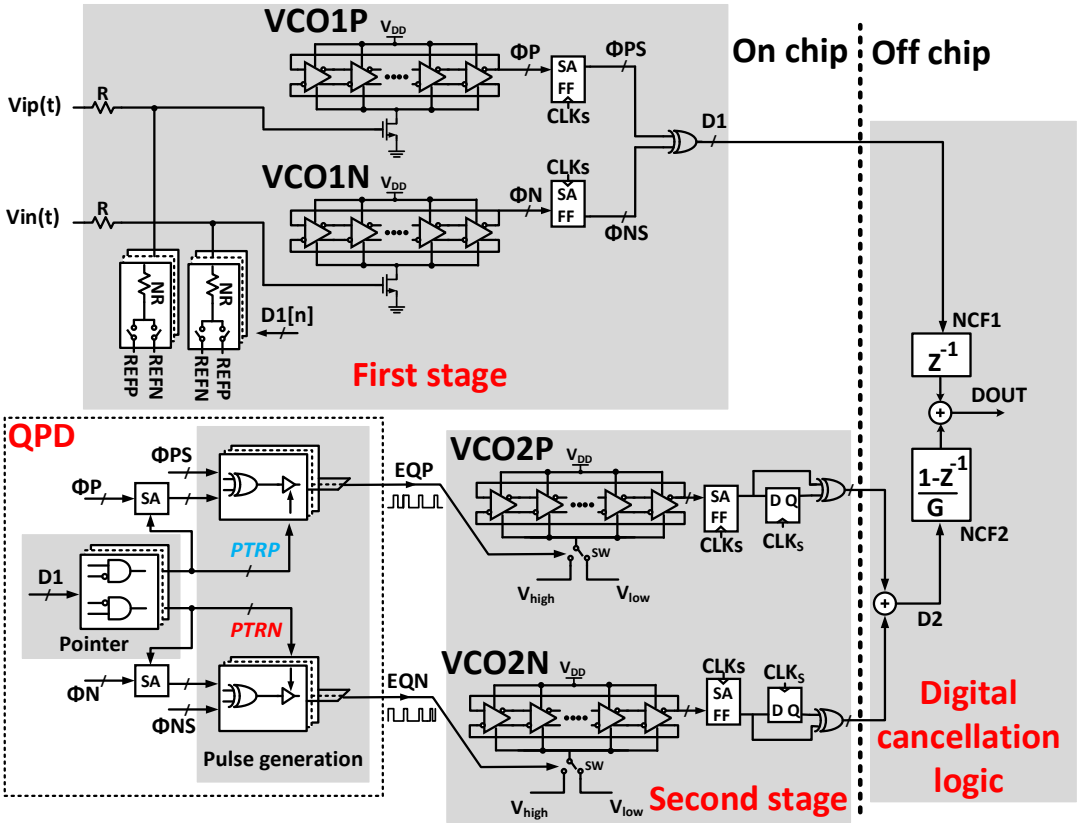


Figure 3.8: Simplified schematic of the proposed 1-1 MASH ADC.

added at the input, large size delay cells have been used to lower the phase noise of VCO_1.

In this design, the VCO_2 delay cells have been implemented by two cross-coupled inverter pairs. Here, also the width of the inner pair is one-fourth of the outer pair. Unlike the first stage VCOs, no tail current is used in the second stage VCOs and the frequency of the VCOs is controlled by changing their supply voltage. Since, the input referred thermal noise of the second stage is first order

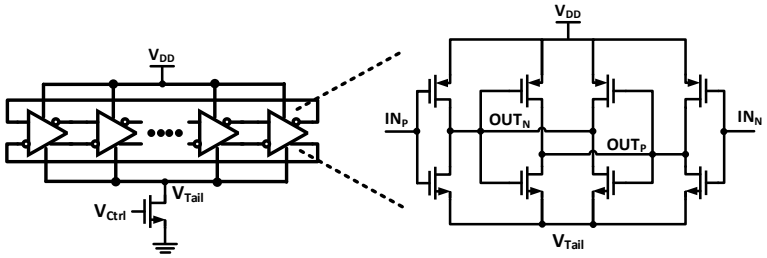


Figure 3.9: Delay cell used in the first stage VCO.

shaped, standard cell inverter gates with the minimum length are used to simplify the design and the layout. The frequency of the second stage VCO is changed by switching the lower supply voltage of $\text{VCO}_{2P,N}$ between V_{High} and V_{Low} through a pair of T-gate switches.

3.4.2 Sense amplifiers

The output signals of the VCOs are not rail-to-rail. Therefore, sense amplifier blocks are needed to convert these signals to rail-to-rail and feed them to to the following digital circuitry.

As can be seen in Fig. 3.8, sense amplifier flip-flops (SA-FFs) are used in the first and second stage. SA-FFs only operate for the rising edge of the CLK_S and they keep their output values for the rest of the time. This way, they consume a small amount of power. On the other hand, the sense amplifiers (SAs) used in the QPD block are required to operate continuously and, therefore, their power consumption can be high. To avoid a high power consumption of the SAs used in QPD block, only one SA is on during each sampling period and the rest of the

31 SAs are kept off. The proper SA is selected using the PTR signal. This way, the corresponding VCO output tap is amplified rail-to-rail and sent to the pulse extraction circuit.

3.4.3 Pulse extension

As can be seen in (3.12) the pulse width has a linear relationship with ϕ_{qC1}. Therefore, this pulse width can be very narrow. If it is too small, the pulse can not be completely generated due to the non-zero rise/fall time of the QPD block. In addition, in practice if the pulse width is too small the second stage VCO frequency can't reach its expected high frequency before the pulse goes down again. In this case some of the ϕ_{qC1} will be lost which will result in a performance degradation. To avoid this issue a pulse extension technique is used. In this technique, an offset is added to all the pulses to make sure, the frequency of the second stage VCO is able to switch completely between f_{High} and f_{Low} for any ϕ_{qC1} value.

In this design an offset value of two LSBs has been added to all the samples. Fig. 3.10 shows the modified pulse generation circuit where the pulse extension technique is incorporated. By XORing each sample VCO phase tap ($\phi_{PS,i}$) with the third next phase tap ($\phi_{P,i+3}$), two LSB are added to all the samples. Note that due to the usage of the pulse extension technique, the limited rise/fall times won't affect the ϕ_{qC1} extraction if the added time offset size is designed to be larger than the rise time required for $E_{Q1}(t)$ to settle to the high value before it has to go to the low value again [35].

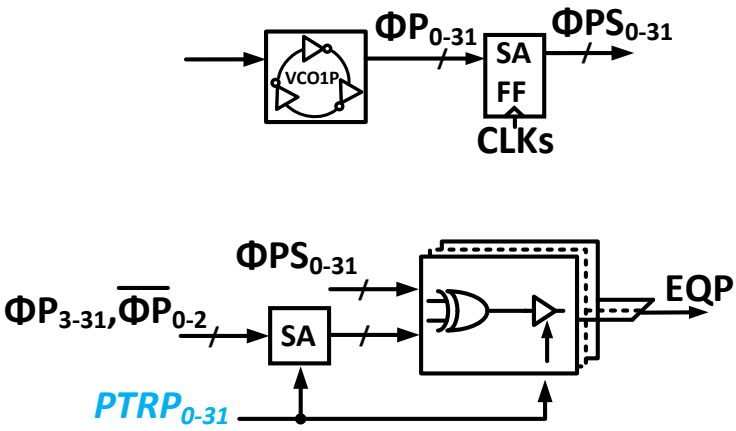


Figure 3.10: Pulse extension.

3.5 Measurement Results

The prototype ADC was fabricated in a 65 nm CMOS process with an active area of 0.26 mm^2. The chip is assembled in a 48 pin QFN package. Fig. 3.11 shows the test board, package and the die micrograph.

In this design for layout ease the first stage and the QPD blocks are partitioned to 32 equivalent sub-blocks. Each sub-block contains one element of the required pseudo differential circuitry including the VCO$_1$ delay cell, DAC elements, SA, SA-FF and the required ϕ_{qC1} extraction circuitry of each VCO$_1$ phase tap. Therefore, by drawing the layout of one sub-block, the entire first stage and QPD which contains 32 of these sub-blocks can be easily laid out. While creating the layout in this way is easier, it is not an optimum method to minimize the layout size.

The performance of the ADC is summarized in Table 3.1 and compared with

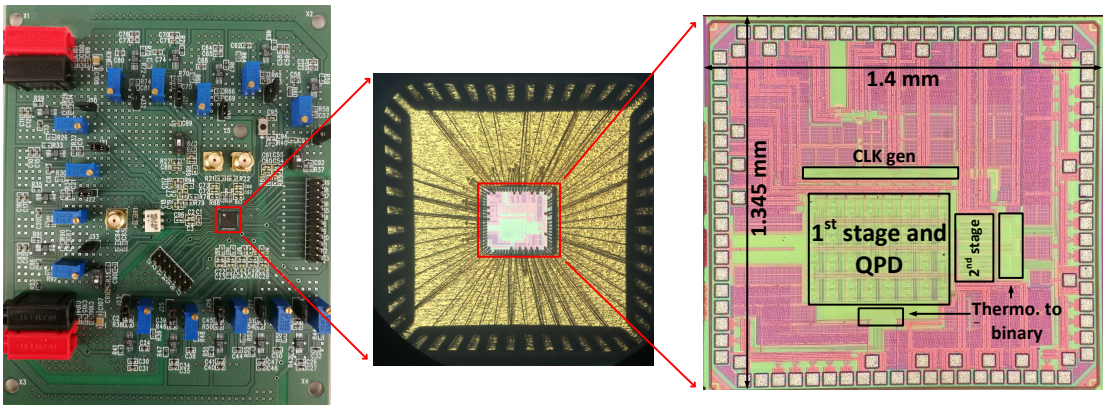


Figure 3.11: Test board, the package and the die micrograph.

the state of the art CT $\Delta\Sigma$ modulators with similar specifications. The ADC consumes 1.248 mW at a sampling frequency of 125 MHz from a 0.9 V supply. Fig. 3.12 shows the power breakdown of the ADC. The analog blocks (VCOs and DAC) consume 279 µW and the digital blocks consume 968 µW. The ADC achieves peak DR/SFDR/SNR/SNDR of 82.7/88.7/80.3/79.7 dB in a 2 MHz signal BW resulting in an ENOB of 12.95 and FoM$_S$ of 171.7 dB. The output power spectral densities (PSD) of the first stage along with the final output are shown in Fig. 3.13(a) with a 500 kHz, -1 dBFS (1.25 Vpp) differential input signal. The first stage shows 1^{st} order noise shaping while the final output shows second order noise shaping. The measured SNR and SNDR plotted as functions of the input amplitude are shown in Fig. 3.13(b); the modulator achieves a dynamic range of 82.7 dB. NCF_2 gain, G (shown in Fig. 3.8) has a value of 6.6. As shown in Fig. 3.14 a less than 1 dB drop in SNDR is observed for G varying by $\pm 10\%$.

A highly linear 2^{nd} order OTA-less VCO-based ADC is realized by using low

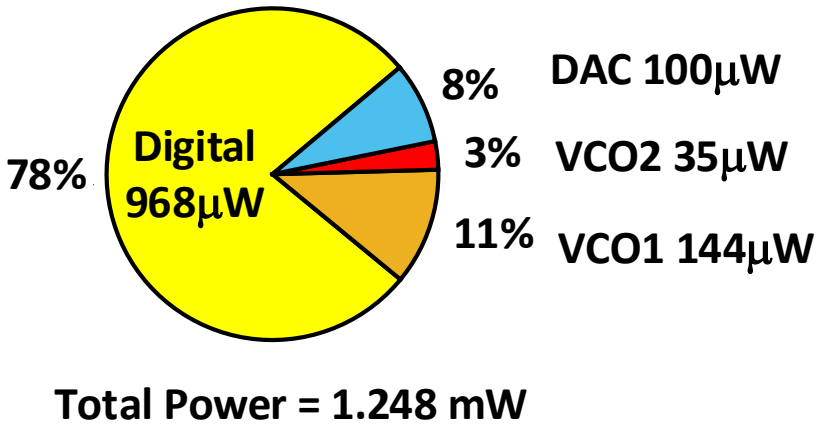
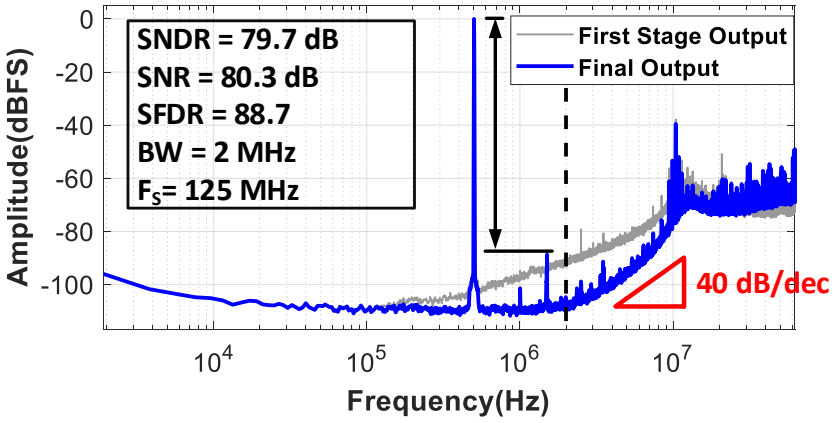


Figure 3.12: Power breakdown.

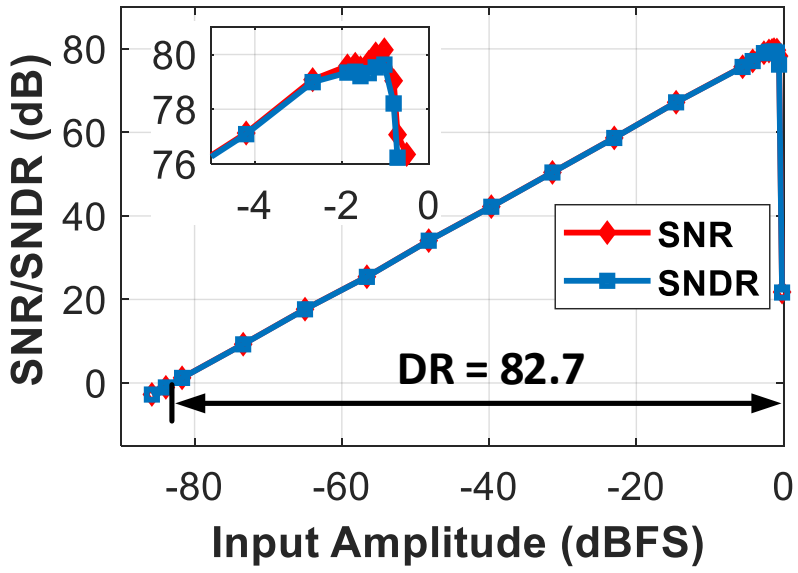
power and scaling friendly circuits. The performance of the ADC compares favorably with state-of-the-art CT $\Delta\Sigma$ modulators.

3.6 Conclusion

A highly linear 1-1 MASH VCO-based ADC is implemented without the use of OTAs or power hungry linearization methods. The measured prototype ADC has a 79.7 dB SNDR with an FoM$_S$ of 171.7 dB. This is the best FoM$_S$ reported for VCO-based ADCs to date. This performance is achieved by utilizing a novel circuit to extract the quantization error of a multi-phase VCO-based phase quantizer in the time domain as a PWM signal. Since the proposed ADC employs digital scaling friendly blocks, this architecture will benefit from technology scaling.



(a)



(b)

Figure 3.13: (a) Measured output PSD. (b) Measured SNR/SNDR versus input amplitude. The measurements have been done for 65536 sampled points.

Table 3.1: Performance summary and comparison to prior art

Architecture	**VCO-based CTDSM**					**Conventional CTDSM**			
Reference	**This work**	[36]	[37]	[33]	[38]	[39]	[40]	[41]	[42]
NTF order	**2**nd	2nd	2nd	3rd	1st	3rd	4th	4th	3rd
Need OTA	**No**	No	Yes	No	No	Yes	Yes	Yes	Yes
Process(nm)	**65**	40	90	65	130	65	55	130	65
Fs(MHz)	**125**	330	600	1600	250	1000	140	256	320
BW(MHz)	**2**	6	10	10	2	10	2.2	2	2
SNDR(dB)	**79.7**	68.6	78	65.7	74.7	72.2	90.4	74.4	69.1
SNR(dB)	**80.3**	–	79.1	66.2	–	76	–	80.5	–
DR(dB)	**82.7**	70.8	–	71	77.6	77	92	82	76.2
Power(mW)	**1.248**	0.524	16	3.7	1.05	1.57	4.5	5	0.256
Area(mm2)	**0.26**	0.028	0.36	0.01	0.13	0.027	0.09	0.33	0.013
FOM$_W$(fJ/step)1	**39.6**	19.9	123.2	119.3	59	23.6	37.8	291.4	27.5
FOM$_S$(dB)2	**171.7**	169.2	166	160	167.5	170.2	177.3	160.4	168

1 $FOM_W = \text{Power}/(2\times\text{BW})/2^{ENOB}$

2 $FOM_S = SNDR + 10 \times log_{10}(\text{BW}/\text{Power})$

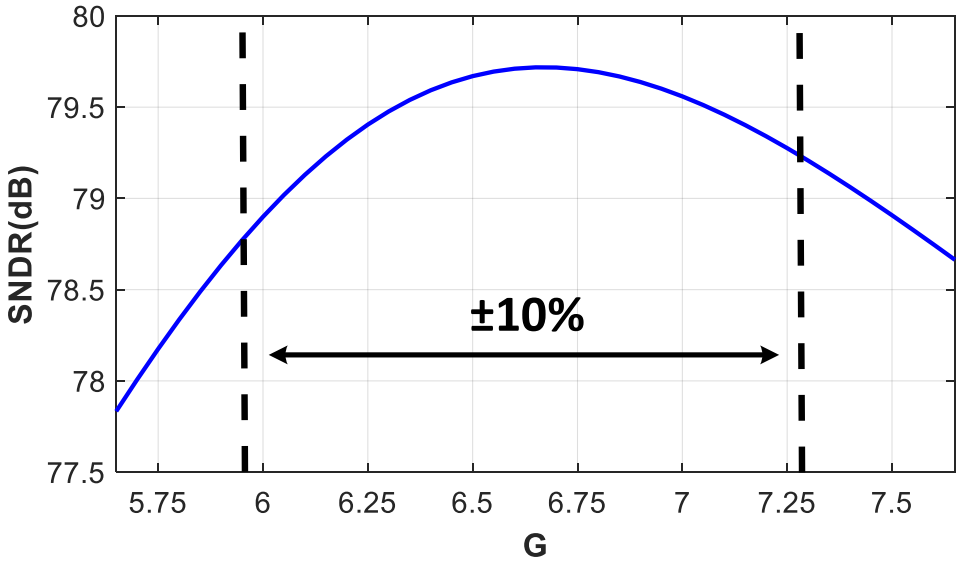


Figure 3.14: Effect of NCF_2 gain (G) variation from its nominal value.

Bibliography

[1] C. Yang, W. Shen, and X. Wang, "The internet of things in manufacturing: Key issues and potential applications," *IEEE Systems, Man, and Cybernetics Magazine*, vol. 4, no. 1, pp. 6–15, 2018.

[2] S. S. Reka and T. Dragicevic, "Future effectual role of energy delivery: A comprehensive review of Internet of Things and smart grid," *Renewable and Sustainable Energy Reviews*, vol. 91, pp. 90–108, 2018.

[3] M. H. Maghami, A. M. Sodagar, A. Lashay, H. Riazi-Esfahani, and M. Riazi-Esfahani, "Visual prostheses: The enabling technology to give sight to the blind," *Journal of ophthalmic & vision research*, vol. 9, no. 4, p. 494, 2014.

[4] M. Ghayoor *et al.*, "Microstructural Analysis of Additively Manufactured 304L Stainless Steel Oxide Dispersion Strengthened Alloy," *Microscopy and Microanalysis*, 2019.

[5] M. S. Nahvi *et al.*, "Design, fabrication, and test of flexible thin-film microelectrode arrays for neural interfaces," in *2017 IEEE 30th Canadian Conference on Electrical and Computer Engineering (CCECE)*. IEEE, 2017, pp. 1–4.

[6] P. Payandehnia *et al.*, "High speed CML latch using active inductor in 0.18 μm CMOS technology," in *2011 19th Iranian Conference on Electrical Engineering*. IEEE, 2011, pp. 1–4.

[7] M. Ghayoor, K. Lee, Y. He, C.-h. Chang, B. K. Paul, and S. Pasebani, "The Role of Volumetric Energy Density on the Microstructure and Texture of 304L Stainless Steel Produced via Selective Laser Melting," *Additive Manufacturing*, 2019.

[8] H. H. Boo, D. S. Boning, and H.-S. Lee, "15.6 12b 250MS/S pipelined ADC with virtual ground reference buffers," in *Solid-State Circuits Conference-(ISSCC), 2015 IEEE International*. IEEE, 2015, pp. 1–3.

[9] S. Leuenberger, P. K. Venkatachala, A. ElShater, M. Oatman, C. Lee, B. Xiao, and U.-K. Moon, "An empirical study of the settling performance of ring amplifiers for pipelined ADCs," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2018, pp. 1–5.

[10] K. Nanbakhsh, H. Maghami, S. Sheikhaei, N. Masoumi, and P. Payandehnia, "A low power 9.5 ENOB 100MS/s pipeline ADC using correlated level shifting," in *Electrical and Computer Engineering (CCECE), 2011 24th Canadian Conference on*. IEEE, 2011, pp. 001 379–001 382.

[11] M. H. Naderi and J. Silva-Martinez, "Algorithmic-pipelined ADC with a modified residue curve for better linearity," in *2017 IEEE 60th International Mid-*

west Symposium on Circuits and Systems (MWSCAS), Boston, MA, USA, 2017, pp. 1446–1449.

[12] M. Liu, P. Harpe, R. van Dommele, and A. van Roermund, "15.4 a 0.8 v 10b 80ks/s sar adc with duty-cycled reference generation," in *Solid-State Circuits Conference-(ISSCC), 2015 IEEE International*. IEEE, 2015, pp. 1–3.

[13] C. Lee, S. Leuenberger, P. K. Venkatachala, A. ElShater, M. Oatman, B. Xiao, and U.-K. Moon, "A Power Efficient SAR Algorithm for High Resolution ADCs," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2018, pp. 1–5.

[14] M. Tohidian, I. Madadi, and R. B. Staszewski, "Analysis and design of a high-order discrete-time passive iir low-pass filter," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 11, pp. 2575–2587, 2014.

[15] P. Payandehnia, H. Maghami, H. Mirzaie, M. Kareppagoudr, S. Dey, M. Tohidian, and G. C. Temes, "A 0.49-13.3 MHz Tunable Fourth-Order LPF with Complex Poles Achieving 28.7 dBm OIP3," *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2018.

[16] M. H. Maghami and A. M. Sodagar, "Fully-integrated, large-time-constant, low-pass, Gm-C filter based on current conveyors," in *2011 18th IEEE International Conference on Electronics, Circuits, and Systems*. IEEE, 2011, pp. 281–284.

[17] J. A. Fredenburg and M. P. Flynn, "A 90-MS/s 11-MHz-bandwidth 62-dB SNDR Noise-Shaping SAR ADC," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 2898–2904, 2012.

[18] P. Payandehnia, H. Mirzaie, H. Maghami, J. Muhlestein, and G. Temes, "Fully passive third-order noise shaping SAR ADC," *Electronics Letters*, vol. 53, no. 8, pp. 528–530, 2017.

[19] H. Ghaedrahmati and J. Zhou, "160 MS/s 20 MHz bandwidth third-order noise shaping SAR ADC," *Electronics Letters*, vol. 54, no. 3, pp. 128–130, 2018.

[20] N. Maghari and U.-K. Moon, "A Third-Order DT $\Delta\Sigma$ modulator using noise-shaped bi-directional single-slope quantizer," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 12, pp. 2882–2891, 2011.

[21] H. Mirzaie, H. Maghami, R. Zanbaghi, P. Payandehnia, K. Mayaram, and T. S. Fiez, "A 72.4 dB SNDR 92 dB SFDR Blocker Tolerant CT $\Delta\Sigma$ Modulator with Inherent DWA," *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2018.

[22] M. H. Maghami and M. Yavari, "Multirate double-sampling hybrid CT/DT sigma-delta modulators for wideband applications," in *2009 IEEE International Symposium on Circuits and Systems*. IEEE, 2009, pp. 2253–2256.

[23] S. Dey, K. Reddy, K. Mayaram, and T. S. Fiez, "A 50 MHz BW 76.1 dB DR Two-Stage Continuous-Time DeltaSigma Modulator With VCO Quan-

tizer Nonlinearity Cancellation," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 3, pp. 799–813, March 2018.

[24] P. K. Venkatachala, S. Leuenberger, A. ElShater, C. Lee, J. Muhlestein, B. Xiao, M. Oatman, and U. Moon, "Passive compensation for improved settling and large signal stabilization of ring amplifiers," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2018, pp. 1–5.

[25] M. Z. Straayer and M. H. Perrott, "A 12-bit, 10-MHz bandwidth, continuous-time $\Sigma\Delta$ ADC with a 5-bit, 950-MS/s VCO-based quantizer," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 4, pp. 805–814, 2008.

[26] K. Reddy, S. Rao, R. Inti, B. Young, A. Elshazly, M. Talegaonkar, and P. K. Hanumolu, "A 16mW 78dB-SNDR 10MHz-BW CT- ADC using residue-cancelling VCO-based quantizer," in *2012 IEEE International Solid-State Circuits Conference*, Feb 2012, pp. 152–154.

[27] P. Zhu, X. Xing, and G. Gielen, "A 40 MHz-BW 35 fJ/step-FoM nonlinearity-cancelling two-step ADC with dual-input VCO-based quantizer," in *Proc. IEEE European Solid State Circuits Conference (ESSCIRC)*, 2014, pp. 63–66.

[28] W. Yu, K. Kim, and S. Cho, "A 148 fs_{rms} Integrated Noise 4 MHz Bandwidth Second-Order $\Delta\Sigma$ Time-to-Digital Converter With Gated Switched-Ring Oscillator," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 8, pp. 2281–2289, 2014.

[29] S. B. Rao, "Linearizing techniques for voltage controlled oscillator based analog to digital converters," Ph.D. dissertation, 2013.

[30] M. Park and M. H. Perrott, "A 78 dB SNDR 87 mW 20 MHz Bandwidth Continuous-Time $\Delta\Sigma$ ADC With VCO-Based Integrator and Quantizer Implemented in 0.13 μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3344–3358, 2009.

[31] K. Reddy, S. Dey, S. Rao, B. Young, P. Prabha, and P. K. Hanumolu, "A 54mW 1.2 GS/s 71.5 dB SNDR 50MHz BW VCO-Based CT $\Delta\Sigma$ ADC Using Dual Phase/Frequency Feedback in 65nm CMOS," in *Proc. IEEE Symp. VLSI Circuits Dig. Tech. Papers*, 2015, pp. C256–C257.

[32] K. Lee, Y. Yoon, and N. Sun, "A Scaling-Friendly Low-Power Small-Area$\delta\sigma$ ADC with VCO-Based Integrator and Intrinsic Mismatch Shaping Capability," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 5, no. 4, pp. 561–573, Dec 2015.

[33] A. Babaie-Fishani and P. Rombouts, "A mostly digital VCO-based CT-SDM with third-order noise shaping," *IEEE J. of Solid-State Circuits*, vol. 52, no. 8, pp. 2141–2153, 2017.

[34] H. Maghami, P. Payandehnia, H. Mirzaie, R. Zanbaghi, S. Dey, J. Goins, K. Mayaram, and T. S. Fiez, "A 0.9V 79.7dB SNDR 2MHz-BW 1-1 MASH OTA-less VCO-based $\Delta\Sigma$ ADC with a Novel Phase Quantization Noise Ex-

traction Technique," in *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, 2019, pp. 1–4.

[35] H. Maghami, P. Payandehnia, H. Mirzaie, R. Zanbaghi, S. Dey, K. Mayaram, and T. S. Fiez, "A Highly Linear OTA-Free VCO-Based 1-1 MASH $\Delta\Sigma$ ADC," *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2019.

[36] S. Li and N. Sun, "A 0.028 mm^2 19.8 fJ/step 2^{nd}-order VCO-based CT $\Delta\Sigma$ modulator using an inherent passive integrator and capacitive feedback in 40nm CMOS," in *Proc. IEEE Symp. VLSI Circuits Dig. Tech. Papers*, June 2017, pp. C36–C37.

[37] K. Reddy, S. Rao, R. Inti, B. Young, A. Elshazly, M. Talegaonkar, and P. K. Hanumolu, "A 16mW 78dB-SNDR 10MHz-BW CT-$\Delta\Sigma$ ADC Using Residue-Cancelling VCO-Based Quantizer," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*. IEEE, 2012, pp. 152–154.

[38] S. Li and N. Sun, "A 174.3 dB FoM VCO-based CT $\Delta\Sigma$ modulator with a fully digital phase extended quantizer and tri-level resistor DAC in 130nm CMOS," in *ESSCIRC Conference*, Sept. 2016, pp. 241–244.

[39] N. F. S. V. Paulino and J. C. d. P. Goes, "A 1V 77dB-DR 72dB-SNDR 10MHz-BW 2-1 MASH CT SDM," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2016, pp. 274–276.

[40] C. Ho, C. Liu, C. Lo, H. Tsai, T. Wang, and Y. Lin, "15.2 A 4.5mW CT self-coupled modulator with 2.2MHz BW and 90.4dB SNDR using residual ELD compensation," in *Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2015, pp. 1–3.

[41] R. Rajan and S. Pavan, "A 5mW CT $\Delta\Sigma$ ADC With Embedded 2^{nd}-order Active Filter and VGA Achieving 82dB DR in 2MHz BW," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 478–479.

[42] J. L. A. de Melo, J. Goes, and N. Paulino, "A 0.7 V 256 μW $\Delta\Sigma$ Modulator With Passive RC Integrators Achieving 76 dB DR in 2 MHz BW," in *Proc. IEEE Symp. VLSI Circuits Dig. Tech. Papers*, June 2015, pp. C290–C291.

Chapter 4: A Novel Time-Domain Phase Quantization Noise Extraction for a VCO-based Quantizer

A highly linear SAR-VCO MASH delta-sigma ADC architecture is presented. OTA based analog integrators are not needed whereby the ADC is mostly digital and process scaling friendly. A new technique is introduced to extract the quantization noise of the VCO-based quantizer as a PWM signal using digital circuitry. This technique is independent of the OSR and the input signal amplitude of the VCO-based quantizer making it attractive for higher bandwidth applications. The proposed technique is demonstrated with a 0-1-1 MASH delta-sigma architecture. Behavioral simulations show second order noise shaping with 75dB SNDR for an OSR of 20.

4.1 Introduction

Advances in silicon chips, software, storage, sensors, additive manufacturing and networking is reshaping everything in today's lives. It is creating vast new opportunities for individuals and challenges for the designers. These systems are required to operate with optimized energy efficiency to make their implementation economically attractive [1–7].

In this matter reducing power consumption is an important feature in analog

and mixed signal circuits such as filters [8, 9] and data converters [10, 11]. For medium-resolution and medium-speed ADCs, SAR ADCs [11–14] and pipeline ADCs [15, 16] are two popular architectures. SAR ADCs feature lower power consumption compared to pipeline ADCs. However, comparator noise is one of the main performance limiting issues.

Oversampling and noise shaping in SAR ADCs have been used to reduce the effect of comparator noise [11,17,18]. In [11] an OTA is used, which is not process scaling friendly. Whereas, in passive implementations [17,18], more capacitors are used which increases the chip area considerably. Hence, these approaches are not power and area efficient. For this reason, the digital friendly nature of VCO based quantizers makes them attractive in advanced nanometer CMOS processes [19]. However, often the major performance limitation of VCO-based quantizers is the VCO nonlinearity.

To mitigate the comparator noise problem of the SAR ADC and also the VCO nonlinearity, a two stage SAR-VCO ADC is introduced in [20]. The first stage is a coarse SAR ADC and the second stage is a VCO-based quantizer. The 0-1 multi-stage noise-shaping (MASH) architecture is implemented by feeding the quantization noise of the first stage to the second stage. Since the signal amplitude at the input of the VCO is small, the effect of the VCO nonlinearity is negligible. This architecture solves the VCO nonlinearity issue without using OTAs. However, the order of noise shaping is still limited to one. To increase the order of noise shaping in oversampling ADCs, several techniques including error feedback, and MASH ADC architectures can be used [21, 22]. In the MASH architecture, the

quantization noise of each stage must be extracted and fed to the next stage. However, the quantization noise of the VCO is in the phase domain and is not explicitly available. In [23], a quantization noise extraction technique for VCO based quantizers is introduced. This approach has a limited accuracy in extracting the quantization noise.

In this chapter and [24], a new method for extracting the VCO quantization noise, is proposed. Using the proposed technique, the quantization noise of a VCO-based quantizer is extracted precisely in the time domain as a PWM signal. By applying this pulse signal to another VCO-based quantizer, higher order MASH structures can be implemented. To show a proof of concept, an OTA free, digital friendly 0-1-1 MASH ADC is designed. The first stage is a coarse SAR ADC and the second and the third stages are VCO-based quantizers. Based on the architecture, the input of the first VCO is the quantization noise of the SAR ADC which is a small signal and the input of the second VCO is a two-level PWM signal. Therefore, the VCO nonlinearity does not limit the overall ADC performance. The proposed method can be further used to increase the order of the MASH by adding more VCO-based quantizer stages.

The rest of this chapter is organized as follows. In Section 4.2, a prior architecture related to phase quantization noise extraction presented in [23], is reviewed. The proposed phase quantization noise extraction technique is presented in Section 4.3. Simulation results are provided in Section 4.4. Section 4.5 concludes the chapter.

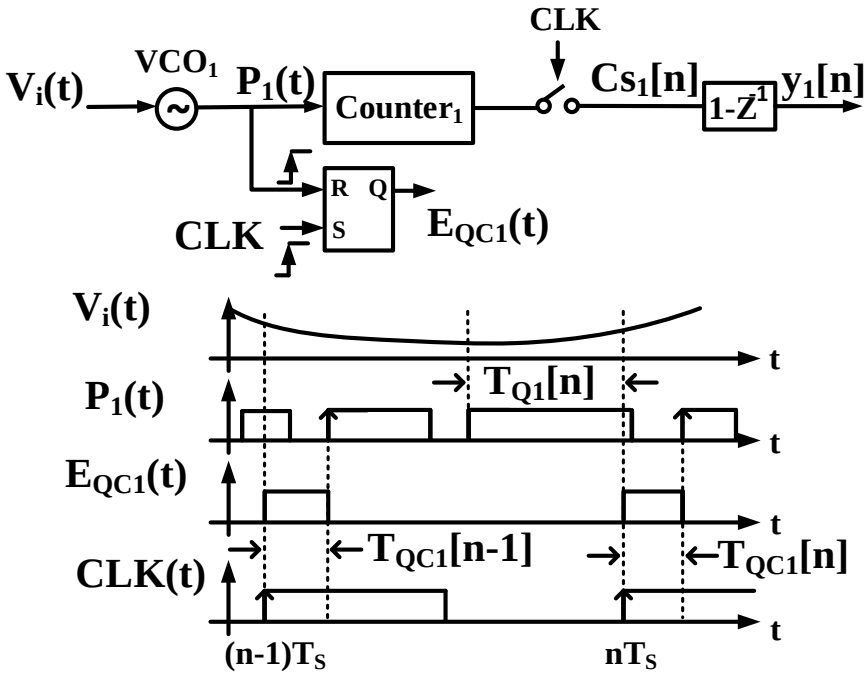


Figure 4.1: Conventional open-loop VCO-based ADC [19].

4.2 Prior Art

Fig. 4.1 shows a conventional open-loop VCO-based ADC using a counter as the quantizer [19]. The timing diagram of this VCO-based quantizer is also shown. The VCO acts as a phase integrator. The VCO output signal is P1(t), the frequency of which is a linear function of the VCO input signal $V_i(t)$. The relationship between the VCO1 output phase and its input voltage is as follows:

$$\phi_1(t) = 2\pi \int_{-\infty}^{t} (K_{VCO1} V_i(t) + f_{fr1})\, dt \tag{4.1}$$

where, K_{VCO1} and f_{fr1} are the voltage-to-frequency gain and the free-running frequency of VCO_1, respectively. $\mathrm{Counter}_1$ output increases by one unit for each rising edge of $P_1(t)$ which is equal to a 2π radian phase change of the VCO output. The counter output is sampled at the rising edge of CLK. Equation (4.2) shows the sampled $\mathrm{Counter}_1$ output ($Cs_1[n]$).

$$Cs_1[n] = \frac{\phi_1(nT_S) - \phi_{q1}[n]}{2\pi} = \int_{-\infty}^{nT_S} (K_{VCO1}V_i(t) + f_{fr1})\,dt - \frac{\phi_{q1}[n]}{2\pi} \tag{4.2}$$

In this equation $\phi_1(nT_S)$ is the VCO output phase at the sampling instant of nT_S and $\phi_{q1}[n]$ is the phase quantization noise of the ADC at the n^{th} sampling instant. The $\phi_{q1}[n]$ is the VCO output phase change from the last rising edge of $P_1(t)$ to the rising edge of $CLK(t)$ in each sampling period. This time difference is shown by $T_{Q1}[n]$ in Fig. 4.1. Therefore $\phi_{q1}[n]$ is as follows:

$$\phi_{q1}[n] = 2\pi \int_{T_{Q1}[n]} (K_{VCO1}V_i(t) + f_{fr1})\,dt \tag{4.3}$$

Since, the VCO output phase change is equal to 2π between the two rising edges of $P_1(t)$, $\phi_{qc1}[n]$ can be defined as:

$$\phi_{qc1}[n] = 2\pi - \phi_{q1}[n] = 2\pi \int_{T_{QC1}[n]} (K_{VCO1}V_i(t) + f_{fr1})\,dt \tag{4.4}$$

where $T_{QC1}[n]$ is the time difference between the rising edge of the clock (nT_S) and the first rising edge of the VCO output ($P_1(t)$) in that clock period. This time difference is shown in Fig. 4.1 as a pulse signal $E_{QC1}(t)$. As (4.4) shows, $\phi_{qc1}[n]$ is the shifted value of -$\phi_{q1}[n]$ by 2π. In a real implementation extracting $T_{QC1}[n]$ is simpler than $T_{Q1}[n]$. Therefore, $\phi_{qc1}[n]$ is used in the analysis provided here after.

A digital differentiator is used after the counter. The generated output code is a representation of the VCO frequency and is equal to:

$$y_1[n] = \int_{(n-1)T_S}^{nT_S} (K_{VCO1}V_i(t) + f_{fr1})\,dt + \frac{\phi_{qc1}[n] - \phi_{qc1}[n-1]}{2\pi} \tag{4.5}$$

The counter output roll overs after reaching its maximum value. The digital differentiator is designed similar to [25] to provide the correct value.

Assuming the sampling frequency is much higher than the input signal bandwidth, the input signal can be considered a fixed value between two consecutive samples. Thus, using Z-transforms the ADC output is:

$$Y_1(z) = \left(K_{VCO1}T_S z^{-1}\right) V_i(z) + f_{fr1}T_S + \left(1 - z^{-1}\right) \frac{\phi_{qc1}(z)}{2\pi} \tag{4.6}$$

where $f_{fr1}T_S$ is a constant value and represents the output common-mode code. It can be seen from (4.6) that the phase quantization noise is 1^{st}-order noise shaped.

The quantization noise of the VCO-based ADC is in the phase domain and

is not explicitly available. As shown in (4.4), the phase quantization noise is the VCO output phase change over the $T_{QC1}[n]$ time period. As (4.4) shows, $\phi_{qc1}[n]$ is a nonlinear function of both $T_{QC1}[n]$ and the input signal ($V_i(t)$). Thus, $E_{QC1}(t)$ alone cannot be a representation of ϕ_{qc1}.

Fig. 4.2 shows the method used in [23] to approximately extract the phase quantization noise of a VCO as a pulse signal in the time domain. Compared to Fig. 4.1, there is no digital differentiator after the counter and the VCO is used in a closed feedback loop. VCO_1 is used in the phase domain and operates as an integrator. Counter_1 works as a phase quantizer and its output is sampled by a register which generates the output codes. This circuit is a 1^{st}-order continuous-time $\Delta\Sigma$ modulator and, therefore, provides 1^{st}-order noise shaping similar to Fig. 4.1. Similar to (4.4), the phase quantization noise (ϕ_{qc1}) can be derived as a function of the VCO_1 input signal ($G_1(t)$) as follows:

$$\phi_{qc1}[n] = \int_{T_{QC1}[n]} 2\pi \left(K_{VCO1} G_1(t) + f_{fr1}\right) dt \tag{4.7}$$

As shown in [23], by using the VCO as an integrator in a feedback loop, the VCO input signal variation is much smaller than that in the architecture shown in Fig. 4.1. This results in a small variation in the VCO frequency. Considering the frequency variation of VCO_1 is much smaller than f_{fr1}, (4.7) can be approximated as:

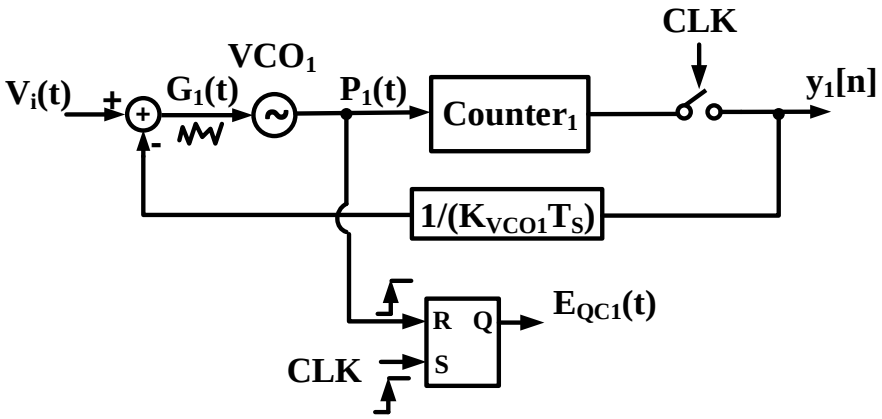


Figure 4.2: VCO quantization noise extraction reported in [23].

$$\phi_{qc1}[n] \approx 2\pi \int_{T_{QC1}[n]} f_{fr1} dt \tag{4.8}$$

Therefore, the $E_{QC1}(t)$ pulse width (T_{QC1}) has a linear relation with ϕ_{qc1} as follows:

$$T_{QC1}[n] \approx \frac{\phi_{qc1}[n]}{2\pi f_{fr1}} \tag{4.9}$$

Equation (4.9) shows that the pulse width of the $E_{QC1}(t)$ signal (T_{QC1}) is an approximate value of the phase quantization noise. In [23], this pulse is then used to drive a second stage VCO-based quantizer in a 1-1 MASH architecture.

It should be noted that, the $E_{QC1}(t)$ pulse width is an approximation of the

phase quantization noise. To make this approximation more accurate, the signal variation at the input of the VCO ($G_1(t)$) has to be reduced [23]. Therefore, a high number of quantizer levels and a high oversampling ratio (OSR) are required. A higher OSR limits the maximum input signal bandwidth. Also, this architecture requires a multi-bit DAC.

4.3 Proposed Structure

In this section, first, a novel method for extracting the quantization noise of a VCO-based quantizer is proposed. The proposed technique has higher accuracy compared to the technique introduced in [23]. Then, the proposed method, is applied to a MASH architecture as a proof of concept.

4.3.1 Proposed phase quantization noise extraction

Fig. 4.3 shows the proposed open-loop VCO-based quantizer along with the timing diagram. The proposed scheme extracts the phase quantization noise of the VCO precisely in the time domain as a pulse signal. As shown in Fig. 4.3, in the tracking mode, the input signal is connected to the VCO, and when CLK_{Track} is low, the VCO input is connected to a fixed voltage and the VCO oscillates with a fixed frequency. Similar to (4.5), the output of the ADC can be expressed as:

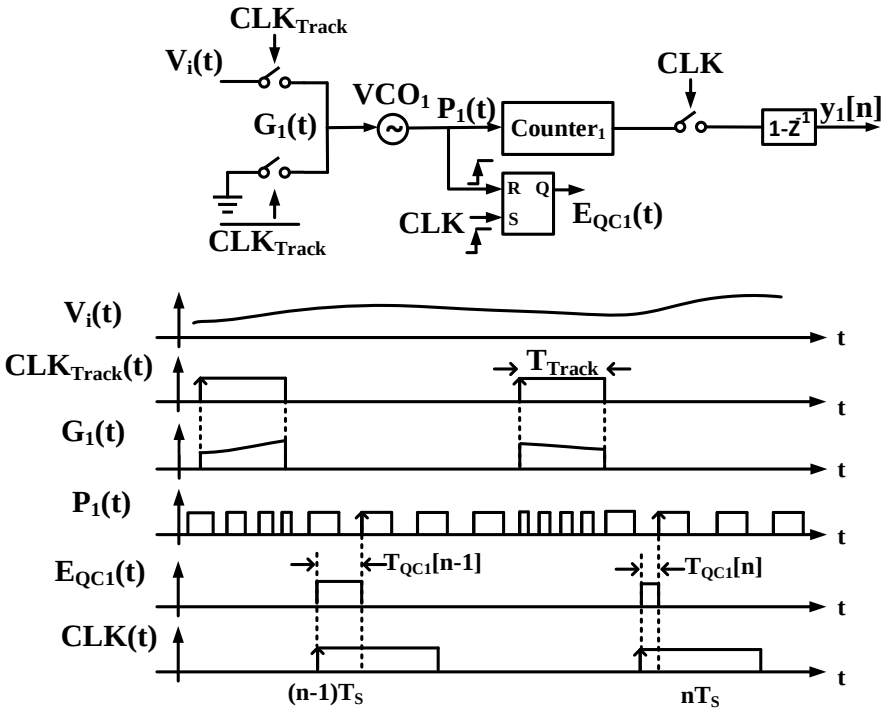


Figure 4.3: Proposed phase quantization noise extraction.

$$y_1[n] = \int_{(n-1)T_S}^{nT_S} \left(K_{VCO1} G_1(t) + f_{fr1}\right) dt + \frac{\phi_{qc1}[n] - \phi_{qc1}[n-1]}{2\pi} \tag{4.10}$$

During each sampling period, $G_1(t)$ tracks $V_i(t)$ for T_{Track}, therefore, (4.8) can be written as:

$$y_1[n] = \int_{T_{Track}} K_{VCO1} V_i(t) dt + f_{fr1} T_S + \frac{\phi_{qc1}[n] - \phi_{qc1}[n-1]}{2\pi} \tag{4.11}$$

Using Z-transforms the ADC output is:

$$Y_1(z) = \left(K_{VCO1} T_{Track} z^{-1}\right) V_i(z) + f_{fr1} T_S + \left(1 - z^{-1}\right) \frac{\phi_{qc1}(z)}{2\pi} \tag{4.12}$$

As the timing diagram shows, the VCO phase quantization takes place when CLK_{Track} is low. The phase quantization noise is generated at the rising edge of CLK. Since the VCO input signal ($G_1(t)$) is a fixed voltage at the rising edge of CLK, and remains constant for the T_{QC1} period, ϕ_{qc1} can be written as:

$$\phi_{qc1}[n] = 2\pi \int_{T_{QC1}[n]} f_{fr1} dt = 2\pi f_{fr1} T_{QC1}[n] \tag{4.13}$$

ϕ_{qc1} has a linear relationship to T_{QC1} and, therefore, the $E_{QC1}(t)$ pulse width precisely represents the phase quantization noise in the time domain.

Compared to the technique introduced in [23], the proposed method extracts the phase quantization noise independent of the OSR value and the VCO input signal variation.

4.3.2 Proposed MASH architecture

By having the quantization noise of the VCO-based quantizer available, MASH architectures can be easily constructed without using complex DACs and using only simple digital logic. Although the proposed phase quantization noise extraction is completely independent of the input signal variation, in reality the nonlinearity of the VCO has to be considered to avoid signal dependent harmonics. Therefore, to suppress the VCO nonlinearity problem, the input of the VCO has to be small enough. In the following, the proposed phase quantization noise extraction technique is used in a 0-1-1 MASH ADC to validate the idea. Fig. 4.4 shows the proposed 0-1-1 MASH ADC. The first stage is a conventional SAR ADC. Therefore, the output of the first stage is equal to:

$$Y_1(z) = V_i(z) + Q_1(z) \tag{4.14}$$

where $Q_1(z)$ is the quantization noise of the SAR ADC. Q_1 is available on the SARs DAC after the SAR conversion cycle is completed. When CLK_{Track} is high, Q_1 is connected to the second stage VCO and when CLK_{Track} is low, the VCO_1 input is connected to a fixed voltage. Similar to (4.12), the output of the second stage is the scaled value of Q_1 plus the shaped phase quantization noise of the second stage and is expressed as:

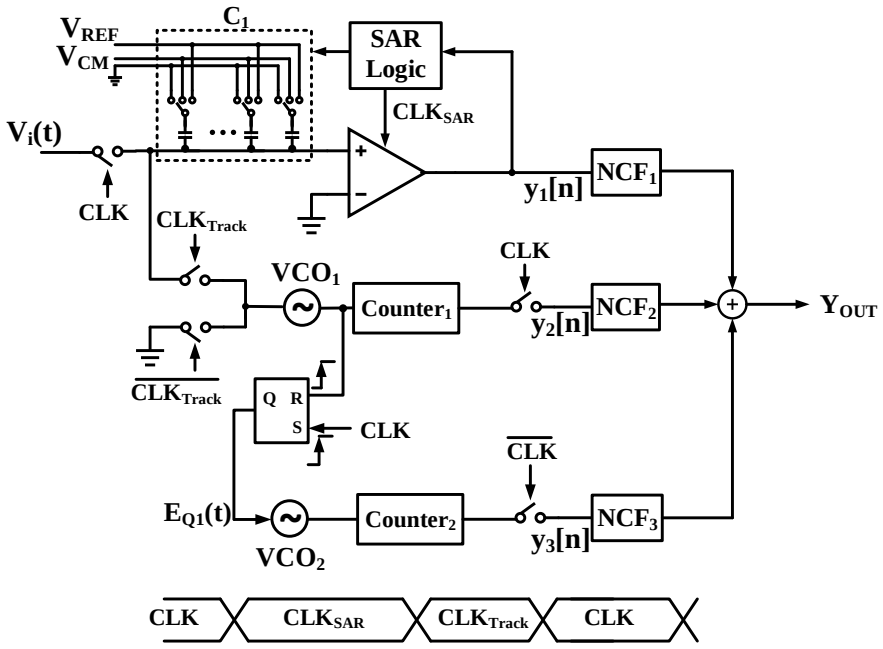


Figure 4.4: Proposed 0-1-1 MASH ADC structure.

$$Y_2(z) = \left(K_{VCO1} T_{Track} z^{-1}\right) Q_1(z) + \left(1 - z^{-1}\right) \frac{\phi_{q2}(z)}{2\pi} \tag{4.15}$$

The quantization of the second stage occurs when the VCO_1 input is connected to a fixed voltage. Therefore the quantization noise of the second stage, which is in the phase domain, can be precisely extracted in the time domain as a two level pulse signal. This pulse signal is fed to the third stage VCO quantizer. The output of the third stage is the scaled value of the second stage phase quantization noise plus the shaped phase quantization noise of the third stage [23].

$$Y_3(z) = \left(\frac{K_{VCO2}V_{DD}}{f_{fr1}}z^{-1}\right)\frac{\phi_{q2}(z)}{2\pi} + \left(1-z^{-1}\right)\frac{\phi_{q3}(z)}{2\pi} \tag{4.16}$$

Using the following simple digital noise cancellation filters (NCFs), a 0-1-1 MASH is realized.

$$\begin{aligned} NCF_1(z) &= z^{-2} \qquad NCF_2(z) = \tfrac{1}{K_{VCO1}T_{Track}} \times z^{-1} \\ NCF_3(z) &= \tfrac{1}{K_{VCO1}T_{Track}} \times \tfrac{f_{fr1}}{K_{VCO2}V_{DD}} \times (1-z^{-1}) \end{aligned} \tag{4.17}$$

Therefore, the final output realizes second order noise shaping.

$$Y_{out}(z) = V_i(z) \times z^{-2} + \tfrac{\phi_{q3}(z)}{2\pi} \times \tfrac{f_{fr1}}{K_{VCO1}T_{Track}K_{VCO2}V_{DD}} \times (1-z^{-1})^2 \tag{4.18}$$

Since, the input of VCO_1 is a small signal and the VCO_2 input is a two level PWM signal, the VCO nonlinearity does not limit the ADC performance.

4.4 Simulation Results

The proposed ADC shown in Fig. 4.4 has been simulated using a behavioral model in Cadence to validate the concept. A 5-bit SAR is used in the first stage to suppress the signal swing at the input of the second stage. The second and third

stage VCOs are identical with $K_{VCO} = 30f_s$ and $f_{fr} = 16f_s$, respectively. Since, the input of VCO_1 is a small signal and the VCO gain is not too high, a simple one bit counter is used as the second stage counter. Also, in this design a two bit counter is used in the third stage. Using low bit counters simplifies the design. In this design T_{Track} is set to be $0.2/f_s$. Fig. 4.5 shows the PSD of the proposed 0-1-1 MASH. A tone of -1dBFS is applied to the ADC. Considering an OSR=20, 75 dB of $SQNR$ with second order noise shaping is achieved. Fig. 4.6, shows the output $SQNR$ variation due to 10% mismatch between the values in NCF_2 and NCF_3 and their ideal analog values. As can be seen, variations in NCF_2 cause around 10dB reduction in $SNDR$ while variations in NCF_3 have only a negligible effect. Variations in NCF_2 results in Q_1 leakage to the output. Q_1 is the quantization noise of the coarse SAR ADC which is not shaped. While, variations in NCF_3 result in the second stage quantization noise leakage, which is already first-order shaped and, therefore, has a much smaller effect on the performance. In order to deal with the analog-digital filtering mismatch of NCF_2, the calibration method of [20] can be used.

4.5 Conclusion

A new method to precisely extract the phase quantization noise of a VCO-based quantizer has been proposed. By means of proper quantization timing and simple digital circuity, phase quantization noise is exactly mapped in the time domain as a PWM signal. Using this two level pulse signal, VCO-based MASH structures can

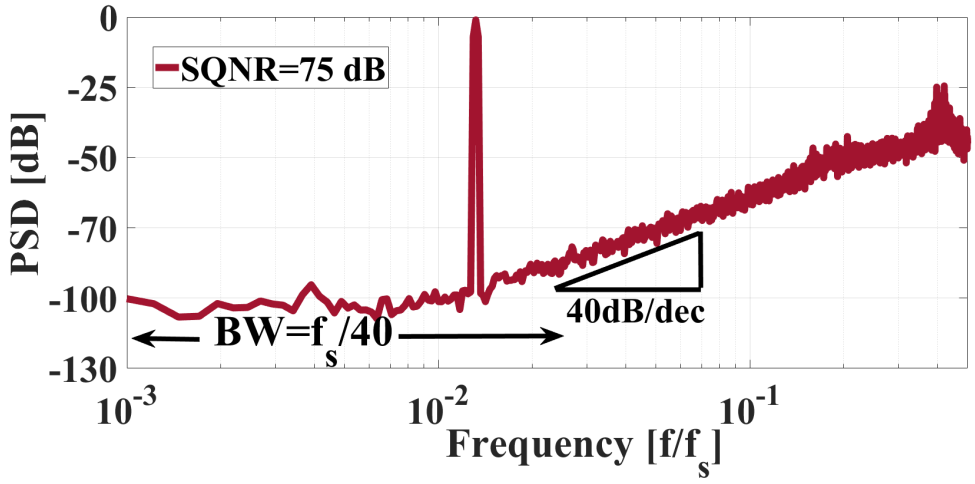


Figure 4.5: PSD of the proposed 0-1-1 MASH ADC.

be realized. Simulation results verify the performance of this method. As a proof of concept, a 0-1-1 MASH structure is designed and second order noise shaping is achieved without the need for an OTA. Since the input of the first VCO has a small amplitude and the input of the second VCO is inherently a PWM signal, the VCO nonlinearity does not degrade the performance.

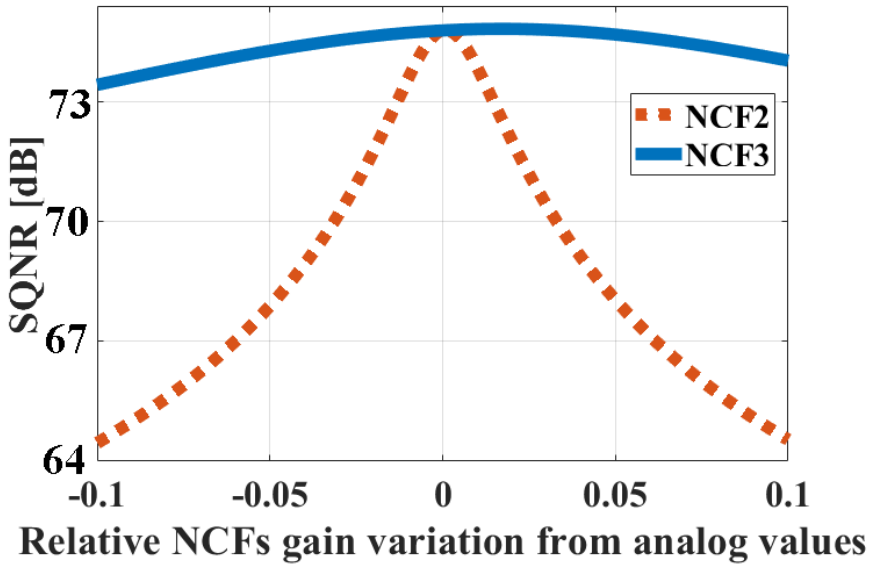


Figure 4.6: $SNDR$ VS. NCFs gain variation from their nominal values.

Bibliography

[1] T. L. Friedman, *Thank You for Being Late: An Optimist's Guide to Thriving in the Age of Accelerations (Version 2.0, With a New Afterword)*. Picador/Farrar Straus and Giroux, 2017.

[2] A. Aslani *et al.*, "Robustness of US Economy and Energy Supply/Demand Fluctuations," *International Journal of Energy Optimization and Engineering (IJEOE)*, vol. 6, no. 4, pp. 1–15, 2017.

[3] N. Ghorbani *et al.*, "Optimizing a hybrid wind-PV-battery system using GA-PSO and MOPSO for reducing cost and increasing reliability," *Energy*, vol. 154, pp. 581–591, 2018.

[4] M. H. Maghami, A. M. Sodagar, A. Lashay, H. Riazi-Esfahani, and M. Riazi-Esfahani, "Visual prostheses: The enabling technology to give sight to the blind," *Journal of ophthalmic & vision research*, vol. 9, no. 4, p. 494, 2014.

[5] M. G. Baghbani *et al.*, "Transient Liquid Phase Bonding of Al/Mg2Si Composite Using a Cu-Ni Mixed Powder," in *Advanced Materials Research*, vol. 829. Trans Tech Publ, 2014, pp. 632–637.

[6] M. Ghayoor *et al.*, "Water Atomized 17-4 PH Stainless Steel Powder as a Cheaper Alternative Powder Feedstock for Selective Laser Melting," in *Materials Science Forum*, vol. 941. Trans Tech Publ, 2018, pp. 698–703.

[7] S. Pasebani *et al.*, "Effects of atomizing media and post processing on mechanical properties of 17-4 PH stainless steel manufactured via selective laser melting," *Additive Manufacturing*, vol. 22, pp. 127–137, 2018.

[8] Y. Xu, S. Leuenberger, P. K. Venkatachala, and U.-K. Moon, "A 0.6 mW 31MHz 4 th-order low-pass filter with+ 29dBm IIP3 using self-coupled source follower based biquads in 0.18 μm CMOS," in *2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits)*. IEEE, 2016, pp. 1–2.

[9] P. Payandehnia *et al.*, "Passive switched-capacitor filter with complex poles for high-speed applications," *Electronics Letters*, vol. 52, no. 19, pp. 1592–1594, 2016.

[10] H. Mirzaie *et al.*, "A 72.4 dB SNDR 92 dB SFDR Blocker Tolerant CT $\Delta\Sigma$ Modulator with Inherent DWA," *IEEE Transactions on Circuits and Systems II: Express Briefs*, pp. 1–1, 2018.

[11] J. A. Fredenburg and M. P. Flynn, "A 90-MS/s 11-MHz-bandwidth 62-dB SNDR noise-shaping SAR ADC," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 2898–2904, 2012.

[12] P. Payandehnia *et al.*, "High-linearity SAR-VCO MASH $\Delta\Sigma$ ADC with second-order noise shaping," *Electronics Letters*, vol. 54, no. 24, pp. 1366–1368, 2018.

[13] A. ElShater, C. Y. Lee, P. K. Venkatachala, J. Muhlestein, S. Leuenberger, K. Sobue, K. Hamashita, and U.-K. Moon, "3.7 A 10mW 16b 15MS/s Two-Step SAR ADC with 95dB DR Using Dual-Deadzone Ring-Amplifier," in *2019 IEEE International Solid-State Circuits Conference-(ISSCC)*. IEEE, 2019, pp. 70–72.

[14] P. Payandehnia, H. Maghami, H. Mirzaie, M. L. Johnston, and G. C. Temes, "An Amplifier-Free 0–2 SAR-VCO MASH $\Delta\Sigma$ ADC," in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2019, pp. 1–5.

[15] M. H. Naderi and J. Silva-Martinez, "Algorithmic-pipelined ADC with a modified residue curve for better linearity," in *2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS), Boston, MA, USA*, 2017, pp. 1446–1449.

[16] P. K. Venkatachala, A. ElShater, Y. Xu, M. El-Chammas, and U.-K. Moon, "Voltage domain correction technique for timing skew errors in time interleaved ADCs," in *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2017, pp. 1–4.

[17] P. Payandehnia *et al.*, "Fully passive third-order noise shaping SAR ADC," *Electronics Letters*, vol. 53, no. 8, pp. 528–530, 2017.

[18] H. Ghaedrahmati and J. Zhou, "160 MS/s 20 MHz bandwidth third-order noise shaping SAR ADC," *Electronics Letters*, vol. 54, no. 3, pp. 128–130, 2018.

[19] M. Z. Straayer and M. H. Perrott, "A 12-bit, 10-MHz bandwidth, continuous-time $\Sigma\Delta$ ADC with a 5-bit, 950-MS/s VCO-based quantizer," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 4, pp. 805–814, 2008.

[20] A. Sanyal and N. Sun, "An Energy-Efficient Hybrid SAR-VCO $\Delta\Sigma$ Capacitance-to-Digital Converter in 40-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 7, pp. 1966–1976, 2017.

[21] S. Pavan, R. Schreier, and G. C. Temes, *Understanding Delta-Sigma Data Converters*. John Wiley & Sons, 2017.

[22] M. N. Alizadeh, S. M. Taleie, and D. Seo, "Error-feedback digital-to-analog converter (dac)," Dec. 26 2017, uS Patent 9,853,654.

[23] H. Maghami *et al.*, "A Highly Linear OTA-Free VCO-Based 1-1 MASH $\Delta\Sigma$ ADC," in *Proc. IEEE International Symposium on Circuits and Systems*, 2017.

[24] H. Maghami, H. Mirzaie, P. Payandehnia, K. Mayaram, R. Zanbaghi, and T. Fiez, "A Novel Time-Domain Phase Quantization Noise Extraction for a

VCO-based Quantizer," in *2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS)*. IEEE, 2018, pp. 145–148.

[25] P. Prabha *et al.*, "A highly digital VCO-based ADC architecture for current sensing applications," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 8, pp. 1785–1795, 2015.

Chapter 5: Conclusion

5.1 Conclusion

As Moore predicted, the scaling of the transistors, which are the key building blocks in the digital systems, has enormously impacted the microelectronics industry. Shrinking the transistor size has enabled the realization of extremely complex electronic devices we use in our daily lives. Although transistor scaling is desirable for digital systems, it makes the design of the analog systems such as ADCs more complicated.

ADCs often use conventional analog blocks such as OTAs or multi-bit voltage domain quantizers in their implementation. By moving to the smaller process nodes, the intrinsic gain of the transistors as well as the supply voltage decreases. Therefore, designing these analog blocks is the bottleneck in advanced CMOS processes.

In this thesis, alternative digital solutions are introduced to replace traditional analog blocks. In the proposed solutions, the major processing is done in time-domain rather than the voltage-domain. This way the proposed ADCs benefit from process scaling as the gate delays reduce.

In Chapter 2 a highly linear VCO-based 1-1 MASH $\Delta\Sigma$ ADC is presented. The proposed architecture does not require any OTA-based analog integrators or power

hungry linearization methods. Simulation results show that 2^{nd} order noise shaping is achieved by using a VCO as an integrator in the feedback loop of the first stage and an open loop VCO quantizer in the second stage. In this architecture single phase VCOs are utilized and the non-ideality effects are thoroughly examined and discussed.

In Chapter 3 multi-phase VCOs are used to implement the MASH ADC presented in the previous chapter. In this chapter a technique is introduced to extract the quantization noise of a multi-phase VCO in the time domian. The prototype is fabricated in a 65nm CMOS technology and achieves 2^{nd} order noise shaping. The measurement results show a DR/SFDR/SNR/SNDR of 82.7/88.7/80.3/79.7 dB for an input signal BW of 2 MHz. The fabricated design consumes 1.248 mW from a 0.9 V supply.

Chapter 4 describes another novel time-domain phase quantization noise extraction for a VCO-based quantizer. This technique is a highly accurate extraction method and is independent of the OSR and the input signal amplitude of the VCO-based quantizer. Therefore, it is an attractive method for higher bandwidth applications. Using this technique, a highly linear 2^{nd} order SAR-VCO MASH delta-sigma ADC architecture is presented. Simulation results show 2^{nd} order noise shaping with 75dB SNDR for an OSR of 20.

Each new process technology provides opportunities for new electronic devices to have more functionality. New process technologies also bring new challenges for analog/mixed-signal designers. This dissertation shows a collection of techniques to address the challenges faced due to process scaling. In the proposed techniques

the majority of the processing is done in the time-domain and high resolution and low power ADCs are designed. Also the digital nature of a VCO-based ADC lends itself well to a simple implementation and benefits from process scaling. These solutions show great potential to implement ADCs in future CMOS processes.

5.2 Future work

The fabricated VCO-based 1-1 MASH ADC is the first proof of concept. The power efficiency is not optimized and even better performance can be achieved as this architecture gets more mature. The performance is limited to the thermal noise and most of the power is consumed in the digital blocks. Therefore, using lower quantizer levels can lower the power consumption while having a small effect on the performance. Also, the first stage VCO phase noise is the main contributor of the noise while only a small fraction of the power is consumed by this block. Increasing the power consumption of the first stage VCO can help with improving the noise performance while increasing the overall power only slightly.

To have a robust performance, a calibration technique is introduced. The presented method is foreground and the ADC needs to be stopped every time calibration is needed. A background calibration can be implemented to avoid interrupting the ADC functionality.

In Chapter 4 a promising power efficient ADC architecture is presented. This ADC is capable of providing high performance at low OSRs which is desirable for high speed applications. Unfortunately, proof in silicon is not available for this

architecture. Fabrication of this ADC in a scaled CMOS process will provide a better idea of the achievable performance of the proposed scheme.