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Title: DESIGN, FABRICATION AND CHARACTERIZATION OF A COMPLEMENTARY GaAs MODFET STRUCTURE

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John Arthur

This thesis will describe design considerations, fabrication and characterization of a complementary GaAs Modulation Doped Field Effect Transistor (MODFET). A MODFET structure has the advantages of high speed and low power dissipation. Complementary MODFETs structures are desirable for improved simplicity, speed and circuit application. However, complementary MODFETs structures have previously been realized only with complex processing steps. In this work, we report a simple fabrication scheme for complementary MODFETs involving a single epitaxial growth step. A theoretical model for the I-V characteristics has been developed, which includes the parallel conduction in the AlGaAs layer. Comparison of the calculated I-V characteristics with the measured results from our device indicates that parallel conduction is an important mechanism in real devices. Previous modeling efforts have ignored this possibility. Our MODFETs with 2.5 um gate length show an unit gain frequency at 5 GHz. It should be possible to increase this frequency significantly with improved processing.

DESIGN, FABRICATION AND CHARACTERIZATION OF A COMPLEMENTARY GaAs MODFET STRUCTURE

by

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DESIGN, FABRICATION AND CHARACTERIZATION OF A COMPLEMENTARY GaAs MODFET STRUCTURE

1. Introduction

This thesis describes design considerations, material growth, fabrication and characterization of a complementary Gallium Arsenide (GaAs)/Aluminum Gallium Arsenide (AlGaAs) Modulation Doped Field Effect Transistor (MODFET).

Since the invention of the transistor in 1947, semiconductor materials have been a key research area. Since the early 1960s silicon (Si) became the major material for semiconductor fabrication. It has been studied most widely among all semiconductor materials. Silicon technology is by far the most mature among all other semiconductor technologies.

In spite of the preeminence of Si, other semiconductor materials have been utilized for their unique properties. For example, the III-V compound semiconductors have been extensively studied for their high speed circuit performance, and gallium arsenide has been widely used for microwave amplification since the late 1960s.

One important area of research in semiconductor technology is the crystal growth between two different materials. When an interface between two different materials is formed, the energy band gap across the interface is discontinuous. The interface is called a heterointerface or

heterojunction interface. The band gap discontinuity can be used advantageously in the design of new semiconductor devices. The MODFET is one application of the heterostructure technique.

A MODFET is a heterojunction device which has the desirable properties of high-speed operation and low-power dissipation. Carriers in this device form a two dimensional electron or hole gas at the heterointerface, in which very high carrier mobility can be achieved. The structure of a typical MODFET device is shown in figure 1.1 as an example. There are four layers in this structure : an intrinsic GaAs buffer layer, an undoped AlGaAs spacer layer, a doped AlGaAs donor layer, and the cap layer. The physical reason for each for these layers will be discussed later.

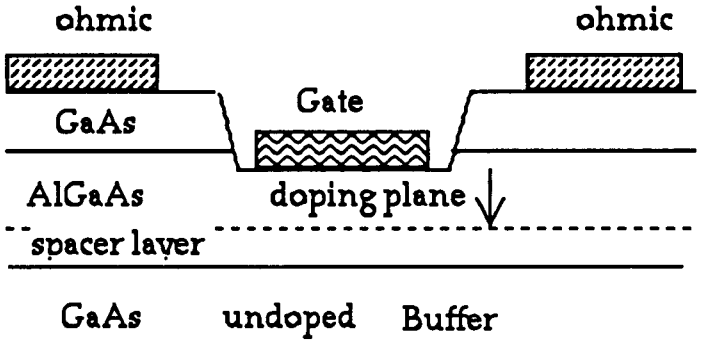

Figure 1.1 Cross section of a typical MODFET structure.

1.1 High Electron Mobility Transistor

R. A. Anderson first predicted that a two dimensional electron gas (2DEG) will form at the heterojunction interface in 1960 [1]. In 1969, L. Esaki and R. Tsu suggested that the mobility of 2DEG will be enhanced

because of the spatial separation of the carriers from their parent impurity atoms [2]. R. Dingle, et al. first reported the mobility enhancement phenomena in the modulation doped GaAs/AlGaAs heterojunction supperlattice in 1978 [3]. In 1980, T. Mimura et al. fabricated the first MODFET devices [4].

The energy band gap of GaAs is 1.424 electron volt at room temperature. AlGaAs has a larger energy band gap than GaAs and the value of the AlGaAs band gap increases as the Al mole fraction increases. Equations for the energy band gap are listed below, where x is the Al mole fraction [5].

$$E_g = 1.424 + 1.247 \cdot x \qquad 0 < x < 0.45$$

$$= 1.900 + 0.125 \cdot x + 0.143 \cdot x^2 \qquad x > 0.45$$

Carriers in the semiconductor always occupy the lowest possible energy states. Therefore, free carriers in a wide band gap material such as AlGaAs tend to diffuse to a narrow band gap material such as GaAs. The heterojunction interface is formed between the intrinsic GaAs buffer layer and the undoped AlGaAs spacer layer. Carriers in the doped AlGaAs layer will transfer into the GaAs buffer layer forming a conductive channel. The ionized impurities in the doped layer and the accumulated carriers in the channel will thus create a large electric field across the heterojunction interface. This electric field causes band bending in the interface resulting in the formation of a triangular potential well. Carriers from the doped region are confined in this potential well and form a two

dimensional carrier gas. Energy quantization also occurs in the quantum well. The quantum mechanical problem of a particle in a triangular potential well is well known [6]. The energy band diagram of a uniform doped n-MODFET is shown in figure 1.2.

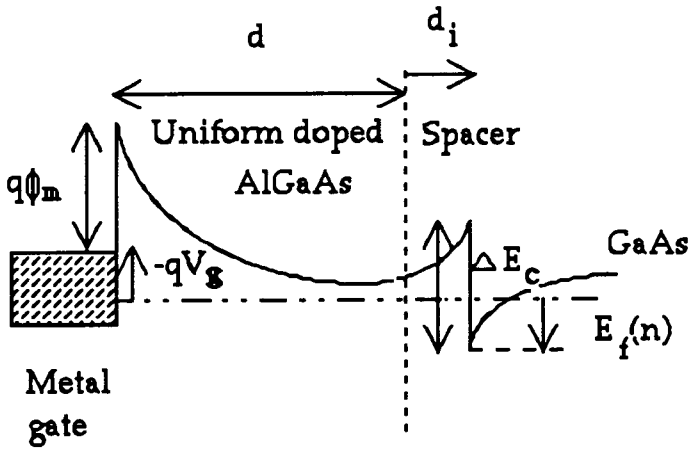

Figure 1.2 Conduction energy band diagram

The mobility in the active region is high because the carriers reside in undoped GaAs. Such mobility enhancement is the result of physical separation of the channel carriers from ionized impurities which suppresses impurity scattering. The mobility enhancement at low temperature is more pronounced because impurity scattering is the dominant scattering mechanism at low temperature. Increasing the spacer layer thickness also increases the carrier mobility, but the device peak transconductance decreases as the spacer layer becomes thicker due to a smaller number of carriers in the channel [7,8].

Two doping methods are commonly used in MODFET devices. The first is the uniform doping method in which the impurity concentration in the AlGaAs layer is constant outside the spacer layer. This is the original scheme used in early MODFETs. Recently it has been realized that the MODFETs can be fabricated by delta doping, where only a very narrow AlGaAs region is heavily doped. The carrier transfer efficiency has been reported to be higher with delta doping than with uniform doping [9]. The ideal condition for delta doping is when all impurity atoms reside in one atomic plane. However, the impurity atoms tend to diffuse away from the doping plane during crystal growth. Therefore, the real impurity concentration profile is a gaussian distribution. We describe the distribution in terms of the full width half-maximum (FWHM) defined as the thickness of AlGaAs layer in which the Si doping concentration is higher than 50% of the maximum Si concentration in the doping layer. The major factor determining such spreading is the substrate temperature during growth. For example, a FWHM of 5 nm for a Si profile was reported for a substrate temperature of 500 ^{o}C in an $Al_{0.3}Ga_{0.7}As$ delta doped layer [10]. If the substrate temperature was increased to 600 ^{o}C, the FWHM value increased to 12 nm, and increased further to 30 nm at a substrate temperature of 700 ^{o}C. For all materials used in the present thesis, the substrate temperature was kept between 570 ^{o}C and 580 ^{o}C which resulted in a FWHM of roughly 10 nm. Further decrease of the substrate temperature is not desirable since the AlGaAs layer grows well only when the substrate temperature is higher than 550 ^{o}C.

1.2 Complementary Devices

Many studies have been done on n-type MODFET devices [11,12,13,14,15]. However, in modern circuit designs, complementary devices are of great importance. Most published papers on GaAs complementary devices have considered devices prepared either by crystal re-growth or by ion implantation [16,17]. In this work, we describe the growth and fabrication of a complementary MODFET structure by MBE.

Molecular Beam Epitaxy (MBE) has good controllability of the crystal growth in the vertical direction, but selective growth across the wafer is difficult to achieve. One way to fabricate complementary GaAs devices is by a selective crystal re-growth technique. The growth and process steps become complicated in such re-growth technique. Since two epitaxial growth steps are required, the sample must be properly prepared twice during the process. After growth of the p-channel layers, the wafer must be removed from the MBE machine and windows are then defined by photolithography. In the window area the wafer is etched down to the buffer GaAs. The wafer is then re-loaded back to the machine and the n-channel structures are grown in the windows. However, it is very difficult to avoid some wafer contamination during all the external processing steps. This contamination can cause serious problems with the re-growth.

Another way to fabricate complementary GaAs devices is by means of selective ion implantation. By simply changing the impurity species for

the implantation, both n and p devices can be made on one wafer. After implantation, the dopant impurities must be activated by thermal annealing which can decrease the crystal damage caused by the implantation process. Self-alignment of the gate and source/drain contacts is easy to achieve by using the gate metal as the mask during ion implantation. The source and drain resistance can be reduced by the self-alignment technique which is also helpful in device process and performance. The basic geometry of a self aligned, ion-implanted device in figure 1.3 [16].

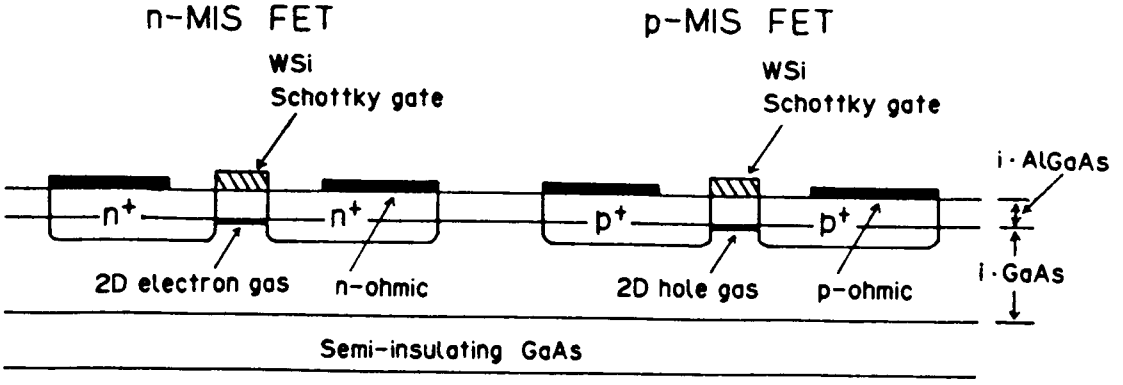

Figure 1.3 Complementary N-MISFET and P-MISFET.

Another approach, which is the one we have used, is to use a multi-layer structure by first growing a n-type MODFET, followed by an etching barrier, and finally, a p-type MODFET. By selectively etching away the p-MODFETs in some areas to access the underlying n-MODFET's, a complementary structure can be realized. This structure is relatively easy

to process and fabricate using facilities available at Oregon State University. Figure 2.1 shows the cross section of the structure.

This fabrication process is somewhat similar to that described by Kiehl and Gossard [18]. In that work, a n-GaAs/p-AlGaAs/i-GaAs structure was grown. The electrons were confined by the n-GaAs/p-AlGaAs junction for the n-type MESFET and the p-AlGaAs/i-GaAs layers acted as a p-MODFET.

2. Experimental Work

MODFETs were fabricated in the following sequence. First, material was grown by MBE for the desired structure. Second, the wafer was processed into actual devices; this involved a five mask level process : device isolation by mesa etch, metalization for ohmic contacts, gate recess and gate metalization, passivation and final bonding. Finally the devices were tested and all necessary device parameters like contact resistance and frequency response were measured.

2.1 Material Growth and Layer Structures

All samples studied were grown by MBE. An important advantage of MBE is that it can produce very abrupt interfaces between the AlGaAs and the GaAs layer. This reduces the effect of surface roughness scattering at the interface. Meanwhile, the growth rate of the sample can be controlled precisely and reproducibly. When the MBE system is in good condition, background impurity levels can be less than 1E15/cm^3. Thus, high quality material can be obtained.

The MBE system has three vacuum chambers : an introduction chamber, analysis chamber and growth chamber. The introduction chamber is used to transfer samples between atmosphere and the very high vacuum analysis chamber. The analysis chamber contains a heater for the sample outgassing and an Auger Spectrometer for surface analysis. The growth chamber contains seven source ovens : Al, In, Be, Si, As and

two Ga ovens, Reflection High Energy Electron Diffraction (RHEED), an optical pyrometer which can measure the substrate temperature during material growth and a Quadrupole Mass Spectrometer (QMS). The QMS is used to detect how many kinds of elements appear in the growth chamber as well as the quantity ratio of each element.

Five ovens were used during material growth. They contained Ga, Al, Si, As and Be. The Ga, Al and As provided material for the epi-layers while the Si and Be provided n-type and p-type impurities. The purity of all source materials is at least 99.9999 %. All source materials are thermally evaporated from boron nitride crucibles, and the flux rates are controlled by the crucible temperature.

The oven temperature to obtain a specific growth rate is calibrated by observations of RHEED oscillations [19]. During growth, the intensity of the RHEED diffraction spots oscillates with one period corresponding to the growth of one atomic monolayer. The RHEED pattern is displayed on a phosphor screen and the light signal at a particular spot on the screen is picked up by an optical fiber. At the end of the optical fiber is a photomultiplier, which converts the light signal into an electrical signal. This signal is then transmitted to the oscilloscope to displayed the spot intensity as a function of time. Thus from the time dependence of the intensity maxima we can count how many atomic monolayers were grown per second. All the calibration procedures are done on a specific wafer which is used for the growth rate calibration only. The device of the desired structure is grown on a different wafer. The gallium oven is heated to a temperature to provide a growth rate of 0.5 monolayer/sec.

The aluminum oven temperature is calibrated to have a 0.15 monolayer/sec growth rate. 23% Al concentration in the n-type MODFETs ($Al_{0.23}Ga_{0.77}As$) can be obtained by the combination growth rate of 0.15 monolayer/sec Al and 0.5 monolayer/sec Ga. During the later stages of growth the Al oven needs to be heated to a higher temperature in order to have 50% Al concentration in the p-type MODFETs ($Al_{0.5}Ga_{0.5}As$). The aluminum oven flux is calibrated again in order to determine the temperature necessary for a 0.5 monolayer/sec growth rate. For the growth of the actual device, the Al oven temperature is first set to provide the lower growth rate, then increased to provide the higher growth rate at the appropriate time. The material growth begins with the preparation of a suitable GaAs substrate wafer. It is a semi-insulating wafer grown by the method called Liquid Encapsulated Czochralski with <100> crystal orientation. The wafer was cleaned by the standard cleaning and etching procedure described by John Ebner [19] and loaded on a two inch solderless molybdenum holder. The sample was then introduced into the introduction chamber first. After pumping to high vacuum, the wafer was transferred to the analysis chamber, and heated to about 250 °C for 24 hours in order to desorb water. Surface analysis to determine impurity content was taken before and after the actual growth by Auger Electron Spectroscopy. The sample was transferred to the growth chamber for device growth. It was heated up to 585 °C by the substrate heater at which temperature the wafer began to desorb oxygen. After the wafer was free of oxide as determined by the RHEED pattern, the actual device was grown. First a 0.5 um undoped GaAs buffer layer at 580 °C was grown in order to

smooth the surface. Then a 10 nm undoped $Al_{0.23}Ga_{0.77}As$ was grown as the spacer layer. A silicon layer was deposited with the doping dose set at $4X10^{12}$ #/cm^2 calculated according to the previous Si doping calibration. Si deposition was done with all shutters closed except the arsenic and silicon. The shutter was opened for 2.4 minutes at the silicon atom flux rate $1.667X10^{12}$ #/cm^2 - minute, which gave the total doping dose of $4X10^{12}$ #/cm^2. This corresponds to 0.006 monolayer of Si. After doping, another 40 nm intrinsic $Al_{0.23}Ga_{0.77}As$ layer was grown and followed with a 20 nm n type GaAs cap doped with Si at $1X10^{18}$ #/cm^3. On top of the cap was deposited a 50 nm $Al_{0.5}Ga_{0.5}As$ which acts as the stop etching layer. On top of this stop etching layer, 150 nm undoped GaAs was grown as the buffer layer for the p-MODFET, 10 nm undoped $Al_{0.5}Ga_{0.5}As$ for the spacer, a Be doping plane at the dose of $4X10^{12}$ #/cm^2. 40 nm undoped $Al_{0.5}Ga_{0.5}As$ and 20 nm $1X10^{18}$ #/cm^3 p type cap to complete the device. Figure 2.1 shows the cross section of the proposed structure after device processing. The devices used in this thesis were processed by Terry McMahon.

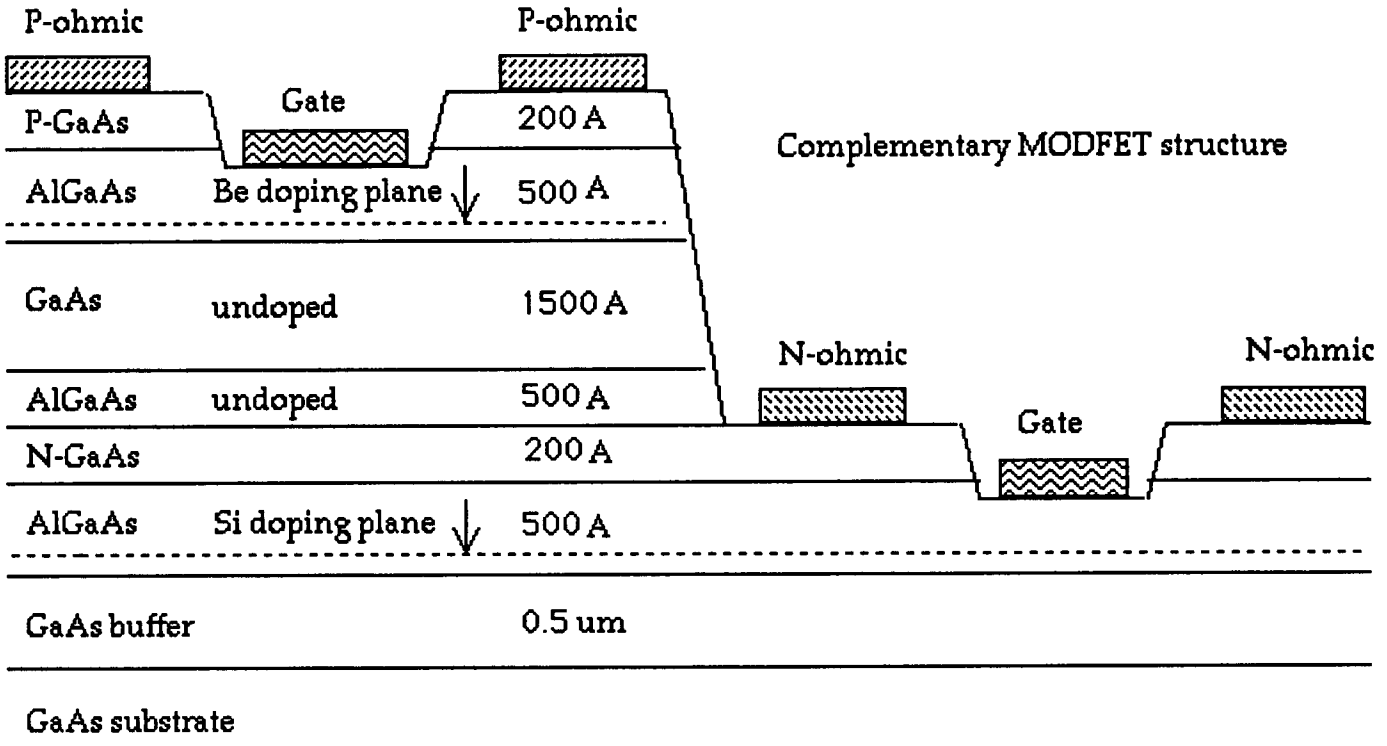

Figure 2.1 Cross section of the complementary MODFET structure

The reason for choosing 23% Al in the n-MODFETs is to avoid deep level traps in AlGaAs; 23% Al is about the composition for the onset of deep level traps [20]. These traps do not appear in p-type material, so we are able to use 50% Al in the p-MODFETs in order to have a larger valence band gap discontinuity.

The structure of this complementary device is a dual layer structure with the p-MODFETs on the top and the n-MODFETs at the bottom. In order to process the n-MODFETs, it is necessary to etch away all the top p-channel layers and stop at the cap of the n-channel device. It is important to stop the etching precisely at the n-MODFET cap layer. This is possible by putting a 50 nm $Al_{0.5}Ga_{0.5}As$ layer on top of the n channel cap layer. This 50 nm $Al_{0.5}Ga_{0.5}As$ layer is not etched by citric acid; however citric acid does etch the n-channel GaAs buffer layer. On the other hand, HF (24%) etches $Al_{0.5}Ga_{0.5}As$ but not GaAs. In this way either the AlGaAs or the GaAs can be removed depending on the etching solution.

2.2 Process Procedure

Both n type and p type MODFETs were fabricated from the epitaxial material described above. Wet etching was used to define individual devices and gate recess. A mesa etch is used for device isolation which prevents current flow from one device to another. It etches away about 1 um of material between the individual devices. The mesa etch is a uniform etching solution for all device layers with an etching rate of 250

nm per minute. The chemical composition of the mesa etch solution is $NH_4OH : H_2O_2 : H_2O$ (2 : 1 : 100).

A citric acid solution is used for selective etching. It is composed of ten parts citric acid to one part H_2O_2. Citric acid is a highly selective etching solution, which only etches GaAs but not $Al_{0.5}Ga_{0.5}As$. HF (24%), on the other hand, etches only $Al_{0.5}Ga_{0.5}As$ but not GaAs.

During the process of n-type MODFETs, it is necessary to etch all the upper p-channel layers. The etching process has to be highly selective so that it can be stopped on top of the n type cap layer. The complete etching procedure for n-MODFETs is given below.

Etch away p-channel layers in the following sequence of steps.

1. Soak in $NH_4OH : H_2O$ (1 : 3) for 10 seconds to remove oxide.
2. Mesa etch : $NH_4OH : H_2O_2 : H_2O$ (2 : 1 : 100) for 30 seconds.
3. Etch by Citric acid : H_2O (10 : 1) for 1 minute.
4. Etch by 24% HF solution for 20 seconds, rinse with DI water.

The sample is first mesa etched for 30 seconds. Roughly 120 nm top layer material is removed, leaving the surface in the p-channel GaAs buffer region. The following one minute citric acid etching removes all the GaAs buffer layer and stops on the $Al_{0.5}Ga_{0.5}As$ layer. Twenty seconds in dilute HF (24%) solution removes 50 nm $Al_{0.5}Ga_{0.5}As$ layer and stops on top of the n-channel cap layer.

Device isolation.

1. Spin photoresist at 5000 rpm for 30 seconds.
2. Soft bake 5 minutes at 85 °C and expose to UV light with integrated set at 9.5.
3. Develop and hard bake 5 minutes at 120 °C.
4. $NH_4OH : H_2O_2 : H_2O$ (2 : 1 : 100) for 60 seconds.

Ohmic contact deposition.

1. Standard clean and spin photoresist 5000 rpm for 60 seconds.
2. Soft bake 25 minutes at 85 °C and expose at setting 9.5 UV light.
3. Soak in chlorobenzene for 5 minutes, develop and soft bake 5 minutes at 85 °C.
4. Evaporate ohmic contacts : Ni 10 nm, AuGe 100 nm, Au 150 nm and then lift off with acetone as solvent for photoresist.
5. Anneal ohmic contacts in forming gas 5 minutes at 450 °C.

Gate recess and metalization.

1. Spin photoresist 5000 rpm for 30 seconds, and soft bake 25 minutes at 85 °C.
2. Expose to UV light , soak in chlorobenzene 5 minutes and develop wafer.
3. Soft bake 5 minutes at 85 °C and then gate recess etch by citric acid 30 seconds.
4. Evaporate gate metal : Ti 50 nm, Au 50 nm and then lift off with acetone.

Passivation

1. Deposit SiO_2 100 nm for passivation layer by PECVD.
2. Spin photoresist at 5000 rpm for 60 seconds, Soft bake 25 minutes at 85 °C and expose to UV light with integrated set at 9.5.
3. Develop wafer, hard bake 5 minutes at 120 °C and then etch by HF with 4.6% concentration solution for 10 seconds.

Bonding pads.

1. Spin photoresist at 5000 rpm for 60 seconds, Soft bake 5 minutes at 85 °C and expose to UV light with integrated set at 9.5.
2. Soak in Chlorobenzene for 5 minutes, develop and soft bake 5 minutes at 85 °C.
3. Evaporate bonding pad metal : Ti 50 nm, Au 200 nm and lift off with acetone.

The processing of the p-MODFET is very similar to the n-MODFET. The differences are ohmic contact compositions : Ti 10 nm, Au 50 nm, Zn 50 nm, Au 150 nm for n-MODFET and of course no pre-etching procedure is needed.

There is a crucial factor to mention, which is that the AlGaAs stop layer between the p and n devices has to be thick enough, ~ 50 nm, in order to stop etching by citric acid. If it is too thin, < 10 nm, the citric acid will penetrate this stop layer and etch away the n-MODFET cap layer. The n-MODFET can not be processed if this occurs.

2.3 Van der Pauw Hall Sample

The carrier mobility in the MODFETs is an important parameter related to device performance. Higher mobility leads to better device electrical performance. The MBE grown material studied here was characterized by Van der Pauw mobility measurements. Samples were cut into small squares (figure 2.2, approximately 5 mm square). The p-type contact alloy is composed of 10% Zn and 90% In, and the n-type alloy is 10% Sn and 90% In. Contacts are made using a very fine tip soldering gun in order to minimize contact area, and then annealed in a 450 ^{o}C oven with forming gas. This annealing process is required to obtained an ohmic contact instead of a Schottky contact. The annealing time is 4 minutes for the n-type sample and 3.5 minutes for p-type. The annealing time for p-type samples are critical because the structure of the device is a 2-layer structure. If the annealing time is too short, a poor ohmic contact results. However, if it is too long the Zn will diffuse into the n-channel region which decreases the channel mobility. After annealing several different samples at 2.5 minutes, 3 minutes, 3.5 minutes, 4 minutes and 4.5 minutes, the best annealing time for the p-channel samples was found to be 3.5 minutes based on the observation of the highest carrier mobility.

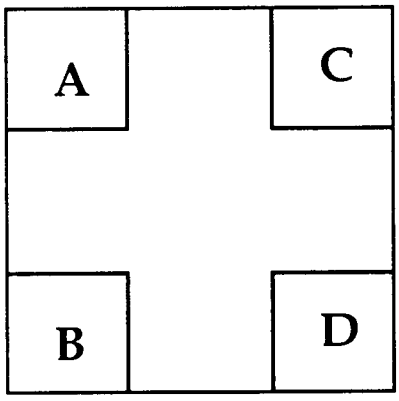

Figure 2.2 Van der Pauw Hall Sample

Some of the important formulas and the symbols are given below, which are used in the Van der Pauw analysis program [21]. The corresponding points A,B,C,D of the sample used in the formulas are shown above in Fig 2.2.

U_x : voltage at point x

I_{AB} : current flow through point AB

d : thickness of the film

B : magnetic field intensity

n : carrier density

q : 1.6E-19

μ : carrier mobility

R_H : hall coefficient

ρ : resistivity

$\Delta R_{AC,BD}$: average difference of R between no magnetic and applied magnetic field on the sample.

n is the carrier density which we want to know by measurement. $\Delta R_{AC,BD}$ is the average voltage difference when the magnetic field is applied.

$$R_{AB,CD} = \frac{U_D - U_C}{I_{AB}} \qquad R_{AC,BD} = \frac{U_D - U_B}{I_{AC}}$$

$$R_H = \frac{d}{B} \cdot \Delta R_{AC,BD} = \frac{1}{n \cdot q}$$

$$\mu = \frac{R_H}{\rho}$$

Van der Pauw measurements are typically performed at both 300K and 77K for the present work. By passing a small current through any two contacts, the voltage is measured at the other two contacts. By permuting the current contacts and the voltage contacts to average out contact variability, one can then determine the resistivity of the sample. It is necessary to have several sets of data by permuting the contacts. The possible non ideal effects such as ohmic contact resistance and the imperfect shape of the sample can be minimized by taking the average of the measured data. The mobility and carrier concentration are calculated from the film thickness and the Hall coefficient which can be determined by the effect of an applied external magnetic field on the voltage measurement.

As long as the sample is uniformly thick and the area of ohmic contacts on all four corners is small, the Van der Pauw method can determine the sheet resistivity and carrier mobility of any shaped sample.

3. Results

This section describes the experimental results obtained from our devices. The Van der Pauw Hall measurement gives carrier type, mobility and concentration. After processing into both n-MODFETs and p-MODFETs, device performance was then measured for DC I-V curve, transconductance, and saturation current versus gate bias and gate current versus gate bias.

3.1 Van der Pauw Mobility Data

Results of typical n and p hall sample measurements are listed below.

FILM THICKNESS (MICRON) ---------- 1.0

MAGNETIC FIELD (GAUSS) ---------- 3200

SAMPLE TYPE ---------- n

TEMPERATURE (K)	300	77
MOBILITY (CM^2/V-SEC)	6283	57190
DOPING LEVEL ($\#/CM^3$)	$1.17X10^{16}$	$1.24X10^{16}$
CARRIER DENSITY ($\#/CM^2$)	$1.17X10^{12}$	$1.24X10^{12}$
RESISTIVITY (Ohm-Cm)	$8.51X10^{-2}$	$8.81X10^{-2}$
CURRENT (mA)	0.1	0.5

FILM THICKNESS (MICRON) ---------- 1.0

MAGNETIC FIELD (GAUSS) ---------- 3200

SAMPLE TYPE ---------- p

TEMPERATURE (K)	300	77
MOBILITY (CM^2/V-SEC)	113	1411
DOPING LEVEL (#/CM^3)	$5.28X10^{16}$	$2.34X10^{16}$
CARRIER DENSITY (#/CM^2)	$5.28X10^{12}$	$2.34X10^{12}$
RESISTIVITY (Ohm-Cm)	$8.77X10^{-1}$	$1.89X10^{-1}$
CURRENT (mA)	0.01	0.01

It should be noted that the carrier density of the p-type sample decreases dramatically from 300K to 77K. The reason for such an effect is most likely that the room temperature measurements include conductivity for both the two dimensional carrier channel and the parasitic AlGaAs layer. The mobility and conductivity in the parasitic AlGaAs layer is close to that in the carrier channel, so the room temperature measurement combines the effect of both conductance. At 77K this effect will be suppressed by the mobility enhancement in the channel. The mobility in the channel is about 10 to 20 times higher than that in the parasitic AlGaAs layer at 77K. The parasitic effect is then negligible. For all calculation and computer simulations involving the carrier density, we use the data obtained at 77K.

3.2 Device Testing

After both n and p devices were fabricated, DC I-V curves were then taken using a HP 4145B analyzer. All the measurements were taken at room temperature. Gate width of all the devices was 75 um. The spacing between gate to drain and gate to source was 5 um in all devices. Figure 3.1 shows the DC characteristic result of a 2.5 um gate length p-type MODFET. The sources was grounded and drain voltage varied from 0 volt to -5 volt. By decreasing gate voltage 0.2 volt each step with the initial gate voltage set at 1.2 volt, a family of DC I-V curves was measured. The bottom curve corresponds to a gate voltage of 1.2 volt. The upper most curve corresponds to a gate voltage of 0 volt. From the data, it is clear that the cut off voltage was at 1.2 volt. Figure 3.2 is the result of a 5 um gate length p-MODFET with gate voltage varied 0.4 volt each step. The bottom curve was taken at 1.2 volt gate voltage, and upper curve at -0.4 gate voltage. Comparing the data in Fig 3.2 with that in Fig 3.1, it is evident that at same bias gate voltage the current is smaller with the longer gate length device as we expected. Figure 3.3 and 3.4 show the results of a 2.5 um gate length n-MODFET and a 5 um gate length n-MODFET respectively. The bottom curve in both figures were taken at -1 volt gate voltage, and 0 volt gate voltage for the most uppermost curve.

Figure 3.5 and figure 3.6 are device transconductance of a 2.5 um gate length p-MODFET and a 2.5 um gate length n-MODFET. Maximum peak transconductance after normalized gate width is 70 ms/mm for the n device, and 5.5 ms/mm for the p device. Once transconductance reaches

the maximum, further gate bias will decrease the transconductance due to the increasing effect of parasitic conductance. The set up of the n-MODFET is that the source was grounded and drain voltage was set at 5 volt, so the device was operated at saturation region for the practical circuit operation purpose. For the p-MODFET, drain was set up at -3 volt and source was grounded. Transconductance in the p device is much smaller than in the n device because the mobility of electrons is much larger than the mobility of holes.

Figure 3.7 is drain to source current and gate current versus gate voltage of the 5 um gate length p-MODFET. Drain voltage was set at -3 volts, and the source was connected to ground. Figure 3.8 shows the drain to source current and gate current versus gate voltages of the 5 um gate length n device. We can notice the drain current saturates when gate voltage is higher than 1.5 V in figure 3.8. In chapter 4 we will simulate this saturation current and explain the phenomenon. We also tested the n-MODFET frequency response using an HP network analyzer 8510. The n-MODFET is connected in the common source configuration with standard 50 ohms loading at the drain. The unit power gain frequency is 5 GHz and 3 GHz for 3 dB corner frequency.

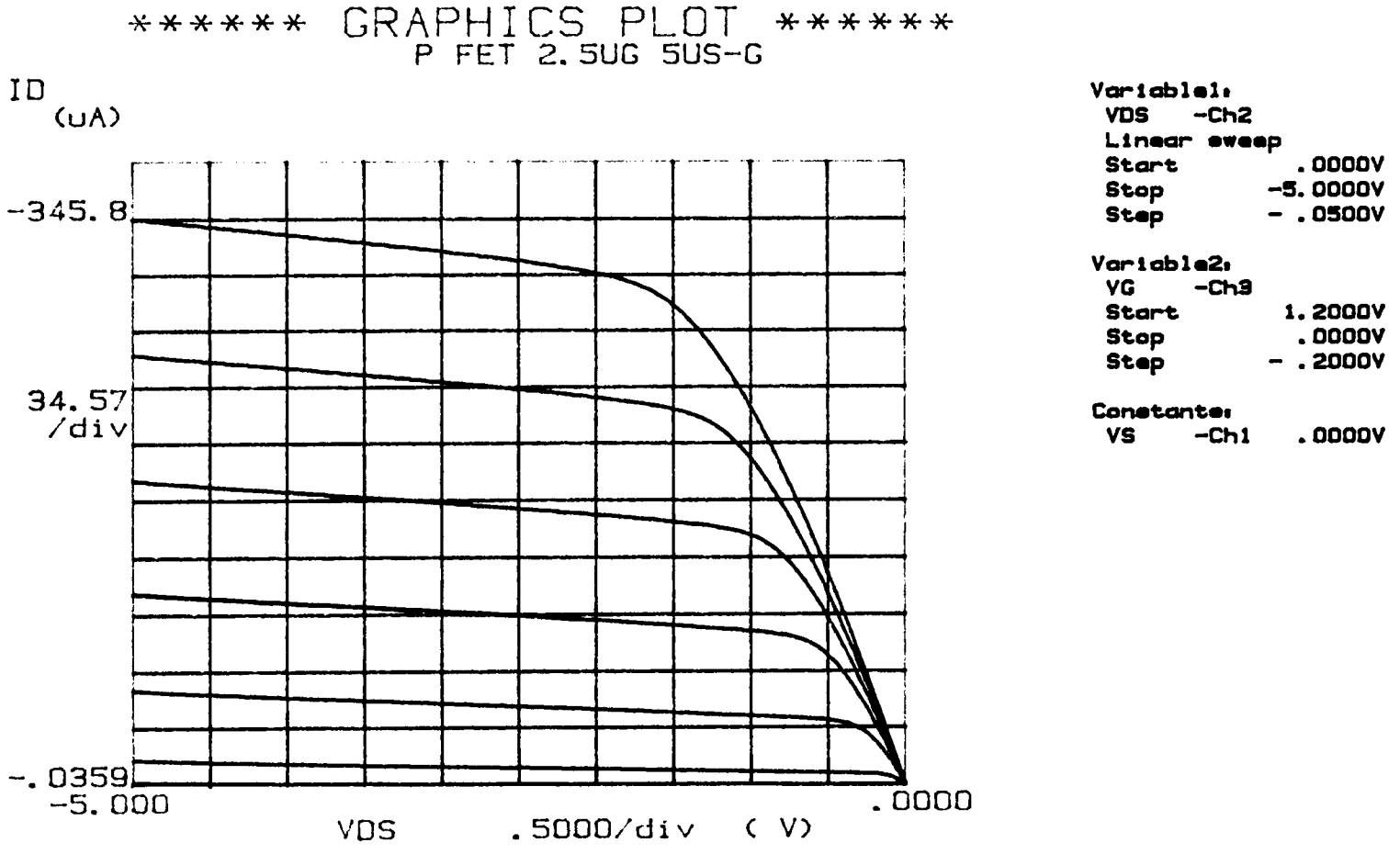

Figure 3.1 I-V curve of a 2.5 um gate length p-MODFET

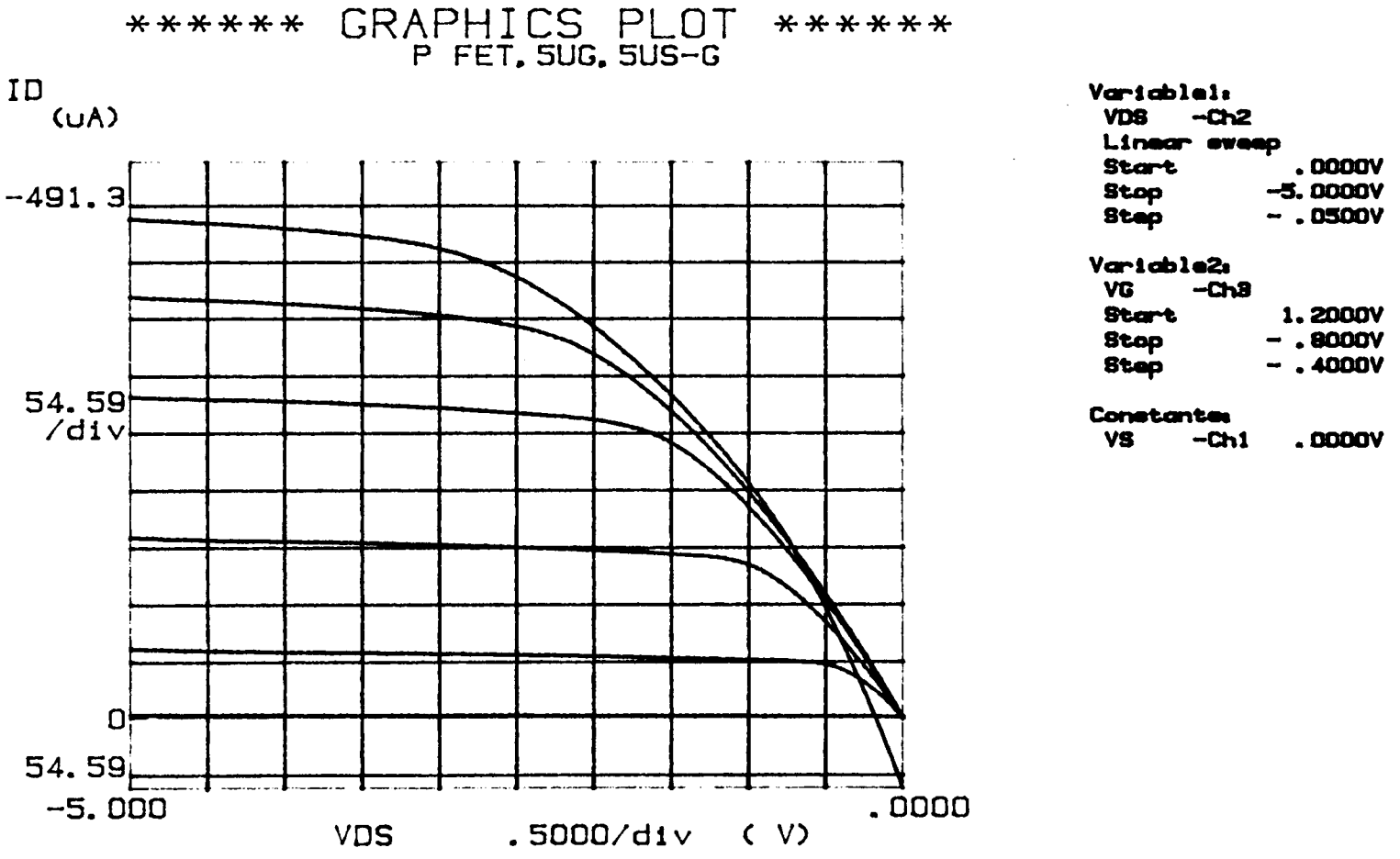

Figure 3.2 I-V curve of a 5 um gate length p-MODFET

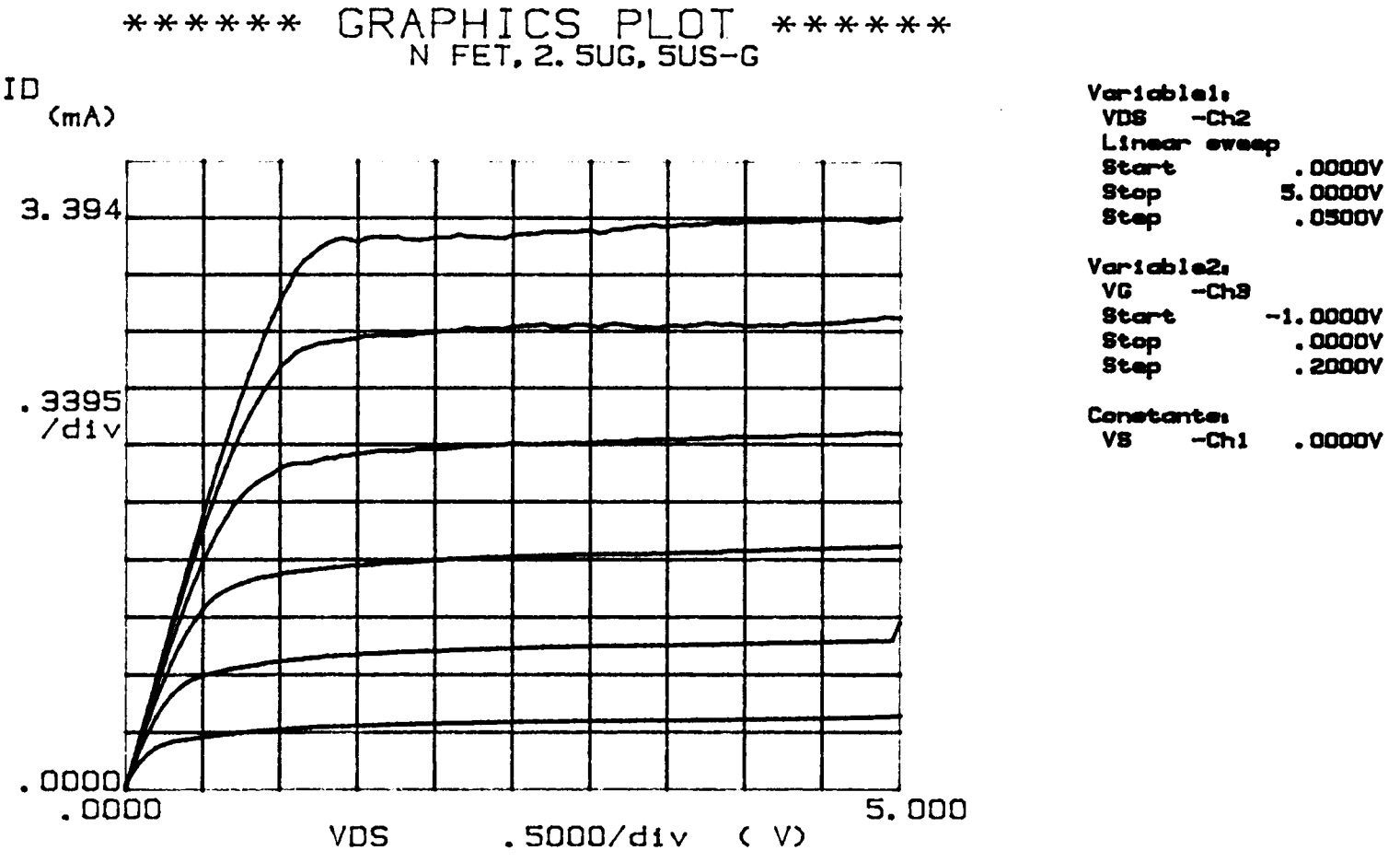

Figure 3.3 I-V curve of a 2.5 um gate length n-MODFET

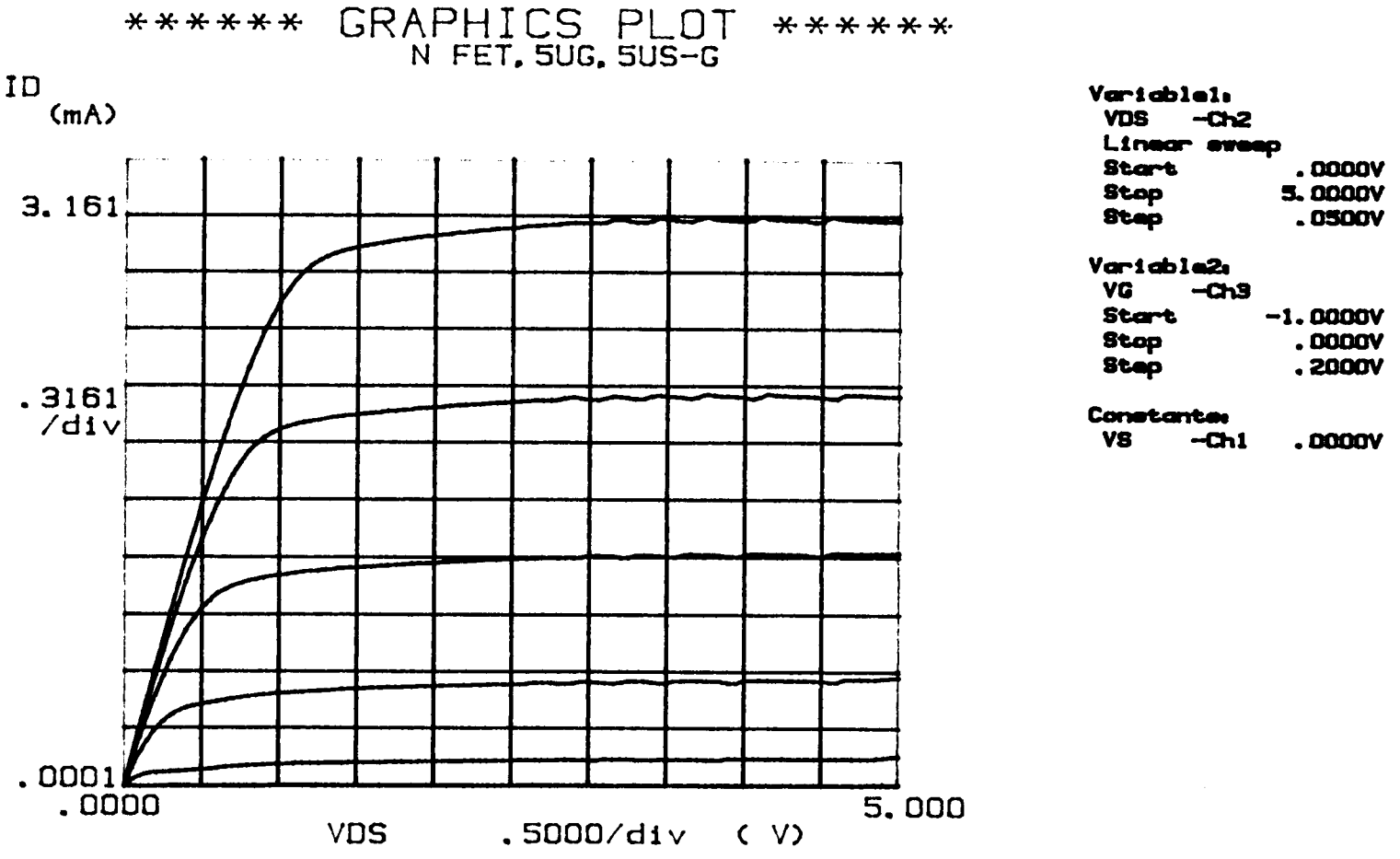

Figure 3.4 I-V curve of a 5 um gate length n-MODFET

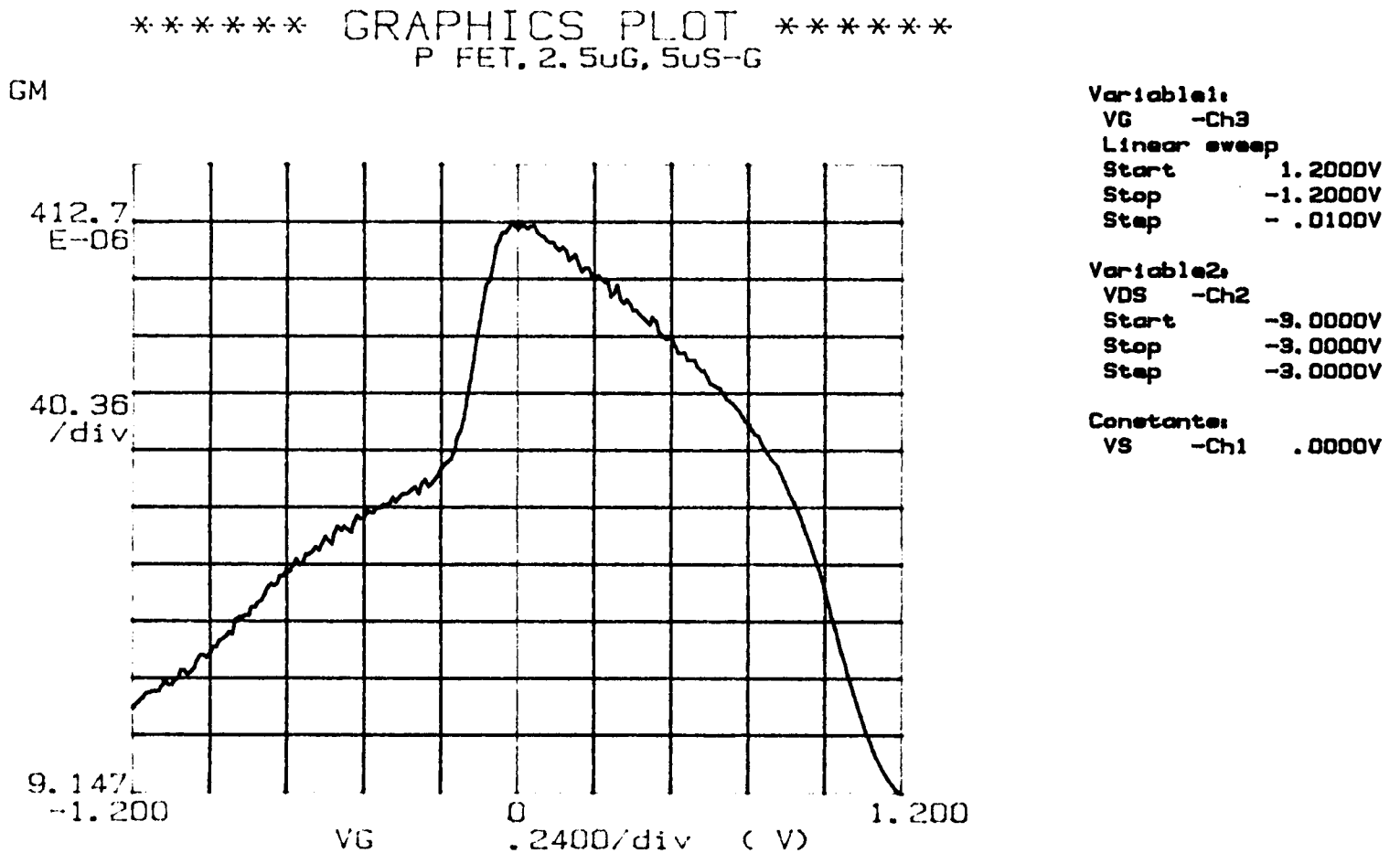

Figure 3.5 Measurement of the transconductance of the 2.5 um gate length p-MODFET

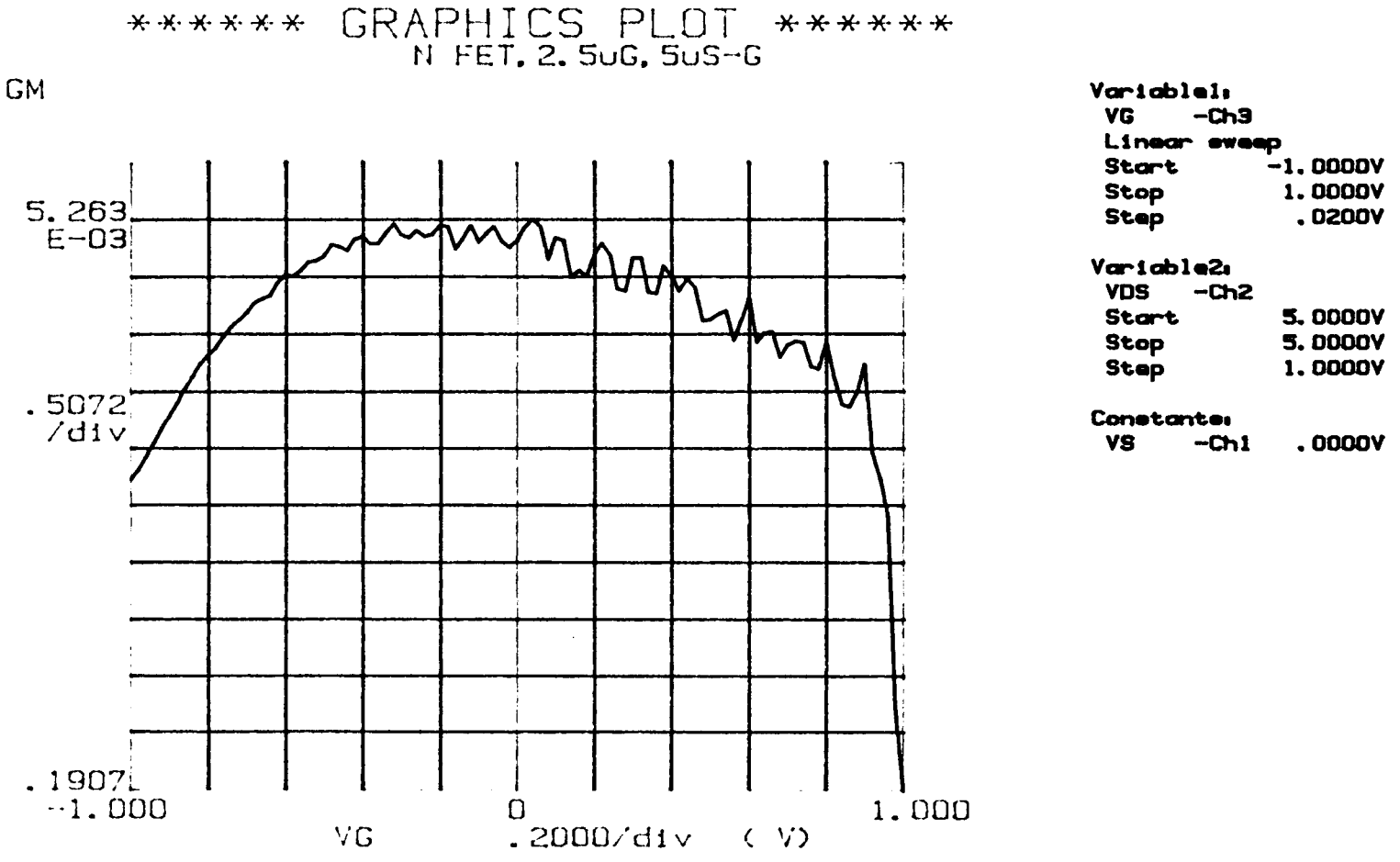

Figure 3.6 Measurement of the transconductance of the 2.5 um gate length n-MODFET

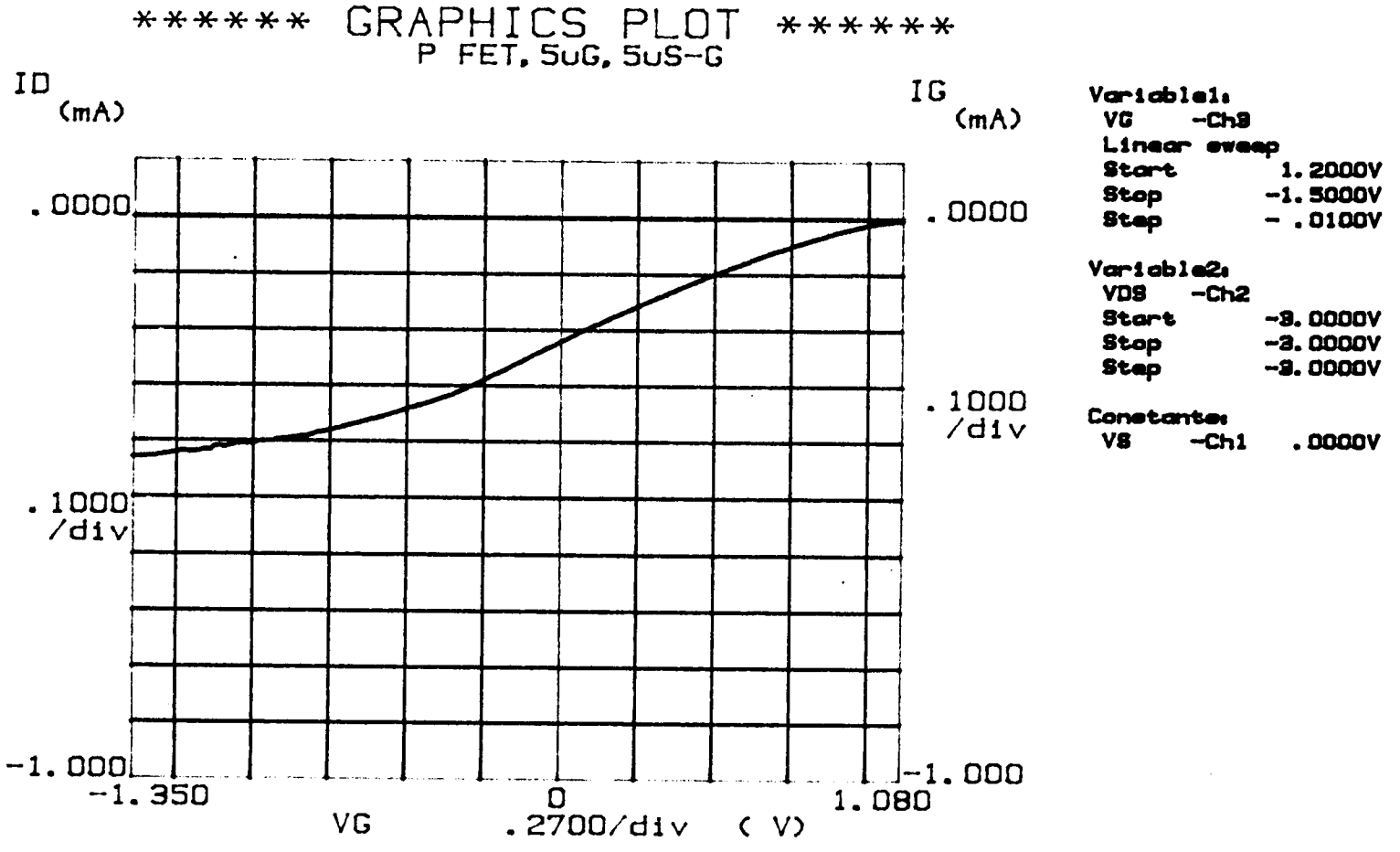

Figure 3.7 Gate current and I_{ds} current versus gate bias of the 5 um gate length p-MODFET

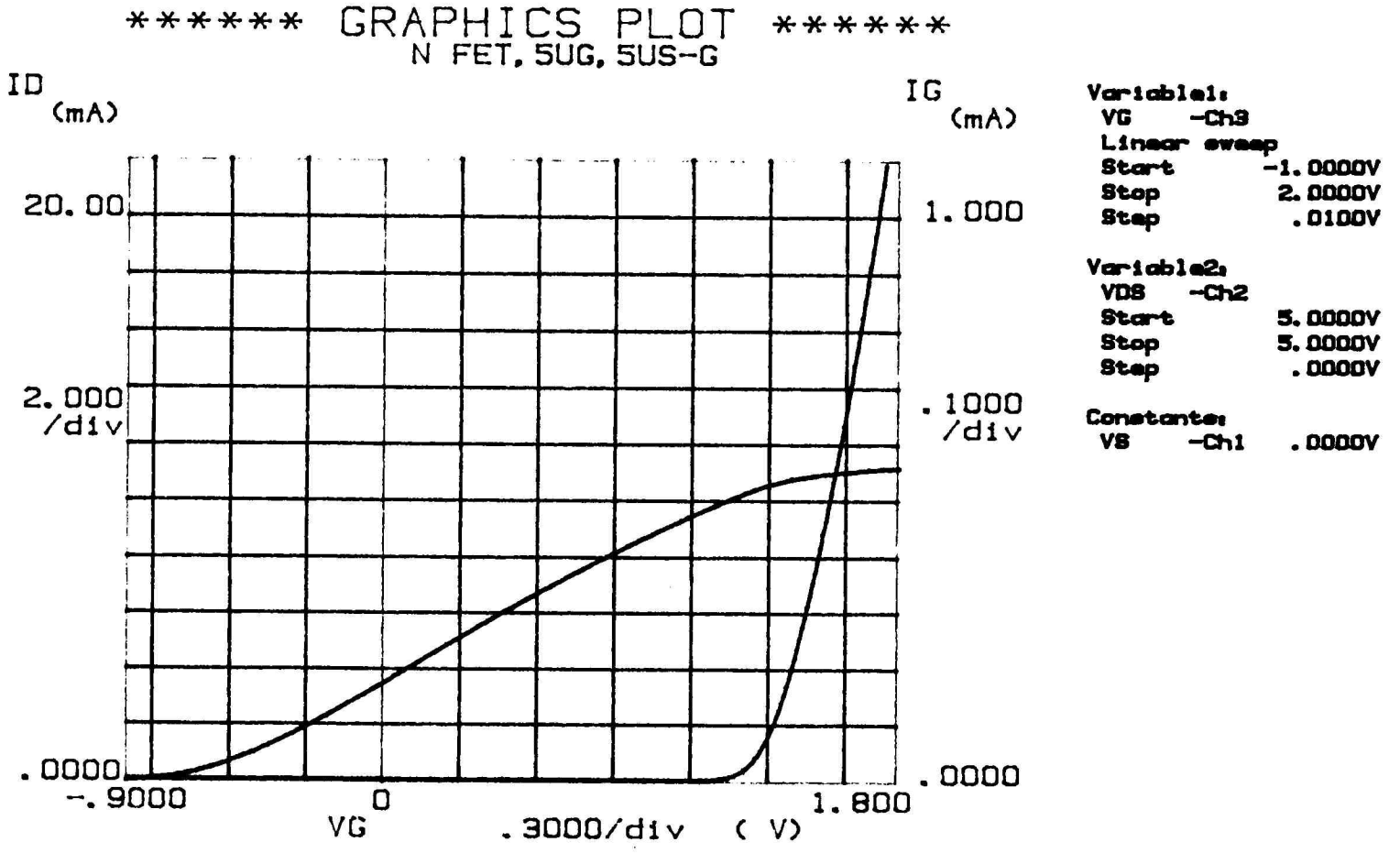

Figure 3.8 Gate current and I_{ds} current versus gate bias of the 5 um gate length n-MODFET

4. A Simple Model of The Device

In this section we develop a simple model to simulate the I-V response of a MODFET. This model considers both the parallel conduction current in the AlGaAs layer and the current in the two dimensional electron gas (2DEG). The simulation results give qualitative agreement with the experimental results.

4.1 Charge Control Model

All the processed devices are planar doped. It is assumed that all donors or acceptors are totally ionized. A simple charge control model is used from which the induced carrier density and the threshold voltage in terms of gate voltage, doping level and other device parameters is derived. By applying Gauss law, the electric field can be calculated. The electric potential distribution can be derived from the electric field intensity and Poisson's equation. The carrier density can then be related to the potential and the doping level (Eq. 2). The electric potential can also be written in terms of gate voltage, Schottky barrier height and energy band discontinuity (Eq. 1). From Eqs 1 and 2, the device cut off voltage and channel carrier density can be obtained.

Below is a list all the symbols used in the diagrams and equations :

d : thickness of AlGaAs from doping plane to gate contact surface.

d_i : thickness of spacer layer.

ϕ_m : potential barrier height of metal semiconductor interface.

V_g : applied gate voltage.

ΔE_c : conduction band discontinuity at AlGaAs GaAs interface.

$E_f(n)$: Fermi energy measured at the heterojunction interface; n is the carrier density.

E : electric field intensity.

Q : total charge enclosed by Gauss surface.

V_t : device cut off voltage.

C : gate capacitance.

μ_n : electron mobility in the channel.

n_{2d} : two dimensional carrier density.

N_{2d} : net positive charge on the doping plane.

The energy band diagram is shown in fig 4.1 below.

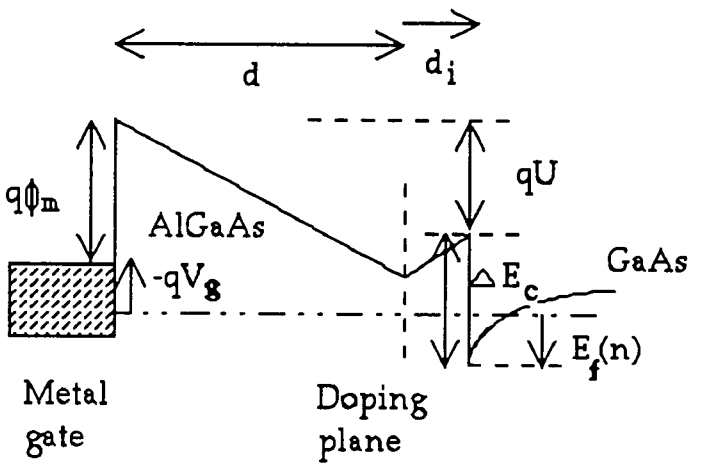

Figure 4.1 Conduction band diagram

From the figure it is clear that

$$U = (\phi_m - V_g) - \frac{\Delta E_c - E_f(n)}{q} \qquad (1)$$

The Fermi energy, $E_f(n)$, is measured as the energy difference from conduction band to the Fermi energy at the interface.

From Gauss law

$$\int_S E \cdot ds = \frac{Q}{\varepsilon_s}$$

where E is the electric field and Q is the total electric charge in the volume bounded by S. ε_s is the dielectric constant in the AlGaAs material here. One can obtain the electric field intensity in the device by taking the surface integral over a cylinder of unit cross section area as shown below.

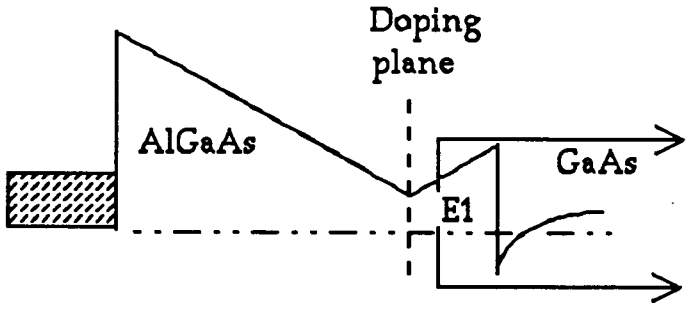

Figure 4.2 Domain for the electric field calculation

We obtain

$$E_1 = \frac{q \cdot n_{2d}}{\varepsilon_s}$$

by the following argument. E_1 is the electric field intensity normal to the unit area face of the cylinder shown above, which extends to the right hand side to infinity. n_{2d} is the carrier density in the quantum well, and ε_s is the dielectric constant in AlGaAs. When the cylinder is chosen for surface integration, the only integration contribution is from the face of the cylinder over which the electric field is perpendicular to the surface. The total charge enclosed in the cylinder comes from the 2DEG, which does not depend on the location of the cylinder face. This implies that the electric field is a constant between the doping plane and the interface.

We now integrate the Poisson equation twice to solve for the electrical potential difference U in figure 4.1. The charge distribution between the gate and the AlGaAs/GaAs interface is assumed to be a delta plane of net doping level N_{2d}. We choose the origin at the interface. The coordinate of the doping plane is then $x = -d_i$, and the gate metal coordinate is $x = -(d+d_i)$, i.e.

$N(x) = N_{2d}$ at $x = -d_i$

$N(x) = 0$ elsewhere

The Poisson equation is, for a positive charged donor, N(x),

$$\frac{d^2V(x)}{dx^2} = \frac{q \cdot N(x)}{\varepsilon_s}$$

Integrating once from 0 to x.

$$\int_0^x \frac{d^2V(x)}{dx^2}\,dx = \frac{q}{\varepsilon_s}\int_0^x N(x)\delta(x+d_l)\,dx$$

$$\frac{dV(x)}{dx} - \frac{dV(0)}{dx} = \frac{q}{\varepsilon_s}\int_0^x N(x)\delta(x+d_l)\,dx \qquad \text{where } -\frac{dV(0)}{dx} = E1$$

The boundary condition is that the electric field is E1 at x=0. Integrating both side of the equation again from 0 to -(d+d_i).

$$\int_0^{-d-d_i} \frac{dV(x)}{dx}\,dx + \int_0^{-d-d_i} E1\,dx = \frac{q}{\varepsilon_s}\int_0^{-d-d_i} dx \int_0^{\infty} N(x')\delta(x'+d_l)\,dx'$$

$$V(-d-d_l) - V(0) = -U = E1\cdot(d+d_l) + \frac{q}{\varepsilon_s}\int_0^{-d-d_i} N(x')\theta(x'+d_l)\,dx$$

where $\delta(x)$ is the delta function and $\theta(x'+d_i)$ is a step function defined as follows :

$$\theta(x'+d_i) = \begin{cases} 1 & x' <= -d_i \\ 0 & x' > -d_i \end{cases}$$

Simplifying

$$-U = E1\,(d+d_i) + q\,(-d)\,N_{2d} / \varepsilon_s$$

or

$$U = \frac{q\cdot(N_{2d}-n_{2d})}{\varepsilon_s}\cdot d - \frac{q\cdot n_{2d}}{\varepsilon_s}\cdot d_i \qquad (2)$$

Then equating equations (1) and (2),

$$\phi_m - V_g - \frac{\Delta E_c - E_f(n)}{q} = \frac{q\,(N_{2d}-n_{2d})}{\varepsilon_s} d - \frac{q\,n_{2d}}{\varepsilon_s} d_i ;$$

and solving for n_{2d}

$$n_{2d} = \frac{\varepsilon_s}{q\,(d+d_i)}\left(V_g - \phi_m + \frac{\Delta E_c - E_f(n)}{q} + \frac{q\,N_{2d}\,d}{\varepsilon_s} \right)$$

For carrier densities between $5X10^{11}$ #/cm^2 and $1.5X10^{12}$ #/cm^2, the Fermi energy can be approximated by a fairly accurate analytical approximation to the exact computer solution as shown in Ref. [11]

$$\frac{E_f(n)}{q} = a \cdot n_{2d}, \text{ where } a = 1.25E{-}17 (v/m^2) \text{ at } 300K.$$

Substituting this equation in the above n_{2d} equation and simplifying, we obtain the following linear relationship :

$$n_{2d} = \frac{1}{a + \frac{q(d+d_i)}{\varepsilon_s}} \left(V_g - \phi_m + \frac{\Delta E_c}{q} + \frac{q N_{2d} d}{\varepsilon_s} \right) \tag{3}$$

If we let Schottky barrier height equal to 1 volt, the conduction band discontinuity 0.172 volt, d=400 Å, d_i=100 Å, and N_{2d}=4X10^{12} #/cm^2, we obtain the following numerical expression,

n_{2d} = 1.18E16 (V_g + 1.5) #/m^2.

This equation predicts the channel carrier density is linearly proportional to the gate voltage. Fig 4.9 shows a calculation of the total carrier density versus gate voltage using a more exact computer program, which clearly shows a linear relation between carrier density and gate voltage. The software package used to obtain Fig. 4.9 will be discussed in more detail later in section 4.2.

The threshold voltage V_t is defined as the gate voltage at which n_{2d} equals zero, and thus

$$V_t = \phi_m - \frac{\Delta E_c - E_f(n)}{q} - \frac{q \cdot N_{2d} \cdot d}{\varepsilon_s}$$

The first term in Eq. (3) has units of capacitance. Thus

$$q n_{2d} = C (V_g - V_t), \qquad \text{where } C = \frac{q}{a + \frac{q(d+d_i)}{\varepsilon_s}} \tag{4}$$

For a uniform doped MODFET with an impurity doping density N_{3d}, Delagebeaudeuf and Linh [12] have obtained a similar expression except for a minor difference of the last term, i.e.

$$V_t = \phi_m - \frac{\Delta E_c - E_f(n)}{q} - \frac{q\, d^2\, N_{2d}}{2\, \varepsilon_s}$$

For the p-MODFETs, one obtains similar expressions

$$p_{2d} = C \cdot (V_{off} - V_g)$$

$$V_t = \frac{\Delta E_v - E_f(p)}{q} - \phi_m + \frac{q\, N_{2d}\, d}{\varepsilon_s}$$

p_{2d} : 2 dimensional hole density.

4.2 Device I-V curve

The equivalent circuit of our device model is shown in fig 4.3. This includes both the conduction channel in the GaAs and the parasitic channel in the AlGaAs and includes the effect of the resistance between the gate to source and gate to drain. Both the pinch off and velocity saturation limits are considered. Pinch off occurs when the conducting channel becomes completely depleted by the gate voltage, thus conduction becomes limited. Velocity saturation occurs when the carrier drift velocity in the material reaches its maximum value, thus limiting the source to drain current. A current-voltage relation is derived for the pinch off mechanism. For the velocity saturation mechanism, a current-voltage equation given by M. Shur is used [22].

Two assumptions are used in this model. We first assume that below a certain gate voltage the parasitic channel is empty of carriers, and at higher gate voltages this parasitic channel conducts. The induced carrier density is a function of gate voltage, so the resistance under the gate is also a function of gate voltage. Figures 4.4 to figure 4.8 are calculations of the n-MODFETs conduction band and carrier density profiles in the device vertical direction. These are the results obtained from a program developed at the University of York by Professor John Wood and colleagues, which iteratively solves Poisson's equation and the Schrodinger equation until convergence is obtained. The output gives the electron density distribution, quantized energy levels and conduction band energy profile. In these simulations the gate voltage is varied : -0.7, -0.3, 0, 0.3 and 0.8 volts. The carrier density in the channel is : $5.2X10^{17}$, $6.3X10^{17}$, $6.8X10^{17}$, $7.1X10^{17}$ and $7.5X10^{17}$ per cm^3 respectively. The carrier density in AlGaAs increases from $4X10^{16}$ per cm^3 at gate bias -0.7 to $3.5X10^{17}$ per cm^3 at gate bias 0.8. Clearly, the number of carriers in the AlGaAs is large enough to affect the current in the device; hence it is necessary to include the effect of parallel conduction in any model. While it is not realistic to assume that parallel conduction begins abruptly at a certain gate voltage, the concentration of carriers in the AlGaAs channel increases so rapidly with gate bias that in fact parallel conduction only becomes significant in a narrow range of gate voltages. Fig 4.9 shows the total induced carriers in both the AlGaAs and the channel versus gate bias. The slope of the curve corresponds to the capacitance. The capacitance is a constant when the gate voltage is between -0.4V and 0.4V, and is

calculated to be $4.8X10^{-8}$ F for figure 4.9. The value from our Eq. (4) gives 2.1E-7 F. It is assumed that the parasitic effect becomes important when the slope changes, which occurs at about 0.4 volt. At this point the capacitance begins to increase as charge accumulates in the AlGaAs. Therefore, the parasitic capacitance will only be included after the gate voltage is larger than 0.4 volt. For p-MODFETs, this gate voltage is determined by the transconductance measurement. It is believed that the parasitic effect becomes important after the gate voltage reaches peak transconductance, which is zero volts from the measurement data (Fig. 3.5).

The second assumption is that the maximum carrier density in the device is no greater than the impurity doping density. If all the dopant are ionized, further bias of the gate can not induce more carriers [23].

The source to gate resistance is also calculated in this model. Impurities in the 5 um open region between gate and source, and between gate to drain is assumed to be totally ionized. With the above two assumptions, the current-voltage relationship can be derived as follow. First we list all symbols and parameters used in the model.

W : channel width; 75 um.

R_s' : resistance between gate to source in open region.

R_d' : resistance between gate to drain in open region.

R_s : total resistance between gate to source which includes ohmic contact resistance.

R_d : total resistance between gate to drain which includes

ohmic contact resistance.

Id : source to drain current.

L : gate length.

L': gate to source distance, 5 um.

n_{3d} : 3 dimension electron density.

n_{2d} : 2 dimension electron density.

Δd : 7 nm, 2DEG separation distance to interface.

$\upsilon(x)$: electron velocity along the channel.

E(x) : electric field along channel.

Q(x) : carrier density along channel.

V(x) : voltage at position x along the channel.

V_g' : $V_g - V_{off}$.

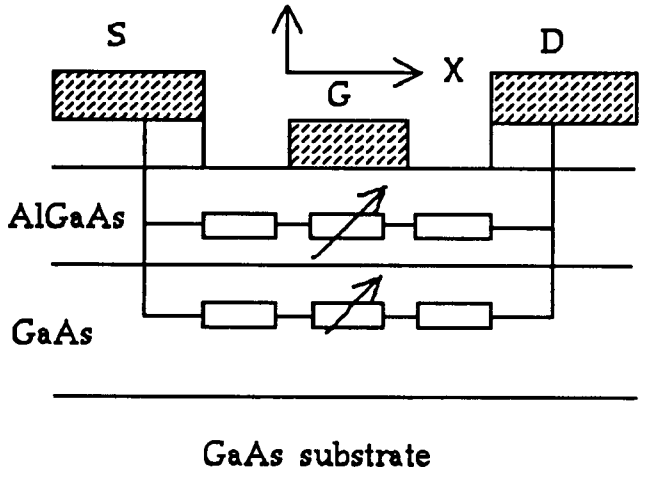

Figure 4.3 Device current voltage model

The resistance between gate to source is calculated first.

$$R_s' = \rho \cdot \frac{L'}{A} = \frac{L'}{q \cdot \mu_n \cdot n_{3d} \cdot W(d+d_i+70A)} = \frac{L'}{q \cdot \mu_n \cdot n_{2d} \cdot W}$$

By substituting appropriate values into above equation, 5 um L', 75 um for W, 6283 cm^2/V-sec for mobility, $4X10^{12}$ #/cm^2 for n_{2d}, the source to gate channel resistance can be obtained about 50 ohms. With the same equation, we can also calculate the open area resistance in the parasitic channel, which is about 40 ohms.

The 2DEG density, assuming the gradual channel approximation , depends on the gate voltage, V_g, and the potential, V(x), in the 2DEG channel according to following equation in the linear region :

$$Q(x) = \frac{\varepsilon_s}{(d+\Delta d)} \cdot (V_g - V_{off} - \upsilon(x)) \quad \text{or } Q(x) = C \cdot (V_g' - V(x))$$

Since the source to drain current is the same at all positions under the gate, it can be expressed as the product of charge density and velocity, i.e.

$$I_d = I(x) = W \cdot Q(x) \cdot \upsilon(x) \; ; \qquad (5)$$

we then integrate over the gate length from zero to L. The right hand side of the equation is integrated from the effective gate voltage near the source side of the gate to the effective gate voltage near the drain side of the gate. Rs is the total resistance from gate to source which includes ohmic contact resistance. Substituting the relation that the electron velocity is equal to the mobility times electrical field into Eq (5),

$$\upsilon(x) = \mu_n \cdot \frac{dV(x)}{dx}$$

we then have

$$\int_0^L I_d \, dx = \mu_n W C \int_{IR_s}^{V_d - IR_s} [V_g' - V(x)] \, d(V(x))$$

or

$$I_d \cdot L = \mu_n WC\left[V_g'(V_d - I_d r) - \frac{(V_d - I_d R_d)^2 - I_d^2 R_s^2}{2}\right]$$

Assuming that $R_s = R_d$ and letting r = Rs + Rd, we obtain an expression for the drain current.

$$I_d = \frac{V_d\left(V_g' - \frac{V_d}{2}\right)}{\frac{L}{\mu_n WC} + r\left(V_g' - \frac{V_d}{2}\right)} \tag{4}$$

This is the current-voltage relationship when saturation is due to pinch off. If r=0, the equation is identical to that derived from the two-piece model [24]. I_d saturates when Vg' equals to $V_d(L)$, where $V_d(L)$ is the effective voltage at the channel at x=L. L is the gate length.

Thus when $U_d(L) \geq U_g' + I_d R_s$, pinch off occurs, and the current saturates. The above current-voltage relation is true in both the GaAs channel and the parasitic AlGaAs layer. In the simulation program, currents in the channel and in the parasitic layer are calculated separately. The total current is the sum of these two currents.

It is also possible for current saturation to take place by a velocity saturation mechanism. In this case the saturation current can be expressed as shown by Shur [22].

$$I_d = \beta v_o^2 \frac{\sqrt{1+2\beta R_s U_g' + (U_g'/v_o)^2} - \beta R_s U_g' - 1}{1 - (\beta R_s v_o)^2}$$

$$\beta = \frac{\varepsilon_s \mu_n W}{(d+\Delta d)\ L}\ ,\ v_0 = F_s L,\quad F_s = 1E7\ (V/M)$$

where F_S is the electric field intensity which cause the electron velocity saturation and L is the gate length. All other parameters are defined same as previous.

The induced carriers in AlGaAs layer are considered to be significant after a gate bias larger than 0.4 volt in n-MODFETs. It is assumed that all the voltage drop is on the channel if the gate bias voltage is smaller than 0.4 volt. After 0.4 volt bias on the gate, we assumed the voltage drop is applied on the AlGaAs layer. Therefore, the effective gate bias on the n-MODFET AlGaAs is :

$V_{eff} = V_g - 0.4$

and the induced charge in the AlGaAs is :

$$Q = \frac{\varepsilon_s}{d_1} \cdot V_{eff}$$

where d_1 is the distance from the gate to the doping plane. This carrier density will also saturate because the total induced carrier density can not exceed impurity doping density.

The value for the parasitic turn-on voltage for the p-MODFETs is chosen at zero volt, which is based on the measurements of transconductance in actual devices. After the gate bias becomes smaller

than 0 volt in p-MODFETs, the transconductance drops very abruptly. It is because that the parasitic effect reduces the transconductance [25].

A computer program based in this model was written to simulate the current-voltage relation (Appendix 1). Currents in the channel and in the parasitic layer are calculated separately, and the drain to source current is the sum of these two currents. Equation (4) describes the transistor I-V curve in the linear region. The current value of the saturation region is determined by either pinch off or the velocity saturation mechanism. Using a constant gate bias, the computer program calculates two maximum saturation currents using both mechanisms. These two values are then compared and the model yielding the smallest saturation current is chosen as the dominant saturation mechanism. Figure 4.10 is the result calculated for a velocity saturation mechanism, and figure 4.11 is calculated for a pinch off mechanism. It is clear that the velocity saturation mechanism is the limiting factor.

The velocity saturation mechanism applies primarily to short channel devices, e.g. sub-micron devices in silicon. At a given gate bias, as the gate length decreases the corresponding field along the channel increases. Due to the large electric fields present in short channel devices, velocity saturation tends to be the limiting mechanism. In our devices, the high mobility makes it easier for the electrons to reach the saturation velocity. Both our 2.5 um and 5 um n-MODFETs are limited by velocity saturation. However, the mobility in the p-MODFET channel and parasitic layer is much lower than that in the n-MODFET channel. Thus our

simulations for p-MODFETs and parasitic layer are based on the pinch off model.

During the simulations, the value of the contact resistance in n-MODFETs and p-MODFETs are chosen by curve fitting. We list the values below : 60 ohm-mm for p-type ohmic contact resistance, 9.35 ohm-mm for 2.5 um gate length n-type ohmic contact resistance, and 3.74 ohm-mm for 5 um gate length n-type ohmic contact resistance. Two different ohmic contact values of the n-MODFETs indicates the process of forming ohmic contacts is not reproducible. The mobility in the p-MODFET channel and the parasitic AlGaAs layer are also chosen by curve fitting. The values are : 6283 cm^2/V-sec for n-MODFET channel, 3500 cm^2/V-sec for n-MODFET parasitic layer, 220 cm^2/V-sec for p-MODFET channel and 120 cm^2/V-sec for p-MODFET parasitic layer. Figure 4.12 is the simulation result of a 5 um gate length n-MODFET. Figures 4.13 and 4.14 are simulations for 2.5 um gate length and 5 um gate length p-MODFETs respectively. Figures 4.15 and 4.16 are saturation currents versus gate bias voltage of a 5 um gate length n-MODFET and a 5 um gate length p-MODFET. In order to compare the simulation results and the measured data, we list the results in table 4.1 and 4.2.

	2.5 um gate			5 um gate	
	measured	simulated		measured	simulated
V_g	I_{ds} (V_{ds}=5)	I_{ds}	V_g	I_{ds} (V_{ds}=5)	I_{ds}
-1	0.42 ma	0.33 ma	-1		
-0.8	0.88 ma	0.9 ma	-0.8	0.1 ma	0.26 ma
-0.6	1.4 ma	1.5 ma	-0.6	0.5 ma	0.8 ma
-0.4	2.1 ma	2.2 ma	-0.4	1.2 ma	1.5 ma
-0.2	2.8 ma	2.9 ma	-0.2	2.1 ma	2.3 ma
0	3.4 ma	3.6 ma	0	3.2 ma	3.2 ma

Table 4.1 Comparison of measurement and simulation of n-MODFETs

	2.5 um gate			5 um gate	
	measured	simulated		measured	simulated
V_g	I_{ds} (V_{ds}=5)	I_{ds}	V_g	I_{ds} (V_{ds}=5)	I_{ds}
1	17 ua	18 ua			
0.8	58 ua	59 ua	0.8	67 ua	37 ua
0.6	114 ua	112 ua	0.4	178 ua	118 ua
0.4	183 ua	173 ua	0	307 ua	225 ua
0.2	259 ua	240 ua	-0.4	403 ua	253 ua
0	346 ua	310 ua	-0.8	480 ua	311 ua

Table 4.2 Comparison of measurement and simulation of p-MODFETs

Figures 4.17 and 4.18 show the calculated source-drain current versus gate bias with varying AlGaAs electron mobility (Fig. 4.17) and doping level (Fig. 4.18). The current reaches a maximum value at a certain gate bias, i.e. I_{ds} saturates. This is the direct result of the second assumption, which limits the highest possible carrier density in the device. Therefore, if the gate bias is high enough to make all impurities ionized, further increase of the gate bias will not increase the channel carrier density nor the current. Varying the AlGaAs layer mobility only changes the value of the saturation current (Fig. 4.17), but has no effect on the gate bias value with the corresponding saturation current. The doping density determines the gate bias for maximum I_{ds}. Experimentally the saturation gate bias can be obtained from actual device measurements, hence the doping level can be obtained by fitting the data to calculated curves such as Fig. 4.17, 4.18. Once the doping level is determined, the mobility of the AlGaAs layer can be obtained by fitting the saturation current value. The best fit to the data in Fig. 3.8 shown in Fig. 4.15 gives the following parameters: doping density - $3.8X10^{12}$ #/cm^2, mobility in AlGaAs - 3500 cm^2/V-sec. The mobility in AlGaAs is much higher than that reported by Chang and Morkoc [26]. For 24 percent Al and Si doping density at the level of $1X10^{18}$ #/cm^3, the AlGaAs mobility is about 900 cm^2/V-sec, and 2000 cm^2/V-sec for Si doping level at $1X10^{17}$ #/cm^3. These values could indicate that the mobility in a planar doping layer is higher than that in a uniform layer. This possibility will be discussed in the next section.

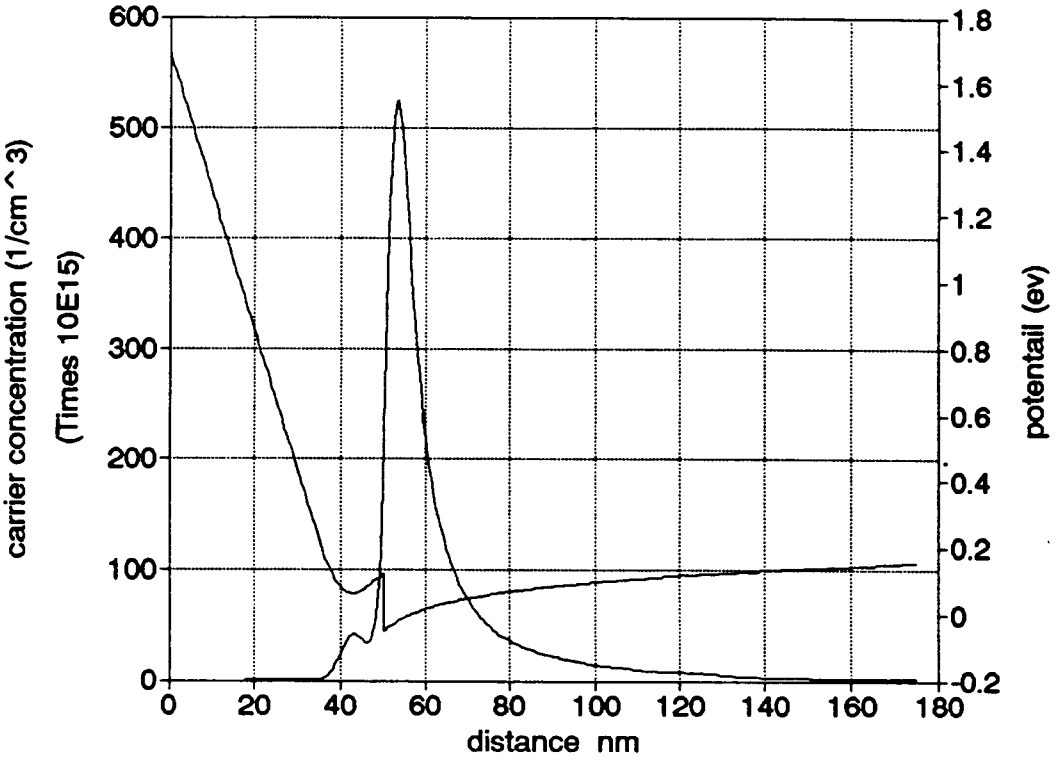

Figure 4.4 Charge distribution and conduction band profile at -0.7 volt gate bias in the n-MODFETs

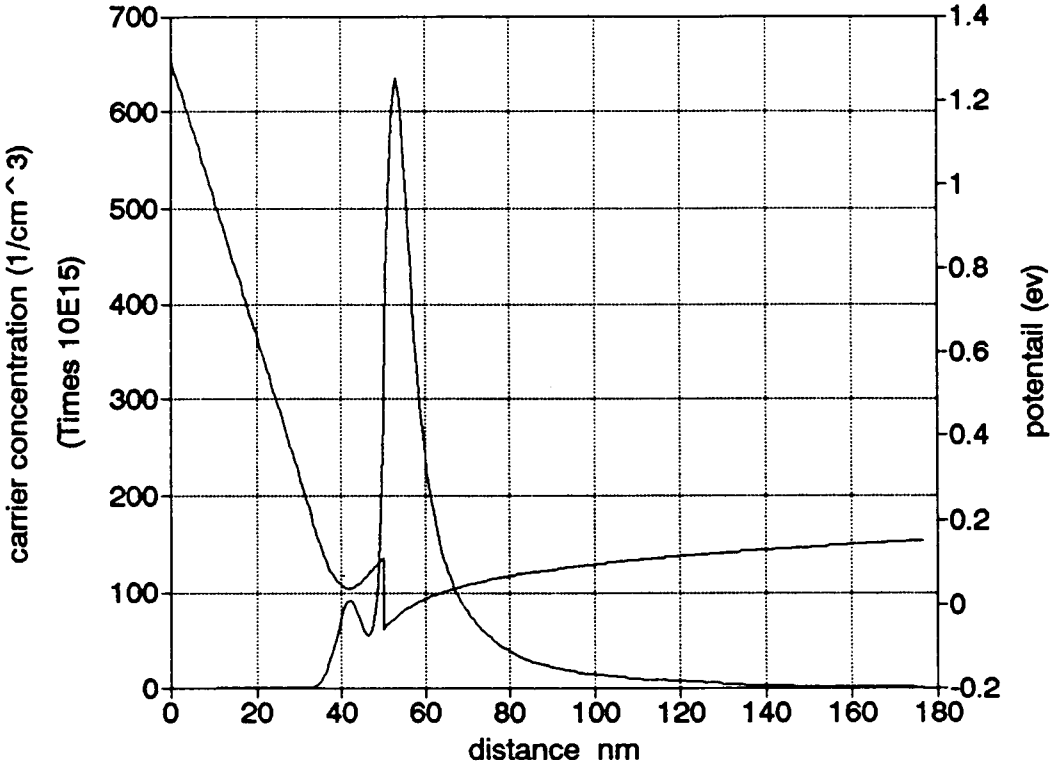

Figure 4.5 Charge distribution and conduction band profile at -0.3 volt gate bias in the n-MODFETs

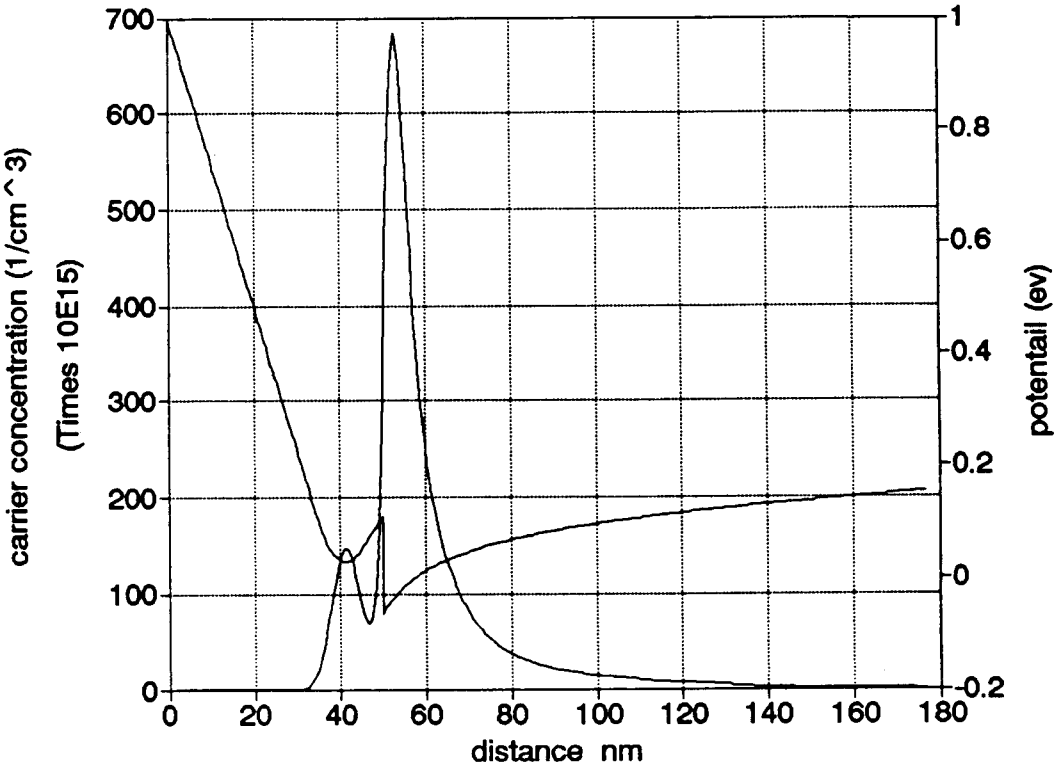

Figure 4.6 Charge distribution and conduction band profile at 0 volt gate bias in the n-MODFETs

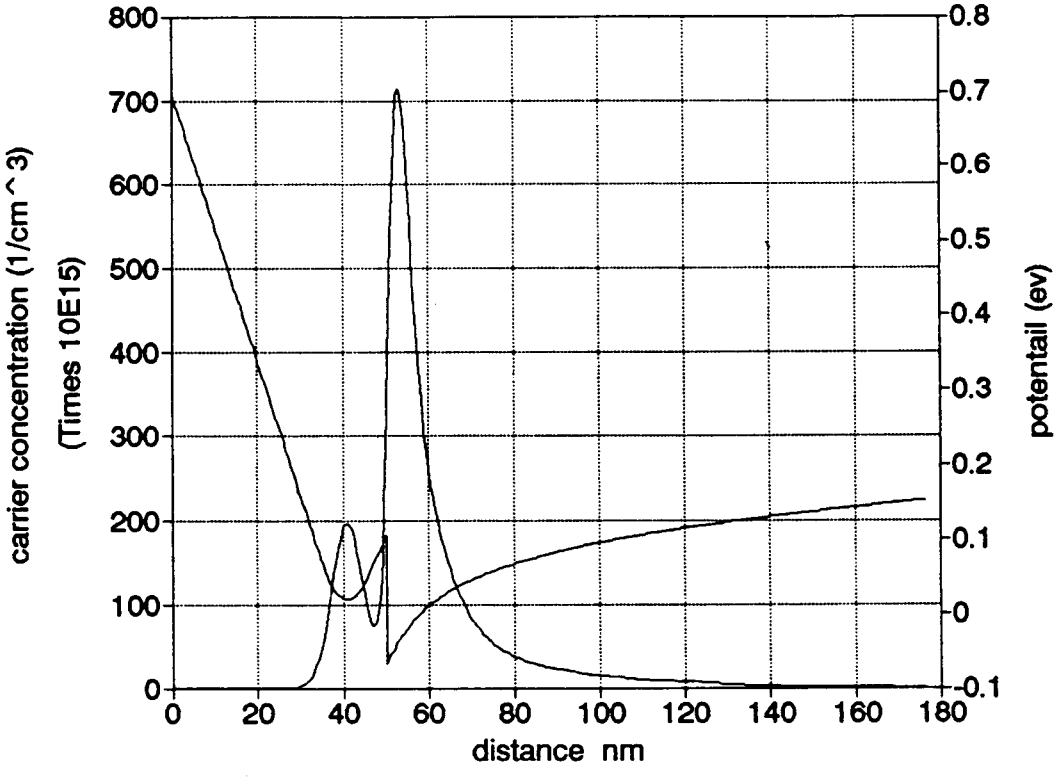

Figure 4.7 Charge distribution and conduction band profile at 0.3 volt gate bias in the n-MODFETs

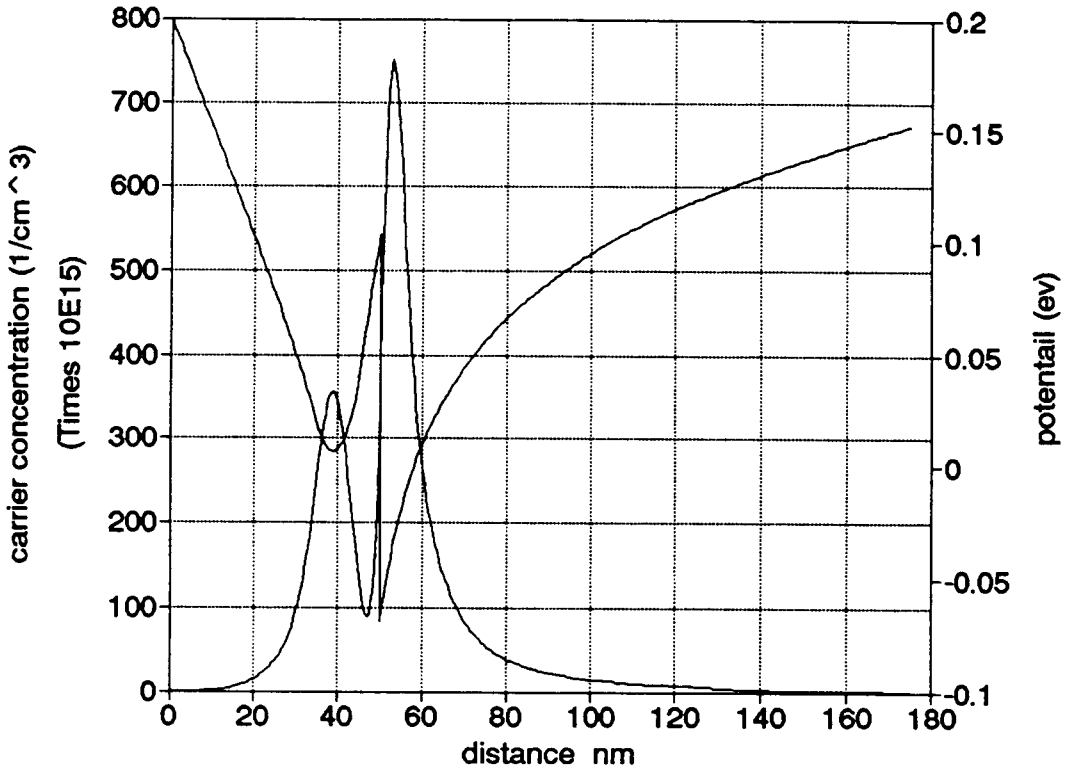

Figure 4.8 Charge distribution and conduction band profile at 0.8 volt gate bias in the n-MODFETs

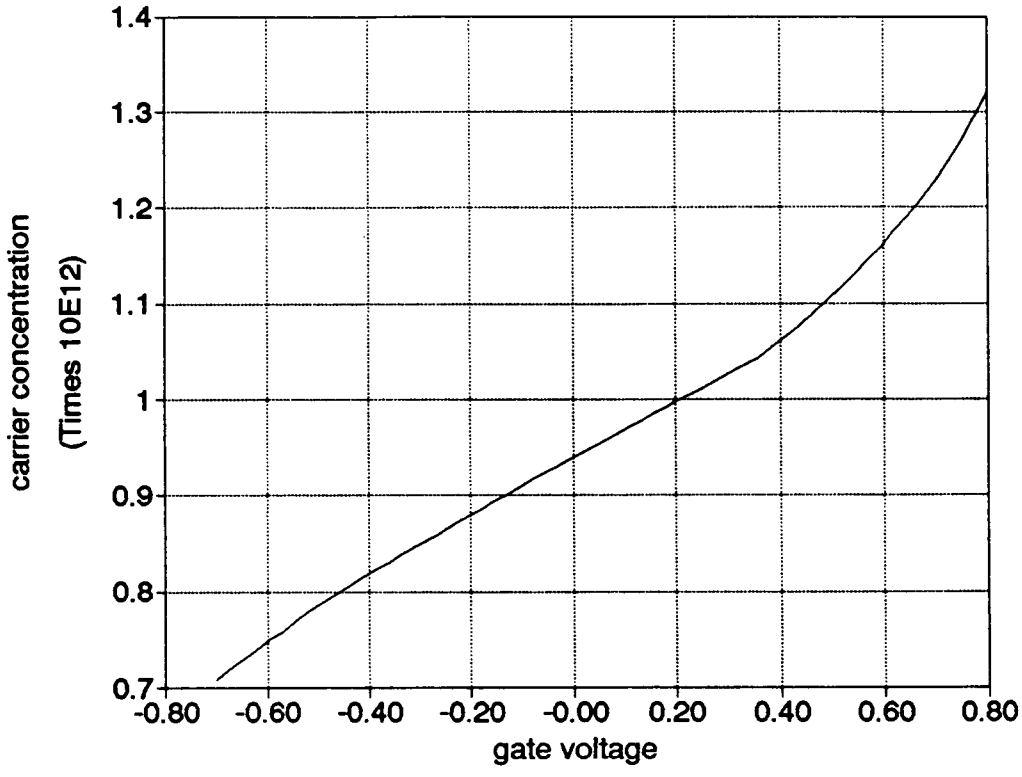

Figure 4.9 Carrier density under the gate at different gate bias voltage

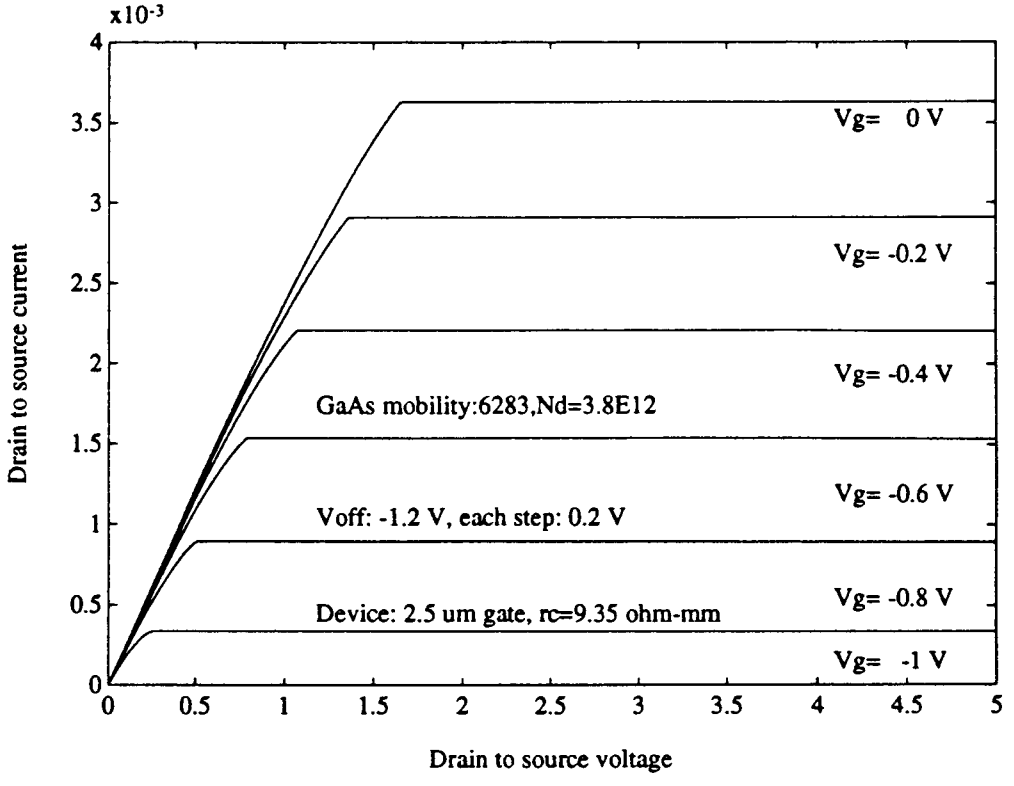

Figure 4.10 Simulation of the I-V curves of the 2.5 um gate length n-MODFET by velocity saturation mechanism

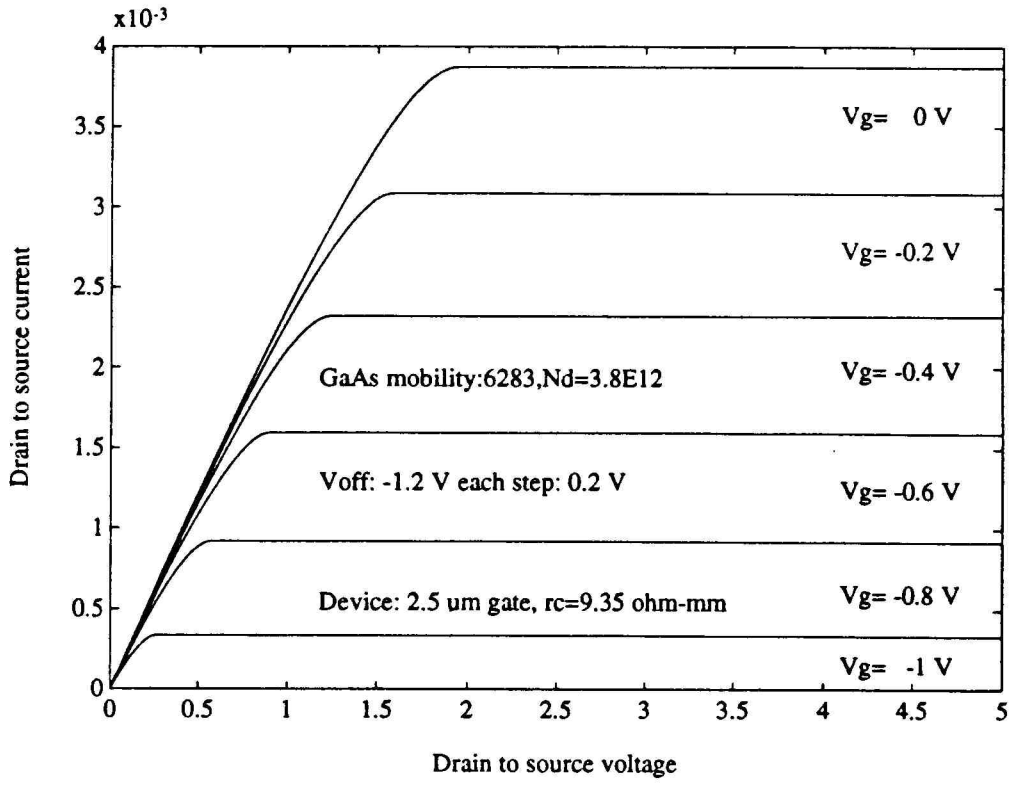

Figure 4.11 Simulation of the I-V curves of the 2.5 um gate length n-MODFET by pinch off mechanism

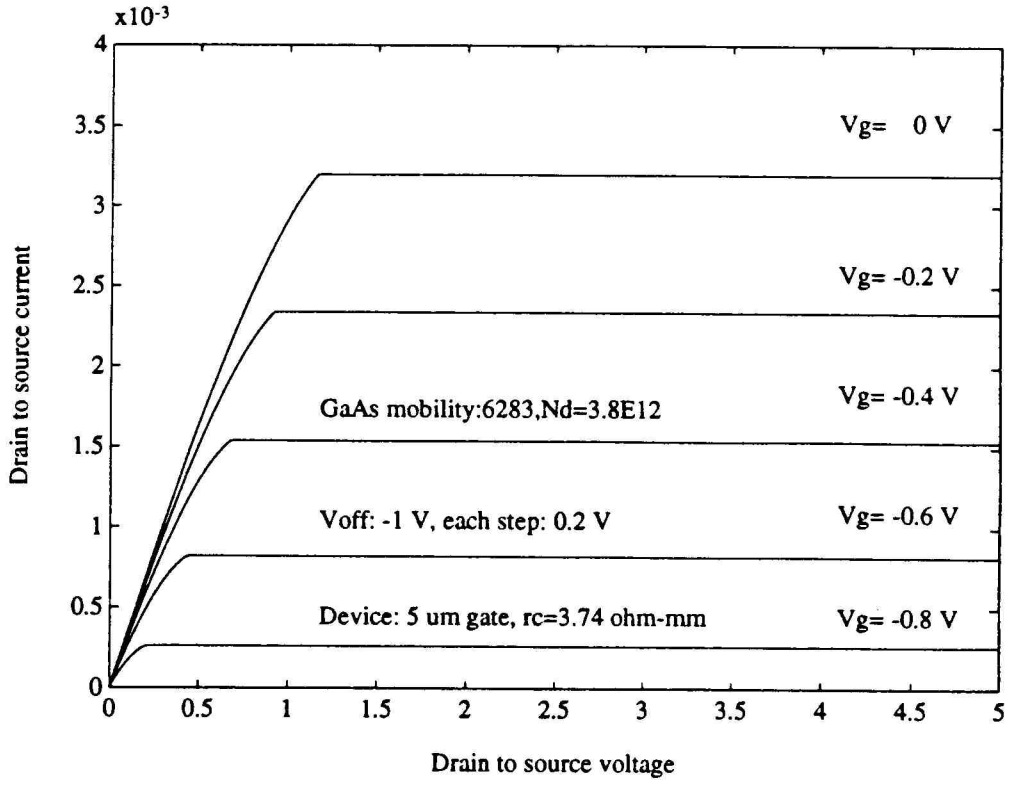

Figure 4.12 Simulation of the I-V curves of the 5 um gate length n-MODFET

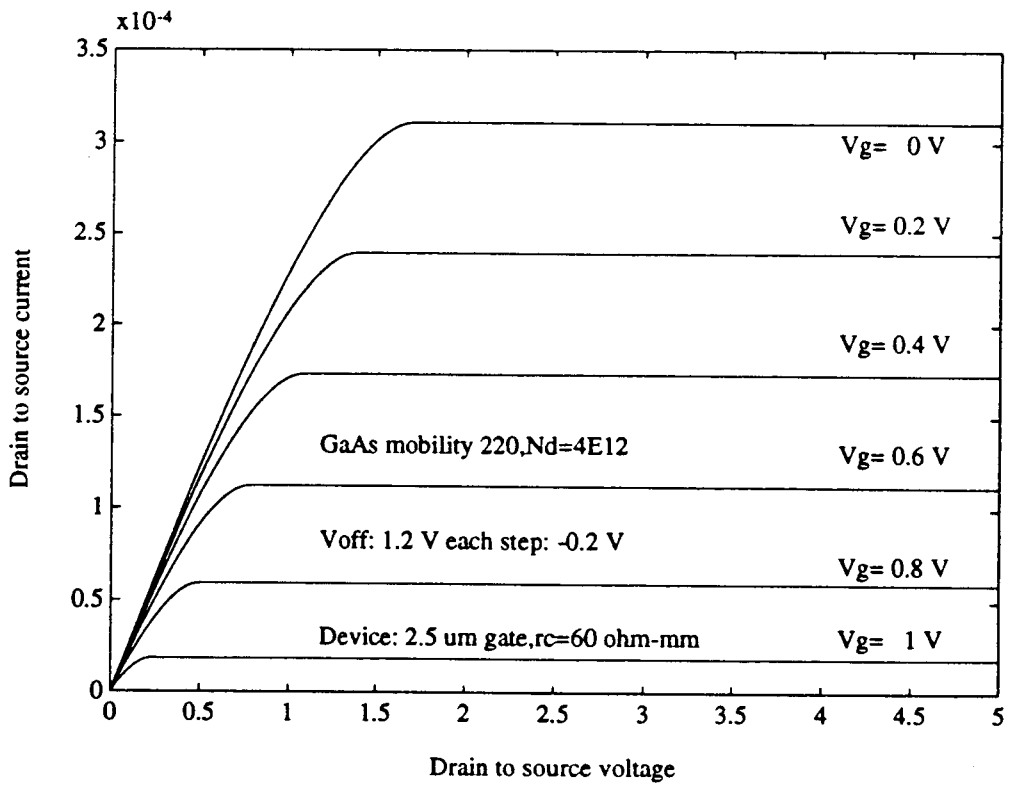

Figure 4.13 Simulation of the I-V curves of the 2.5 um gate length p-MODFET

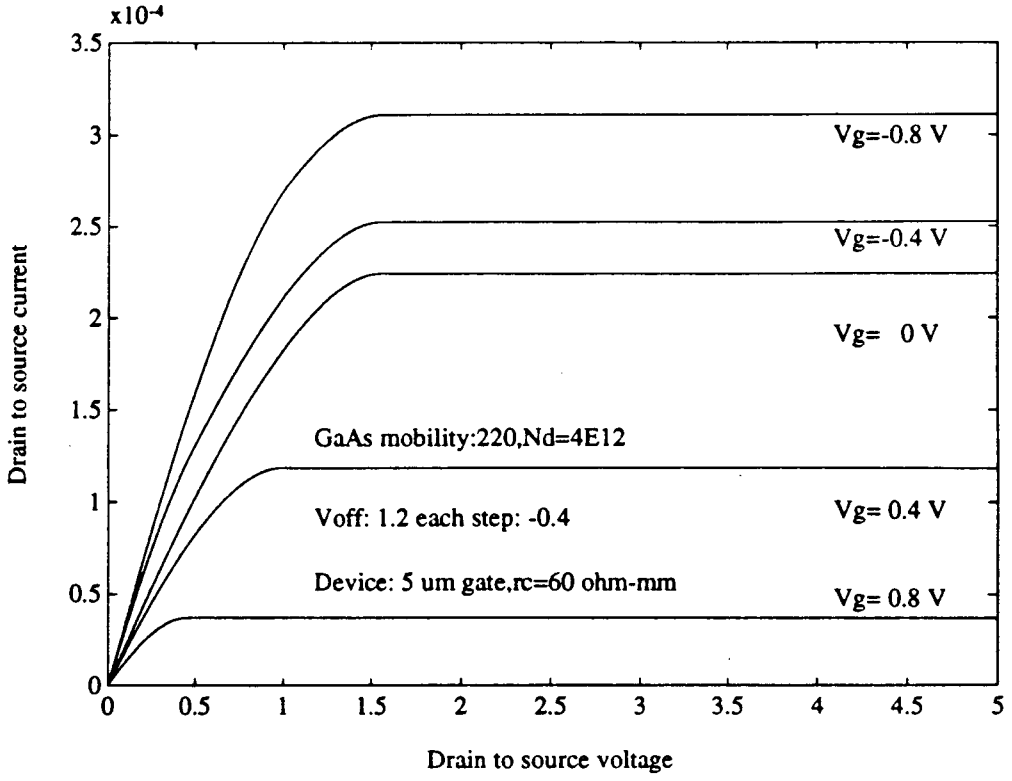

Figure 4.14 Simulation of the I-V curves of the 5 um gate length p-MODFET

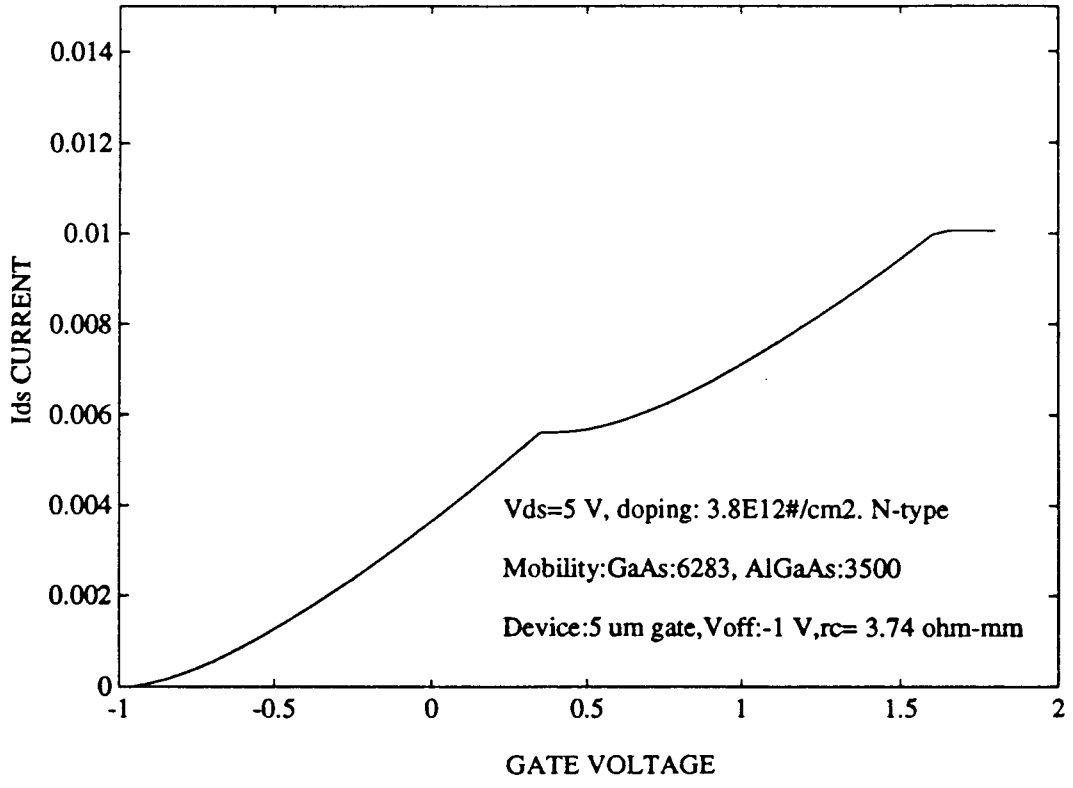

Figure 4.15 Simulation results of the source to drain current at device saturation region versus gate bias of the 5 um gate length n-MODFET

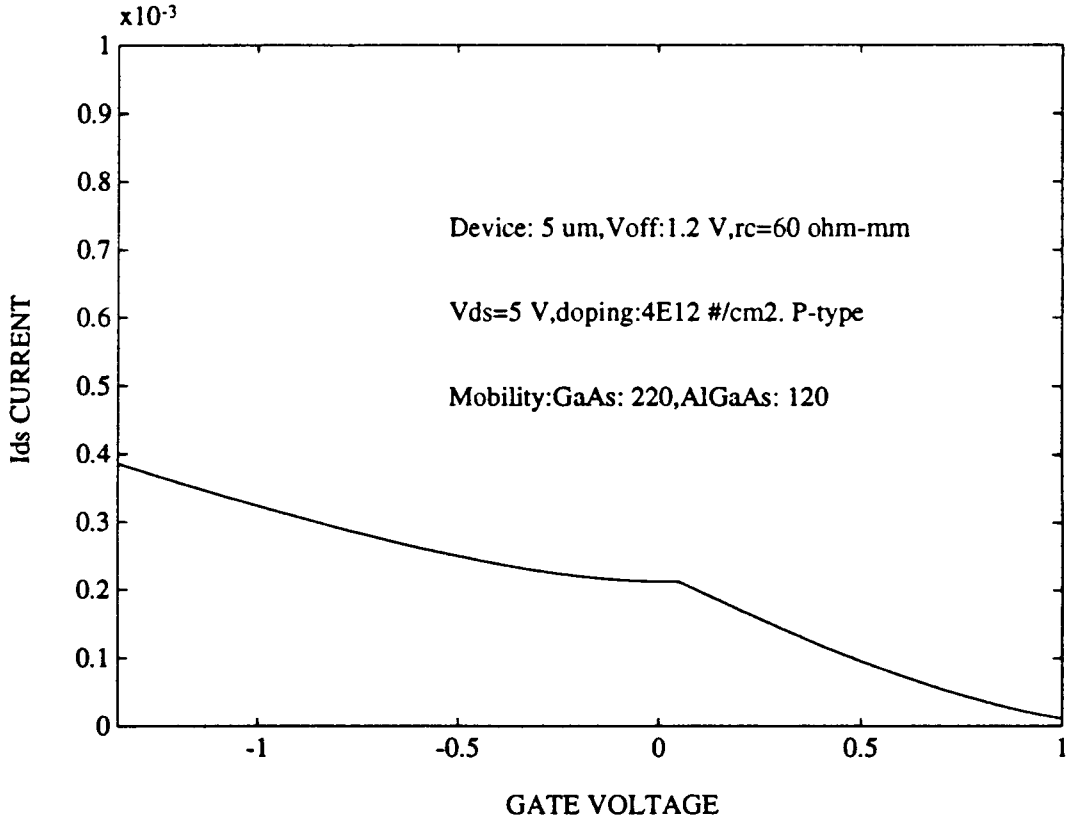

Figure 4.16 Simulation results of the source to drain current at device saturation region versus gate bias of the 5 um gate length p-MODFET

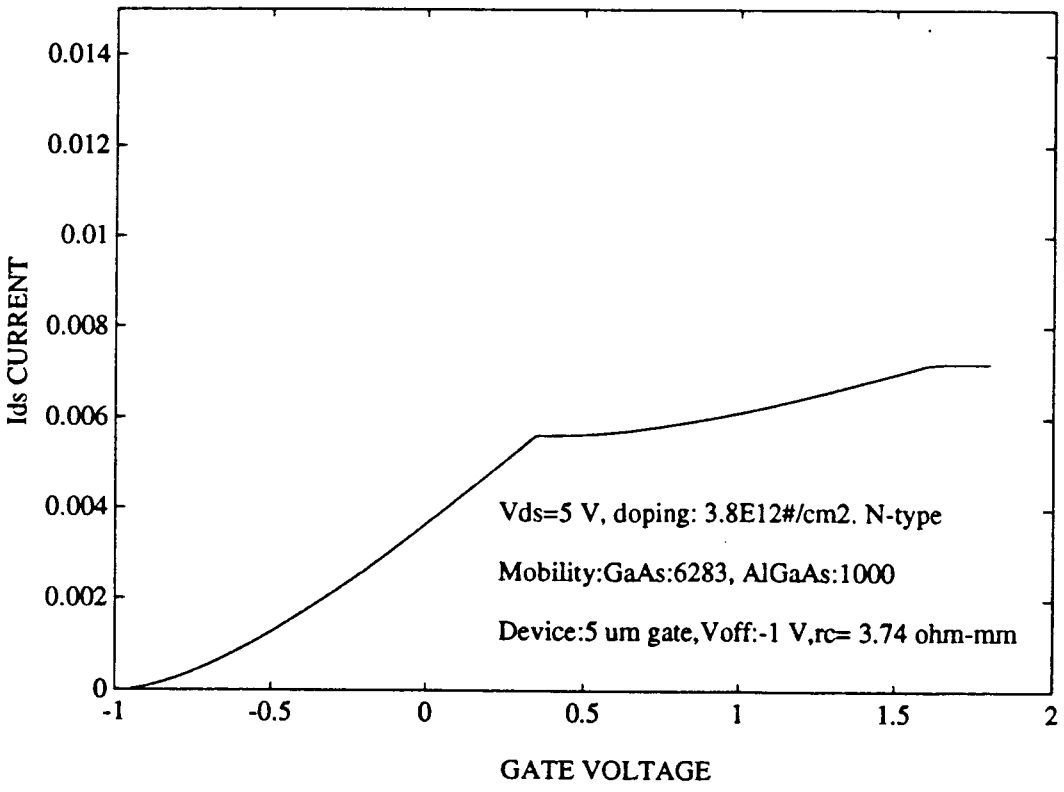

Figure 4.17 Simulation results of the source to drain current at device saturation region versus gate bias of the 5 um gate length n-MODFET under different AlGaAs mobility

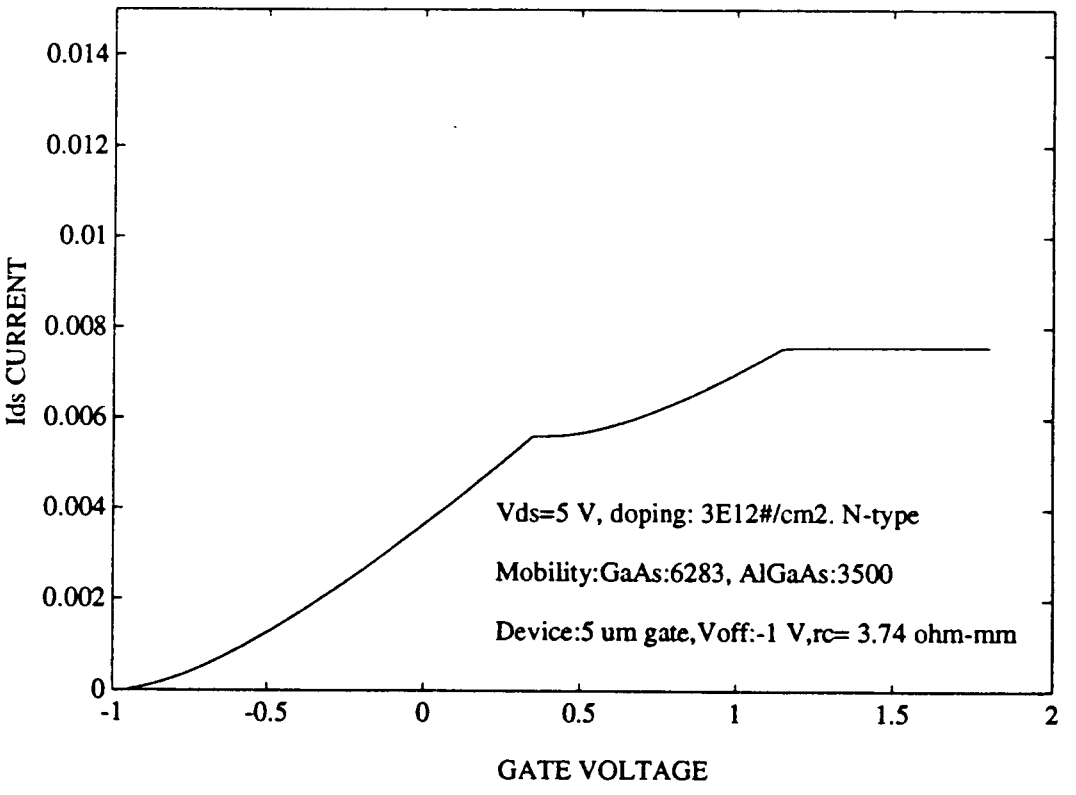

Figure 4.18 Simulation results of the source to drain current at device saturation region versus gate bias of the 5 um gate length n-MODFET under different impurity doping level

5. Discussion

In order to calculate the I-V characteristics of our MODFETs, a simple device model was proposed in this work which includes the parasitic current in the AlGaAs layer. There are two simplifying assumptions in the model. First the parasitic AlGaAs current is assumed to become significant only after the GaAs channel reaches the maximum carrier confinement. This is certainly an over-simplification because the parasitic current actually turns on smoothly rather than abruptly. The effect of an abrupt turn-on can be seen in figures 4.17 and 4.18. The real carrier density in the AlGaAs layer increases smoothly as gate bias increases.

The second assumption is that the maximum carrier density is the same as the doping concentration [23]. After total ionization of the doping atoms, further gate bias will not increase carrier density in the channel. It has been observed in our device characterization that saturation current does not increase after a certain gate bias (Fig. 3.8). The factor which determines this gate voltage is the impurity doping concentration. Therefore, we can extract the doping level from the device I-V curve. The best fit to the data in figure 3.8 is shown in figure 4.15 for an impurity doping concentration for a n-MODFET of $3.8X10^{12}$ #/cm^2; this is very close to the expected impurity level, $4X10^{12}$ #/cm^2, calculated from the Si oven doping calibration. Thus the experimental results verify that over limited range of gate bias, the carrier density does not exceed the donor level.

An alternative explanation of the fact that the saturation current does not increase after a certain gate bias is that the gate becomes "leaky" at high gate bias voltage. High gate bias voltage only generates additional gate leakage current, and the parallel conduction channel is not biased further.

Once the doping concentration is determined, the mobility in the AlGaAs can be extracted by fitting the simulation saturation current (fig. 4.15) to the measured data (Fig. 3.8). The mobility extracted by this curve fitting is 3500 cm^2/ V-sec. The mobility that was measured for a uniform doped AlGaAs Hall sample at a Si doping level $1X10^{18}$ #/cm^3 is in the range of 1000 cm^2/ V-sec. Therefore, the extracted mobility in the delta doped AlGaAs layer is clearly higher than that observed in uniformly doped devices.

One possible explanation for such a phenomenon is that the electron distribution is wider than the impurity distribution. Therefore, when electrons flow through the 40 nm thick AlGaAs layer, the impurity scattering rate depends on the location of the electrons relative to the doping plane. Near the doping plane where the Si ions are located, electron mobility is low. Away from the doping plane, the electron mobility is high. The average mobility in planar doped layer will be higher than in a uniform doped layer because of reduced impurity scattering.

In the p-MODFET device, the gate voltage was not high enough to observe a current saturation effect. It should be possible to observe the same phenomena by further biasing the gate. Results have already been shown in figures at the end of chapter three.

Several single layer structure (Fig. 1.1) n-MODFETs were also processed and characterized separately. With the complementary structures, more processing steps of the n-MODFETs are required in order to remove the upper p layers. There was concern that the n-MODFETs device performance might be degraded due to the extra chemical steps. However, comparison of the electrical results from the n-MODFET devices after etching away the p layers with other n-MODFET devices grown without p-layer, shows no degradation of the device performance. Therefore, the extra chemical etching steps appear to cause no serious effects on device performance.

6. Conclusion and future work

In this work, a simple complementary MODFET process scheme has been demonstrated. Individual p and n MODFET devices were fabricated and characterized. The Van der Pauw hall data shows 113 cm^2/v-sec and 1411 cm^2/v-sec p type device mobility at 300K and 77K respectively, and 6283 cm^2/v-sec and 57190 cm^2/v-sec n type device mobility at 300K and 77K. The maximum device transconductance of 2.5 um gate length are 5.5 mS/mm for P-MODFET and 70 mS/mm for N-MODFET at room temperature. Th ohmic contact resistance was also measured and the data is 60 ohm-mm for p type, 9.35 ohm-mm for 2.5 um gate and 3.74 ohm-mm for 5 um gate length n type.

The devices in this work had a minimum 2.5 um gate length, and the gates were not self-aligned. A problem with such a process is caused by the open area between gate to source and gate to drain, which increases gate to drain resistance and gate to source resistance. Device performance is limited by this restriction. In order to improved the device performance, it would be desirable to use a self-aligned process. Another step for improvement is to have a 1 um process technique instead of 2.5 um. The smaller gate length, the better device performance. With the combination of above techniques, it will certainly improve the device performance.

A simple current voltage model was developed to fit the measurement data. Both the parasitic effect of parallel conduction in the AlGaAs layer, and the gate to source/drain resistance were considered in the model. A comparison of the experimental results with the model

calculations suggests that a higher electron mobility in the planar doped AlGaAs layer than in uniformly doped AlGaAs. Further development and verification of the model would be a useful step in the design of the MODFETs.

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APPENDIX

Appendix

```
% THIS PROGRAM SOLVES N CHANNEL 2.5 UM GATE LENGTH DC
% I-V CURVE. ALL PROGRAMS ARE WRITTEN IN MATLAB.
hori=[zeros(1:500)];
tmp=[zeros(1:500)];
tmp1=[zeros(1:500)];
vert1=[zeros(1:500)];
vert2=[zeros(1:500)];
vert3=[zeros(1:500)];
vert4=[zeros(1:500)];
vert5=[zeros(1:500)];
vert6=[zeros(1:500)];
q=1.6E-19;
diel=12.5*8.85E-14; % gaas diel const,var;
voff=-1.2;          % cut off voltage,var;
u=6283;             % mobility,var;
d=570E-8;           % d+70A capacitance,var;
ns=1E12;            % carrier density,var;
l=10E-4;            % open area lenth,var;
L=2.5E-4;           % gate length,var;
w=75E-4;            % gate width,var;
r=1/q/u/ns/w        % resistance in Rsd+Rs;
rc=100;             % contact resist,var;
rc=rc*187/75;
sp=100E-8;          % spacer,var;
up=3500;            % algaas mobility,var;
nd=3.8E12;          % doping level,var;
rp=1/q/up/(nd-ns)/w;% resistance in algaas;
rp=rp+rc;
r=rc+r              % total open area resistance;
vg=-1.2;

beta=diel*u*w/d/L;
v0=1E7/u*L;
rs=r/2;

for cnt=1:6
vg=vg+0.2
  if vg >= 0.4
     vd=0;
     while  vd<=500
          vd=vd+1;
          vd=vd/100;
          vg3=0.4-voff
          upper=vd*(vg3-vd/2);
          lower=L/u/w/(diel/d)+r*(vg3-vd/2);
          id=upper/lower;
          vd=100*vd;
```

```
          tmp1(vd)=id;
          vd=vd/100;
        isat=beta*v0^2/(1-beta^2*rs^2*v0^2);
        isat=isat*(sqrt(1+2*beta*rs*vg3+vg3^2/v0^2)-1-
             beta*rs*vg3);
        isat=isat-0.0001;
        if id >= isat
           vd=vd*100;
           while vd < 501
             tmp1(vd)=id;
             vd=vd+1;
           end
        end
        vd=vd*100;
   end
end

vd=0;
while vd<=500
    vd=vd+1;
    vd=vd/100;
    if vg <= 0.4
       upper=vd*(vg-voff-vd/2);
       lower=L/u/w/(diel/d)+r*(vg-voff-vd/2);
       id=upper/lower;
       vd=100*vd;
       if cnt == 1
          vert1(vd)=id;
          elseif cnt == 2
          vert2(vd)=id;
          elseif cnt == 3
          vert3(vd)=id;
          elseif cnt == 4
          vert4(vd)=id;
          elseif cnt == 5
          vert5(vd)=id;
          elseif cnt == 6
          vert6(vd)=id;
       end
         vd=vd/100;
       vg3=vg-voff;
       isat=beta*v0^2/(1-beta^2*rs^2*v0^2)*(sqrt
           (1+2*beta*rs*vg3+vg3^2/v0^2)-1-
            beta*rs*vg3);
       if id > isat
          vd=vd*100;
          while vd < 501
             if cnt == 1
                vert1(vd)=id;
                elseif cnt == 2
                vert2(vd)=id;
```

```
                    elseif cnt == 3
                    vert3(vd)=id;
                    elseif cnt == 4
                    vert4(vd)=id;
                    elseif cnt == 5
                    vert5(vd)=id;
                    elseif cnt == 6
                    vert6(vd)=id;
                 end
                vd=vd+1;
             end
          end
       else
          vg1=vg-0.4
          upper=vd*(vg1-vd/2);
          lower=L/up/w/(diel/400E-8)+rp*(vg1-vd/2);
          id1=upper/lower;
          tmp(vd*100)=id1;
          if (vd-rp*id1/2) >= vg1
             vd=vd*100;
             while vd < 501
                   tmp(vd)=id1;
                   vd=vd+1;
             end
             for k=1:500
                 tmp(k)=tmp(k)+tmp1(k);
                 if cnt ==1
                    vert1(k)=tmp(k);
                 elseif cnt == 2
                    vert2(k)=tmp(k);
                 elseif cnt == 3
                    vert3(k)=tmp(k);
                 elseif cnt == 4
                    vert4(k)=tmp(k);
                 elseif cnt == 5
                    vert5(k)=tmp(k);
                 elseif cnt == 6
                    vert6(k)=tmp(k);
                 end
             end
          end
       end
       vd=vd*100;
   end

end


for k=1:500
    hori(k)=k/100;
```

```
end
axis([0,5,0,0.004]);
plot(hori,vert1,'-',hori,vert2,'-',hori,vert3,'-
',hori,vert4,'-',hori,vert5,'-',hori,vert6,'-');
xlabel('Drain to source voltage')
ylabel('Drain to source current')
text(0.8,0.14,'Vg=   -1 V','sc')
text(0.8,0.22,'Vg= -0.8 V','sc')
text(0.8,0.35,'Vg= -0.6 V','sc')
text(0.8,0.50,'Vg= -0.4 V','sc')
text(0.8,0.65,'Vg= -0.2 V','sc')
text(0.8,0.82,'Vg=    0 V','sc')
text(0.3,0.46,'GaAs mobility:6283,Nd=3.8E12','sc')
text(0.3,0.32,'Voff: -1.2 V, each step: 0.2 V','sc')
text(0.3,0.2,'Device: 2.5 um gate, rc=9.35 ohm-mm','sc')
```

```
% THIS PROGRAM SOLVES P CHANNEL 2.5 UM GATE LENGTH DC
% I-V CURVE
hori=[zeros(1:500)];
tmp=[zeros(1:500)];
tmp1=[zeros(1:500)];
vert1=[zeros(1:500)];
vert2=[zeros(1:500)];
vert3=[zeros(1:500)];
vert4=[zeros(1:500)];
vert5=[zeros(1:500)];
vert6=[zeros(1:500)];
q=1.6E-19;
diel=12.5*8.85E-14;  % gaas diel const,var;
voff=1.2;            % cut off voltage,var;
u=220;               % mobility,var;
d=570E-8;            % d capacitance,var;
ns=2.3E12;           % carrier density,var;
l=10E-4;             % open area lenth,var;
L=2.5E-4;            % gate length,var;
w=75E-4;             % gate width,var;
r=1/q/u/ns/w*l;      % resistance in Rsd+Rs;
rc=640;              % contact resist,var;
rc=rc*187/75;
sp=100E-8;           % spaver,var;
up=130;              % algaas mobility,var;
nd=4E12;             % doping level,var;
rp=l/q/up/(nd-ns)/w; % resistance in algaas;
rp=rp+rc;
r=rc+r;              % total open area resistance;
vg=1.2;


for cnt=1:6
vg=vg-0.2

  if vg <= 0
     vd=0;
     while  vd<=500
         vd=vd+1;
         vd=vd/100;
         vg3=voff-0;
         upper=vd*(vg3-vd/2);
         lower=L/u/w/(diel/d)+r*(vg3-vd/2);
         id=upper/lower;
         vd=100*vd;
           tmp1(vd)=id;
           vd=vd/100;
         if (vd-r*id/2) >= vg3
            vd=vd*100;
```

```
            while vd < 501
              tmp1(vd)=id;
              vd=vd+1;
            end
        end
        vd=vd*100;
    end
end

vd=0;
while vd<=500
    vd=vd+1;
    vd=vd/100;
    if vg >= 0
       upper=vd*(voff-vg-vd/2);
       lower=L/u/w/(diel/d)+r*(voff-vg-vd/2);
       id=upper/lower;
       vd=100*vd;
       if cnt == 1
          vert1(vd)=id;
          elseif cnt == 2
          vert2(vd)=id;
          elseif cnt == 3
          vert3(vd)=id;
          elseif cnt == 4
          vert4(vd)=id;
          elseif cnt == 5
          vert5(vd)=id;
          elseif cnt == 6
          vert6(vd)=id;
       end
         vd=vd/100;
       if (vd-r*id/2) >= (voff-vg)
          vd=vd*100;
          while vd < 501
             if cnt == 1
                vert1(vd)=id;
                elseif cnt == 2
                vert2(vd)=id;
                elseif cnt == 3
                vert3(vd)=id;
                elseif cnt == 4
                vert4(vd)=id;
                elseif cnt == 5
                vert5(vd)=id;
                elseif cnt == 6
                vert6(vd)=id;
             end
            vd=vd+1;
          end
       end
```

```
        else
           vg1=-vg;
           upper=vd*(vg1-vd/2);
           lower=L/up/w/(diel/400E-8)+rp*(vg1-vd/2);
           id1=upper/lower;
           tmp(vd*100)=id1;
           if (vd-rp*id1/2) >= vg1
              vd=vd*100;
              while vd < 501
                    tmp(vd)=id1;
                    vd=vd+1;
              end
              for k=1:500
                  tmp(k)=tmp(k)+tmp1(k);
                  if cnt ==1
                     vert1(k)=tmp(k);
                  elseif cnt == 2
                     vert2(k)=tmp(k);
                  elseif cnt == 3
                     vert3(k)=tmp(k);
                  elseif cnt == 4
                     vert4(k)=tmp(k);
                  elseif cnt == 5
                     vert5(k)=tmp(k);
                  elseif cnt == 6
                     vert6(k)=tmp(k);
                  end
              end
           end
        end
        vd=vd*100;
    end

end


axis([0,5,0,0.00035])
for k=1:500
    hori(k)=k/100;
end

plot(hori,vert1,'-',hori,vert2,'-',hori,vert3,
'-',hori,vert4,'-',hori,vert5,'-',hori,vert6,'-');
xlabel('Drain to source voltage');
ylabel('Drain to source current');
text(0.8,0.18,'Vg=   1 V','sc')
text(0.8,0.27,'Vg= 0.8 V','sc')
text(0.8,0.41,'Vg= 0.6 V','sc')
text(0.8,0.55,'Vg= 0.4 V','sc')
text(0.8,0.7, 'Vg= 0.2 V','sc')
text(0.8,0.8, 'Vg=   0 V','sc')
```

```
text(0.3,0.42,'GaAs mobility 220,Nd=4E12 ','sc')
text(0.3,0.30,'Voff: 1.2 V each step: -0.2 V','sc')
text(0.3,0.18,'Device: 2.5 um gate,rc=60 ohm-mm','sc')
```