AN ABSTRACT OF THE THESIS OF

Peroly Natesan for the degree of Master of Science in Electrical and Computer Engineering presented on October 6, 2003.

Title: COMPARISON AND ANALYSIS OF JITTER IN CMOS RING OSCILLATORS

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A comparison and analysis of jitter for five different architectures of ring oscillators using a novel simulation technique developed by Professor Forbes' group is presented. Ring oscillators have become an essential building block in many digital and synchronous communications system due to their integrated nature and are widely used in phase-locked loops (PLL) for clock and data recovery, frequency synthesis and on-chip clock distribution and generation. The five different architecture circuits were injected with white noise and flicker noise according to our simulation technique and their jitter performance has been analyzed.

COMPARISON AND ANALYSIS OF JITTER IN CMOS RING OSCILLATORS

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COMPARISON AND ANALYSIS OF JITTER IN CMOS RING OSCILLATORS

1. INTRODUCTION

Ring oscillators have become an essential building block in many digital and synchronous communications system due to their integrated nature and are widely used in phase-locked loops (PLL) for clock and data recovery, frequency synthesis, on-chip clock distribution etc., [3]. The trend toward large-scale integration and low cost makes implementation of monolithic oscillators desirable. Ring oscillators have become an active area of research, it has been proposed they are a better choice for implementation of monolithic CMOS PLLs.

Though resonator-based oscillators like LC balanced oscillators have dominated RF industry due to their superior phase noise performance, resonator-less oscillators like ring oscillators have emerged as strong competitor because of low cost of CMOS only technology. Research is going on in developing new architectures and better design techniques due to increasing demand in high speed circuits, low power consumption and better noise performance.

In both RF and synchronous digital systems, accurate clock sources are required for the correct operation. Continuous advances in high-speed communication and measurement systems require higher levels of performance from system clocks and references. Oscillator uncertainty in these systems has many adverse effects, such as increasing the required channel separation in RF systems,

and reducing timing margins in digital systems. One of the most important applications of oscillators is clock generation.

Though CMOS LC tank oscillators have better phase noise performance [7][8], these oscillators make use of high quality on-chip spiral inductors. Taking care of parasitic effects requires extra non-standard processing steps[7][9]. Also, these suffer from a narrow tuning range, so that the performance of a frequency synthesizer is based on the process variations. Ring oscillator implementations takes care of these limitations. It has a smooth integration into a standard CMOS process without any extra steps and it has a wide tuning range. Ring oscillators are also used for determining inverter time delays as a means to evaluate a CMOS fabrication process.

1.1. PHASE LOCKED LOOPS

VCO's are widely used as a critical blocks in frequency synthesizers and phase locked loops (PLLs) which are an important component in wireless systems. Generally in PLLs, a single high-precision oscillator generates a reference signal which is used by the PLL to force the phase error of the local oscillator to nearly zero. The figure 1.1 shows the basic block diagram of PLLs.

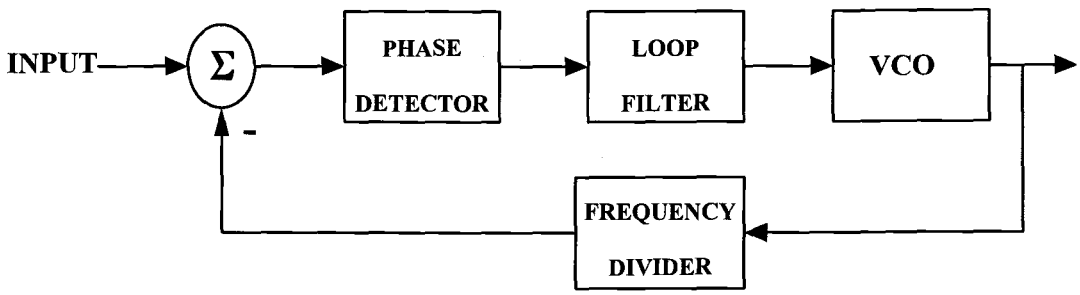

FIGURE 1.1 The basic block diagram of a phase locked loop.

The block diagram consists of a phase detector followed by a loop filter and a VCO in a feedback loop. The phase detector generates an error signal based on the comparison of phases of the high-precision oscillator reference signal and VCO output. The loop filter is a low pass filter which presents a dc level to oscillator. The output of the filter gives the control voltage to the VCO which varies the oscillation frequency until the loop is locked and the phases are aligned. It is important to reduce the phase noise of the VCO because phase noise of the system outside the loop bandwidth of the PLL is dominated by it.

1.2. OSCILLATORS OVERVIEW

Oscillators are closed loop systems with a positive feedback loop. Oscillators can be classified as resonator-less oscillators (ring oscillator, relaxation oscillator) or resonator based oscillator (LC oscillator). Consider a system with an open loop transfer function, A, and a feedback gain, β, as shown in the figure 1.2,

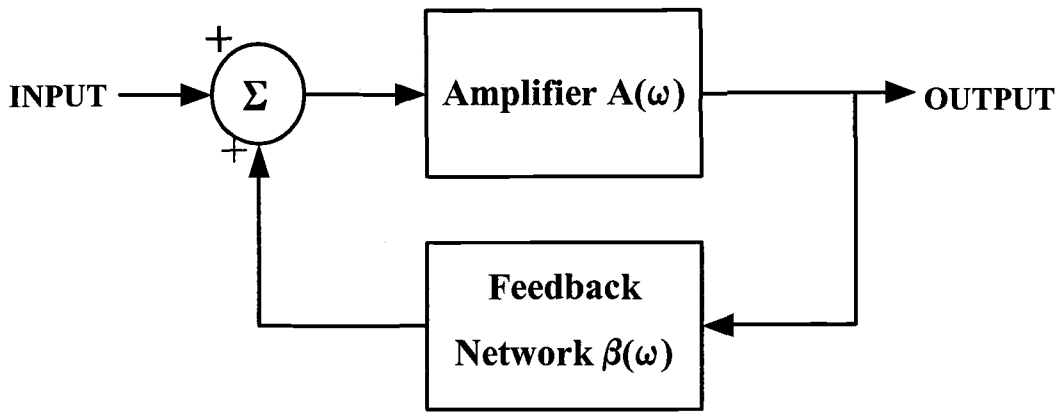

FIGURE 1.2 The block diagram of an oscillator.

The transfer function of the system is given as,

$$\frac{Vout}{Vin} = \frac{A(s)}{1 - A(s)\beta(s)} \tag{1.1}$$

The loop gain of the circuit is

$$L(s) = A(s)\,\beta(s) \tag{1.2}$$

The key to designing an oscillator is ensuring $L(j\omega_0) = A(j\omega_0)\beta(j\omega_0) = 1$. The above condition is called the Barkhausen Criterion. So the condition for oscillation at ω_0 is that the loop gain should be unity and the phase of the loop gain must be zero.

Oscillators don't require an externally applied input signal. Instead, they use some fraction of the output signal created by the feedback network as the input signal. Oscillation results when the feedback system is not able to find a stable steady-state.

For a negative feedback system, as the phase shift approaches 180° and $|A\beta|=1$, the output voltage of the now-unstable system tends to infinity and here it is limited to the finite values by an energy-limited power supply. The active devices in the amplifiers change gain as soon as the output voltage approaches either power rail. This causes the value of A to change and forces $A\beta$ away from the singularity, thus the tending towards an infinite voltage slows and eventually stops.

At this stage, one of the three things can occur [5]: (a) Nonlinearity in saturation or cutoff causes the system to become stable and lock up at the current power rail. (b) The initial change causes the system to saturate (or cutoff) and stay that way for a long time before it becomes linear and heads for the opposite power rail. (c) The system stays linear and reverses direction, heading for the opposite power rail.

Highly distorted oscillation is produced by the second condition and these resulting oscillators are called relaxation oscillators. Sine-wave oscillation is produced by the third condition.

At the oscillation frequency, the oscillator gain must be equal to unity. Under normal conditions, the circuit becomes stable when the gain exceeds unity, and the oscillations cease. However, when the gain exceeds unity with a phase shift of – 180°, the nonlinearity of the active device reduces the gain to unity and the circuit oscillates.

Predicting phase noise and jitter accurately for oscillator circuits is a difficult task. Though there are commercial simulators like SpectreRF from Cadence, ADS from Agilent-EEsof and ELDO from Mentor graphics, there is no detailed

comparison between simulation and measurements. Similar oscillator circuits give different phase noise readings when simulated under different commercial simulators. A lot of features are still under development. Though most of the simulators predict phase noise to an agreeable accuracy, they don't give values of different jitters.

1.3. THESIS ORGANIZATION

This work analyses the different techniques employed to determine and calculate jitter and phase noise in ring oscillators. I compared and analyzed jitter and phase noise in five different ring oscillator architectures based on the novel simulation technique [6]. The chapter 2 consists of definitions of different types of jitters and phase noise. It also deals with the study of the previous work done in ring oscillators. It also contains a brief description of the SPICE models used to simulate and determine the jitter. Chapter 3 describes the different architectures used. Chapter 3 also gives a detail account of procedures involved in finding jitter in oscillator circuits. It describes how white noise and flicker noise are modeled and injected into the circuits and how a transient analysis is done and how jitter is calculated from the data obtained from the transient analysis. Chapter 4 gives the different tables and graphs of the observations. Chapter 5 gives conclusions and outline future work that might be carried out.

2. PHASE NOISE AND JITTER

Phase noise and timing jitter are both measures of uncertainty in the output of an oscillator in the frequency and time domains respectively. Defining and measuring the jitter is critical to the performance of synchronous communication systems.

2.1 INTRODUCTION

2.1.1 PHASE NOISE

The output of a practical oscillator can be written as

$$\text{Vout(t)} = A(t).f(\omega_o t + \phi(t)) \qquad (2.1)$$

Where the function f is periodic in 2π and $\phi(t)$ and A(t) model fluctuations in amplitude and phase due to internal and external noise sources.

The statistical process in $\phi(t)$ and A(t) give rise to sidebands about the carriers. Phase noise is the normalization of power in a 1 Hz bandwidth with respect to the carrier. As can be seen from the figure 2.1, phase noise is a function of offset frequency from the carrier.

$$L\{\Delta\omega\} = 10 \bullet \log\left[\frac{P_{sideband}(\omega_0 + \Delta\omega, 1Hz)}{P_{carrier}}\right] \qquad (2.2)$$

It is measured as dB below the carrier per unit bandwidth, Hz.

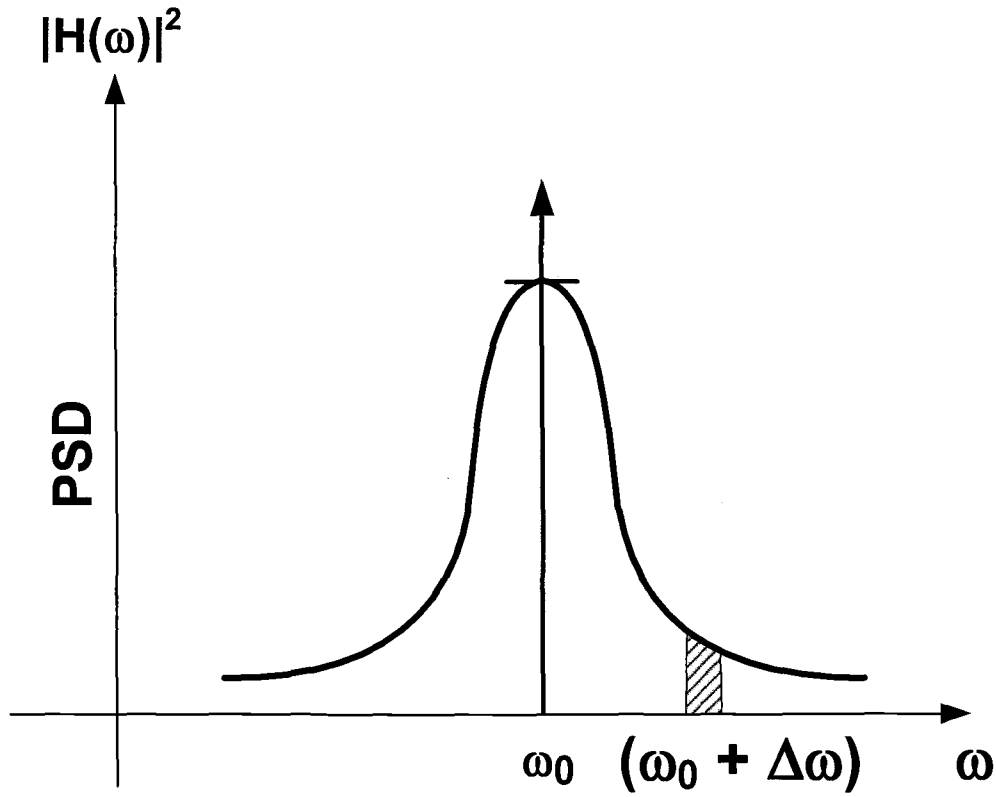

Figure 2.1 Phase noise at the offset frequency of $\omega_0 + \Delta\omega$.

2.1.2 JITTER

Jitter refers to a waveform's timing uncertainty as shown in figure 2.2. Jitter on the data signal or clock reduces the width of the effective "window" available for determining ONE or ZERO values. For each doubling of frequency, the maximum "window" available for reading the effective window for data reading therefore shrinks significantly with increasing frequency.

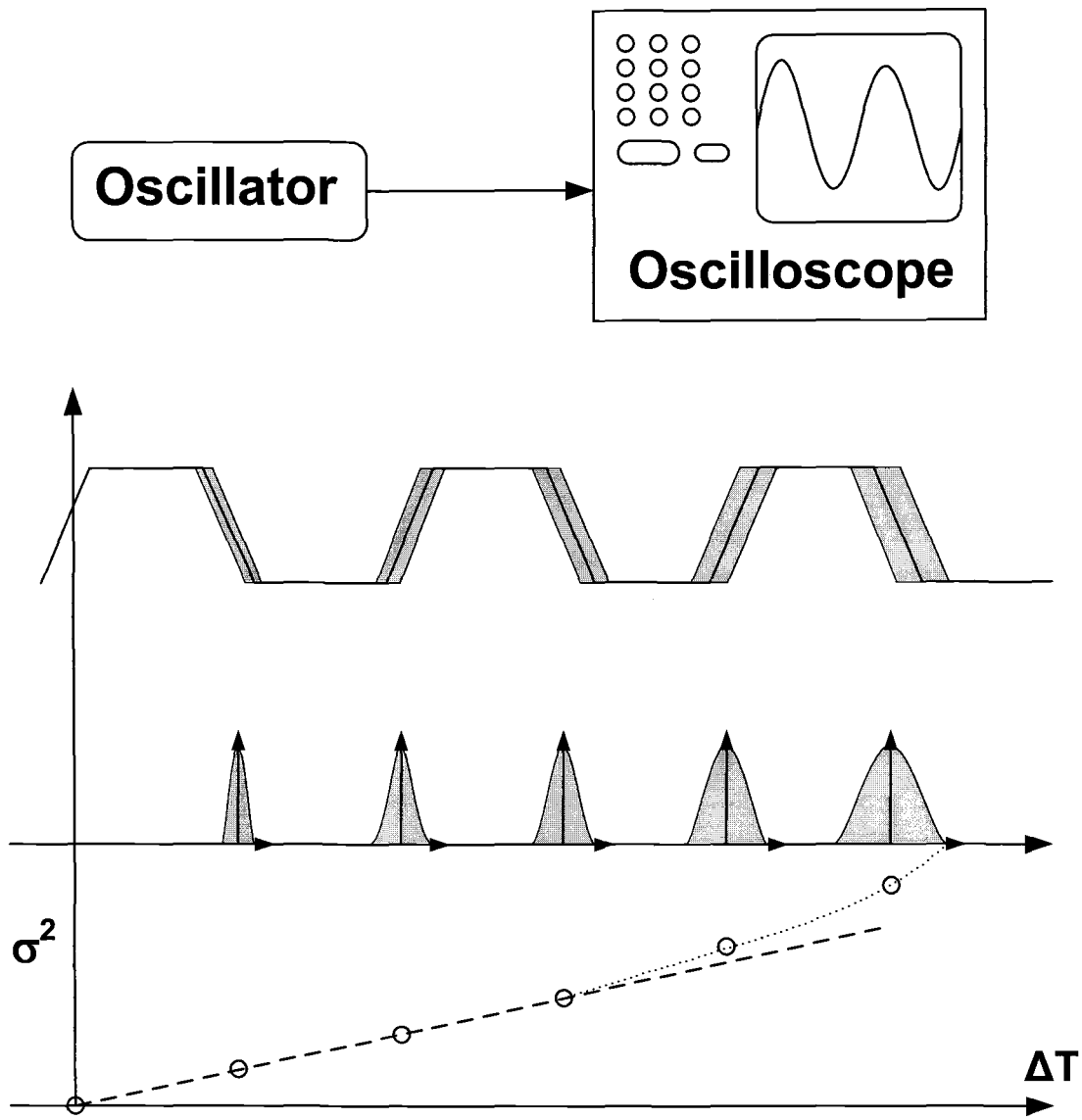

FIGURE 2.2 Timing jitter

Definition of Jitter

Consider an output voltage Vout(t) of an oscillator. The time point of the nth minus-to-plus zero crossing of Vout(t) is referred to as t_n. The n^{th} period is then defined as $T_n = t_{n+1} - t_n$. For an ideal oscillator, this T_n is constant independent of n but in reality it varies with n as a result of noise it the circuit. The deviation from ideal reference is an indication of jitter, noted as $\Delta T_n = T_n - \overline{T}$, where n refers to nth period, T_n is the nth period, $\overline{T}$ is the ideal reference.

2.2 WHY DIFFERENT TYPES OF JITTER?

Because the noise process is very random and one cannot identify a specific value of voltage at a particular time and zero crossing is also very random. The only course of action is to characterize the noise with statistical measure, such as mean square or RMS. Absolute jitter, cycle to cycle jitter, peak jitter, cycle jitter are different statistical measures of jitter.

Absolute or Long-term Jitter

Absolute or long-term jitter is the total phase error with respect to an ideal oscillator as shown in figure 2.3. Absolute jitter is ill suited to describe the performance of oscillators because ΔT_{abs} diverges with time.

$$\Delta T_{abs}(N) = \sum_{n=1}^{N} \Delta T_n \qquad (2.3)$$

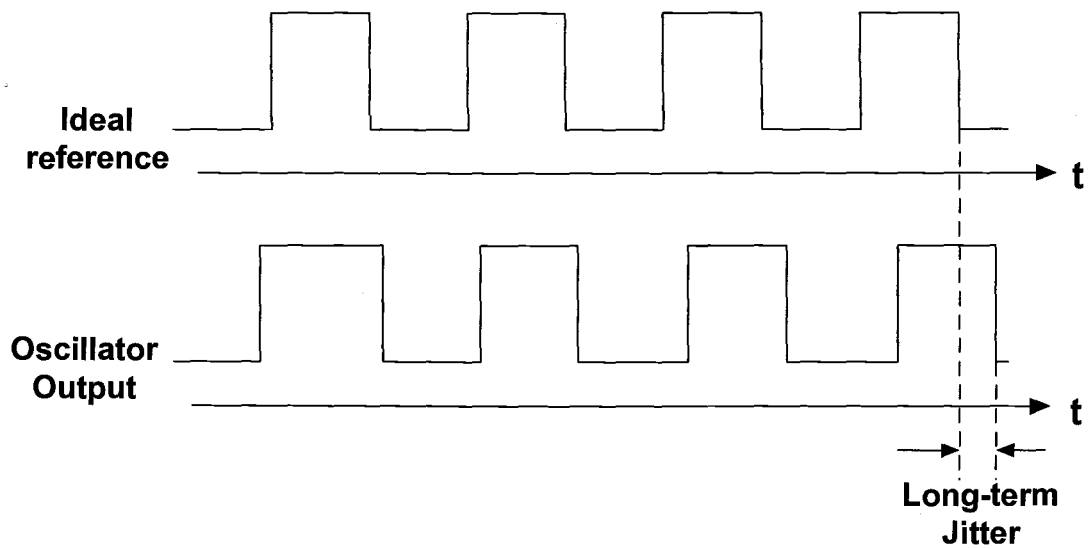

Figure 2.3 Absolute or Long-term jitter

Cycle Jitter

Cycle jitter describes the magnitude of the period fluctuations. But it does not contain information about the dynamics [20].

$$\Delta T_C = \lim_{N\to\infty} \sqrt{\frac{1}{N}\sum_{n=1}^{N} \Delta T_n^2} \tag{2.4}$$

Cycle-to-Cycle Jitter

Cycle-to-Cycle jitter represents the rms difference between two consecutive periods as shown in figure 2.4.

$$\Delta T_{CC} = \lim_{N\to\infty} \sqrt{\frac{1}{N}\sum_{n=1}^{N} (\Delta T_{n+1} - \Delta T_n)^2} \tag{2.5}$$

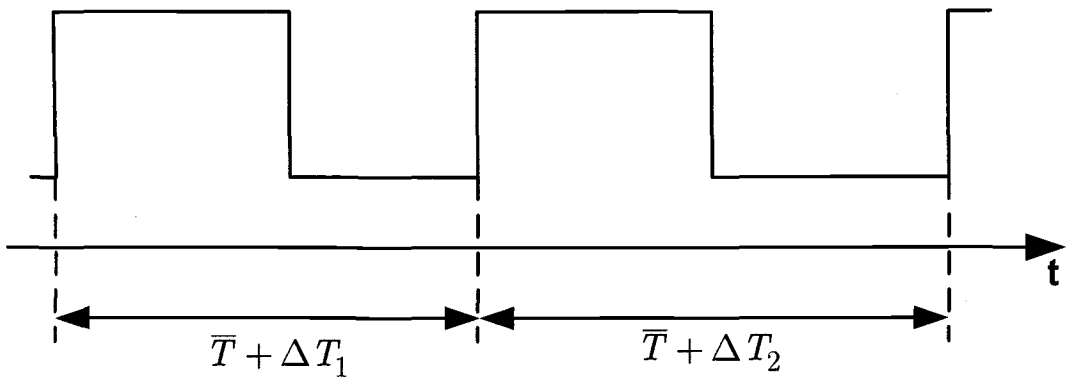

Figure 2.4 Cycle to Cycle Jitter.

Other Jitter Terminology

Timing Jitter

Timing jitter is the uncertainty in the zero-crossing point of a signal. If the total instantaneous phase function of a signal is given by $\phi(t)$ and the ideal zero crossing is at a time nT, then the timing jitter is the time variation of $\phi(nT)$ from nT:

$$\frac{\Delta\phi(nT)}{2\pi f_0} \tag{2.6}$$

Where f_0 (=1/T) is the average frequency of the signal.

Period Jitter

Period jitter (commonly called as jitter in digital systems) is the variation of the period, T. This jitter, J, is defined in terms of timing jitter by: [2]

$$J(n) = \frac{\Delta\phi((n+1)T) - \Delta\phi(nT)}{2\pi f_0} \tag{2.7}$$

2.3 SOURCES OF JITTER

Jitter is caused by thermal noise, instabilities in the oscillator electronics, and external interference through the power supply, ground, and even through the output connections of the oscillator.

Deterministic jitter is created by identifiable interference signals. It is always bounded in amplitude. Deterministic jitter can be generated by cross-talk between adjacent signal traces. This happens when incremental inductance from one conductor converts induced magnetic field from an adjacent signal line into induced current. This induced current increases or decreases the voltage, thus causing jitter.

Deterministic jitter can be caused by EMI radiation. A sensitive signal path can be affected by the magnetic field from an EMI source like power supplies, AC power lines, and RF- signal sources. Like cross-talk, a noise current is induced on the timing signal path which thereby modulates the timing signal voltage level.

Random jitter comes from many sources. Thermal vibrations of semiconductor crystal structure causes mobility to vary depending upon the instantaneous temperature of the material. Another source of random jitter comes from the imperfections due to semiconductor process variation such as non-uniform doping density.

Intrinsic Device Noise

Phase noise and jitter are caused by external sources and intrinsic device noise. External sources can be eliminated with little planning. In a fully optimized design

the main source of timing jitter is the intrinsic device noise; hence this work mainly concentrates on jitter due to intrinsic device noise. Intrinsic device noises are thermal noise and flicker noise.

Thermal Noise

Thermal noise is caused by random thermal motion of electrons. Thermal noise is directly proportional to the absolute temperature and it is not affected by the presence or absence of DC current. The power spectral density of thermal noise is flat with frequency hence it is called white noise.

Flicker Noise

Flicker noise is believed to be due to electrons being trapped and released in gate oxide of MOSFET. The 1/f spectral shape is of the power spectral density is due to the time constants involved in the trap and release mechanism.[10]

At low frequencies flicker noise dominates and at high frequency thermal noise dominates as shown in the figure 2.5.

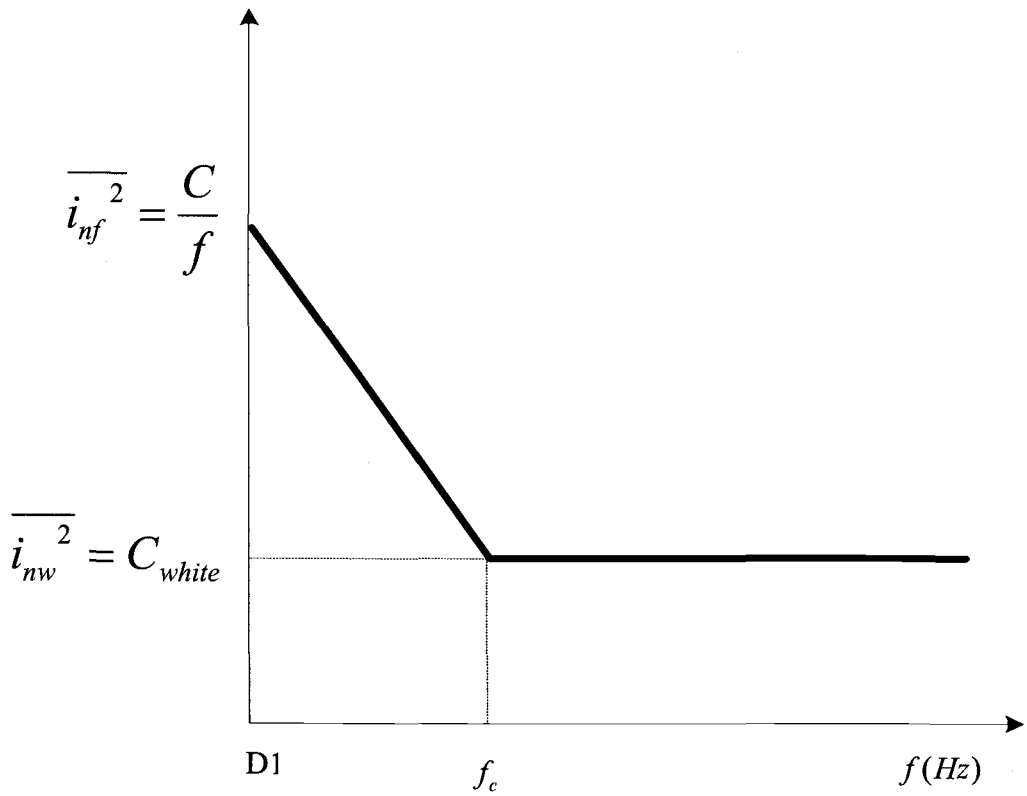

Figure 2.5: Flicker noise dominating at low frequencies.

The point where both thermal and flicker noise intersect is referred to as 1/f corner frequency and in MOS devices it is usually between 2 Mhz and 10 Mhz.

2.4 NOISE MODELING

Understanding MOSFET models

Usually, the selection of the MOSFET model type for use in analysis depends on the electrical parameters critical to the application. When precision is required as for analog data acquisition circuitry, more detailed models such as PSPICE level 6, IDS models or one of the BSIM models (Level 13, 39 or 49) can be used.

For precision modeling of integrated circuits, the BSIM models take into account the variation of model parameters, as a function, of sensitivity of the geometric parameters [14]. The BSIM models also reference a MOS charge conservation model for precision modeling of MOS capacitor effects.

2.4.1 HSPICE VERSUS BSIM3V3

UCB BSIM3V3.X uses a selector parameter called "NOIMOD", where as HSPICE uses a selection parameter called "NLEV". The selector settings choose different thermal and flicker noise equations in each case. Both selection parameters offer the "SPICE2" model and another more advanced model. However, the advanced models are different. BSIM3V3.X uses a model developed by K.K. Hung et al., whereas HSPICE uses an older Gray and Meyer model.

The noise model flag, NLEV, is used to choose different combinations of flicker and thermal noise. The values are indicated in Table 2.2. The H97.1 L49 model does contain the BSIM3V3 noise model. To activate this model instead of the HSpice noise model, we must not set NLEV, and we must also have VERSION=3.1 set. Setting NLEV invokes the HSpice noise model and NLEV overrides noiMod in HSpice simulations.

2.4.2 HSPICE MODELS

Noise parameters

The noise parameters used in this model are given in table 2.1

Name	Description	Default
AF	Flicker noise exponent	1
KF	Flicker noise coefficient Reasonable values for KF are in the range 1e-19 to 1e-25.	0
NLEV	Noise Equation Selector	2
GDSNOI	Channel thermal noise coefficient	1

Table 2.1 Noise parameters in HSpice models.

NLEV

NLEV is a Noise Equation Selector which is used to select different combination of thermal and flicker noise equations and it is shown in Table 2.2.

Nlev	Flicker	Thermal
0	SPICE	SPICE
1	*SPICE	SPICE
2	HSPICE	SPICE
3	HSPICE	HSPICE

* SPICE model, but with $Leff^2$ replaced with Weff*Leff

TABLE 2.2 NLEV settings

Thermal Noise Equations

For NLEV < 3,

$$\text{SPICE2 Channel thermal noise} = \left(\frac{8\kappa T \cdot gm}{3}\right)^{1/2} \tag{2.8}$$

The above formula if used in a linear region gives wrong result. For example, at VDS =0, channel thermal noise becomes zero because gm=0. So we used in our simulation, NLEV =3, Star-Hspice uses a different equation which is valid in both linear and saturation regions.

For NLEV =3,

$$\text{Channel Thermal Noise} = \left(\frac{8\kappa T}{3} \cdot \beta \cdot (vgs - vth) \cdot \frac{1+\alpha+\alpha^2}{1+\alpha} \cdot GDSNOI\right)^{1/2} \tag{2.9}$$

Where

$\alpha = 1 - \frac{vds}{vdsat}$ for Linear Region

$\alpha = 0$ for Saturation Region

Flicker Noise Equations

For NLEV = 0,

$$\text{SPICE2 Flicker Noise} = \left(\frac{KF \cdot Ids^{AF}}{COX \cdot Leff^2 \cdot f}\right)^{1/2} \tag{2.10}$$

For NLEV = 1,

$$\text{*SPICE2 Flicker Noise} = \left(\frac{KF \cdot Ids^{AF}}{COX \cdot Weff \cdot Leff \cdot f}\right)^{1/2} \tag{2.11}$$

For NLEV =2,3

$$\text{Flicker Noise} = \left(\frac{KF \cdot gm^2}{COX \cdot Weff \cdot Leff \cdot f^{AF}} \right)^{1/2} \qquad (2.12)$$

AF and KF are flicker noise parameters.

2.4.3 BSIM3 MODELS

Noise Parameters

The noise parameters used in BSIM3 models and their default values is given in table 2.3

Name	Description	Default
Noia	Noise parameter A	(NMOS) 1e20 (PMOS) 9.9e18
Noib	Noise parameter B	(NMOS) 5e4 (PMOS) 2.4e3
Noic	Noise parameter C	(NMOS) -1.4e-12 (PMOS) 1.4e-12
Em	Saturation field	4.1e7
Af	Flicker noise exponent	1
Ef	Flicker noise exponent	1
Kf	Flicker noise coefficient	0

Table 2.3 Noise parameters in BSIM3 models.

Noise Model Flag

A model flag, noiMod is used to select different combination of flicker and thermal noise models discussed above with possible options described in the Table 2.4 below.

noiMod Flag	Flicker noise model	Thermal noise model
1	SPICE 2	SPICE 2
2	BSIM3V3	BSIM3V3
3	BSIM3V3	SPICE 2
4	SPICE 2	BSIM3V3

Table 2.4 noiMod noise model flag

Thermal Noise Equations

$$\text{SPICE2 Thermal noise} = \left(\frac{8\kappa T(gm+gds+gmb)}{3}\right)^{1/2} \tag{2.13}$$

$$\text{Thermal noise} = \frac{4\kappa_B T\mu_{eff}}{L_{eff}^2}|Q_{inv}| \tag{2.14}$$

Q_{inv} is the inversion channel charge computed from the capacitance models (capMod = 0, 1, 2, or 3).

Flicker Noise Equations

$$\text{SPICE2 Flicker Noise} = \left(\frac{KF\cdot Ids^{AF}}{COX\cdot Leff^2\cdot f^{EF}}\right)^{1/2} \tag{2.15}$$

BSIM3V3 Flicker noise equation

For flicker noise, in addition to the above SPICE models, BSIM3 models also exist, which is developed in UC Berkeley [18].

If Vgs > Vth + 0.1,

$$\text{fn}= \frac{q^2 \kappa T \mu_{eff} I_{ds}}{C_{ox} L_{eff}^2 f^{ef} \cdot 10^8}\left(Noia \cdot \log\left(\frac{N_0 + 2\times 10^{14}}{N_l + 2\times 10^{14}}\right) + Noib \cdot (N_0 - N_l) + \frac{Noic}{2}\left(N_0^2 - N_l^2\right)\right) + \frac{V_{tm} I_{ds} \Delta L_{clm}}{W_{eff} \cdot L_{eff}^2 \cdot 10^8} \cdot \frac{Noia + Noib \cdot N_l + Noic \cdot N_l^2}{\left(N_l + 2\times 10^{14}\right)^2} \tag{2.16}$$

Where V_{tm} is the thermal voltage, μ_{eff} is the effective mobility at the given bias condition, and L_{eff} and W_{eff} are the effective channel length and width, respectively. The parameter N_0 is the charge density at the source side given by

$$N_0 = \frac{C_{ox}(V_{gs} - V_{th})}{q} \tag{2.17}$$

The parameter N_l is the charge density at the drain end given by

$$N_l = \frac{C_{ox}\left(V_{gs} - V_{th} - \min(V_{ds}, V_{dsat})\right)}{q} \tag{2.18}$$

ΔL_{clm} is the channel length reduction due to channel length modulation and given by

$$\Delta L_{clm} = Litl \cdot \log\left[\frac{\frac{V_{ds} - V_{dsat}}{Litl} + E_m}{E_{sat}}\right] \quad (for \quad V_{ds} > V_{dsat}) \tag{2.19}$$

$$= 0 \qquad (otherwise)$$

where $E_{sat} = \frac{2 \times v_{sat}}{\mu_{eff}}$, $Litl = \sqrt{3 X_j T_{ox}}$

Otherwise,

$$\text{Noise density} = \frac{S_{\lim it} \times S_{wi}}{S_{\lim it} + S_{wi}} \tag{2.20}$$

Where, S_{limit} is the flicker noise calculated at $V_{gs} = V_{th} + 0.1$ and S_{wi} is given by

$$S_{wi} = \frac{Noia \cdot V_{tm} \cdot I_{ds}^2}{W_{eff} L_{eff} \cdot f^{ef} \cdot 4 \times 10^{36}} \tag{2.21}$$

2.5 PREVIOUS WORK

The following works have great significance though they are different from our simulation technique. Our simulation analysis is validated using the methods described below in addition to the measurements [6].

2.5.1 JITTER AND PHASE NOISE IN RING OSCILLATORS BY HAJIMIRI AND LEE

Hajimiri and Lee developed a phase noise and jitter model which is based on an analytical method [4] and it is difficult to implement for different oscillators. Also calculating the ISF is difficult and involves lot of approximations. The procedure involved in finding phase noise in terms of impulse sensitive function developed by Hajimiri and Lee is explained below,

We know that the output of a practical oscillator can be modeled with amplitude and phase fluctuations as

$$V_{out}(t) = A(t)^* \, f[\omega_0 \, t + \phi(t)] \tag{2.22}$$

Where the function f is periodic in 2π and A(t) and $\phi(t)$ are fluctuations in amplitude and phase respectively.

Consider a single current source on one of the nodes of a single ended ring oscillator as shown in the Figure 2.6. If the current source consists of an impulse of current with area Δq occurring at time $t = \tau$, then it will cause an instantaneous change in the voltage which is given by

$$\Delta V = \frac{\Delta q}{Cnode} \tag{2.23}$$

where Cnode is the effective capacitance on that node at the time of charge injection.

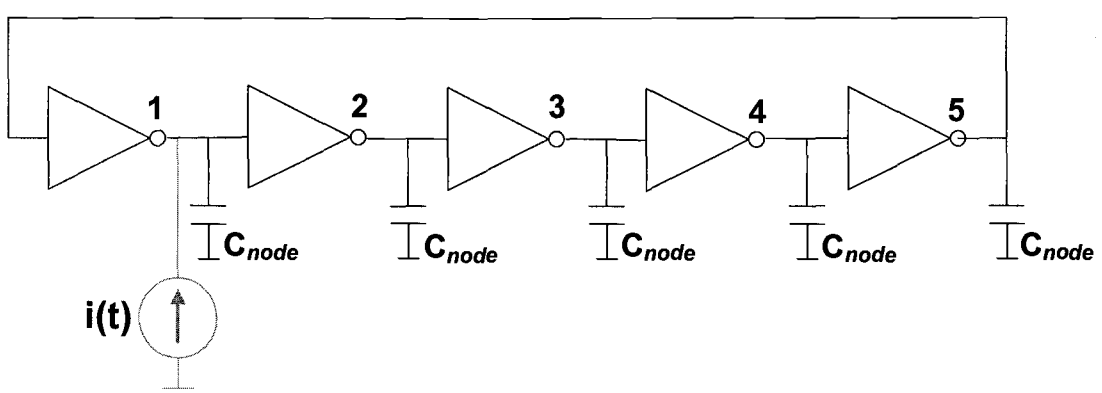

Figure 2.6 Injection of impulse for the calculation of ISF.

This voltage produces a shift in the transition time and since for small ΔV, the change in the phase is proportional to the injected charge,

$$\Delta\phi = \Gamma(\omega_0 t)\frac{\Delta V}{V_{swing}} = \Gamma(\omega_0 t)\frac{\Delta q}{q_{swing}} \tag{2.24}$$

where V_{swing} is the voltage swing across the capacitor. The dimensionless $\Gamma(\omega_0 t)$ is the time-varying proportionality constant and is periodic in 2π. Since $\Gamma(x)$ represents the sensitivity of every point of the waveform to a perturbation, it is called the impulse sensitivity function.

The time dependent impulse response for excess phase is given as [11],

$$h_\phi(t,\tau) = \frac{\Gamma(\omega_0 \tau)}{q_{\max}} u(t-\tau) \tag{2.25}$$

where u(t) is a unit step. The authors calculated $\phi(t)$ in response to any injected current using superposition integral as

$$\phi(t) = \int_{-\infty}^{t} \frac{\Gamma(\omega_0 \tau)}{q_{\max}} i(\tau) d\tau \tag{2.26}$$

The above equation gives phase variation in terms of impulse sensitive function. The relationship between single-sideband phase-noise spectrum due to a white-noise current source is given by [11] as

$$L\{f_{off}\} = \frac{\Gamma_{rms}^2}{8\pi^2 f_{off}^2} \bullet \frac{i_n^2/\Delta f}{q_{\max}^2} \tag{2.27}$$

JITTER

The spacing between transitions varies for practical oscillator and this uncertainty called clock jitter increases with measurement interval ΔT as shown in the Figure 2.7 below.

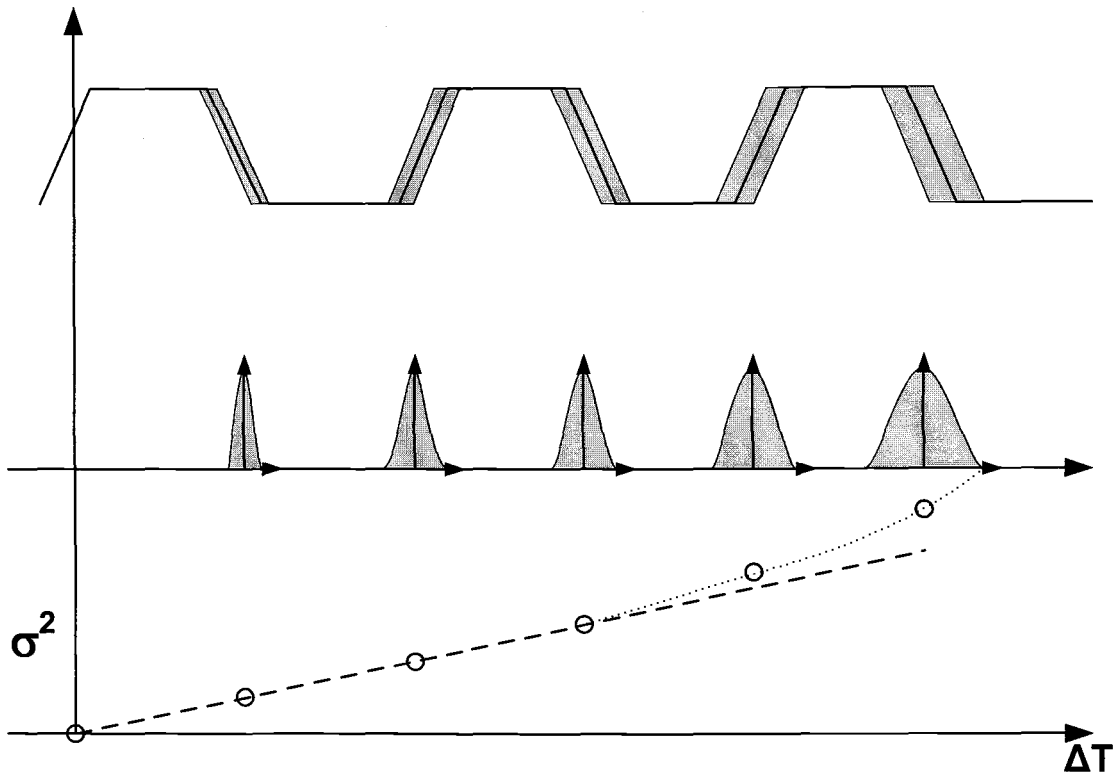

Figure 2.7 Clock jitter increasing with time.

This jitter accumulation occurs because any uncertainty in an earlier transition affects all the following transition. For a ring oscillator with identical stages, the jitter variance is given as $m\sigma_s^2$ for statistical purpose, where m is the number of transitions during ΔT and σ_s^2 is the variance of uncertainty introduced by one stage during one transition. Since m is proportional to ΔT, the standard deviation of the jitter after ΔT is given [12] as

$$\sigma_{\Delta T} = \kappa\sqrt{\Delta T} \tag{2.28}$$

The above equation is for thermal noise because thermal noise of a device is usually modeled as uncorrelated. Substrate and supply noise and 1/f noise are approximated as partially or fully correlated sources. So standard deviations rather than the variances add. Therefore the standard deviation of the jitter after ΔT seconds is proportional to ΔT

$$\sigma_{\Delta T} = \zeta\sqrt{\Delta T} \tag{2.29}$$

where κ and ζ are proportionality constant.

The proportionality constant κ is calculated to be

$$\kappa = \frac{\Gamma_{rms}}{q_{\max}\omega_0}\sqrt{\frac{1}{2}\frac{i_n^2}{\Delta f}} \tag{2.30}$$

Impulse sensitive function for ring oscillator

Hajimiri and Lee actually calculated the ISF by injecting a narrow current pulse into one of the nodes of the oscillator and then measuring the resulting phase shift after a few cycles later in simulation. Assuming symmetry i.e., equality of rising and falling time, Γ_{rms} is estimated as

$$\Gamma_{rms}^2 = \frac{2}{3\pi}\left(\frac{1}{f'_{\max}}\right)^3 \tag{2.31}$$

The approximate expression for Γ_{rms} is obtained by H and L as

$$\Gamma_{rms} = \sqrt{\frac{2\pi^2}{3\eta^3}} \frac{1}{N^{1.5}} \tag{2.32}$$

They also showed that the $1/N^{1.5}$ dependence of Γ_{rms} is independent of the value of η. The Γ_{rms} is primarily a function of N because the effect of variations in other parameters such as q_{max} and device noise, have already been decoupled from $\Gamma(x)$.

We cannot conclude from the above equation that increasing number of stages will reduce phase noise though Γ_{rms} decreases as the number of stages increases, because the number of noise sources as well as their magnitude also increases for a given total power dissipation and frequency of oscillation.

Phase noise and jitter for single ended ring oscillator

The following is an expression for phase noise and jitter for single ended ring oscillator. The maximum total channel noise from NMOS and PMOS device when the input and output are at $V_{DD}/2$ is given by

$$\frac{i_n^2}{\Delta f} = \left(\frac{i_n^2}{\Delta}\right)_N + \left(\frac{i_n^2}{\Delta f}\right)_N = 4kT\gamma\mu_{eff}C_{ox}\frac{W_{eff}}{L}\Delta V \tag{2.33}$$

where

$$W_{eff} = W_n + W_p$$

$$\mu_{eff} = \frac{\mu_n W_n + \mu_p W_p}{W_n + W_p}$$

The final expression for phase noise and jitter for single ended ring oscillator is given as by combining (2.27),(2.32),(2.33).

$$L\{\Delta f\} \approx \frac{8}{3\eta} \cdot \frac{kT}{P} \cdot \frac{V_{DD}}{V_{char}} \cdot \frac{f_0^2}{\Delta f^2} \tag{2.34}$$

$$\kappa \approx \sqrt{\frac{8}{3\eta}} \cdot \sqrt{\frac{kT}{P} \cdot \frac{V_{DD}}{V_{char}}} \tag{2.35}$$

where

P is the total power dissipation given by,

$$P = 2\eta N V_{DD} q_{\max} f_0 \tag{2.36}$$

And the frequency of oscillation f_0 is given by,

$$f_0 \approx \frac{\mu_{eff} W_{eff} C_{ox} \Delta V^2}{8\eta N L q_{\max}} \tag{2.37}$$

Expression for Phase noise and Jitter for Differential Ring Oscillators

Similarly, Hajimiri and Lee derived the phase noise and jitter expression for a differential ring oscillator with resistive load R_L as

$$L_{\min}\{\Delta f\} = \frac{8}{3\eta} \cdot N \cdot \frac{kT}{P} \cdot \left(\frac{V_{DD}}{V_{char}} + \frac{V_{DD}}{R_L I_{tail}} \right) \cdot \frac{f_0^2}{\Delta f^2} \tag{2.38}$$

$$\kappa_{\min} = \sqrt{\frac{8}{3\eta}} \cdot \sqrt{N \cdot \frac{kT}{P} \cdot \left(\frac{V_{DD}}{V_{char}} + \frac{V_{DD}}{R_L I_{tail}} \right)}$$

(2.39)

where

P the total power dissipation is,

$$P = NI_{tail}V_{DD} \tag{2.40}$$

and the Frequency of oscillation f_0 is,

$$f_0 \approx \frac{I_{tail}}{2\eta N q_{\max}} \tag{2.41}$$

In our analysis, we inject the circuit with noise modeled as current sources. Basically these noise current sources can be treated as impulses of random magnitude and phase. Instead of calculating the ISF which involves lot of approximation, in our analysis we allow the HSPICE to calculate the transient with the effect of injected noise current sources. From these transient data, we calculate jitter.

2.5.2 COMPARISON AND ANALYSIS OF PHASE NOISE IN RING OSCILLATORS BY LIANG DAI AND RAMESH HARJANI

They designed, fabricated and measured the phase noise of a ring oscillator. The oscillator output is measured with an HP E4408B spectrum analyzer and SSB phase noise is calculated using the following definition

$$L(\Delta\omega) = \frac{PSD@f = \omega_0 \pm \Delta\omega}{Total\ Signal\ Power} \tag{2.42}$$

This is not a simulation method and they considered only thermal noise for analyzing the phase noise. They modified the Leeson's model which predicts the SSB phase noise of an LC tank oscillator for a 3-stage ring oscillator [15]. Their phase noise for a 3-stage ring oscillator is given by,

$$L(\Delta\omega) \approx 10 \cdot \log\left\{\frac{8F\gamma\kappa T g_{ds0}}{9I_{rms}^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2\right\} \tag{2.43}$$

where I_{rms} is the RMS value for the internal current swing and is a measure of the oscillation signal amplitude, F is the excess noise factor, g_{ds0} is the drain to source conductance at V_{ds} =0, κ is the Boltzmann's constant, and T is the absolute temperature.

For a given center frequency ω_0 and offset frequency $\Delta\omega$, the phase noise is determined by F, I_{rms} and g_{ds0}. Their equations clearly showed that phase noise is affected by two factors namely intrinsic device noise which is determined by F and g_{ds0} and circuit noise sensitivity which is determined by I_{rms}. It can be clearly seen from the above equation that in order to reduce the phase noise, F and g_{ds0} have to be minimized and I_{rms} has to be maximized. The number of devices must be small and the transistor widths cannot be too large for keeping F and g_{ds0} low and |Vgs| of the load devices have to be as small as possible for keeping g_{ds0} low. We know that for a given tail current and oscillation frequency, I_{rms} can only be increased by

improving current switching efficiency and which is only possible with increased voltage swing.

Unfortunately since the designs of these parameters are correlated, it is difficult to optimize the design and lot of trade offs are involved. For example, efficient switching cannot be achieved with very narrow devices.

2.5.3 LEESON'S PHASE NOISE MODEL

The observation that the region close to the carrier has 30 dB decade slope followed by a 20 dB decade slope and a flat noise floor region in an PSD of phase noise versus frequency was first made by D.B. Leeson. He published his linear, time invariant model in 1966 [17].

Leeson's model predicted the phase noise as

$$L(\Delta\omega) = 10 \bullet \log\left\{\frac{2FkT}{P_s}\left[1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]\left(1+\frac{\Delta\omega_{1/f}}{|\Delta\omega|}\right)\right\} \tag{2.44}$$

where P_S is the power of the waveform, F is the empirical excessive noise factor, k is the Boltzmann's constant, T is absolute temperature, Q is the quality factor. The quantity $\Delta\omega_{1/f}$ is the frequency corner between $1/f^3$ and $1/f^2$ regions.

Leeson expressed the phase noise in the $1/f^3$ region as the result of device $1/f$ noise up converting to frequencies close to the carrier, and the phase noise in the $1/f^2$ region as a result of thermal noise.

In the phase noise expression, the spectrum of input phase noise uncertainty has two component, one component is the additive white noise at frequencies around

the oscillator frequency, as well as noise at other frequencies mixed into the pass band of interest by nonlinearities. The other component includes both white noise and flicker noise which has a PSD inversely proportional to frequency.

Since F is an empirical factor, it cannot predict phase noise from circuit noise analysis. Leeson's model assumes no knowledge of circuit topology for the phase noise analysis and so it cannot provide a direction for circuit improvement.

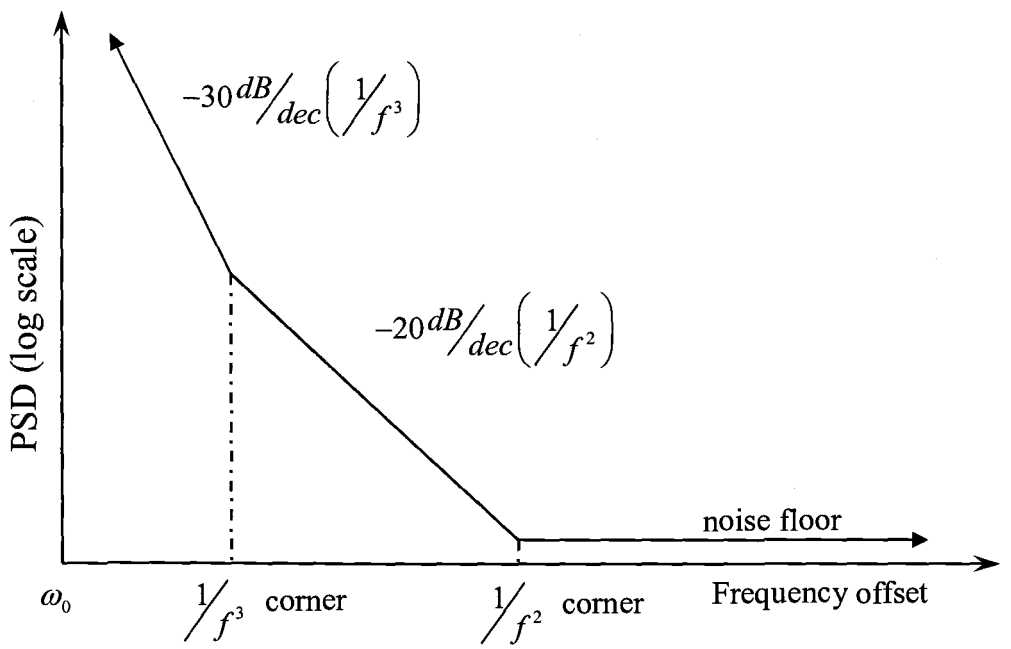

Figure 2.8 Leeson's phase noise model

3. SIMULATION METHOD

3.1 NOISE ANALYSIS PROCEDURE

The procedure involved in doing noise analysis on an oscillator circuit is discussed briefly below.

I. The ring oscillator circuit for a chosen oscillation frequency and desired total power consumption is designed. Then the single stage of ring oscillator is taken and biased to operate in the desired region of operation. For example, a differential inverter with PMOS load can either be used with load being in saturation or triode. The bias voltage for the triode load is modified by adjusting the current source and the current mirror to ensure that the load is in triode. Before doing the noise analysis it is essential to check whether all the frequency and power specifications are met. Then the noise parameters are extracted by doing the noise analysis as given in step II.

II. Extracting Noise parameters "C & C_{white}" from the circuit

For this the common mode (dc) voltage, which is taken from the output of each node when the single stage is working as a ring oscillator, is applied to the inputs and a capacitive load of 1 Farad is connected to the output node as shown in Figure 3.1. A capacitive load of 1 Farad is mainly taken for ease of computing the noise parameter "C & C_{white}" values and basically it provides a path of least resistance to the ground.

A noise analysis is done for the circuit using the .noise statement [14] at the output node with respect to the input. The circuit is connected as shown in the figure 3.1 and the ac voltage is swept from .1 Hz to 1000 Hz. The total output noise voltage at 1 Hz is used for calculating C. The HSPICE output file contains information about both C & C_{white}. The output file contains the thermal and flicker noise contributed by each transistor to the output node.

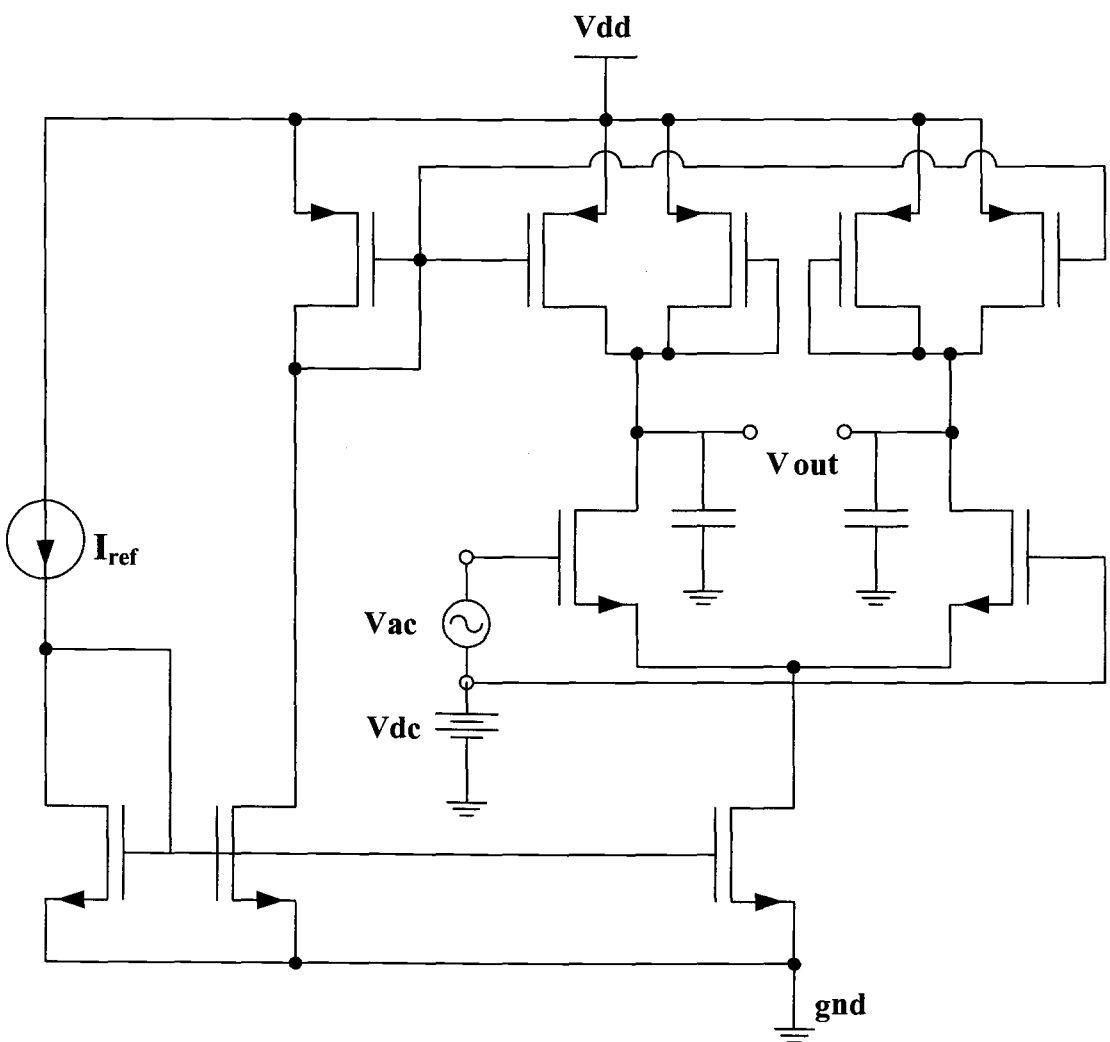

Figure 3.1 Circuit for noise analysis of a differential inverter with Maneatis load.

III. The C value is used to generate flicker noise and the C_{white} value is used to generate white noise using separate Matlab programs shown in Appendix B. The modeling of thermal and flicker noise is discussed in the next sections.

IV. This modeled noise is then injected at the output of each stage of the ring oscillators. For differential inverter ring oscillators, the noise is injected at one of the output node of each stage. Then a transient analysis is done.

V. The useful timing data's are processed from the transient output file and all the jitter values are calculated from the processed data's using another Matlab program shown in Appendix C.

3.2 MODELING OF RANDOM PHASE FLICKER NOISE AND WHITE NOISE

The flicker noise and white noise are modeled [19][13] as

$$\overline{i_{nf}^2} = \frac{C}{f} \tag{3.1}$$

$$\overline{i_{nw}^2} = C_{white} \tag{3.2}$$

where C is the noise power for flicker noise at 1 Hz, C_{white} is the white noise power.

We can use Equation (3.1) and Equation (3.2) to describe different power spectral density values of flicker or white noise in a range of frequencies with a step

frequency, fs. Then the amplitudes of current components, I_{amp} (A), associated with the flicker noise or white noise can be calculated by the following equations:

$$I_{flick} = (\overline{i_{nf}^{\,2}})^{1/2} \quad or \quad I_{white} = (\overline{i_{nw}^{\,2}})^{1/2} \tag{3.3}$$

$$I_{amp} = I_{flick} \bullet (f_s)^{1/2} \quad or \quad I_{amp} = I_{white} \bullet (f_s)^{1/2} \tag{3.4}$$

An ideal sinusoidal current signal can then be expressed as

$$Ind(i) = Iamp(i) \bullet \sin[2\pi f(i)t + \Phi(i)] \tag{3.5}$$

where Φ(i) is the random phase, f is frequency, i is the index of the frequency, which changes from 1 to the end of the frequency range used in the simulation.

The "rand" function in MATLAB is used to create a pseudo-random Φ(i), by using randomly created internal data in the computer. Then, all the individual current components, Ind(i), are summed together to get the random-phase flicker noise, I_{flick}', or random-phase white noise, I_{white}', in the defined frequency range as shown in Figure 3.2 and Figure 3.3.

$$I_{flick}' = \Sigma Ind(i) \quad or \quad I_{white}' = \Sigma Ind(i); \qquad \text{i=range of the frequencies} \tag{3.6}$$

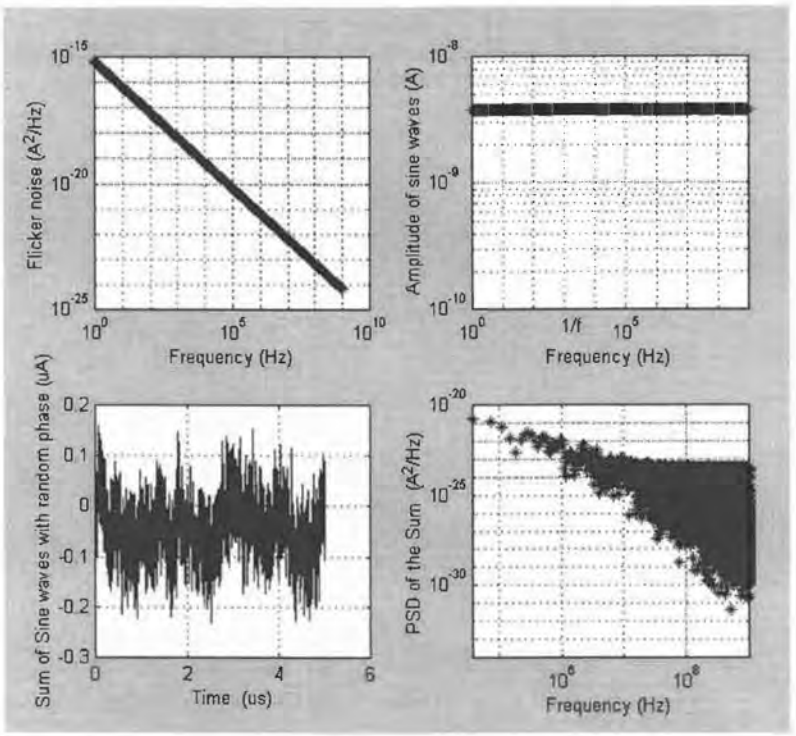

Figure 3.2 Flicker noise plot generated by Matlab

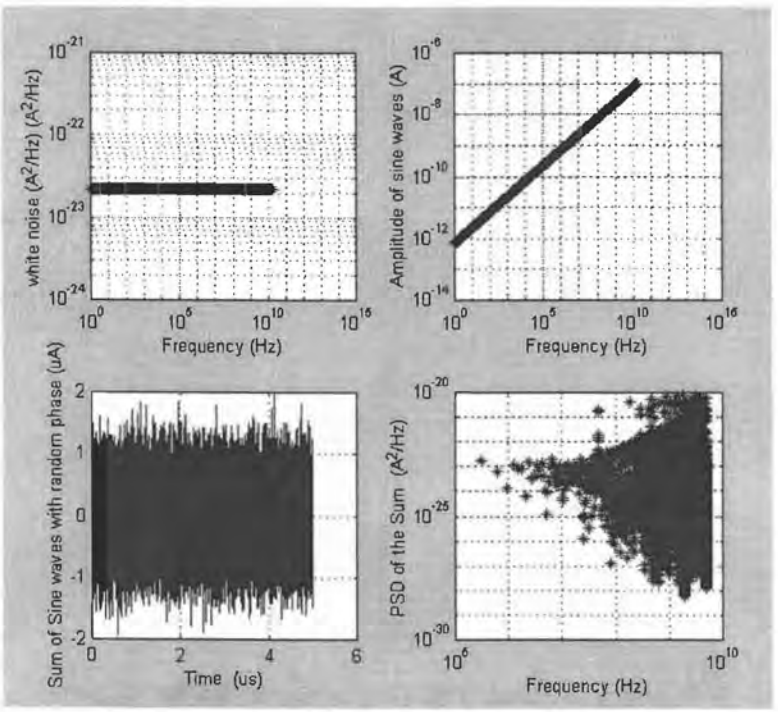

Figure 3.3 White noise plot generated by Matlab

4. RING OSCILLATOR ARCHITECTURE

The simple ring oscillator contains an odd number of cascaded inverters, with the output of the cascade fed back to the input of the inverter chain as shown in the Figure 4.1.

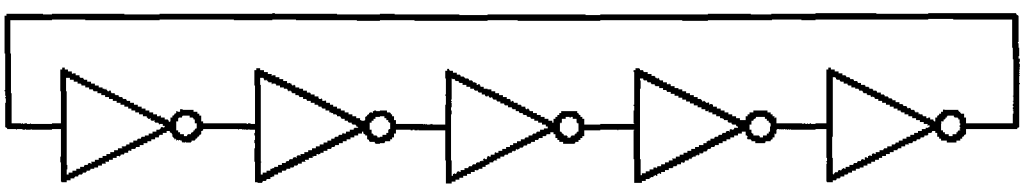

Figure 4.1 Simple ring oscillator configuration

4.1.1 SIMPLE SINGLE ENDED INVERTER

In this configuration, the oscillator frequency is completely dependent on the inherent inverter time delay and is therefore not externally controllable as shown in Figure 4.2. The inverter pair delay is a function of the charge and discharge rate of the driving circuit and the capacitive load C that it drives. In our circuit the aspect ratios of each inverter are adjusted so that $K_N(W/L)_N = K_P(W/L)_P$, for symmetric switching. The oscillation frequency can be approximately given as

$$f_{osc} = \frac{V_{DD} K_N (\frac{W}{L})_N}{8NC} \qquad (4.1)$$

where N is the number of stages in the ring oscillator, V_{DD} is the power supply voltage and C is the capacitance at the output node.

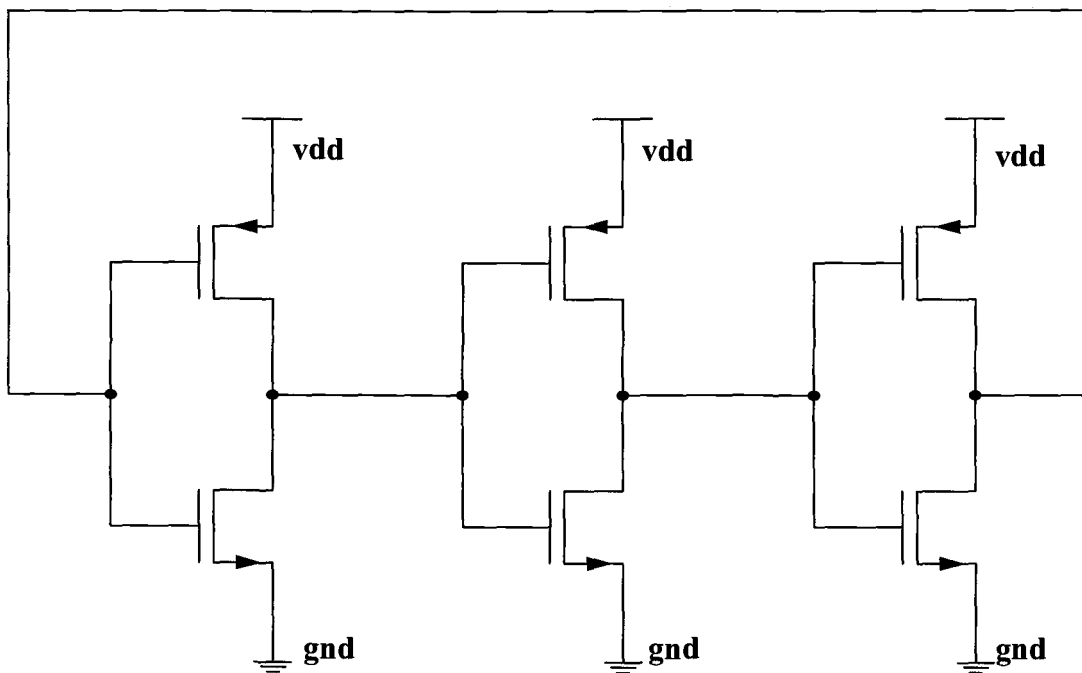

Figure 4.2 Three stage singled ended inverter oscillator

In the single ended ring oscillators, the simplified linear phase noise model does not apply because most of the devices experiences complete switching between on and off states.

4.1.2 SIMPLE DIFFERENTIAL INVERTER WITH RESISTIVE LOAD

Resistive load contribute to white noise but not flicker noise. The load resistance R_L shown in Figure 4.3 is 28.5 Kilo ohm, each resistor contributes $1.463e^{-26}$ sq v/Hz to thermal noise.

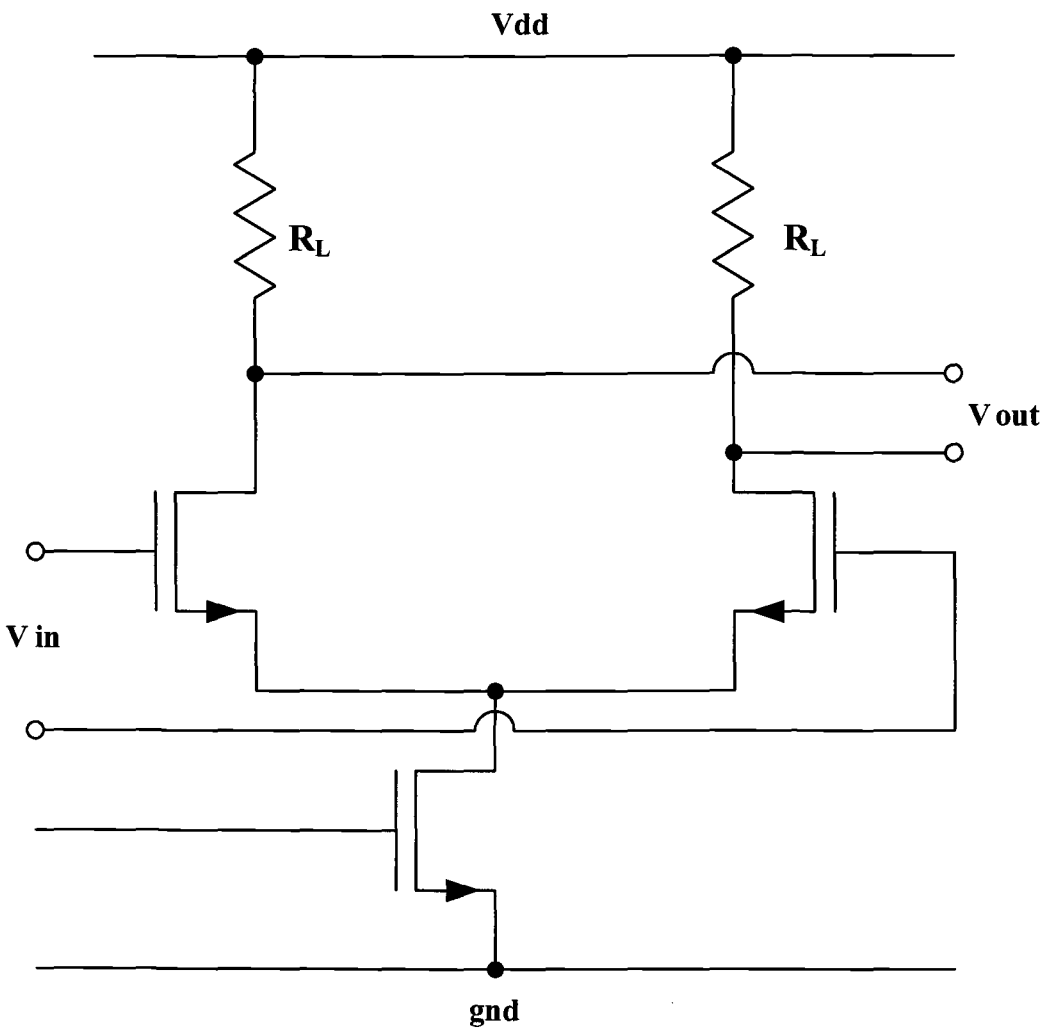

Figure 4.3 Differential inverter with Resistive load

4.1.3 DIFFERENTIAL INVERTER WITH PMOS SATURATION AND TRIODE LOAD

The figure 4.4 shows a differential inverter with PMOS load in saturation or triode load. The load is operated in saturation region or triode region by adjusting the bias voltage.

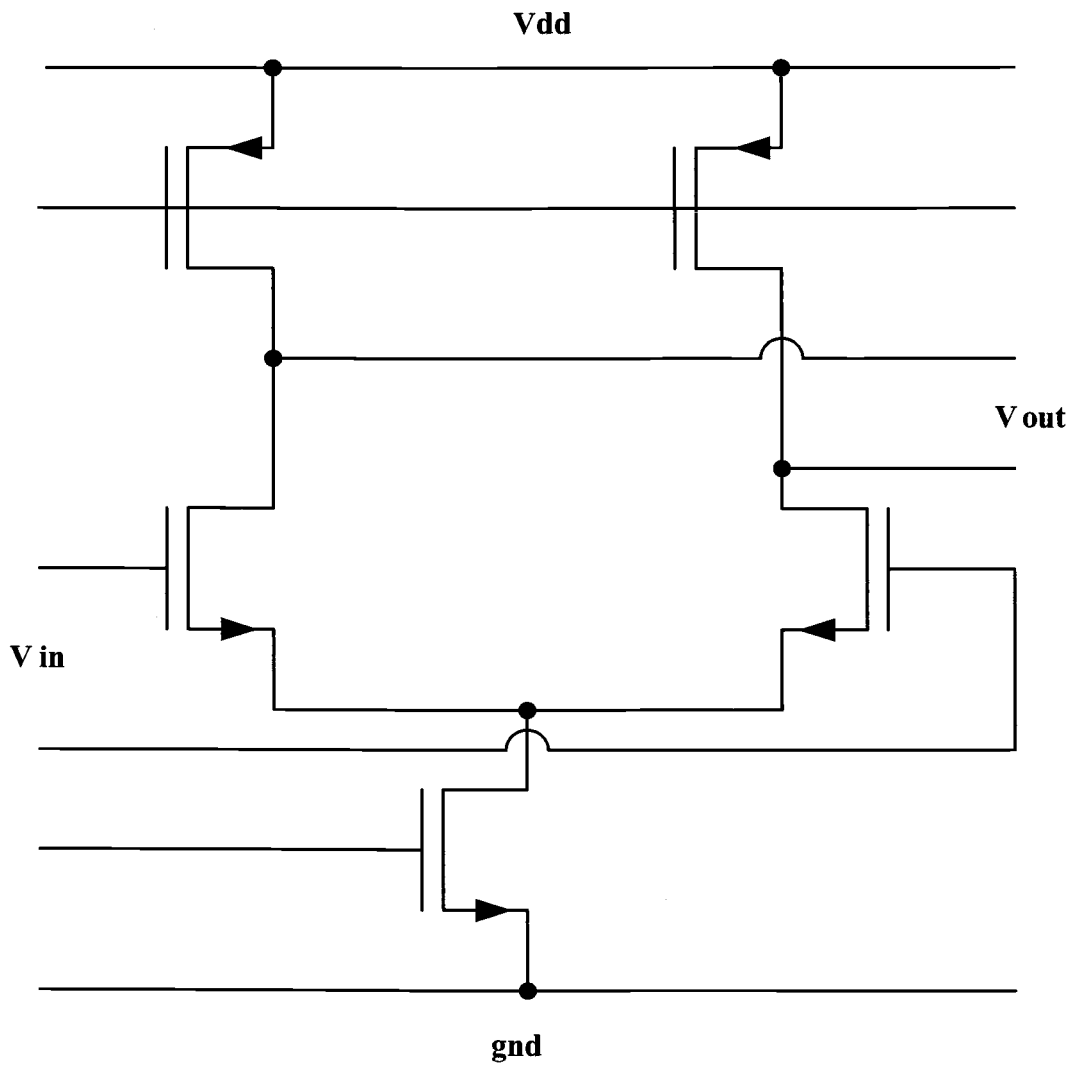

Figure 4.4 Differential inverter with PMOS load.

4.1.4 DIFFERENTIAL INVERTER WITH MANEATIS LOAD

The delay stage is implemented with a fully differential pair and combined PMOS load [1] as shown in Figure 4.5. The load transistors are equally sized to provide more linear I-V characteristics. A sample HSpice code is shown in Appendix A. If only the diode connected load is present, the load consumes voltage headroom, thus creating a trade-off between the output voltage swing, the voltage gain, and the input CM range. The idea of Maneatis load shown in Figure 4.5 and Figure 4.6 is to lower the gm of the load devices by reducing their current rather than their aspect ratio. The PMOS load transistors carry 80 % of drain current of input transistor; the current through the diode connected PMOS transistors is reduced by a factor of 5 [16].

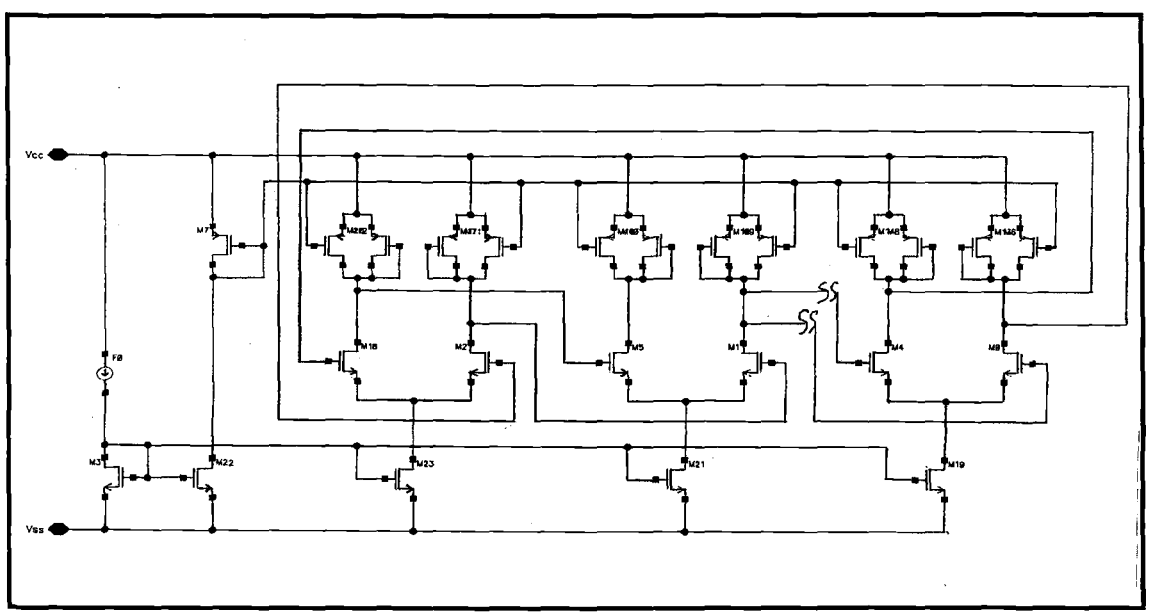

Figure 4.5 Three stage differential inverter with Maneatis load.

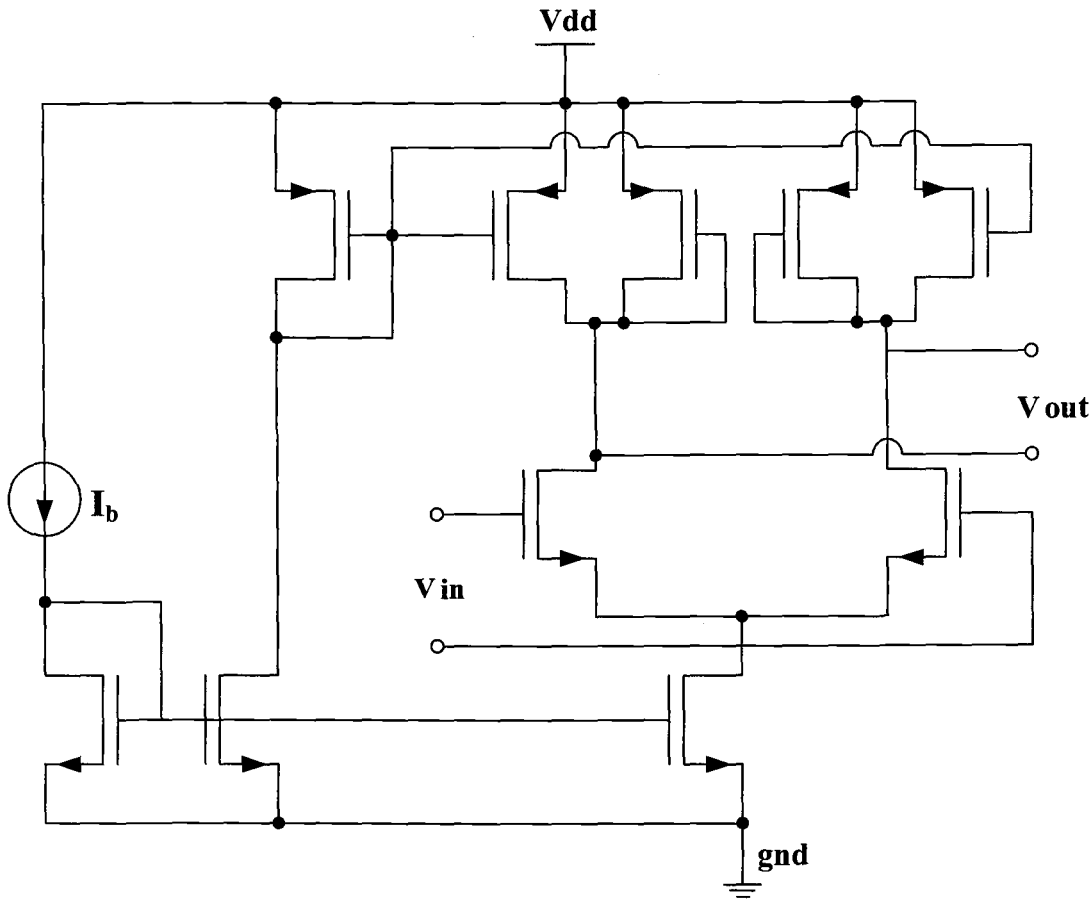

Figure 4.6 Single stage of a three stage differential inverter with Maneatis load

4.2 DESIGN CONSIDERATION TO MINIMIZE JITTER

To minimize jitter in ring oscillators, a good understanding of its mechanism is essential. So, our objectives were to first compare and analyze the phase noise/jitter in different ring oscillators. Totally five different ring oscillator configurations were analyzed. Two types of single-ended inverters and three different types of differential inverters were used. The Current-starved inverter is a VCO as shown in Figure 4.7. The transistor above and below the normal inverter transistor acts as current source and by controlling this current, we can vary the frequency of the oscillator.

Two types of Single-ended Inverters which are used as ring oscillators are,

1. Simple Inverter

2. Current–starved Inverter

.

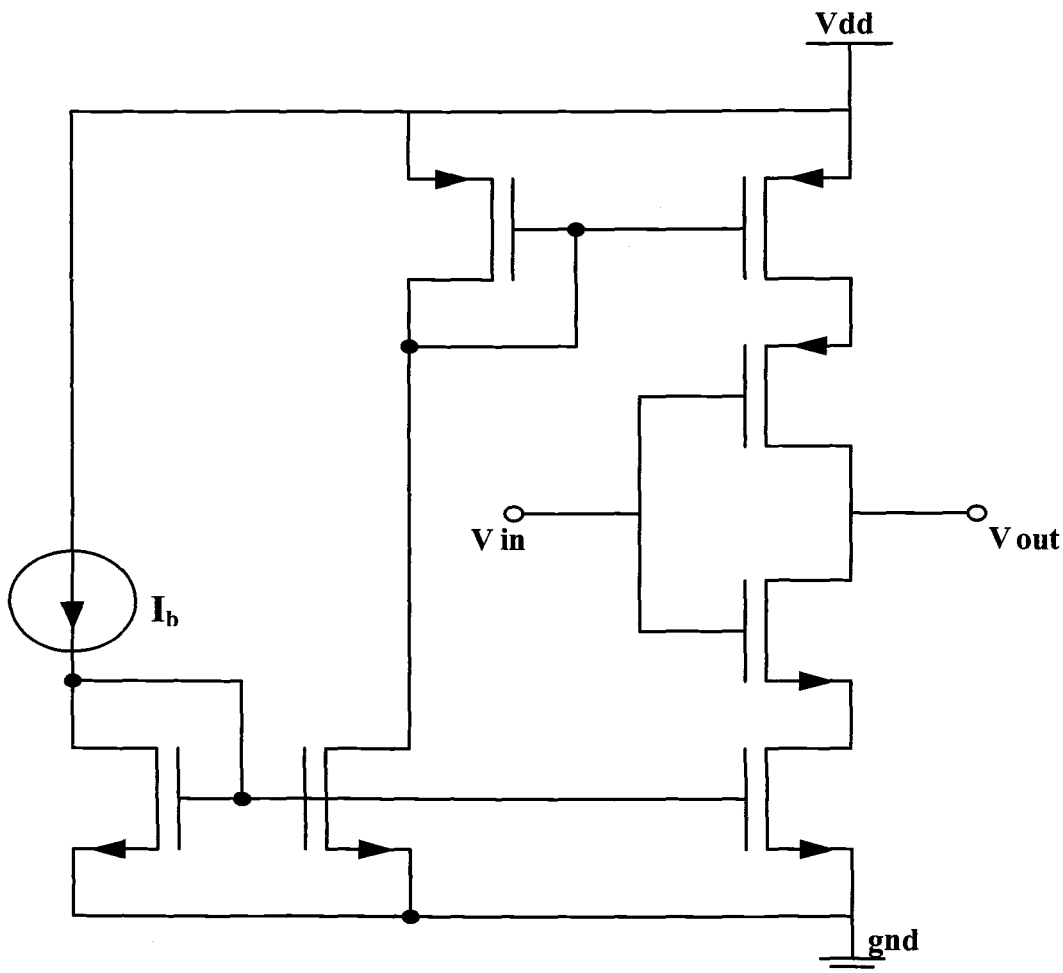

Figure 4.7 Single stage of a current-starved inverter oscillator

The current-starved inverter ring oscillator had better jitter performance than differential inverters with PMOS load in saturation region and PMOS load in triode region.

Three types of Differential inverters are used as ring oscillators,

1. The Differential inverter with Maneatis load
2. The Differential inverter with PMOS load in the saturation region
3. The Differential inverter with PMOS load in the triode region

The jitter performance of different architecture is compared, by keeping the oscillation frequency and total power of each circuit approximately equal.

Advantage of Differential Operation

An important advantage of a ring oscillator with differential inverter is higher immunity to environmental noise and high linearity. Another useful property of differential signaling is the increase in maximum achievable voltage swings. Generally, large signal swing and sharp transition improve the noise performance. Fully differential signals help reject noise from the substrate as well as from pass-transistor switches turning off in switched-capacitor applications.

4.3 SIMULATION OF TIMING JITTER IN RING OSCILLATORS

4.3.1 PERFORMANCE OF SINGLE ENDED & DIFFERENTIAL INVERTER WITH RESISTIVE LOAD

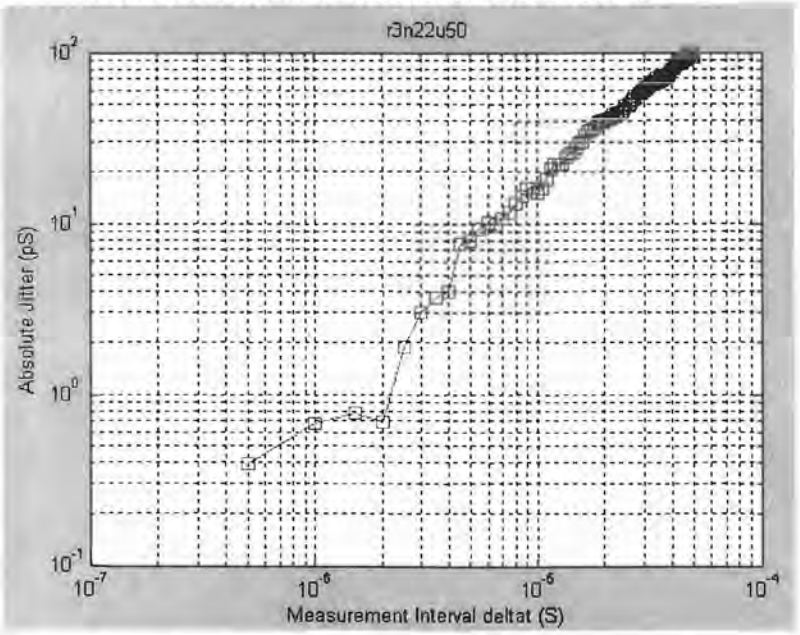

Figure 4.8 Absolute jitter for differential inverter with resistive load.

The Figure 4.8 shows that absolute jitter varies $t^{0.5}$ times measurement interval when injected with white noise. When injected with white noise of different magnitude into both the circuits and simulated using HSPICE, it was observed that the differential inverter had better jitter performance than the single ended inverter. The absolute jitter was approximately 10 times more for the single ended inverter as shown in Table 4.1.

3-stage inverter (white)	Single ended	Differential
Noise 2.112e-18	1100ps	500ps
Noise 2.112e-20	110ps	8ps
Noise 2.112e-22	13ps	1.4ps

Table 4.1 Absolute Jitter Performance of Single Ended and Differential Inverter

The Table 4.1 clearly shows that singled ended inverters are more sensitive to noise than differential inverters. Single ended inverters have small magnitude of flicker and white noise due to the smaller number of transistors. But their performance is not very good compared to the magnitude of difference in the output noise voltage. Since, most of the time, oscillators are usually employed in system-on-chip along with other digital circuits, oscillators less sensitive to switching and substrate noise are desired. Hence, it is advisable to use differential inverters rather than single ended inverters.

4.3.2 PERFORMANCE OF DIFFERENTIAL INVERTER WITH DIFFERENT LOADS

To compare and analyze differential inverters with different loads, the frequency and power consumption of different architectures were kept approximately equal at 1 GHz and 5.7 milliwatts.

It was observed that the ring oscillator with saturation load has the largest voltage swing and fastest transition, while the ring oscillator with triode load has the smallest voltage swing and slowest transitions. On the other hand, the oscillator with the saturation load has a more non-linear behavior than the other two loads. The absolute jitter of differential inverter with different load is shown in Figure 4.9, Figure 4.10, Figure 4.11.

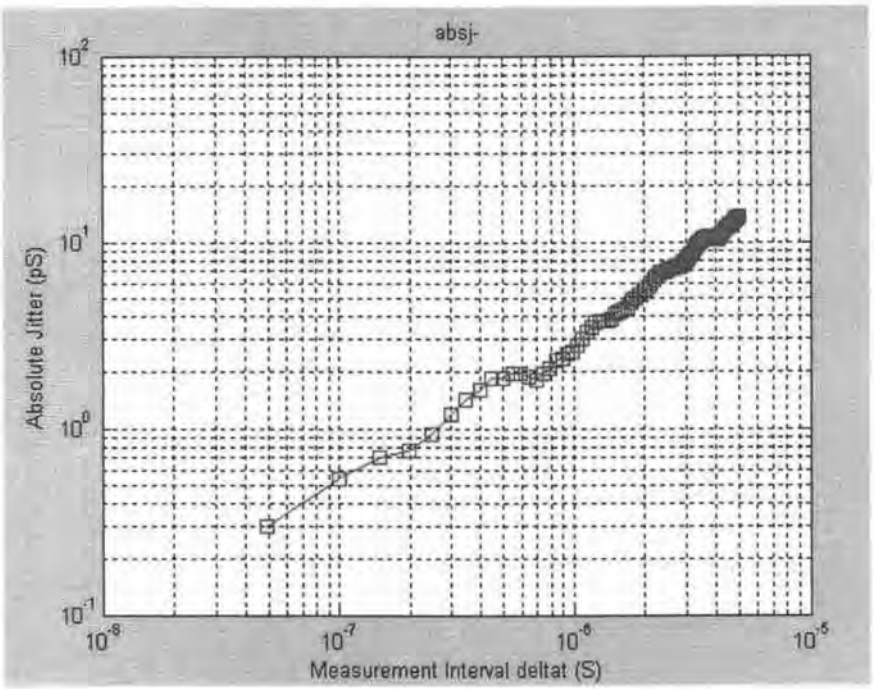

Figure 4.9 Absolute jitter plot of a 3-stage ring oscillator with Maneatis load

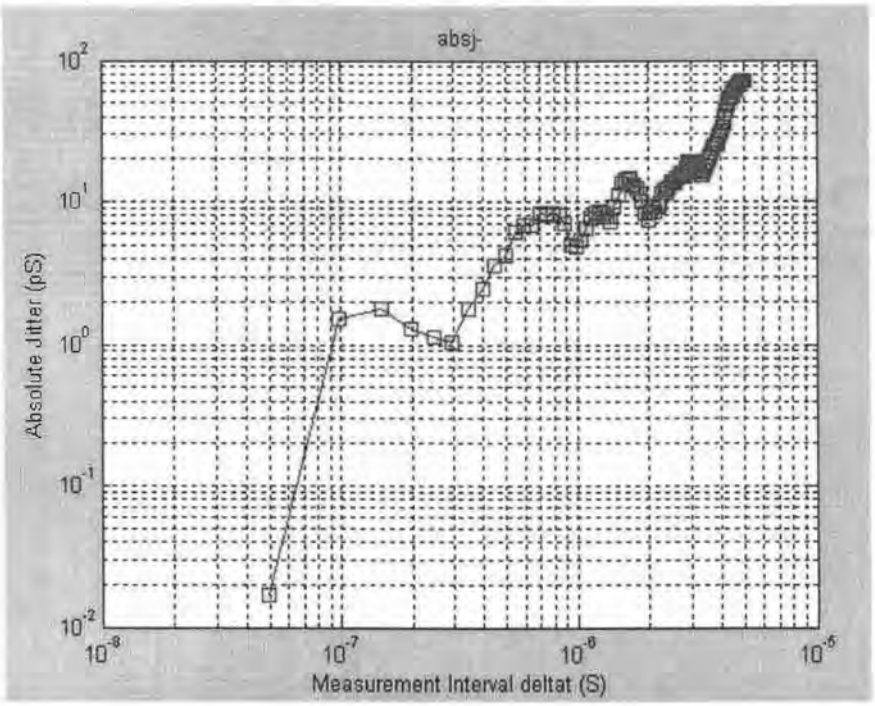

Figure 4.10 Absolute jitter plot of a 3-stage ring oscillator with PMOS load in saturation region

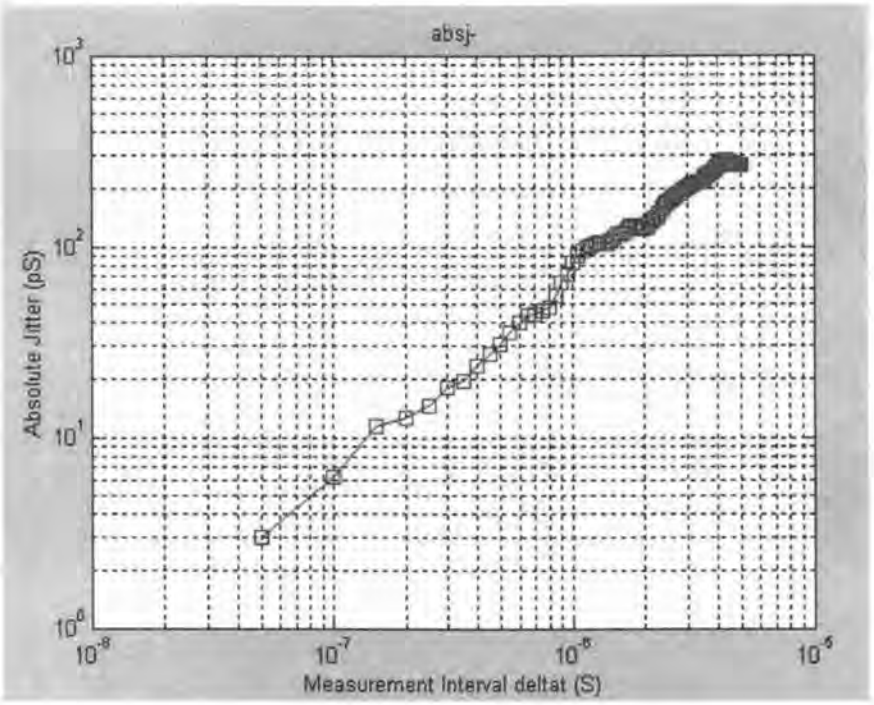

Figure 4.11 Absolute jitter plot of a 3-stage ring oscillator with PMOS load in triode region

The Table 4.2 clearly shows that the differential inverter with Maneatis load clearly out performs the differential inverter with the PMOS load in saturation region as well as the PMOS load in triode region. The absolute jitter plot of the differential inverter are shown in Table 4.2 is shown in figure 4.9, figure 4.10, figure 4.11. Differential inverter with maneatis load had only 13.6 ps of absolute jitter at 5 micro second measurement interval, where as differential inverter with PMOS load in saturation region had 72 ps and differential inverter with PMOS load in triode region had 265 ps.

Diff. Inverter With	Absolute Jitter (ps)	Cycle Jitter (ps)	Cycle to Cycle Jitter (ps)	Peak to Peak Jitter (ps)
Maneatis Load C=15.266E-18	@3μs = 8 @5μs = 13.6	@3μs = 6.7E-3 @5μs = 6.9E-3	@3μs = 8.7E-3 @5μs = 8.7E-3	@3us = 0.047 @5μs = 0.047
Saturation Load C=3.465E-17	@3μs = 20 @5μs = 72	@3μs = 0.03 @5μs = 0.0353	@3μs = 1.2E-2 @5μs = 1.2E-2	@3μs = 0.19 @5μs = 0.2
Triode Load C=1.820E-17	@3μs = 200 @5μs = 265	@3μs = 0.095 @5μs = 0.09	@3μs = 0.019 @5μs = 0.019	@3μs = 0.43 @5μs = 0.44

Table 4.2 Absolute jitter performance of differential inverters when injected with flicker noise.

The Table 4.3 and Table 4.4 confirms that the linear characteristics provided by the Maneatis load result in better phase noise performance. The Table 4.3 also shows that triode load has the worst phase noise performance because it has the smallest internal signal swing. The Table 4.4 also clearly shows that the differential inverter with PMOS load in saturation region has worst jitter performance due to white noise due to its non-linear behaviour. The worst absolute jitter performance of differential inverter with PMOS triode load due to flicker noise can be observed in Figure 4.12 and the worst absolute jitter performance of differential inverter with PMOS load in saturation can be observed in Figure 4.13. The better performance of differential inverter with Maneatis load can be observed in both Figure 4.12 and Figure 4.13.

Inverter Circuit	Absolute Jitter (ps)				Cycle Jitter (ps)		Cycle to Cycle Jiiter (ps)		Peak to Peak Jitter (ps)	
	2 μs	3 μs	4 μs	5 μs	3 μs	5 μs	3 μs	5 μs	3 μs	5 μs
Maneatis Load	13	20	27	32.5	0.0143	0.0143	0.019	0.019	0.1	0.1
PMOS Sat. Load	60	90	110	125	0.035	0.034	0.012	0.012	0.105	0.11
PMOS Triode Load	75	170	240	280	0.062	0.06	0.0108	0.0108	0.12	0.12
Modeled RC Load	43	70	90	110	0.0227	0.0227	0.00725	0.00725	0.033	0.033
Current Starved	35	50	70	90	0.0186	0.01865	0.0055	0.0055	0.0255	0.0255
Resistive load	55	75	90	100	0.0245	0.022	0.006	0.006	0.055	0.065
Simple Single ended	25	35	50	60	0.013	0.013	0.009	0.009	0.028	0.03

Table 4.3 Jitter values of 7 different circuits injected with flicker noise

Inverter Circuit	Absolute Jitter (ps)				Cycle Jitter (ps)		Cycle to Cycle Jitter (ps)		Peak to Peak Jitter (ps)	
	2 μs	3 μs	4 μs	5 μs	3 μs	5 μs	3 μs	5 μs	3 μs	5 μs
Maneatis Load	22	34	45	55	0.135	0.135	0.2	0.2	0.95	0.95
PMOS Sat. Load	65	100	140	165	0.09	0.09	0.12	0.12	0.62	0.62
PMOS Triode Load	15	17	22	25	0.18	0.18	0.208	0.208	1.1	1.23
Modeled RC Load	55	80	120	140	0.0518	0.0518	0.062	0.062	0.32	0.32
Current Starved	40	65	88	110	0.048	0.048	0.07	0.07	0.27	0.29
Resistive load	35	50	70	84	0.0552	0.0552	0.059	0.059	0.375	0.375
Simple Single ended	30	45	60	74	0.0225	0.0225	0.0243	0.0244	0.125	0.125

Table 4.4 Jitter values of 7 different circuits injected with white noise

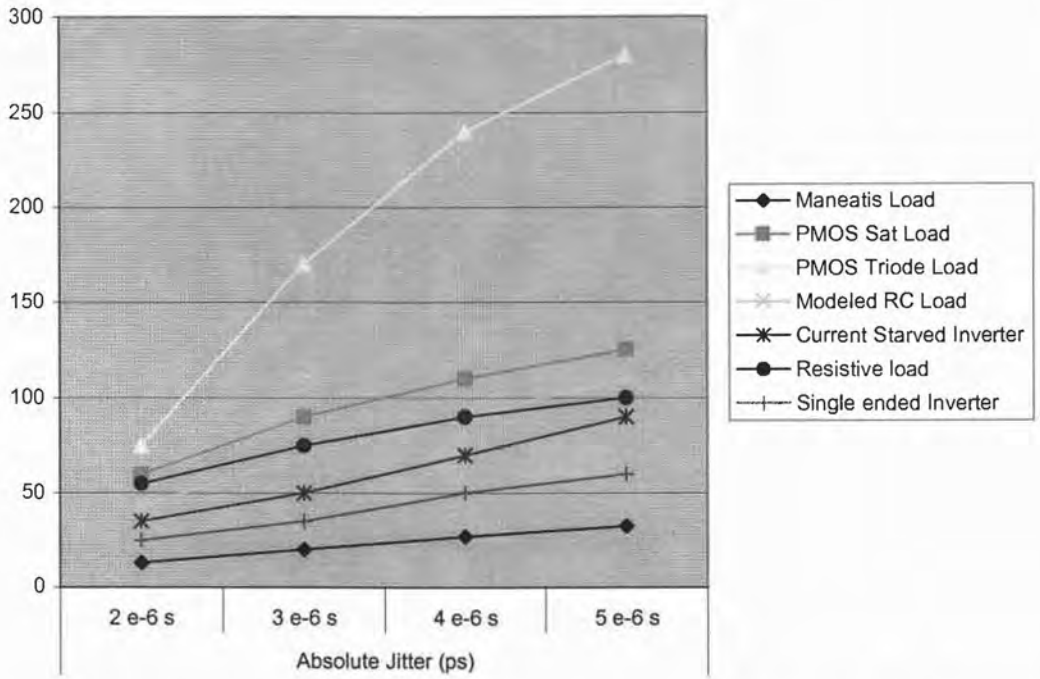

Figure 4.12 Absolute Jitter Excel plot of 7 different circuits injected with flicker noise

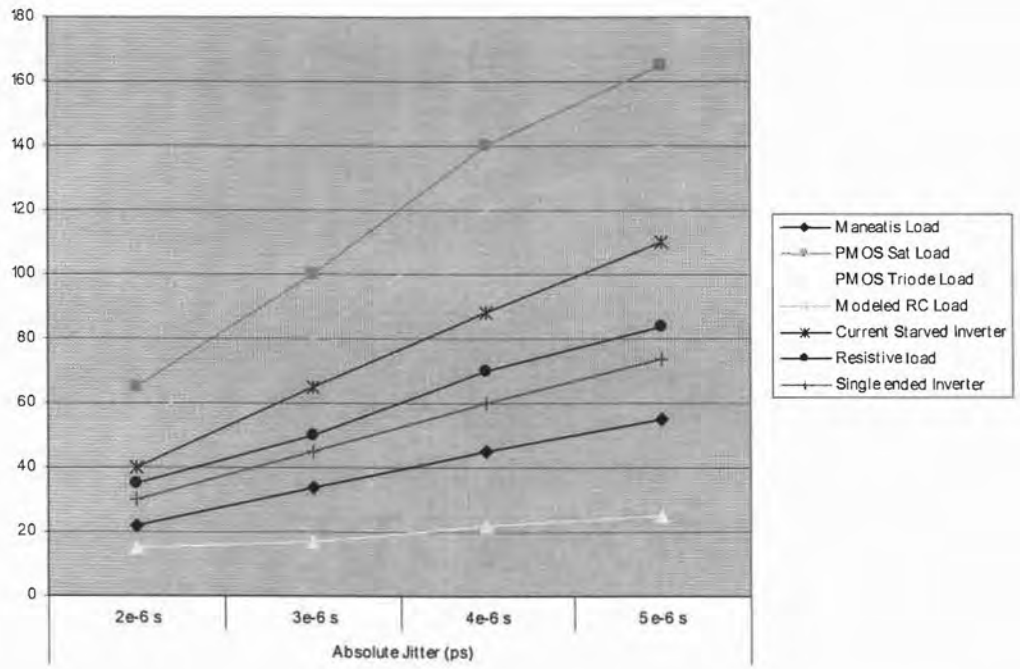

Figure 4.13 Absolute Jitter Excel plot of 7 different circuits injected with white noise

5. CONCLUSION AND FUTURE WORK

5.1 CONCLUSION

The differential inverter with a Maneatis load had the lowest jitter; hence it is more suitable to be used as a clock generator. When injected with flicker noise, the differential inverter with Maneatis load had an absolute jitter of approximately 10ps for a running time of 5μs. Our simulation results confirm that the linear characteristics provided by the Maneatis load improve phase noise and jitter performance. Our simulation shows that the variation of absolute jitter due to flicker noise has t dependence and that variation due to white noise has $t^{0.5}$ dependence which is consistent with accepted theory [3,4].

The objective of the research, which was to gain insight into the design of oscillator with minimum jitter without actual fabrication, was achieved. It was desirable to choose the circuit which has less jitter due to both flicker noise and white noise. Maneatis load had 32.5 ps absolute jitter due to flicker noise and 55 ps absolute jitter due to white noise at 5 μs as shown in Table 4.4 and Table 4.5.

5.2 FUTURE WORK

Using this jitter simulation technique, an analytical formula for jitter due to flicker noise can be developed in the future. Also techniques to convert jitter into phase noise and vice versa can be developed. New tools for optimizing jitter or phase noise in oscillators can be developed by understanding the design tradeoff involved.

BIBLIOGRAPHY

[1] J. G. Maneatis, "Low-jitter process-independent DLL and PLL based on self-biased techniques," IEEE J. Solid-State Circuits, vol.31, pp.1723-1732, November 1996.

[2] T. J. Yamaguchi, M. Soma, D. Halter, J. Nissen, R. Raina, M. Ishida, and T. Watanabe, "Jitter Measurements of a Power-PC Microprocessor Using a Analytic Signal Method," Proc. International Test Conference, pp.955-964, October 2000.

[3] T. C. Weigandt, B. Kim and P. R. Gray, "Analysis of timing jitter in CMOS ring oscillators", Proc. ISCAS, vol. 4, pp. 27-30, June 1994.

[4] A. Hajimiri, S. Limotyrakis, and T. Lee, "Jitter and phase noise in ring oscillators", IEEE J. Solid-State Circuits, vol. 34, pp.790-804, June 1999.

[5] Texas Instruments Application notes 2001: Sine-Wave Oscillator, Ron Mancini and Richard Palmer HPL (Dallas).

[6] C.W. Zhang and L. Forbes, "Timing Jitter In A 1.35-Ghz Single-Ended Ring Oscillator," Proc. 2002 Midwest Symp. on Circuits and Systems, Tulsa OK, pp. 308-311, August 2002.

[7] A. Rofourgan, J. Rael, M. Rofourgan, and A. Abidi, "A 900MHz CMOS LC-Oscillator with quadrature outputs," ISSCC Dig. Tech. Papers, San Francisco, CA, pp. 392-393, February 1996..

[8] J. Craninckx and M. Stayeart, "A 1.8 GHz low-phase noise CMOS VCO using optimized hollow spiral inductors," IEEE J. Solid State Circuits, vol. 32, pp. 736-744, May 1997.

[9] P. Basedau and Q.Huang, "A 1GHz, 1.5 V monolithic LC oscillator in 1μm CMOS," in Proc. European Solid-State Circuits Conference, Germany, pp. 172-175, 1994.

[10] P. R. Gray and R. G. Meyer, Analysis and Design of Analog Integrated Circuits, John Wiley and Sons, 1993.

[11] A. Hajimiri and T.H. Lee, " A general theory of phase noise in electrical oscillators," IEEE J. Solid-State Circuits, vol. 33, pp. 179-194, Feb. 1998.

[12] J. McNeil, "Jitter in ring oscillators," IEEE J. Solid-State Circuits, vol. 32, pp. 870-879, June 1997.

[13] L. Forbes, M. Cheng and J.Zhou, "Simulation of phase noise generated by white noise in a 1.7 GHz CMOS LC oscillator," IEE Electronics Letters, vol.36, no.23, pp.1909-1911, 2000.

[14] HSpice Manual release 2001.

[15] L. Dai and R. Harjani, "Comparison and Analysis of Phase Noise in Ring Oscillators," ISCAS 2000, Geneva, Switzerland, May 2000.

[16] B. Razavi, Design of Analog CMOS Integrated Circuits, International Edition, McGraw-Hill, 2001.

[17] D. B. Leeson, "A simple model of feedback oscillator noise spectrum," Proc. IEEE, vol. 54, pp. 329-330, February 1966.

[18] W. Liu et al, BSIM3V3.2.2 MOSFET Model Users' Manual, University of California, Berkeley 1999.

[19] D. Xie, and L. Forbes, "Phase noise on a 2-GHz CMOS LC Oscillator", IEEE Trans. On Computer-Aided Design of Integrated Circuits and Systems, vol. 36, pp. 1909-1911, 2000.

[20] F. Herzel and B. Razavi, "A Study of Oscillator Jitter Due to Supply and Substrate Noise," IEEE Trans. On Circuits and Systems-II, Analog and Digital Signal Processing, vol. 46, January 1999.

APPENDICES

APPENDIX A – HSPICE CODE

HSPICE CODE FOR DIFFERENTIAL INVERTER WITH MANEATIS LOAD – TRANSIENT ANALYSIS

```
* Differential inverter with Maneatis loads
****ring oscillator

*POWER SUPPLIES

Vcca 100 0 dc=3.3v


*CURRENT SOURCE
Iref 100 vb1 150ua


*CURRENT MIRROR

Mn2 vb1 vb1 0 0 CMOSN w=20u  l=2u m=2


*BIAS FOR MANEATIS LOAD

Mn3 vb7 vb1 0 0 CMOSN w=20u  l=2u m=2

Mp7 vb7 vb7 100 100 CMOSP w=7.2u  l=0.36u m=2

* SUBCIRCUIT STARTS


.subckt drml vin1 vin2 vout1 vout2 100 0  vb1 vb7

*INPUT TRANSISTORS

Mn11 vout1 vin1 200 0 CMOSN w= 5.76u l=0.36u m=2
Mn12 vout2 vin2 200 0 CMOSN w= 5.76u l=0.36u m=2

*Active Loads

Mp0 vout1 vb7 100 100 CMOSP w= 7.2u  l=0.36u

Mp1 vout1 vout1 100 100 CMOSP w= 7.2u  l=0.36u

Mp4 vout2  vout2 100 100 CMOSP w= 7.2u  l=0.36u

Mp5 vout2  vb7 100 100 CMOSP w= 7.2u  l=0.36u

*ISS

Mn6 200  vb1  0 0 CMOSN w= 20u l=2u m=2

.ends drml

*THREE STAGE
```

```
x1   1 2 3 4 100 0   vb1 vb7 drml

x2   3 4 5 6 100 0   vb1 vb7 drml

x3   5 6 1 2 100 0   vb1 vb7 drml


*FLICKER NOISE FILE
.inc fmla.dat
.inc fmlb.dat
.inc fmlc.dat

.op
.option post
.inc mt38n8cs.txt

.ic V(1)=2 V(2)=1
.options ACCURATE=1 INGOLD=1 NUMDGT=10

.tran 1e-12 5us start=10ns
.print tran v(1,2)

.end
```

****

APPENDIX B – MATLAB FLICKER NOISE GENERATION

%MATLAB PROGRAM FOR FLICKER NOISE GENERATION

```
% Random-Phase Flicker Noise Simulation by Matlab

clear all; close all

%Cf VALUE FOR MANEATIS LOAD
c=1.6708e-17;

% Frequency changes from 1Hz to 1000MHz in logspace

f=logspace(0,9,1000);
nf=length(f);
deltaf=diff(f);
f(:,nf)=[ ];

rand('state',sum(100*clock));          % rand function in MATLAB

x=rand(length(f),1);

flicker=c./f;
Ind=flicker.^0.5;              % unit=A/Hz^0.5

% Amplitude of drain current noise
Iamp=Ind.*deltaf.^(1/2);              % unit=A

% Save data into files for MS EXCEL use
f1=f'; flicker1=flicker'; Iamp1=Iamp';
outputdata1=[f1 flicker1]; outputdata2=[f1 Iamp1];
save figure1.dat outputdata1 -ascii
save figure2.dat outputdata2 -ascii

subplot(2,2,1)
loglog(f,flicker,'-*'); grid on;
%title('Modeling flicker noise with KF= ');
xlabel('Frequency (Hz)');
ylabel('Flicker noise (A^2/Hz)'); zoom on

subplot(2,2,2)
      loglog(f,Iamp,'*'); grid on;
      axis([1e0,1e9,1e-10, 1e-8]);
      %title('Calculated amplitude of sine waves with KF= ');
      xlabel('Frequency (Hz)');
      ylabel('Amplitude of sine waves (A)');
zoom on

n=10;
tstart=0;
tstop=0.5e-6;
outputdata3=[ ];

for i=1:n
```

```
% total MATLAB simulation time with 100ps sampling delay
% total simulation time needs to be larger than the final Tstop
% Value in the transient analysis
t=tstart:1e-10:tstop;


Imat=repmat(Iamp',1,length(t));
fmat=repmat(f',1,length(t));
tmat=repmat(t,length(f),1);

xmat=repmat(x,1,length(t));

sum1=Imat.*sin(2*pi*fmat.*tmat+2*pi*xmat);

sum2=sum(sum1);

t1=t'; sum3=sum2';
noise1=[t1 sum3];
noise2=[outputdata3;noise1];
outputdata3=noise2;

clear t t1 *mat sum* noise*;

tstart=tstop+1e-10;
tstop=tstop+0.5e-6;

end

% Save data into file for HSPICE simulation and EXCEL use

save figure3.dat outputdata3 -ascii

% 1/f noise with random phase
% data is taken from Matlab simulation
load 'figure3.dat'
time=figure3(:,1);
noise=figure3(:,2);

subplot(2,2,3)
      plot(time*1e6,noise*1e6); grid on;
      xlabel('Time  (us)');
      ylabel('Sum of Sine waves with random phase (uA)');
      %title('Sum of sine waves with random phase with KF= ');

fs=1e10;                % sampling frequency

L=262144;   % L is also a window size. As L get larger magnitude of
fft gets closer
% to theoritical value

%SETUP AXIS
f1 = fs.* ( 0:1/L:1-1/L ); % up to f=fs
a = L/2;
a = round(a);
f = f1(2:a);            % up to fs/2
```

```
mag = fft(noise,L); % L is the size of windows

% Power Spectral Density (PSD)
power = mag.* conj(mag) /(fs* L);
power = power(2:a);
subplot(2,2,4);
      loglog(f,power,'*')
      axis([0,1e9,1e-34, 1e-20]);
      grid on;
      %title('Power spectral density of the sum of sine waves with
random phase');
      xlabel('Frequency (Hz)');
      ylabel('PSD of the Sum  (A^2/Hz)');
      hold on;
loglog(f,1e-10./f.^1,'k'), text(1e6, 2e-16, '1/f');
zoom on;

% Save data into file for EXCEL use
f2=f'; mag1=power;
outputdata4=[f2 mag1];
save figure4.dat outputdata4 -ascii
```

****

APPENDIX C – MATLAB JITTER SIMULATION

%MATLAB PROGRAM FOR SIMULATION OF CLOCK JITTER

```
% Simulation of clock jitter (First Part)

clear all; close all;

format long;

% Noise-Free Case
% Load Data

S=load('dm_noisefree.lis');

%S(1:7999,:)=[ ];

Vmax=max(S);

Vmin=min(S);

Vc=(Vmax(1,2)+Vmin(1,2))/2;

tI=S(1:20000,1);

VI=S(1:20000,2);

ndim=size(S);

nvj=ndim(1,1);
%nvj=15990000

for i=1:nvj

      S(i,2)=S(i,2)-Vc;

end

for i=2:nvj

      if S(i-1,1)==S(i,1);
      error(['Error i=',int2str(i)]);
      end
end

disp('Right, processing...1');


j=0;

for i=1:2

      if S(i,2)==0 & S(i+1,2)>0;
      j=j+1;
      Z(j)=S(i,1);
```

```
        elseif S(i,2)<0 & S(i+1,2)>0
      Y=[S(i,1) S(i+1,1) S(i+2,1) S(i+3,1) S(i+4,1) S(i+5,1)];
      X=[S(i,2) S(i+1,2) S(i+2,2) S(i+3,2) S(i+4,2) S(i+5,2)];
      j=j+1;
      Z(j)=interp1(X,Y,0,'spline');
        end
end

for i=4:nvj-2

      if S(i-1,2)==0 & S(i,2)>0;
      j=j+1;
      Z(j)=S(i-1,1);
        elseif S(i-1,2)<0 & S(i,2)>0
      Y=[S(i-3,1) S(i-2,1) S(i-1,1) S(i,1) S(i+1,1) S(i+2,1)];
      X=[S(i-3,2) S(i-2,2) S(i-1,2) S(i,2) S(i+1,2) S(i+2,2)];
      j=j+1;
      Z(j)=interp1(X,Y,0,'spline');
        end
end

for i=nvj-2:nvj-1

      if S(i,2)==0 & S(i+1,2)>0;
      j=j+1;
      Z(j)=S(i,1);
        elseif S(i,2)<0 & S(i+1,2)>0
      Y=[S(i-4,1) S(i-3,1) S(i-2,1) S(i-1,1) S(i,1) S(i+1,1)];
      X=[S(i-4,2) S(i-3,2) S(i-2,2) S(i-1,2) S(i,2) S(i+1,2)];
      j=j+1;
      Z(j)=interp1(X,Y,0,'spline');
        end
end

if S(nvj,2)==0 & S(nvj-1,2)<0;
      j=j+1;
      Z(j)=S(nvj,1);
end

clear S;

ZI=Z;

PTI=diff(ZI);

PTI=PTI*1e12;

nI=length(PTI);

save ZPTVNI ZI PTI tI VI nI;
```

```
% Simulation of clock jitter (Second Part)

clear all; close all;

format long;

% Noise-Injected Case

% Load Data

S=load('wdm_wn2.lis');

%S(1:7999,:)=[ ];

Vmax=max(S);

Vmin=min(S);

Vc=(Vmax(1,2)+Vmin(1,2))/2;

tN=S(1:20000,1);

VN=S(1:20000,2);

ndim=size(S);

nvj=ndim(1,1);
%nvj=15990000

for i=1:nvj

      S(i,2)=S(i,2)-Vc;

end

for i=2:nvj

      if S(i-1,1)==S(i,1);
      error(['Error i=',int2str(i)]);
      end
end

disp('Right, processing...2');


j=0;

for i=1:2

      if S(i,2)==0 & S(i+1,2)>0;
      j=j+1;
      Z(j)=S(i,1);
        elseif S(i,2)<0 & S(i+1,2)>0
```

```
      Y=[S(i,1) S(i+1,1) S(i+2,1) S(i+3,1) S(i+4,1) S(i+5,1)];
      X=[S(i,2) S(i+1,2) S(i+2,2) S(i+3,2) S(i+4,2) S(i+5,2)];
      j=j+1;
      Z(j)=interp1(X,Y,0,'spline');
        end
end

for i=4:nvj-2

      if S(i-1,2)==0 & S(i,2)>0;
      j=j+1;
      Z(j)=S(i-1,1);
        elseif S(i-1,2)<0 & S(i,2)>0
      Y=[S(i-3,1) S(i-2,1) S(i-1,1) S(i,1) S(i+1,1) S(i+2,1)];
      X=[S(i-3,2) S(i-2,2) S(i-1,2) S(i,2) S(i+1,2) S(i+2,2)];
      j=j+1;
      Z(j)=interp1(X,Y,0,'spline');
        end
end

for i=nvj-2:nvj-1

      if S(i,2)==0 & S(i+1,2)>0;
      j=j+1;
      Z(j)=S(i,1);
        elseif S(i,2)<0 & S(i+1,2)>0
      Y=[S(i-4,1) S(i-3,1) S(i-2,1) S(i-1,1) S(i,1) S(i+1,1)];
      X=[S(i-4,2) S(i-3,2) S(i-2,2) S(i-1,2) S(i,2) S(i+1,2)];
      j=j+1;
      Z(j)=interp1(X,Y,0,'spline');
        end
end

if S(nvj,2)==0 & S(nvj-1,2)<0;
      j=j+1;
      Z(j)=S(nvj,1);
end

clear S;

load ZPTVNI;

% Plot clock output

figure(1);

plot(tI,VI,'r');

figure(2);

hist(PTI,64);

xlabel('psec');
title(['Total periods n=',int2str(nI)]);
```

```
% Plot clock output

figure(3);

plot(tN,VN,'r');


ZN=Z;

PTN=diff(ZN);

PTN=PTN*1e12;

nN=length(PTN);

save ZPTVNN ZN PTN tN VN nN;

figure(4);

hist(PTN,64);

xlabel('psec');
title(['Total periods n=',int2str(nN)]);

if nN>=nI;

nf=nI;
ZN=ZN(1:nf+1);
PTN=PTN(1:nf);

elseif nN<nI;
nf=nN;
ZI=ZI(1:nf+1);
PTI=PTI(1:nf);

end

deltaT=PTN-PTI;
nr=1000;
a=floor(nf/nr);

for i=1:nr-1

n=a*i;

deltaTc=deltaT(1:n);

pkpt(i)=max(deltaTc)-min(deltaTc);

absjitter(i)=abs(sum(deltaTc));

cjitter(i)=sqrt((sum(deltaTc.^2))/n);

ccjitter(i)=sqrt((sum((diff(deltaTc)).^2))/(n-1));
```

```
t(i)=ZN(n+1);

mdeltat(i)=ZN(n+1)-ZN(1);

end

i=i+1;

n=nf;

deltaTc=deltaT;

pkpt(i)=max(deltaTc)-min(deltaTc);

absjitter(i)=abs(sum(deltaTc));

cjitter(i)=sqrt((sum(deltaTc.^2))/n);

ccjitter(i)=sqrt((sum((diff(deltaTc)).^2))/(n-1));

t(i)=ZN(n+1);

mdeltat(i)=ZN(n+1)-ZN(1);

save NOISEJ;

% --- Final output plot

figure(5);
plot(mdeltat,absjitter,'rs-'); grid on;
title('absj-');
xlabel('Measurement Interval deltat (S)');
ylabel('Absolute Jitter (pS)');

figure(6);
loglog(mdeltat,absjitter,'rs-'); grid on;
title('absj-');
xlabel('Measurement Interval deltat (S)');
ylabel('Absolute Jitter (pS)');

figure(7);
plot(mdeltat,pkpt,'rs-'); grid on;
title(' pkpt-');
xlabel('Measurement Interval deltat (S)');
ylabel('pkpt  Jitter (pS)');

figure(8);
loglog(mdeltat,pkpt,'rs-'); grid on;
title(' pkpt-');
xlabel('Measurement Interval deltat (S)');
ylabel('pkpt  Jitter (pS)');

figure(9);
plot(mdeltat,cjitter,'rs-'); grid on;
title('cj- ');
```

```
xlabel('Measurement Interval deltat (S)');
ylabel('c Jitter (pS)');

figure(10);
loglog(mdeltat,cjitter,'rs-'); grid on;
title('cj- ');
xlabel('Measurement Interval deltat (S)');
ylabel('c Jitter (pS)');

figure(11);
plot(mdeltat,ccjitter,'rs-'); grid on;
title('ccj-');
xlabel('Measurement Interval deltat (S)');
ylabel('cc Jitter (pS)');

figure(12);
loglog(mdeltat,ccjitter,'rs-'); grid on;
title('ccj-');
xlabel('Measurement Interval deltat (S)');
ylabel('cc Jitter (pS)');
```

****

APPENDIX D – JITTER FIGURES

JITTER FIGURES DUE TO FLICKER NOISE

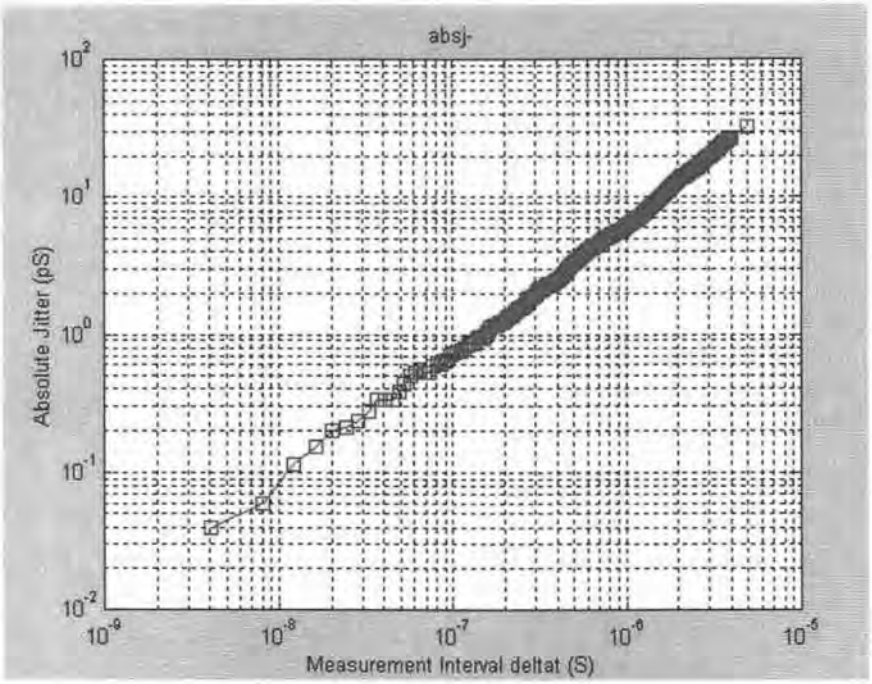

Figure D.1 Absolute jitter –Differential inverter with Maneatis load

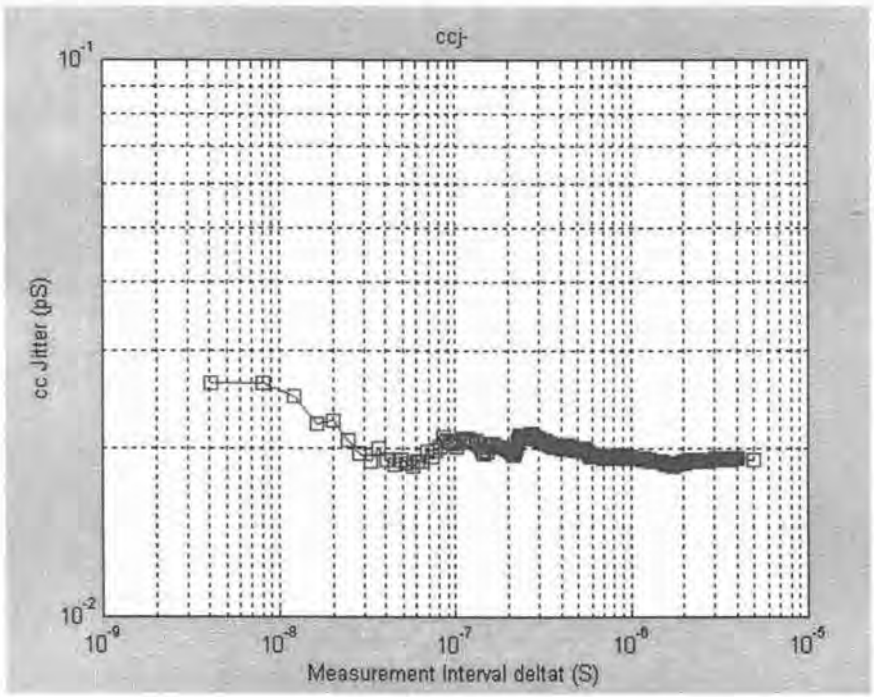

Figure D.2 Cycle to Cycle jitter – Differential inverter with Maneatis load

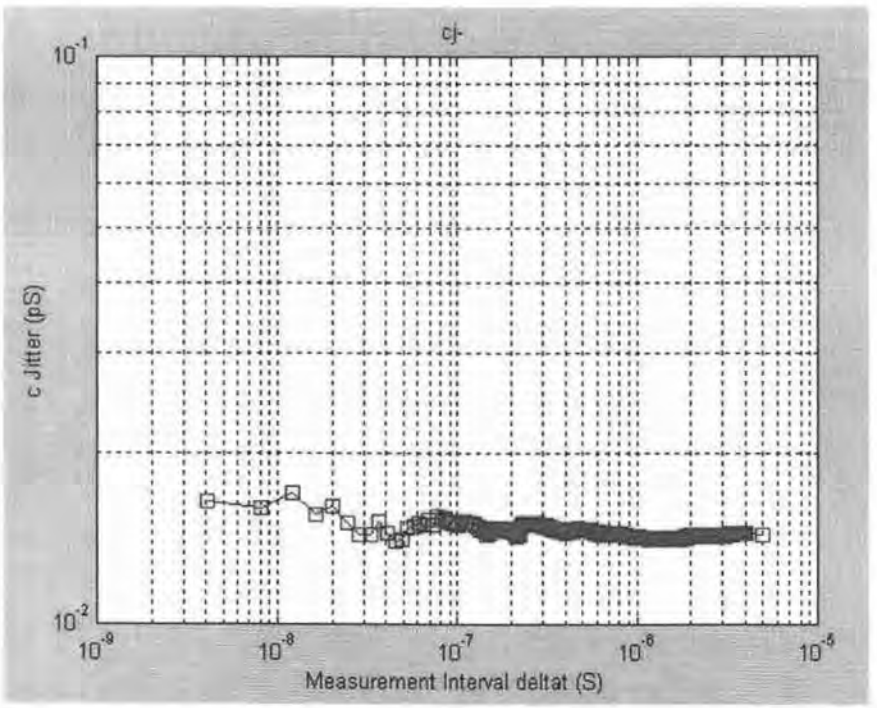

Figure D.3 Cycle jitter – Differential inverter with Maneatis load

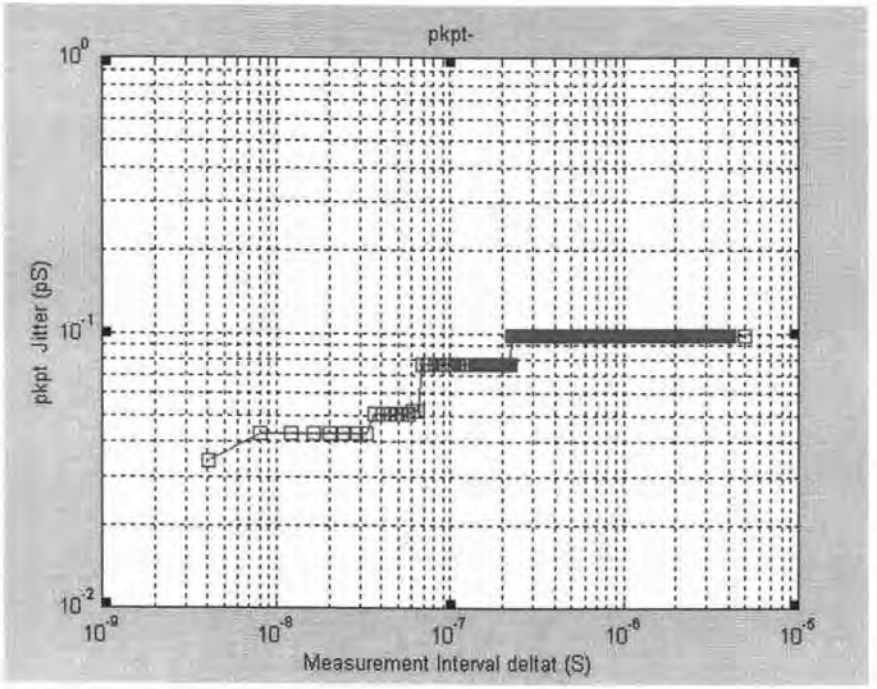

Figure D.4 Peak to Peak jitter – Differential inverter with Maneatis load

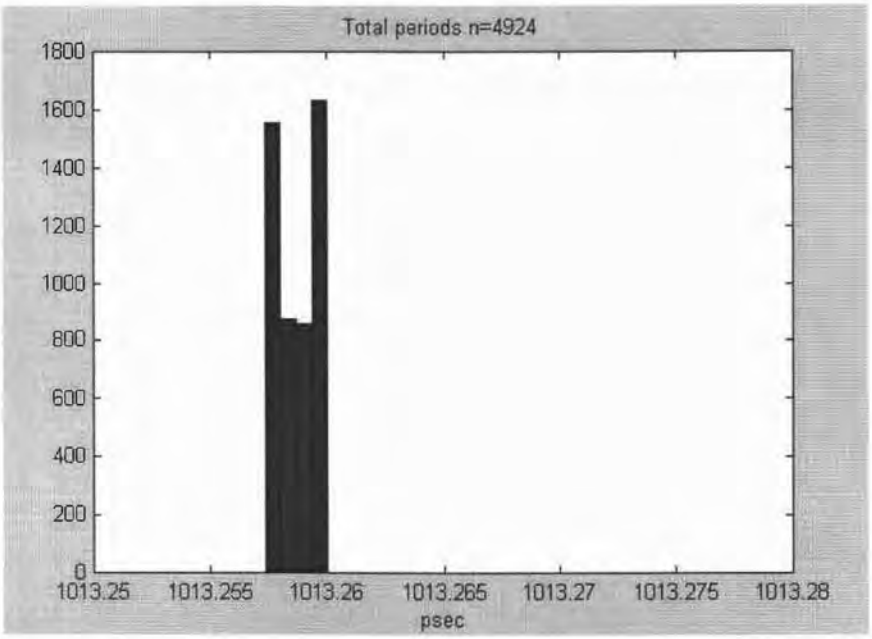

Figure D.5 Histogram noise free case –Differential inverter with Maneatis load

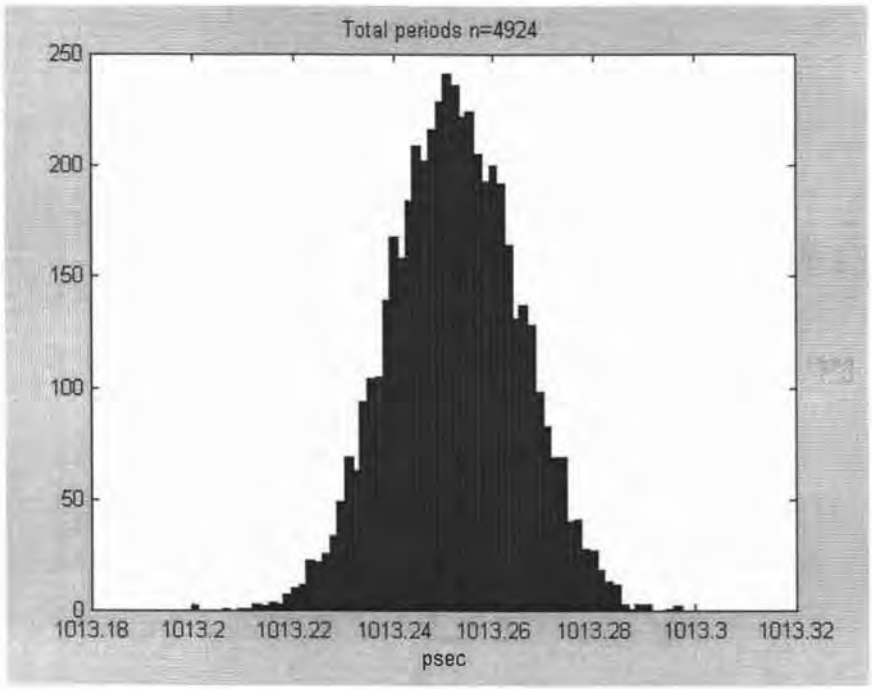

Figure D.6 Histogram for flicker noise injected case – Differential inverter with Maneatis load

JITTER FIGURES DUE TO WHITE NOISE

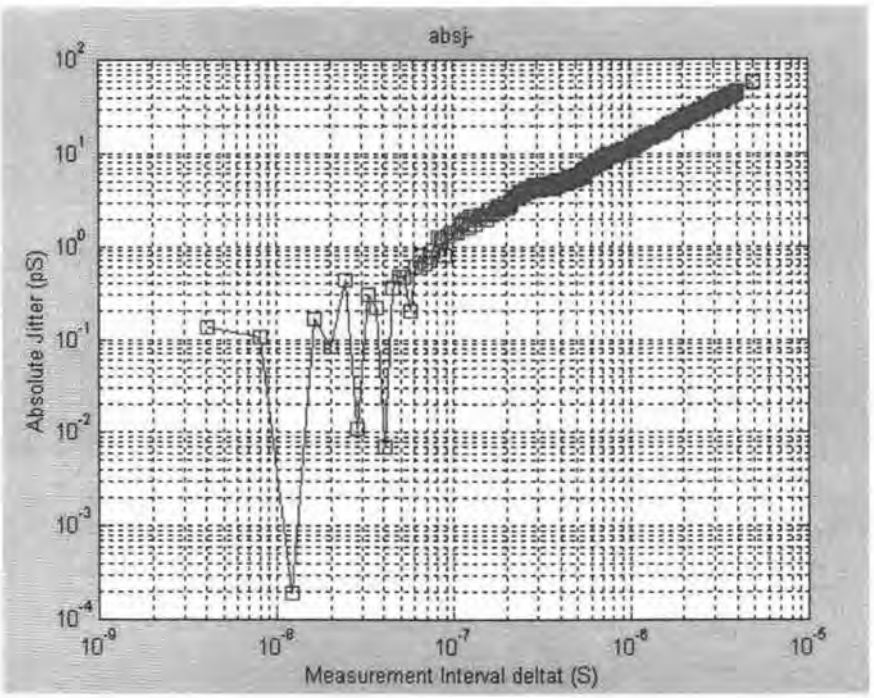

Figure D.7 Absolute jitter –Differential inverter with Maneatis load

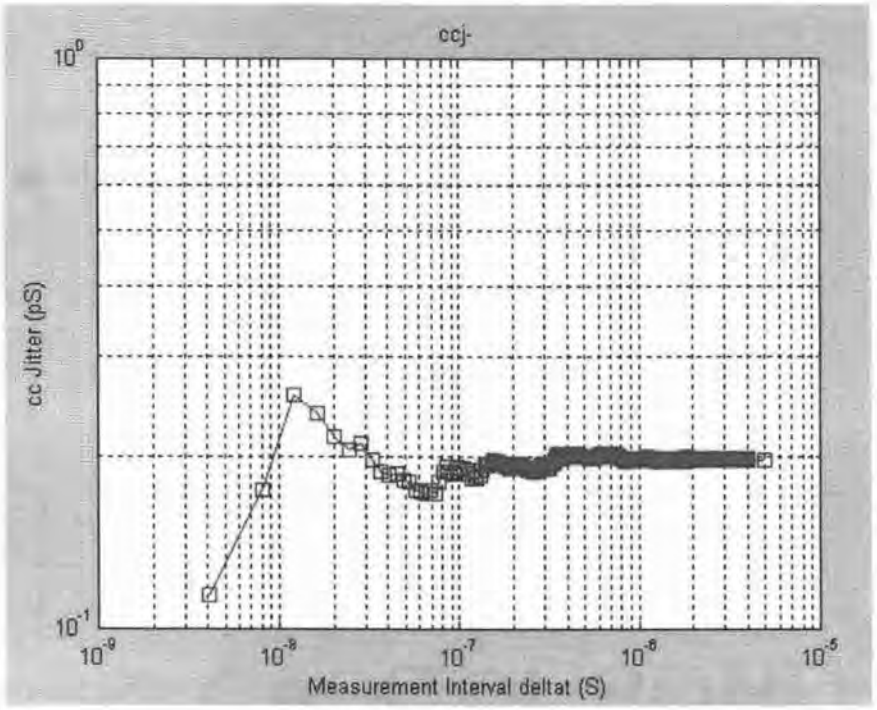

Figure D.8 Cycle to Cycle jitter – Differential inverter with Maneatis load

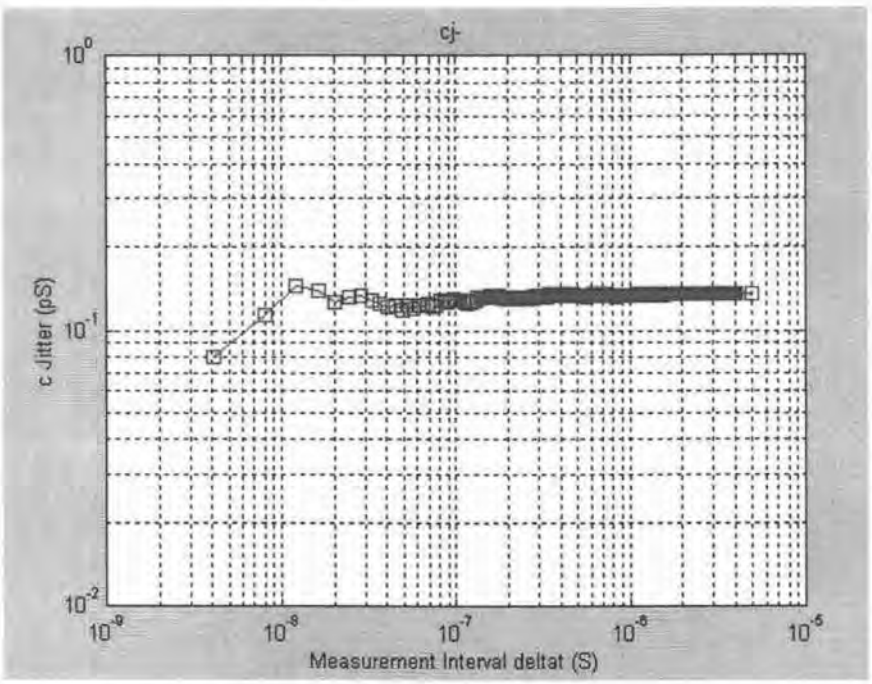

Figure D.9 Cycle jitter – Differential inverter with Maneatis load

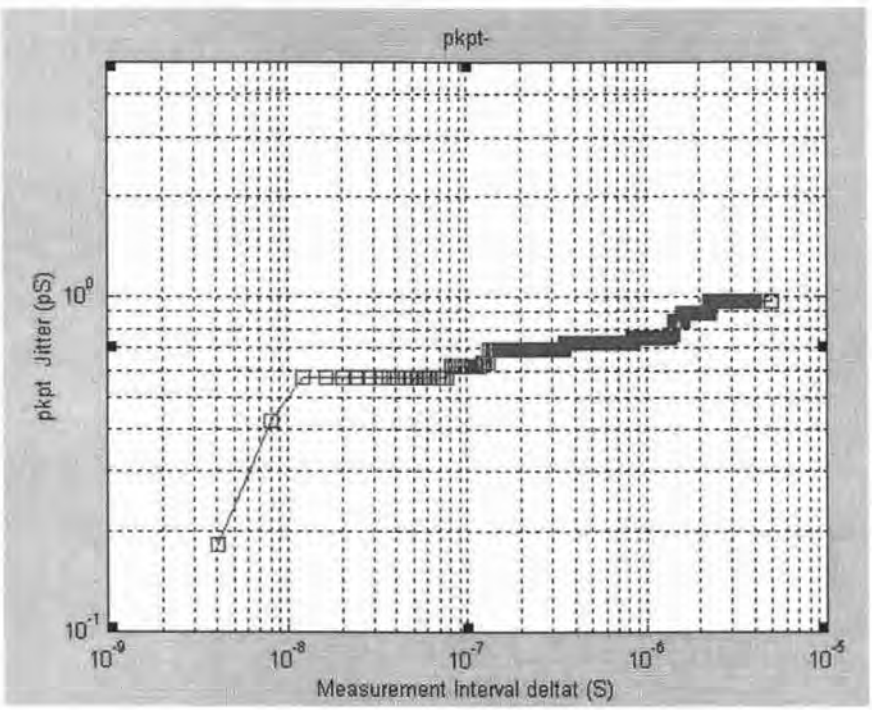

Figure D.10 Peak to Peak jitter – Differential inverter with Maneatis load

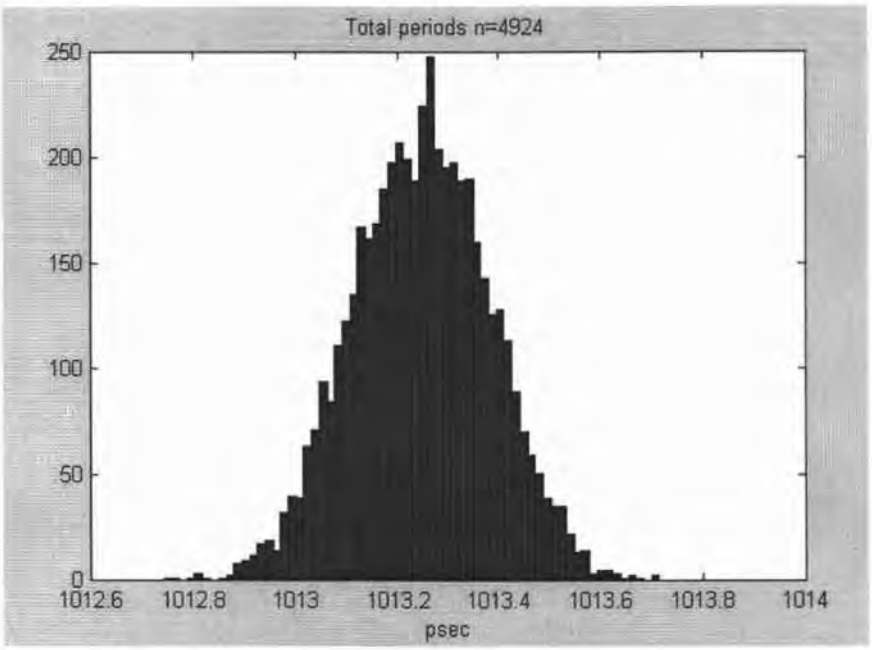

Figure D.11 Histogram for white noise injected case – Differential inverter with Maneatis load