AN ABSTRACT OF THE THESIS OF

David Hong for the degree of Master of Science in

Electrical and Computer Engineering presented on June 3, 2005.

Title: Process Development and Modeling of Thin-Film Transistors.

Redacted for Privacy

Abstract approved: _____

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A class of high-performance thin-film transistor (TFT) channel materials has emerged involving oxides composed of heavy-metal cations (HMCs) with $(n-1)d^{10}ns^0$ ($n \geq 4$) electronic configurations. This thesis is devoted to the pursuit of three topics involving the development of these materials for TFT applications: modeling TFT current-voltage characteristics, an exploratory method for the evaluation of multicomponent HMC oxide systems, and passivation of zinc tin oxide TFTs.

The first topic involves generic, modeling of the current-voltage characteristics of a TFT. Initially, a general equation, the conductance integral equation, is derived. This equation expresses the drain current as an integral of the channel conductance with respect to the gate voltage. The utility of the conductance integral equation is demonstrated via derivation of the square-law model current-voltage equation, which constitutes the basic TFT model. Finally, a comprehensive current-voltage equation expressing $I_D$ for a depletion-mode field-effect transistor is derived from the conductance integral equation.

The second topic relates to the development of a novel deposition methodology which is employed for exploratory development of HMC oxides for channel layers in TFTs. The method involves sequential RF sputter deposition of thin, single cation oxide layers and subsequent post-deposition annealing in order to obtain a multi-component oxide thin film. The viability of this rapid materials development

methodology is demonstrated through the realization of high-performance TTFTs with channel layers composed of combinations of zinc oxide/tin oxide, and tin oxide/indium oxide.

The third topic concerns the development of a methodology for the passivation of bottom-gate TFTs utilizing zinc tin oxide as the channel layer and silicon dioxide as the passivation layer. This methodology involves annealing of the TFT after channel layer deposition and an additional anneal after thermal evaporation of a silicon dioxide passivation layer. Passivated zinc tin oxide TFTs possess electrical characteristics equivalent to those of unpassivated, air-exposed devices. In contrast, TFT electrical performance is dramatically degraded if a zinc tin oxide TFT is covered with a dielectric layer and does not undergo both types of anneal. In addition to silicon dioxide, successful passivation of zinc tin oxide TFTs is accomplished using thermally evaporated calcium fluoride, germanium oxide, strontium fluoride, or antimony oxide as passivation dielectrics.

Process Development and Modeling of Thin-Film Transistors.

by

David Hong

A THESIS

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Master of Science

Presented June 3, 2005
Commencement June 2006

Master of Science thesis of David Hong presented on June 3, 2005

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David Hong, Author

# ACKNOWLEDGMENTS

I would like to thank my family for their support and encouragement throughout my education and life. They have instilled in me a work ethic and ambition that has led me this far.

I would also like to thank many of my friends and coworkers who have contributed greatly during my graduate program. Hai Chiang and Nicci Dehuff have been great resources for encouragement and insight into many topics. John Wager has provided great direction and discussion. Chris Tasker provided a work ethic to follow, great direction and support in and outside of the cleanroom. Manfred Dittrich has provided exceptional fabrication work and mechanical knowledge.

A number of industry people deserve acknowledgements. Randy Hoffman, inventor of the inorganic transparent thin-film transistor, has been a great innovator and a great resource. Dr. Jeff Bender has provided invaluable dialogue and inspiration.

To the optimist the glass is half full. To the pessimist the glass is half empty. To the engineer, the glass is twice as big as it needs to be.

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TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF FIGURES

LIST OF TABLES

# PROCESS DEVELOPMENT AND MODELING OF THIN-FILM TRANSISTORS.

## 1. INTRODUCTION

Amorphous multicomponent oxides composed of heavy-metal cations (a-MHMCs) with $(n\text{-}1)d^{10}ns^0$ ($n \geq 4$) electronic configurations, such as zinc tin oxide, constitute an interesting class of materials since they are often transparent in the visible portion of the electromagnetic spectrum, but yet also possess relatively high electron mobilities in spite of their amorphous character [1, 2, 3]. When employed as a channel layer, such materials have yielded high-performance thin-film transistors (TFTs) [4, 5, 6, 7].

Three primary topics are pursued in this thesis, all related to the development of a-MHMC TFTs or TTFTs: modeling of TFT current-voltage characteristics, an exploratory methodology for evaluating a-MHMC oxides as channel layers for TTFTs, and passivation of a TFT utilizing an a-MHMC oxide, zinc tin oxide, as the channel layer.

The structure of this thesis is as follows. Chapter 2 contains a review of the pertinent literature and provides the technical background necessary to establish a context within which experimental results can be discussed. Chapter 3 provides a description of important fabrication tools and techniques employed, followed by a discussion of relevant electrical TFT characterization methodology. Chapter 4 is devoted to current-voltage modeling of TFTs. Chapter 5 presents a method for exploring various combinations of a-MHMC oxides for use as channel layers in TFTs.

Chapter 6 presents a method for passivation of zinc tin oxide TFTs. Finally, Chapter 7 contains conclusions and recommendations for future work.

# 2. THIN-FILM TRANSISTOR FUNDAMENTALS

In this chapter, device structure and device operation is presented and existing literature pertaining to thin-film transistors (TFTs) and transparent thin-film transistors (TTFTs) is reviewed.

## 2.1 Transistor overview

Figure 2.1 shows the basic structure of a TFT and several energy band diagrams as viewed through the gate of an n-channel, accumulation-mode TFT. [8] The energy band diagram of Fig. 2.1b shows the device at equilibrium, with 0 V applied to the source, drain, and gate. Figure 2.1c shows an energy band diagram with the gate negatively biased. The applied negative bias repels mobile electrons from the channel, leaving a depletion region near the insulator-channel interface. When compared to Fig. 2.1b, this biasing condition has a reduced conductance due to the reduced number of mobile electrons in the channel. Figure 2.1d shows an energy band diagram with the gate positively biased. The applied positive bias attracts mobile electrons, forming an accumulation region near the insulator-channel interface. These excess mobile electrons lead to an increase in the conductance.

Beginning with the case where the gate is biased positively and accumulation is established, i.e., Fig. 2.1d, consider the effect of an applied drain-source voltage, $V_{DS}$. Initially the channel is modeled as a resistor, i.e. linearly increasing current with $V_{DS}$. As $V_{DS}$ increases, accumulation near the drain decreases. As $V_{DS}$ is increased further, the region near the drain eventually begins to deplete. The voltage

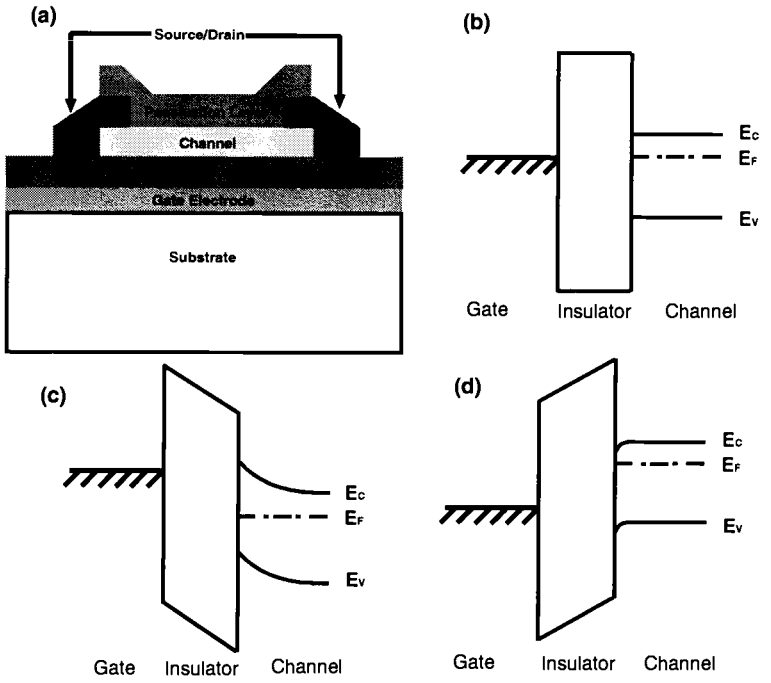


Figure 2.1: (a)The basic structure of a TFT and corresponding energy band diagrams as viewed through the gate for several biasing conditions: (b)equilibrium, (c) $V_{GS}$ <0 V and (d) $V_{GS}$ >0 V

at which the channel region near the drain is fully depleted of carriers is denoted the pinch-off voltage. Therefore, application of $V_{DS}$ greater than the pinch-off voltage results in a saturated drain current characteristic.

TFT device structures can differ from that shown in Fig. 2.1a. Four possible TFT device structures are shown in Fig. 2.2. [9] As evident from Fig. 2.2, devices can be either staggered or coplanar. In a coplanar configuration, as shown in Figs. 2.2b and 2.2d, the source and drain contacts and the insulator are on the same side of the channel. In such an arrangement, the source-drain contacts are in direct contact with the induced channel. In a staggered configuration, as shown in Figs. 2.2a and 2.2c, the source and drain contacts are on the opposite side of the channel from the

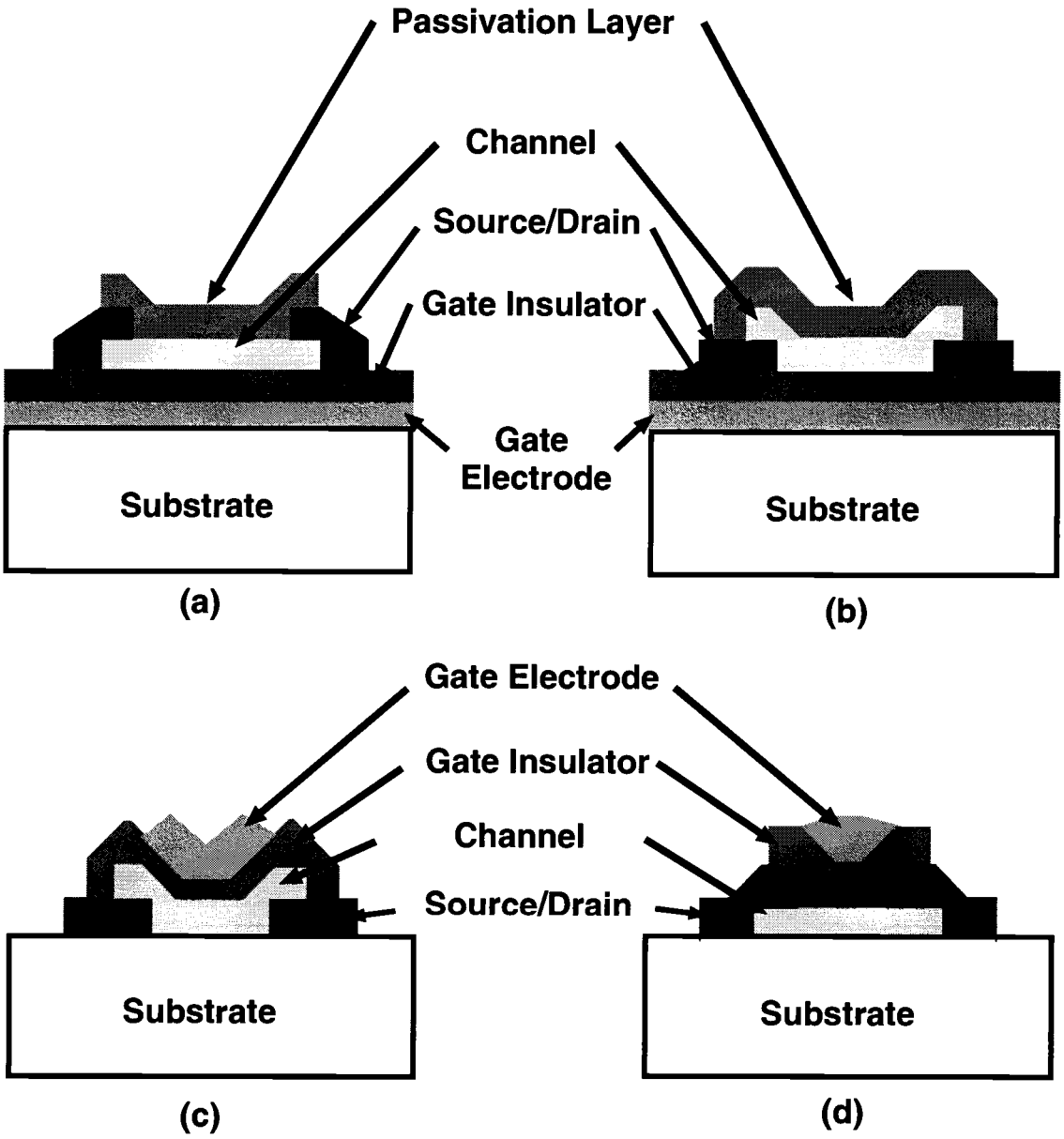


Figure 2.2: Four general thin-film transistor configurations, including: (a) staggered bottom-gate, (b) coplanar bottom-gate, (c) staggered top-gate, and (d) coplanar top-gate.

insulator; thus, there is no direct connection to the induced channel. However, the contact area is very large when a staggered structure is used.

In addition to coplanar and staggered configurations, TFTs can be classified as either bottom-gate or top-gate devices. A bottom-gate TFT, which is sometimes referred to as an inverted TFT, has the gate insulator and gate electrode located beneath the channel, as shown in Figs. 2.2a and 2.2b. The top surface of a bottom-gate TFT is exposed to air or is passivated by coating the top surface with a protective layer. A top-gate TFT, as shown in Figs. 2.2c and 2.2d, has the gate and insulator located on top of the channel. In a top-gate device, the channel is covered by a gate insulator so that the top surface is inherently passivated.

## 2.2 Thin-film transistor history

The first TFT was presented in 1961 by Paul Weimer at the IRE-AIEE Device Research Conference. This TFT, fabricated at RCA Laboratories in Princeton, New Jersey, used CdS as the channel layer, gold for the source and drain contacts, and shadow masks for patterning. [10]

Weimer's work inspired Peter Brody at Westinghouse's Research Lab. Brody aggressively pursued many TFT projects, including TFTs deposited on paper, and a half-watt audio amplifier on a strip of aluminum foil. By 1968, Brody's work led to the introduction of TFTs into Westinghouse's electroluminescent displays.[11] By the late 1970's an active-matrix liquid-crystal display (LCD) was demonstrated that used TFTs. These displays became a commercial product in 1983.

In the 1980's interest in TFTs, to a large extent, had waned. It was not until the 1990's, when brighter LCDs were fabricated using an amorphous silicon switching TFT incorporated into each pixel, that interest in TFTs was resurrected.

Today, thin-film transistors are used in many applications. The primary application of TFTs is still in displays where they are used in amplification and control circuitry. There is much work currently devoted towards the development of both organic and inorganic TFTs to provide an inexpensive alternative to single crystal semiconductor technology.

The dominant channel material currently used in commercial TFTs is silicon. Polycrystalline silicon TFTs processed below 1000°C have yielded devices with a peak incremental mobility of up to 100 $cm^2V^{-1}s^{-1}$. [12] Amorphous silicon TFTs deposited on flexible substrates, Kapton E polyimide, have demonstrated incremental mobilities of $\sim 0.45$ $cm^2V^{-1}s^{-1}$. [13]

In addition to silicon TFTs, another class of TFTs has been demonstrated which employ organic materials as the channel layer. [14] These materials exhibit mobilities of $10^{-3}$-1 $cm^2V^{-1}s^{-1}$. However, the low mobility of these organic TFTs is offset by the low cost of deposition, such as spin coating or printing. In addition, the processing temperature of these devices is below 300°C, allowing for deposition onto plastic substrates. Most of these organic channel materials are p-type. However, an n-type organic TFT has been demonstrated using an organic channel layer. [15] This n-type organic TFT demonstrated mobilities of up to 0.1 $cm^2V^{-1}s^{-1}$.

In addition to organic TFTs, combinations of organics and inorganics, referred to as hybrid materials, have also been explored for TFT applications. [16]

Hybrid materials use a mixture of organic and inorganic chemicals to attain desired physical and chemical properties. TFTs made from a tin(II) iodide perovskite, $(C_6H_5C_2H_4NH_3)_2SnI_4$, have been fabricated with incremental mobilities of $\sim$ 0.61 $cm^2V^{-1}s^{-1}$. [16]

## 2.3 Transparent thin-film transistor history

Hoffman et al. reported the first fully-transparent thin-film transistor (TTFT) in 2003. [17] This transistor utilized a zinc oxide channel layer deposited via ion-beam sputtering and indium tin oxide (ITO) source and drain contacts. ITO was also used as the gate electrode and a superlattice of aluminum oxide and titanium oxide was used as the gate dielectric. This device yielded a channel mobility of $\sim$ 2.5 $cm^2V^{-1}s^{-1}$, threshold voltage of $\sim$ 10 V and turn-on voltage of $\sim$ -10 V. It should be noted that the maximum processing temperature of this device was 700°C.

Since then, zinc oxide has been explored in other TFTs and TTFTs. [18, 19, 20, 21, 22, 23] Room temperature deposition of zinc oxide yielded TFTs with peak incremental mobilities of $\sim$ 2 $cm^2V^{-1}s^{-1}$. [22] These room-temperature deposited TFTs used RF sputtered zinc oxide as the channel layer and gold with a titanium adhesion layer as the source and drain contacts. The entire device was fabricated on a heavily doped p-type silicon substrate with thermal silicon dioxide as the gate dielectric. These devices exhibit on-to-off ratios of $10^6$, threshold voltages of $\sim$ 0 V, and turn-on voltages of $\sim$ -2 V .

A TTFT was fabricated utilizing zinc oxide by pulsed laser deposition (PLD). [20] PLD deposited zinc oxide yielded TFTs with peak incremental mobilities of $\sim$ 1

$cm^2V^{-1}s^{-1}$. These devices used ITO as the source and drain contacts, as well as the gate electrode. For this TTFT, a combination of silicon nitride and silicon dioxide, both via plasma-enhanced chemical vapor deposition, was used as the gate dielectric. These devices, however, did not have patterned gate electrodes, nor patterned channel layers, which would result in an artificially high extracted mobility. On-to-off ratio was $10^5$ for these devices, threshold voltage was $\sim$ 3 V, and turn-on voltage was $\sim$ -2 V.

Zinc oxide by PLD deposition was also studied by Nishii et al. [19] These devices were processed at 300°C and showed mobilities of $\sim$ 7 $cm^2V^{-1}s^{-1}$, a threshold voltage of $\sim$ 10 V, and a turn-on voltage of $\sim$ 0 V.

Zinc oxide via liquid deposition was also explored. [21] These TTFTs had a post-deposition annealing temperature of 600°C and showed mobilities of $\sim$ 0.2 $cm^2V^{-1}s^{-1}$, a threshold voltage of $\sim$ 5 V, and a turn-on voltage of $\sim$ 3 V.

Recently zinc oxide TFTs with peak incremental mobilities as high as $\sim$ 25 $cm^2V^{-1}s^{-1}$ have been reported. [18] These devices utilized RF sputtered zinc oxide on heavily doped silicon substrates with a thermal silicon dioxide layer as the gate dielectric. These devices have a turn-on voltage of $\sim$ -2 V and a threshold voltage of $\sim$ 5 V.

Mobilities of $\sim$ 27 $cm^2V^{-1}s^{-1}$ have been reported for RF sputtered zinc oxide, [23] however these devices were unpatterned so that the reported mobility is artificially high. However, the processing of functional devices utilizing RF sputtering at room temperature is impressive.

In addition to zinc oxide, tin oxide TTFTs have been fabricated. [24] Tin oxide TTFTs showed mobilities of $\sim$ 2 $cm^2V^{-1}s^{-1}$, a threshold voltage of $\sim$ 10 V, and a turn-on voltage of $\sim$ -20 V.

Amorphous oxides composed of heavy-metal cations (HMCs) with $(n-1)d^{10}ns^0$ ($n \geq 4$) electronic configurations, of which zinc oxide and tin oxide are included, has been the basis of several new types of high-performance TTFTs. [1, 5, 6, 4, 7] These semiconductors have a conduction band composed primarily of symmetric s orbitals. Some of these materials have shown improved mobilities over their respective polycrystalline phases due to the lack of grain boundaries in the amorphous phase. [5]

A TTFT utilizing a HMC oxide yielded a high peak channel mobility of $\sim$ 80 $cm^2V^{-1}s^{-1}$. [7] These devices were fabricated using a single crystal $InGaO_3(ZnO)_5$ channel. These devices underwent an extremely high processing temperature of 1400°C to reach the single crystal phase. It should be noted that the high performance TTFTs utilized hafnium oxide as the gate insulator; when aluminum oxide was used as the gate insulator, a peak channel mobility of $\sim$ 2 $cm^2V^{-1}s^{-1}$ was measured. The threshold voltage for this device was $\sim$ 3 V and the turn-on voltage was $\sim$ -1 V. These devices exhibited on-off ratios of $10^6$

An amorphous phase of $InGaO_3(ZnO)_5$, deposited by PLD, was used recently to fabricate a flexible TTFT. [4] Polyethylene terephthalate was the substrate. ITO was used as the source/drain contacts and gate electrode. Yttrium oxide was used as the gate dielectric. These devices exhibited a saturation mobility of $\sim$ 2 $cm^2V^{-1}s^{-1}$. Turn-on voltage, threshold voltage, and on-to-off ratio were $\sim$ 1 V, $\sim$ 1.6 V, and $10^3$, respectively.

Other HMC oxides studied to date include zinc tin oxide and zinc indium oxide. [5, 6] TTFTs based on these material systems were fabricated in a similar fashion. These TTFTs utilized ITO and aluminum oxide-titanium oxide for the gate and gate dielectric. ITO was also used for the source and drain. Channels were fabricated by RF sputtering. Zinc tin oxide and zinc indium oxide were amorphous. In spite of their amorphous nature, they yielded high incremental mobilities: 20-50 $cm^2V^{-1}s^{-1}$ for zinc tin oxide and 45-55 $cm^2V^{-1}s^{-1}$ for zinc indium oxide. Zinc tin oxide TFTs exhibited on-to-off ratios of $10^6$, threshold voltages between 0 V and 10 V, and turn-on voltages between -5 and 5 V. On-to-off ratios for zinc indium oxide TFTs were $10^6$, turn-on voltages were measured between -23 V and -13 V, and threshold voltages were between -20 V and -10 V.

Table 2.1 summarizes the data that is presented in this section.

Table 2.1: Summary of transparent thin-film transistor characteristics.

| Material | Deposition | Channel mobility ($cm^2V^{-1}s^{-1}$)) | $V_T$ (V) | $V_{ON}$ (V) | On-to-off ratio | Maximum processing temp. (°C) | |
|---|---|---|---|---|---|---|---|
| Zinc oxide | Ion-Beam Sputtering | 2.5 | 10 | -10 | $10^7$ | 700 | [17] |
| Zinc oxide | RF Sputtering | 2 | 0 | -2 | $10^5$ | Room temp. | [22] |
| Zinc oxide | PLD | 1[a] | 3 | -2 | $10^5$ | 450 | [20] |
| Zinc oxide | PLD | 7 | 10 | 0 | $10^6$ | 300 | [19] |
| Zinc oxide | RF Sputtering | 25 | 5 | -2 | $10^6$ | 600 | [18] |
| Zinc oxide | RF Sputtering | 27[a] | 19 | 11 | $10^6$ | Room temp. | [23] |
| Zinc oxide | Spin Coating | .2 | 5 | 3 | $10^7$ | 600 | [21] |
| Tin oxide | RF Sputtering | 2 | 10 | -20 | $10^5$ | 600 | [24] |
| Zinc indium gallium oxide | PLD | 80 | 3 | -1 | $10^6$ | 1400 | [7] |
| Zinc indium gallium oxide | PLD | 2 | 1.6 | 1 | $10^3$ | Room temp. | [4] |
| Zinc tin oxide | RF Sputtering | 15 | -3 | -5 | $10^7$ | 300 | [5] |
| Zinc tin oxide | RF Sputtering | 25 | 8 | -5 | $10^7$ | 600 | [5] |
| Zinc indium oxide | RF Sputtering | 30 | 10 | 8 | $10^6$ | 300 | [6] |
| Zinc indium oxide | RF Sputtering | 55 | -20 | -23 | $10^6$ | 600 | [6] |

[a]Unpatterned gate and channel.

## 2.4 Conclusion

This chapter presents basic information and a review of existing literature pertaining to thin-film transistors (TFTs) and transparent thin-film transistors (TTFTs). First, the operation and device structure of TFTs is discussed. Then, existing literature pertaining to TFTs and TTFTs is reviewed.

# 3. TFT FABRICATION AND CHARACTERIZATION

This chapter presents information regarding the fabrication and characterization of TFTs and TTFTs. First, deposition techniques used in TFT and TTFT fabrication are discussed. Second, electrical characterization of TFTs is discussed. Finally, a model is derived to account for peripheral fringing current artifacts in unpatterned channels in TFTs.

## 3.1 Thin-film deposition and processing

This section covers deposition and processing techniques that are used for this research. Many other processing techniques are available, as explained in detail elsewhere. [25]

### 3.1.1 Evaporation

Evaporation is a deposition technique whereby the material to be deposited begins as a solid, goes into a vapor phase, and then recondenses back to a solid thin film.[25] The transition from solid to vapor can either be direct, referred to as sublimation, or indirect via a transition from a solid to a liquid phase, melting, and subsequently from a liquid to a vapor phase, vaporization. Whether the material sublimes or melts and vaporizes depends on the pressure of the deposition chamber, the heating source, and the material to be deposited.

Evaporation is accomplished using one of two systems, a Veeco thermal evaporator and a small desktop evaporator manufactured by Polaron. For both systems, the main chamber is comprised of a glass bell jar assembly. High-vacuum is achieved

in both systems with a diffusion pump. The Veeco evaporator has a liquid nitrogen cold trap.

For the research described in this thesis, the Polaron is used for deposition of aluminum, while the Veeco is used for thermal evaporation of silicon dioxide and other passivation materials.

### 3.1.2 Sputtering

Sputtering is a common thin film deposition technique whereby a plume of the source material is created by energetic ions. For this thesis, two magnetron RF sputtering systems, a modified Control Process Apparatus (CPA) sputtering system and a custom built sputtering system denoted the Tasker/Chiang (Tang) sputtering system, are used. [26, 27]

The CPA is a rectangular, stainless-steel, load-locked chamber. [27] High-vacuum is achieved using a diffusion pump with a liquid nitrogen cold trap. The system has 2 side-mounted sputtering guns which utilize 2" targets. Both sputtering guns are on the same side of the system. Gas flow for the system is controlled via four mass flow controllers which can introduce up to four different gas sources into the chamber.

The Tang is a cylindrical, stainless-steel, load-locked chamber. [26] High-vacuum is achieved using a turbomolecular pump. The Tang has one side-mounted 2" sputtering gun and one side-mounted 3" sputtering gun. Gas flow is controlled via four mass flow controllers which can introduce up to four different gas compositions.

For this thesis, channel layers are deposited in both systems. The Tang is also used for the deposition of ITO contacts.

### 3.1.3 Post-deposition thermal processing

After deposition, many films require a thermal anneal. Annealing is accomplished by controlling the ambient pressure, ambient composition and the temperature of the substrate. During thermal annealing, thin films can react with the processing ambient, which can consist of, for example, oxidizing or reducing gases. Thin films can also undergo crystallization, diffusion, and change in film stress due to thermal annealing.

For the research discussed in this thesis, a Thermolyne 47900 box furnace is used for thermal annealing. This furnace utilizes resistive coils as the heating element and room air as the annealing ambient. No vacuum pump or gases are connected to this system. Samples are placed on alumina discs during annealing to prevent contamination.

## 3.2 Thin-film transistor fabrication

Figure 3.1 shows the two TFT structures fabricated for this thesis: a fully-transparent TTFT and a non-transparent TFT built on a silicon substrate. Both TFTs are bottom-gate staggererd TFTs, as shown in Fig. 2.2.

### 3.2.1 Fully-transparent TTFT

Figure 3.1a shows a cross section of a fully-transparent TFT. A fully-transparent TTFT is prepared on Nippon Electric Company glass substrates (NEG OA2) coated with a 100 nm sputtered indium tin oxide (ITO) gate electrode film and a 220 nm atomic layer deposited superlattice of $AlO_x$ and $TiO_x$ (ATO). The ATO has a dielectric constant of $\sim$15. The ITO and ATO layers constitute the gate contact and

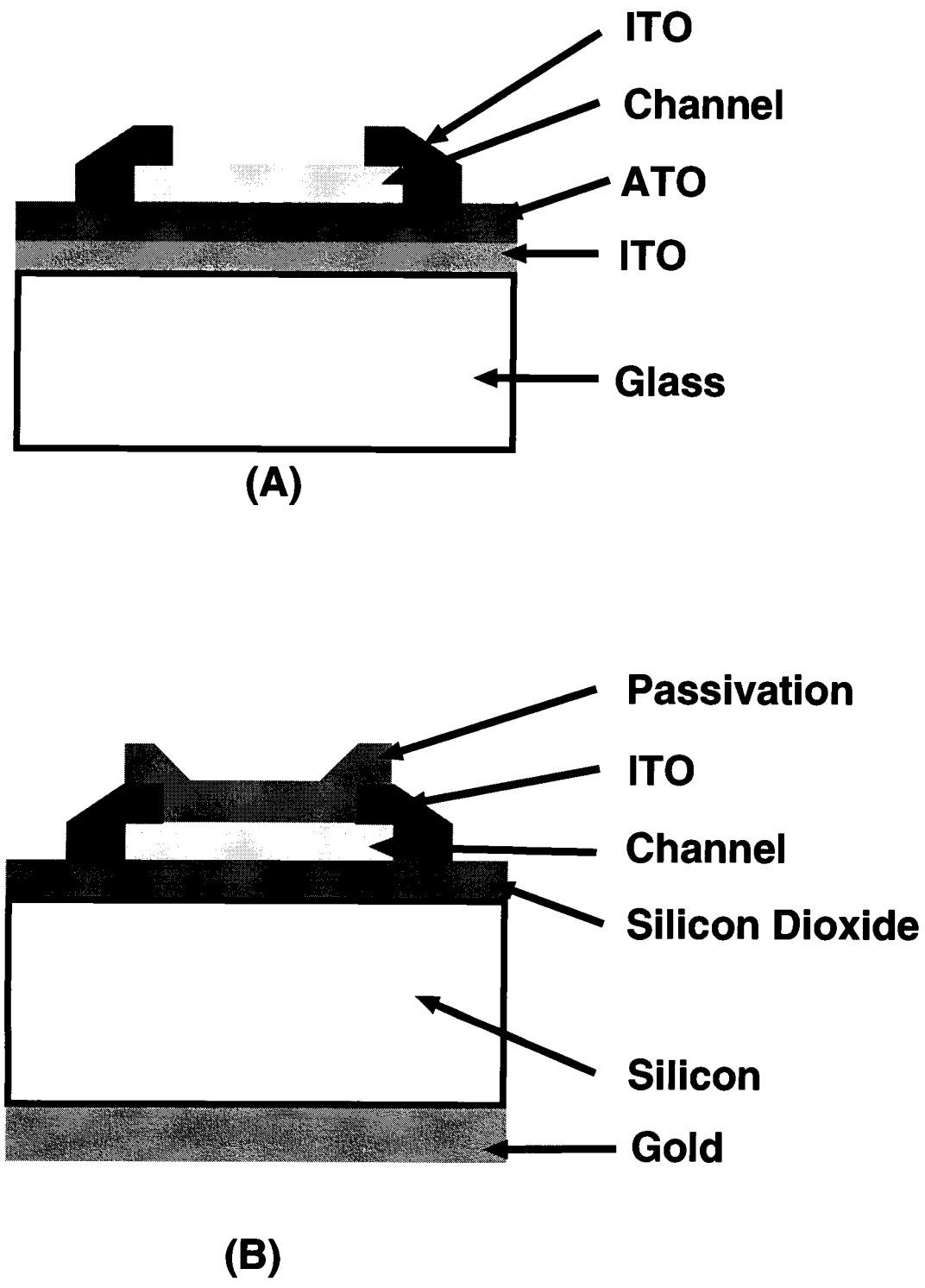


Figure 3.1: TFT structures used for the research discussed in this thesis, including (a) fully-transparent thin-film transistor and (b) non-transparent thin-film transistor.

insulator, respectively, of a bottom-gate TTFT. An ~20 nm channel layer is then deposited via RF magnetron sputtering through a shadow mask for channel definition using 2" diameter sputter targets, a target-to-substrate distance of ~7.5 cm, a power of 50 W, a pressure of 5 mTorr, and an Ar:$O_2$ ratio of 9:1. Next, an ~200 nm layer of ITO is deposited by RF sputtering through a shadow mask for source and drain patterning using a 3" target in pure Ar at a pressure of 30 mTorr. Aluminum deposited via thermal evaporation is used as an alternative source and drain contact material. There is no measureable difference between aluminum source/drain TTFTs and ITO source/drain TTFTs. The channel length and width are 1520 $\mu$m and 7170 $\mu$m, respectively. The entire thin film stack is then furnace annealed in air using a one hour ramp and a 10 minute hold at the processing temperature for 10 minutes; the sample is then allowed to cool inside the furnace for 5 hours to reach room temperature. Annealing occurs prior to aluminum source/drain deposition when it is utilized.

### 3.2.2 Non-transparent TFT

Figure 3.1a shows a cross section of a non-transparent TFT. A non-transparent TFT is prepared on heavily-doped p-type silicon substrates with 100 nm of thermal silicon dioxide and a gold back contact. Note that the heavily doped silicon acts as both the substrate and the gate electrode. An ~80 nm channel layer is then deposited via RF magnetron sputtering through a shadow mask for channel definition using a 2" diameter sputter target, a target-to-substrate distance of ~7.5 cm, a power of 50 W, a pressure of 5 mTorr, and an Ar:$O_2$ ratio of 9:1. Next, an ~200 nm layer of indium tin oxide (ITO) is deposited by RF sputtering using a 3" diameter target in pure Ar

at a pressure of 30 mTorr. Both the channel layer and source/drain electrodes (ITO) are patterned through the use of shadow masks; the channel length and width are 100 $\mu$m and 1000 $\mu$m, respectively. The thin film stack is then furnace annealed similar to the fully-transparent TTFT. TFT passivation begins with an ~100 nm passivation layer that is deposited over the thin-film stack via thermal evaporation. The device stack is again furnace annealed in air with a one hour ramp and a 10 minute hold at various temperatures.

## 3.3 Thin-film transistor device characteristics

This section discusses two important TFT figures-of-merit, threshold voltage and mobility, and their estimation from experimental data.

### 3.3.1 Threshold voltage and turn-on voltage

Threshold voltage, $V_T$ is an important TFT parameter indicative of the onset of drain current. [28] Unfortunately, it is not possible to uniquely define $V_T$, which sometimes leads to ambiguous or even misleading conclusions. Thus, an alternative figure-of-merit for the onset of drain current, the turn-on voltage, is introduced at the end of this section and is extensively employed in this thesis.

$V_T$ may be estimated graphically by plotting the TFT channel conductivity, $G_D$, as a function of the gate-source voltage, $V_{GS}$. [28] Using the square-law model of a TFT, [29] $I_D$ is given by

$$I_D = \mu C_I \frac{W}{L} \left( V_{DS} \left( V_{GS} - V_T \right) - \frac{V_{DS}^2}{2} \right), \tag{3.1}$$

where W is the width of the channel, L is the length from source to drain, $\mu$ is the mobility in the channel, $C_I$ is the gate insulator capacitance, $V_{DS}$ is the drain-source voltage, and $V_{GS}$ is the gate-source voltage. Evaluating $G_D$ as the derivative of $I_D$ with respect to $V_{DS}$ leads to

$$G_D = \left.\frac{dI_D}{dV_{DS}}\right|_{V_{GS}=constant} = \mu C_I \frac{W}{L}\left(V_{GS} - V_T - V_{DS}\right). \tag{3.2}$$

Notice that $G_D$ is directly proportional to $V_{GS}$, and thus, is linear with respect to $V_{GS}$. Also note that $G_D$ approaches zero as $V_{GS}$ approaches $V_T + V_{DS}$. Thus, a $G_D$-$V_{GS}$ plot should be linear and an extrapolation of the linear portion of this curve to the $V_{GS}$-axis is equal to $V_T + V_{DS}$.

Figure 3.2 shows a $G_D$-$V_{GS}$ curve for a TFT with a zinc tin oxide channel layer whose top surface is passivated with silicon dioxide. For $V_{GS} > 30$ V, the curve is linear. Using linear extrapolation of this curve to the $V_{GS}$-axis intercept yields a value of 25 V. Since this plot is taken at $V_{DS} = 1$ V, $V_T$ is estimated to be 24 V for this device.

An alternative procedure for assessing the initiation of current flow in a TFT is to employ a $\log(I_D)$-$V_{GS}$ curve and to define a turn-on voltage, $V_{ON}$, as the voltage at which $I_D$ begins to increase with increasing $V_{GS}$. [18] This definition of turn-on voltage corresponds to the applied gate bias at which an appreciable density of mobile carriers are present within the channel.

Figure 3.3 shows a $\log(I_D)$-$V_{GS}$ plot for the same TFT as shown in Fig. 3.2. $V_{ON}$ for this device is 1 V. It is evident from Fig. 3.3 that $V_{ON}$ is a more accurate

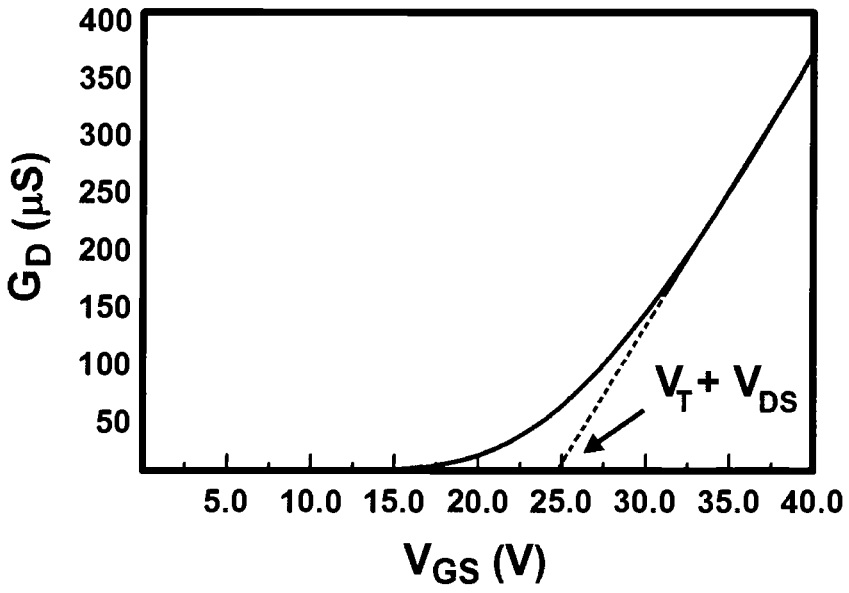


Figure 3.2: Drain conductance-drain voltage ($G_D$-$V_{DS}$) characteristic illustrating threshold voltage estimation via extrapolation of the linear portion of this curve to the $V_{GS}$-axis intercept for a passivated zinc tin oxide channel layer TFT with a width-to-length ratio of 10:1. $G_D$ is assessed as $I_D/V_{DS}$ at $V_{DS} = 1$ V.

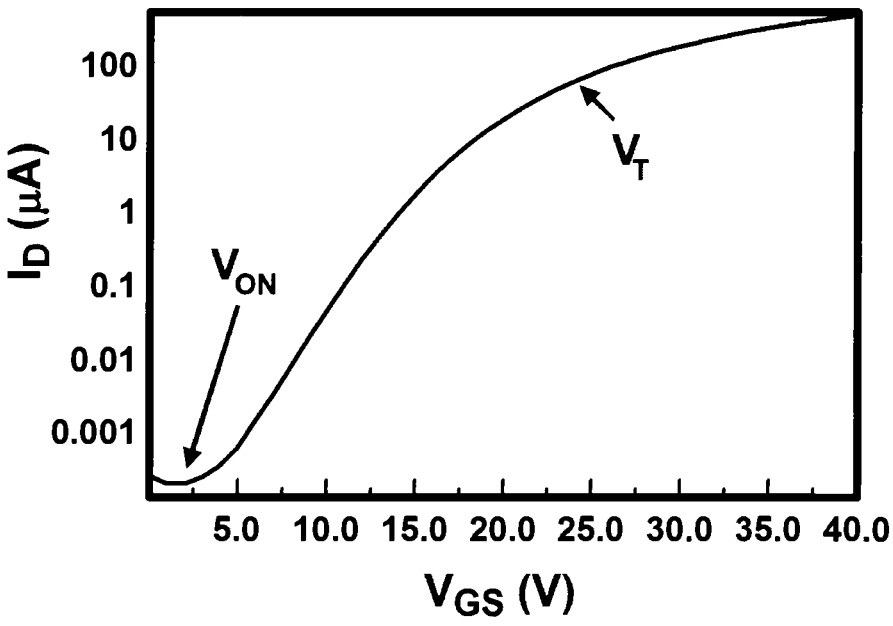


Figure 3.3: Log($I_D$-$V_{GS}$) characteristics showing the turn-on voltage, $V_{ON}$, and the threshold voltage, $V_T$ for the same device as shown in Fig. 3.2.

indicator of the onset of current than $V_T$. Thus, for the research reported in this thesis, $V_{ON}$ is preferred to $V_T$ as a TFT parameter.

### 3.3.2 Mobility

Along with threshold voltage, mobility is the other key figure of merit for transistors. Mobility is a measure of the mobile carrier transport in the channel and thus relates information about the current drive of the TFT. A higher mobility corresponds to a higher current drive. Three types of mobility are considered in this thesis: average mobility ($\mu_{AVG}$), incremental mobility ($\mu_{INC}$), and saturation mobility ($\mu_{SAT}$).[18, 28]

Average mobility is the average mobility of the all charges induced into the channel by an applied gate bias, $V_{GS}$. [18] Average mobility is calculated using

$$\mu_{AVG}(V_{GS}) = \frac{G_D(V_{GS})}{\frac{W}{L}C_I(V_{GS} - V_{ON})}\Bigg|_{V_{DS}\to 0} \tag{3.3}$$

where $G_D(V_{GS})$ is the drain conductance as a function of applied gate bias, W and L are the width and length of the TFT, and $C_I$ is the gate insulator capacitance. $G_D$ is calculated in the linear regime, as indicated by the notation $\Big|_{V_{DS}\to 0}$, such that the TFT can be modeled as a resistor. The drain conductance is also evaluated at small values of $V_{DS}$ and is calculated as [18]

$$G_D(V_{GS}) = \frac{I_D}{V_{DS}}\Bigg|_{V_{DS}\to 0}. \tag{3.4}$$

Incremental mobility is the mobility of charges incrementally added to the channel by a corresponding incremental change in $V_{GS}$. [18] Incremental mobility is calculated as [18]

$$\mu_{INC}(V_{GS}) = \frac{G'_D(V_{GS})}{\frac{W}{L}C_I}\Bigg|_{V_{DS}\to 0} \tag{3.5}$$

where G'$_D$($V_{GS}$)is the change in drain conductance due to a corresponding change to $V_{GS}$. Numerically, this is calculated as

$$G'_D(V_{GS}) = \frac{\Delta G_D}{\Delta V_{GS}}\Bigg|_{V_{DS}\to 0}. \tag{3.6}$$

Saturation mobility is extracted from a $I_D$-$V_{GS}$ curve, measured with the device held in saturation. [28] Saturation mobility is calculated as [28]

$$\mu_{SAT} = \frac{2m^2}{\frac{W}{L}C_I}\Bigg|_{Saturation} \tag{3.7}$$

where m is the slope of a plot of $I_{D,SAT}$ against ($V_{GS}$ - $V_T$.)

## 3.4 Effective width-to-length ratio

The width-to-length ratio, $\frac{W}{L}$ is a key TFT parameter. For a TFT that has a clearly defined channel, $\frac{W}{L}$ is given simply as the drawn width-to-length ratio. However, when the channel is unpatterned, peripheral current flows due to fringing electric fields outside the drawn channel. To correct for this peripheral current artifact, $\frac{W}{L}$ must be replaced by an effective width-to-length ratio, $\frac{W}{L}_{EFF}$, as derived in the remainder of this section.

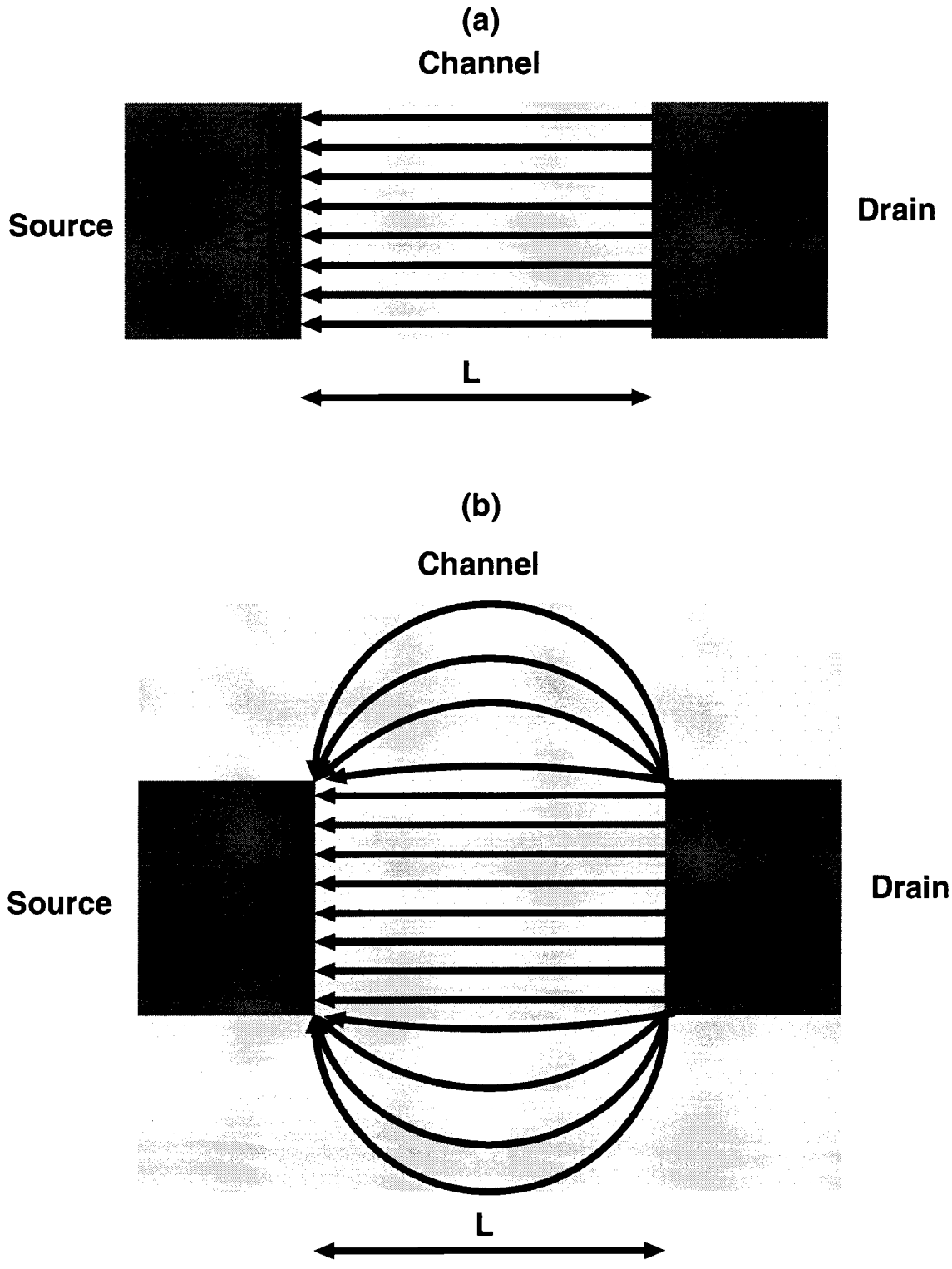


Figure 3.4: Top-down views of two TFTs, showing the current pathways in (a) a TFT with a patterned channel and (b) a TFT with an unpatterned channel.

Figure 3.4 shows top-down views of two different TFTs with identical drawn widths (W) and lengths (L) illustrating the current pathways in each device. In Fig. 3.4a, the channel is patterned. Thus, current ($I_P$) is restricted to the patterned region between the source and drain. In Fig. 3.4b, the channel is unpatterned. In this case, current is no longer restricted to the area between the source and drain. In addition to $I_P$, fringing current ($I_F$) also contributes to the total current. It is evident that the current in the TFT with an unpatterned channel is greater than in the TFT with a patterned channel. If this fringing current is not properly taken into account, it would lead to an overestimated mobility of an unpatterned TFT when mobility is extracted from experimental data.

Returning to Fig. 3.4, it can be seen that the current in the area between the source and drain is the same magnitude as the current in the patterned TFT, $I_P$. Numerically this current is equal to [28]

$$I_P = \frac{W}{L} G_{SH} V_{DS}, \tag{3.8}$$

where $G_{SH}$ is the sheet conductance and where it is assumed that $V_{DS}$ is small enough that the TFT current flow can be modeled as resistive. There is also additional current, $I_F$, outside of the area between the source and drain. An equation for $I_F$ is derived assuming that the magnitude of W has no affect on the fringing current. By shrinking W, such that W approaches 0, it can be seen that the fringing current behaves similarly to current flowing between two point contacts. The current between

two point contacts and, thus, the fringing current, for a thin film is given by [28, 30]

$$I_F = \frac{\pi}{ln2} G_{SH} V_{DS}, \tag{3.9}$$

To find the total current in the unpatterned TFT, $I_F$ and $I_P$ are added together, yielding

$$I_D = I_F + I_P = \left( \frac{\pi}{ln2} + \frac{W}{L} \right) G_{SH} V_{DS}. \tag{3.10}$$

Comparing the total current of an unpatterned device, Eq. 3.10, to the total current of a patterned device, Eq. 3.8, only the first terms differ. For the patterned device the first term is $\frac{W}{L}$, whereas it is $(\frac{\pi}{ln2} + \frac{W}{L})$ for the unpatterned device. Thus, an effective width-to-length ratio can be defined as

$$\left( \frac{W}{L} \right)_{EFF} = \left( \frac{\pi}{ln2} + \frac{W}{L} \right), \tag{3.11}$$

for an unpatterned device.

Returning to Eq. 3.10, notice that the first term, $\left(\frac{\pi}{ln2} + \frac{W}{L}\right)$ is a constant which depends on the TFT geometry, whereas the second term, $G_{SH}V_{DS}$ is a factor which depends on the current-voltage relationship used to model the TFT. Recognizing this, Eq. 3.10 can be generalized to

$$I_D = f(geometric\ parameters) g(electrical\ parameters), \tag{3.12}$$

where f and g, respectively, denote functions involving the TFT geometry and current-voltage model. In Eq. 3.10 these functions can be identified as

$$f(W,L) = \frac{\pi}{ln2} + \frac{W}{L}, \tag{3.13}$$

assuming that the fringing current is modeled using a point-contact geometry, and

$$g(V_{GS}, V_{DS}) = G_{SH} V_{DS}, \tag{3.14}$$

assuming that the TFT current flow is modeled as a resistor. If TFT current flow is modeled using square-law theory [29]

$$g(V_{GS}, V_{DS}) = \mu C_I \left( (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right), \tag{3.15}$$

where $\mu$ is mobility, $C_I$ is the insulator capacitance, $V_{GS}$ is the gate voltage referenced to the source, and $V_T$ is the threshold voltage. For this situation, if the fringing current is modeled assuming a point-contact geometry,

$$I_P = \left( \frac{\pi}{ln2} + \frac{W}{L} \right) g(V_{GS}, V_{DS}) \equiv \left( \frac{W}{L} \right)_{EFF} g(V_{GS}, V_{DS}). \tag{3.16}$$

Thus, $(\frac{W}{L})_{EFF}$, which constitutes a function of geometric parameters that includes fringing current in an unpatterned TFT, depends only upon the device geometry, but not on how the TFT current-voltage characteristics are modeled. $(\frac{W}{L})_{EFF}$ indicated in Eq. 3.11 is predicated upon a point-contact geometry to account for $I_F$. In reality,

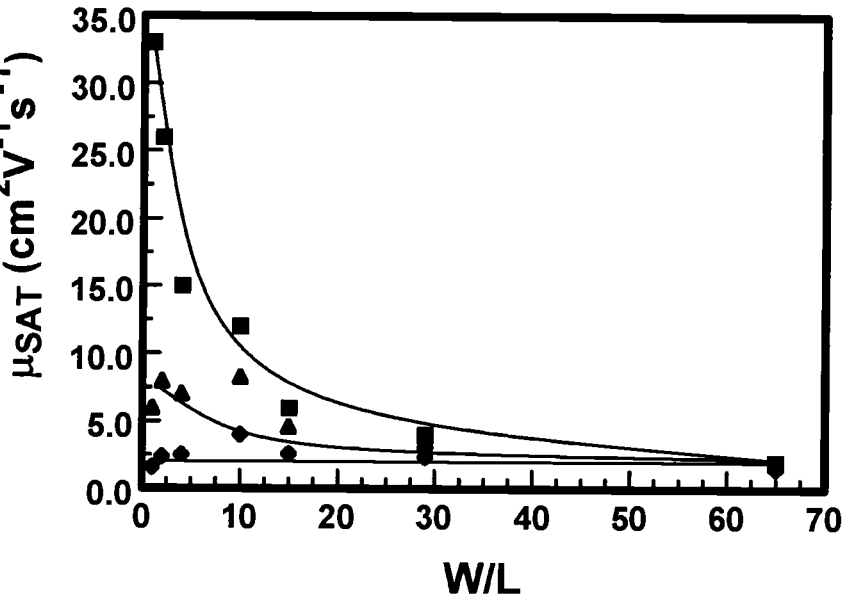


Figure 3.5: Saturation mobility as a function of $\frac{W}{L}$ for an unpatterned zinc oxide TFT. Three mobility trends are shown: mobilities obtained using the drawn $\frac{W}{L}$ (square), mobilities obtained using a point-contact model for fringing current(triangle), and mobilities obtained using an extracted equation for fringing current.

$I_F$ likely flows along the entire edges of the source and drain, such that a point-contact geometry likely underestimates the magnitude of the fringing current.

For accurate mobility estimation of a nonpatterned TFT, $(\frac{W}{L})_{EFF}$ should be used instead of $\frac{W}{L}$ in mobility assessment equations such as Eqs. 3.3 or 3.5. Since the term $\frac{\pi}{ln2}$ is equal to 4.53, the mobility can be significantly overestimated for TFTs with small $\frac{W}{L}$ ratios.

Mobility data obtained from the literature appears to confirm the existence of this fringing current artifact. Figure 3.5 shows the saturation mobility $\mu_{SAT}$ as a function of drawn $\frac{W}{L}$ for an unpatterned zinc oxide TTFT. [23] Three mobility trends are shown: mobilities (squares) obtained using the drawn $\frac{W}{L}$, mobilities (triangles) obtained using $(\frac{W}{L})_{EFF}$ assuming a point-contact geometry, and mobilities (diamonds) obtained using

$$\left(\frac{W}{L}\right)_{EFF} = \left(20 + \frac{W}{L}\right). \tag{3.17}$$

where Eq. 3.17 is deduced by varying the term $\frac{\pi}{ln2}$ in Eq. 3.11 until a flat mobility curve is achieved. The solid lines are guides for the eyes, rather than least-square fits to the data. Notice that $\mu_{SAT}$ using the drawn $\frac{W}{L}$ shows a dramatic increase as $\frac{W}{L}$ decreases. A more constant $\mu_{SAT}$ is seen by taking into account the fringing current point-contact model, although a slight curvature still exists, indicating that the point-contact model underestimates $I_F$. An almost flat mobility curve is obtained using Eq. 3.17. Rather than the reported $\mu_{SAT}$ of 27 $cm^2V^{-1}s^{-1}$, a more accurate estimate of $\mu_{SAT}$ is 2 $cm^2V^{-1}s^{-1}$, corresponding to the more physically reasonable flat mobility curve.

# 4. THIN-FILM TRANSISTOR MODELING

In this chapter, several equations are derived to model the current-voltage characteristics of thin-film transistors (TFTs). First a general equation, the conductance integral equation, is derived. This equation expresses the drain current, $I_D$, as an integral of the channel conductance with respect to the gate voltage. The conductance integral equation is then used to derive the square-law model current-voltage equation which constitutes the basic TFT model. Finally, an equation expressing $I_D$ for a depletion-mode device is derived from the conductance integral equation.

## 4.1 The conductance integral equation

Figure 4.1 shows a simple bottom-gate TFT. Source and drain contacts are idealized so that the cross section of the channel is uniform from source to drain. The source is grounded, $V_G$ is applied to the gate, and $V_D$ is applied to the drain. Voltage in the channel, $V_{CH}$, varies from 0 V at the source to $V_D$ at the drain. Conductivity of the channel varies from the source to the drain and depends on both $V_G$ and $V_{CH}$.

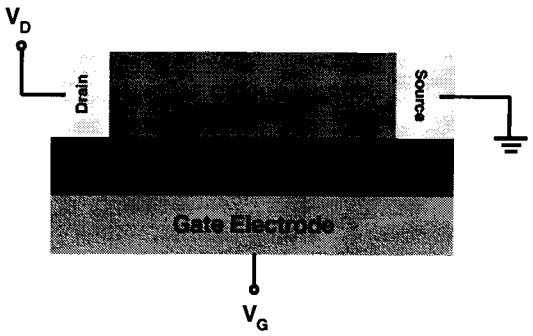


Figure 4.1: Simplified cross-section diagram of a thin-film transistor.

Shockley derives a very general field-effect transistor (FET) equation relating current to voltage for a p-channel device as [31]

$$I = \frac{Z}{L} \int_{W_S}^{W_D} g(W) dW, \tag{4.1}$$

where, employing Shockley's original notation, I is the current through the device, Z is the width of the device, L is the length of the device, W is the control voltage, $W_S$ is the control voltage evaluated at the source, $W_D$ is the control voltage evaluated at the drain, and g(W) is the sheet conductance of the channel as a function of W. It should be noted that the primary assumption underlying Eq. 4.1 is the gradual channel approximation which assumes that the change in the electric field along the channel (i.e., from the source to the drain) is much smaller than the change in the electric field in a perpendicular direction (i.e., from the gate to the channel.) An analogous equation for an n-type FET is

$$I = \frac{Z}{L} \int_{W_D}^{W_S} g(W) dW. \tag{4.2}$$

where the negative sign associated with a reversal in the direction of current flow is cancelled by the negative sign associated with a reversal of the integration limits.

The objective of the remainder of this section is to reformulate Eq. 4.2 in terms of more conventional nomenclature and directly measureable electrical quantities. To accomplish this, first consider the control voltage, W, which establishes the sheet conductance of the channel, g(W). In a TFT, W corresponds to the gate-to-channel

voltage ($V_{GC}$),

$$W = V_{GC} = V_G - V_{CH}. \tag{4.3}$$

Evaluating W at the source and at the drain to derive the limits of integration yields $V_{GS}$, the gate voltage referenced to the source, and $V_{GD}$, the gate voltage referenced to the drain. Thus, for an n-channel TFT, using a more conventional voltage notation, Eq. 4.2 can be recast as

$$I_D = \frac{Z}{L} \int_{V_{GD}}^{V_{GS}} g(V_{GC}) dV_{GC}, \tag{4.4}$$

where $g(V_{GC})$ is the sheet conductance of the channel as a function of $V_{GC}$, and $I_D$ explicitly recognizes the current of interest as the drain current.

Now, consider $g(V_{GC})$. This term is the sheet conductance of the channel with respect to $V_{GC}$. The function relating g to $V_{GC}$ can be found by analyzing the transistor in the linear region of TFT operation. The linear region is defined as the region of operation where $V_{DS} \sim 0$ V. More precisely, for a long-channel device, the linear region of operation is specified by $V_{DS} << V_{DSAT}$, where $V_{DSAT}$ is the drain voltage corresponding to the onset of the pinch-off of the channel near the drain; according to the square-law model, $V_{DSAT} = V_{GS} - V_T$, where $V_T$ is denoted the threshold voltage. [8] In the linear region of operation, the channel conductivity is approximately uniform across the channel, in accordance with the gradual channel approximation. Therefore, the sheet conductance can be expressed as

$$g(V_{GC}) = \frac{G_D^{LIN}(V_{GC})}{\frac{Z}{L}}, \tag{4.5}$$

where $G_D^{LIN}$ explicitly specifies that the channel conductance is evaluated in the linear region of operation. Also recognize that in the linear region of operation, the source is at ground potential and the drain is very close to ground potential; thus, the entire channel is essentially grounded. Therefore, $V_{GC}$ is approximately equal to the applied gate voltage $V_G$. This being the case, Eq. 4.5 may be approximated as

$$g(V_{GC}) = \frac{G_D^{LIN}(V_G)}{\frac{Z}{L}}. \tag{4.6}$$

Substituting Eq. 4.6 into Eq. 4.4 yields

$$I_D = \int_{V_{GD}}^{V_{GS}} G_D^{LIN}(V_G) dV_G. \tag{4.7}$$

This is the conductance integral equation. Equation 4.7 asserts that $I_D$ can be calculated for all $V_{DS}$ and $V_{GS}$ values if the drain conductance evaluated in the linear region is known over a sufficiently wide range of $V_G$. $I_D$ at any $V_{GS}$ and $V_{DS}$ is simply the area under a $G_D^{LIN}$-$V_G$ curve from $V_{GD}$ to $V_{GS}$, as explicitly shown in Section 4.2 of this thesis. In terms of measured quantities, $G_D^{LIN}$ is calculated as

$$G_D^{LIN}(V_G) = \left. \frac{I_D(V_{GS}, V_{DS})}{V_{DS}} \right|_{V_{DS} \to 0}. \tag{4.8}$$

An important modeling consequence of the conductance integral equation is that different functional forms of $G_D^{LIN}(V_{GS})$ give rise to different mathematical forms of $I_D(V_{GS}, V_{DS})$, as shown in the Section 4.2 and 4.3 of this thesis.

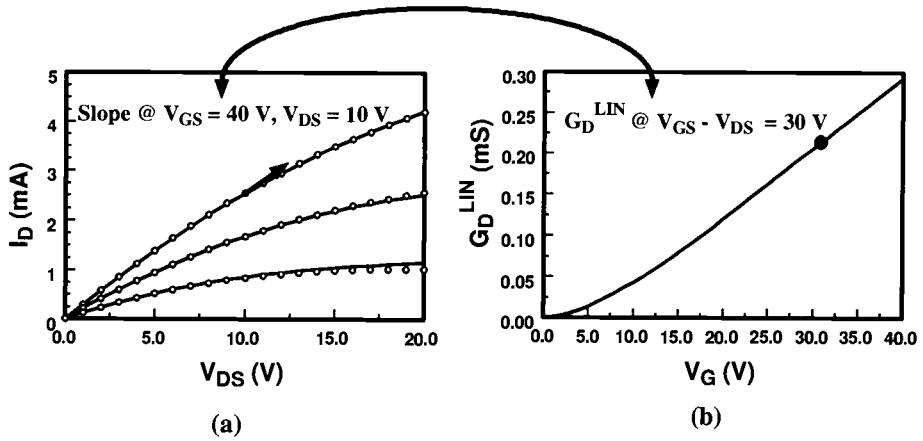


Figure 4.2: (a) $I_D$-$V_{DS}$ and (b) $G_D^{LIN}$-$V_G$ characteristics of a zinc tin oxide TFT. The solid lines shown in (a) are calculated curves from measured $G_D^{LIN}$ data shown in (b), using the conductance integral equation. The circles shown in (a) are measured data. $V_{GS}$ is decreased from 40 V (top curve, showing maximum current) to 20 V in 10 V steps. The arrow shown in (a) indicates the slope of the $I_D$-$V_{DS}$ line at $V_{GS} = 40$ V, $V_{DS} = 10$ V which is equal to $G_D^{LIN}$ at $V_G = 30$ V, as indicated by the solid circle shown in (b).

Another consequence of the conductance integral equation is that from a $G_D^{LIN}(V_{GS})$ set of data, $I_D$-$V_{DS}$ curves can be calculated. Figure 4.2a shows measured and calculated values of of $I_D$-$V_{DS}$ characteristics for a zinc tin oxide TFT; the corresponding $G_D^{LIN}$-$V_{GS}$ curve is shown in Fig. 4.2b. The circles in (a) are measured data. The solid lines in (a) are calculated using the measured $G_D^{LIN}$ data indicated in (b) and the conductance integral equation. Notice that the measured and calculated curves are nearly identical. This excellent agreement between the measured and the calculated data is typical of a large majority of the devices investigated. A few devices yielded poor agreement, which is attributed to gate leakage; the conductance integral equation does not model gate leakage.

An equally important implication of the conductance integral equation is that $G_D^{LIN}$-$V_{GS}$ can be calculated from a single $I_D$-$V_{DS}$ curve. To see this, first differen-

tiate the conductance integral equation, Eq. 4.7, with respect to $V_{DS}$,

$$\frac{dI_D(V_{GS}, V_{GD})}{dV_{DS}} = \frac{d}{dV_{DS}} \int_{V_{GD}}^{V_{GS}} G_D^{LIN}(V_G) dV_G. \tag{4.9}$$

Next recognize that $V_{GD}$ = $V_{GS}$ - $V_{DS}$ and also that $V_{GS}$, $V_{GD}$, and $V_{DS}$ are not independent of one another so that the drain current functional dependence can be equivalently expressed as $I_D(V_{GS}, V_{DS})$. Solution of the integral on the right side of Eq. 4.9 is accomplished using [32]

$$\frac{d}{dx} \int_{u(x)}^{v(x)} f(t)dt = f(v)\frac{dv}{dx} - f(u)\frac{du}{dx} \tag{4.10}$$

which, after rearrangement, results in

$$G_D^{LIN}(V_{GS} - V_{DS}) = \frac{dI_D(V_{GS}, V_{DS})}{dV_{DS}}. \tag{4.11}$$

Equation 4.11 states that the slope of an $I_D$-$V_{DS}$ curve evaluated at $V_{DS}$ and $V_{GS}$ yields $G_D^{LIN}$ evaluated at a value of $V_{GS}$ - $V_{DS}$. To see this, return to Fig. 4.2. The top curve shown in Fig 4.2a corresponds to $V_{GS}$ = 40 V. The slope of this $I_D$-$V_{DS}$ curve at $V_{DS}$ = 10 V, as indicated by the arrow, is equal to $G_D^{LIN}$ assessed at a value of $V_{GS}$ - $V_{DS}$ = 40 V - 10 V = 30 V, as indicated in Fig. 4.2b by the solid circle. This method for extracting $G_D^{LIN}(V_G)$ can aid in channel mobility estimation in situations in which accurate $G_D^{LIN}$ assessment is not possible because the linear region of operation for an $I_D$-$V_{DS}$ curve is dominated by contact or series resistance.

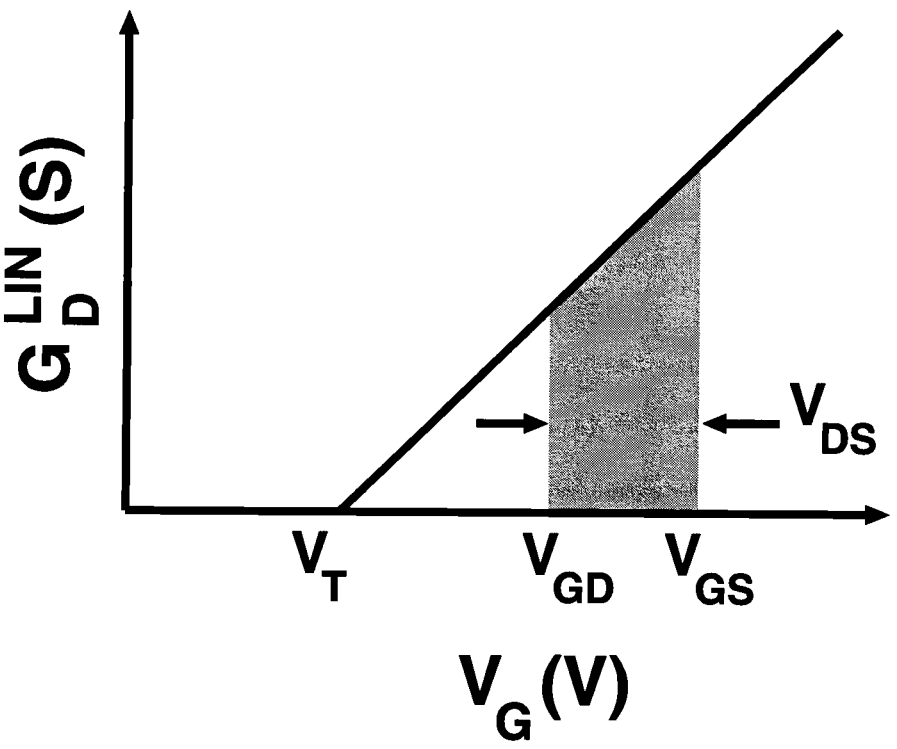


Figure 4.3: $G_D^{LIN}$-$V_G$ plot for an idealized transistor. The equation of the line is $\frac{Z\mu C_I}{L}(V_G - V_T)$. $V_{DS}$ corresponds to the difference between $V_{GS}$ and $V_{GD}$ The area of the shaded region under the $G_D^{LIN}$ curve evaluated between $V_{GS}$ and $V_{GD}$ corresponds to $I_D$.

## 4.2 Enhancement-mode current model

In this section, the conductance integral equation, Eq. 4.7, is used to derive an $I_D(V_{GS},V_{DS})$ equation for an enhancement-mode TFT. The equation derived is then shown to be equivalent to the square-law model for a TFT. [29]

Figure 4.3 shows a $G_D^{LIN}$-$V_G$ characteristic for an idealized transistor, in which the source-drain conductance in the linear region is modeled as [8]

$$G_D^{LIN} = \frac{Z\mu C_I}{L}(V_G - V_T), \tag{4.12}$$

where $\mu$ is the carrier mobility (assumed to be constant with respect to $V_{GS}$) and $V_T$ is the threshold voltage. $V_{GS}$ is the applied voltage from the gate to the source. $V_{GD}$ is the applied voltage from the gate to the drain. $V_{DS}$ is the difference between $V_{GS}$ and $V_{GD}$. The shaded region area corresponds to $I_D$, as described by Eq. 4.7.

Now consider the mathematical consequence of Fig. 4.3 in conjunction with the conductance integral equation. Substituting Eq. 4.12 into Eq. 4.7,

$$I_D = \int_{V_{GD}}^{V_{GS}} \frac{Z\mu C_I}{L}(V_G - V_T)dV_G = \frac{Z\mu C_I}{L}\left[\frac{V_{GS}^2}{2} - V_{GS}V_T - \frac{V_{GD}^2}{2} + V_{GD}V_T\right]. \quad (4.13)$$

Notice from Fig. 4.3 that

$$V_{GD} = V_{GS} - V_{DS}. \quad (4.14)$$

Substituting Eq. 4.14 into Eq. 4.13 and collecting terms yields

$$I_D = \frac{Z\mu C_I}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]. \quad (4.15)$$

This equation is valid for $V_{GD}$ greater than $V_T$. Returning to Fig. 4.3, notice that for values of $V_G$ less than $V_T$, $G_D^{LIN}$ is zero and there is no area under the $G_D^{LIN}$-$V_G$ curve. If $V_{GS}$ is held constant, the maximum area of the shaded region is reached when $V_{GD} = V_T$. At this point, the channel is pinched off and saturation occurs so that

$$I_D \equiv I_{DSAT} = \frac{Z\mu C_I}{2L}(V_{GS} - V_T)^2. \quad (4.16)$$

As $V_{GD}$ is reduced below $V_T$, or if the gate is held constant as $V_{DS}$ is increased above $V_{GS}$ - $V_T$, the area of the shaded region, $I_D$, does not increase. $I_D$ saturates at this

point. Decreasing $V_{GD}$ below $V_T$ or increasing $V_{DS}$ above $V_{GS}$ - $V_T$ has no effect on $I_D$.

Equations 4.15 and 4.16 correspond to the square-law model for an ideal long-channel transistor. [29] Thus, the square-law model is derived from the conductance integral equation, Eq. 4.7, assuming that the linear region channel conductance depends linearly on the gate voltage

## 4.3 Depletion-mode current model

In this section, the current-voltage characteristics are derived for a depletion-mode TFT. First, expressions for $G_D^{LIN}(V_G)$ are developed. Then, these expressions for $G_D^{LIN}(V_G)$ are substituted into the conductance integral equation in order to generate a corresponding set of current-voltage relationships.

### 4.3.1 Depletion-mode conductance

Consider an n-channel TFT with a carrier concentration $N_D$. Application of a positive bias to the gate induces an electron accumulation region in the channel. In contrast, application of a negative bias results in depletion of the channel. Since appreciable drain current can flow in a depletion-mode TFT in both depletion and accumulation, the channel conductance must be modeled in both regions of operation.

For a depletion-mode TFT, the linear region channel conductance, $G_D^{LIN}$, is modeled as [8]

$$G_D^{LIN} = \frac{Z}{L}\mu q N_e, \tag{4.17}$$

where $N_e$ is the number of mobile electrons per $cm^2$ of gate area. In accumulation, the electron density in the channel is comprised of bulk electrons already present due to doping and of electrons which are induced into the channel as a consequence of the application of a gate voltage, [8]

$$N_e = N_D t_S + V_G C_I, \tag{4.18}$$

where $t_S$ is the channel thickness. Thus, for a depletion-mode TFT operating in accumulation

$$G_D^{LIN}\Big|_{ACC} = \frac{Z}{L}\mu q(N_D t_S + V_G C_I). \tag{4.19}$$

In depletion, the electron density in the channel decreases as the gate voltage-induced depletion region widens,

$$N_e = N_D(t_S - W_{DEP}), \tag{4.20}$$

where $W_{DEP}$ is the depletion space charge width. $W_{DEP}$ is given by [33]

$$W_{DEP} = \left(\frac{\varepsilon_S^2}{C_I^2} - \frac{2V_G\varepsilon_S}{qN_D}\right)^{\frac{1}{2}} - \frac{\varepsilon_S}{C_I}, \tag{4.21}$$

where $\varepsilon_S$ is the permittivity of the channel. Factoring out $t_S$ from the right hand side of Eq. 4.21 and defining a new term, $C_S = \frac{\varepsilon_S}{t_S}$, corresponding to the semiconductor (i.e., the channel) capacitance yields

$$W_{DEP} = t_S\left[\left(\frac{C_S^2}{C_I^2} - \frac{2V_G\varepsilon_S}{qN_D t_S^2}\right)^{\frac{1}{2}} - \frac{C_S}{C_I}\right], \tag{4.22}$$

Introducing the pinch-off voltage, $V_P$, which corresponds to the gate voltage required to completely deplete the channel if no insulator is present and is calculated as [8]

$$V_P = -\frac{qN_D t_S^2}{2\varepsilon_S}. \tag{4.23}$$

Substituting Eq. 4.23 into Eq. 4.22 yields

$$W_{DEP} = t_S \left[ \left( \frac{C_S^2}{C_I^2} + \frac{V_G}{V_P} \right)^{\frac{1}{2}} - \frac{C_S}{C_I} \right]. \tag{4.24}$$

Substituting Eq. 4.24 into Eq. 4.20 yields

$$N_e = N_D t_S \left[ 1 + \frac{C_S}{C_I} - \left( \frac{C_S^2}{C_I^2} + \frac{V_G}{V_P} \right)^{\frac{1}{2}} \right]. \tag{4.25}$$

Finally, substituting Eq. 4.25 into Eq. 4.17 yields the $G_D^{LIN}$ relation appropriate for a depletion-mode TFT operating in depletion

$$G_D^{LIN}\Big|_{DEPL} = \frac{Z}{L}\sigma t_S \left[ 1 + \frac{C_S}{C_I} - \left( \frac{C_S^2}{C_I^2} + \frac{V_G}{V_P} \right)^{\frac{1}{2}} \right], \tag{4.26}$$

where $\sigma$ is the conductivity of the channel and is calculated as

$$\sigma = \mu q N_D. \tag{4.27}$$

Equations 4.19 and 4.26 constitute the $G_D^{LIN}$ relations required to generate the current-voltage characteristic equations appropriate for a depletion-mode TFT.

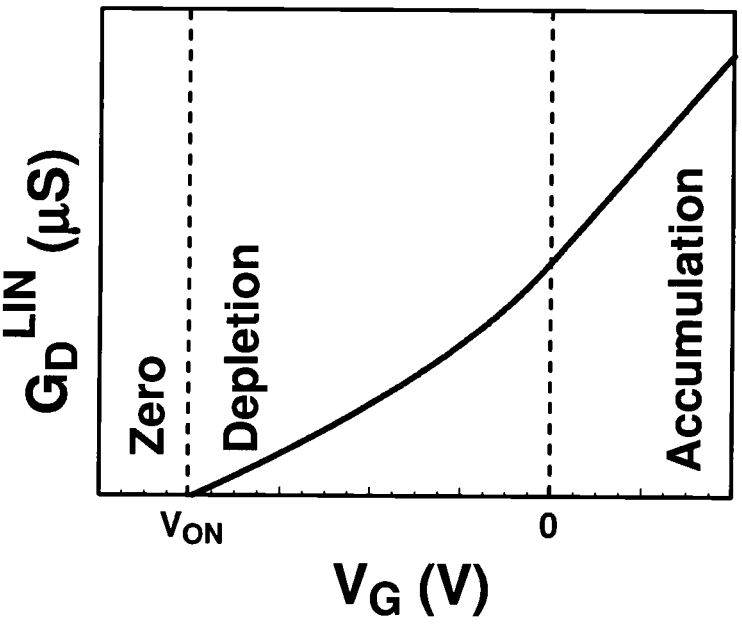


Figure 4.4: $G_D^{LIN}$-$V_G$ plot for an idealized depletion-mode TFT.

### 4.3.2 Depletion-mode current-voltage relationship

Figure 4.4 shows the $G_D^{LIN}$-$V_G$ characteristics of an idealized n-channel depletion-mode TFT. Three regions of conductance are shown; the zero region is where the conductance is zero, the depletion region is where $G_D^{LIN}\Big|_{DEPL}$ is evaluated via Eq. 4.26, and the accumulation region is where $G_D^{LIN}\Big|_{ACC}$ is modeled according to Eq. 4.19. The transition from the zero region to the depletion region is established by the turn-on voltage, $V_{ON}$, which is calculated by setting Eq. 4.26 equal to zero and solving for $V_G$, yielding

$$V_G\left(G_D^{LIN}\Big|_{DEPL}=0\right)\equiv V_{ON}=V_P-\frac{qN_Dt_s}{C_I}. \tag{4.28}$$

Notice that the first term on the right side of Eq. 4.28 corresponds to the pinch-off voltage, $V_P$, which is the voltage dropped across the semiconductor when the channel is fully depleted. The second term, $\frac{-qN_D t_s}{C_I}$, is the voltage dropped across the insulator when the channel is fully depleted. Note that $V_P$ is a negative term; thus $V_{ON}$ is always a negative quantity. Returning to Fig. 4.4, notice that the transition from depletion to accumulation occurs at 0 V.

Figure 4.5 shows the cross section and corresponding $G_D^{LIN}$-$V_G$ plots of three operating regions for an n-channel, depletion-mode TFT. Figure 4.5a shows the device with applied voltages such that a depletion region exists in the channel from the source to drain. Figure 4.5b shows the device with applied voltages such that an accumulation region exists in the channel from the source to the drain. Figure 4.5c shows the intermediate case in which the channel is partially depleted and partially accumulated.

Consider the depleted channel case indicated in Fig. 4.5a. As indicated in this figure, a depletion region exists in the channel from the source to the drain, when both $V_{GD}$ and $V_{GS}$ are between $V_{ON}$ and zero volts. In this region of operation, the conductance through the entire channel is modeled using Eq. 4.26. Substituting Eq. 4.26 into the conductance integral equation, Eq. 4.7, yields

$$I_D = \frac{Z}{L}\sigma t_S \left[ \left(1 + \frac{C_S}{C_I}\right) V_{DS} + \frac{2}{3} V_P \left( \left( \frac{C_S^2}{C_I^2} + \frac{V_{GS}}{V_P} \right)^{\frac{3}{2}} - \left( \frac{C_S^2}{C_I^2} + \frac{V_{GD}}{V_P} \right)^{\frac{3}{2}} \right) \right] \quad (4.29)$$

Notice that for values of $V_G$ less than $V_{ON}$, $G_D^{LIN}$ is zero and there is no area under the $G_D^{LIN}$-$V_G$ curve. If $V_{GS}$ is held constant, the maximum $I_D$ is reached when

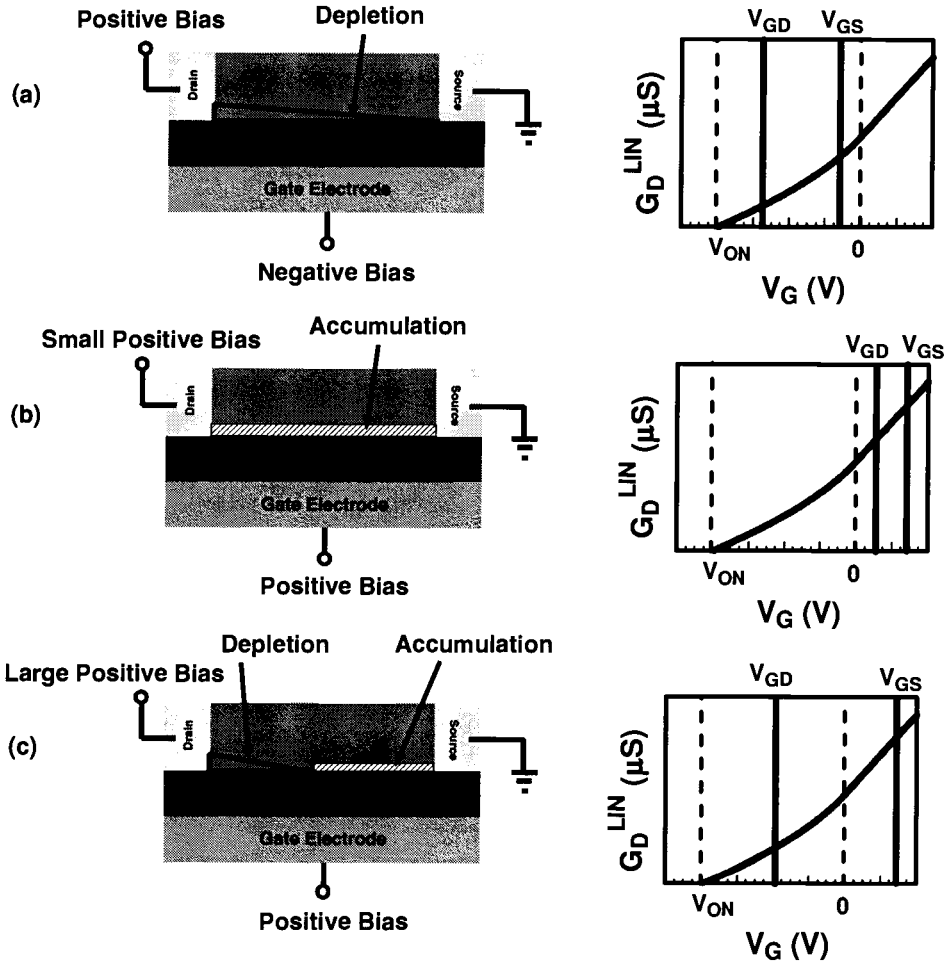


Figure 4.5: Depletion-mode TFT cross section and corresponding $G_D^{LIN}$-$V_G$ plot showing three operating conditions: (a) the channel has a depletion region extending from the source to the drain, (b) the channel has an accumulation region extending from the source to the drain, and (c) the channel is depleted near the drain and is accumulated near the source. Note that the magnitude of $V_{GD}$ and $V_{GS}$ with respect to $V_{ON}$ and zero volts determine which operating region applies.

$V_{GD} = V_{ON}$. At this point, the channel is pinched off and saturation occurs so that

$$I_D = \frac{Z}{L}\sigma t_S \left[ \left(1 + \frac{C_S}{C_I}\right) V_{DSAT} + \frac{2}{3} V_P \left( \left( \frac{C_S^2}{C_I^2} + \frac{V_{GS}}{V_P} \right)^{\frac{3}{2}} - \left( \frac{C_S^2}{C_I^2} + \frac{V_{ON}}{V_P} \right)^{\frac{3}{2}} \right) \right], \tag{4.30}$$

where

$$V_{DS}(V_{GD} = V_{ON}) \equiv V_{DSAT} = V_{GS} - V_{ON}. \tag{4.31}$$

As $V_{GD}$ is reduced below $V_{ON}$, or if the gate is held constant as $V_{DS}$ is increased above $V_{GS}$ - $V_{ON}$, $I_D$ does not increase. Thus, $I_D$ saturates at this point. Equations 4.29 and 4.30 constitute the pre-pinch-off and post-pinch-off, respectively, current-voltage characteristics describing an n-channel, depletion-mode TFT operating in full channel depletion, as illustrated in Fig 4.5a.

Next, consider the accumulated channel case shown in Fig. 4.5b. The channel near the source is accumulated when $V_{GS} > 0$ V and the channel near the drain is accumulated when $V_{GD} > 0$ V. Because accumulation occurs throughout the entire length of channel, $G_D^{LIN}$ is calculated using Eq. 4.19. Substituting Eq. 4.19 into the conductance integral equation, Eq. 4.7, yields

$$I_D = \frac{Z}{L} \left[ \mu C_I \left( (V_{GS}) V_{DS} - \frac{V_{DS}^2}{2} \right) + \sigma t_s V_{DS} \right]. \tag{4.32}$$

Equation 4.32 is the pre-pinch-off current-voltage characteristic describing an n-channel, depletion-mode TFT operating in full channel accumulation, as illustrated in Fig. 4.5b. Note that this equation corresponds to the pre-pinch-off square-law

model, representing the accumulation channel current, in parallel with a resistor, representing current through the 'bulk' channel.

Beginning with Fig. 4.5b, as the drain voltage is increased, such that $V_{GD}$ decreases below 0 V, the channel near the drain is depleted, resulting in the situation shown in Fig. 4.5c. Because both an accumulation region and a depletion region exist along the length of the channel, both Eq. 4.19 and Eq. 4.26 must be used to calculate the channel conductance. Substituting both of these into the conductance integral equation, Eq. 4.7, yields

$$I_D = \left[ \int_{V_{GD}}^{0} G_D^{LIN}(V_G) \Big|_{ACC} dV_G + \int_{0}^{V_{GS}} G_D^{LIN}(V_G) \Big|_{DEP} dV_G \right]. \tag{4.33}$$

Notice that this results in two integrals, one integral evaluating $G_D^{LIN}$ for the accumulation region and one integral evaluating $G_D^{LIN}$ for the depletion region. Evaluating this integral leads to

$$I_D = I_{ACC} + I_{DEP}, \tag{4.34}$$

where

$$I_{ACC} = \frac{Z\mu C_I}{2L}(V_{GS})^2 + \frac{Zt_s\sigma}{L}(V_{GS}), \tag{4.35}$$

and

$$I_{DEP} = \frac{Z}{L}\sigma t_S \left[ \left(1 + \frac{C_S}{C_I}\right)(V_{DS} - V_{GS}) + \frac{2}{3}V_P \left( \frac{C_S^3}{C_I^3} - \left( \frac{C_S^2}{C_I^2} + \frac{V_{GD}}{V_P} \right)^{\frac{3}{2}} \right) \right]. \tag{4.36}$$

Decreasing $V_{GD}$ below $V_{ON}$ again leads to a saturated $I_D$ which is calculated as

$$I_D = I_{ACC} + I_{DEP2}, \tag{4.37}$$

where

$$I_{DEP2} = \frac{Z}{L}\sigma t_S \left[ \left(1 + \frac{C_S}{C_I}\right)(V_{ON}) + \frac{2}{3}V_P \left( \frac{C_S^3}{C_I^3} - \left( \frac{C_S^2}{C_I^2} + \frac{V_{ON}}{V_P} \right)^{\frac{3}{2}} \right) \right]. \tag{4.38}$$

Equations 4.34 and 4.37 constitute the pre-pinch-off and post-pinch-off current-voltage characteristics describing an n-channel, depletion-mode TFT operating in a partially depleted and partially accumulated channel, as illustrated in Fig. 4.5c.

Collectively, Eqs. 4.29 - 4.38 comprise the basic current-voltage equations constituting the comprehensive n-channel, depletion-mode TFT model. A more detailed description of this model is provided in Table 4.1. Five regimes of TFT operation are indicated: depletion (DEPL), depletion-saturation (DEPL-SAT), accumulation (ACC), accumulation-depletion (ACC-DEPL), and accumulation-saturation (ACC-SAT). The corresponding constraint relations specify $V_{GS}$ and $V_{DS}$ for each of the five regimes of operation.

Table 4.1: Summary of the comprehensive n-channel depletion-mode TFT model.

| | Variable definition | Equation |
|---|---|---|
| | Channel conductance | $\sigma = \mu q N_D$ |
| | Pinch-off voltage | $V_P = \frac{qN_D t_S^2}{2\varepsilon_S}$ |
| | Turn-on voltage | $V_{ON} = V_P - \frac{qN_D t_s}{C_I}$ |
| | Saturation voltage | $V_{DSAT} = V_{GS} - V_{ON}$ |
| | Channel capacitance | $C_S = \frac{\varepsilon_S}{t_S}$ |
| | ACC-DEPL accumulation current | $I_{ACC} = \frac{Z\mu C_I}{2L}(V_{GS})^2 + \frac{Zt_s\sigma}{L}(V_{GS})$ |
| | ACC-DEPL depletion current | $I_{DEP} = \frac{Z}{L}\sigma t_S \left[\left(1+\frac{C_S}{C_I}\right)(V_{DS}-V_{GS}) + \frac{2}{3}V_P\left(\frac{C_S^3}{C_I^3} - \left(\frac{C_S^2}{C_I^2}+\frac{V_{GD}}{V_P}\right)^{\frac{3}{2}}\right)\right]$ |
| | ACC-DEPL depletion-saturation current | $I_{DEP2} = \frac{Z}{L}\sigma t_S \left[\left(1+\frac{C_S}{C_I}\right)(V_{ON}) + \frac{2}{3}V_P\left(\frac{C_S^3}{C_I^3} - \left(\frac{C_S^2}{C_I^2}+\frac{V_{ON}}{V_P}\right)^{\frac{3}{2}}\right)\right]$ |

| Regime | Equation | Constraints |
|---|---|---|
| DEPL | $I_D = \frac{Z}{L}\sigma t_S \left[\left(1+\frac{C_S}{C_I}\right)V_{DS} + \frac{2}{3}V_P\left(\left(\frac{C_S^2}{C_I^2}+\frac{V_{GS}}{V_P}\right)^{\frac{3}{2}} - \left(\frac{C_S^2}{C_I^2}+\frac{V_{GD}}{V_P}\right)^{\frac{3}{2}}\right)\right]$ | $V_{GS} \leq 0$ V, $V_{DS} \leq V_{DSAT}$ |
| DEPL-SAT | $I_D = \frac{Z}{L}\sigma t_S \left[\left(1+\frac{C_S}{C_I}\right)(V_{GS}-V_{ON}) + \frac{2}{3}V_P\left(\left(\frac{C_S^2}{C_I^2}+\frac{V_{GS}}{V_P}\right)^{\frac{3}{2}} - \left(\frac{C_S^2}{C_I^2}+\frac{V_{ON}}{V_P}\right)^{\frac{3}{2}}\right)\right]$ | $V_{GS} \leq 0$ V, $V_{DS} > V_{DSAT}$ |
| ACC | $I_D = \frac{Z}{L}\left(\mu C_I\left((V_{GS})V_{DS} - \frac{V_{DS}^2}{2}\right) + \sigma t_s V_{DS}\right)$ | $V_{GS} > 0$ V, $V_{DS} \leq V_{GS}$ |
| ACC-DEPL | $I_D = I_{ACC} + I_{DEP}$ | $V_{GS} > 0$ V, $V_{GS} < V_{DS} \leq V_{DSAT}$ |
| ACC-SAT | $I_D = I_{ACC} + I_{DEP2}$ | $V_{GS} > 0$ V, $V_{DS} > V_{DSAT}$ |
| Model parameters | Geometric-based | Z, L, $t_S$, $C_I$ |
| | Channel-based | $N_D$, $\mu$, $\varepsilon_S$ |

Table 4.2: Parameters used in the comprehensive n-channel depletion-mode TFT model to simulate the current-voltage curves shown in Fig. 4.6 and Fig. 4.7.

| | |
|---|---|
| Mobility ($cm^2V^{-1}s^{-1}$) | 5 |
| Intrinsic Carrier Concentration ($cm^{-3}$) | $3 \times 10^{17}$ |
| Relative Insulator Dielectric Constant | 3.9 |
| Semiconductor Dielectric Constant | 10 |
| Insulator Layer Thickness (nm) | 200 |
| Channel Layer Thickness (nm) | 80 |
| Width-to-Length Ratio | 10 |

Figure 4.6 shows a representative set of $I_D$-$V_{DS}$ characteristics simulated using the comprehensive n-channel, depletion-mode TFT model. The approximate regions of operation defined in Table 4.1 are labeled in Fig. 4.6. The parameters that are used for this simulation are collected in Table 4.2. The $I_D$ curves shown in Fig. 4.6 exhibit saturation and appear very similar to characteristics typically observed for zinc tin oxide depletion-mode TFTs fabricated during this thesis research.

Figure 4.7 shows the $\log(I_D)$-$V_{GS}$ curve corresponding to Fig. 4.6. This curve is assessed in the saturation region, such that $V_{DS} = V_{DSAT}$. $V_{ON}$ for this device is ~-24 V. Notice that there is a sharp increase in the current at $V_{GS}$ above $V_{ON}$, which levels off with increasing $V_{GS}$. Again, this curve is similar to characteristics typically observed for zinc tin oxide depletion-mode TFTs fabricated during this thesis research.

It can be shown that the comprehensive n-channel, depletion-mode TFT model simplifies to the square-law model in the limit $C_S >> C_I$. There are several ways to justify the limit $C_S >> C_I$. Perhaps the simplest justification involves recognizing that if this limit is satisfied, all of the voltage applied to the gate of the TFT is

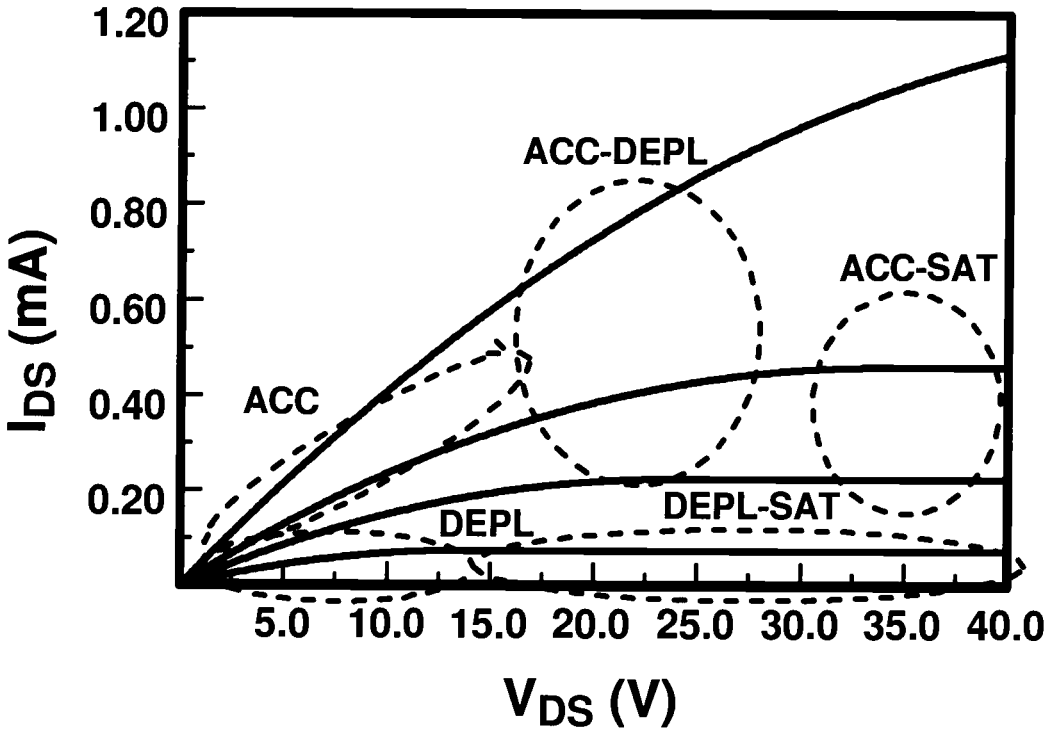


Figure 4.6: $I_D$-$V_{DS}$ characteristic simulated using the comprehensive depletion-mode TFT model of Table 4.1 using the model parameters listed in Table 4.2. The five regimes of device operation are indicated. $V_{GS}$ is decreased from 30 V (top curve, showing maximum current) to -20 V in 10 V steps.

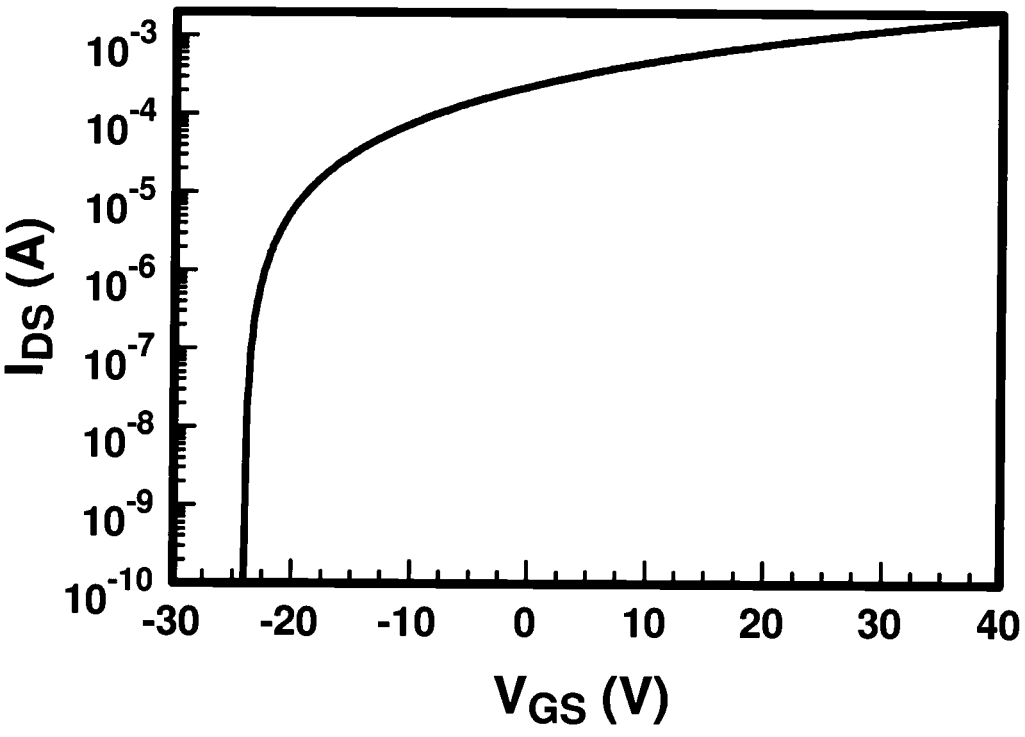


Figure 4.7: Log($I_D$)-$V_{GS}$ characteristic simulated using the depletion-mode TFT model of Table 4.1 using the model parameters listed in Table 4.2. $V_{ON}$ for this device is $\sim$ -24 V. The current approaches zero, as $V_{GS}$ approaches $V_{ON}$.

dropped across the insulator. This implies that the charge induced in the channel is equal to $C_I(V_{GS}\text{-}V_{ON})$ so that

$$G_D^{LIN} = \frac{Z}{L}\mu C_I(V_{GS} - V_{ON}), \tag{4.39}$$

which is identical to Eq. 4.12, which is used to derive the square-law model, except that $V_T$ is replaced by $V_{ON}$.

Figure 4.8 elucidates how the limit $C_S >> C_I$ affects $G_D^{LIN}$. In the case where $\frac{C_S}{C_I}$ is large, the far right curve, $G_D^{LIN}$ is almost a straight line, indicating consistency with the square-law model. In contrast, when $\frac{C_S}{C_I}$ is small, the far left curve, a noticeable deviation from linearity exists such that the square-law model would be a poor approximation for this case. Typical $\frac{C_S}{C_I}$ values for zinc tin oxide TFTs fabricated during this thesis research vary between 3-6.

Note that the model presented in this section includes both 'bulk' conduction and interface conduction. In the plots presented in this chapter bulk and interface mobilities are assumed to be identical, which may not be the case in an actual device where the interface mobility is expected to be somewhat smaller than the bulk mobility.

## 4.4 Conclusion

In this chapter, several equations are derived to model the current-voltage characteristics of TFTs. First a general equation, the conductance integral equation, is derived, which expresses the drain current, $I_D$, as an integral of the channel conductance with respect to the gate voltage. The conductance integral equation is then

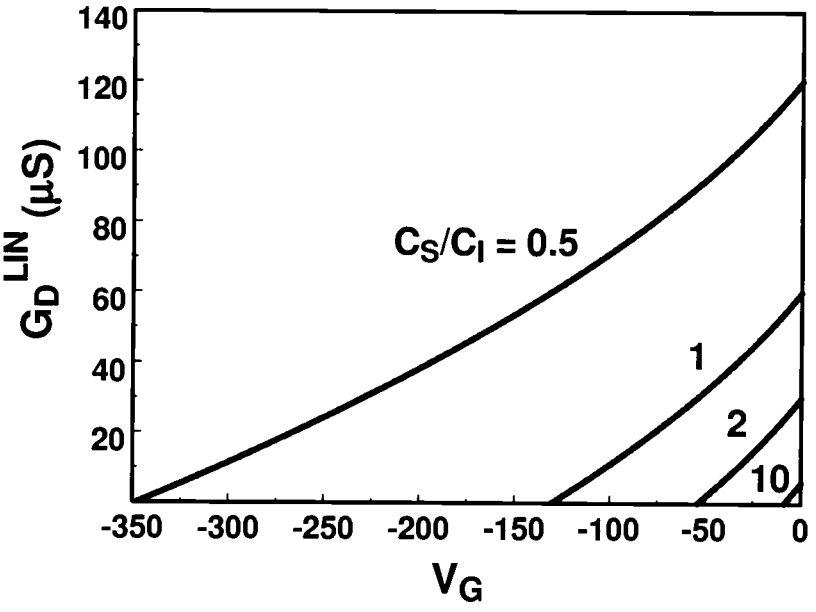


Figure 4.8: $G_D^{LIN}$-$V_G$ plot for various channel capacitance-insulator capacitance ratios, $\frac{C_S}{C_I}$. As $\frac{C_S}{C_I}$ increases, the $G_D^{LIN}$-$V_G$ curve becomes linear.

used to derive the square-law model current-voltage equation which constitutes the basic TFT model. Finally, a comprehensive set of equations expressing $I_D$ for a depletion-mode device is derived from the conductance integral equation.

# 5. SEQUENTIAL SPUTTERING AND ANNEALING METHODOLOGY

## 5.1 Introduction

A novel deposition methodology is employed for exploratory development of a class of high-performance transparent thin-film transistor (TTFT) channel materials involving oxides composed of heavy-metal cations with $(n\text{-}1)d^{10}ns^0$ ($n \geq 4$) electronic configurations. The method involves sequential RF sputter deposition of thin, single cation oxide layers and subsequent post-deposition annealing in order to obtain a multi-component oxide thin film. The viability of this rapid materials development methodology is demonstrated through the realization of high-performance TTFTs with channel layers composed of zinc oxide/tin oxide, and tin oxide/indium oxide.

A fundamental challenge inherent in utilizing HMC ternary oxides involves basic materials selection. Since fifteen elements have been identified as candidate HMCs [2], i.e., Cu, Zn, Ga, Ge, As, Ag, Cd, In, Sn, Sb, Au, Hg, Tl, Pb, and Bi, there are 105 possible ternary oxide combinations. Moreover, the composition of a ternary oxide, in terms of the relative amount of each single cation oxide constituent, is variable. For example, the fraction of ZnO to $SnO_2$ in zinc tin oxide may be specified as $(ZnO)_x(SnO_2)_{1-x}$, where $0 \leq x \leq 1$, underscoring that the relative single cation oxide composition is continuously variable from zero to one. Finally, there is no reason to restrict attention exclusively to ternary oxide combinations; it is possible that optimal HMC materials will involve multiple combinations of single

cation constituent oxides. These considerations suggest that HMC multi-component oxide materials selection and optimization may be complicated and time-consuming.

The purpose of this chapter is to describe an effective approach for the exploration of HMC multi-component oxides. The method involves sequential RF sputter deposition of thin binary oxide layers and subsequent interdiffusion via post-deposition annealing. The viability of this rapid materials development methodology as a screening technique for assessing the potential of multi-component oxide combinations is demonstrated via identification of indium tin oxide as a promising material system for TTFT channel layer applications.

## 5.2 Deposition technique

Devices discussed in this chapter are transparent, bottom-gate TTFTs as generically described in Chapter 3. Device fabrication procedures specific to the sequential sputtering and annealing methodology are summarized in the following paragraph.

Consider zinc tin oxide as an example of the multi-component oxide channel layer deposition procedure employed. Deposition of layered zinc tin oxide is accomplished by first positioning the ITO/ATO substrate directly in front of a 2" $SnO_2$ target to deposit a layer of $SnO_2$, after which the substrate is moved directly in front of a 2" ZnO target to deposit a layer of ZnO. The deposition duration is approximately 30 seconds for each layer. Typically, this process is repeated for a total of four layers, two $SnO_2$ layers and two ZnO layers. A 2" $Zn_2SnO_4$ $[(ZnO)_{0.67}(SnO_2)_{0.33}]$ target and identical RF sputtering deposition processing parameters are used to fabricate TTFTs for comparison.

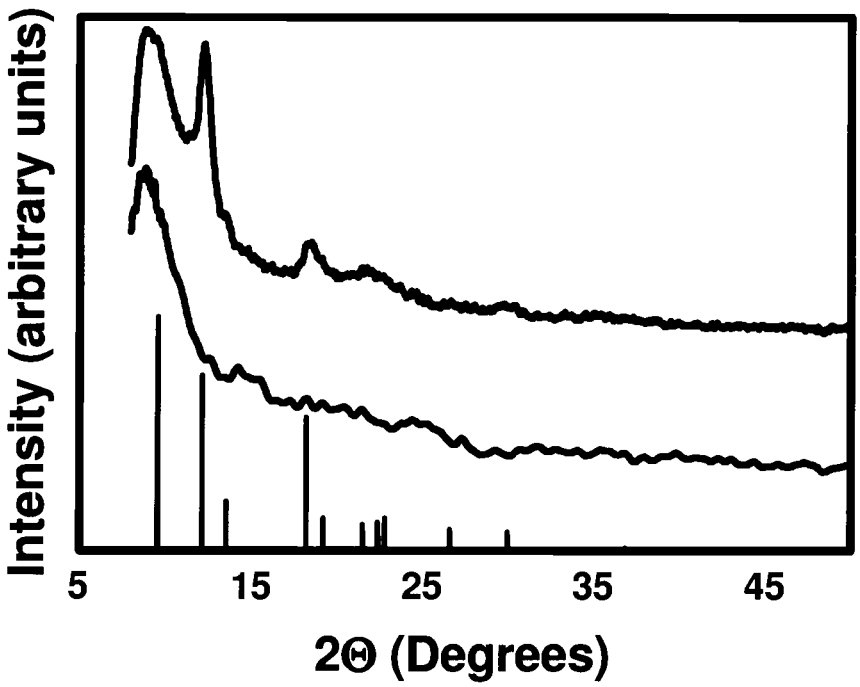


Figure 5.1: Glancing angle x-ray diffraction patterns from a layered structure of zinc oxide and tin oxide (top curve) and a corresponding plot of zinc tin oxide sputtered from a single target (bottom curve). Vertical bars represent $SnO_2$ (JCPDS # 41-1445.) The zinc tin oxide sample sputtered from a single target shows very strong amorphous tendency. The layered sample exhibits a strong amorphous tendency, superimposed on a background of crystallized tin oxide.

## 5.3 Results and discussion

A 150 nm XRD layered sample consists of 20 total layers of zinc oxide and tin oxide, tin oxide being the bottom layer. The sample is deposited directly on Corning 1737 glass substrates and annealed at 600°C. All other processing conditions are as described previously. A corresponding 120 nm zinc tin oxide sample is deposited directly on Corning 1737 glass substrate and annealed at 600°C for comparison. Figure 5.1 shows an XRD pattern of layered zinc oxide/tin oxide and zinc tin oxide samples.

The layered structure appears to be an amorphous film of zinc tin oxide with phase-segregated $SnO_2$ inclusions. The zinc tin oxide sample exhibits a rather broad peak at $2\theta \sim 9°$, characteristic of an amorphous film. The layered sample exhibits a very similar XRD pattern to the amorphous zinc tin oxide. However there are additional peaks at $2\theta$ values of 12 and 18, corresponding to crystalline $SnO_2$. Electron probe microanalysis of the layered sample shows a high zinc-to-tin ratio, 1.3:1. However, the XRD pattern shows no zinc oxide peaks, indicating that all of the zinc is in the form of zinc tin oxide.

Electrical characteristics also indicate that the layers have intermixed. The transistor characteristics of layered zinc oxide/tin oxide TTFTs are vastly improved compared to tin oxide transistors and zinc oxide transistors, and are very similar to zinc tin oxide TTFTs sputtered from a single target.

Figure 5.2 illustrates the drain current-drain voltage ($I_D$-$V_{DS}$) curves of a TTFT with a channel layer composed of alternating layers of zinc oxide and tin oxide, for a total of four layers with a bottom layer of tin oxide. An interesting feature is the presence of a negative $I_D$ slope in the saturation regime, which is attributed to slow traps, as discussed later in this section. The peak incremental mobility, $\mu_{INC}$ [18], for this TTFT is 12 $cm^2V^{-1}s^{-1}$. The threshold voltage for the TTFT shown in Fig. 5.2 is ~5 V, as estimated by linear extrapolation of an $I_D$-$V_{GS}$ curve (not shown) [28]. The turn-on voltage is ~-2 V for this TTFT, where turn-on voltage is defined as the gate voltage corresponding to the onset of the initial sharp increase in current in a $\log(I_D)$-$V_{GS}$ curve [18]. Typical TTFTs fabricated with a layered zinc oxide/tin oxide channel layer possess peak incremental mobilities of ~5-15 $cm^2V^{-1}s^{-1}$, thresh-

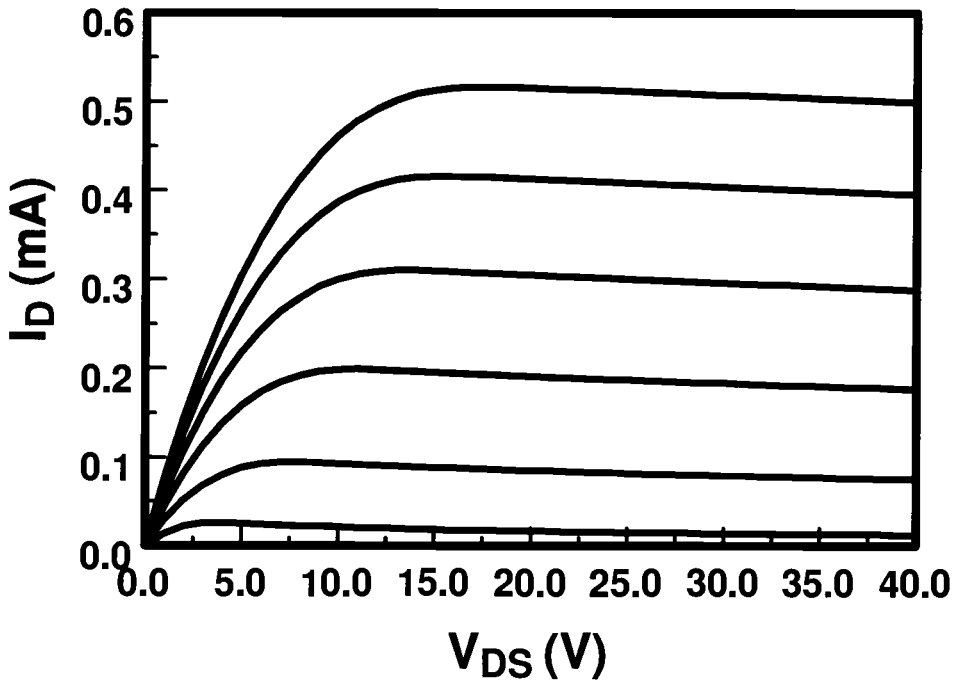


Figure 5.2: Drain current-drain voltage ($I_D$-$V_{DS}$) characteristics of a representative layered zinc oxide/tin oxide channel layer TTFT with a width-to-length ratio of 4.7. $V_{GS}$ is decreased from 30 V (top curve, showing maximum current) to 0 V in 5 V steps. The channel consists of alternating layers of zinc oxide and tin oxide, for a total of four layers with a bottom layer of tin oxide.

old voltages of ~5-10 V, turn-on voltages of ~-5 to +5 V, and drain current on-to-off ratios of $\sim 10^6$.

TTFTs having a zinc oxide or a tin oxide channel layer, and which are processed using the same parameters as employed for layered zinc tin oxide channels, have peak incremental mobilities of 2-5 $cm^2V^{-1}s^{-1}$ and 0.8-1 $cm^2V^{-1}s^{-1}$, respectively. The transistor performance of TTFTs with a layered zinc oxide/tin oxide channel layer is found to be superior to that of TTFTs with either zinc oxide or tin oxide channel layers, indicating that the transistor characteristics are no longer zinc oxide or tin oxide dominated.

Zinc tin oxide TTFTs fabricated using a $Zn_2SnO_4$ sputtering target and identical process parameters as used to deposit the layered zinc tin oxide channel layers have peak incremental mobilities of 5-15 $cm^2V^{-1}s^{-1}$, threshold voltages of ~5 V, turn-on voltages of ~-5 V, and drain current on-to-off ratios of $\sim 10^6$. Thus, layered zinc tin oxide TTFTs exhibit similar device characteristics to those of TTFTs in which the zinc tin oxide channel layer is sputtered from a single target. Other stoichiometries of zinc tin oxide show similar characteristics to $Zn_2SnO_4$ [5].

The improved transistor performance of the layered zinc oxide/tin oxide TTFTs over TTFTs with zinc oxide or tin oxide channel layers and the similar characteristics between the layered TTFTs and single channel layer zinc tin oxide TTFTs indicate that the post-deposition anneal induces interdiffusion and remixing of the binary oxide constituents, thus resulting in the formation of a predominantly ternary oxide. Several additional observations support this hypothesis that the layers remix. First, appreciable interdiffusion of $SnO_2$ and ZnO is witnessed at temperatures as low as

350°C [34]. In addition very similar TTFT device performance trends are observed when the layer sequence is reversed. These observations suggest that the individual zinc oxide and tin oxide layers have formed a single zinc tin oxide layer.

A study of other material systems also indicates the remixing of binary constituents because layering of zinc oxide or tin oxide with other binary oxides yields varying results. Zinc oxide/titanium oxide channel layer TTFTs and tin oxide/titanium oxide channel layer TTFTs show no transistor behavior; both of the channels containing titanium oxide result in highly resistive films that show no channel formation under any applied gate bias. The specific combination of zinc oxide layered with tin oxide results in good transistor characteristics. Other systems composed of HMC oxides also show good transistor characteristics. Successful TTFT channel layer combinations identified to date include zinc oxide/tin oxide, zinc oxide/indium oxide, gallium oxide/indium oxide, and indium oxide/tin oxide, all of which exhibit gate modulation when used as a channel material. These systems indicate that the layering methodology is a good option for exploring chemical systems for use as channel materials and indicate several HMC oxide systems are good candidates for use as channel materials in TTFTs.

Figure 5.3 shows the $I_D$-$V_{DS}$ characteristics of one of the successful combinations, a TTFT with a channel layer composed of four alternating layers of indium oxide and tin oxide, tin oxide constituting the bottom layer. The magnitude of $I_D$ is very large for this TTFT, whose width-to-length ratio is 4.7. Figure 5.4 shows the corresponding incremental mobility as a function of applied gate bias for $V_{DS}$ of 1 V. This TTFT exhibits a peak incremental mobility of 40 $cm^2V^{-1}s^{-1}$. The relatively

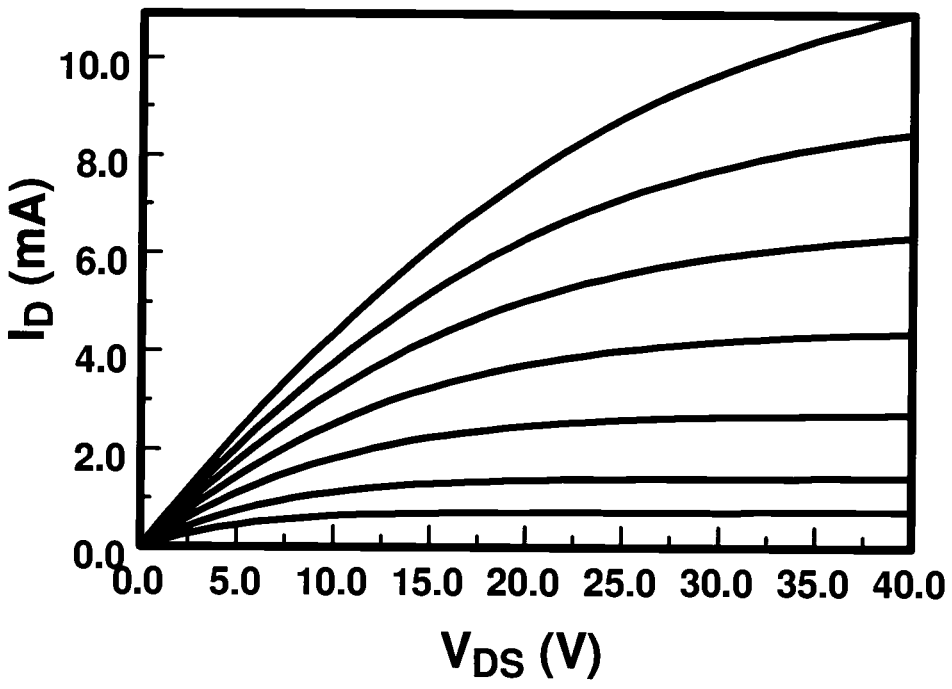


Figure 5.3: Drain current-drain voltage ($I_D$-$V_{DS}$) characteristic of a representative layered indium oxide/tin oxide channel layer TTFT with a width-to-length ratio of 4.7. $V_{GS}$ is decreased from 30 V (top curve, showing maximum current) to 0 V in 5 V steps. The channel consists of alternating layers of indium oxide and tin oxide, for a total of four layers with a bottom layer of tin oxide.

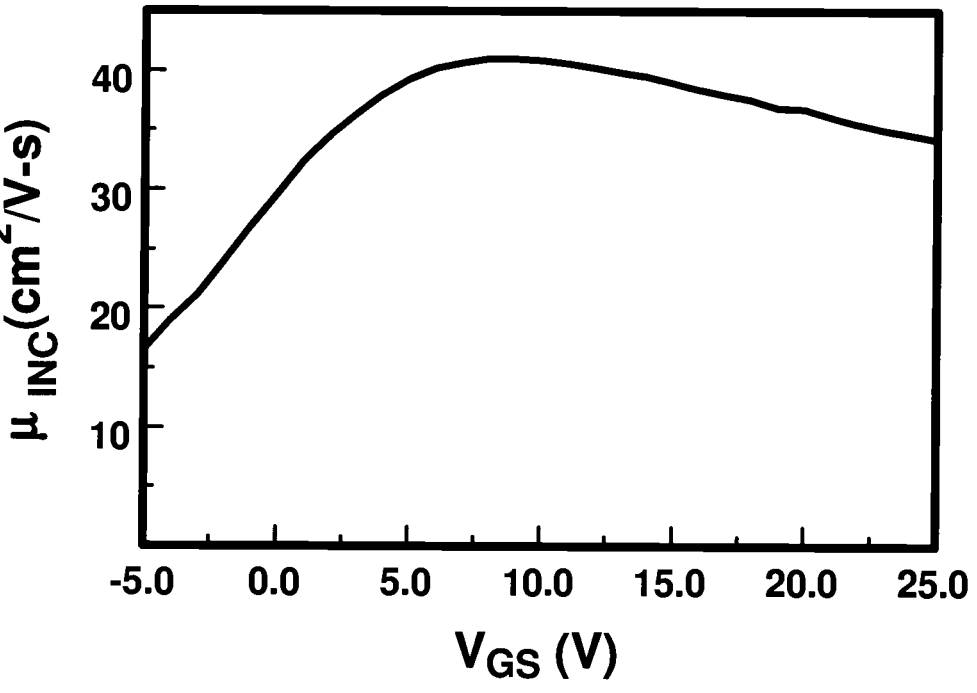


Figure 5.4: Incremental mobility ($\mu_{INC}$) as a function of gate voltage ( $V_{GS}$) for a representative layered indium oxide-tin oxide channel layer TTFT. This curve is derived from an assessment of the $I_D$-$V_{DS}$ data shown in Fig. 5.3.

high current drive capability and mobility of this TTFT suggest that indium tin oxide holds promise as a channel layer for TTFT applications. However, note that this is a depletion-mode TTFT with a threshold voltage of ~-8 V; enhancement-mode behavior is preferable. Additionally, this TTFT exhibits a very small drain current on-to-off ratio of $10^2$. Even though the performance of this layered channel TTFT is rather poor in terms of its depletion-mode behavior, and drain current on-to-off ratio, indium tin oxide merits further consideration as a TTFT channel material since a non-optimized process leads to high mobilities and large current drive.

As mentioned previously some TTFTs exhibit a slight negative slope in the saturation regime of a $I_D$-$V_{DS}$ plot. The ideal square-law model for a long-channel transistor predicts only a flat $I_D$ in saturation, due to pinch off, or a positive slope, due to bulk conductance. The negative slope is attributed to slow traps near the semiconductor-insulator interface, which is not taken into account when deriving the ideal model. Several experiments point to the existence of slow traps. By holding a constant $V_{GS}$ and sweeping $V_{DS}$ multiple times from 0 V to 40 V, $I_D$ decreases for each progressive scan as more traps are filled. Also, when holding both $V_{GS}$ and $V_{DS}$ constant, the current diminishes as time progresses. Filled slow traps reduce the number of free carriers, resulting in a diminishing current. By holding a constant $V_{DS}$ and sweeping $V_{GS}$ from 0 V to 40 V, $I_D$ does not decrease significantly for each subsequent sweep, indicating that the slow traps are emptied when a $V_{GS}$ of 0 V is applied. It should be noted that a negative saturation slope is also observed sometimes in single layer channel TTFTs, showing that this phenomenon is not peculiar to

layered structures. Moreover, not all zinc oxide/tin oxide layered TTFTs exhibit a negative saturation slope.

Returning to the sequential layer deposition/thermal annealing methodology, a similar approach has been employed previously to form Y-Ba-Cu-O thin films for superconductor applications [35]. Layers of three different materials, yttrium, copper and a barium/copper ceramic, interdiffused to form a single layer when annealed at temperatures of 800°C to 930°C. The high temperature required for interdiffusion is specific to the Y-Ba-Cu-O films under consideration. As indicated previously, interdiffusion of $SnO_2$ and ZnO is witnessed at temperatures as low as 350°C [34].

Other reports have shown that zinc oxide does not diffuse into an adjacent film during a post-deposition anneal if the film is highly crystalline[36, 37]. Specifically, a zinc oxide layer deposited at a 300°C substrate temperature, resulting in a highly crystalline zinc oxide film, does not diffuse into ITO at a post-deposition temperature of 350°C [37]. Remixing of binary oxide constituents appears to depend strongly on the crystallinity of the individual layers; enhanced crystallinity inhibits interdiffusion. Polycrystalline zinc oxide films exhibit significant atomic reordering at room temperature when imaged in a high-resolution transmission electron microscope with an irradiation density of 3 X $10^5$ $Am^{-2}$, the extent of which appreciably diminishes as the film approaches single crystal [36]. Interdiffusion can also diminish with increasing crystallinity because of the decrease of diffusion via grain boundaries and defect sites.

As-deposited zinc oxide thin films experience substantial atomic reordering during the annealing process, as evident from the fact that Scherrer crystallite size is $\sim$10

nm for the as-deposited film, increasing to ~60 nm after a 700°C post-deposition anneal.

One of the benefits of employing the sequential layer deposition/thermal annealing methodology is that the indium tin oxide system could be explored as a TTFT channel material even though it has not yet been possible to acquire an indium doped tin oxide target from a commercial vendor. Other advantages of the sequential layer deposition/thermal annealing methodology include the fact that no specialized equipment is required, film uniformity can be controlled via process parameters for the individual layers, and composition gradients across the sample can be engineered into the film by varying the substrate angle or substrate scan speed.

## 5.4 Conclusions

Sequential layer deposition/thermal annealing is demonstrated to be a viable exporatory methodology for TTFT channel layer applications. XRD assessment and electrical characterization indicates that a single layer is present after post-deposition annealing, resulting from the interdiffusion of multiple layers into a single channel layer.

Indium tin oxide is identified as a promising TTFT channel layer, yielding TTFTs with large current drive, high mobility, and a mobility which is relatively constant over a wide range of applied gate bias. Additionally, zinc oxide/tin oxide, zinc oxide/indium oxide, gallium oxide/indium oxide, and indium oxide/tin oxide are identified as promising TTFT channel layers. In additional to these chemical systems, a sequential sputtering exploratory method could also be useful for the study

of materials outside the realm of HMC oxides, such as systems containing sulfides or nitrides when the deposition and the anneal are carried out in a suitable environment.

# 6. ZINC TIN OXIDE THIN-FILM TRANSISTOR PASSIVATION

The purpose of this chapter is to present an effective method for the passivation of zinc tin oxide channel TFTs using thermally evaporated silicon dioxide as the passivation layer. This passivation scheme involves a post-deposition anneal of the channel material and a second post-passivation anneal of the entire thin film stack after deposition of the passivation layer. Such a passivation procedure produces devices with comparable transistor performance to that of unpassivated TFTs with air-exposed channel layers.

Devices used for this chapter are non-transparent bottom gate TFTs as described in Chapter 3.

## 6.1 Air-exposed thin-film transistors

Figure 6.1 shows the drain current-drain voltage ($I_D$-$V_{DS}$) characteristics of an unpassivated (i.e., the channel surface is uncovered, so that it is exposed to the atmosphere) zinc tin oxide TFT in which the channel layer is annealed at 600°C. This TFT exhibits qualitatively ideal saturation, showing little change in current with increasing $V_{DS}$ above pinch-off, where pinch-off corresponds to the minimum drain voltage, $V_{DSAT}$, at which the channel layer near the drain is fully depleted of carriers. Pinch-off occurs when

$$V_{DS} \equiv V_{DSAT} = V_{GS} - V_{ON} \tag{6.1}$$

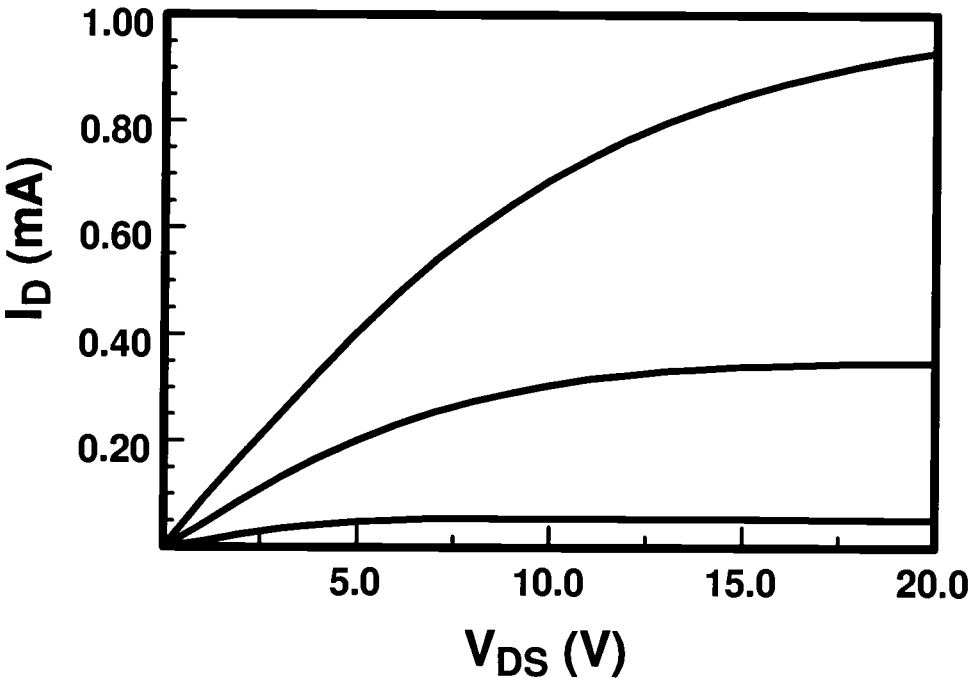


Figure 6.1: Drain current-drain voltage ($I_D$-$V_{DS}$) characteristics of a zinc tin oxide TFT in which the channel layer is annealed in air at 600°C. This device is unpassivated. $V_{GS}$ is decreased from 40 V (top curve, showing maximum current) to 0 V in 10 V steps.

where $V_{GS}$ is the gate voltage and $V_{ON}$ is the turn-on voltage, defined as the gate voltage corresponding to the onset of the initial sharp increase in current in a $\log(I_D)$-$V_{GS}$ curve [18]. The turn-on voltage is ~1 V for this TFT. Note that the top two $I_D$ curves shown in Fig. 6.1, $V_{GS}$ = 40 V and 30 V, do not fully saturate because $V_{DS}$ is not large enough to reach pinch-off.

It is also evident from Fig. 6.1 that there is large spacing between $I_D$ curves, indicating that this device has a large transconductance and, therefore, a high channel mobility [28]. The peak incremental mobility, $\mu_{INC}$, for this TFT is 20 $cm^2V^{-1}s^{-1}$, where $\mu_{INC}$ is numerically equivalent to the field-effect mobility; $\mu_{INC}$ corresponds to the mobility of carriers incrementally added to the channel by a corresponding incremental change in $V_{GS}$ [18].

## 6.2 Passivated thin-film transistors

Figure 6.2 displays the $I_D$-$V_{DS}$ characteristics of a zinc tin oxide TFT in which the channel layer is annealed in air at 600°C, after which an ~100 nm thick, thermally evaporated $SiO_2$ passivation layer is deposited. For this device, no additional anneal is performed after the $SiO_2$ deposition. As evident from Fig. 6.2, the passivation layer deposition causes this device to operate poorly as a transistor; in fact, this device is more precisely identified as a non-linear gate-controlled resistor, rather than a transistor, since it cannot be turned off with application of a practical gate voltage and the $I_D$ curves do not exhibit saturation. For such a device, $V_{ON}$ assessment requires an inappropriately large gate voltage. However, the fact that there is substantial

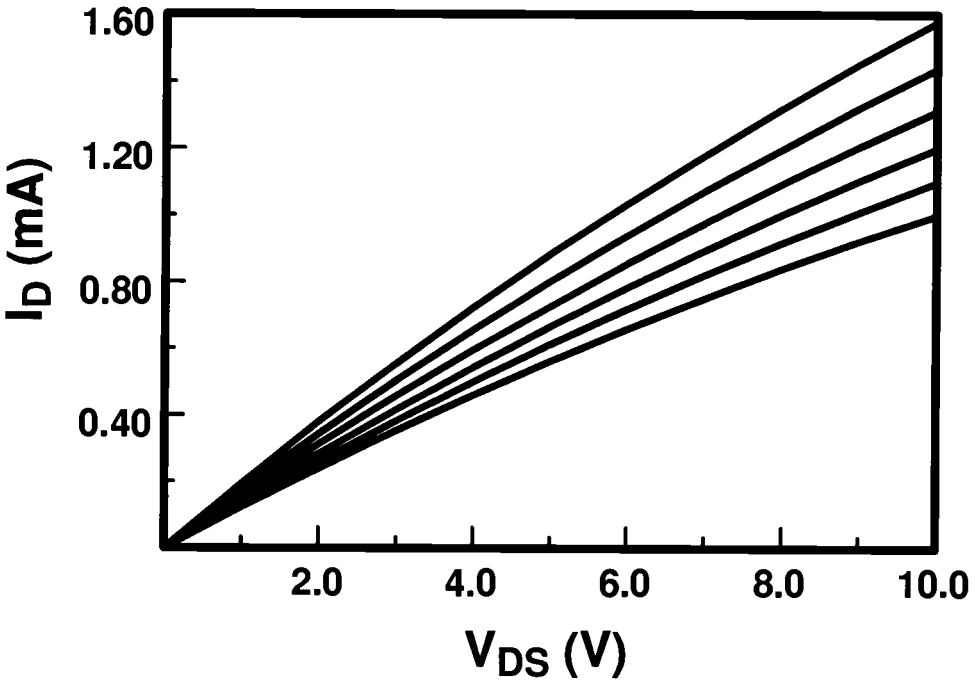


Figure 6.2: Drain current-drain voltage ($I_D$-$V_{DS}$) characteristics of a zinc tin oxide TFT which is capped with an ~100 nm thick, thermally evaporated $SiO_2$ layer. The channel layer is furnace annealed in air at 600°C prior to deposition of the $SiO_2$ passivation layer. No additional anneal is performed after the $SiO_2$ deposition. $V_{GS}$ is decreased from 10 V (top curve, showing maximum current) to 0 V in 2 V steps.

separation between $I_D$ curves indicates significant transconductance, corresponding to an incremental mobility of $\sim$20 $cm^2V^{-1}s^{-1}$.

The dramatic difference in $I_D$-$V_{DS}$ characteristics as shown in Figs. 6.1 and 6.2 can best be explained by assuming that an air-exposed zinc tin oxide surface behaves similarly to that of an air-exposed zinc oxide surface. This requires first reviewing what is known about zinc oxide surfaces [38, 39, 40].

Oxygen adsorption onto an n-type zinc oxide surface results in the introduction of an acceptor-like surface state. More specifically, physisorbed molecular oxygen and chemisorbed oxygen present on the zinc oxide surface constitute, respectively, the unoccupied/electronically neutral and the occupied/negative charge states of an acceptor-like surface state [38, 39, 40]. The process of oxygen chemisorption requires capture of conduction band electrons from the zinc oxide, thus resulting in depletion of a zinc oxide air-exposed surface.

Assuming that zinc oxide and zinc tin oxide air-exposed surfaces behave in a similar manner, the qualitatively ideal $I_D$-$V_{DS}$ characteristics witnessed in Fig. 6.1 are attributed to depletion of the zinc tin oxide by acceptor-like surface states associated with chemisorbed oxygen. Additionally, the poor electrical performance of the improperly passivated zinc tin oxide TFT, as exemplified by Fig. 6.2, is attributed to the elimination of oxygen-adsorption-related acceptor-like surface states. Essentially, coating of the zinc tin oxide with a deposited overlayer changes the surface/interface boundary conditions so that the top surface/interface is no longer depleted, but is now accumulated with conduction band electrons and, thus, creating an additional current pathway between the source and drain. The extent of this top surface elec-

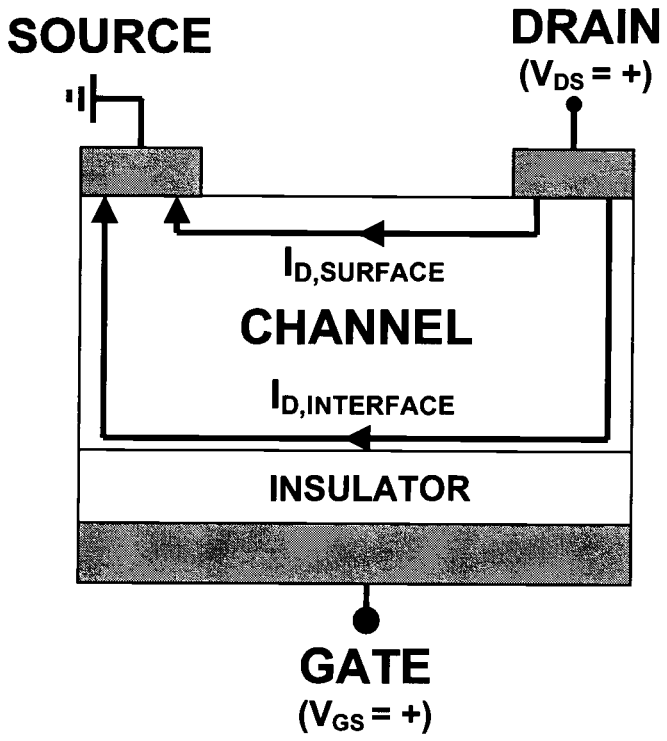


Figure 6.3: Schematic of a bottom-gate TFT and current pathways that can contribute to the overall current in a TFT. $I_{D,INTERFACE}$ is due to induced carriers from an applied gate bias at the channel layer-gate insulator interface. $I_{D,SURFACE}$ is due to mobile carriers at the channel layer-passivation layer interface.

tron accumulation depends on the sign and magnitude of the charge present in the deposited insulator and interface states. The extremely poor electrical performance of the Fig. 6.2 device suggests that a significant density of positive charge is present in the deposited insulator and/or its interface.

Figure 6.3 shows a schematic of a bottom-gate TFT illustrating two parallel current paths. The primary current pathway, $I_{D,INTERFACE}$, corresponds to interface conduction along the channel layer-gate insulator interface, and constitutes the current mechanism of an ideal transistor. The second pathway, $I_{D,SURFACE}$, is due to

surface conduction along the channel layer-passivation layer interface associated with mobile electrons in the surface accumulation layer. The strong similarity between the incremental mobility of the air-exposed TFT (i.e., the Fig. 6.1 device) and the improperly passivated device (i.e., the Fig. 6.2 device) indicates that $I_{D,INTERFACE}$ is, to a large extent, unaffected by the passivation process. The extreme shift in $V_{ON}$ also indicates that $I_{D,SURFACE}$ is dramatically increased. The similarity in incremental mobility of the Fig. 6.1 and the Fig. 6.2 device is not surprising in the context of the model presented in Fig. 6.3 since the $I_{D,INTERFACE}$ and $I_{D,SURFACE}$ mechanisms are essentially independent of one another, with each current contribution adding in parallel.

Figure 6.4 shows the $I_D$-$V_{DS}$ characteristics of a properly passivated zinc tin oxide TFT in which the channel layer is annealed in air at 600°C, after which an ~100 nm thick, thermally evaporated $SiO_2$ passivation layer is deposited. The entire device stack is then annealed in air at 300°C. This TFT exhibits qualitatively ideal saturation and turn-off characteristics and equivalent channel mobility when compared with an unpassivated TFT. The turn-on voltage is -1 V and peak incremental mobility is 26 $cm^2V^{-1}s^{-1}$ for this device. Therefore, this dual anneal passivation procedure produces TFTs with electrical characteristics similar to those of unpassivated air-exposed devices.

An alternative zinc tin oxide passivation scheme is also examined, but yielded transistors with diminished performance. After channel layer deposition, an ~100 nm thick, thermally evaporated $SiO_2$ passivation layer is deposited. The entire device stack is then annealed in air at 600°C. For this TFT, no anneal occurs between channel

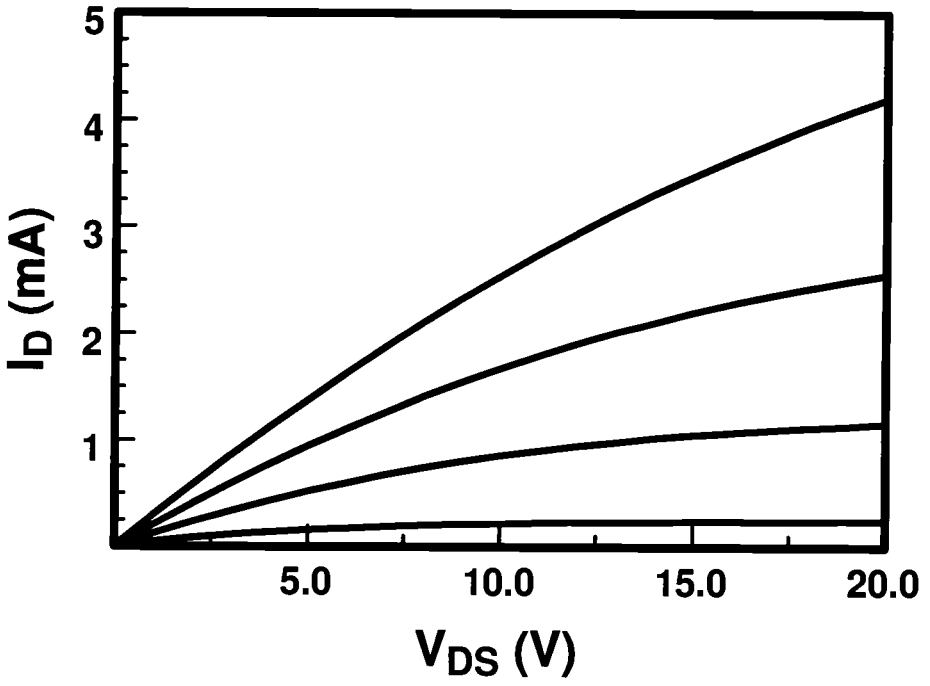


Figure 6.4: Drain current-drain voltage ($I_D$-$V_{DS}$) characteristics of a zinc tin oxide TFT which is capped with an ~100nm thick, thermally evaporated $SiO_2$ layer. The channel layer is furnace annealed in air at 600°C prior to deposition of the $SiO_2$ passivation layer. Additionally, the device stack is annealed in air at 300°C after $SiO_2$ deposition. $V_{GS}$ is decreased from 40 V (top curve, showing maximum current) to 0 V in 10 V steps.

Table 6.1: Zinc tin oxide TFT passivation summary involving thermally evaporated $SiO_2$ as the passivation layer. $T_1$ and $T_2$ are the channel layer annealing temperature and post-passivation annealing temperature respectively. Peak $\mu_{INC}$ and $V_{ON}$ refer, respectively, to the maximum incremental mobility and the turn-on voltage.

| Passivation | $T_1$ (°C) | $T_2$ (°C) | Peak $\mu_{INC}$ ($cm^2V^{-1}s^{-1}$) | $V_{on}$ (V) |
|---|---|---|---|---|
| None | 300 | None | 3 | 2 |
| None | 600 | None | 20 | 1 |
| $SiO_2$ | 600 | None | 20 | unmeasureable |
| $SiO_2$ | 600 | 200 | 18 | unmeasureable |
| $SiO_2$ | 600 | 300 | 26 | -1 |
| $SiO_2$ | 600 | 600 | 15 | -2 |
| $SiO_2$ | None | 300 | 4 | 2 |
| $SiO_2$ | None | 600 | 9 | -2 |

layer deposition and passivation-layer deposition. This TFT exhibits qualitatively ideal saturation, with a $V_{ON}$ of -2 V, however, the channel mobility is diminished compared to that of an unpassivated device with a peak incremental mobility of 9 $cm^2V^{-1}s^{-1}$.

Overall results obtained from this passivation study are summarized in Table I. The first two rows of Table I correspond to the TFT characteristics for unpassivated zinc tin oxide TFTs; a higher temperature anneal yields a higher mobility. The next four rows of Table I demonstrate that a second anneal is required for proper passivation, but that there is an optimal second annealing temperature which is lower than that of the first annealing temperature. The final two rows of Table I demonstrate that zinc tin oxide TFTs can indeed be passivated using only a single anneal subsequent to deposition of the passivation layer. However, this single anneal passivation procedure results in a lower channel mobility.

## 6.3 Passivation materials

Zinc tin oxide channel layer TFTs utilizing calcium fluoride, germanium oxide, strontium fluoride, and antimony oxide as passivation layers all show similar characteristics to TFTs fabricated using a thermally evaporated silicon dioxide passivation layer. Using a nickel oxide passivation layer, however, results in a reduced peak incremental mobility. Zinc sulfide and cesium oxide passivation layers yield TFTs with no measurable channel conduction at any applied gate bias.

## 6.4 Conclusion

This chapter presents a discussion of the passivation of zinc tin oxide thin-film transistors. A passivation scheme involving a post-deposition anneal of the channel material and a second post-passivation anneal of the entire thin film stack after deposition of the passivation layer produces devices with comparable transistor performance to that of unpassivated TFTs with air-exposed channel layers.

# 7. CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

## 7.1 Conclusions

This thesis focuses on three topics involving thin-film transistors (TFTs): modeling of TFTs, a methodology for the exploratory development of ternary oxides for use as channel layers in TFTs, and passivation of zinc tin oxide TFTs. Conclusions relevent to each of these three topics are briefly and sequentially summarized as follows.

First, a model for TFTs relating drain current to the integral of conductance in the linear region of operation is presented. Beginning with Shockley's gradual channel approximation for a general field-effect transistor, the conductance integral equation is derived. This equation expresses the drain current, $I_D$, as an integral of the channel conductance with respect to the gate voltage. The conductance integral equation is then used to derive the square-law model current-voltage equation, which constitutes the basic TFT model. Finally, an equation expressing $I_D$ for an n-channel, depletion-mode TFT is derived from the conductance integral equation.

Second, a novel deposition methodology is employed for exploratory development of a class of high-performance transparent thin-film transistor (TTFT) channel materials involving oxides composed of heavy-metal cations with $(n\text{-}1)d^{10}ns^0$ ($n \geq 4$) electronic configurations. The method involves sequential RF sputter deposition of thin, single cation oxide layers and subsequent post-deposition annealing in order to obtain a multi-component oxide thin film. The viability of this rapid materials de-

velopment methodology is demonstrated through the realization of high-performance TTFTs with channel layers composed of zinc oxide/tin oxide, and tin oxide/indium oxide.

Finally, an effective method for the passivation of zinc tin oxide channel TFTs using thermally evaporated silicon dioxide as the passivation layer is presented. This passivation scheme involves a post-deposition anneal of the channel material and a second post-passivation anneal of the entire thin film stack after deposition of the passivation layer. Such a passivation procedure produces devices with comparable transistor performance to that of unpassivated TFTs with air-exposed channel layers.

## 7.2 Recommendations for future work

The completion of this thesis has left many questions unanswered. The purpose of this section is to summarize potential directions for further research based upon that presented in this thesis.

Many binary and ternary heavy metal cation oxides are still unexplored for use as channel materials. In particular, various combinations of copper, gallium, germanium, indium, tin, antimony, and bismuth have not been explored. Indium tin oxide and gallium indium oxide are promising candidates for additional analysis.

In addition to oxides, nitrides of HMC cations should also be studied as possible channel materials. Nitrogen is less electronegative and a larger atom than oxygen, which may lead to better orbital overlap and thus higher mobility.

Passivation of zinc tin oxide-based TFTs via dielectric materials other than thermally evaporated silicon dioxide should also be explored. Two categories of

passivation materials should be considered: low-permittivity insulators and high-permittivity insulators. Low permittivity passivation layers electrically isolate individual TFTs from surrounding devices, such as other TFTs and liquid crystal displays. One low permittivity insulator that should be considered for passivation layers is silicon dioxide via chemical vapor deposition. High permittivity insulators, such as hafnium oxide, zirconium oxide, and silicon nitride may find use as gate insulators in TFTs. Successful passivation using a high permittivity insulator would allow fabrication of a top-gate or a double-gate TFT.

# BIBLIOGRAPHY


1. H. Hosono, N. Kikuchi, N. Ueda, and H. Kawazoe, "Working hypothesis to explore novel wide band gap electrically conducting amorphous oxides and examples," *J. Non-Crys. Sol.*, vol. 165, pp. 198–200, 1996.

2. H. Hosono, M. Yasukawa, and H. Kawazoe, "Novel oxide amorphous semiconductors: transparent conducting amorphous oxides," *J. Non-Crys. Sol.*, vol. 203, p. 334, 1996.

3. S. Narushima, M. Orita, M. Hirano, and H. Hosono, "Electronic structure and transport properties in the transparent amorphous oxide semiconductor-cadmium oxide-germanium oxide," *Phys. Rev. B*, vol. 66, p. 035203, 2002.

4. K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, p. 488, 2004.

5. H. Q. Chiang, R. L. Hoffman, J. Jeong, J. F. Wager, and D. A. Keszler, "High mobility transparent thin-film transistors with amorphous zinc tin oxide channel layer," *Appl. Phys. Lett.*, vol. 86, p. 13503, 2005.

6. N. L. Dehuff, E. S. Kettenring, D. Hong, H. Q. Chiang, J. F. Wager, R. L. Hoffman, C. H. Park, and D. A. Keszler, "Transparent thin-film transistors with zinc indium oxide channel layer," *J. Appl. Phys.*, vol. 97, no. 6, p. 4505, 2005.

7. K. Nomura, H. Ohta, K. Ueda, T. Kamiya, M. Hirano, and H. Hosono, "Thin-film transistor fabricated in single-crystalline transparent oxide semiconductor," *Science*, vol. 300, p. 1269, 2003.

8. S. M. Sze, *Physics of semiconductor devices.* New York: John Wiley & Sons, second ed., 1981.

9. C. R. Kagan and P. Andry, *Thin-film transistors.* New York: Marcel Dekker, Inc., 2003.

10. P. K. Weimer, "The TFT-a new thin film transistor," *Proc. IRE*, vol. 50, p. 1462, 1962.

11. P. Brody, "A 6x6 inch 20-lpi electroluminescent display panel," *IEEE Trans. El, Dev.*, vol. 22, p. 739, 1975.

12. L. Pichon, K. Mourgues, F. Raoult, T. Mohammed-Brahim, K. Kis-Sion, D. Briand, and O. Bonnaud, "Thin film transistors fabricated by in situ doped unhydrogenated polysilicon films obtained by solid phase crystallization," *Semi. Sci. and Tech.*, vol. 16, no. 11, pp. 918–924, 2001.

13. H. Gleskova, P. I. Hsu, Z. Xi, J. C. Sturm, Z. Suo, and S. Wagner, "Field-effect mobility of amorphous silicon thin-film transistors under strain," *J. Non-Crys. Sol.*, p. 203, 1996.

14. C. D. Dimitrakopoulos and D. J. Mascaro, "Organic thin-film transistors: A review of recent advances," *IBM J. of Res. and Dev*, vol. 45, no. 1, p. 3, 2001.

15. H. E. Katz, A. J. Lovinger, J. Johnson, C. Kloc, T. Siegrist, W. Li, Y.-Y. Lin, and A. Dodalapur, "A soluble and air-stable organic semiconductor with high electron mobility," *Nature*, vol. 404, p. 478, 2000.

16. D. B. Mitzi, K. Chondroudis, and C. R. Kagan, "Organic thin-film transistors: A review of recent advances," *IBM J. of Res. and Dev*, vol. 45, no. 1, p. 29, 2001.

17. R. L. Hoffman, B. J. Norris, and J. F. Wager, "Zinc oxide based transparent thin film transistor," *Appl. Phys. Lett.*, vol. 82, no. 5, p. 733, 2003.

18. R. L. Hoffman, "Zinc oxide-channel thin-film transistors: Channel mobility," *J. Appl. Phys.*, vol. 95, p. 5813, 2004.

19. J. Nishii, F. M. Hossain, S. Takagi, T. Aita, K. Saikusa, Y. Ohmaki, I. O. S. Kishimoto, A. Ohtomo, T. Fukumura, F. Matsukura, Y. Ohno, H. Koinuma, H. Ohno, and M. Kawasaki, "High mobility thin film transistors with transparent ZnO channels," *Jpn. J. Appl. Phys*, vol. 42, p. 347, 2003.

20. S. Masuda, K. Kitamura, Y. Okumura, S. Miyatake, H. Tabata, and T. Kawai, "Transparent thin film transistors using ZnO as an active channel layer and their electrical properties," *J. Appl. Phys.*, vol. 93, p. 1624, 2003.

21. B. J. Norris, J. Anderson, J. F. Wager, and D. A. Keszler2, "Spin-coated zinc oxide transparent transistors," *J. Phys. D: Appl. Phys.*, vol. 36, no. 20, p. L105, 2003.

22. P. F. Carcia, R. S. McLean, M. H. Reilly, and G. N. Jr, "Transparent ZnO thin film transistor fabricated by rf magnetron sputtering," *Appl. Phys. Lett.*, vol. 82, p. 1117, 2003.

23. E. M. C. Fortunato, P. M. C. Barquinha, A. C. M. B. G. Pimentel, A. M. F. Goncalvez, A. J. S. Marques, R. F. P. Martins, and L. M. N. Pereira, "Wide-bandgap high-mobility ZnO thin-film transistors produced at room temperature," *Appl. Phys. Lett.*, vol. 85, no. 13, p. 2541, 2004.

24. R. E. Presley, C. L. Munsee, C. H. Park, D. Hong, J. F. Wager, and D. A. Keszler, "Tin oxide transparent thin-film transistors," *J. Phys. D: Appl. Phys.*, vol. 37, p. 2810, 2004.

25. D. L. Smith, *Thin-Film Deposition Principle & Practice.* New York: McGraw-Hill, 1995.

26. H. Q. Chiang, "Development of zinc tin oxide-based transparent thin-film transistors.," M.S. thesis, Oregon State University, 2003.

27. J. P. Bender, "Manufacture and characterization of novel actfel materials and devices," Ph.D. thesis, Oregon State University, 2003.

28. D. K. Schroder, *Semiconductor Material and Device Characterization.* New York: John Wiley & Sons, Inc., 2 ed., 1998.

29. A. C. Tickle, *Thin-film transistors.* New York: John Wily and Sons, 1969.

30. L. B. Valdes, "Resistivity measurements on germanium for transistors," *Proceedings of the IRE*, p. 420, 1954.

31. W. Shockley, "A unipolar "field-effect" transistor," *Proc. IRE*, vol. 40, p. 1365, 1952.

32. M. L. Boas, *Mathematical Methods in the Physical Sciences.* New York: John Wiley & Sons, second ed., 1983.

33. A. Goetzberger and E. H. Nicollian, "Transient voltage breakdown due to avalanche in mis capacitors," *Appl. Phys. Lett.*, vol. 9, no. 12, p. 444, 1966.

34. W. Wang, S. Wang, and X. Pan, "Deposition and characterization of zinc oxide and tin oxide ultrafine particle bilayer thin films," *Thin Solid Films*, vol. 345, p. 212, 1999.

35. V. N. Alfeev, V. A. Rukavishnikov, S. M. Gusev, A. O.Sokolov, , and E. A. Klimanov, "Synthesis of Y-Ba-Cu-O thin films by magnetron sputtering of three targets," *Superconductivity*, vol. 4, p. 470, 1991.

36. T. Kizuka, "Atomic processes of grain-boundary migration and phase transformation in zinc oxide nanocrystallites," *Phil. Mag. Lett*, vol. 79, no. 7, p. 417, 1999.

37. X. W. Sun, L. D. Wang, and H. S. Kwok, "Improved ITO thin films with a thin ZnO buffer layer by sputtering," *J. Appl. Phys.*, vol. 360, p. 75, 2000.

38. P. Mark, "Chemisorption and trapping on insulator surfaces," *Trans. N. Y. Acad. Sci.*, vol. 27, p. 946, 1965.

39. A. Many, "Relation between physical and chemical processes on semiconductor surfaces," *CRC Crit. Rev. Solid State Mater. Sci.*, vol. 4, p. 515, 1974.

40. D. Eger, Y. Goldstein, and A. Many, "Oxygen chemisorption and photodesorption processes on ZnO surfaces," *R. C. A. Rev.*, vol. 36, p. 508, 1975.