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This fault detection scheme is based on sampling the instantaneous phase voltages and checking their sum and magnitude against a specified voltage. Faults on the system cause unbalances and distortion of the phase voltages and currents. The currents and voltages change in magnitude and/or phase position with respect to the prefault condition. The measurement of this deviation from the normal condition indicates a fault. This scheme detected the fault within one-half cycle (8 milliseconds) in the laboratory. It is shown that this scheme is simpler and faster to implement than conventional detection schemes.
Hybrid, High Speed Fault Detection Based On Instantaneous Line Voltages

by

Hiranand Balchand Ramchandani

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Approved:

Redacted for Privacy

Professor of Electrical and Computer Engineering
in charge of major

Redacted for Privacy

Head of Department of Electrical and Computer Engineering

Redacted for Privacy

Dean of Graduate School

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Typed by Eula Weathers for Hiranand Balchand Ramchandani
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# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>Chapter</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>1</td>
</tr>
<tr>
<td>II</td>
<td>5</td>
</tr>
<tr>
<td>III</td>
<td>18</td>
</tr>
<tr>
<td>IV</td>
<td>24</td>
</tr>
<tr>
<td>V</td>
<td>33</td>
</tr>
<tr>
<td>VI</td>
<td>35</td>
</tr>
<tr>
<td>VII</td>
<td>36</td>
</tr>
</tbody>
</table>

### BIBLIOGRAPHY

### APPENDICES
<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Phase voltages under normal balanced condition</td>
<td>6</td>
</tr>
<tr>
<td>2</td>
<td>Voltage phasor diagram for normal condition</td>
<td>7</td>
</tr>
<tr>
<td>3</td>
<td>Power system</td>
<td>7</td>
</tr>
<tr>
<td>4</td>
<td>Phase voltages for a line to ground fault with a fault resistance</td>
<td>8</td>
</tr>
<tr>
<td>5</td>
<td>Phase voltages for two line to ground fault with a fault resistance</td>
<td>9</td>
</tr>
<tr>
<td>6</td>
<td>Phase voltages for line to line fault with a fault resistance</td>
<td>10</td>
</tr>
<tr>
<td>7</td>
<td>Phase voltages for three line to ground fault with a fault resistance</td>
<td>11</td>
</tr>
<tr>
<td>8</td>
<td>Current and voltage phasor diagrams for a line to ground fault and two line to ground fault</td>
<td>12</td>
</tr>
<tr>
<td>9</td>
<td>Current and voltage phasor diagrams for a line to line fault and three line to ground fault</td>
<td>13</td>
</tr>
<tr>
<td>10</td>
<td>Test installation</td>
<td>19</td>
</tr>
<tr>
<td>11</td>
<td>Block diagram for the sampling clock</td>
<td>21</td>
</tr>
<tr>
<td>12</td>
<td>Sampling clock circuit</td>
<td>22</td>
</tr>
<tr>
<td>13</td>
<td>Block diagram for the fault detection</td>
<td>26</td>
</tr>
<tr>
<td>14</td>
<td>Block diagram to find line to ground faults</td>
<td>31</td>
</tr>
<tr>
<td>15</td>
<td>Block diagram to find line to line fault</td>
<td>32</td>
</tr>
<tr>
<td>16</td>
<td>Laboratory test set-up showing the faults on the system</td>
<td>34</td>
</tr>
<tr>
<td>17</td>
<td>Power system</td>
<td>40</td>
</tr>
<tr>
<td>Figure</td>
<td>Description</td>
<td>Page</td>
</tr>
<tr>
<td>--------</td>
<td>------------------------------------------------------------------------------</td>
<td>------</td>
</tr>
<tr>
<td>18</td>
<td>One-line diagram of the positive sequence network</td>
<td>41</td>
</tr>
<tr>
<td>19</td>
<td>Sequence network for SLG fault</td>
<td>42</td>
</tr>
<tr>
<td>20</td>
<td>A 2LG fault network</td>
<td>45</td>
</tr>
<tr>
<td>21</td>
<td>Sequence network connection for a LL fault</td>
<td>48</td>
</tr>
<tr>
<td>22</td>
<td>TI 960A computer block diagram</td>
<td>55</td>
</tr>
</tbody>
</table>
HYBRID, HIGH SPEED FAULT DETECTION BASED ON INSTANTANEOUS LINE VOLTAGES

I. INTRODUCTION

Function of a Relay

A power system is designed to generate, transmit, and distribute electric power of sufficient quantity to meet present and estimated future demands of the users in some particular area. The main parts of the system are generators, transformers, transmission lines, switch gear and distribution circuits. Each part is an essential component and failure of any part destroys the capacity and function of the system. To insure reliable service and a reasonable return on the investment, the whole system should be kept in service to deliver energy without interruption.

This may be accomplished in two ways. One way is to maintain each component to prevent failure and to provide alternate links. The maintenance and the cost of alternate links allow this course to proceed to a limit. A second way is to minimize and control the effects of the failures that do occur. The main functions of protection are to minimize damage to apparatus, maintain safety and to minimize interference of the fault with the normal operation of the system.

Fault is herein defined as the failure of high voltage insulation, which will cause the system to become short-circuited at a point.
unfaulted parts of the system.

The above function of protection is performed by the device known as a protective relay. The relays are the sensing devices which detect and analyze the fault and operate the circuit breaker to isolate the faulted circuit. The protective relay recognizes and analyzes the fault by detecting the change in magnitude of electrical quantities. The basic quantities, which may change when a fault occurs are current, voltage, phase angle (direction), and frequency.

**Development**

The art of protective relaying has been established for many years. The relay devices and their application have undergone continued progressive development keeping close pace with the growth and requirement of electric power systems.

The protection characteristics for early power systems were simple and direct because the power systems were simple, consisting only of power stations supplying power over short distance to local loads.

The system growth and interconnection have given rise to an increased need for faster and better protection. As a result, a great deal of work has been performed in the study of relay protection under service conditions, the reconstruction and adoption of old forms of protection and the introduction of new types of relays and
protection schemes.

Although the electro-mechanical devices are highly reliable, much work has been conducted in order to develop solid state and digital relays. Thus relay systems have improved in both reliability and accuracy as well as showing some increase in operating speed.

The development of electro-mechanical and solid state relays has been described in detail in literature. In this thesis only the development of the digital relays is discussed briefly.

**Digital Relaying**

The use of a minicomputer for protection was first considered in late 1960's. Since then more attention has been given to this subject. Mann and Morrison (10) used a minicomputer for the protection of a single three phase line. They detected, classified, and calculated the impedance of the faulted line in less than 10 milliseconds (one-half cycle on 50 Hz base) in the laboratory after the occurrence of the fault. Rockefeller and Udren (15, 16) used a modified method of Mann and Morrison (10) to protect the line. They were able to detect the fault and send a trip signal to the circuit breaker, under simulated field conditions, from 1/4 to 3 cycle (60 Hz base) after the occurrence of the fault. In all cases, a single dedicated minicomputer was used to perform the protection for a single three-phase line terminal.
Most of the above schemes proposed to date monopolize computer time by continually scanning current and voltage waves in order to detect a fault condition. The purpose of this thesis is to develop a detection method which will use less computer time and memory without sacrificing the efficiency of fault detection. The saving in computer time and memory will allow enough time for the computer to perform other substation tasks or monitor additional transmission lines.
II. THEORY

This detection scheme works on the principle that the sum of the three phase-voltages of a three-phase system in the steady state is nearly equal to zero as shown by Figures 1 and 2.

Faults on the system cause unbalances and distortion of the phase voltages and currents. The currents and voltages change in magnitude and/or phase position with respect to their prefault condition. The magnitude of the currents and voltages depends on the different sources that generate them and their reactances up to the fault location. Sources of the short-circuit currents are utility systems, generators, synchronous motors, induction motors and transformers.

The current magnitude is highest during the first half cycle and decreases in value after a few cycles as the equivalent reactances of the machines change from subtransient to transient state. The magnitude of the short-circuit current is further increased during the first few cycles by the so-called dc component.

The effects of a fault on the phase voltages is best illustrated by simulating faults on a simple power system as shown in Figure 3.

The following faults were simulated on the system shown in Figure 3:
1) Single line to ground

2) Double line to ground

3) Line to line

4) Three phase to ground

The method of symmetrical components was used to calculate the short circuit voltages and currents, assuming a value of fault resistance. The complete analytical solution is given in Appendix I. In above example the subtransient reactance of the generator was used to show the change in the voltage magnitudes during first few cycles of the fault condition. Figures 4 through 7 show the instantaneous phase voltages for first few cycles after occurrence of a fault. Figures 8 and 9 show the phasor diagrams associated with the post fault wave forms.
PHASE VOLTAGES UNDER NORMAL BALANCED CONDITION

FIGURE 1
VOLTAGE PHASOR DIAGRAM
FOR NORMAL CONDITION

FIGURE 2

POWER SYSTEM

FIGURE 3
Phase voltages for line to ground fault with a fault resistance

Figure 4
PHASE VOLTAGES FOR TWO LINE TO GROUND FAULT WITH A FAULT RESISTANCE

FIGURE 5
PHASE VOLTAGES FOR LINE TO LINE FAULT WITH A FAULT RESISTANCE

FIGURE 6
PHASE VOLTAGES FOR THREE LINE TO GROUND FAULT WITH A FAULT RESISTANCE

FIGURE 7
TWO LINE TO GROUND FAULT

LINE TO GROUND FAULT

CURRENTS AND VOLTAGES PHASOR DIAGRAMS

FIGURE B
THREE LINE TO GROUND FAULT

LINE TO LINE FAULT

CURRENTS AND VOLTAGES PHASOR DIAGRAMS

FIGURE 9
The exact conditions that exist when a fault occurs vary widely in different systems. The distortion also depends on the severity of the fault and the system reactance to the fault.

From Figure 1 (a balanced prefault condition), we observe that at each zero crossing of the three voltage waveforms, the sum of the other two voltages is zero and at each peak the other two voltages are equal. This is analytically shown below:

Let

\[ V_a = V_m \cos (\omega t) \]
\[ V_b = V_m \cos (\omega t - 120^\circ) \]
\[ V_c = V_m \cos (\omega t + 120^\circ) \]

Case 1

\[ V_m = 1.0 \text{ unit and voltage } V_b \text{ waveform is crossing zero at } \omega t = 30^\circ \text{ (Figure 1).} \]

Therefore

\[ V_a = \cos (30^\circ) = 0.866 \text{ pu} \]
\[ V_b = \cos (-90^\circ) = 0 \]
\[ V_c = \cos (150^\circ) = -0.866 \text{ pu} \]

This proves that at the zero crossing of the voltage waveform, the sum of the other two voltages is zero \((V_a + V_c = 0)\).
Case 2

Voltage $V_b$ waveform is at the peak at $\omega t = 120^\circ$. Therefore

$$V_a = \cos (120^\circ) = -0.5 \text{ pu}$$
$$V_b = \cos (0^\circ) = 1.0 \text{ pu}$$
$$V_c = \cos (240^\circ) = -0.5 \text{ pu}$$

This proves that at the peak of the voltage waveform, the other two voltages are equal ($V_a = V_c$).

From Figures 4 through 7 we observe that these conditions do not exist when the system is under fault and the samples are taken at the zero crossing and peak times of the prefault voltage waveforms.

From Figures 4 through 7, we also observe that the magnitude of the phase voltages is different from the prefault value. This is analytically shown below in the case of a line to ground fault.

Instantaneous phase voltages in the case of a line to ground fault are: (data taken from Appendix I)

$$V_a = 0.466 \cos (\omega t - 42.8^\circ)$$
$$V_b = 0.994 \cos (\omega t - 118.3^\circ)$$
$$V_c = 0.994 \cos (\omega t + 118.3^\circ)$$

Case 1

Prefault zero crossing of the voltage $V_b$ occurs when $\omega t = 30^\circ$.

Therefore, the phase voltages at that instant are:
\[ V_a = 0.466 \cos (30 - 42.8°) = 0.456 \text{ pu} \]
\[ V_b = 0.994 \cos (30 - 118.3°) = 0.0289 \text{ pu} \]
\[ V_c = 0.994 \cos (30 + 118.3°) = -0.846 \text{ pu} \]

This proves that the sum of the other two voltages is not equal to zero \((V_a + V_c = -0.39)\). We also observe that the voltage \(V_a\) is not equal to its prefault value.

Case 2

Prefault peak of the voltage \(V_b\) occurs when \(\omega t = 120°\).

Therefore, the phase voltages at instant are:
\[ V_a = 0.466 \cos (120 - 42.8°) = 0.103 \text{ pu} \]
\[ V_b = 0.994 \cos (120 - 118.3°) = 0.993 \text{ pu} \]
\[ V_c = 0.994 \cos (120 + 118.3°) = -0.521 \text{ pu} \]

This proves that the two voltages are not equal \((V_a \neq V_c)\) and the magnitude of \(V_a\) is not equal to its prefault value. For other types of faults, the magnitudes of the phase voltages at the prefault zero crossing and peak of \(V_b\) are given in Appendix I.

In the case of a three phase-to-ground fault, there is a possibility that the sum of the voltages is equal to zero, but that there will always be a change in voltage magnitude.

This scheme takes advantage of the above abnormalities of the system voltages during the faults and detects the change in the system parameters from normal to abnormal conditions.
change is more than a specified tolerance limit, a fault is indicated.

The detection tolerance limit will depend upon the sensitivity of the detection scheme and the normal system operating unbalances.
III. CONSTRUCTION

Figure 10 shows the laboratory test installation for the fault detection scheme which was used for verification of the design theory. There are two major parts of the scheme:

1) Minicomputer
2) Control Logic

The main characteristics of each part are described below.

Minicomputer

T1960A minicomputer was used to sample the transmission lines and to carry out the necessary calculation and control functions. This particular minicomputer was not specially designed for the fault detection scheme but was employed because of its availability. T1960A computer is manufactured by the Texas Instruments, Inc. Figure 22 shows the computer block diagrams of the basic internal functional relationships of the computer. The main characteristics of the computer are given in Appendix II.

Control Logic

The control logic consists of three independent sampling clocks. Each sampling clock is synchronized to system frequency prior to the fault. The main parts of the sampling clock are shown by block
TEST INSTALLATION
FIGURE 10
diagrams in Figure 11. The function of each part of the block
diagram is explained below. The complete details of the circuit are
given in Figure 12.

a. **Zero-crossing detector** - the R. C. A. zero-voltage crossing
detector (CA3059) was used and found to give accurately
synchronized output pulses each time the voltage crosses
zero.

b. **Sampling clock** - The sampling clock was built by using
two schmitt-trigger monostable multivibrators (SN74121).
The clock frequency was set at 240 Hz. This gives a
pulse at each zero crossing and each peak of the voltage
waveform.

The sampling clock is always synchronized with line frequency
except when a fault occurs. During the fault, or any other time, if
the line frequency changes more than 5% from its last cycle, the
clock locks itself to a frequency of 240 Hz.

c. **Reset circuit** - The sampling clock is set at 240 Hz, but
the line frequency can vary from 58 to 62 Hz (± 3.5% from
normal frequency of 60 Hz). To minimize error due to
this change in frequency, it was found that resetting the
sampling clock every two cycles was sufficient.

d. **Frequency change detector** - This portion of the circuit
detects the change in system frequency from one cycle to
FROM LINE
ZERO CROSSING DETECTOR

PHASE SHIFT OR FREQUENCY CHANGE DETECTOR

CIRCUIT TO SYNCHRONISE CLOCK WITH LINE FREQUENCY PRIOR TO FAULT

CIRCUIT TO RESET CLOCK EVERY TWO CYCLES

SAMPLING CLOCK 740 HZ

TO COMPUTER

BLOCK DIAGRAM FOR THE SAMPLING CLOCK

FIGURE 11
the next. If the time between pulses from the zero-crossing detector does not vary more than 5\%, the system frequency is assumed to be within limits. Otherwise, it sends the signal to sampling clock and locks the sampling clock at its original line frequency.
IV. COMPUTER OPERATION

The fault detection program, written in assembly language (SAL960A) for the T1960A computer, is responsible for performing the major logic function of fault detection. It was compiled on a CDC 3300 computer. SAL960A reads a source file of instruction written in the assembly language and outputs an object file of instruction on paper tape for loading. It also outputs a list which includes the source statements and corresponding object words generated by SAL960A, along with error indicators, the location of each instruction and source statement number. The listing of the program is given in Appendix III.

The program has two main parts:

1) Detection program

2) Fault type analysis

Each part is described below.

Detection Program

The detection consists of two parts:

a) initialization and b) fault detection

Initialization

The initialization part of the program initializes all registers
and counters. It clears all flags and sets the limit for the parameters. It finds the phase-sequence of the transmission line voltages and sets the sampling order for the detection portion. The sampling order depends on the phase sequence of the sampled phase voltages.

When the phase relation is abc, the computer will sample lines b, and c when clock 1 issues a pulse and waits for the pulse from number 2 clock. When it receives an interrupt from clock 2, it samples lines a and c and waits for an interrupt from clock 3. When clock 3 issues its pulse, it samples lines a and b. This cycle is repeated. If the sequence is acb, then the computer will sample line voltages when it receives interrupts from the clocks in a sequence 1, 3, 2.

**Fault Detection**

The fault detection is the only part of the program which is used to monitor the system. The logic of the program is based upon the theory explained in Chapter II.

Figure 13 shows the complete block diagram of the logical steps taken by the computer to detect a fault. Voltage samples are taken only at each zero crossing and peak of the voltage waveforms. The program is initiated from a phase A, which is arbitrarily chosen. Following the interrupt from phase A clock, the computer samples the other phase voltages, $V_b$ and $V_c$. 
INITIALIZE ALL REGISTERS AND COUNTERS

DETERMINE THE SEQUENCE OF THE PHASE VOLTAGES AND SET THE SAMPLING SEQUENCE

CHECK IF PHASE A CLOCK IS HIGH
SAMPLE LINE VOLTAGE VB AND VC

CHECK IF VOLTAGE VA IS CROSSING ZERO

SUBTRACT VB FROM VC
SET FLAG ZP1 HIGH

ADD VOLTAGES VB AND VC

STORE THE RESULT R1
CHECK IF FLAG ZP1 IS HIGH

COMPARE THE MAGNITUDE OF PHASE VOLTAGE VB AGAINST VALUE VP

COMPARE THE MAGNITUDE OF PHASE VOLTAGE VB AGAINST VALUE VZ

BLOCK DIAGRAM FOR THE FAULT DETECTION

FIGURE 13
IF MAGNITUDE WITHIN LIMITS

CHECK IF旗 F6 IS HIGH

SET FLAG F6 LOW
DECREASE PHASE B FAULT COUNTER (NB) 1

SET FLAG F6 HIGH
INCREASE PHASE B FAULT COUNTER (NB) 1

CHECK IF NB IS GREATER THAN THREE

FAULT ON LINE
JUMP TO SUBROUTINE

CHECK IF FLAG ZP1 IS HIGH

SET FLAG ZP1 LOW
COMPARE THE MAGNITUDE OF PHASE VOLTAGE VC AGAINST VP

COMPARE THE MAGNITUDE OF PHASE VOLTAGE VC AGAINST VZ

IS MAGNITUDE WITHIN LIMITS

CHECK IF FLAG F7 IS HIGH

SET FLAG F7 LOW
DECREASE PHASE C FAULT COUNTER NC BY 1

SET FLAG F7 HIGH
INCREASE PHASE C FAULT COUNTER NC BY 1

CHECK IF NC IS GREATER THAN 3

FAULT ON LINE. JUMP TO SUBROUTINE FOR FAULT ANALYSIS

BLOCK DIAGRAM FOR THE FAULT DETECTION
CHECK IF SUM OF VOLTAGE R1 IS WITHIN SPECIFIED LIMITS

- YES
  - CHECK IF FLAG 4 IS HIGH
    - YES
      - SET FLAG F4 LOW INCREASE ERROR MESSAGE REGISTER 1
    - NO
      - SET FLAG F4 HIGH DECREASE ERROR MESSAGE REGISTER 1
  - NO
    - CHECK IF ERROR MESSAGE REGISTER CHANGED THE SIGN
      - YES
        - JUMP TO SUBROUTINE FOR FAULT ANALYSIS
      - NO
        - REPEAT THE PROCESS FOR PHASE CLOCKS B AND C

BLOCK DIAGRAM FOR THE FAULT DETECTION
The detection program compares the sampled voltage $V_b$ with a specified tolerance limit ($V_z$ or $V_p$), which depends on $V_a$ being at zero or peak. If the variation is greater than specified tolerance limit, the phase fault counter $N_b$ is increased by one. The counter $N_b$ is decreased by one if the variation is within the limits and $N_b$ is greater than zero. The logic is repeated for the phase voltage $V_c$.

The detection program also checks the sum of the two voltages $V_b$ and $V_c$ against a specified limit ($T_z$) if $V_a$ is at a zero crossing or the difference of $V_b$ and $V_c$ against a specified limit ($T_p$) if $V_a$ is at peak. If the sum or difference lies outside the tolerance limit, the fault counter $N_f$ is incremented. If the sum or difference lies within the limits, $N_f$ is decremented, if it is not already zero.

The above process is repeated for the phase B and C clocks. A fault is indicated if any of the fault counters, $N_a$, $N_b$, $N_c$ exceeds three or if $N_f$ exceeds two.

The maximum time to detect a fault is about 8 milliseconds after the fault has occurred. It is also seen from the above scheme that the transient or spikes of short duration, less than 3 milliseconds, will not affect the operation.

The values of the variable parameters $V_z$ and $V_p$ depend upon normal operating phase-voltages. The values of the tolerance limits $T_z$ and $T_p$ depend on the sensitivity of the system.
Fault Type Analysis

This is performed by subroutine CLASSFY and was specially written for the case where sampling device was located at the receiving end S2, shown in Figure 10. The subroutine classifies a fault as a line to ground, double line to ground, line to line, or three phase to ground.

CLASSFY program examines the counters Na, Nb, and Nc for each phase looking for the symptoms which indicate which phases are involved in phase to ground fault. A value of greater than 3 indicates phase is involved in ground fault. If none of the counters is greater than 3, the computer samples line voltages a, b, c and classifies the fault as a line to line fault. The phases involved are found by comparing the phase voltages. The two voltages, which are equal in magnitude, are assumed to be involved in the line to line fault. The block diagrams in Figures 14, 15 give the complete details of the procedure.
PART1

CHECK IF FAULT COUNTER NA FOR PHASE 1 IS GREATER THAN 3

NO

CHECK IF FAULT COUNTER NB FOR PHASE 2 IS GREATER THAN 3

NO

CHECK IF FAULT COUNT NC FOR PHASE 3 IS GREATER THAN 3

NO

LINE 1 TO GROUND FAULT

PART 2

CHECK IF FAULT COUNTER NC FOR PHASE 3 IS GREATER THAN 3

NO

LINE 3 TO GROUND FAULT

EXIT

CHECK IF FAULT COUNTER NB FOR PHASE 2 IS GREATER THAN 3

NO

CHECK IF FAULT COUNT NC FOR PHASE 3 IS GREATER THAN 3

NO

LINE 2 TO GROUND FAULT

EXIT

LINE 1,3 TO GROUND FAULT

LINE 1,2 TO GROUND FAULT

LINE 1,2,3 TO GROUND FAULT

EXIT

BLOCK DIAGRAM TO FIND LINE TO GROUND FAULTS

FIGURE 14
PART 2

SAMPLE PHASE VOLTAGES VA, VB, VC
AT THE POINT WHEN VA IS AT PEAK

CHECK IF VA, VB ARE EQUAL

NO

YES

LINE 1 TO LINE 2 FAULT

EXIT

CHECK IF VB, VC ARE EQUAL

NO

YES

LINE 2 TO LINE 3 FAULT

EXIT

EXIT

CHECK IF VC, VA ARE EQUAL

NO

YES

LINE 3 TO LINE 1 FAULT

EXIT

BLOCK DIAGRAM TO FIND LINE TO LINE FAULT

FIGURE 15
V. TESTS

The operation of the detection scheme was tested on line for the following faults in the laboratory: (Figure 16)

a) Line to ground
b) Double line to ground
c) Line to line
d) Three line to ground

Two separate tests were conducted. In the first test run, the voltage samples were taken at point S1, the sending end, and in the second test run, the voltage samples were taken at S2, the receiving end (Figure 10). All faults were created at the receiving end.

The fault detection program was tested for both fault positions. The fault analysis program was tested for the receiving end only.
LINE TO GROUND FAULT

LINE TO LINE FAULT

TWO LINES TO GROUND FAULT

THREE LINE FAULT

FIGURE 16
VI. CONCLUSION

A working Hybrid Fault Detection scheme has been developed for a three phase transmission line using solid state devices and minicomputer. The scheme was found to be reliable in the laboratory under following values of the parameters

\[ V_z = V_{za} \pm 10\% \times V_{za} \]

where \( V_{za} \) = Running average value of the voltages under normal condition when one of the voltage is crossing zero

\[ V_p = V_{pa} \pm 15\% \times V_{pa} \]

where \( V_{pa} \) = Running average value of the voltages under normal condition when one of the voltages is at its peak

\( T_z \) and \( T_p \) were set at 0.5 volts.

For Fault Analysis program \( V_z \) and \( V_p \) were set at 1 volt.

The above values of the parameters are not fixed. They are dependent upon normal system unbalances and change of the voltage magnitude under fault condition.

The average time between samples is about 1/12 of cycle (1.38 milliseconds on 60 Hz base) and the average time the computer program took between two sampling points was about 350 microseconds (average number of instruction = 70, average instruction execution time = 5 microseconds).
The scheme detects the fault within one-half cycle (8 milliseconds). It was shown that scheme can be used to classify the fault as in test 2. The main advantages of the scheme are:

a. High speed, one-half cycle operation.

b. Simple three phase fault detection.

c. A small amount of information has to be transferred to the computer, thus saving computer time and memory.

d. Transient voltage bursts of less than 3 milliseconds will not affect the operation.

e. Fault data is always compared with prefault data.
VII. FUTURE DEVELOPMENT

At the present time, there has been little development in the use of a computer in system protection in real time. To take advantage of the new solid state technology, the development should be directed towards the use of mini or micro computers at each primary substation. The computer can carry out initial processing of information. The computer should be able to detect the nature and location of an abnormality and initiate any corrective action to be taken locally. The computer should supply information to a central or adjacent local computer when action has to be taken at other locations.

A complete surveillance system by the hybrid computer terminals is required to utilize the advantages of the detection method discussed herein. One isolated installation has little advantage over the present system of "Fault Protection".

The development of a complete and reliable surveillance system will require continued research and development in the following areas:

a) Modify the scheme to sample the phase currents to classify the fault.

b) The establishment of communication between computers or processors. From this information, it will be possible to
locate the fault and initiate the opening of appropriate circuit breaker to isolate the fault.

c) Improve the scheme to avoid false indication due to long time-constant switching surges.
BIBLIOGRAPHY


APPENDIX I

1) Line to Ground

The simple power system shown in Figure 17 consists of a generator, transformer, transmission line, load transformer, and load. Consider a SLG fault at bus C with a fault resistance of 4 ohms. The following data concerning the system is known.

Generator: 25 MVA, 10 kV, x = 0.125 pu, connected Y-grounded

T1: 30 MVA, 10-20 kV, x = 0.105, connected Δ-Y-grounded

Line: Z = 2 + j4 Ω

T2: 20 MVA, 5-20 kV, x = 0.05 pu, connected Y-Δ

Load: static (constant z) load of 10 + j5 MVA at 5 kV

Solution

Select $S_B = 20$ MVA, a load voltage of 5 kV, and compute all system impedances.

Generator: \( x = (0.125)(20/25) = 0.10 \text{ pu} \)

T1: \( x = (0.105)(20/30) = 0.07 \text{ pu} \)

Line: \( z = [(2 + 4j)(20)]/(20)^2 = 0.1 + j0.2 \text{ pu} \)

T2: \( x = 0.05 \text{ pu} \)

Load (as series impedance):

\[
R = \frac{(V)^2 (S_B)^P}{P^2 + Q^2} = \frac{(1.0)^2 (20 \times 10^6)(10 \times 10^6)}{(10 \times 10^6)^2 + (5 \times 10^6)^2} = \frac{200}{125} = 1.6 \text{ pu}
\]

Similarly, \( x = 100/125 = 0.8 \text{ pu} \). Then the positive sequence network for a SLG fault at bus C is represented as shown in Figure 18.

![Figure 18. One-line diagram of the positive sequence network.](image)

The load current \( I_L \) is (with \( V \) as the reference phasor)

\[
I_L = \frac{P - jQ}{V} = \frac{10 - j5}{20} = 0.5 - j0.25 \text{ pu}
\]

The Thevenin voltage at bus C is
\[ V_F = 1.0 + j0 + (0.5 - j0.25)(j0.05) \]
\[ = 1.0125 + j0.025 = 1.0125/127^\circ \text{ pu} \]

We set \( V_F = 1.0125/0^\circ \) and it becomes the reference phasor in the fault calculations. The impedance seen looking in at \( F1 \) with \( E \) shorted is \( 0.1 + j0.37 \) on the left in parallel with \( 1.6 + j0.85 \) on the right, or

\[
Z_1 = \frac{(0.1 + j0.37)(1.6 + j0.85)}{1.7 + j1.22} = 0.332/67.3^\circ = 0.128 + j0.307 \text{ pu}
\]

This is the impedance to the flow of both positive and negative sequence currents.

The zero sequence current sees an open circuit to the left of bus \( A \) with \( A \) grounded (because of the Y-grounded connection) and an open circuit to the right of bus \( C \). Thus \( Z_0 \) is the sum of the line and \( T1 \) impedances, or \( Z_0 = 0.1 + j0.27 \text{ pu} \).

---

**Figure 19.** Sequence networks for SLG fault at bus C.
The complete connection of sequence networks is shown in Figure 19, where \( Z_f \) is shown to be
\[
Z_f = \frac{4 + j0}{Z_B} = \frac{4}{20} = 0.2 \text{ pu}
\]

The total circuit impedance is
\[
Z_t = Z_0 + Z_1 + Z_2 + 3Z_f = 0.956 + j0.884 = 1.3/42.8^\circ \text{ pu}
\]
\[
I_{al} = \frac{V_F}{Z_t}
\]
\[
I_{al} = \frac{1.0125/0^\circ}{1.3/42.8^\circ} = 0.78/-42.8^\circ = 0.572 - j0.530 \text{ pu}
\]

Then \( I_a = 3I_{al} = 2.34/-42.8^\circ \text{ pu.} \)

We may synthesize the phase voltages by first computing the sequence voltages.
\[
V_{a0} = -Z_0 I_{a0} = -(0.288/69.7^\circ)(0.78/-42.8^\circ)
\]
\[
= -0.225/26.9^\circ = -0.200 - j0.102 \text{ pu}
\]
\[
V_{a1} = V_F - Z_1 I_{al} = (1.0125 + j0) - (0.332/67.3^\circ)(0.78/-42.8^\circ)
\]
\[
= (1.0125 + j0) - (0.236 + j0.1075) = 0.7765 - j0.1075
\]
\[
V_{a2} = -Z_2 I_{a2} = -0.236 - j0.1075
\]

Thus
\[
V_a = V_{a0} + V_{a1} + V_{a2} = 0.3405 - j0.3170 = 0.466/42.9^\circ \text{ pu}
\]
\[
V_b = V_{a0} + a^2 V_{a1} + aV_{a2}
\]
\[
= -0.200 - j0.102 - 0.4826 - j0.6212 + 0.2111 - j0.1512
\]
\[
V_c = V_{a0} + aV_{a1} + a^2 F_{a2}
\]

\[
= -0.200 - j0.102 - 0.2964 + j0.7288 + 0.0249 + j0.2588
\]

\[
= -0.4715 + j0.8856 = 0.994/118.3^\circ \text{ pu}
\]

Therefore, instantaneous phase voltages are:

\[
V_a = .466 \cos(\omega t - 42.9^\circ)
\]

\[
V_b = .994 \cos(\omega t - 118.3^\circ)
\]

\[
V_c = .994 \cos(\omega t + 118.3^\circ)
\]

2) Double line to ground fault

Refer again to the system in Figure 17, this time with a 2LG fault and with fault impedances of \( Z_f = 4 \) ohms and \( Z_g = 8 \) ohms.

The fault is at bus C, so the sequence networks are internally the same as those of Figure 19.

Solution

The pu impedances are

\[
Z_0 = 0.1 + j0.27,
\]

\[
Z_1 = Z_2 = 0.128 + j0.307
\]

\[
Z_f = 0.2 + j0,
\]

\[
Z_g = 0.4 + j0
\]

As before, \( V_F = 1.0125 + j0 \) pu. The network to be solved appears schematically as shown in Figure 20.

The total impedance seen by current \( I_{a1} \) is
\[ Z_t = 0.328 + j0.307 + \frac{(0.328 + j0.307)(1.5 + j0.27)}{1.828 + j0.577} \]

\[ = 0.617 + j0.515 = 0.805/39.8^\circ \text{ pu} \]

Then \( I_{al} \) is

\[ I_{al} = \frac{1.0125/0^\circ}{0.805/39.8^\circ} = 1.259/-39.8^\circ = 0.965 - j0.805 \text{ pu} \]

**Figure 20. A 2LG fault network.**

By inspection of Figure 20 we compute

\[ I_{a0} = -\frac{Z_2 + Z_f}{Z_2 + Z_0 + 2Z_f + 3Z_g} I_{al} \]

\[ = \frac{0.449/43.1^\circ}{1.92/17.5^\circ} (1.259/-39.8^\circ) = -0.294/-14.2^\circ \]

\[ = -(0.285 - j0.072) \text{ pu} \]

Similarly,

\[ I_{a2} = -\frac{Z_0 + Z_f + 3Z_g}{Z_2 + Z_0 + 2Z_f + 3Z_g} I_{al} = -\frac{1.525/10.2^\circ}{1.92/17.5^\circ} (1.259/-39.8^\circ) \]

\[ = -1.00/ -47.1^\circ = -(0.68 - j0.732) \text{ pu} \]
Checking these results, we compute 
\[ I_a = I_{a0} + I_{a1} + I_{a2} = 0 - j0.001 = 0. \]

Synthesizing the other phase currents, we have
\[
I_b = I_{a0} + aI_{a1} + a^2I_{a2} \\
= -0.285 + j0.072 - 1.181 - j0.432 - 0.293 - j0.955 \\
= -1.759 - j1.315 = -2.195/36.8° \text{ pu}
\]

and
\[
I_c = I_{a0} + aI_{a1} + a^2I_{a2} \\
= -0.285 + j0.072 + 0.215 + j1.24 + 0.977 + j0.210 \\
= 0.907 + j1.522 = 1.774/59.2° \text{ pu}
\]

The sequence voltages are
\[
V_{a0} = -Z_0 I_{a0} = -(0.1 + j0.27)(-0.285 + j0.072) \\
= 0.048 + j0.07 \text{ pu}
\]

\[
V_{a1} = V_F - Z_1 I_{a1} = 1.0125 - (0.128 + j0.307)(0.965 - j0.805) \\
= 1.0125 - (0.370 + j0.193) - 0.6425 - j0.193 \text{ pu}
\]

\[
V_{a2} = -Z_2 I_{a2} = -(0.128 + j0.307)(-0.68 - j0.732) \\
= 0.311 + j0.115 \text{ pu}
\]

The phase voltages are
\[
V_a = V_{a0} + V_{a1} + V_{a2} = 1.001 - j0.008 \text{ pu} \quad 1.001/0 \text{ pu}
\]

\[
V_b = V_{a0} + a^2 V_{a1} + aV_{a2} \\
= 0.0479 + j0.07 - 0.488 - j0.4595 - 0.2552 + j0.212 \\
= -0.6953 - j0.1775 = -0.717/-165.7° \text{ pu}
\]


\[ V_c = V_{a0} + aV_{a1} + a^2V_{a2} \]
\[ = 0.0497 + j0.07 - 0.154 + j0.6525 - 0.0558 - j0.3270 \]
\[ = -0.1619 + j0.2555 = -0.303/122.4^\circ \text{ pu} \]

Therefore, instantaneous phase voltages are:

\[ V_a = 1.001 \cos (\omega t) \]
\[ V_b = .717 \cos (\omega t - 165.7^\circ) \]
\[ V_c = .303 \cos (\omega t + 122.4^\circ) \]

3) Line to line fault

Compute the phase voltages and currents for a LL fault at bus C of Figure 17 where a fault impedance of 4 ohms is assumed between phases b and c.

Solution

The sequence networks are exactly as shown in Figure 19, but their interconnection is that of Figure 21. With the new connection the total impedance is

\[ Z_t = Z_1 + Z_2 + Z_f = 0.456 + j0.614 = 0.765/53.4^\circ \text{ pu} \]

Then

\[ I_{al} = I_{a2} = \frac{V_F}{Z_t} = \frac{1.0125/0^\circ}{0.765/53.4^\circ} \]
\[ = 1.325/\overline{53.4^\circ} = 0.788 - j1.065 \text{ pu} \]
\[ I_c = -I_c = -j\sqrt{3}I_{al} = -1.86 - j1.38 = -2.32/\overline{36.6^\circ} \text{ pu} = 1320 \text{ A} \]

This system voltages may also be synthesized from a knowledge of
the sequence currents and sequence network connections.

\[ V_{a1} = V_F - Z_1 I_{a1} = 1.0125 - (0.332/67.3^\circ)(1.325/-53.4^\circ) \]
\[ = 1.0125 - 0.427 - j0.1055 = 0.5855 - j0.1055 \text{ pu} \]

\[ V_{a2} = -Z_2 I_{a2} = -(0.332/67.3^\circ)(-1.325/-53.4^\circ) \]
\[ = 0.44/13.9^\circ = 0.427 + j0.1055 \text{ pu} \]

and we compute

\[ V_a = V_{a1} + V_{a2} = 1.0125 + j0 = 1.0125/0 \]
\[ V_b = a^2 V_{a1} + aV_{a2} = -0.389 - j0.448 - 0.310 + j0.317 \]
\[ = -0.699 - j0.131 = 0.705/-168.4^\circ \]
\[ V_c = aV_{a1} + a^2 V_{a2} = -0.196 + j0.554 - 0.118 - j0.423 \]
\[ = -0.314 + j0.131 = 0.342/157.4^\circ \]

Figure 21. Sequence network connection for a LL fault

Therefore, instantaneous phase voltages are:

\[ V_a = 1.012 \cos (\omega t) \]
\[ V_b = 0.705 \cos (\omega t - 168.4^\circ) \]
\[ V_c = 0.342 \cos (\omega t + 157.4^\circ) \]
4) Three phase to ground fault

A three phase fault with fault impedance of 4 ohms \(Z_f = 4 \text{ ohm}\) at bus C of Figure 17.

Solution

The pu fault impedance is \(Z_f = \frac{4}{Z_B} = \frac{4}{20} = 0.2 \text{ pu}\). Thus

\[
I_{al} = I_a = \frac{V_F}{Z_1 + Z_f} = \frac{1.0125 + j0}{0.328 + j0.307}
\]

or

\[
I_{al} = \frac{1.0125/0^\circ}{0.449/43.1^\circ} = 2.255/\text{-}43.1^\circ = 1.647 - j1.54 \text{ pu}
\]

The voltage at the fault is

\[
V_a = V_{al} = Z_f I_{al} = (0.2)(1.647 - j1.54) = 0.329 - j0.308
\]

\[
= 0.451/\text{-}43.1^\circ \text{ pu}
\]

Currents and voltages in phases b and c are found by applying phase rotations of -120° and +120° respectively to the above results.

Therefore instantaneous phase voltages are:

\[
V_a = 0.451 \cos (\omega t - 43.1^\circ)
\]

\[
V_b = 0.451 \cos (\omega t - 163.1^\circ)
\]

\[
V_c = 0.451 \cos (\omega t + 76.1^\circ)
\]

The magnitude of the phase voltages under various fault conditions at the prefault zero crossing and peak of the voltage \(v_b\) waveform.
Case 1

Phase voltages at prefault zero crossing of the voltage $V_b$

which occurs at $\omega t = 30^\circ$

a) Line to ground fault

\[
V_a = 0.466 \cos (\omega t-42.8^\circ) = 0.456 \text{ pu}
\]

\[
V_b = 0.994 \cos (\omega t-118.3^\circ) = 0.0289 \text{ pu}
\]

\[
V_c = 0.994 \cos (\omega t+118.3^\circ) = -0.846 \text{ pu}
\]

b) Double line to ground fault

\[
V_a = 1.001 \cos (\omega t) = 0.866 \text{ pu}
\]

\[
V_b = 0.717 \cos (\omega t-165.7^\circ) = -0.5136 \text{ pu}
\]

\[
V_c = 0.303 \cos (\omega t+122.4^\circ) = -0.268 \text{ pu}
\]

c) Line to line fault

\[
V_a = 1.012 \cos (\omega t) = 0.866 \text{ pu}
\]

\[
V_b = 0.705 \cos (\omega t-168.4^\circ) = -0.524 \text{ pu}
\]

\[
V_c = 0.342 \cos (\omega t+157.4^\circ) = -0.339 \text{ pu}
\]

d) Three phase to ground fault

\[
V_a = 0.451 \cos (\omega t-43.1^\circ) = 0.439 \text{ pu}
\]

\[
V_b = 0.451 \cos (\omega t-163.1^\circ) = -0.308 \text{ pu}
\]

\[
V_c = 0.451 \cos (\omega t+76.1^\circ) = -0.131 \text{ pu}
\]

Case 2

Phase voltages at the prefault peak of the voltage $V_b$ which occurs at $\omega t = 120^\circ$
a) Line to ground fault

\[ V_a = 0.466 \cos(\omega t - 42.8^\circ) = 0.103 \text{ pu} \]

\[ V_b = 0.994 \cos(\omega t - 118.3^\circ) = 0.993 \text{ pu} \]

\[ V_c = 0.994 \cos(\omega t + 118.3^\circ) = -0.52 \text{ pu} \]

b) Double line to ground fault

\[ V_a = 1.001 \cos(\omega t) = -0.5 \text{ pu} \]

\[ V_b = 0.717 \cos(\omega t - 165.7^\circ) = 0.5 \text{ pu} \]

\[ V_c = 0.303 \cos(\omega t + 122.4^\circ) = -0.139 \text{ pu} \]

c) Line to line fault

\[ V_a = 1.012 \cos(\omega t) = -0.5 \text{ pu} \]

\[ V_b = 0.705 \cos(\omega t - 168.4^\circ) = 0.467 \text{ pu} \]

\[ V_c = 0.342 \cos(\omega t + 157.4^\circ) = 0.042 \text{ pu} \]

d) Three phase to ground fault

\[ V_a = 0.451 \cos(\omega t - 43.1^\circ) = 0.1019 \text{ pu} \]

\[ V_b = 0.451 \cos(\omega t - 163.1^\circ) = 0.329 \text{ pu} \]

\[ V_c = 0.451 \cos(\omega t + 76.1^\circ) = -0.431 \text{ pu} \]
APPENDIX II

COMPUTER CHARACTERISTICS

The computer block diagram (Figure 22) shows the basic internal function relationships of the 960A computer.

a) The standard semiconductor (MOS) memory of the 960A has a storage capacity ranging from 4096 to 65,536 words. Space is provided within the 960A enclosure for 32,768 words of semiconductor memory.

NOTE
The maximum storage capacity of the 960A computer is 65,536 words. This storage may optionally be externally mounted core memory which is available in 4096 word increments.

b) The Central Processing Unit (CPU) can address the memory, perform arithmetic and logic functions, and sequence and control the exchange of information between memory and other elements of the computer. The CPU features an arithmetic unit and a read-only memory controller.

c) The Communication Register Unit (CRU) controls the exchange of information between the computer and external equipment.

d) The Direct Memory Access Channel (DMAC) interfaces the computer with high-speed automatic computer peripherals,
such as disc storage units, line printers, and magnetic tape units. By using a separate controller for each device, concurrent operation of high speed peripherals is achieved.

**Specifications**

a) Organization

Parallel Operation

Single and double address logic

Direct addressing of entire memory

Indirect addressing with pre-indexing or post indexing

32 bit instruction word

16 bit data word

16 active hardware registers (16-bit) for arithmetic, index, or mask operations, and base addressing

Supervisor and worker execution mode architecture

Memory protect feature for variable amounts of memory

Three levels of priority interrupts

b) Performance

4 MHz system clock rate

500 nanosecond memory store sequence

750 nanosecond memory fetch sequence

500 nanosecond memory access time

Hardware multiply/divide option
Execution times:

Load: 3.3 microseconds
Store: 3.6 microseconds
Add: 3.6 microseconds
Set CRU bit: 2.8 microseconds
Load register in CRU: 4.2 - 8.2 microseconds
(1-16 bits)

c) Memory

Semiconductor memory using 1024 X 1-bit dynamic MOS arrays

Internal storage for up to 32,768 words of MOS memory in increments of 1024 words

Power failure protection

Magnetic core memory interface option

Minimum storage capacity, 4096 words
Maximum storage capacity, 65,536 words

d) Input/Output System

Direct Memory Access Channel (expandable to 8) with 16-bit parallel transfer, 1 million words per second burst rate, and parity checking interface

Communications Register Unit with up to 4096 I/O points and 4 million bits per second burst rate
TI 960A COMPUTER BLOCK DIAGRAM

FIGURE 22
e) Instruction Set - 78 instructions
   9-bit and field manipulating instructions
   36 register-memory instructions
   5 powerful memory-memory instructions
   28 flexible program control instructions

f) Physical Characteristics
   Dimension (rack mount configuration)
      Height - 12.25 inches
      Width - 19 inches
      Depth - 24 inches
      Weight - 75 pounds
   Power Requirements: 115V ± 10%, 47-63 Hz
   Power Consumption: 420 watts, average

g) Operating conditions:
   Temperature (@ sea level)
      0°C to 50°C
      32°F to 122°F
   Humidity 10% - 95%
   Altitude 0-10,000 feet
APPENDIX III

Computer Program for the Fault Detection
Computer Program for the Fault Detection
<table>
<thead>
<tr>
<th>Location</th>
<th>Condition</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Clock 3 or C? is high</td>
<td>Check if clock 3 or C? is high</td>
</tr>
<tr>
<td>1</td>
<td>Channel 4 conversion cycle</td>
<td>Check if line 1 is GND</td>
</tr>
<tr>
<td>1</td>
<td>Line 1 is GND</td>
<td>Check if line 1 is GND</td>
</tr>
</tbody>
</table>

Computer Program for the Fault Detection
Computer Program for the Fault Detection

<table>
<thead>
<tr>
<th>GT7</th>
<th>GET</th>
<th>GT6</th>
<th>GT5</th>
<th>G7H</th>
<th>PK6</th>
<th>PK5</th>
<th>PK4</th>
<th>PK3</th>
<th>PK2</th>
<th>PK1</th>
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<td>Y3</td>
<td>Y2</td>
<td>Y1</td>
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<tr>
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<td>Y1</td>
<td>Y1</td>
</tr>
</tbody>
</table>

CHECK IF LINE 2 IS GND

Computer Program finds type of line fault

LINE 3 TO GND FAULT

LINE TO LINE FAULT 1, 3

LINE TO LINE FAULT 2, 3

LINE 1 TO GND FAULT

LINE TO LINE FAULT 1, 3
Computer Program for the Fault Detection