AN ABSTRACT OF THE THESIS OF

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Title: Hybrid, High Speed Fault Detection Based on Instantaneous

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John F. Engle

This fault detection scheme is based on sampling the instan-taneous phase voltages and checking their sum and magnitude against a specified voltage. Faults on the system cause unbalances and distortion of the phase voltages and currents. The currents and voltages change in magnitude and/or phase position with respect to the prefault condition. The measurement of this deviation from the normal condition indicates a fault. This scheme detected the fault within one-half cycle (8 milliseconds) in the laboratory. It is shown that this scheme is simpler and faster to implement than conventional detection schemes.

Hybrid, High Speed Fault Detection Based On
Instantaneous Line Voltages

by

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Typed by Eula Weathers for Hiranand Balchand Ramchandani

ACKNOWLEDGMENTS

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HYBRID, HIGH SPEED FAULT DETECTION BASED ON INSTANTANEOUS LINE VOLTAGES

I. INTRODUCTION

Function of a Relay

A power system is designed to generate, transmit, and distribute electric power of sufficient quantity to meet present and estimated future demands of the users in some particular area. The main parts of the system are generators, transformers, transmission lines, switch gear and distribution circuits. Each part is an essential component and failure of any part destroys the capacity and function of the system. To insure reliable service and a reasonable return on the investment, the whole system should be kept in service to delivery energy without interruption.

This may be accomplished in two ways. One way is to maintain each component to prevent failure and to provide alternate links. The maintenance and the cost of alternate links allow this course to proceed to a limit. A second way is to minimize and control the effects of the failures that do occur. The main functions of protection are to minimize damage to apparatus, maintain safety and to minimize interference of the fault[1] with the normal operation of the

Fault is herein defined as the failure of high voltage insulation, which will cause the system to become short-circuited at a point.

unfaulted parts of the system.

The above function of protection is performed by the device known as a protective relay. The relays are the sensing devices which detect and analyze the fault and operate the circuit breaker to isolate the faulted circuit. The protective relay recognizes and analyzes the fault by detecting the change in magnitude of electrical quantities. The basic quantities, which may change when a fault occurs are current, voltage, phase angle (direction), and frequency.

Development

The art of protective relaying has been established for many years. The relay devices and their application have undergone continued progressive development keeping close pace with the growth and requirement of electric power systems.

The protection characteristics for early power systems were simple and direct because the power systems were simple, consisting only of power stations supplying power over short distance to local loads.

The system growth and interconnection have given rise to an increased need for faster and better protection. As a result, a great deal of work has been performed in the study of relay protection under service conditions, the reconstruction and adoption of old forms of protection and the introduction of new types of relays and

protection schemes.

Although the electro-mechanical devices are highly reliable, much work has been conducted in order to develop solid state and digital relays. Thus relay systems have improved in both reliability and accuracy as well as showing some increase in operating speed.

The development of electro-mechanical and solid state relays has been described in detail in literature. In this thesis only the development of the digital relays is discussed briefly.

Digital Relaying

The use of a minicomputer for protection was first considered in late 1960's (14). Since then more attention has been given to this subject (3, 4, 6, 9, 10, 11, 12, 14, 15, 16, 17, 18). Mann and Morrison (10) used a minicomputer for the protection of a single three phase line. They detected, classified, and calculated the impedance of the faulted line in less than 10 milliseconds (one-half cycle on 50 Hz base) in the laboratory after the occurrence of the fault. Rockefeller and Udren (15, 16) used a modified method of Mann and Morrison (10) to protect the line. They were able to detect the fault and send a trip signal to the circuit breaker, under simulated field conditions, from 1/4 to 3 cycle (60 Hz base) after the occurrence of the fault. In all cases, a single dedicated minicomputer was used to perform the protection for a single three-phase line terminal.

Most of the above schemes proposed to date monopolize computer time by continually scanning current and voltage waves in order to detect a fault condition. The purpose of this thesis is to develop a detection method which will use less computer time and memory without sacrificing the efficiency of fault detection. The saving in computer time and memory will allow enough time for the computer to perform other substation tasks or monitor additional transmission lines.

II. THEORY

This detection scheme works on the principle that the sum of the three phase-voltages of a three-phase system in the steady state is nearly equal to zero as shown by Figures 1 and 2.

Faults on the system cause unbalances and distortion of the phase voltages and currents. The currents and voltages change in magnitude and/or phase position with respect to their prefault condition. The magnitude of the currents and voltages depends on the different sources that generate them and their reactances up to the fault location. Sources of the short-circuit currents are utility systems, generators, sychronous motors, induction motors and transformers.

The current magnitude is highest during the first half cycle and decreases in value after a few cycles as the equivalent reactances of the machines change from subtransient to transient state. The magnitude of the short-circuit current is further increased during the first few cycles by the so-called dc component.

The effects of a fault on the phase voltages is best illustrated by simulating faults on a simple power system as shown in Figure 3.

The following faults were simulated on the system shown in Figure 3:

1) Single line to ground

2) Double line to ground

3) Line to line

4) Three phase to ground

The method of symmetrical components was used to calculate the short circuit voltages and currents, assuming a value of fault resistance. The complete analytical solution is given in Appendix I. In above example the subtransient reactance of the generator was used to show the change in the voltage magnitudes during first few cycles of the fault condition. Figures 4 through 7 show the instantaneous phase voltages for first few cycles after occurrence of a fault. Figures 8 and 9 show the phasor diagrams associated with the post fault wave forms.
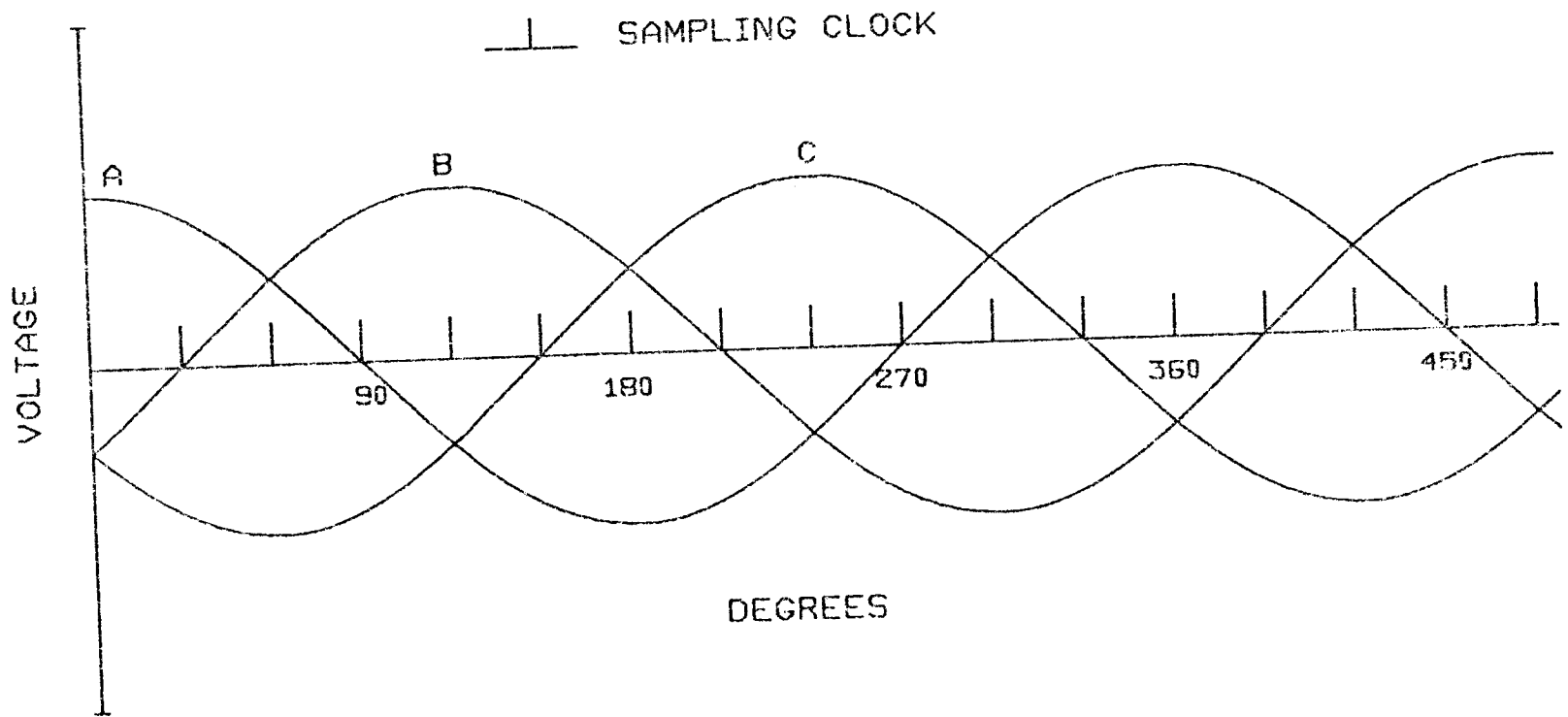
PHASE VOLTAGES UNDER NORMAL
BALANCED CONDITION

FIGURE 1

VCA   VCN   VAB

VAN

VBN

VBC
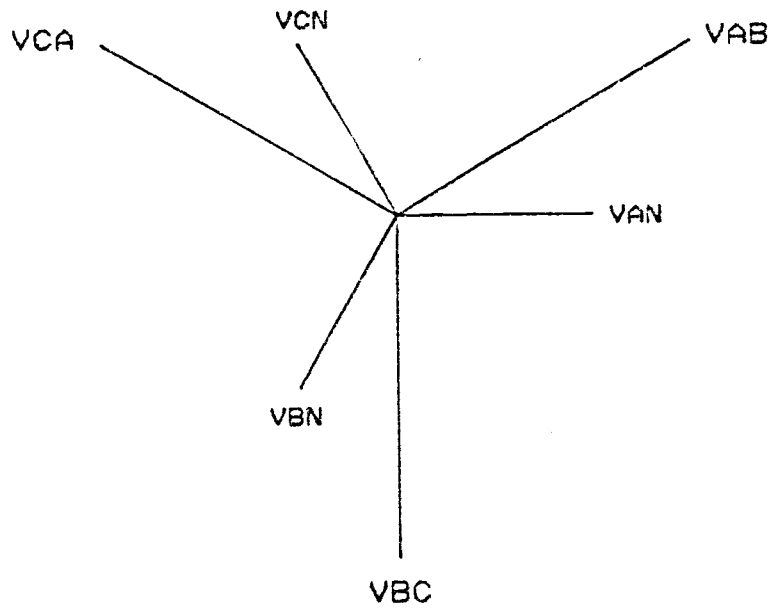
VOLTAGE PHASOR DIAGRAM
FOR NORMAL CONDITION

FIGURE 2

TRANSFORMER   TRANSFORMER

GEN   TRANSMISSION LINE   LOAD
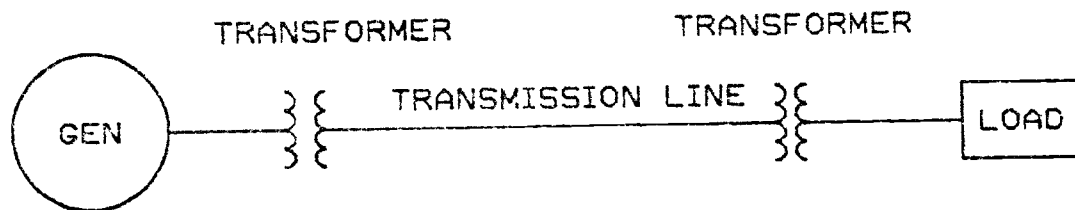
POWER SYSTEM
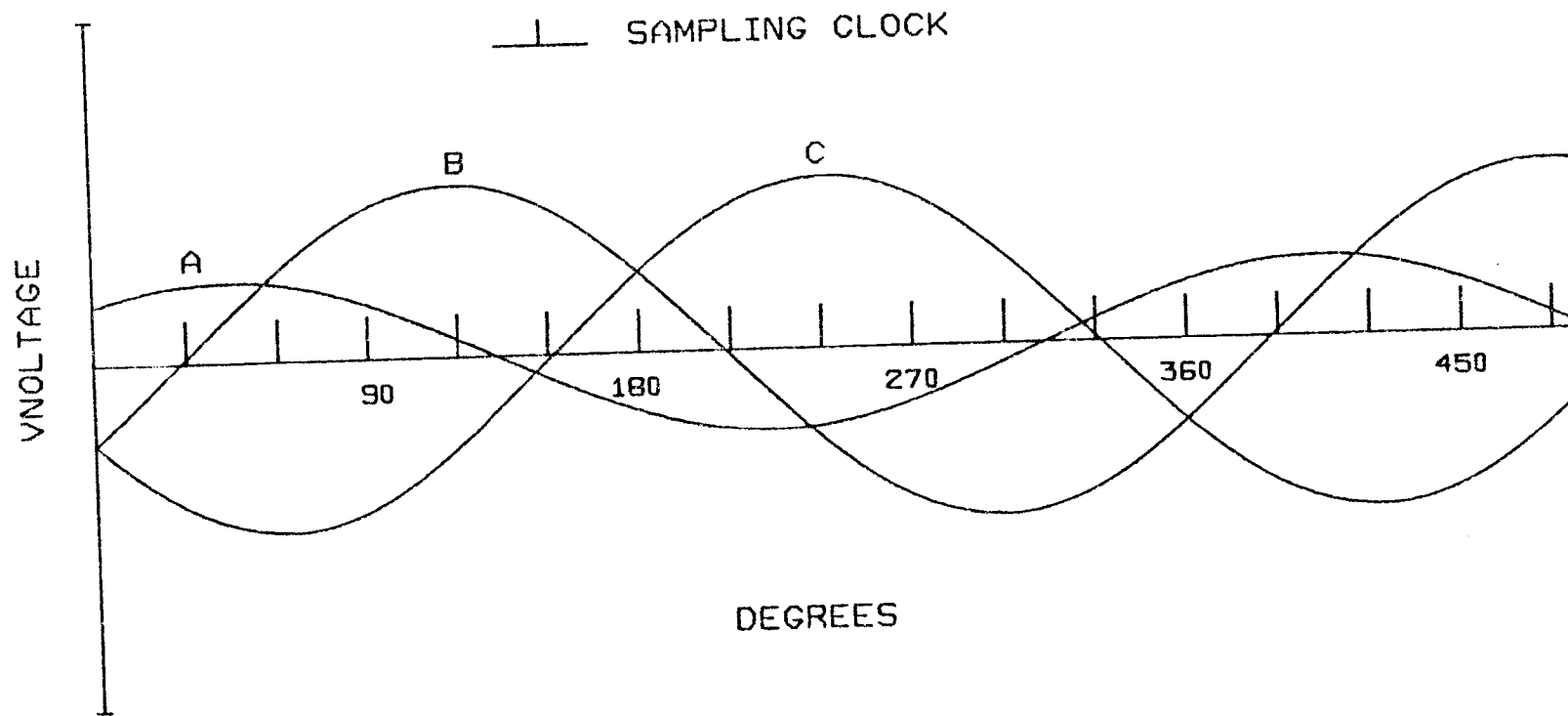
FIGURE 3

PHASE VOLTAGES FOR LINE TO GROUND
FAULT WITH A FAULT RESISTANCE

FIGURE 4
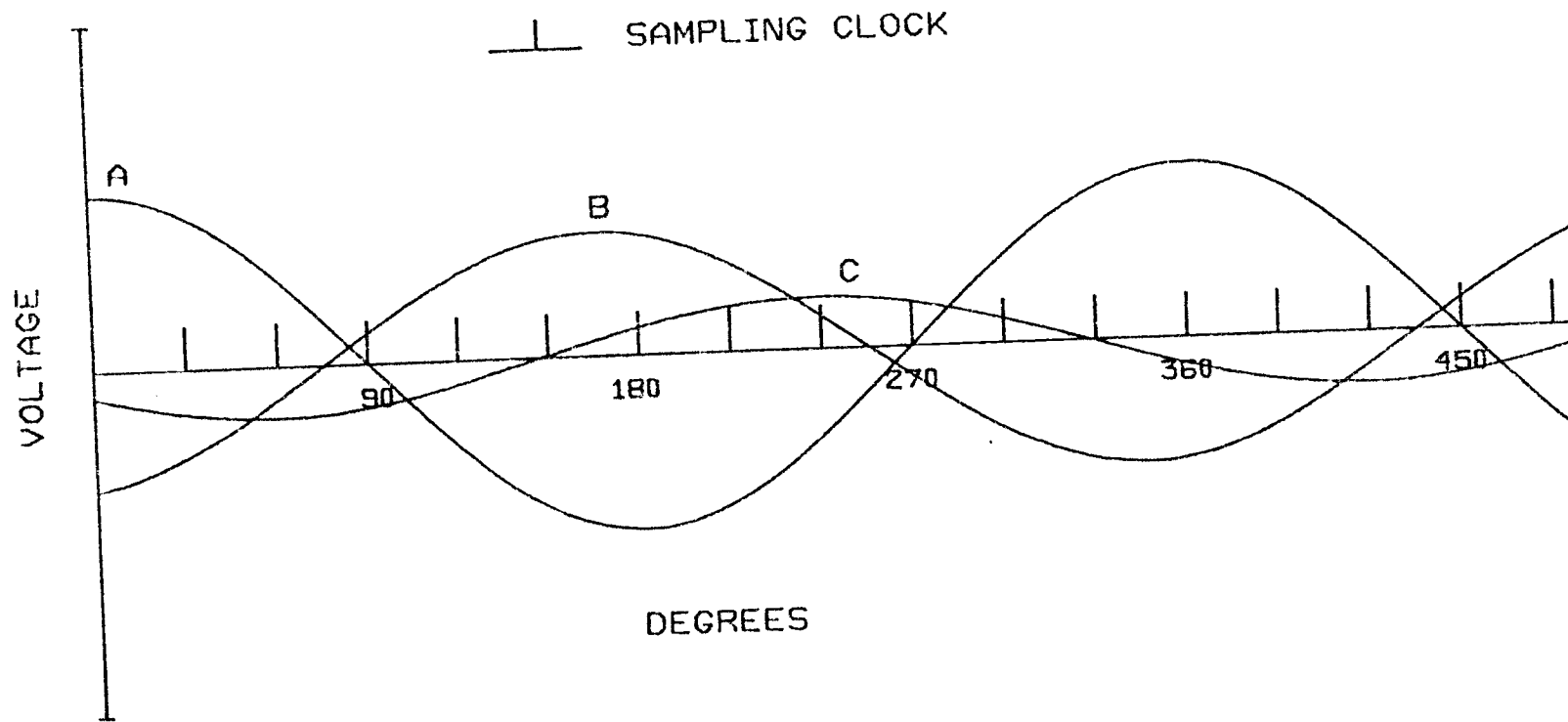
PHASE VOLTAGES FOR TWO LINE TO GROUND
FAULT WITH A FAULT RESISTANCE

FIGURE 5

SAMPLING CLOCK

VOLTAGE

A

B

C

90   180   270   360   450

DEGREES
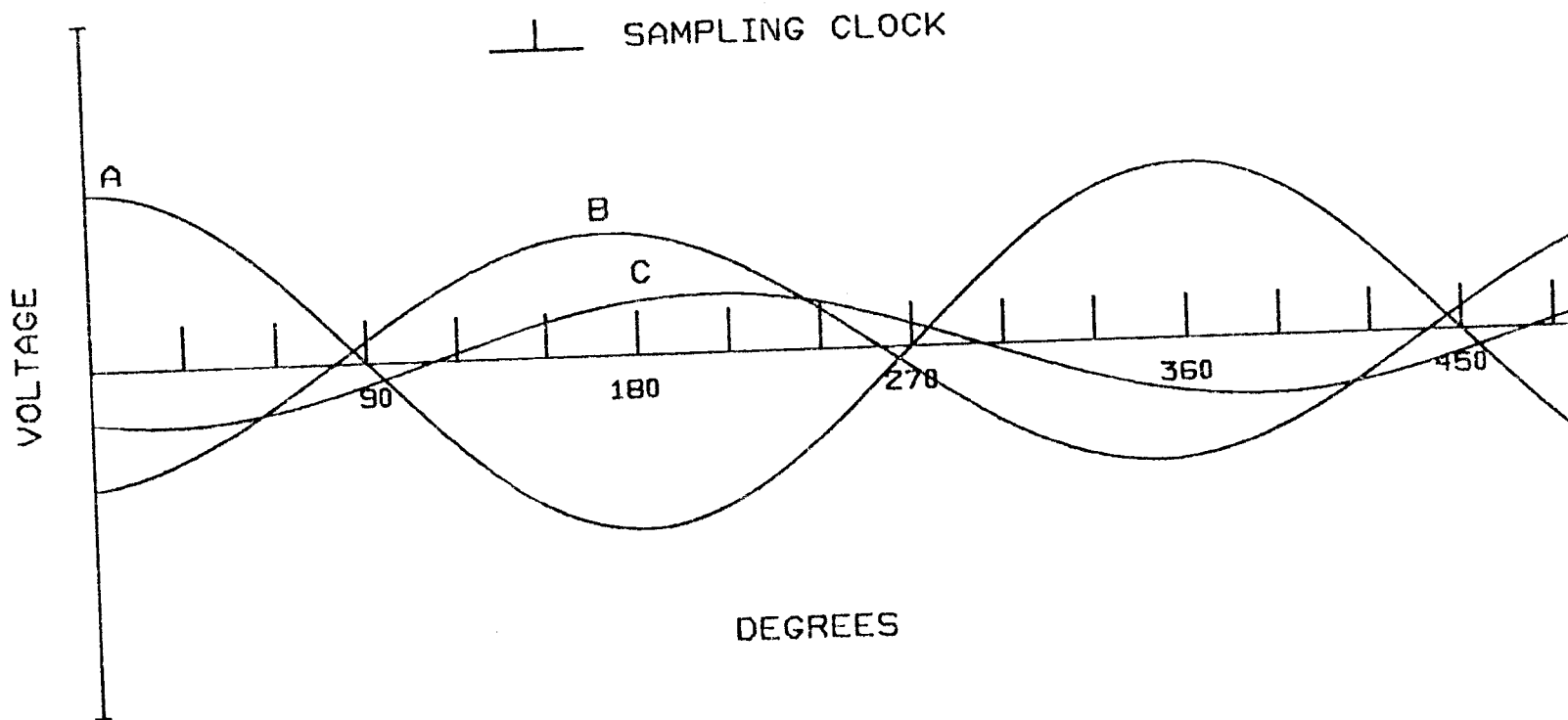
PHASE VOLTAGES FOR LINE TO LINE
FAULT WITH A FAULT RESISTANCE

FIGURE 6

10

┴ SAMPLING CLOCK
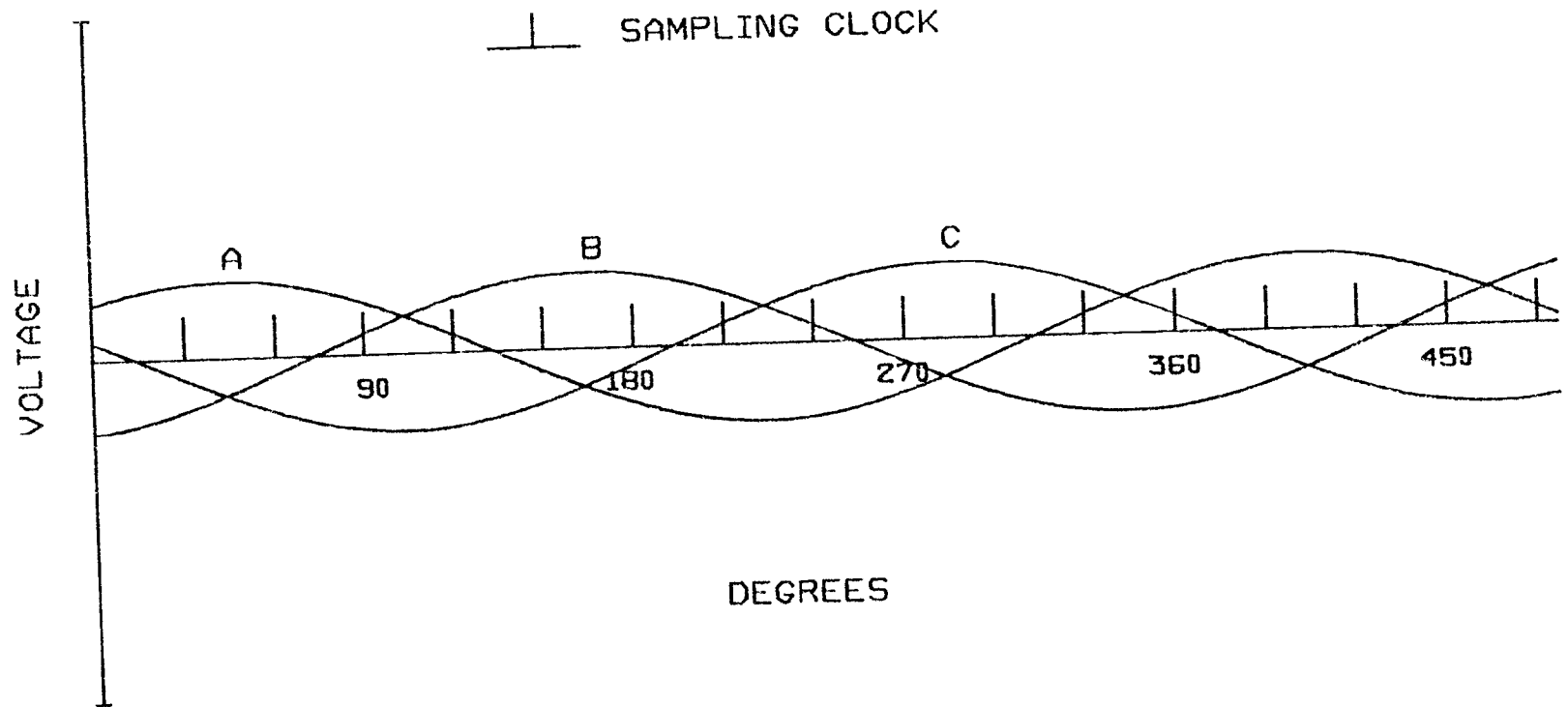
PHASE VOLTAGES FOR THREE LINE TO GROUND
FAULT WITH A FAULT RESISTANCE

FIGURE 7
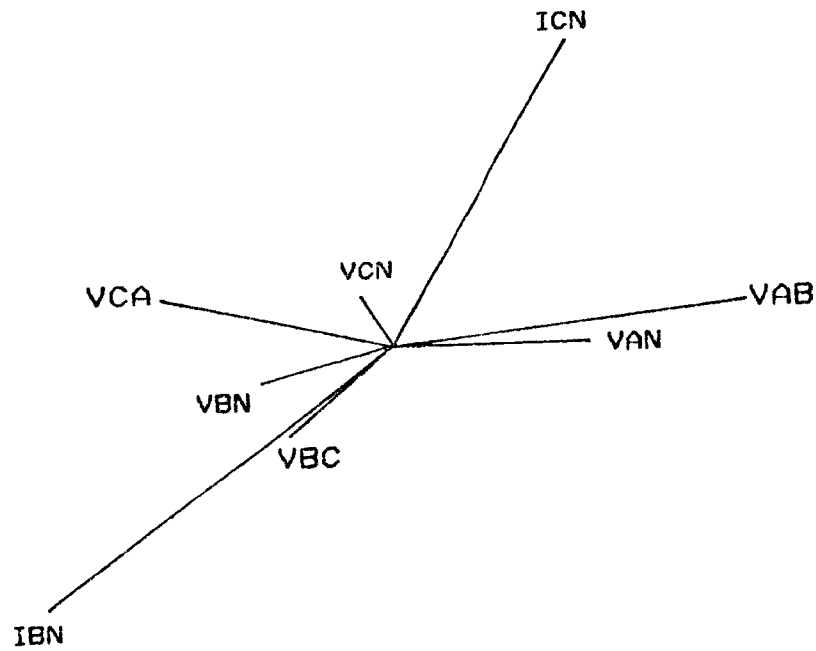
TWO LINE TO GROUND FAULT
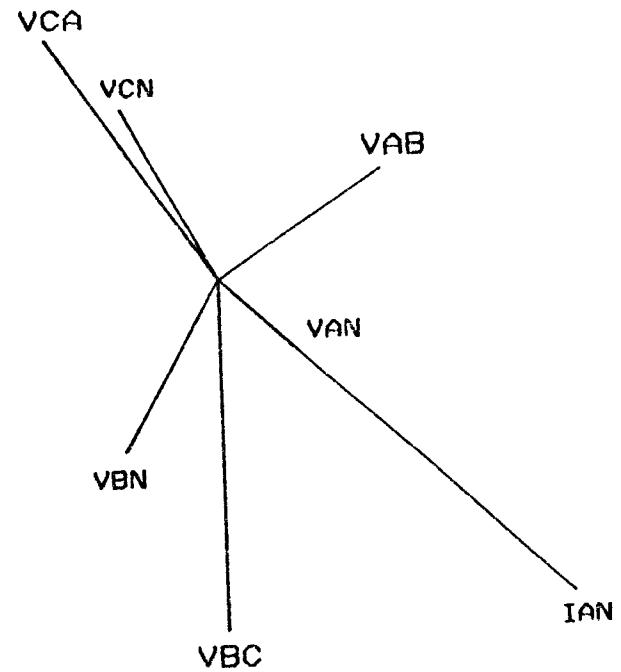
LINE TO GROUND FAULT

CURRENTS AND VOLTAGES PHASOR DIAGRAMS

FIGURE 8

ICN

VCA

VCN

VBN

VAB

VAN

VBC

IBN

IAN

ICN

VCA VCN VAB

VBN VAN

VBC

IBN
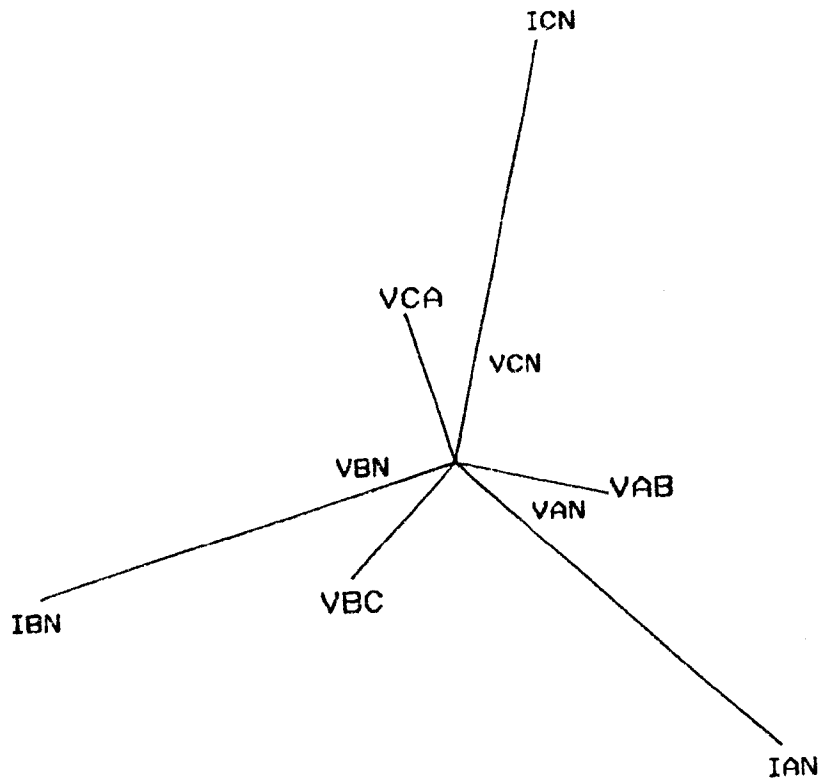
THREE LINE TO GROUND FAULT
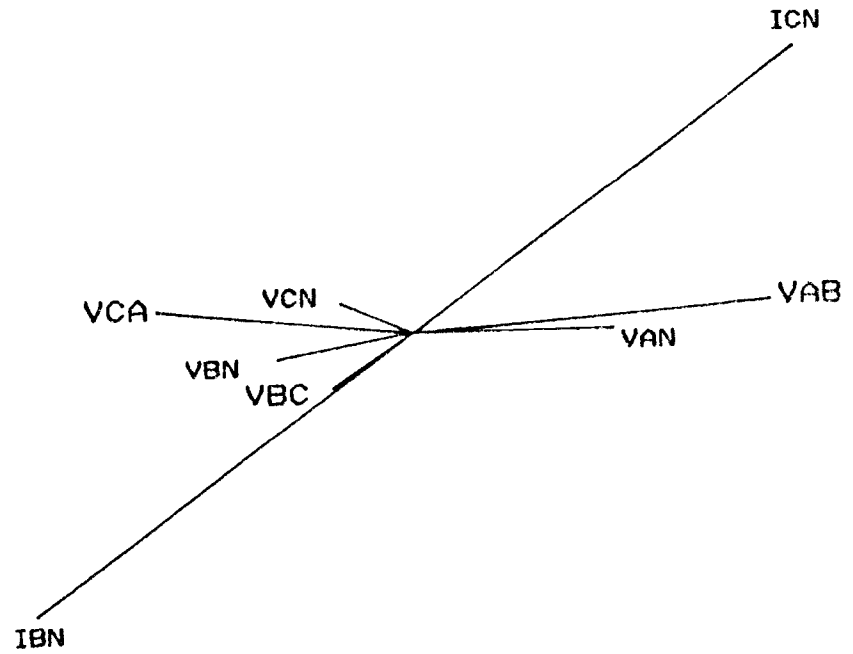
LINE TO LINE FAULT

CURRENTS AND VOLTAGES PHASOR DIAGRAMS
FIGURE 9

13

The exact conditions that exist when a fault occurs vary widely in different systems. The distortion also depends on the severity of the fault and the system reactance to the fault.

From Figure 1 (a balanced prefault condition), we observe that at each zero crossing of the three voltage waveforms, the sum of the other two voltages is zero and at each peak the other two voltages are equal. This is analytically shown below:

Let

$$V_a = V_m \cos(\omega t)$$

$$V_b = V_m \cos(\omega t - 120°)$$

$$V_c = V_m \cos(\omega t + 120°)$$

Case 1

$V_m = 1.0$ unit and voltage V_b waveform is crossing zero at $\omega t = 30°$ (Figure 1).

Therefore

$$V_a = \cos(30°) = 0.866 \text{ pu}$$

$$V_b = \cos(-90°) = 0$$

$$V_c = \cos(150°) = -0.866 \text{ pu}$$

This proves that at the zero crossing of the voltage waveform, the sum of the other two voltages is zero ($V_a + V_c = 0$).

Case 2

Voltage V_b waveform is at the peak at $\omega t = 120°$. Therefore

$$V_a = \cos(120°) = -0.5 \text{ pu}$$

$$V_b = \cos(0°) = 1.0 \text{ pu}$$

$$V_c = \cos(240°) = -0.5 \text{ pu}$$

This proves that at the peak of the voltage waveform, the other two voltages are equal ($V_a = V_c$).

From Figures 4 through 7 we observe that these conditions do not exist when the system is under fault and the samples are taken at the zero crossing and peak times of the prefault voltage waveforms. From Figures 4 through 7, we also observe that the magnitude of the phase voltages is different from the prefault value. This is analytically shown below in the case of a line to ground fault.

Instantaneous phase voltages in the case of a line to ground fault are: (data taken from Appendix I)

$$V_a = .466 \cos(\omega t - 42.8°)$$

$$V_b = .994 \cos(\omega t - 118.3°)$$

$$V_c = .994 \cos(\omega t + 118.3°)$$

Case 1

Prefault zero crossing of the voltage V_b occurs when $\omega t = 30°$. Therefore, the phase voltages at that instant are:

$$V_a = .466 \cos(30-42.8°) = 0.456 \text{ pu}$$

$$V_b = .994 \cos(30-118.3°) = 0.0289 \text{ pu}$$

$$V_c = .994 \cos(30+118.3°) = -0.846 \text{ pu}$$

This proves that the sum of the other two voltages is not equal to zero ($V_a + V_c = -.39$). We also observe that the voltage V_a is not equal to its prefault value.

Case 2

Prefault peak of the voltage V_b occurs when $\omega t = 120°$. Therefore, the phase voltages at instant are:

$$V_a = .466 \cos(120-42.8°) = 0.103 \text{ pu}$$

$$V_b = .994 \cos(120-118.3°) = 0.993 \text{ pu}$$

$$V_c = .994 \cos(120+118.3°) = -0.521 \text{ pu}$$

This proves that the two voltages are not equal ($V_a \neq V_c$) and the magnitude of V_a is not equal to its prefault value. For other types of faults, the magnitudes of the phase voltages at the prefault zero crossing and peak of V_b are given in Appendix I.

In the case of a three phase-to-ground fault, there is a possibility that the sum of the voltages is equal to zero, but that there will always be a change in voltage magnitude.

This scheme takes advantage of the above abnormalities of the system voltages during the faults and detects the change in the system parameters from normal to abnormal conditions. If the

change is more than a specified tolerance limit, a fault is indicated.

The detection tolerance limit will depend upon the sensitivity of the

detection scheme and the normal system operating unbalances.

III. CONSTRUCTION

Figure 10 shows the laboratory test installation for the fault

detection scheme which was used for verification of the design

theory. There are two major parts of the scheme:

1) Minicomputer

2) Control Logic

The main characteristics of each part are described below.

Minicomputer

T1960A minicomputer was used to sample the transmission

lines and to carry out the necessary calculation and control functions.

This particular minicomputer was not specially designed for the fault

detection scheme but was employed becuase of its availability.

T1960A computer is manufactured by the Texas Instruments, Inc.

Figure 22 shows the computer block diagrams of the basic internal

functional relationships of the computer. The main characteristics

of the computer are given in Appendix II.

Control Logic

The control logic consists of three independent sampling clocks.

Each sampling clock is synchronized to system frequency prior to the

fault. The main parts of the sampling clock are shown by block
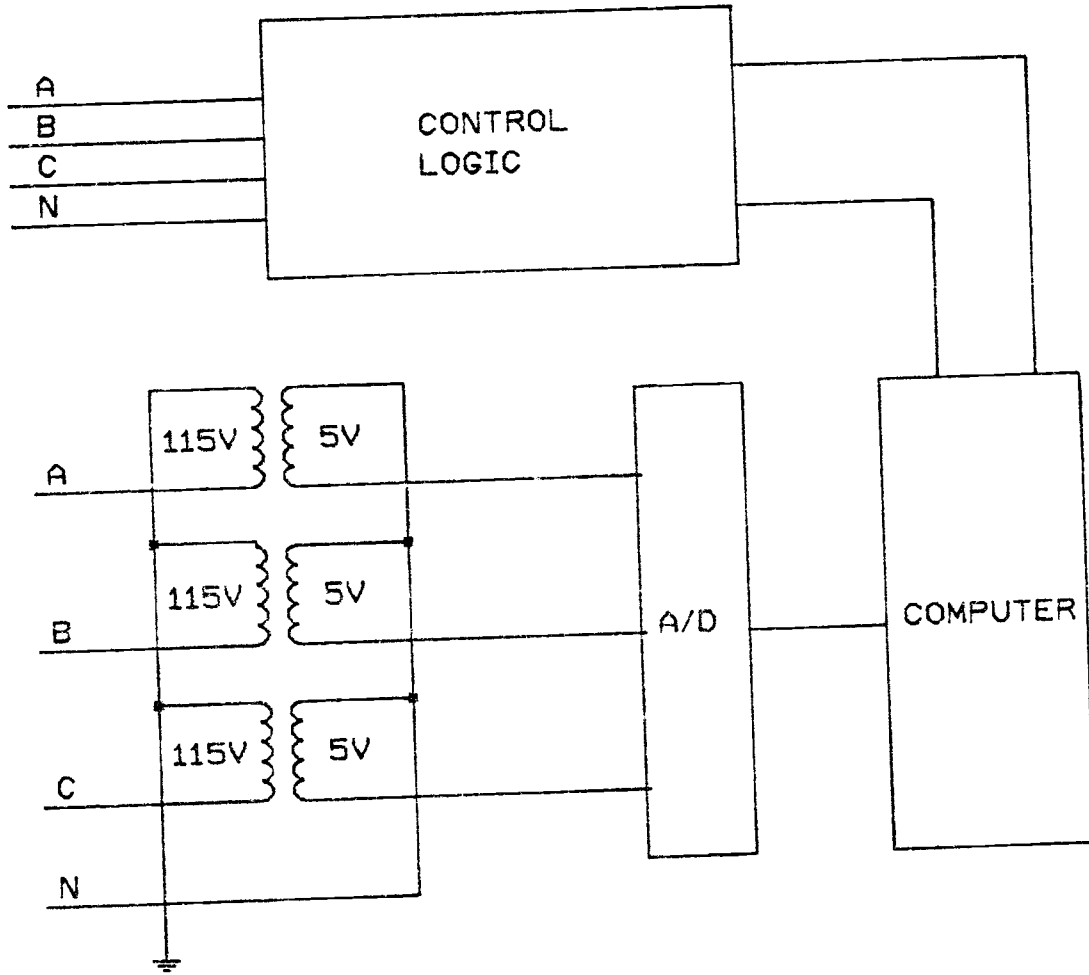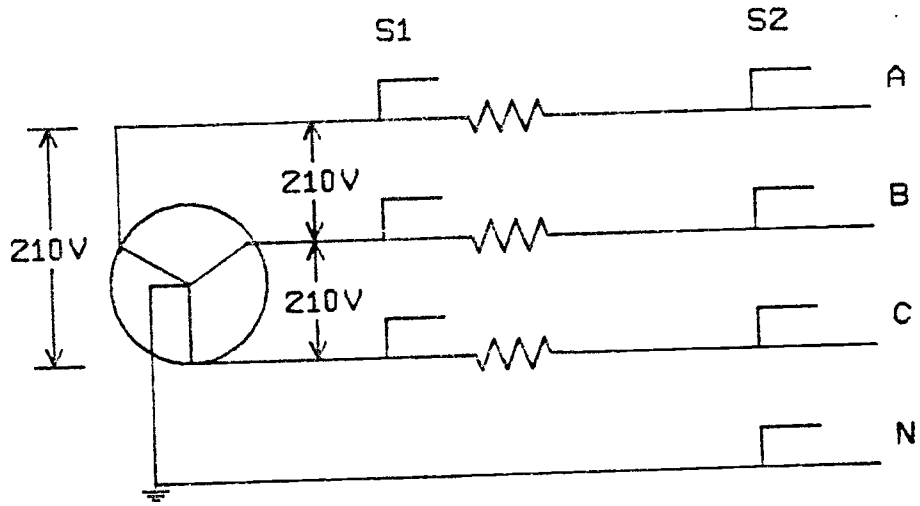
TEST INSTALLATION

FIGURE 10

diagrams in Figure 11. The function of each part of the block diagram is explained below. The complete details of the circuit are given in Figure 12.

  a. Zero-crossing detector - the R. C. A. zero-voltage cross-ing detector (CA3059) was used and found to give accurately synchronized output pulses each time the voltage crosses zero.

  b. Sampling clock - The sampling clock was built by using two schmitt-trigger monostable multivibrators (SN74121). The clock frequency was set at 240 Hz. This gives a pulse at each zero crossing and each peak of the voltage waveform.

The sampling clock is always synchronized with line frequency except when a fault occurs. During the fault, or any other time, if the line frequency changes more than 5% from its last cycle, the clock locks itself to a frequency of 240 Hz.

  c. Reset circuit - The sampling clock is set at 240 Hz, but the line frequency can vary from 58 to 62 Hz ($\pm$ 3.5% from normal frequency of 60 Hz). To minimize error due to this change in frequency, it was found that resetting the sampling clock every two cycles was sufficient.

  d. Frequency change detector - This portion of the circuit detects the change in system frequency from one cycle to
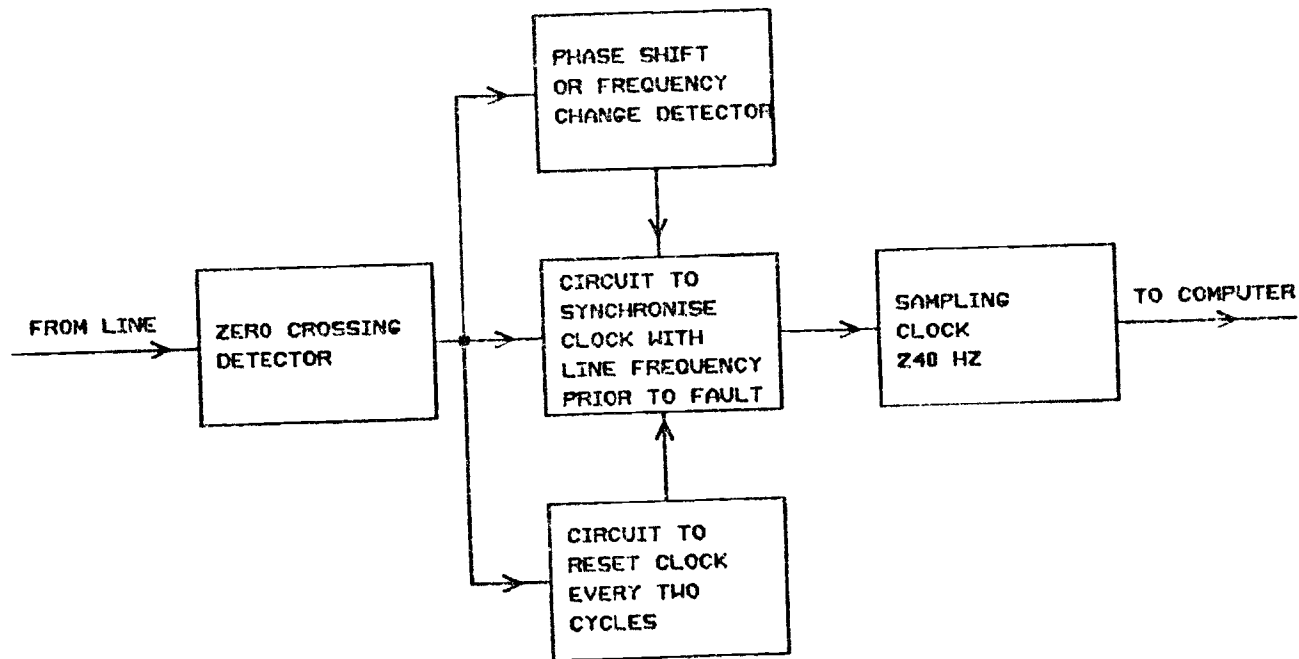
BLOCK DIAGRAM FOR THE SAMPLING CLOCK

FIGURE 11

SAMPLING CLOCK CIRCUIT

FIGURE 12
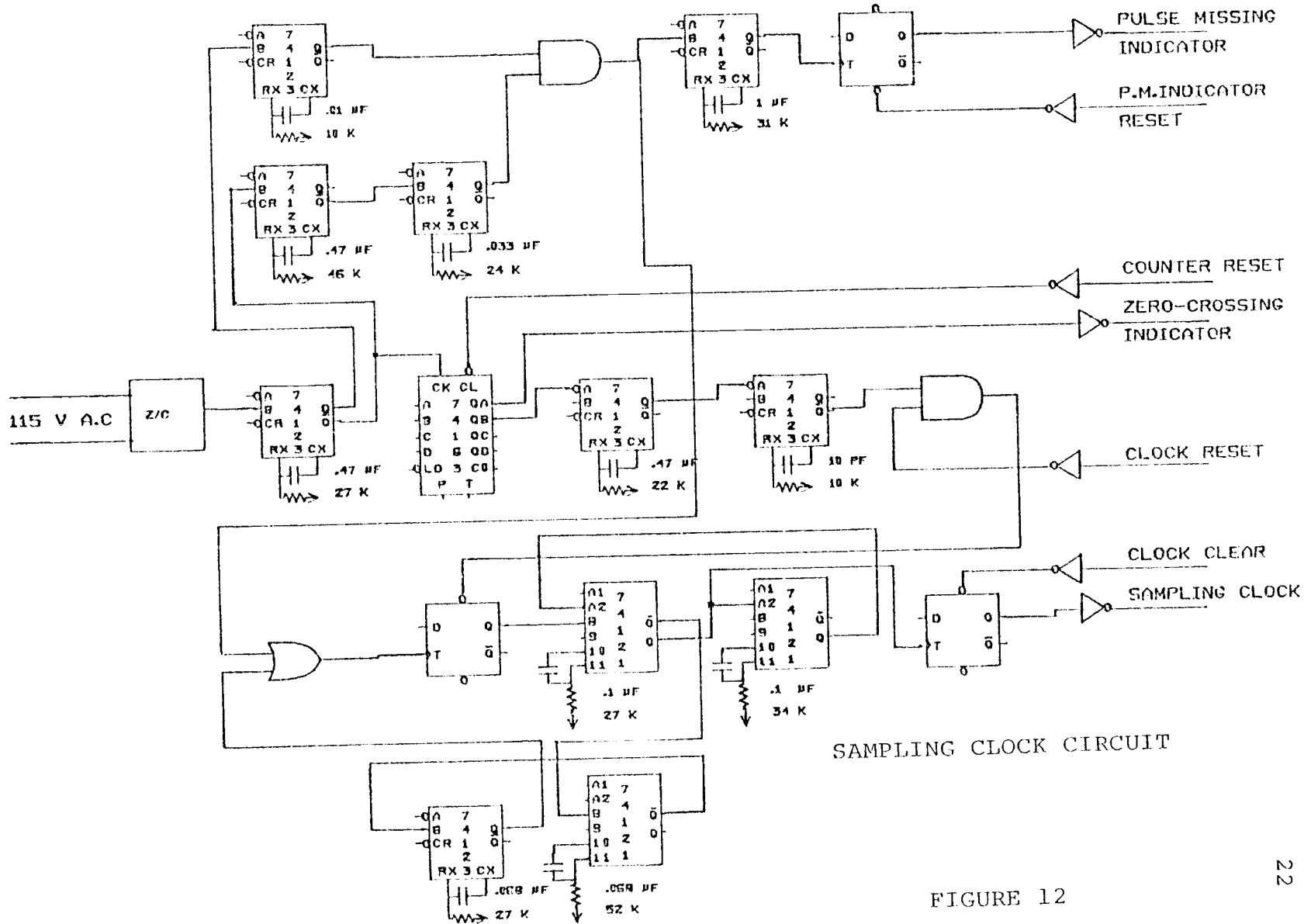
the next. If the time between pulses from the zero-crossing detector does not vary more than 5%, the system frequency is assumed to be within limits. Otherwise, it sends the signal to sampling clock and locks the sampling clock at its original line frequency.

IV. COMPUTER OPERATION

The fault detection program, written in assembly language (SAL960A) for the T1960A computer, is responsible for performing the major logic function of fault detection. It was compiled on a CDC 3300 computer. SAL960A reads a source file of instruction written in the assembly language and outputs an object file of instruction on paper tape for loading. It also outputs a list which includes the source statements and corresponding object words generated by SAL960A, along with error indicators, the location of each instruction and source statement number. The listing of the program is given in Appendix III.

The program has two main parts:

1) Detection program

2) Fault type analysis

Each part is described below.

Detection Program

The detection consists of two parts:

a) initialization and b) fault detection

Initialization

The initialization part of the program initializes all registers

and counters. It clears all flags and sets the limit for the parameters. It finds the phase-sequence of the transmission line voltages and sets the sampling order for the detection portion. The sampling order depends on the phase sequence of the sampled phase voltages.

When the phase relation is abc, the computer will sample lines b, and c when clock 1 issues a pulse and waits for the pulse from number 2 clock. When it receives an interrupt from clock 2, it samples lines a and c and waits for an interrupt from clock 3. When clock 3 issues its pulse, it samples lines a and b. This cycle is repeated. If the sequence is acb, then the computer will sample line voltages when it receives interrupts from the clocks in a sequence 1, 3, 2.

Fault Detection

The fault detection is the only part of the program which is used to monitor the system. The logic of the program is based upon the theory explained in Chapter II.

Figure 13 shows the complete block diagram of the logical steps taken by the computer to detect a fault. Voltage samples are taken only at each zero crossing and peak of the voltage waveforms. The program is initiated from a phase A, which is arbitrarily chosen. Following the interrupt from phase A clock, the computer samples the other phase voltages, V_b and V_c.

INITIALIZE ALL REGISTERS
AND COUNTERS

↓

DETERMINE THE SEQUENCE
OF THE PHASE VOLTAGES
AND SET THE SAMPLING
SEQUENCE

↓

CHECK IF PHASE A CLOCK
IS HIGH
SAMPLE LINE VOLTAGE
VB AND VC

↓

CHECK IF VOLTAGE VA IS
CROSSING ZERO

NO ← → YES

SUBTRACT VB
FROM VC
SET FLAG ZP1 HIGH

ADD VOLTAGES
VB AND VC

↓

STORE THE RESULT R1
CHECK IF FLAG ZP1 IS
HIGH

YES ← → NO

COMPARE THE MAGNITUDE
OF PHASE VOLTAGE VB
AGAINST VALUE VP

COMPARE THE MAGNITUDE
OF PHASE VOLTAGE VB
AGAINST VALUE VZ

(1)

BLOCK DIAGRAM FOR THE FAULT DETECTION

FIGURE 13

1

IS MAGNITUDE WITHIN LIMITS

YES — NO

CHECK IF FLAG F6 IS HIGH

SET FLAG F6 HIGH INCREASE PHASE B FAULT COUNTER (NB) 1

YES — NO

SET FLAG F6 LOW DECREASE PHASE B FAULT COUNTER (NB) 1

CHECK IF NB IS GREATER THAN THREE

NO — YES

FAULT ON LINE JUMP TO SUBROUTINE

CHECK IF FLAG ZP1 IS HIGH

YES — NO

SET FLAG ZP1 LOW COMPARE THE MAGNITUDE OF PHASE VOLTAGE VC AGAINST VP

COMPARE THE MAGNITUDE OF PHASE VOLTAGE VC AGAINST VZ

IS MAGNITUDE WITIN LIMITS

YES — NO

CHECK IF FLAG F7 IS HIGH

SET FLAG F7 HIGH INCREASE PHASE C FAULT COUNTER NC BY 1

YES — NO

SET FLAG F7 LOW DECREASE PHASE C FAULT COUNTER NC BY 1

CHECK IF NC IS GREATER THAN 3

NO — YES

2

FAULT ON LINE. JUMP TO SUBROUTINE FOR FAULT ANALYSIS

BLOCK DIAGRAM FOR THE FAULT DETECTION

BLOCK DIAGRAM FOR THE FAULT DETECTION

The detection program compares the sampled voltage V_b with a specified tolerance limit (V_z or V_p), which depends on V_a being at zero or peak. If the variation is greater than specified tolerance limit, the phase fault counter Nb is increased by one. The counter Nb is decreased by one if the variation is within the limits and Nb is greater than zero. The logic is repeated for the phase voltage V_c.

The detection program also checks the sum of the two voltages V_b and V_c against a specified limit (T_z) if V_a is at a zero crossing or the difference of V_b and V_c against a specified limit (T_p) if V_a is at peak. If the sum or difference lies outside the tolerance limit, the fault counter Nf is incremented. If the sum or difference lies within the limits, Nf is decremented, if it is not already zero.

The above process is repeated for the phase B and C clocks. A fault is indicated if any of the fault counters, Na, Nb, Nc exceeds three or if Nf exceeds two.

The maximum time to detect a fault is about 8 milliseconds after the fault has occurred. It is also seen from the above scheme that the transient or spikes of short duration, less than 3 milliseconds, will not affect the operation.

The values of the variable parameters V_z and V_p depend upon normal operating phase-voltages. The values of the tolerance limits T_z and T_p depend on the sensitivity of the system.

Fault Type Analysis

This is performed by subroutine CLASSFY and was specially written for the case where sampling device was located at the receiving end S2, shown in Figure 10. The subroutine classifies a fault as a line to ground, double line to ground, line to line, or three phase to ground.

CLASSFY program examines the counters Na, Nb, and Nc for each phase looking for the symptoms which indicate which phases are involved in phase to ground fault. A value of greater than 3 indicates phase is involved in ground fault. If none of the counters is greater than 3, the computer samples line voltages a, b, c and classifies the fault as a line to line fault. The phases involved are found by comparing the phase voltages. The two voltages, which are equal in magnitude, are assumed to be involved in the line to line fault. The block diagrams in Figures 14, 15 give the complete details of the procedure.
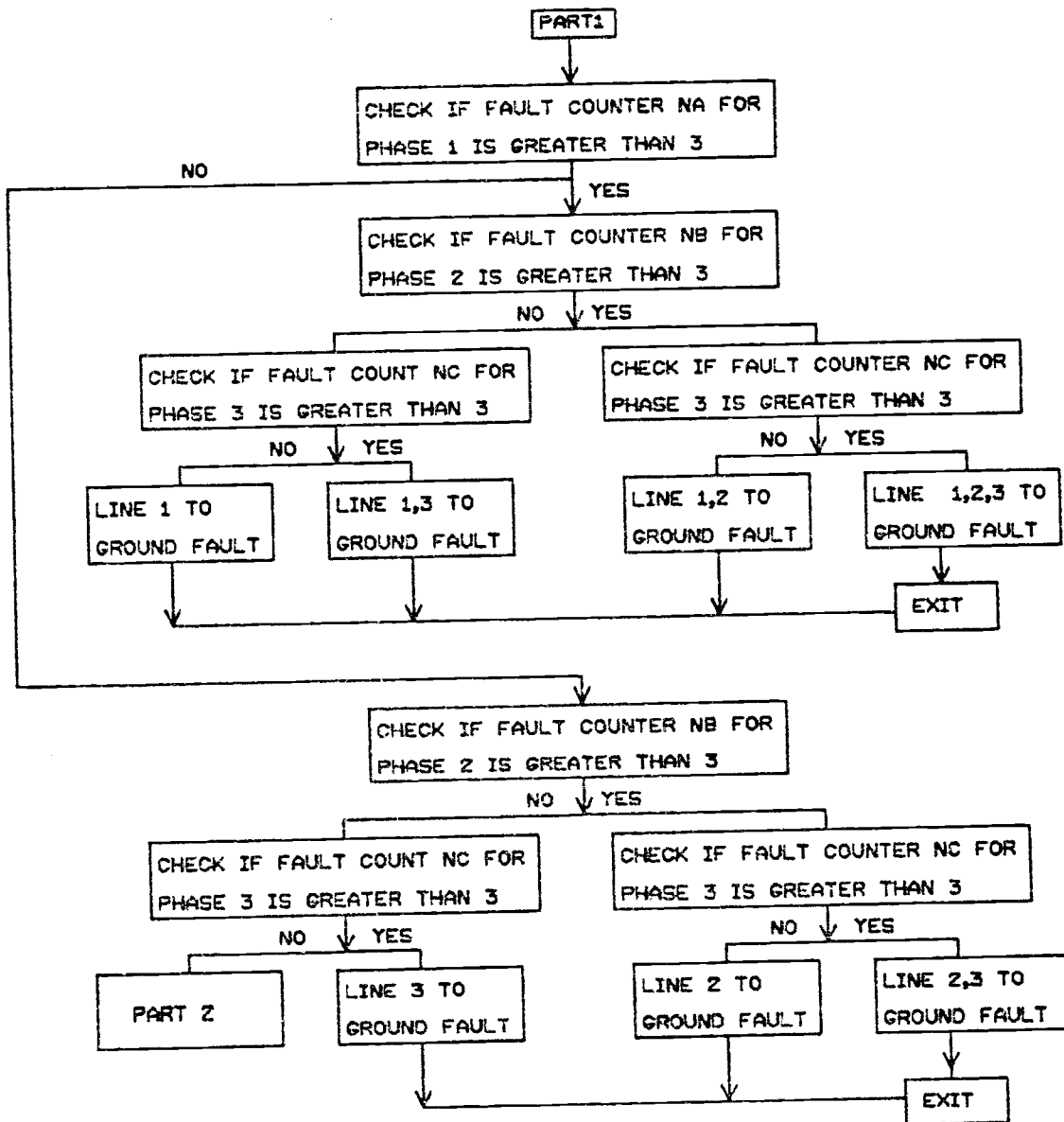
BLOCK DIAGRAM TO FIND LINE TO GROUND FAULTS

FIGURE 14

```
                        ┌─────────────┐
                        │   PART 2    │
                        └──────┬──────┘
                               │
                               ▼
        ┌──────────────────────────────────────────┐
        │ SAMPLE PHASE VOLTAGES VA, VB, VC           │
        │ AT THE POINT WHEN VA IS AT PEAK            │
        └──────────────────────┬─────────────────────┘
                               │
                               ▼
        ┌──────────────────────────────────────────┐
   NO   │ CHECK IF VA, VB ARE EQUAL                  │
  ◄─────┤                                            │
        └──────────────────────┬─────────────────────┘
                               │ YES
                               ▼
        ┌──────────────────────────────────────────┐
        │ LINE 1 TO LINE 2 FAULT                     │
        └──────────────────────┬─────────────────────┘
                               │
                               ▼
                        ┌─────────────┐
                        │    EXIT     │
                        └─────────────┘

        ┌──────────────────────────────────────────┐
   NO   │ CHECK IF VB, VC ARE EQUAL                  │
  ◄─────┤                                            │
        └──────────────────────┬─────────────────────┘
                               │ YES
                               ▼
        ┌──────────────────────────────────────────┐
        │ LINE 2 TO LINE 3 FAULT                     │
        └──────────────────────┬─────────────────────┘
                               │
                               ▼
                        ┌─────────────┐
                        │    EXIT     │
                        └─────────────┘

        ┌──────────────────────────────────────────┐
   NO   │ CHECK IF VC, VA ARE EQUAL                  │
 ┌────┐ │                                            │
 │EXIT├─┤                                            │
 └────┘ └──────────────────────┬─────────────────────┘
                               │ YES
                               ▼
        ┌──────────────────────────────────────────┐
        │ LINE 3 TO LINE 1 FAULT                     │
        └──────────────────────┬─────────────────────┘
                               │
                               ▼
                        ┌─────────────┐
                        │    EXIT     │
                        └─────────────┘
```
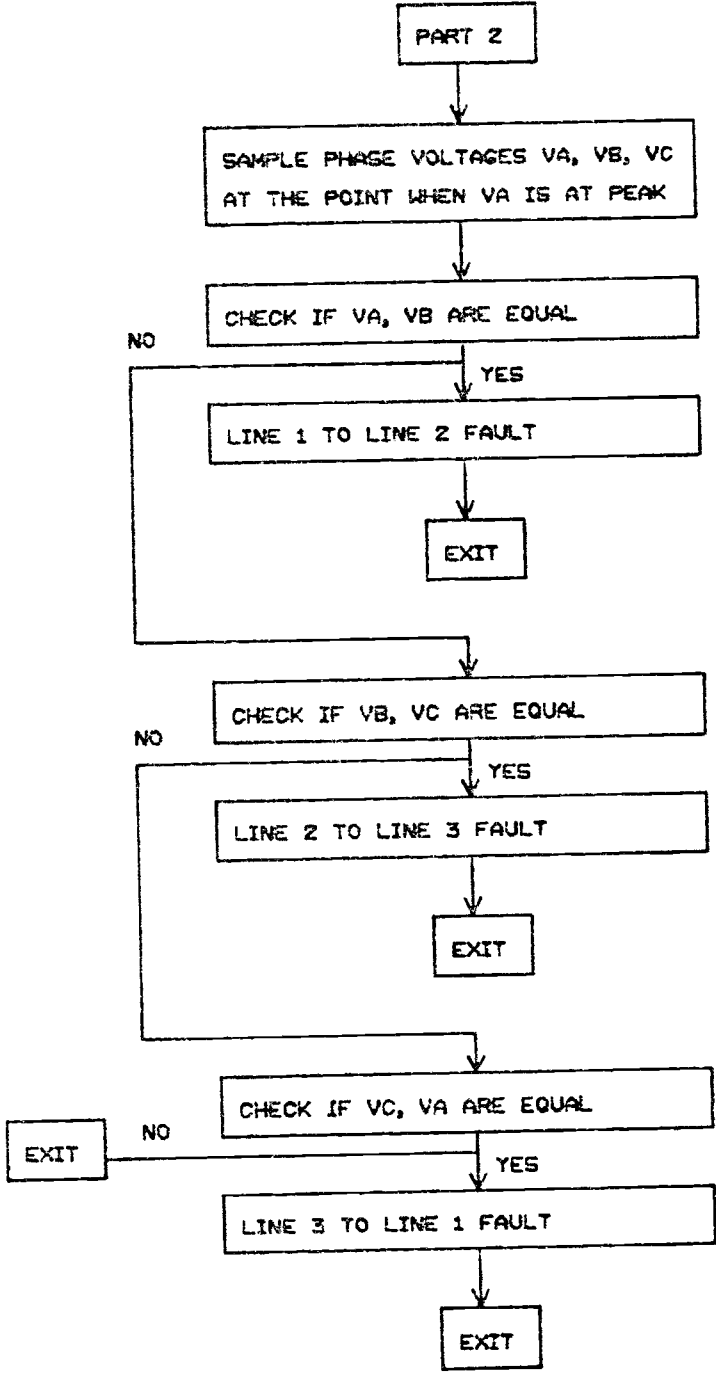
BLOCK DIAGRAM TO FIND LINE TO LINE FAULT

FIGURE 15

V. TESTS

The operation of the detection scheme was tested on line for the following faults in the laboratory: (Figure 16)

a) Line to ground

b) Double line to ground

c) Line to line

d) Three line to ground

Two separate tests were conducted. In the first test run, the voltage samples were taken at point S1, the sending end, and in the second test run, the voltage samples were taken at S2, the receiving end (Figure 10). All faults were created at the receiving end.

The fault detection program was tested for both fault positions. The fault analysis program was tested for the receiving end only.
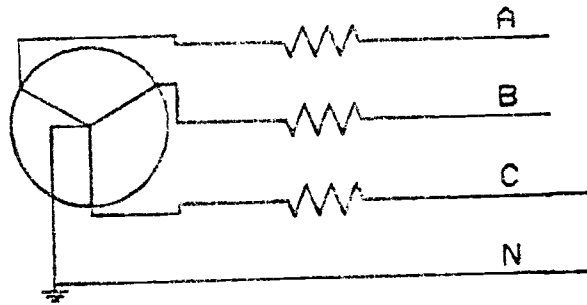
LINE TO GROUND FAULT
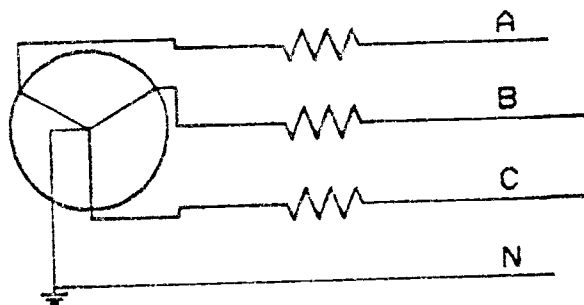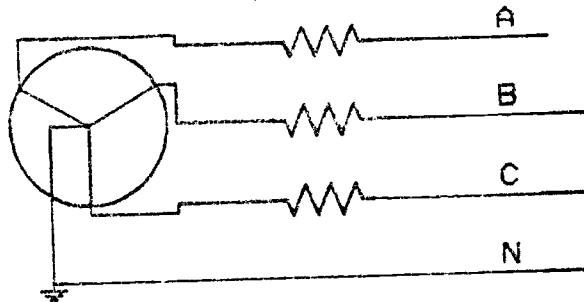
LINE TO LINE FAULT

TWO LINES TO GROUND FAULT
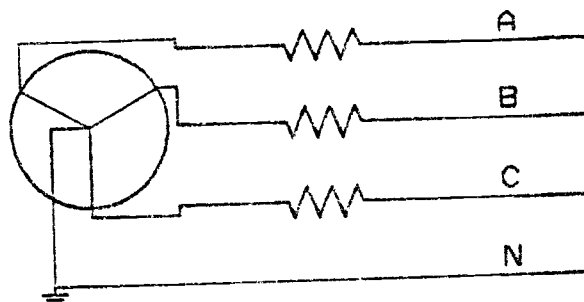
THREE LINE FAULT

FIGURE 16

VI. CONCLUSION

A working Hybrid Fault Detection scheme has been developed for a three phase transmission line using solid state devices and minicomputer. The scheme was found to be reliable in the laboratory under following values of the parameters

$$V_z = V_{za} \pm 10\% \times V_{za}$$

where V_{za} = Running average value of the voltages under normal condition when one of the voltage is crossing zero

$$V_p = V_{pa} \pm 15\% \times V_{pa}$$

where V_{pa} = Running average value of the voltages under normal condition when one of the voltages is at its peak

T_z and T_p were set at 0.5 volts.

For Fault Analysis program V_z and V_p were set at 1 volt.

The above values of the parameters are not fixed. They are dependent upon normal system unbalances and change of the voltage magnitude under fault condition.

The average time between samples is about 1/12 of cycle (1.38 milliseconds on 60 Hz base) and the average time the computer program took between two sampling points was about 350 microseconds (average number of instruction = 70, average instruction execution time = 5 microseconds).

The scheme detects the fault within one-half cycle (8 milliseconds). It was shown that scheme can be used to classify the fault as in test 2. The main advantages of the scheme are:

a. High speed, one-half cycle operation.

b. Simple three phase fault detection.

c. A small amount of information has to be transferred to the computer, thus saving computer time and memory.

d. Transient voltage bursts of less than 3 milliseconds will not affect the operation.

e. Fault data is always compared with prefault data.

VII. FUTURE DEVELOPMENT

At the present time, there has been little development in the use of a computer in system protection in real time. To take advantage of the new solid state technology, the development should be directed towards the use of mini or micro computers at each primary substation. The computer can carry out initial processing of information. The computer should be able to detect the nature and location of an abnormality and initiate any corrective action to be taken locally. The computer should supply information to a central or adjacent local computer when action has to be taken at other locations.

A complete surveillance system by the hybrid computer terminals is required to utilize the advantages of the detection method discussed herein. One isolated installation has little advantage over the present system of "Fault Protection".

The development of a complete and reliable surveillance system will require continued research and development in the following areas:

a) Modify the scheme to sample the phase currents to classify the fault.

b) The establishment of communication between computers or processors. From this information, it will be possible to

locate the fault and initiate the opening of appropriate

circuit breaker to isolate the fault.

c) Improve the scheme to avoid false indication due to long

time-constant switching surges.

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APPENDIX I

1) Line to Ground[*]

The simple power system shown in Figure 17 consists of a generator, transformer, transmission line, load transformer, and load. Consider a SLG fault at bus C with a fault resistance of 4
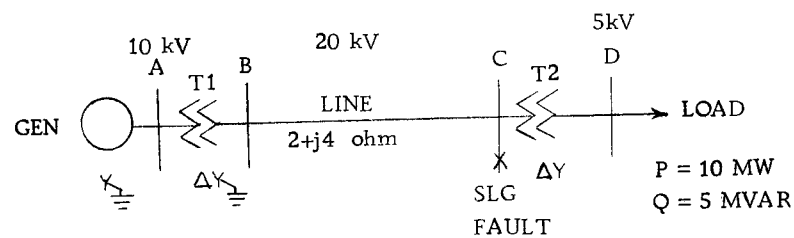
Figure 17. Power system

ohms. The following data concerning the system is known.

Generator: 25 MVA, 10 kV, $x = 0.125$ pu, connected Y-grounded

T1: 30 MVA, 10-20 kV, $x = 0.105$, connected Δ-Y-grounded

Line: $Z = 2 + j4$ Ω

T2: 20 MVA, 5-20 kV, $x = 0.05$ pu, connected Y-Δ

Load: static (constant z) load of $10 + j5$ MVA at 5 kV

Solution

Select $S_B = 20$ MVA, a load voltage of 5 kV, and compute all system impedances.

---

[*] Data taken from Analysis of Faulted Power Systems by Paul M. Anderson, The Iowa State University Press, Ames, Iowa, 1973.

Generator: $x = (0.125)(20/25) = 0.10$ pu

T1: $x = (0.105)(20/30) = 0.07$ pu

Line: $z = [(2 + 4j)(20)]/(20)^2 = 0.1 + j0.2$ pu

T2: $x = 0.05$ pu

Load (as series impedance):

$$R = \frac{(V)^2(S_B)P}{P^2 + Q^2}$$

$$= \frac{(1.0)^2(20 \times 10^6)(10 \times 10^6)}{(10 \times 10^6)^2 + (5 \times 10^6)^2} = \frac{200}{125} = 1.6 \text{ pu}$$

Similarly, $x = 100/125 = 0.8$ pu. Then the positive sequence network for a SLG fault at bus C is represented as shown in Figure 18.
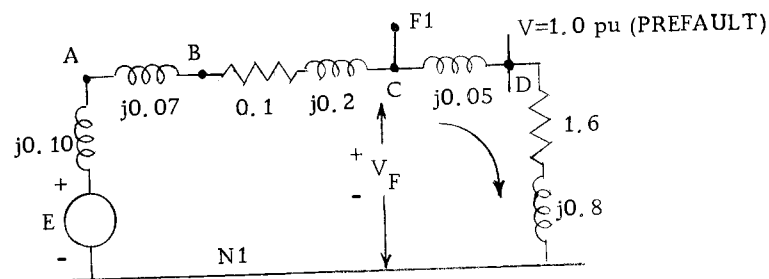
Figure 18. One-line diagram of the positive sequence network.

The load current I_L is (with V as the reference phasor)

$$I_L = \frac{P - jQ}{V*} = \frac{10 - j5}{20} = 0.5 - j0.25 \text{ pu}$$

The Thevenin voltage at bus C is

$$V_F = 1.0 + j0 + (0.5 - j0.25)(j0.05)$$

$$= 1.0125 + j0.025 = 1.0125\underline{/1.27°}\ \text{pu}$$

We set $V_F = 1.0125\underline{/0°}$ and it becomes the reference phasor in the fault calculations. The impedance seen looking in at F1 with E shorted is $0.1 + j0.37$ on the left in parallel with $1.6 + j0.85$ on the right, or

$$Z_1 = \frac{(0.1 + j0.37)(1.6 + j0.85)}{1.7 + j1.22} = 0.332\underline{/67.3°} = 0.128 + j0.307\ \text{pu}$$

This is the impedance to the flow of both positive and negative sequence currents.

The zero sequence current sees an open circuit to the left of bus A, with A grounded (because of the Y-grounded connection) and an open circuit to the right of bus C. Thus Z_0 is the sum of the line and T1 impedances, or $Z_0 = 0.1 + j0.27$ pu.
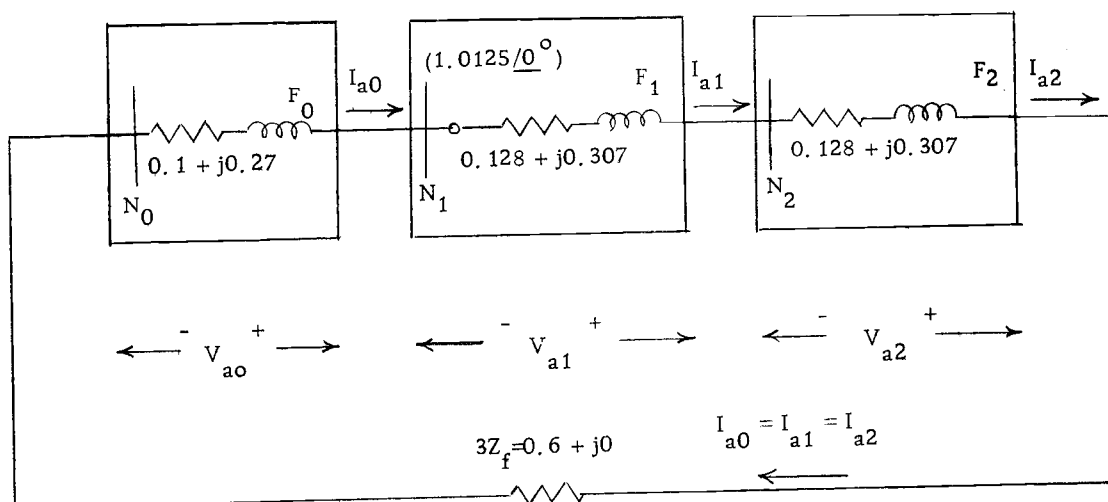
Figure 19. Sequence networks for SLG fault at bus C.

The complete connection of sequence networks is shown in Figure 19, where Z_f is shown to be

$$Z_f = \frac{4 + j0}{Z_B} = \frac{4}{20} = 0.2 \text{ pu}$$

The total circuit impedance is

$$Z_t = Z_0 + Z_1 + Z_2 + 3Z_f = 0.956 + j0.884 = 1.3 \underline{/42.8°} \text{ pu}$$

$$I_{a1} = \frac{V_F}{Z_t}$$

$$I_{a1} = \frac{1.0125 \underline{/0°}}{1.3 \underline{/42.8°}} = 0.78 \underline{/-42.8°} = 0.572 - j0.530 \text{ pu}$$

Then $I_a = 3I_{a1} = 2.34 \underline{/-42.8°}$ pu.

We may synthesize the phase voltages by first computing the sequence voltages.

$$V_{a0} = -Z_0 I_{a0} = -(0.288 \underline{/69.7°})(0.78 \underline{/-42.8°})$$

$$= -0.225 \underline{/26.9°} = -0.200 - j0.102 \text{ pu}$$

$$V_{a1} = V_F - Z_1 I_{a1} = (1.0125 + j0) - (0.332 \underline{/67.3°})(0.78 \underline{/-42.8°})$$

$$= (1.0125 + j0) - (0.236 + j0.1075) = 0.7765 - j0.1075$$

$$V_{a2} = -Z_2 I_{a2} = -0.236 - j0.1075$$

Thus

$$V_a = V_{a0} + V_{a1} + V_{a2} = 0.3405 - j0.3170 = 0.466 \underline{/-42.9°} \text{ pu}$$

$$V_b = V_{a0} + a^2 V_{a1} + a V_{a2}$$

$$= -0.200 - j0.102 - 0.4826 - j0.6212 + 0.2111 - j0.1512$$

$$= -0.4715 - j0.874 = 0.994\underline{/-118.3°} \text{ pu}$$

$$V_c = V_{a0} + aV_{a1} + a^2 F_{a2}$$

$$= -0.200 - j0.102 - 0.2964 + j0.7288 + 0.0249 + j0.2588$$

$$= -0.4715 + j0.8856 = 0.994\underline{/118.3°} \text{ pu}$$

Therefore, instantaneous phase voltages are:

$$V_a = .466 \cos(\omega t - 42.9°)$$

$$V_b = .994 \cos(\omega t - 118.3°)$$

$$V_c = .994 \cos(\omega t + 118.3°)$$

2) Double line to ground fault

Refer again to the system in Figure 17, this time with a 2LG fault and with fault impedances of Z_f = 4 ohms and Z_g = 8 ohms. The fault is at bus C, so the sequence networks are internally the same as those of Figure 19.

Solution

The pu impedances are

$$Z_0 = 0.1 + j0.27, \qquad Z_1 = Z_2 = 0.128 + j0.307$$

$$Z_f = 0.2 + j0, \qquad Z_g = 0.4 + j0$$

As before, V_F = 1.0125 + j0 pu. The network to be solved appears schematically as shown in Figure 20.

The total impedance seen by current I_{a1} is

$$Z_t = 0.328 + j0.307 + \frac{(0.328 + j0.307)(1.5 + j0.27)}{1.828 + j0.577}$$

$$= 0.617 + j0.515 = 0.805\underline{/39.8°} \text{ pu}$$

Then I_{a1} is

$$I_{a1} = \frac{1.0125\underline{/0°}}{0.805\underline{/39.8°}} = 1.259\underline{/-39.8°} = 0.965 - j0.805 \text{ pu}$$
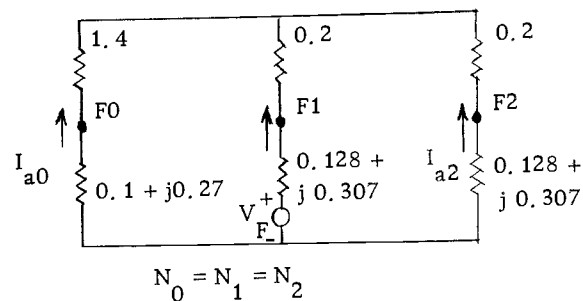
Figure 20. A 2LG fault network.

By inspection of Figure 20 we compute

$$I_{a0} = -\frac{Z_2 + Z_f}{Z_2 + Z_0 + 2Z_f + 3Z_g} I_{a1}$$

$$= \frac{0.449\underline{/43.1°}}{1.92\underline{/17.5°}} (1.259\underline{/-39.8°}) = -0.294\underline{/-14.2°}$$

$$= -(0.285 - j0.072) \text{ pu}$$

Similarly,

$$I_{a2} = -\frac{Z_0 + Z_f + 3Z_g}{Z_2 + Z_0 + 2Z_f + 3Z_g} I_{a1} = -\frac{1.525\underline{/10.2°}}{1.92\underline{/17.5°}} (1.259\underline{/-39.8°})$$

$$= -1.00\underline{/-47.1°} = -(0.68 - j0.732) \text{ pu}$$

Checking these results, we compute $I_a = I_{a0} + I_{a2} = 0 - j0.001 = 0$.

Synthesizing the other phase currents, we have

$$I_b = I_{a0} + a^2 I_{a1} + a I_{a2}$$

$$= -0.285 + j0.072 - 1.181 - j0.432 - 0.293 - j0.955$$

$$= -1.759 - j1.315 = -2.195\underline{/36.8°} \text{ pu}$$

and

$$I_c = I_{a0} + a I_{a1} + a^2 I_{a2}$$

$$= -0.285 + j0.072 + 0.215 + j1.24 + 0.977 + j0.210$$

$$= 0.907 + j1.522 = 1.774\underline{/59.2°} \text{ pu}$$

The sequence voltages are

$$V_{a0} = -Z_0 I_{a0} = -(0.1 + j0.27)(-0.285 + j0.072)$$

$$= 0.048 + j0.07 \text{ pu}$$

$$V_{a1} = V_F - Z_1 I_{a1} = 1.0125 - (0.128 + j0.307)(0.965 - j0.805)$$

$$= 1.0125 - (0.370 + j0.193) = 0.6425 - j0.193 \text{ pu}$$

$$V_{a2} = -Z_2 I_{a2} = -(0.128 + j0.307)(-0.68 - j0.732)$$

$$= 0.311 + j0.115 \text{ pu}$$

The phase voltages are

$$V_a = V_{a0} + V_{a1} + V_{a2} = 1.001 - j0.008 \text{ pu} \quad 1.001\underline{/0} \text{ pu}$$

$$V_b = V_{a0} + a^2 V_{a1} + a V_{a2}$$

$$= 0.0479 + j0.07 - 0.488 - j0.4595 - 0.2552 + j0.212$$

$$= -0.6953 - j0.1775 = -0.717\underline{/-165.7°} \text{ pu}$$

$$V_c = V_{a0} + aV_{a1} + a^2V_{a2}$$

$$= 0.0497 + j0.07 - 0.154 + j0.6525 - 0.0558 - j0.3270$$

$$= -0.1619 + j0.2555 = -0.303\underline{/122.4°}\ pu$$

Therefore, instantaneous phase voltages are:

$$V_a = 1.001 \cos(\omega t)$$

$$V_b = .717 \cos(\omega t - 165.7°)$$

$$V_c = .303 \cos(\omega t + 122.4°)$$

3) Line to line fault

Compute the phase voltages and currents for a LL fault at bus C of Figure 17 where a fault impedance of 4 ohms is assumed between phases b and c.

Solution

The sequence networks are exactly as shown in Figure 19, but their interconnection is that of Figure 21. With the new connection the total impedance is

$$Z_t = Z_1 + Z_2 + Z_f = 0.456 + j0.614 = 0.765\underline{/53.4°}\ pu$$

Then

$$I_{a1} = I_{a2} = V_F / Z_t = \frac{1.0125\underline{/0°}}{0.765\underline{/53.4°}}$$

$$= 1.325\underline{/-53.4°} = 0.788 - j1.065\ pu$$

$$I_b = -I_c = -j\sqrt{3}I_{a1} = -1.86 - j1.38 = -2.32\underline{/36.6°}\ pu = 1320\ A$$

This sytem voltages may also be synthesized from a knowledge of

the sequence currents and sequence network connections.

$$V_{a1} = V_F - Z_1 I_{a1} = 1.0125 - (0.332\underline{/67.3°})(1.325\underline{/-53.4°})$$

$$= 1.0125 - 0.427 - j0.1055 = 0.5855 - j0.1055 \text{ pu}$$

$$V_{a2} = -Z_2 I_{a2} = -(0.332\underline{/67.3°})(-1.325\underline{/-53.4°})$$

$$= 0.44\underline{/13.9°} = 0.427 + j0.1055 \text{ pu}$$

and we compute

$$V_a = V_{a1} + V_{a2} = 1.0125 + j0 = 1.0125\underline{/0}$$

$$V_b = a^2 V_{a1} + a V_{a2} = -0.389 - j0.448 - 0.310 + j0.317$$

$$= -0.699 - j0.131 = 0.705\underline{/-168.4°}$$

$$V_c = a V_{a1} + a^2 V_{a2} = -0.196 + j0.554 - 0.118 - j0.423$$

$$= -0.314 + j0.131 = 0.342\underline{/157.4°}$$
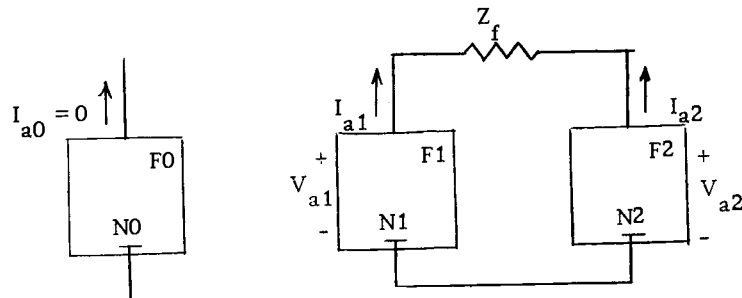
Figure 21. Sequence network connection for a LL fault

Therefore, instantaneous phase voltages are:

$$V_a = 1.012 \cos(\omega t)$$

$$V_b = .705 \cos(\omega t - 168.4°)$$

$$V_c = .342 \cos(\omega t + 157.4°)$$

4) Three phase to ground fault

A three phase fault with fault impedance of 4 ohms (Z_f = 4 ohm)

at bus C of Figure 17.

<u>Solution</u>

The pu fault impedance is $Z_f = 4/Z_B = 4/20 = 0.2$ pu. Thus

$$I_{al} = I_a = \frac{V_F}{Z_1 + Z_f} = \frac{1.0125 + j0}{0.328 + j0.307}$$

or

$$I_{al} = \frac{1.0125 \underline{/0°}}{0.449 \underline{/43.1°}} = 2.255 \underline{/-43.1°} = 1.647 - j1.54 \text{ pu}$$

The voltage at the fault is

$$V_a = V_{al} = Z_f I_{al} = (0.2)(1.647 - j1.54) = 0.329 - j0.308$$

$$= 0.451 \underline{/-43.1°} \text{ pu}$$

Currents and voltages in phases b and c are found by applying phase

rotations of -120° and +120° respectively to the above results.

Therefore instantaneous phase voltages are:

$$V_a = 0.451 \cos(\omega t - 43.1°)$$

$$V_b = 0.451 \cos(\omega t - 163.1°)$$

$$V_c = 0.451 \cos(\omega t + 76.1°)$$

The magnitude of the phase voltages under various fault

conditions at the prefault zero crossing and peak of the voltage

vb waveform.

Case 1

Phase voltages at prefault zero crossing of the voltage V_b which occurs at $\omega t = 30°$

a) Line to ground fault

$V_a = 0.466 \cos(\omega t - 42.8°) = 0.456$ pu

$V_b = 0.994 \cos(\omega t - 118.3°) = 0.0289$ pu

$V_c = 0.994 \cos(\omega t + 118.3°) = -0.846$ pu

b) Double line to ground fault

$V_a = 1.001 \cos(\omega t) = 0.866$ pu

$V_b = 0.717 \cos(\omega t - 165.7°) = -0.5136$ pu

$V_c = 0.303 \cos(\omega t + 122.4°) = -0.268$ pu

c) Line to line fault

$V_a = 1.012 \cos(\omega t) = 0.866$ pu

$V_b = 0.705 \cos(\omega t - 168.4°) = -0.524$ pu

$V_c = 0.342 \cos(\omega t + 157.4°) = -0.339$ pu

d) Three phase to ground fault

$V_a = 0.451 \cos(\omega t - 43.1°) = 0.439$ pu

$V_b = 0.451 \cos(\omega t - 163.1°) = -0.308$ pu

$V_c = 0.451 \cos(\omega t + 76.1°) = -0.131$ pu

Case 2

Phase voltages at the prefault peak of the voltage V_b which occurs at $\omega t = 120°$

a) Line to ground fault

$$V_a = 0.466 \cos(\omega t - 42.8°) = 0.103 \text{ pu}$$

$$V_b = 0.994 \cos(\omega t - 118.3°) = 0.993 \text{ pu}$$

$$V_c = 0.994 \cos(\omega t + 118.3°) = -0.52 \text{ pu}$$

b) Double line to ground fault

$$V_a = 1.001 \cos(\omega t) = -0.5 \text{ pu}$$

$$V_b = 0.717 \cos(\omega t - 165.7°) = 0.5 \text{ pu}$$

$$V_c = 0.303 \cos(\omega t + 122.4°) = -0.139 \text{ pu}$$

c) Line to line fault

$$V_a = 1.012 \cos(\omega t) = -0.5 \text{ pu}$$

$$V_b = 0.705 \cos(\omega t - 168.4°) = 0.467 \text{ pu}$$

$$V_c = 0.342 \cos(\omega t + 157.4°) = 0.042 \text{ pu}$$

d) Three phase to ground fault

$$V_a = 0.451 \cos(\omega t - 43.1°) = 0.1019 \text{ pu}$$

$$V_b = 0.451 \cos(\omega t - 163.1°) = 0.329 \text{ pu}$$

$$V_c = 0.451 \cos(\omega t + 76.1°) = -0.431 \text{ pu}$$

APPENDIX II

COMPUTER CHARACTERISTICS

The computer block diagram (Figure 22) shows the basic internal function relationships of the 960A computer.

a) The standard semiconductor (MOS) memory of the 960A has a storage capacity ranging from 4096 to 65,536 words. Space is provided within the 960A enclosure for 32,768 words of semiconductor memory.

NOTE

The maximum storage capacity of the 960A computer is 65,536 words. This storage may optionally be externally mounted core memory which is available in 4096 word increments.

b) The Central Processing Unit (CPU) can address the memory, perform arithmetic and logic functions, and sequence and control the exchange of information between memory and other elements of the computer. The CPU features an arithmetic unit and a read-only memory controller.

c) The Communication Register Unit (CRU) controls the exchange of information between the computer and external equipment.

d) The Direct Memory Access Channel (DMAC) interfaces the computer with high-speed automatic computer peripherals,

such as disc storage units, line printers, and magnetic tape units. By using a separate controller for each device, concurrent operation of high speed peripherals is achieved.

Specificiations

a) Organization

Parallel Operation

Single and double address logic

Direct addressing of entire memory

Indirect addressing with pre-indexing or post indexing

32 bit instruction word

16 bit data word

16 active hardware registers (16-bit) for arithmetic, index, or mask operations, and base addressing

Supervisor and worker execution mode architecture

Memory protect feature for variable amounts of memory

Three levels of priority interrupts

b) Performance

4 MHz system clock rate

500 nanosecond memory store sequence

750 nanosecond memory fetch sequence

500 nanosecond memory access time

Hardware multiply/divide option

Execution times:

Load: 3.3 microseconds

Store: 3.6 microseconds

Add: 3.6 microseconds

Set CRU bit: 2.8 croseconds

Load register in CRU: 4.2 - 8.2 microseconds

(1-16 bits)

c) Memory

Semiconductor memory using 1024 X 1-bit dynamic MOS

arrays

Internal storage for up to 32,768 words of MOS memory in

increments of 1024 words

Power failure protection

Magnetic core memory interface option

Minimum storage capacity, 4096 words

Maximum storage capacity, 65,536 words

d) Input/Output System

Direct Memory Access Channel (expandable to 8) with 16-bit

parallel transfer, 1 million words per second burst rate,

and parity checking interface

Communications Register Unit with up to 4096 I/O points

and 4 million bits per second burst rate
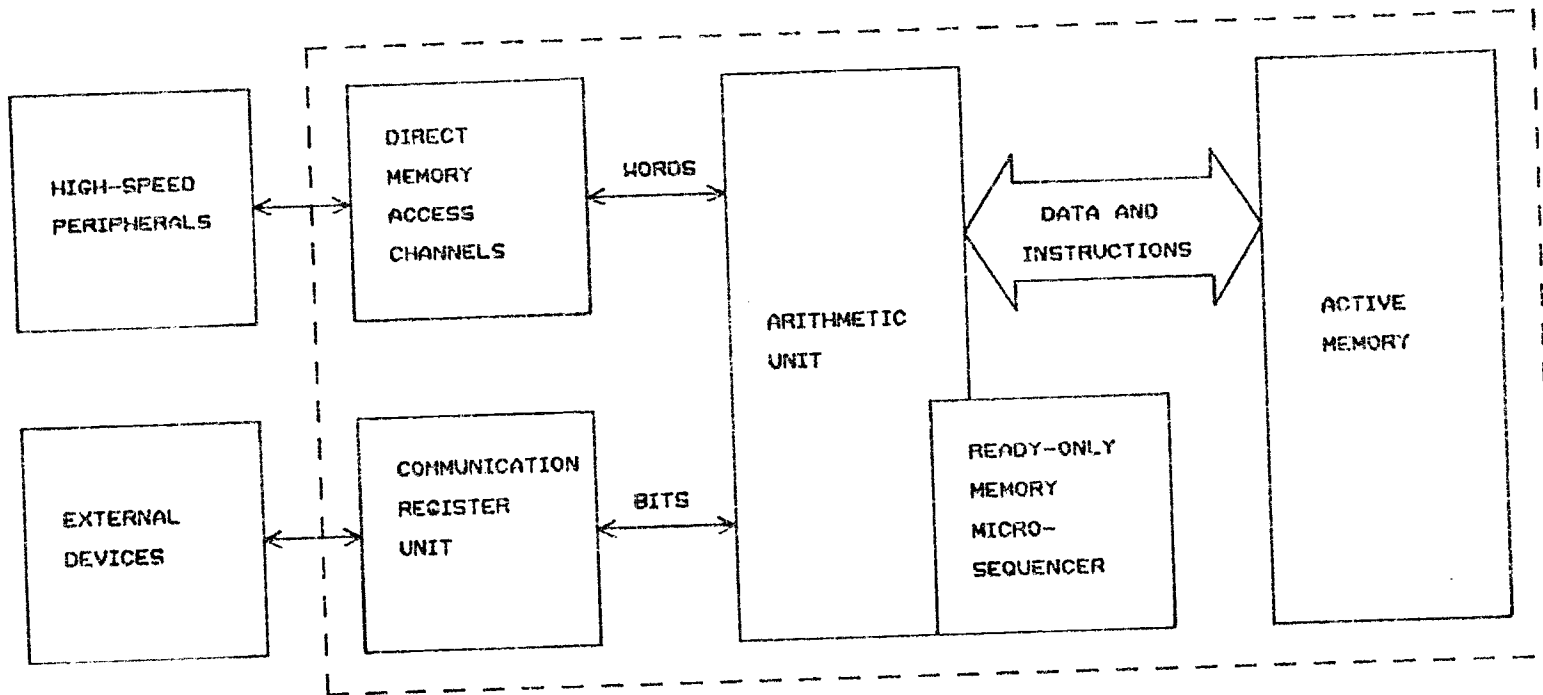
TI 960A COMPUTER BLOCK DIAGRAM

FIGURE 22

e) Instruction Set - 78 instructions

    9-bit and field manipulating instructions

    36 register-memory instructions

    5 powerful memory-memory instructions

    28 flexible program control instructions

f) Physical Characteristics

    Dimension (rank mount configuration)

        Height - 12.25 inches

        Width - 19 inches

        Depth - 24 inches

        Weight - 75 pounds

    Power Requirements: 115V ± 10%, 47-63 Hz

    Power Consumption: 420 watts, average

g) Operating conditions:

    Temperature (@ sea level)

        0° C to 50° C

        32° F to 122° F

    Humidity 10% - 95%

    Altitude 0-10 000 feet

APPENDIX III

```
*        PROGRAM TO FIND FAULT ON 3 PHASE POWER SYSTEM
*        PROGRAM NO 1
*        MAIN PROGRAM NO1
         PSEG
*        SET REGISTERS                      LOCATION FOR UPPER LOWER LIMITS
         LA      0,X#0300#                  NO OF ERROR MESSAGES
         LA      2,X#03F6#                  LOCATION FOR ERROR MESSAGES
         LA      3,X#06C0#                  BASE OF MACHINE DATA
         LA      4,X#0A00#                  BASE OF MACHINE PROCEDURE
         LA      5,X#00B0#                  BASE OF SOFTWARE FLEGS
         LA      6,X#0400#                  BASE OF CRU ADDRESS
         LA      7,X#0540#
*        INITIALIZATION
         LA      1,X#3000#
         ST      1,LOC3
         ST      1,LOC31
         LA      1,X#3400#
         ST      1,LOCS
         ST      1,LOCS1
         ST      1,LOC32A
         ST      1,LOC33A
         ST      1,LOC33B
         LA      1,X#0000#
         ST      1,X#0A00#
         ST      1,X#0A05#
         ST      1,X#0A06#
         ST      1,X#0A07#
         ST      1,X#0A08#
         LA      1,X#0C07#
         ST      1,X#0A09#
         LA      1,X#0000#
         ST      1,X#0A0A#
         LA      1,X#0107#
         ST      1,X#0A08#
         ST      1,X#010F#
         ST      1,X#0A00#
         ST      1,X#0001#
         LA      1,X#0A00#
         ST      1,X#0007#
         LA      1,X#0A0E#
         ST      1,X#0005#
         LA      1,X#0A0F#
         ST      1,X#0003#
         ST      1,X#0A14#
         LA      1,X#0000#
         ST      1,X#0A1C#
         ST      1,X#0A11#
         ST      1,X#0A12#
         LDCR    (X#40#,12),9               CLEAR   CLOCKS
         LDCR    (X#40#,3),10               INPUTS
         LDCR    (X#40#,3),11
         SBETB   X#40#,1
         SBO     X#40#,1
         SBZNE   X#36#,0,8                  SET COUNTER 1 LOW TO COUNT
         SBO     X#43#,1                    CHECK IF 0A1 IS HIGH
         SBZNE   X#36#,1,S                  START CLOCK 1
         SBO     X#4E#,1                    CHECK IF CLOCK 1 IS HIGH
         SBZNE   X#36#,1,9                  START CLOCK 2 AND 3 STOP CLOCK
         LDCR    (X#40#,3),12
         THIS PORTION DETECTS SEQUENCE OF LINES
LOOP3    SBZNE   X#31#,1,LOOP2              CHECK IF CLOCK 2 IS HIGH
         SBZ     LOOP4
LOOP2    SBZNE   X#32#,1,LOOP3             CHECK IF CLOCK 3 IS HIGH
         SETF    SEQF,1
         AMI     LOC3,X#0031#
         AMI     LOCS,X#0004#
         AMI     LOC32A,X#0041#
         AMI     LOC32B,X#0041#           CHANGE ADDRESSES  FOR SEQ
         AMI     LOC33A,X#0042#
         AMI     LOC33B,X#0042#
         AMI     LOC31,X#0132#
         AMI     LOCS1,X#0002#
         SBO     LOC65
LOOP4    AMI     LOC3,X#0032#
```

Computer Program for the Fault Detection

```
            AMT        LOOS,X#1102#
            AMT        LOOO32A,X#0042#
            AMT        LOOO32B,X#0042#
            AMT        LOOO31A,X#0041#
            AMT        LOOO31B,X#0041#
            AMT        LOOOB1,X#1042#
            AMT        LOOO3,X#0042#
LOOPS       BBNE       X#36#,0,5          CHECK IF OA1 IS LOW
            SETB       X#40#,0            CLEAR OUTPUT OF CLOCK 1
            SETB       X#40#,1
            SETB       X#43#,1            SET COUNTER 1 TO COUNT
            BBNE       X#36#,1,5          CHECK IF OA1 IS HIGH
            SETB       X#46#,1            SET CLOCK 1 TO START
            SETB       X#49#,1            CLEAR MISSING PULSE F/FS
            SETB       X#49#,0
            SETB       X#49#,1
            *
            MAIN PROGRAM
M1          BBNE       R4,1,OK1
            AA         2,1
            SETF       R4,0
OK1         BBNE       X#30#,1,8          CHECK IF CLOCK 1 IS HIGH
            SETB       2,1                START CONVERSION ON CHANNEL 2
            BBNE       2,1,5              WAIT
            STOR       (4,12),0006        GET CONVERTED VALUE
            MLA        4,X#1A05#          START CONVERSION ON CHANNEL 3
            SETB       4,1
            BBNE       0,1,5
            STOR       (4,12),0007
            MLA        4,X#0A07#          CLEAR CLOCK 2 OR 3
LOOO32A     SETB       X#0040#,0
            NOP
LOOO32B     SETB       X#0040#,1
            L          1,X#1A05#
            BFNE       (6,0),1,P11
            BFNE       (7,0),1,P13
            B          2,2
P11         BFNE       (7,0),1,P12
P13         L          1,X#0A07#
            SETF       R01,1
            B          J11
P12         L          1,X#0A07#
J11         L          1,X#0A08#
            BFNE       R01,1,ZPN1
            CML        (6,4),(2,0)
            B          GF1
            B          GF1
            BK1
ZPN1        CML        (6,4),(6,0)        CHECK LINE 2 FOR GND FAULT
            B          GF1
            B          GF1
PK1         SETF       R6,1
            AMT        (X#0011#,6),1
            CM         (X#11#,4),(X#5#,4)
            B          GO1
            B          PART1
GF1         BFNE       R6,1,GO1
            AMT        (X#0011#,6),-1
            SETF       R6,0
GO1         BFNE       ZP1,1,ZPN2
            SETF       ZP1,0
            CML        (7,4),(2,0)
            B          GF2
            B          GF2
            BK2
ZPN2        CML        (7,4),(6,0)        CHECK IF LINE 3 IS GROUND
            B          GF2
            B          GF2
PK2         SETF       R7,1
            AMT        (X#0112#,6),1
            CM         (X#12#,4),(X#5#,4)
            B          CMP1
            B          PART1
GF2         BFNE       R7,1,CMP1
```

Computer Program for the Fault Detection

```
              AMT        (X≠0112≠,6),-1
              SETF       F7,0
   CMP1       CML        (0003,4),(0,0)
              B          OSTL1
              B          OSTL1
                         42
   OSTL1      SETF       F4,1
              ASB        -1,OK2,2
              B          PART1
   M2         BFNE       F4,1,OK2
              AA         2,1
              SETF       F4,0
   OK2        NOP
   LOO8       BFNE       X≠30≠,1,8          START CONVERSION ON CHANNEL 1
              SET8       1,1
              B8NE       0,1,8
              STCR       (4,12),0015
              MLA        4,X≠0A05≠
   LOOS       SET8       3,1              START CONVERSION ON CHANNEL 3 OR 2
              B8NE       -,1,1
              STCR       (4,12),0007
              MLA        4,X≠0A07≠
   LOO87A     SET8       X≠00+0≠,0          CLEAR CLOCK 3 OR 2
              NOP
   LOO83B     SET8       X≠0040≠,1
              L          1,X≠0A06≠
              BFNE       (6,0),0,P21
              BFNE       (7,0),1,P23
              B          P22
   P21        BFNE       (7,0),1,P22
   P23        S          1,X≠0A07≠
              SETF       7P2,1
              B          J21
   P22        L          1,X≠0A07≠
   J21        ST         1,X≠0A08≠
              B8NE       7P2,1,ZPN3
              CML        (6,4),(2,0)
              B          GF3
              B          GF3
              B          PK3
   ZPN3       CML        (6,4),(5,0)          CHECK 1 FOR GROUND FAULT
              B          GF3
              B          GF3
              B          PK3
   PK3        SETF       F5,1
              AMT        (X≠0110≠,6),1
              CM         (X≠10≠,4),(X≠C≠,4)
              B          GC2
              B          PART1
              B          PART1
   GF3        BFNE       F5,1,GC2
              AMT        (X≠0010≠,6),-1
              SETF       F5,0
   GC2        BFNE       SEGF,1,GC3
              B8NE       7P2,1,ZPN4
              SETF       7P2,3
              CML        (7,4),(2,0)
              B          GF4
              B          GF4
              B          PK4
   ZPN4       CML        (7,-),(6,0)          CHECK IF LINE 2 IS GND
              B          GF4
              B          GF4
   PK4        SETF       F7,1
              AMI        (X≠12≠,6),1
              CM         (X≠12≠,4),(X≠0F≠,4)
              B          CMP2
              B          PART1
              B          PART1
   GF4        BFNE       F7,1,CMP2
              AMT        (X≠12≠,6),-1
              SETF       F7,0
              B          CMP2
   GC3        BFNE       7P2,1,ZPN5
              SETF       7P2,0
              CML        (7,4),(2,0)
```

Computer Program for the Fault Detection

```
           GF5
           GF5
           PK5
ZPN5   CML  (7,4),(6,0)            CHECK IF LINE 2 IS GND
           GF5
           GF5
PK5    SETF E5,1
       AHT  (X≠11≠,5),1
       CM   (X≠11≠,4),(X≠1F≠,4)
           CMP2
           PART1
           PART1
GF5    BFNE E5,1,CMP2
       AHT  (X≠11≠,5),-1
       SETF E5,0
CMP2   CML  (0008,4),(0,0)
           DSTL2
           DSTL2
DSTL2  SETF E4,1
       ADB  -1,OK3,2
       PART1
K3     BFNE E4,1,OK3
       AA   2,1
       SETF E4,0
OK3    NOP                         CHECK IF CLOCK 3 OR 2 IS HIGH
LOCK31 BBNE Y≠30≠,1,3              START CONVERSION ON CHANNEL 1
       SET3 1,1
       BBNE 7,1,3
       STOR (-,12),0006
       MLA  4,X≠0A06≠
LOOS1  SET3 0,1
       BBNE 0,1,3
       STOR (4,12),0007
       MLA  4,X≠0A07≠
       SET3 Y≠0040≠,1             CLEAR CLOCK 1 OUTPUT
       NOP
       SET3 Y≠0040≠,1
       L    1,X≠0A06≠
       BFNE (6,0),0,P31
       BCNE (7,0),1,P33
           P32
P31    BFNE (7,0),1,P32
P33    SET  1,X≠0A07≠
       SETF EP3,1
           J31
P32    A    1,X≠0A07≠
J31    A    1,X≠0A09≠
       BFNE EP3,1,ZPN6
       CML  (6,4),(2,0)
           GF6
           GF6
ZPN6   CML  (6,4),(6,0)            CHECK IF LINE 1 IS GND
           GF6
           GF6
PK6    SETF E6,1
       AHT  (X≠10≠,6),1
       CM   (X≠10≠,4),(X≠1F≠,4)
           GC4
           PART1
           PART1
GF6    BFNE E6,1,GC4
       AHT  (X≠10≠,6),-1
       SETF E6,0
GC4    BFNE EP0F,1,GC5
       BFNE EP3,1,ZPN7
       SETF EP3,0
       CML  (7,4),(2,0)
           GF7
           GF7
ZPN7   CML  (7,4),(6,0)            CHECK IF LINE 3 IS GND
           GF7
           GF7
```

Computer Program for the Fault Detection

```
PK7       SETF      F7,1
          AL1       (X≠12≠,6),1
          CM        (X≠12≠,L),(X≠0F≠,4)
          B         CMP3
          B         PART1
          B         PART1
GF7       BFNE      F7,1,CMP3
          AMI       (X≠12≠,6),-1
          SETF      F7,2
          B         CMB3
GC5       BFNE      ZP3,1,ZPN8
          SETF      ZP3,1
          CML       (7,4),(2,0)
          B         GF8
          B         GF8
          B         PK8
ZPN8      CML       (7,4),(6,0)          CHECK IF LINE 2 IS GND
          B         GF8
          B         GF8
PK8       SETF      F6,1
          AMI       (X≠11≠,6),1
          CM        (X≠11≠,4),(X≠0F≠,4)     .
          B         CMP3
          B         PART1
          B         PART1
GF8       BFNE      F6,1,CMP3
          AMI       (X≠11≠,6),-1
          SETF      F6,2
CMP3      CML       (0003,4),(0,0)
          B         DSTL3
          B         DSTL3
          B         A1
DSTL3     SETF      F4,1
          AB3       -1,CK1,2
          B         PART1
*                   THIS PORTION OF PROGRAM FINDS TYPE OF THE FAULT
PART1     CM        (X≠10≠,4),(X≠14≠,4)
          B         P1S0
          NOP
          SETF      GL1,1
          CM        (X≠11≠,4),(X≠14≠,4)
          B         P1S1
          NOP
          SETF      GL2,1
          CM        (X≠12≠,4),(X≠14≠,4)
          B         P1S5
          NOP
          SETF      GL3,1
          BFNE      GL2,1,P1S2
          BFNE      GL1,1,P1S3
          SET3      X≠46≠,0
          SET3      X≠4C≠,0
          SET3      X≠40≠,0
          SET3      X≠40≠,0
          B
P1S2      BFNE      GL1,0,P1S4           LINE 3 TO GND FAULT
          SET3      X≠4C≠,0
          SET3      X≠40≠,0
          B
P1S4      SET3      X≠4A≠,0              LINE TO LINE FAULT 1,3
          SET3      X≠4C≠,0
          SET3      X≠40≠,0
          B
P1S3      SET3      X≠4B≠,0              LINE TO LINE FAULT 2,3
          SET3      X≠4C≠,0
          SET3      X≠40≠,0
          B
P1S5      BFNE      GL1,1,P1S6
          BFNE      GL2,0,P1S7           LINE 1 TO GND FAULT
          SET3      X≠4A≠,0
          SET3      X≠40≠,0
          B
P1S7      SET3      X≠4A≠,0              LINE TO LINE FAULT 1,2
          SET3      X≠4B≠,0
          SET3      X≠40≠,0
```

Computer Program for the Fault Detection

```
0156      BPNE      SL2,1,PART2        LINE 2 TO GND FAULT
          SET3      X≠43≠,0
          SET3      X≠40≠,0

PART2     BPNE      X≠33≠,0,?
          NOP
          BPNE      X≠33≠,1,5          START CONVRTION ON LINE 2
          SET3      2,1
          BPNE      0,1,5
          STOR      (4,12),0006        START CONVERTION ON LINE 3
          SET3      ,1
          BPNE      0,1,5
          STOR      (4,12),0007
          MLA       4,X≠0A06≠
          MLA       4,X≠0A07≠
          CML       (16,4),(4,0)       CHECK IF LINE 2 IS GND

          CML       (17,4),(4,0)       CHECK IF LINE 3 IS GND

          BPNE      X≠30≠,0,5
          NOP
          BPNE      X≠39≠,1,5          START CONVERTION ON LINE 1
          SET3      5,1
          BPNE      0,1,5
          STOR      (4,12),0016        START CONVRTION ON LINE 2
          SET3      6,1
          BPNE      0,1,5
          STOR      (4,12),0007        START CONVERTION ON LINE 3
          SET3      7,1
          BPNE      0,1,5
          STOR      (4,12),0008
          MLA       4,X≠0A06≠
          MLA       4,X≠0A07≠
          MLA       4,X≠0A08≠          CHECK IF NO IS +VE
          BPNE      (6,0),0,N1         YES,CHECK IF NO IS +VE
          BPNE      (7,0),0,N2         CHECK IF NO IS -VE
          BPNE      (8,0),1,N000       YES +,+,-
          N12                          CHECK IF NO IS +VE
N2        BPNE      (6,0),0,N23        YES,0,+,0
          N13                          CHECK IF NO IS +VE
N1        BPNE      (7,0),0,N13        YES,CHECK,IF NO IS +VE
          BPNE      (8,0),0,N13        YES,-,+,+
          N23                          CHECK IF NO IS +VE
N3        BPNE      (5,0),0,N100       YES
          N12
N12       L         1,X≠0A06≠
          L         1,X≠0A07≠
          ST        1,X≠0A20≠
          CML       (X≠21≠,4),(0,0)    CHK IF 1,2 ARE EQ

          L         1,X≠0A08≠
          L         1,X≠0A07≠
          A         1,X≠0A06≠
          ST        1,X≠0A20≠
          CML       (X≠20≠,4),(0,0)    IS SUM EQ ZERO

          SET3      X≠4A≠,0            LINE TO LINE FAULT 1,2
          SET3      X≠49≠,0

N23       L         1,X≠0A07≠
          L         1,X≠0A08≠
          ST        1,X≠0A20≠
          CML       (X≠20≠,4),(0,0)    IS LINE 2,3 EQ

          L         1,X≠0A06≠
          L         1,X≠0A07≠
          A         1,X≠0A08≠
          ST        1,X≠0A20≠
          CML       (X≠20≠,4),(0,0)    IS SUM EQ ZERO
```

Computer Program for the Fault Detection

```
        SET3      X#4#,0              LINE TO LINE FAULT 2,3
        SET3      X#40#,0
N13
        LST       1,X#0A06#
                  1,X#0A08#
        ST        1,X#0A20#
        CML       (X#20#,4),(0,0)     IF LINE 1,3 ARE EQ

        LST       1,X#0A07#
                  1,X#0A06#
                  1,X#0A08#
        ST        1,X#0A20#
        CML       (X#20#,4),(0,0)     IS SUM EQ TO ZERO

        SET3      X#4A#,0             LINE TO LINE FAULT 1,3
        SET3      X#40#,0
N000
        LST       1,X#0A06#
                  1,X#0A07#
        ST        1,X#0A20#
        CML       (X#20#,4),(0,0)     IF LINE 1,2 ARE EQ

        LST       1,X#0A07#
                  1,X#0A08#
        ST        1,X#0A20#
        CML       (X#20#,4),(0,0)     LINE 1 2 3 ARE EQ

        SET3      X#4A#,0             LINE TO LINE FAULT 1 2 3
        SET3      X#4B#,0
        SET3      X#40#,0
        END       PROG
        FLAG SEGMENT
        FSEG
        FLAG      F1,F2,F3,F4,F5,F6
                  F7,GL1,GL2,GL3,SEGF,ZP1,ZP2,ZP3
        SETF      F1,0
        SETF      F2,0
        SETF      F3,0
        SETF      F4,0
        SETF      F5,0
        SETF      F6,0
        SETF      F7,0
        SETF      GL1,0
        SETF      GL2,0
        SETF      GL3,0
        SETF      SEGF,0
        SETF      ZP1,0
        SETF      ZP2,0
        SETF      ZP3,0
        END
```

Computer Program for the Fault Detection