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Title: Current-Feedthrough Cancellation Technique In Switched-Current Circuits

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David J. Allstot

Switched-capacitor (SC) circuits suffer from clock-feedthrough effects as do switched-current (SI) circuits. Current-feedthrough in SI circuits is caused by non-ideal characteristics of the Metal Oxide Semiconductor (MOS) switches during the time interval when they are turned off. In this paper, an analysis of the effects of current-feedthrough in SI circuits is given and a current-feedthrough cancellation circuit is presented. This technique allows SI circuits to be implemented with small transistor sizes while realizing good performance. To verify the performance of this circuit, two different versions $\left(\text{mirror transistors } \frac{W}{L} = \frac{100\ \mu m}{10\ \mu m} \text{ and } \frac{W}{L} = \frac{20\ \mu m}{2\ \mu m}\right)$ of fifth-order lowpass Chebyshev filters were implemented using a two-micron P-well CMOS process technology. Both filters used the same switch sizes $\frac{W}{L} = \frac{3\ \mu m}{2\ \mu m}$.

Current-Feedthrough Cancellation Techniques In Switched-Current Circuits

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1. INTRODUCTION

Recently, much interest has been given to analog sampled-data signal processing circuits in which currents instead of voltages are used to represent signals. This is known as the switched-current (SI) technique and has been used in designing filters [1, 2], Analog-digital converters (ADC) [3], and Digtal-analog converters (DAC) [4]. One advantage of this method is its low power supply voltage operation because currents and current mirrors are used instead of voltages and voltage operational amplifiers (VOA). Another advantage of the SI circuit technique is that the fabrication process is very simple. Unlike switched-capacitor (SC) circuits, SI circuits require only Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETS); therefore, non-standard processing options to provide a linear floating capacitor are not required.

Like SC circuits, SI circuits also suffer a similar problem with clock-feedthrough. Clock-feedthrough is caused by the non-ideal nature of the Metal-Oxide-Semiconductor (MOS) switches. When the switches are turned off, channel charge is injected into the data holding node and hence induces error voltage. This error voltage induces error current which is called current-feedthrough. In the SI circuits, current-feedthrough produces DC offset, AC gain error, and harmonic distortion. Although several current-feedthrough cancellation techniques have been proposed, none of them cancels the AC gain error or eliminates harmonic distortion due to the current-feedthrough effect. Other problem that SI circuits have are threshold voltage and device size mismatches due to process variations.

The main purpose of this project was to study the current-feedthrough effects in SI circuits caused by the MOS switches and to develop a current-feedthrough cancellation technique for SI circuits.

In the second chapter, the SI technique is introduced and discussed for the purpose of realizing necessary analog signal processing blocks such as summing, inverting, scaling, and delaying functions.

The third chapter provides the circuit and mathematical model of the switch when it is turned off and an analysis of current-feedthrough effects on SI circuits. The discussion of AC gain errors and harmonic distortion induced by clock-feedthrough is also included. Three dimensional plots of clock-feedthrough voltages and harmonic distortion induced by current-feedthrough in Track-and-Hold (T/H) SI circuits are shown.

The forth chapter illustrates various proposed techniques to solve current-feedthrough problems and their corresponding SPICE (Simulation Program for Integrated Circuits Emphasis) [5] simulation results. In the last part of this chapter, a proposed current-feedthrough cancellation technique and its simulation results are illustrated.

The fifth chapter shows various SI circuits applications (e.g. Chebyshev five-pole lowpass filters and current integrator circuits) which use the proposed current-feedthrough cancellation circuit technique.

The conclusions are given in the sixth chapter.

2. SWITCHED-CURRENT CIRCUIT TECHNIQUE

2.1. The Attractiveness Of SI Circuits.

The SI circuit technique possesses three advantages. First, it requires low power supply voltage because current mirrors are used and current is the signal medium. Second, it offers high frequency operation because of the low impedance nodes. Finally, unlike SC circuits, SI circuits do not need a linear floating capacitor, so a simple standard digital Complementary Metal-Oxide-Semiconductor (CMOS) process technology can be used to implement SI circuits. All of these features of the SI circuit technique are very attractive for the future trend of decreasing power supply voltage, high frequency circuits, and simplicity of process fabrication.

2.1.1. Low Power Supply Voltage Operation

The trend to reduce the minimum feature size to a sub-micron range leads to a reduction of power supply. This reduction in power supply makes the SI circuit technique suitable since its basic building block, the current mirror, requires a very low power supply voltage and still maintains its proper current-amplifying function. As a matter of fact, the minimum power supply voltage can be determined from Fig. 1. Assume that the saturation voltage (V_{dsat}) of the PMOS (P-channel MOS) and NMOS (N-channel MOS) transistors are equal. To keep all transistors in saturation region, the saturation voltage (V_{dsat}) across drain-source of M3 and a threshold voltage (V_t) plus V_{dsat} of M1 is required. By summing all these voltages, the minimum power supply voltage required for this circuit is the threshold voltage of M1 plus twice V_{dsat} ($V_t + 2V_{dsat}$). For a typical two-micron minimum feature size CMOS technology offered by MOS Integration Service (MOSIS), this voltage is approximately 2.2 V. With the trend of having 3.3 V as the future industrial standard power supply, the 2.2 V minimum required to operate any SI circuit is very attractive.

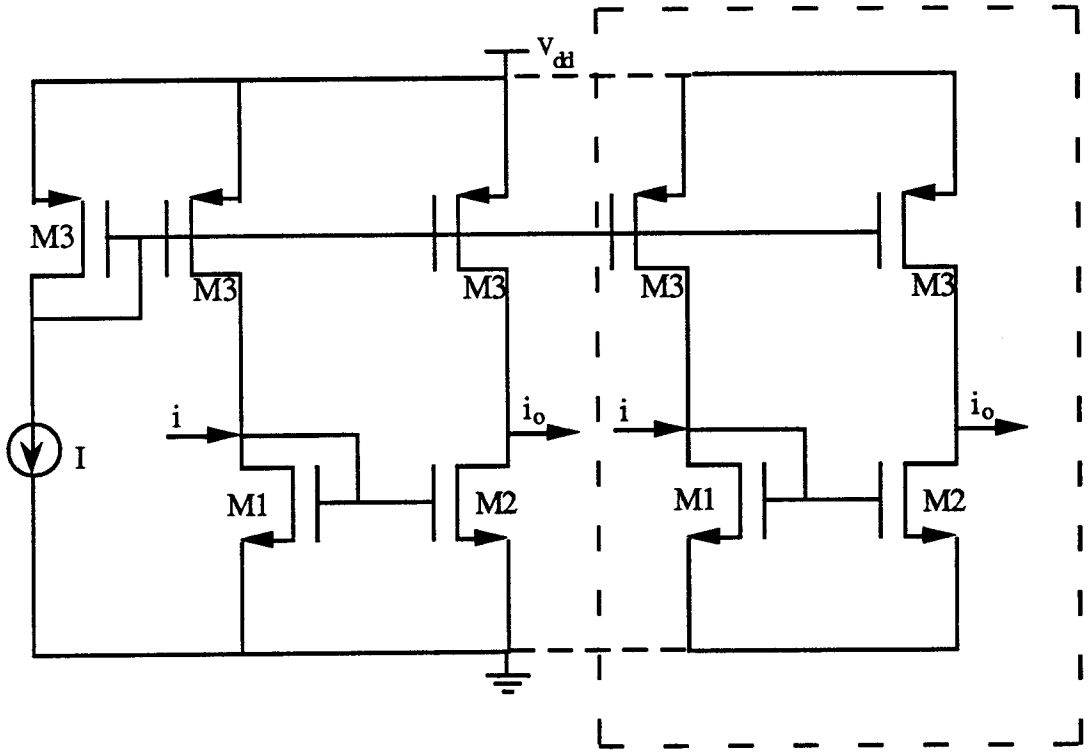


Fig. 1 A simple current mirror

2.1.2. High-Frequency Operation Of SI Circuits

The ability to operate at a high-frequency is one of the most attractive features of the SI circuit technique. The reason for this is that at the diode-connected transistor M1 above, the impedance is low, approximately $\frac{1}{g_m}$. With a total nodal capacitance of $C_{gs1} + C_{gs2}$, the bandwidth at this node is approximately $\frac{g_{m1}}{(C_{gs1} + C_{gs2})}$. Also there is an implicit constant gain-bandwidth product rule in any circuit. As illustrated in Fig. 2, to obtain a high gain in a voltage-mode operational amplifier (VOA), for example, the -3 dB cutoff frequency or bandwidth is very low. In SI circuits, current mirrors are used with ideally unity-gain, so based on Figs. 2, the -3 dB cutoff frequency is potentially very high.

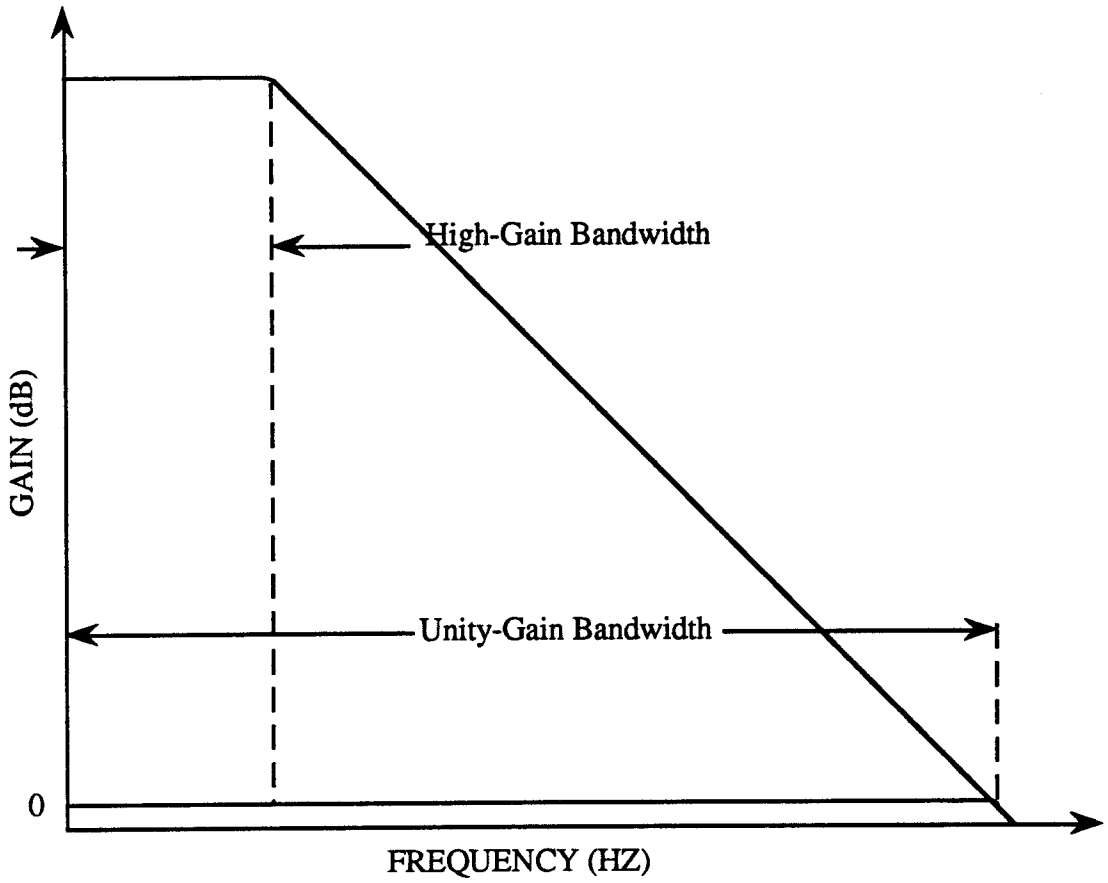


Fig. 2 Gain versus frequency graph

2.1.3. Standard CMOS Fabrication Process

Another major advantage of the SI circuit technique is the fabrication process simplicity. Unlike the SC circuit technique, linear capacitors are not required to implement any SI circuit, Only MOSFETS (MOS Field Effect Transistors) are needed. This eliminates the extra processing options required to fabricate the linear floating capacitors. In fact, to implement any SI circuit, only a standard digital CMOS VLSI (Very Large Scale Integration) process is required.

2.2. Basic Building Block Of Signal Processing

For general-purpose signal processing, there are four basic functions: inverting, summing, scaling, and delay. By using combinations of the above functions, all sorts of signal processing can be done. In the following section, the implementation and operation of these functions in the SI circuit technique is shown and explained.

2.2.1. Inverting, Summing, and Scaling Circuits

As mentioned earlier, current mirrors are used as the basic building block in SI circuits. Three of the four signal processing functions can be implemented from the simple current mirror/amplifier. Illustrated in Fig. 3 "I" defines the DC bias current, "i" defines the input AC signal current, and "A" is the scale factor which is defined as $A = \frac{(W/L)_2}{(W/L)_1}$.

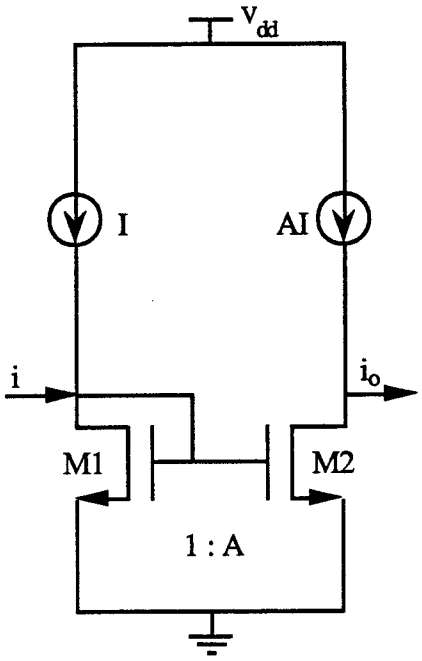


Fig. 3 A simple current mirror/amplifier

An SI inverting circuit

Fig. 4 shows an SI inverting circuit configuration. Assuming an ideal current mirror, the AC signal current plus DC bias current, I + i, enter the input node at the diode-connected transistor M1. Due to the current mirroring action, a replica of the current flows into the drain of M2, I+i. Applying Kirchhoff's current law (KCL) at the output node, the following equations are obtained:

$$i_o + I + i - I = 0 \tag{2.1}$$

$$i_o = -i \tag{2.2}$$

Hence, the output is inverted relative to the input signal current, i.

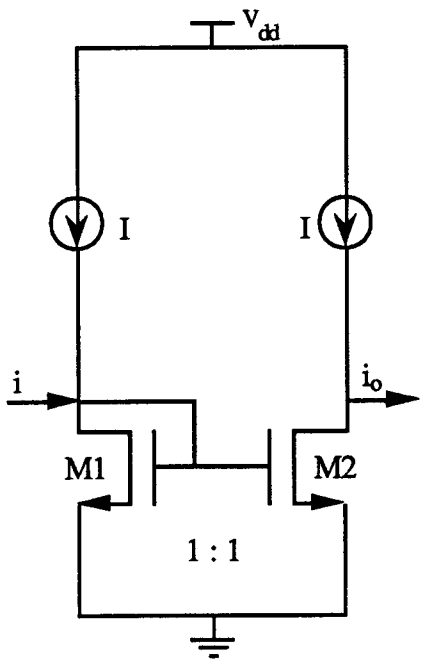


Fig. 4 An SI inverting circuit

An SI summing circuit

In Fig. 5, an SI summing circuit is shown. Since current is the signal medium in SI circuits, summing currents is done by making direct connections to the input low-impedance summing node.

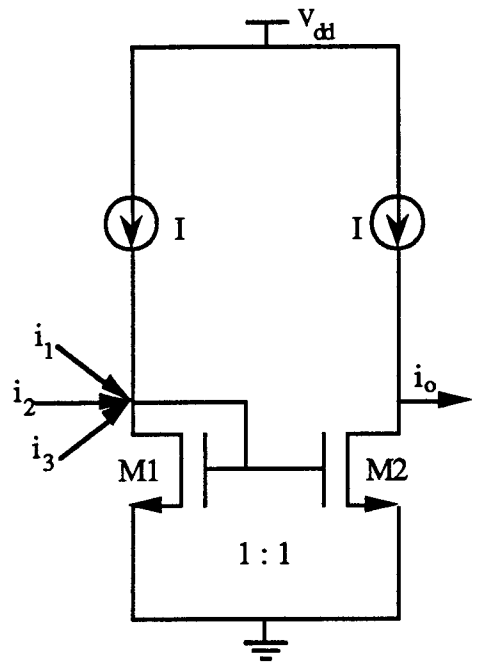


Fig. 5 An SI summing circuit

An SI scaling circuit

The scaling circuit is shown in Fig. 6. To scale the input current by a factor of A, both the bias current and the device ratio, $\frac{(W/L)_2}{(W/L)_1}$, must be scaled by A. The operation of this circuit is easily verified. The current into the drain of M1 is the DC bias current, I, plus the AC signal current, i,

$$I_{d1} = I + i \tag{2.3}$$

If M1 and M2 are perfectly ratioed (i.e. M2 has a width A times greater than M1), then the current into the drain of M2 is

$$I_{d2} = A(I + i) \tag{2.4}$$

Applying KCL at the output node the following equations are obtained:

$$i_o + I_{d2} - AI = 0 \tag{2.5}$$

$$i_o + A(I + i) - AI = i_o + Ai = 0 \tag{2.6}$$

$$i_o = -Ai \tag{2.7}$$

Thus a scaled and inverted version of the input signal is obtained. To obtain a non-inverted output, simply pass this signal through a second inverting SI circuit.

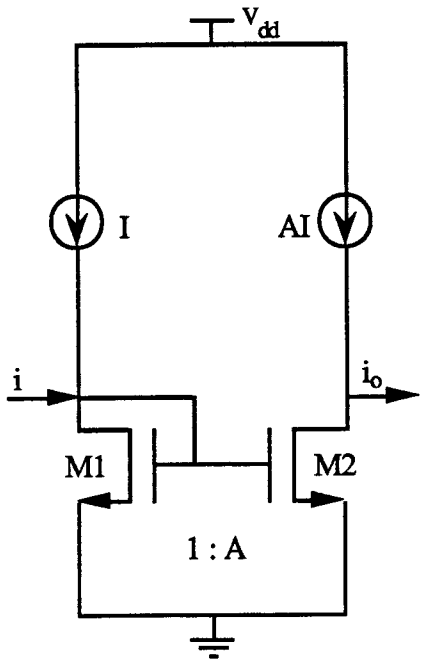


Fig. 6 An SI scaling circuit

2.2.2. An SI Delaying Circuit

The signal is delayed by placing a MOS transistor,MS, between the gates of M1 and M2 as shown in Fig. 7. This transistor acts as a switch that is controlled by applying a clock signal, Φ, to its gate. To analyze this circuit, two cases are considered: the switch is turned on and the switch is turned off.

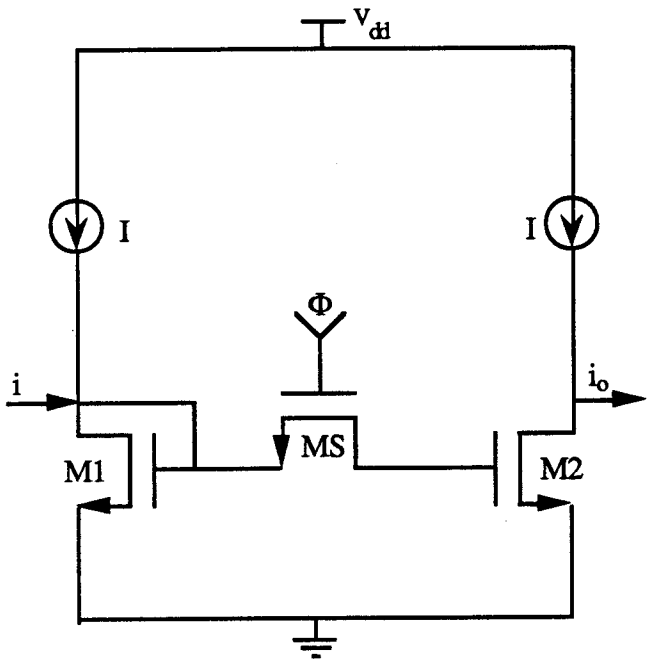


Fig. 7 An SI delaying circuit

Case I: Φ high -- switch is turned on

When the switch closes, the circuit reduces to a simple current mirror/amplifier. Assuming zero switch resistance, an equivalent circuit is shown in Fig. 8. The gate voltages of both transistors M1 and M2 change as the input current changes, i.e. $V_{gs}(t) = V_t + \sqrt{\frac{2(I + i)}{K'(W/L)}}$; W defines the width and L the length of the

transistors. Based on a two micron CMOS process with a gate oxide thickness of 280 Å, K', the device transconductance parameter, is found to be 44.64 $\frac{\mu A}{V^2}$ for NMOS and 25.45 $\frac{\mu A}{V^2}$ for PMOS.

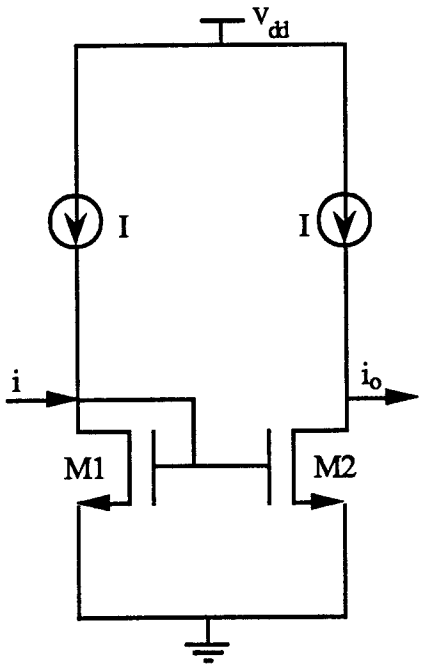


Fig. 8 An equivalent circuit when the switch is turned on

Since V_{gs} of M1 equals V_{gs} of M2, the drain currents into both transistors are equal to I + i. Again, applying Kirchhoff's current law to the output node, the output current is obtained and is equal to:

$$i_o = -i \tag{2.8}$$

This implies that the output is tracking the input signal current with an inversion.

Case II: Φ low -- switch is turned off at time t = T

An equivalent circuit after time t = T when the switch is turned off is shown in Fig. 9. When the switch is turned off, the gates of M1 and M2 are disconnected. The gate voltage that exists at the instant just before the switch is turned off i.e., at time $t = T^-$, is stored on the non-critical gate capacitance of M2. Thus the current through M2 is held at the value corresponding to the current through M1 just before the switch is off, i.e. $i_o(t) = i(T)$. This is the "hold" operation.

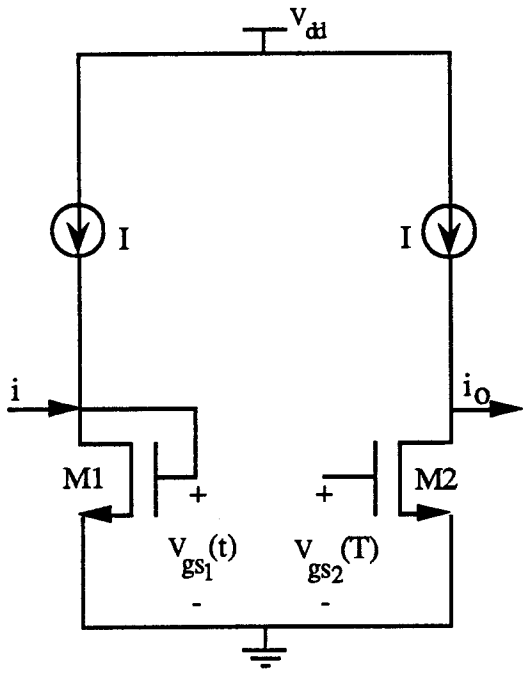


Fig. 9 An equivalent circuit when the switch is turned off

3. POTENTIAL PROBLEM IN SI CIRCUIT

3.1. Current-feedthrough

The most challenging design problem arises from the non-ideal characteristic of the switch when it is turned off. This problem has been variously called "clock-feedthrough" [7], "charge feedthrough" [8], "charge injection" [9], and "charge dumping". Clock-feedthrough reefers to the error voltage caused by the injection of the charge from the channel of the switch to the data holding node. However, in SI circuits, this error voltage eventually causes error current at the output. Hence, this problem is referred to as "current-feedthrough". Shown again in Fig. 10 is the SI track-and-hold (T/H) circuit, and Fig. 11 shows an equivalent circuit model that is very useful in studying clock feedthrough effects [10].

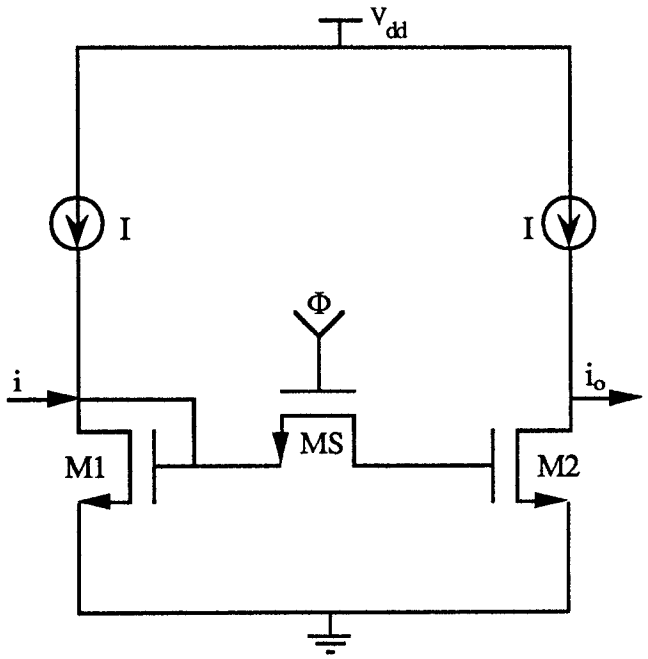


Fig. 10 An SI T/H circuit

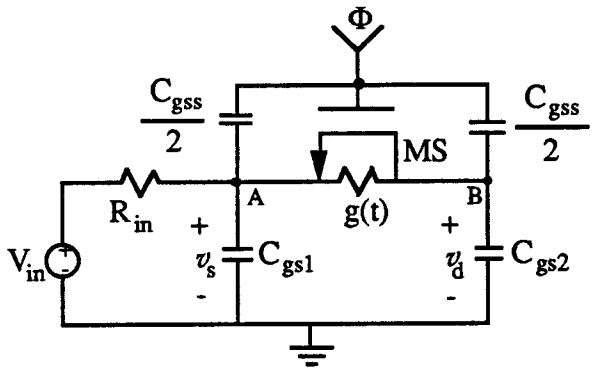


Fig. 11 Modeling T/H SI circuit

C_{gs1} is equal to C_{gs2} because M1 and M2 are assumed to be identical. To a first-order approximation, assuming that R_{in} is constant,

$$R_{in} = \frac{1}{g_{m1}} = \frac{V_{GS1} - V_t}{2I} \tag{3.1}$$

$$V_{in} = V_{gs}(t) = \sqrt{\frac{2(I + i)}{K'(W/L)}} + V_t \tag{3.2}$$

Note that V_{in} depends on the input signal current i which is varying in time. The basic issue in current-feedthrough is where the charge in the channel goes when the switch is turned off. When the switch is fully on ($\Phi = V_{dd}$), there is a charge in the channel of the MOSFET switch given by:

$$Q = C_{ox} W L[V_{dd} - V_{gs}(t) - V_t] \tag{3.3}$$

Where

Q = the charge in the channel of the switch.

C_{ox} = the oxide capacitance of the switch per unit area.

W and L = the width and length of the switch transistor, respectively.

V_{dd} = the power supply voltage.

$V_{gs}(t)$ = the voltage at the source side of the switch.

V_t = the threshold voltage of the switch and including the body effect.

C_{gss} = the gate-source capacitance of the switch transistor.

Hence, from equation 3.3 it is clear that the channel charge decreases with increasing input voltage at the source of the switch. When the switch is turned off, this charge has to flow somewhere. Where this charge flows is dependent on several factors. The charge redistribution depends on several factors such as the ratio of C_{gsol} (the gate-drain overlap capacitance) of the switch to C_{gs} (gate-source capacitance) of M2, R_{in}, the ratio of C_{gs} of M1 to C_{gs} of M2, and α, the rate at which the clock is turned off. For a very slow turnoff time, all of channel charge has time to flow into the low impedance side which is the diode-connected transistor side. In this situation, ideally none of the channel charge is deposited onto the gate of M2. In Fig. 12, the operation regions of the switch when it is turned off are shown.

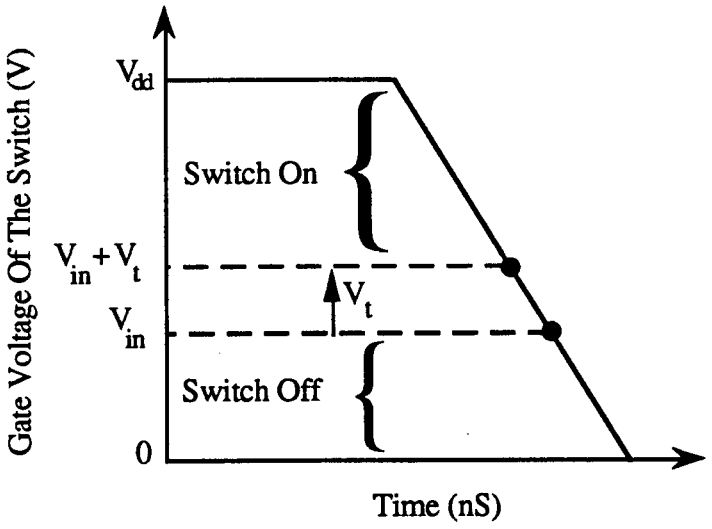


Fig. 12 The behavior of the switch when it is turned off

There are two regions in which the switch operates when it is turned off. The first region is represented by the gate-to-source voltage (V_{gs}) of the switch being greater than the threshold voltage (V_t). In this phase, the charge in the channel exits through both source and drain of the switch transistor, and the channel conductance decreases as the gate voltage decreases. In the second region, the gate-to-source voltage of the switch is less than the threshold voltage of the switch. In this phase, the switch transistor is off and the channel no longer exists. The charge model for this circuit is a simple capacitor divider as shown in Fig. 13.

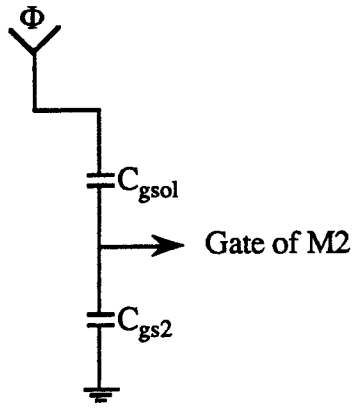


Fig. 13 Modeling T/H circuit on the second region

Consider again the T/H model of Fig. 11. This model is represented by a system of differential equations. Applying KCL to nodes A and B, the following equations are obtained:

$$C_{gs1}\frac{\partial v_s}{\partial t} = g(t)\,(v_d - v_s) - \frac{v_s}{R_{in}} - i_d \tag{3.4}$$

$$C_{gs2}\frac{\partial v_d}{\partial t} = g(t)\,(v_s - v_d) + i_d \tag{3.5}$$

Where

v_s = the clock-feedthrough voltage injected on the source side of the switch.

v_d = the clock-feedthrough voltage injected on the drain side of the switch,

$g(t)$ = the transconductance of the switch defined as

$\frac{\partial I_d}{\partial V_{gs}} = \beta_S(V_{gs} - V_t)$; where $\beta_S = K'\left(\frac{W}{L}\right)_S$.

i_d = the current injection due to the coupling of the switch capacitance to the load capacitance defined as $i_d = (C_{gsol} + \frac{C_{ox}W_{eff}L_{eff}}{2})\alpha$; α is the rate at which the clock is turned off.

R_{in} = the input resistance of transistor M1 as a function of time.

The above set of equations is a first-order system of partial differential equation. With $R_{in} \rightarrow \infty$,This system of equations can be solved for closed-form solutions. But since $R_{in} \neq \infty$, a numerical technique is employed. A well-known procedure for solving this system of equations is the Runge-Kutta method [11]. The numerical solution is obtained by using a computer program called MATHLAB; the programs are given in the appendix. Fig. 14 shows the results plotted as a 3-D plot of clock-feedthrough voltage on the data holding node.

As can be seen from the graph, with a fast clock edge, when V_{gs} increases the clock-feedthrough voltage decreases. This agrees well with our theory, equation 3.3. As the switching rate decreases the clock-feedthrough voltage on the gate of M2 decreases, which is exactly what is expected. The final note is that the clock-feedthrough voltage is signal dependent.

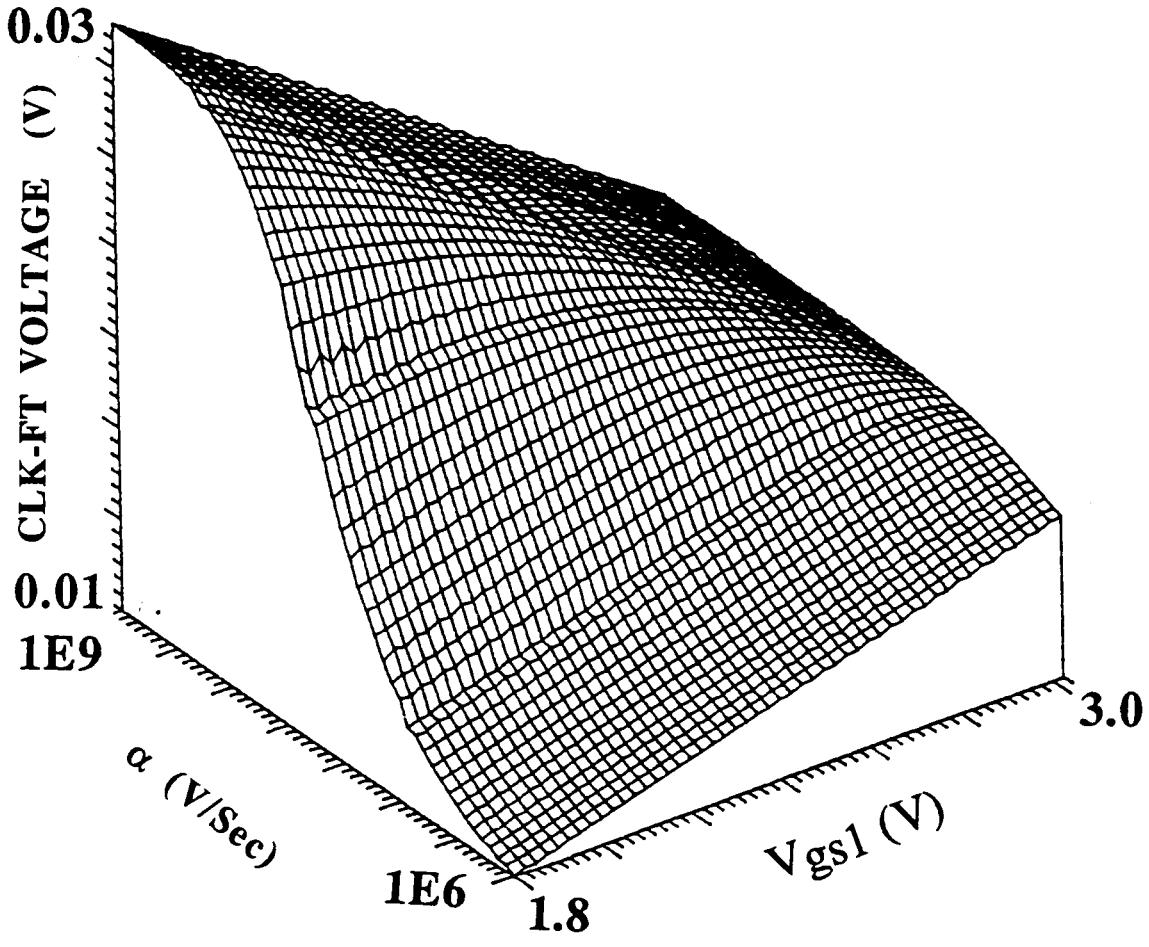


Fig. 14 3-D plot of clock-feedthrough voltage on the data holding node of Fig. 10. The transistor sizes are $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \frac{100\ \mu m}{10\ \mu m}$, and $\left(\frac{W}{L}\right)_S = \frac{6\ \mu m}{3\ \mu m}$

3.2. Distortion In SI Circuits

Harmonic distortion in SI circuits is induced by clock-feedthrough voltages and device mismatches due to process variations of the transistors. For brevity, only harmonic distortion due to clock-feedthrough is considered. The distortion due to K', W/L ratio, and V_t mismatches are analyzed the same way. Fig. 15 repeats the T/H circuit just before the switch is turned off.

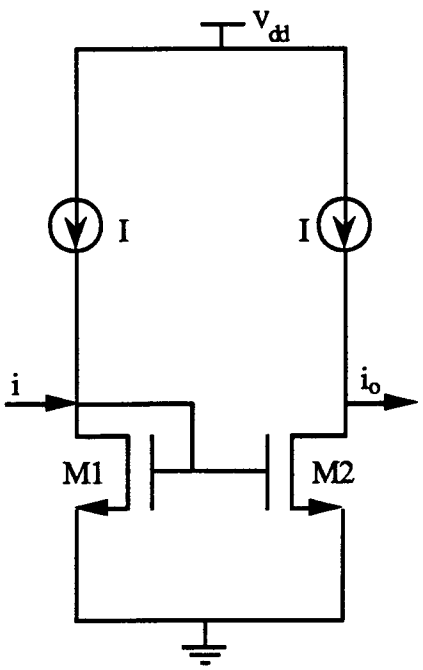


Fig. 15 T/H circuit just before the switch is turned off

The drain current through M1 is I_{d1} and is equal to

$$I_{d1} = I + i = \frac{\beta_1}{2}(V_{gs} - V_{t1})^2 \tag{3.6}$$

and therefore,

$$V_{gs} = \sqrt{\frac{2(I + i)}{\beta_1}} + V_{t1} \tag{3.7}$$

where $\beta_1 = K'\left(\frac{W}{L}\right)_1$.

V_{gs} developed across the diode-connected M1 is applied to the gate of M2. Therefore

$$I_{d2} = \frac{\beta_2}{2}(V_{gs} - V_{t2})^2 \tag{3.8}$$

$$I_{d2} = \frac{\beta_2}{2}\left(\sqrt{\frac{2(I + i)}{\beta_1}} + V_{t1} - V_{t2}\right)^2 \tag{3.9}$$

Where $\beta_2 = K'\left(\frac{W}{L}\right)_2$.

Suppose that the switch is turned off and an additional voltage of ΔV is injected only onto the gate of M2. The equivalent circuit is shown in Fig. 16. With ΔV injected onto the gate of M2, I_{d2} becomes:

$$I_{d2} = \frac{\beta_2}{2}(V_{gs} - V_{t2} + \Delta V)^2 = \frac{\beta_2}{2}\left(\sqrt{\frac{2(I + i)}{\beta_1}} + V_{t1} - V_{t2} + \Delta V\right)^2 \tag{3.10}$$

For simplicity, assume that $V_{t1} = V_{t2}$, and $\beta_1 = \beta_2 = \beta$

$$I_{d2} = \frac{\beta}{2}\left(\sqrt{\frac{2(I+i)}{\beta}} + \Delta V\right)^2 = \frac{\beta}{2}\left(\frac{2(I+i)}{\beta} + 2\Delta V\sqrt{\frac{2(I+i)}{\beta}} + \Delta V^2\right) \quad (3.11)$$

$$i_o = -I_{d2} + I = -i - \beta\Delta V\sqrt{\frac{2(I+i)}{\beta}} - \frac{\beta}{2}\Delta V^2$$

$$= -i - \beta\Delta V\sqrt{\frac{2I}{\beta}}\sqrt{1+\frac{i}{I}} - \frac{\beta}{2}\Delta V^2 \quad (3.12)$$

$$i_o = -i - \beta\Delta V(V_{GS} - V_t)\sqrt{1+\frac{i}{I}} - \frac{\beta}{2}\Delta V^2 \quad (3.13)$$

$$i_o = -i - \frac{2\Delta V I}{(V_{GS} - V_t)}\sqrt{1+\frac{i}{I}} - \frac{\beta}{2}\Delta V^2 \quad (3.14)$$

Applying the binomial expansion to the square root term

$$i_o = -i - \frac{\beta}{2}\Delta V^2 - \frac{2\Delta V I}{V_{GS} - V_t}\left(1 + \frac{1}{2}\left(\frac{i}{I}\right) - \frac{1}{8}\left(\frac{i}{I}\right)^2 + \frac{1}{16}\left(\frac{i}{I}\right)^3 - + \ldots\right) \quad (3.15)$$

$$i_o = -\Delta V\left(\frac{\beta}{2}\Delta V + \frac{2I}{V_{GS} - V_t}\right) - i\left(1 + \frac{\Delta V}{V_{GS} - V_t}\right)$$

$$- \frac{2\Delta V I}{V_{GS} - V_t}\left(- \frac{1}{8}\left(\frac{i}{I}\right)^2 + \frac{1}{16}\left(\frac{i}{I}\right)^3 - + - \ldots\right) \quad (3.16)$$

From equation 3.16, it is clear that the first term is the DC offset, $\frac{\Delta V}{V_{GS} - V_t}$ in the second term is the relative AC gain error, and the remaining terms are the harmonic distortion products caused by the clock-feedthrough, ΔV.

Equation 3.16 is written in polynomial form as:

$$i_o = C + A_1 i + A_2 i^2 + A_3 i^3 + \ldots \tag{3.17}$$

Where

$$C = -\Delta V\left(\frac{\beta \Delta V}{2} + \frac{2I}{V_{GS} - V_t}\right) \tag{3.18}$$

$$A_1 = -1 - \frac{\Delta V}{V_{GS} - V_t} \tag{3.19}$$

$$A_2 = \frac{2\Delta VI}{8(V_{GS} - V_t)I^2} = \frac{\Delta V}{4I(V_{GS} - V_t)} \tag{3.20}$$

$$A_3 = -\frac{2\Delta VI}{16(V_{GS} - V_t)I^3} = -\frac{\Delta V}{8I^2(V_{GS} - V_t)} \tag{3.21}$$

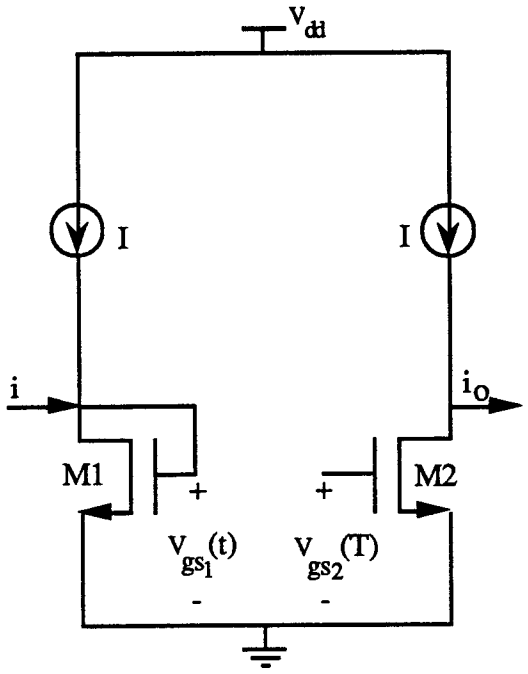


Fig. 16 T/H circuit when the switch is completely off

By definition, fractional harmonic distortion, HD_X , is defined as:

$$HD_X = \frac{\text{Amplitude of X harmonic at the output}}{\text{Amplitude of fundamental at the output}}$$

Now, solving for the fractional harmonic distortion (HD) terms:

$$HD_2 = \frac{1}{2}\frac{A_2}{A_1}\hat{i} \quad \text{and} \quad HD_3 = \frac{1}{4}\frac{A_3}{A_1}\hat{i}; \qquad \text{where } \hat{i} \text{ is the peak value of i.}$$

$$HD_2 = \frac{1}{8}\left(\frac{\Delta V}{V_{GS} - V_t + \Delta V}\right)\left(\frac{\hat{i}}{I}\right) \tag{3.22}$$

$$HD_3 = -\frac{1}{32}\left(\frac{\Delta V}{V_{GS} - V_t + \Delta V}\right)\left(\frac{\hat{i}}{I}\right)^2 \tag{3.23}$$

Total harmonic distortion (THD) is defined as

$$THD = \sqrt{(HD_2)^2 + (HD_3)^2 + (HD_4)^2 + \ldots} \tag{3.24}$$

Usually $HD_2 >> HD_3 >> HD_4$ ... so THD is approximately equal to HD_2.

A three-dimensional plot of total harmonic distortion (THD) is shown in Fig. 17. From equations 3.22 and 3.23, it is clear that as V_{GS} increases, HD_2 and HD_3 decrease. Obviously, the graph shows this relationship also.

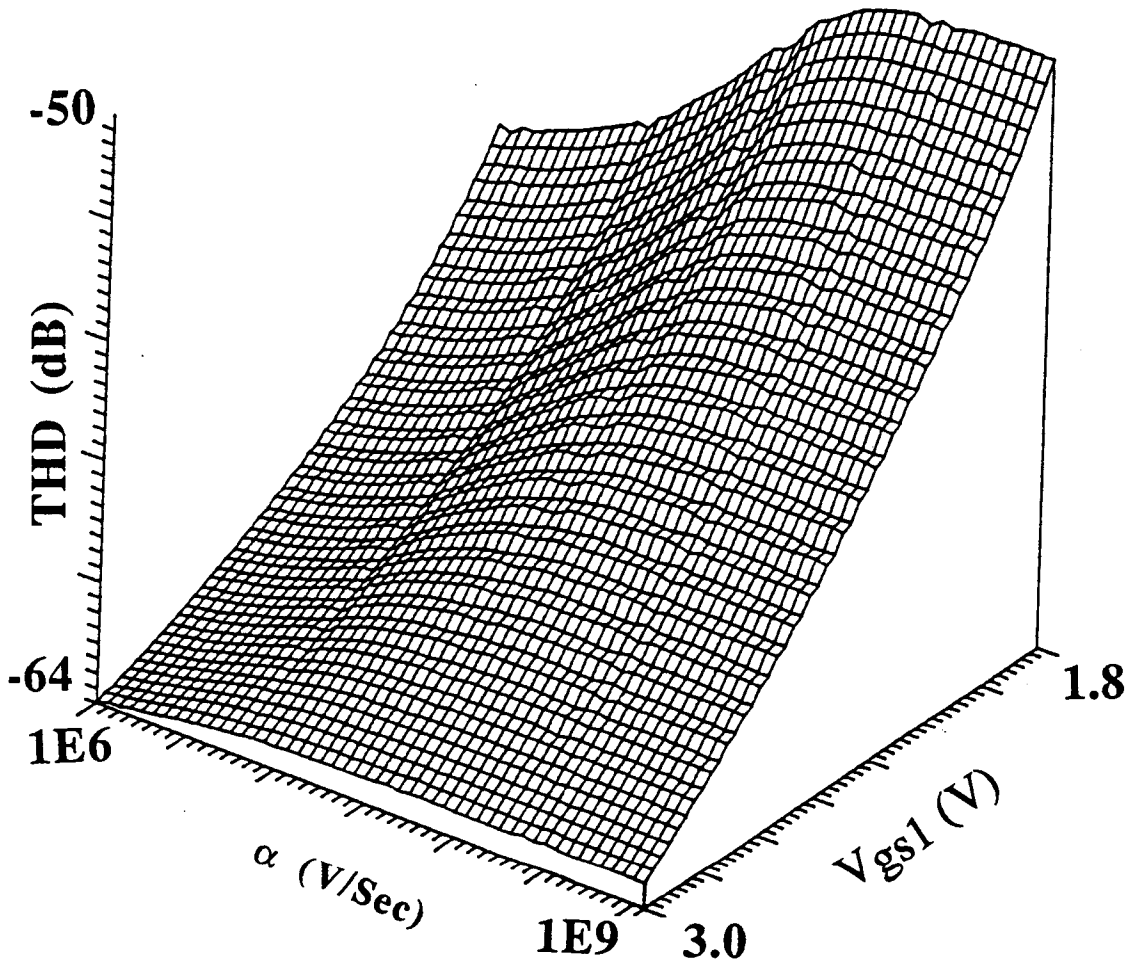


Fig. 17 3-D plot of THD of Fig. 10. The transistor sizes are $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \frac{100\ \mu m}{10\ \mu m}$, $\left(\frac{W}{L}\right)_S = \frac{6\ \mu m}{3\ \mu m}$, and $\frac{i}{I} = 0.3$

3.3. Mismatches

SI circuits suffer one more problem concerning process variations arising from K', $\frac{W}{L}$ ratio, and λV_{DS} mismatches. A similar analysis was performed for these mismatches as clock-feedthrough. These other mismatches only introduce DC offset and AC gain errors. However, threshold voltage mismatches cause not only DC offset and AC gain errors, but also harmonic distortion. A typical threshold voltage mismatch is about 10% for the two micron P-well CMOS process offered by MOSIS (MOS Integration Service). To minimize process induced mismatches in current mirror transistors, layout strategies such as common-centroid and unit-cell technique are used. In the common-centroid layout technique, the transistors are arranged about a centroid such that the effects of directional linear gradients in the fabrication process are cancelled. For the unit-cell layout technique, all mirror transistors are broken up into several unit-sized transistor and hence the edge effects are identical for all devices and therefore cancel in the ratio of device geometries.

4. SOLUTIONS FOR ELIMINATING CURRENT-FEEDTHROUGH

4.1. Existing Solutions To Current-Feedthrough Problem

To illustrate the effects of current-feedthrough, the switched-current mirror in Fig. 10 was simulated. Figs. 18 and 19 show the current-feedthrough effects obtained from SPICE simulation of the SI switched-current circuit for two different device sizes. It is obvious from these figures that the current-feedthrough is greater for smaller transistor sizes. This is explained from the basic equation Q = CV or $V = \frac{Q}{C}$. For a fixed charge Q, due to the constant switch size, the smaller the capacitor, C, the larger the clock-feedthrough voltage,V. Since current-feedthrough in SI circuits is similar to clock-feedthrough in SC circuits, there have been suggestions to solve this problem [12] by using the dummy switch technique as used in SC circuits, or by using fully-differential structures which cancel the common-mode components of current-feedthrough. Recently, there has been another solution to this problem called "Current-feedthrough cancellation" [6]. Unfortunately, this approach does not work well with small devices nor does it cancel signal-dependent current-feedthrough caused by variation in the input AC signal. In the following section, the operation of each circuit is explained and their SPICE simulation results are shown. Finally, the proposed current-feedthrough cancellation circuit is discussed and its SPICE simulation results are shown.

The SPICE simulation conditions are listed in the table below:

	Amplitude	Frequency
I	100 μA	DC
i	50 μA	1 KHz
Φ	0 - 5 V	20 KHz

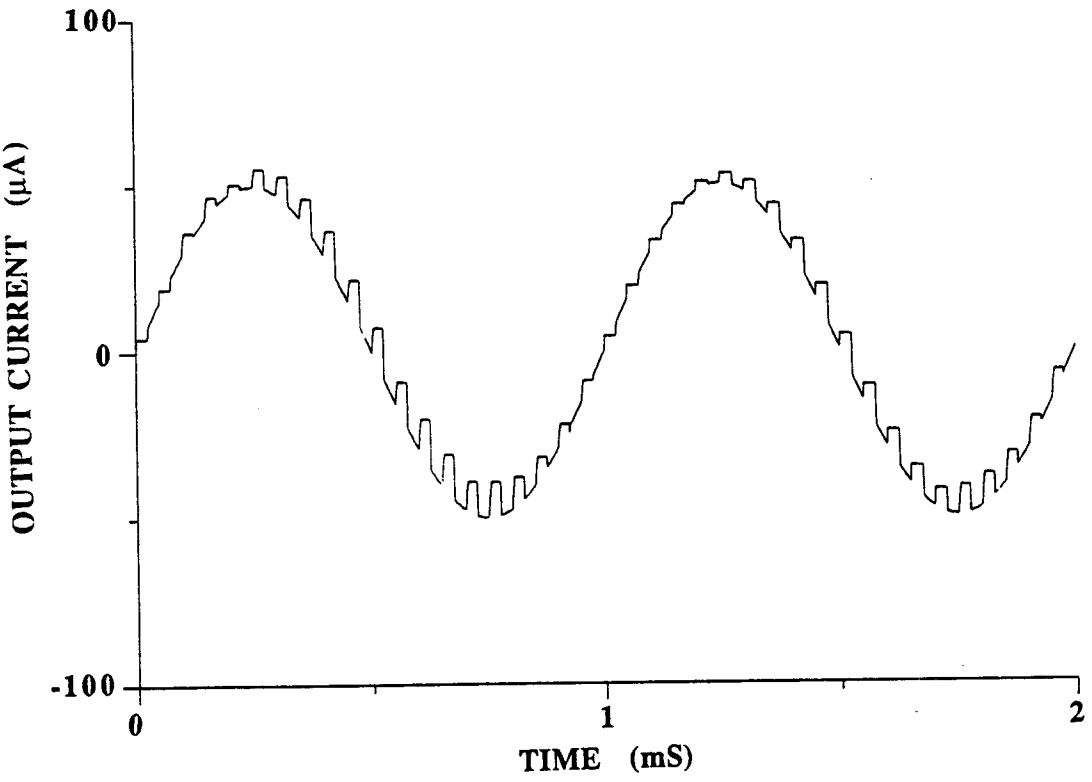


Fig. 18 SPICE simulation of an SI mirror circuit with $\frac{W}{L} = \frac{100\ \mu m}{10\ \mu m}$ and switch $\frac{W}{L} = \frac{3\ \mu m}{2\ \mu m}$

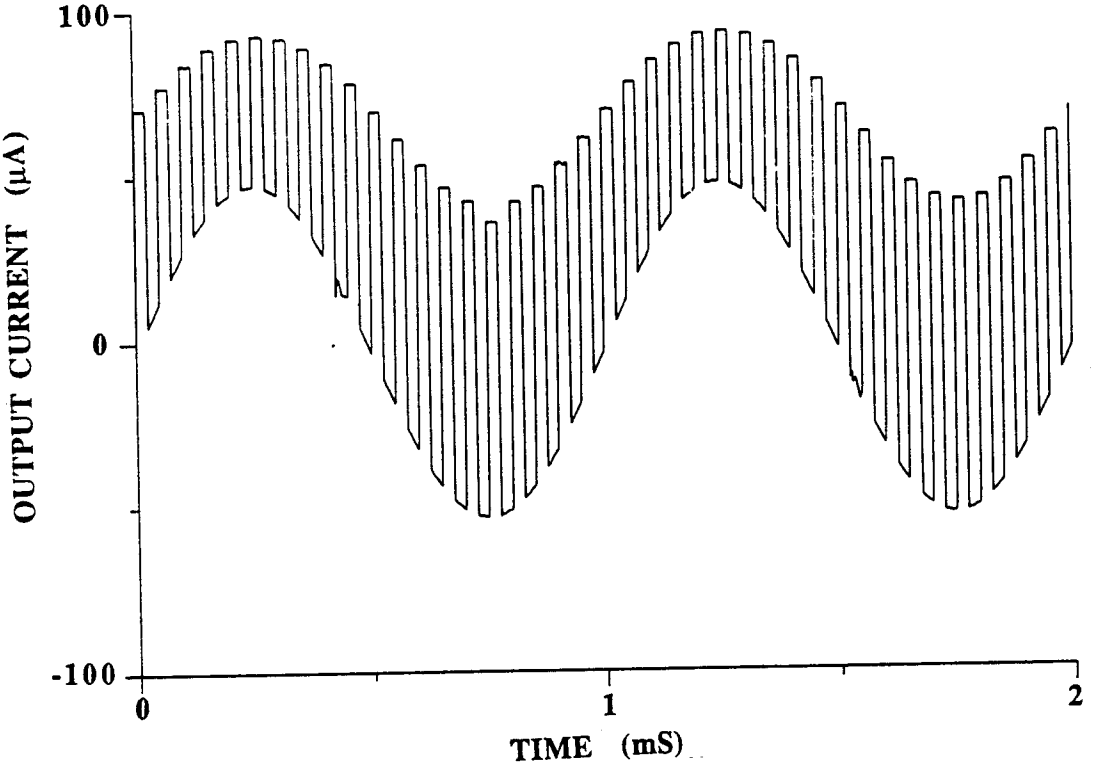


Fig. 19 SPICE simulation of an SI mirror circuit with $\frac{W}{L} = \frac{20\ \mu m}{2\ \mu m}$ and switch $\frac{W}{L} = \frac{3\ \mu m}{2\ \mu m}$

4.1.1. A Dummy Switch Technique

The dummy switch clock-feedthrough cancellation technique applied to SI circuits is illustrated in Fig. 20. SPICE simulation results are shown in Figs. 21 and 22. The circuit is identical to the SI T/H circuit with a dummy switch, MD, added to the right of the main switch, MS. The drain and source of this dummy switch are shorted and the gate is controlled by clock phase opposite to that of the main switch. The idea behind this technique is to have the dummy switch MD turn on and collect the excess charge injected by the main switch MS when it is turned off. Charge cancellation accuracy depends strongly on the precise timing arrangement of both clock phases, which is not easily achievable. From the SPICE simulation results of this circuit, it is clear that this technique is not totally successful for SI circuits due to the signal-dependent source impedance associated with the diode-connected MOSFET M1.

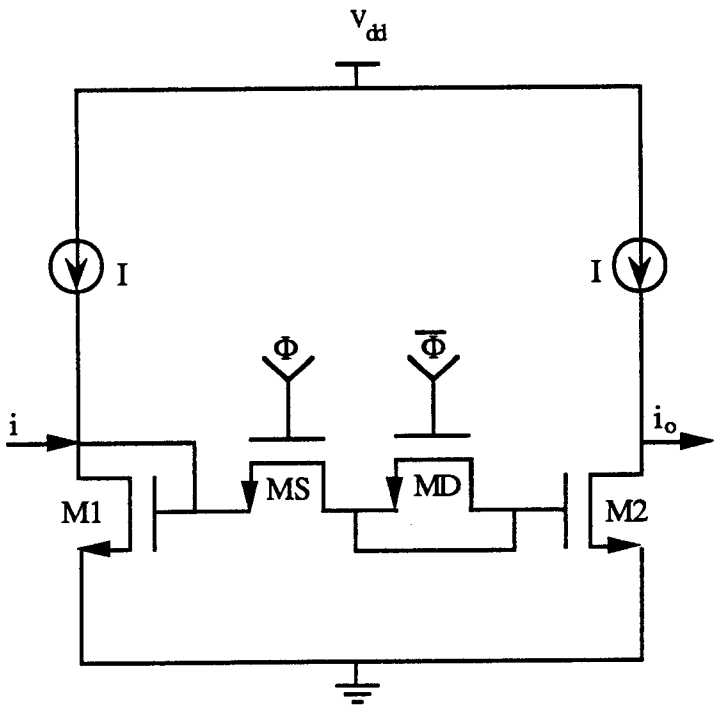


Fig. 20 A dummy switch circuit technique

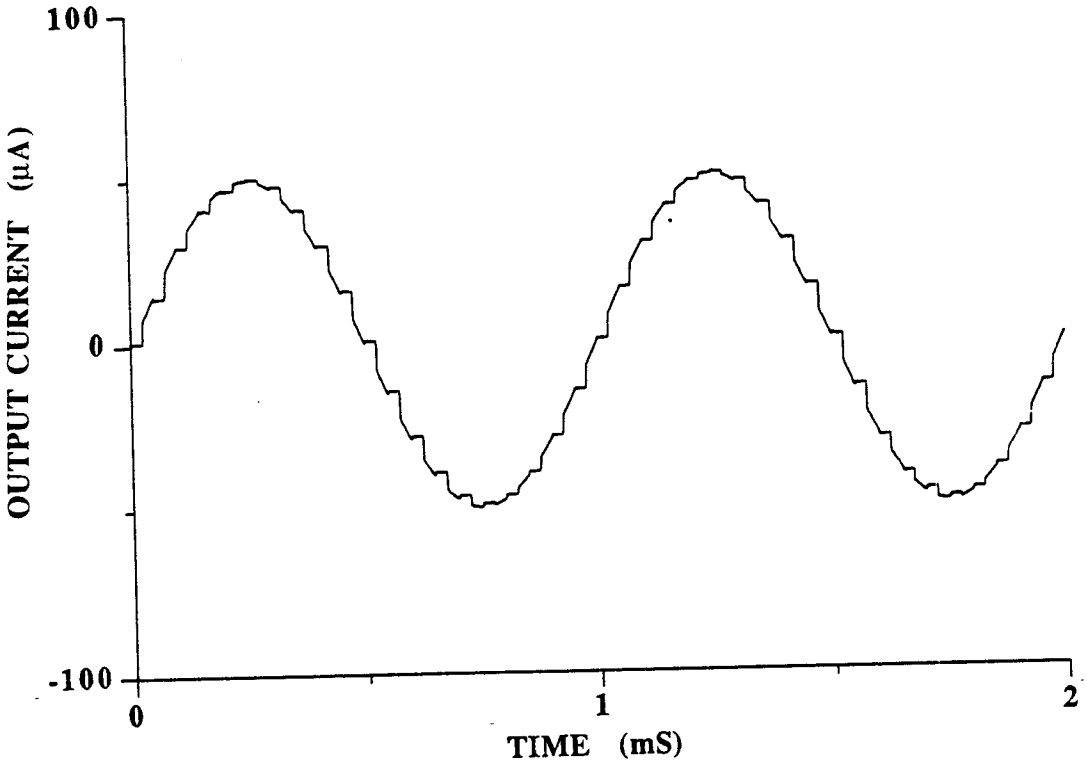


Fig. 21 SPICE simulation of Fig. 20 with $\frac{W}{L} = \frac{100\ \mu m}{10\ \mu m}$ and switch $\frac{W}{L} = \frac{3\ \mu m}{2\ \mu m}$

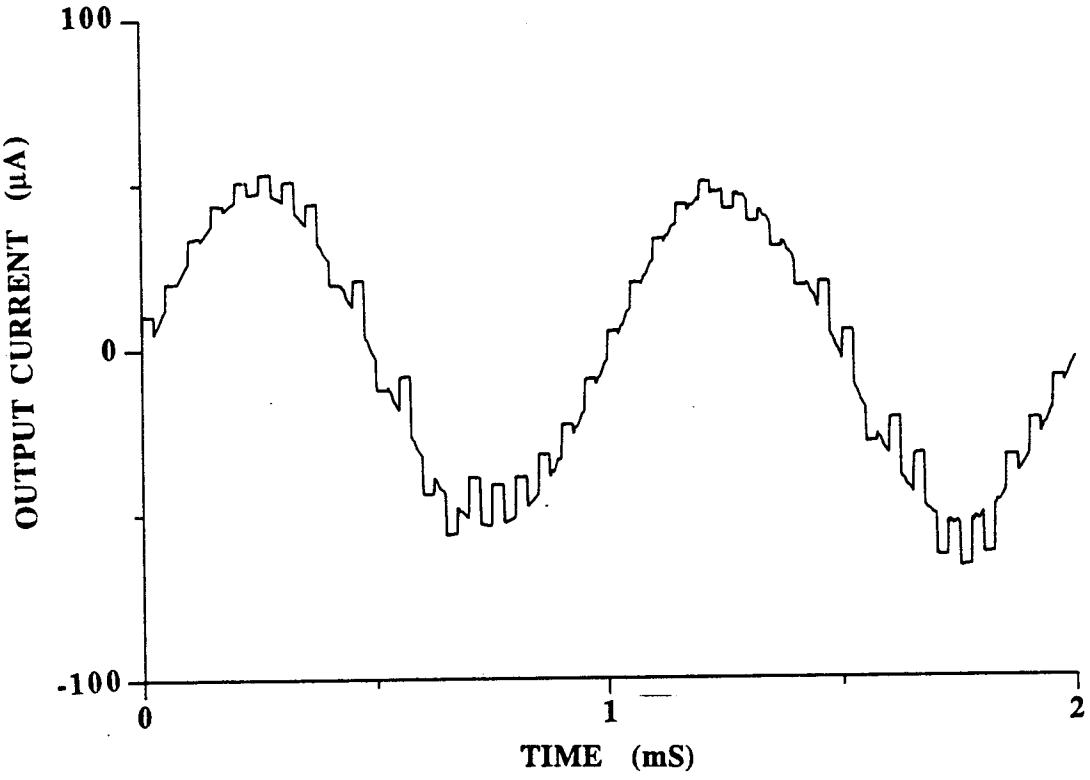


Fig. 22 SPICE simulation of Fig. 20 with $\frac{W}{L} = \frac{20\ \mu m}{2\ \mu m}$ and switch $\frac{W}{L} = \frac{3\ \mu m}{2\ \mu m}$

4.1.2 A Differential Structure Technique

A differential structure has been proposed [12], and the idea is to have the common-mode components of current-feedthrough cancel each other. As mentioned earlier, current-feedthrough in SI circuits is signal dependent. This means current-feedthrough on the positive half cycles is different from that of negative half cycles (see Figs. 18 and 19). Hence the current-feedthrough is not completely cancelled.

4.1.3 Current-Feedthrough Cancellation Technique

Recently, an alternative current-feedthrough cancellation technique has been proposed [6]. This technique eliminates the DC offset part of current-feedthrough, however; it does not eliminate harmonic distortion or current-feedthrough gain errors with a varying input AC signal. Figs. 23, 24, and 25 show the current-feedthrough cancellation circuit and its SPICE simulation results. From Fig. 24, this circuit accurately cancels current-feedthrough if the devices are large. However, for small devices this cancellation technique does not work well. To illustrate this point, device sizes five times smaller was simulated and the results are shown in Fig. 25.

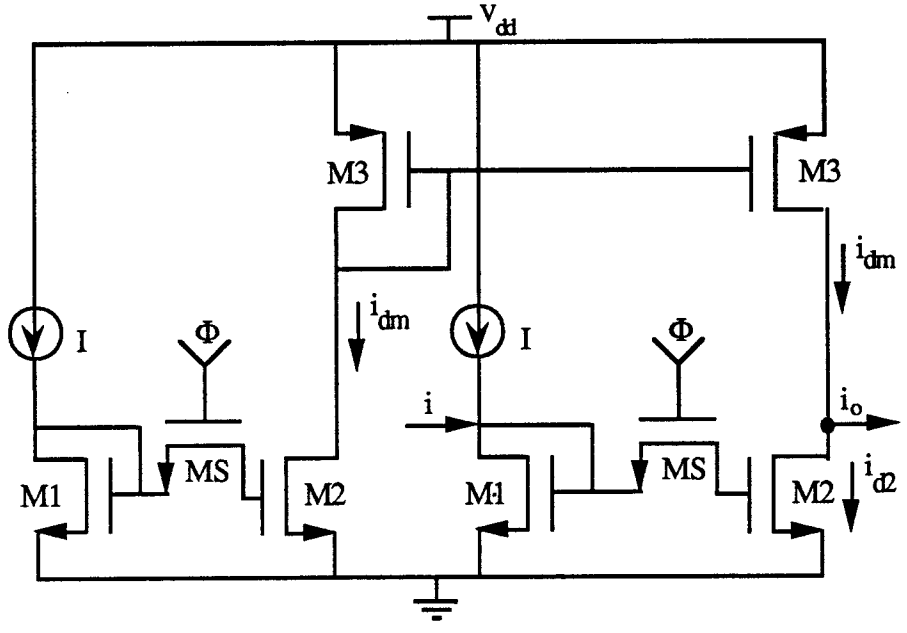


Fig. 23 A current-feedthrough cancellation circuit

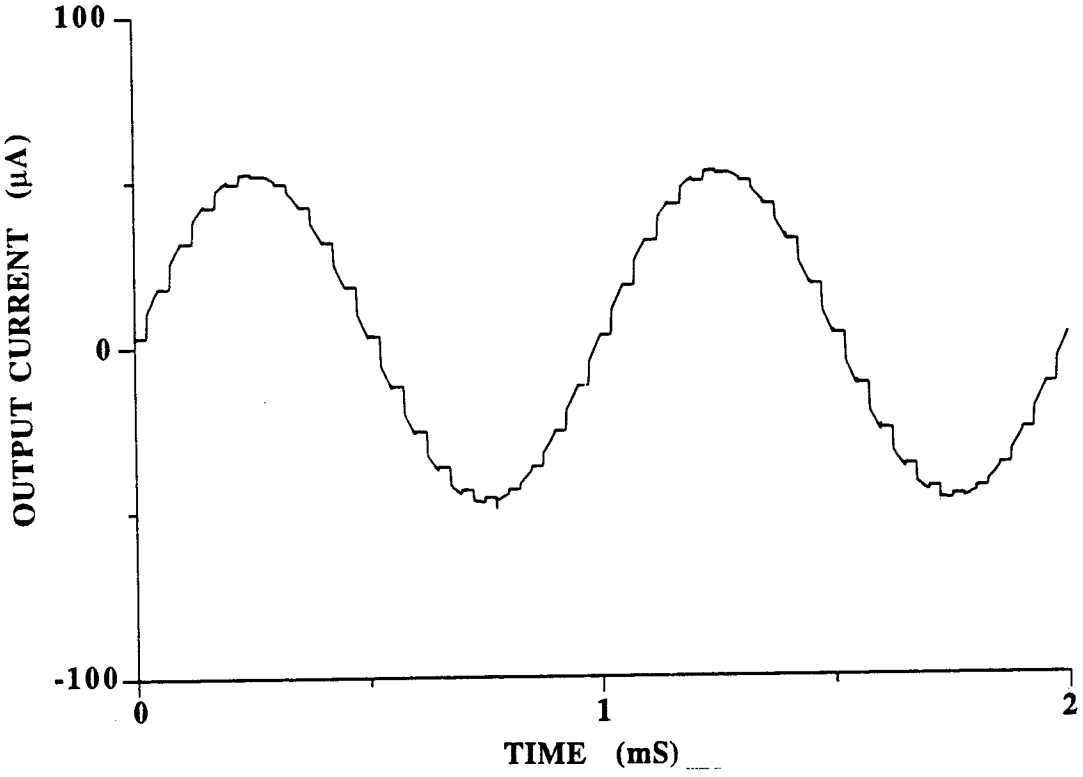


Fig. 24 SPICE simulation of Fig. 23 with $\frac{W}{L} = \frac{100\ \mu m}{10\ \mu m}$ and switch $\frac{W}{L} = \frac{3\ \mu m}{2\ \mu m}$

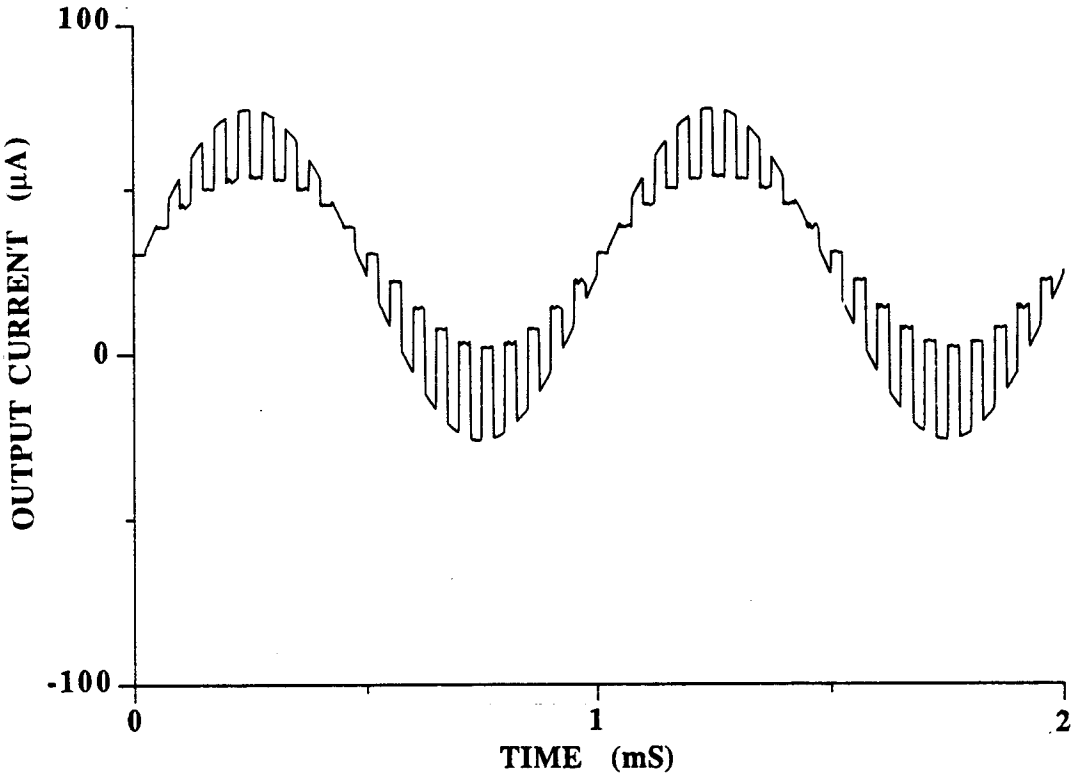


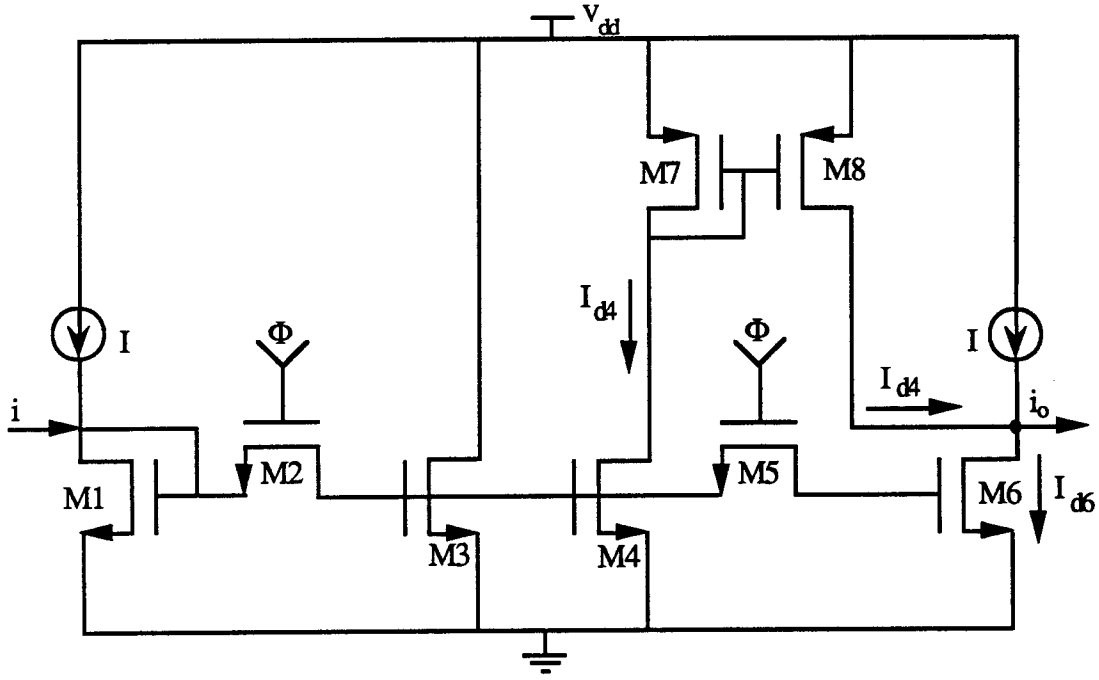
Fig. 25 SPICE simulation of Fig. 23 with $\frac{W}{L} = \frac{20\ \mu m}{2\ \mu m}$ and switch $\frac{W}{L} = \frac{3\ \mu m}{2\ \mu m}$

The basic concept behind this technique is to replicate the amount of current-feedthrough related to the DC bias current, I, and then to mirror this feedthrough current to the output node to be subtracted away. To generate the same amount of current-feedthrough, an exact replica of the current mirror circuit is implemented on the first stage with the mirroring action done by the PMOS mirror on top.

So far, a couple of schemes that was shown either do not completely cancel or only partially cancel current-feedthrough if the devices are large. Based on the above results, it is desirable to develop a better current-feedthrough cancellation technique in order to improve the performance of SI circuits. In the next section, the proposed current-feedthrough cancellation circuit is presented and its operation is analyzed. This technique works well not only for large devices, but also for smaller ones.

4.2. The Proposed Current-Feedthrough Cancellation Circuit

The proposed current-feedthrough cancellation technique for the SI mirror circuit is shown in Fig. 26. The switches M2 and M5 are identical and are controlled by the same clock phase, Φ. Transistors M1, M3, and M4 are identical and M6 has twice the width. M3 acts as a dummy transistor so that the combined capacitance of M3 and M4 is identical to the capacitance of M6. The operation of this circuit is analyzed for two cases; when the switches are on and the switches are off.



M1:M3:M4:M6 = 1:1:1:2

Fig. 26 The proposed current-feedthrough cancellation circuit

Case I: The switches are on

When the switches are on, the equivalent circuit is shown in Fig. 27. Since M4 has the same width as M1, its drain current is equal to the drain current of M1, (I + i), and the drain current of M6 is 2(I + i) because M6 has twice the width of M1. The drain current of M4 is mirrored to the output node. When summing the currents at the output node, the output current is found to be:

$$i_o + I_{d6} - I - I_{d4} = i_o + 2(I + i) - I - (I + i) = 0 \quad (4.1)$$

$$i_o = -i \quad (4.2)$$

So the output current tracks or follows the input current with inversion.

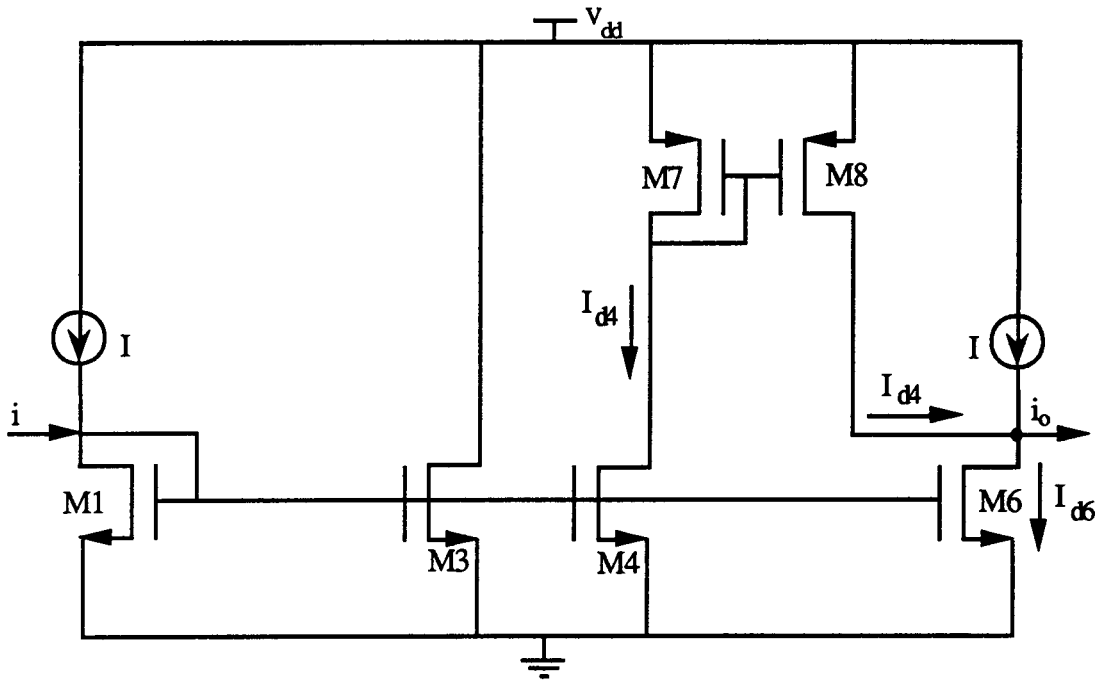


Fig. 27 An equivalent circuit when the switches are turned on

Case II: The switches are off at time t = T

An equivalent circuit is shown in Fig. 28. Just after the switches are turned off, a voltage V_{gs} is stored at the gates of M3, M4, and M6. Assume a charge ΔQ is injected from the switch M5 into the gate of M4 and M6. An equal charge ΔQ is injected into the gates of M3 and M4 from switch M2. So the total voltage injected onto the gate of M4 is $2\Delta V$ and M6 is ΔV. With the above information, the drain current of both transistors, M4 and M6, is calculated as follow:

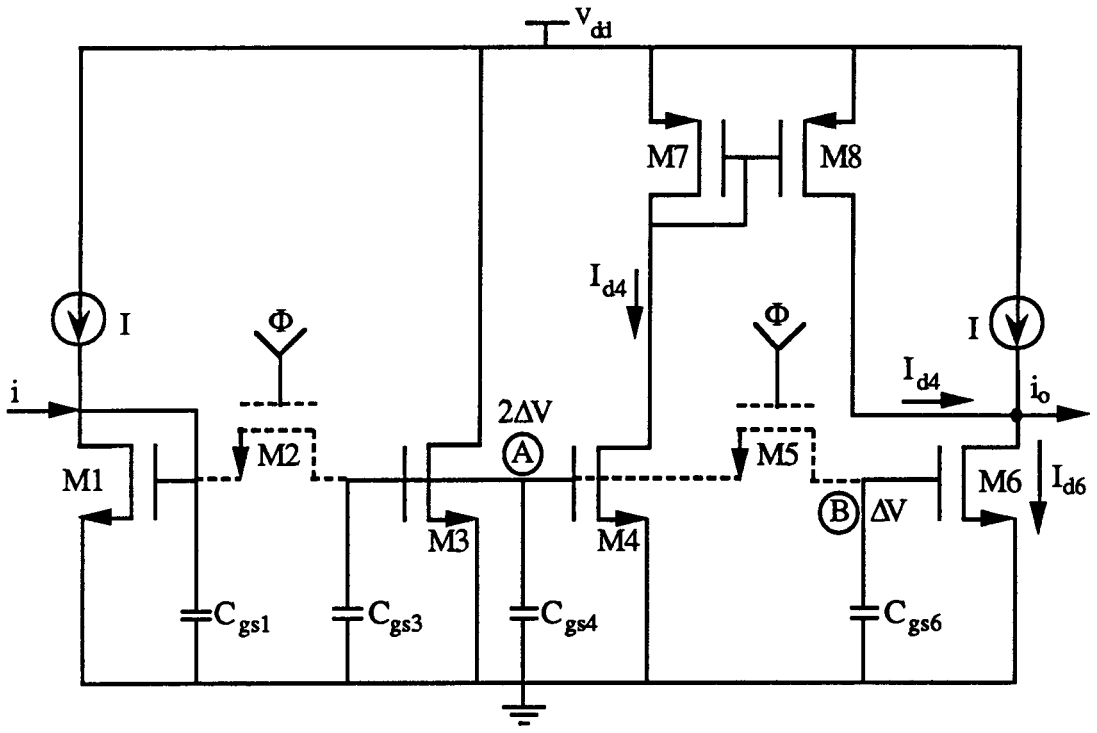


Fig. 28 An equivalent circuit when the switches are turned off

The drain current of M4 at time t = T is

$$I_{d4} = \frac{\beta}{2}\left(V_{gs}(T) - V_t + 2\Delta V\right)^2 \tag{4.3}$$

Where $\beta = K'\left(\frac{W}{L}\right)$.

$$I_{d4} = \frac{\beta}{2}\left[\left(V_{gs}(T) - V_t\right)^2 + 4\left(V_{gs}(T) - V_t\right)\Delta V + 4\Delta V^2\right] \tag{4.4}$$

The drain current of M6 at time t = T is

$$I_{d6} = \frac{2\beta}{2}\left(V_{gs}(T) - V_t + \Delta V\right)^2 \tag{4.5}$$

$$I_{d6} = \frac{2\beta}{2}\left[\left(V_{gs}(T) - V_t\right)^2 + 2\left(V_{gs}(T) - V_t\right)\Delta V + \Delta V^2\right] \tag{4.6}$$

The drain current through M4 is mirrored to and summed at the output node. Applying KCL to the output node gives

$$i_o + I_{d6} - I_{d4} - I = 0 \tag{4.7}$$

$$i_o + \frac{\beta}{2}\left[(V_{gs}(T) - V_t)^2 + 2(V_{gs}(T) - V_t)\Delta V + \Delta V^2\right]$$

$$- \frac{\beta}{2}\left[(V_{gs}(T) - V_t)^2 + 4(V_{gs}(T) - V_t)\Delta V + 4\Delta V^2\right] - I = 0 \tag{4.8}$$

$$i_o + \frac{\beta}{2}\left[(V_{gs}(T) - V_t)^2 - 2\Delta V^2\right] - I = 0 \tag{4.9}$$

$$i_o + \frac{\beta}{2}(V_{gs}(T) - V_t)^2 - \beta\Delta V^2 - I = 0 \tag{4.10}$$

Note that just before the switches are turned off the voltage at the gate of M1 is $V_{gs}(T)$ as are the voltages at the gates of M4 and M6. From the basic MOS equation, the current through the drain of M1 is

$$I_{d1} = \frac{\beta}{2}(V_{gs}(T) - V_t)^2 \tag{4.11}$$

But

$$I_{d1} = I + i(T) \tag{4.12}$$

So

$$I + i(T) = \frac{\beta}{2}(V_{gs}(T) - V_t)^2 \tag{4.13}$$

Substitute equation 4.13 into equation 4.10 results in

$$i_o + I + i(T) - \beta\Delta V^2 - I = 0 \tag{4.14}$$

$$i_o = -i(T) + \beta\Delta V^2 \tag{4.15}$$

From equation 4.15 it is clear that the output current is memorizing or holding the value of input current just before the switch is turned off with a small DC offset error current of $\beta\Delta V^2$. For $\Delta V = 20$ mV with the NMOS W = 20 μm and L = 2 μm, the DC offset error current is 0.179 μA.

The result is obvious that the DC offset error current is small. Most importantly, there are ideally no AC gain errors or harmonic distortion terms using this cancellation technique. So the goal of implementing the current-feedthrough cancellation for SI T/H circuits has been established.

Shown in Figs. 29 and 30 are the SPICE simulation results for the circuit of Fig. 26 with $\frac{W}{L} = \frac{100\ \mu m}{10\ \mu m}$ and $\frac{20\ \mu m}{2\ \mu m}$, respectively. The switches size for both cases are $\frac{W}{L} = \frac{3\ \mu m}{2\ \mu m}$. It is obvious from these results that this circuit performs much better than the other existing schemes that were shown. One main advantage of this technique is that it allows SI circuits to be implemented with small device sizes. Hence, more devices can be fabricated per unit die area.

In the next section, some of the applications that involve the use of this cancellation circuit such as switched-current integrators and switched-current lowpass filters is shown.

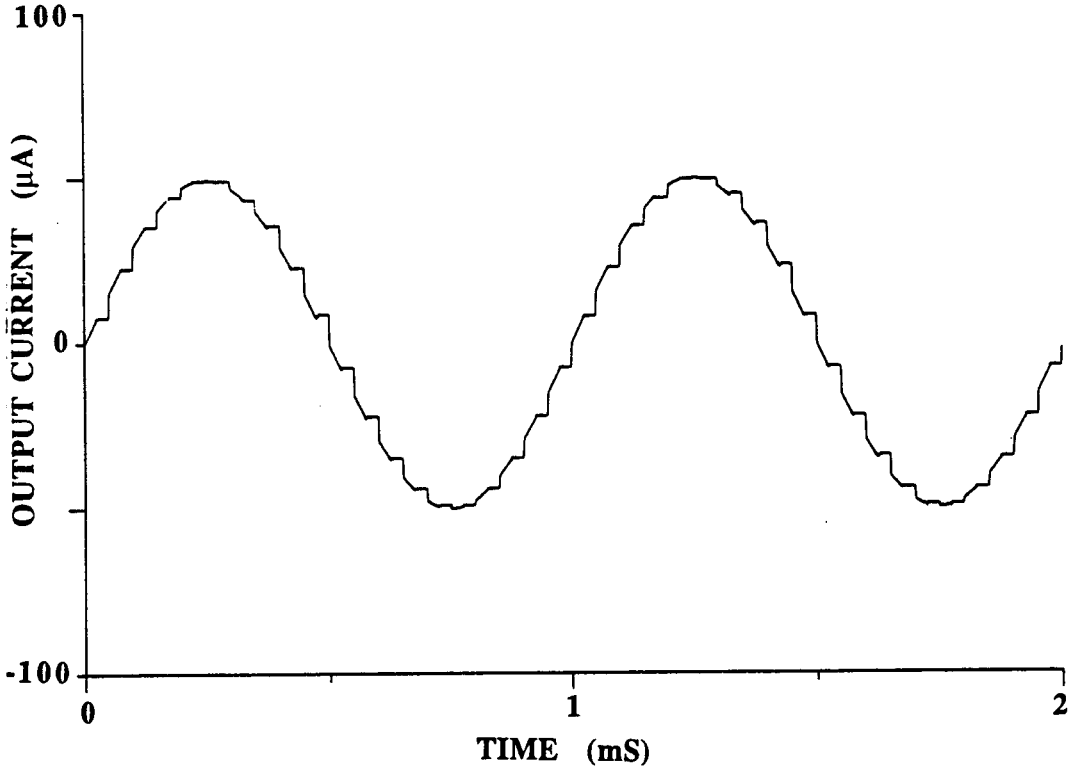


Fig. 29 Spice simulation of Fig. 26 with $\frac{W}{L} = \frac{100\ \mu m}{10\ \mu m}$ and switches $\frac{W}{L} = \frac{3\ \mu m}{2\ \mu m}$

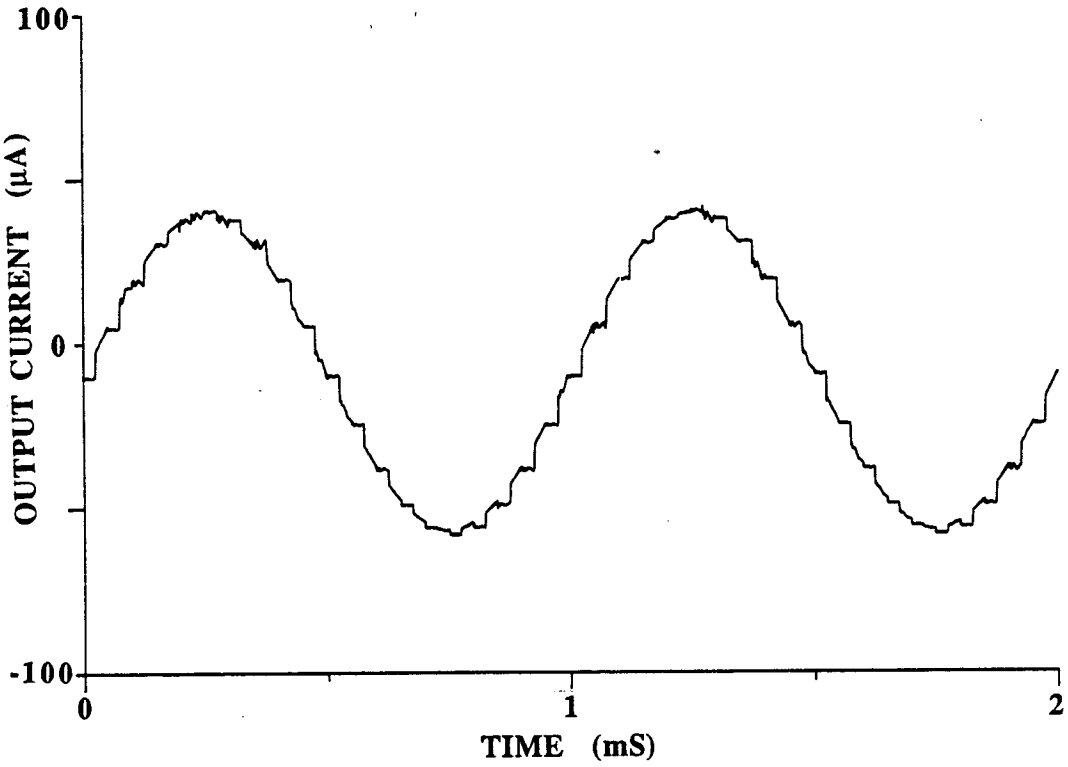


Fig. 30 Spice simulation of Fig. 26 with $\frac{W}{L} = \frac{20\ \mu m}{2\ \mu m}$ and switches $\frac{W}{L} = \frac{3\ \mu m}{2\ \mu m}$

5. APPLICATION OF SI CIRCUITS

5.1. Implementation of SI Integrator Circuits

An integrator circuit is implemented by cascading two T/H circuits with two non-overlapping clock phases Φ and $\overline{\Phi}$ to control the gates of the switches. Fig. 31 shows a current integrator circuit formed by feeding back a portion of the output current from the last stage of T/H SI circuit to the input node. In the z domain, the integrator transfer function is expressed in the form:

$$H(z) = \frac{A_1 + A_2 z^{-\frac{1}{2}} + A_3 z^{-1}}{1 - B z^{-1}} \tag{5.1}$$

Where H(z) is the transfer function of the circuit.

A switched-current integrator is illustrated in Fig. 31. It is easily shown that the circuit in Fig. 31 has the same transfer function as equation 5.1. When the feedback path is broken, at point "X", the equivalent circuit of Fig. 31 is shown in Fig. 32.

$$i z^{-1} + i_f z^{-1} = i_o \tag{5.2}$$

where i_f is the feedback current and z^{-1} represents one period of delay.

$$i_f = i_o \tag{5.3}$$

$$i z^{-1} + i_o z^{-1} = i_o \tag{5.4}$$

$$i_o(1 - z^{-1}) = i z^{-1} \tag{5.5}$$

$$H(z) = \frac{i_o}{i} = \frac{z^{-1}}{1 - z^{-1}} \tag{5.6}$$

It is obvious that equation 5.6 is the same as equation 5.1 with $A_1 = A_2 = 0$, and $A_3 = 1$, and $B = 1$.

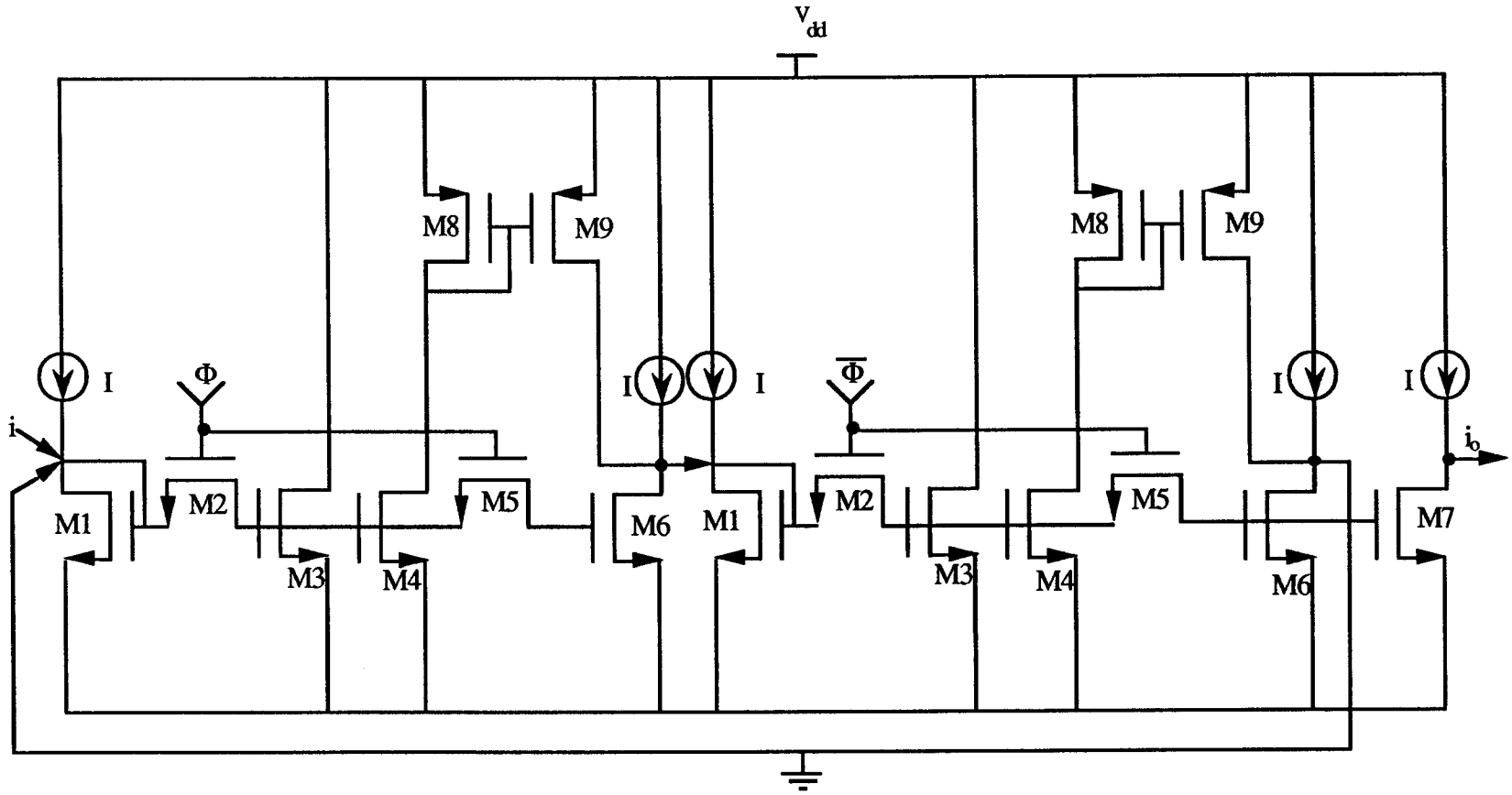


Fig. 31 Switched-current integrator circuit

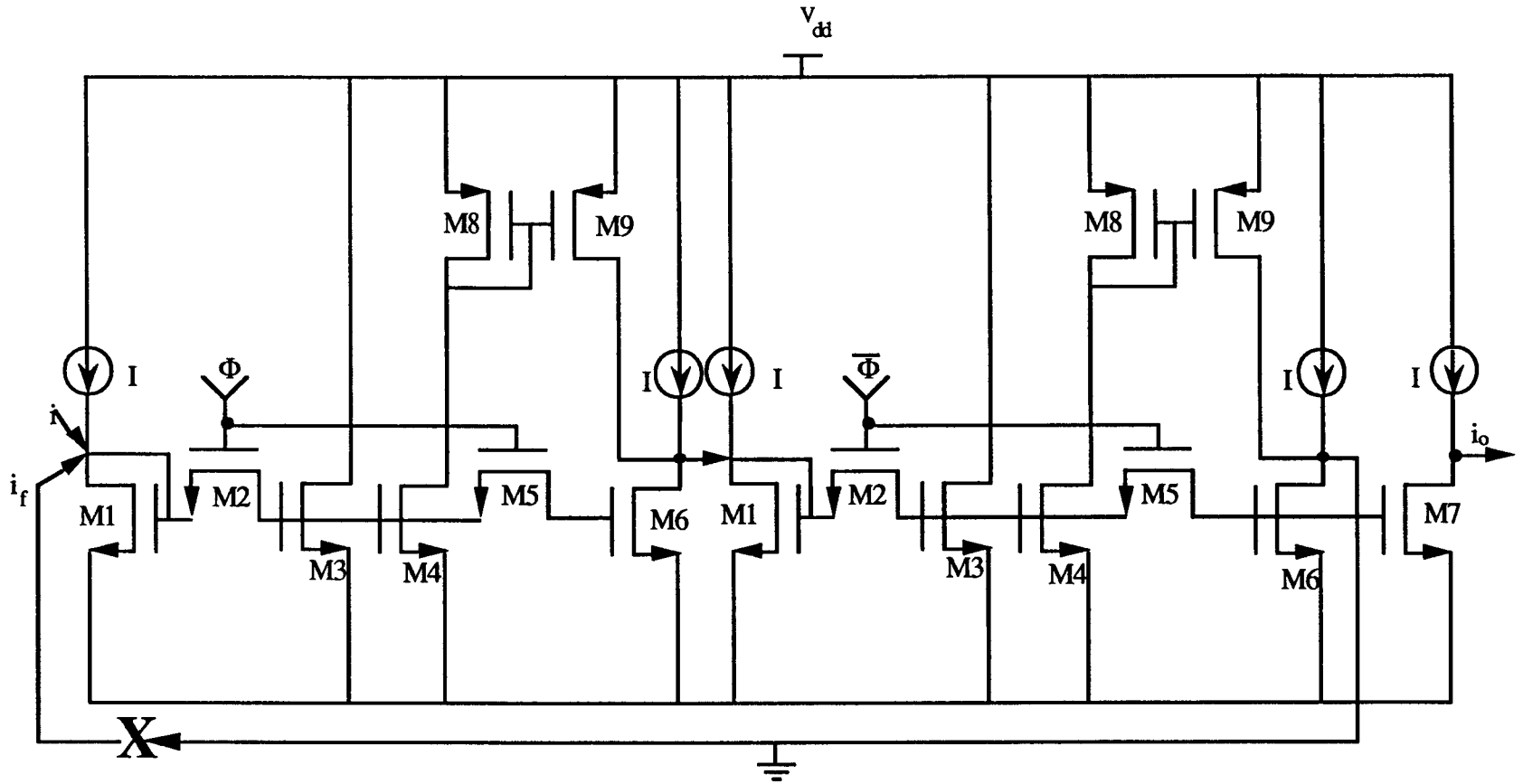


Fig. 32 Switched-current integrator circuit with the feedback path broken

5.2. Implementation Of A Fifth-Order Lowpass Chebyshev SI Filter

To see how this current-feedthrough cancellation circuit performs, two fifth-order lowpass Chebyshev SI filters were implemented with different sizes using a two micron P-well standard CMOS process. High-swing cascode current mirrors were used to design these filters. For the first filter, integrator transistors $\frac{W}{L} = \frac{100\ \mu m}{10\ \mu m}$ and for the switches, $\frac{W}{L} = \frac{3\ \mu m}{2\ \mu m}$. In the second filter, the same switch sizes were used, but the the integrator transistors were $\frac{W}{L} = \frac{20\ \mu m}{2\ \mu m}$.

Signal flowgraph synthesis [13] was used to obtain the integrator scaling factors as in the SC circuit technique. A block diagram of the fifth-order lowpass Chebyshev SI filter is shown in Fig. 33. The two filters were designed for 0.1 dB passband ripple, and a cutoff frequency of 5 KHz when the sampling frequency is 128 KHz.

Fig. 34 shows the layout of the filter which has $\frac{W}{L} = \frac{100\ \mu m}{10\ \mu m}$, and Fig. 35 has $\frac{W}{L} = \frac{20\ \mu m}{2\ \mu m}$. In both of these layouts, the top rows are the P-channel cascode current mirrors, and the next rows are the N-channel cascode current mirrors. Five rows of these pairs are needed to implement the fifth-order lowpass filter with each row representing one pole of the filter.

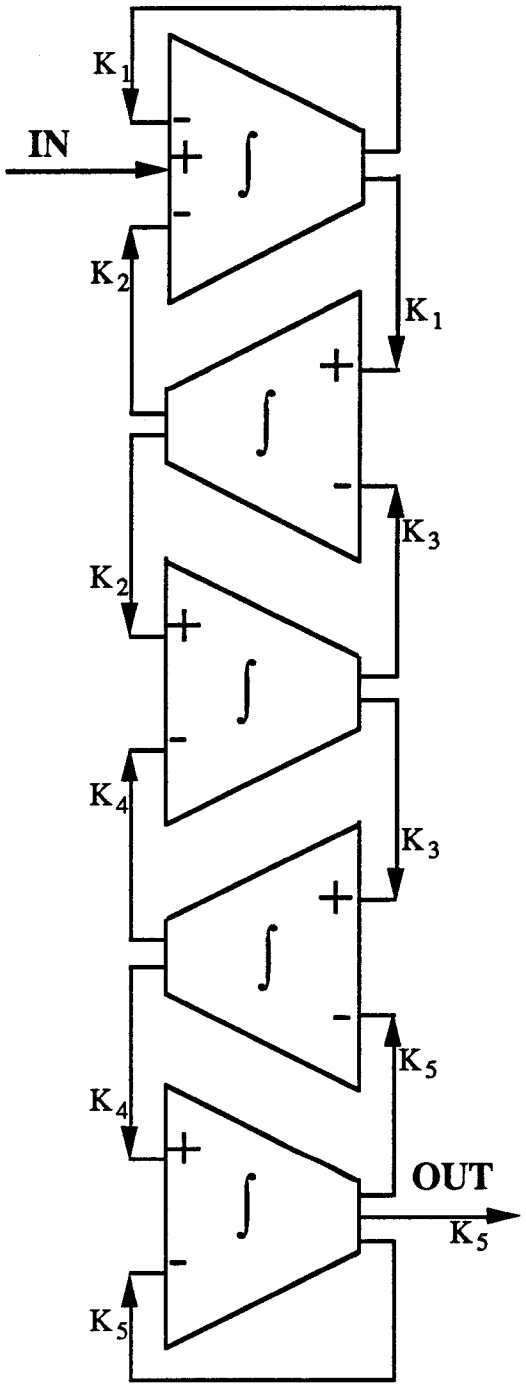


Fig. 33 A block diagram of a five-pole lowpass Chebyshev filter

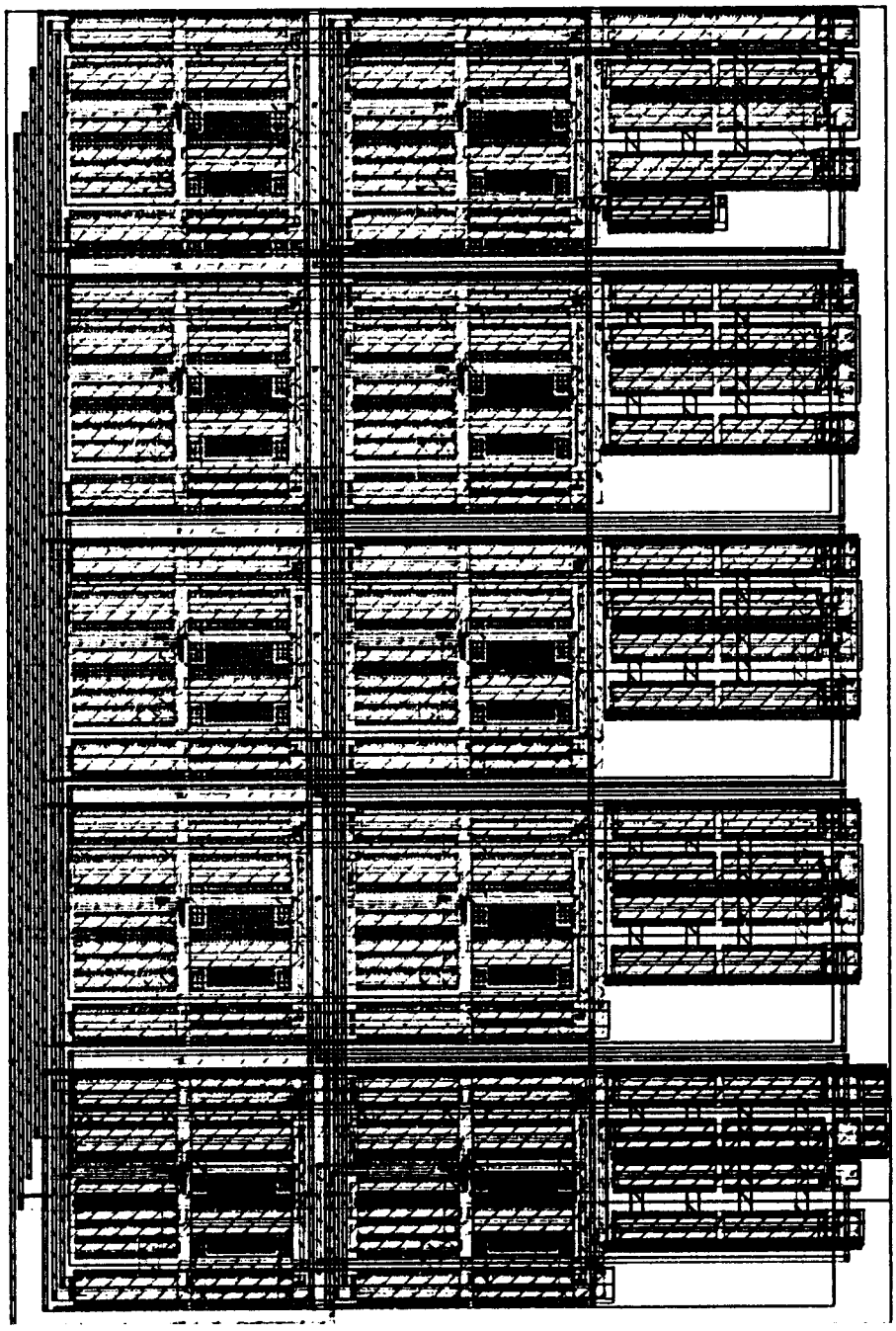


Fig. 34 A chip layout of the five-pole lowpas Chebyshev filter with mirror transistors $\frac{W}{L} = \frac{100\ \mu m}{10\ \mu m}$ and switches $\frac{W}{L} = \frac{3\ \mu m}{2\ \mu m}$

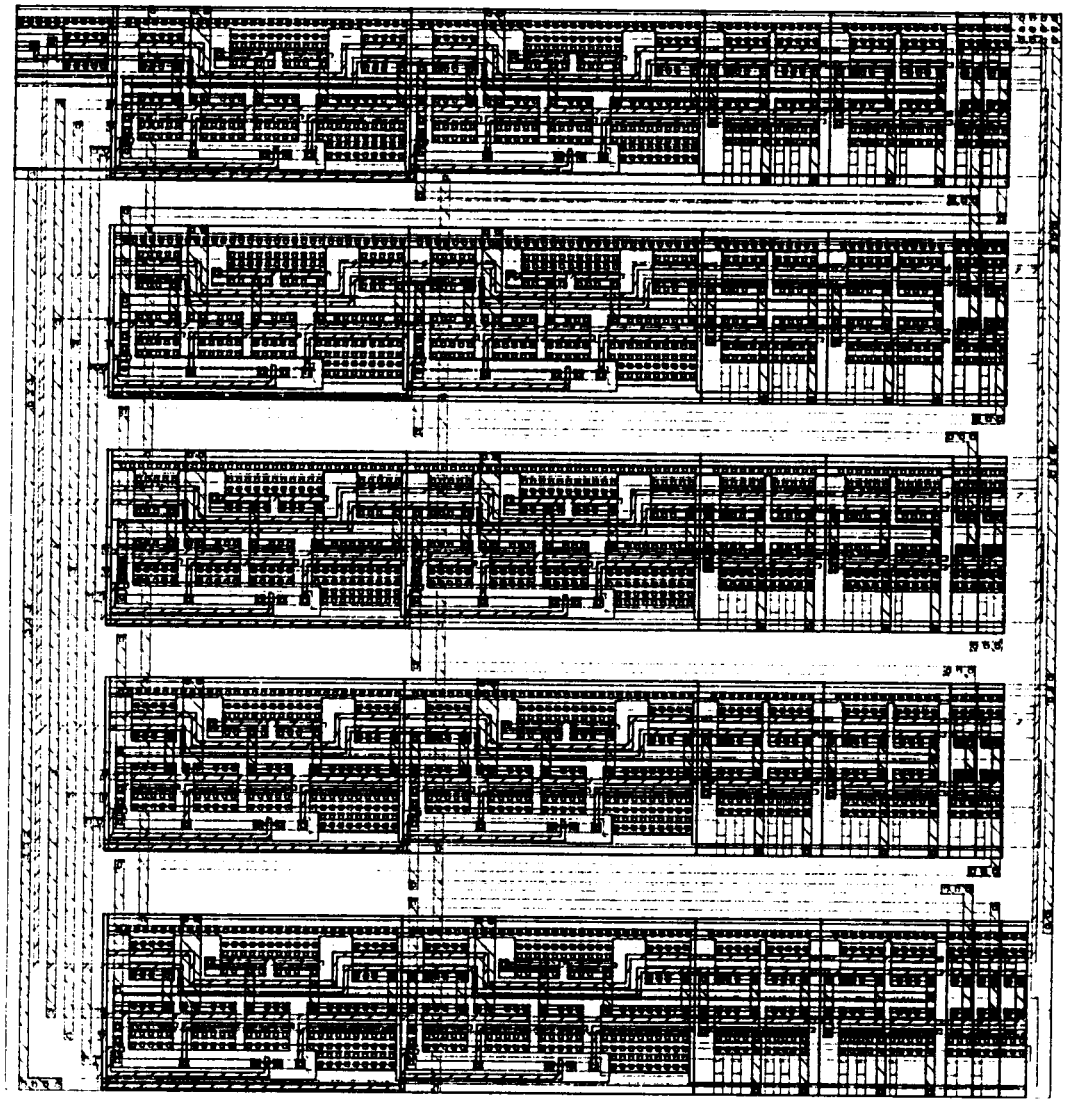


Fig. 35 A chip layout of the five-pole lowpass Chebyshev filter with mirror transistors $\frac{W}{L} = \frac{20\ \mu m}{2\ \mu m}$ and switches $\frac{W}{L} = \frac{3\ \mu m}{2\ \mu m}$

6. CONCLUSIONS

This thesis presented the analysis of current-feedthrough, the effects of current-feedthrough, and the design of current-feedthrough cancellation for SI application. Although the SI circuit technique is very promising for future analog circuit design, there are some performance improvements that must be achieved to make this technique more attractive. Elimination of the current-feedthrough in SI circuits will yield the greatest performance improvement. The SI circuit speed and accuracy will be significantly increased.

The existing schemes that were mentioned cancel current-feedthrough if the area of the mirror transistors is much larger, typically 33 times greater than the area of the switch. With the mirror transistors this large, the capacitances are also large, so the bandwidth becomes small. Hence, to improve the speed and accuracy of SI circuits, a better current-feedthrough cancellation technique must be implemented.

With the goal of having both speed and accuracy, a current-feedthrough cancellation method for SI circuits called current-feedthrough cancellation circuit is developed. This technique allows small mirror transistors, typically 6 times instead of 33 times the area of the switch, to be implemented and still maintains a very small amount of current-feedthrough.

To confirm the performance of this circuit, two different versions $\left(\text{mirror transistors } \frac{W}{L} = \frac{100\ \mu m}{10\ \mu m} \text{ and } \frac{W}{L} = \frac{20\ \mu m}{2\ \mu m}\right)$ of fifth-order lowpass Chebyshev filters were implemented and sent them for fabrication using a two micron P-well CMOS process technology offered by MOSIS. Both filters used the same switch sizes $\frac{W}{L} = \frac{3\ \mu m}{2\ \mu m}$.

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APPENDIX

```
*******************************************
* Main Program used to calculate clock-feedthrough  *
* voltage of the switched-current circuits           *
*******************************************
PHI=1.2;
col=3.2e-15;
CL=824e-15;
GAMMA=0.8759;
VTO=0.93;
global VS ALPHA ;
for i=0:3;
  start=1e6*10^i;
  step=0.5*start   ;
  stop=9.5*start  ;
  for ALPHA=start:step:stop;
    for VS=1.8:0.05:3;
      VT=VTO;
      to=0;
      tfinal=(5-VS-VT)/ALPHA;
      timeend=(5/ALPHA)-tfinal;
      yo=[0 0];
      tol=1e-6;
      trace=0;
       solve=rk45('subpro',to,tfinal,yo,tol,trace);
      si=size(solve);
       x=solve(si(1,1),1);
       y=solve(si(1,1),2);
      vx=-((col*ALPHA*timeend)/(col+CL))+x;
      vy=-(-((col*ALPHA*timeend)/(col+CL))+y)
      logalp=log10(ALPHA);
      m=[m;[VS*3.3 logalp vx vy]];
    end
  end
end
```

```
**********************************************
* Sub-program used to calculate the clock-feedthrough *
* voltage of the switched-current circuits            *
**********************************************
function yprime=subpro(t,y) ;
CL=824e-15;
CI=824e-15;
VH=5;
CG=21.4e-15;
BETA=133.92e-6;
BETACL=BETA/CL;
BETACI=BETA/CI;
VTO=0.93;
GAMMA=0.8759;
PHI=1.2;
VT=VTO+GAMMA*(sqrt(VS+PHI)-(sqrt(PHI)));
A=BETACI*(5-ALPHA*t-VS-3*VT) ;
B=BETACI*(5-ALPHA*t-VS-VT);
CONST=-(CG*ALPHA)/(2*CI);
ESPRIME=A*y(1)+B*y(2)+CONST ;
EDPRIME=B*y(1)-B*y(2)+CONST ;
yprime=[A*y(1)+B*y(2)+CONST ; B*y(1)-B*y(2)+CONST];
```

```
*****************************************
* Sub-program used to solve numerical solution of  *
* ordinary differential equations                  *
*****************************************
function  yout = runge(F, t0, tfinal, y0, tol, trace);
%runge          Integrate a system of ordinary differential equations using
%       4th and 5th order formulas.
% [tout, yout] = runge(F, t0, tfinal, y0, tol, trace)
% INPUT:
% F    - String containing name of user-supplied problem description.
%        Call: yprime = fun(t,y) where F = 'fun'.
%        t     - Time (scalar).
%        y     - Solution column-vector.
%        yprime - Returned derivative column-vector; yprime(i) = dy(i)/dt.
% t0   - Initial value of t.
% tfinal- Final value of t.
% y0   - Initial value column-vector.
% tol  - The desired accuracy. (Default: tol = 1.e-6).
% trace - If nonzero, each step is printed. (Default: trace = 0).
% OUTPUT:
% tout  - Returned integration time points (row-vector).
% yout  - Returned solution, one solution column-vector per tout-value.
% The result can be displayed by: plot(tout, yout).
%   C.B. Moler, 3-25-87.
%   Copyright (c) 1987 by the MathWorks, Inc.
%   All rights reserved.
% The Fehlberg coefficients:
alpha = [1/4  3/8  12/13  1  1/2]';
beta  = [ [   1     0     0    0     0    0]/4
          [   3     9     0    0     0    0]/32
          [ 1932  -7200  7296    0     0    0]/2197
          [ 8341 -32832 29440 -845     0    0]/4104
          [-6080  41040 -28352 9295  -5643    0]/20520 ]';
```

```
gamma = [ [902880  0  3953664  3855735  -1371249  277020]/7618050
          [ -2090  0   22528    21970    -15048  -27360]/752400 ]';
pow = 1/5;
if nargin < 6, trace = 0; end
  if nargin < 5, tol = 1.e-6; end
  % Initialization
  t = t0;
  hmax = (tfinal - t)/5;
  hmin = (tfinal - t)/20000;
  h = (tfinal - t)/100;
  y = y0(:);
  f = y*zeros(1,6);
  tout = t;
  yout = y.';
  tau = tol * max(norm(y, 'inf'), 1);
  if trace
    clc, t, h, y
  end
  % The main loop
  while (t < tfinal) & (h >= hmin)
   if t + h > tfinal, h = tfinal - t; end
     % Compute the slopes
    f(:,1) = feval(F,t,y);
    for j = 1:5
        f(:,j+1) = feval(F, t+alpha(j)*h, y+h*f*beta(:,j));
    end
  % Estimate the error and the acceptable error
  delta = norm(h*f*gamma(:,2),'inf');
  tau = tol*max(norm(y,'inf'),1.0);
  % Update the solution only if the error is acceptable
  if delta <= tau
    t = t + h;
    y = y + h*f*gamma(:,1);
    yout = [yout; y.'];
```

```
  end
  if trace
    home, t, h, y
  end
  % Update the step size
  if delta ~= 0.0
    h = min(hmax, 0.8*h*(tau/delta)^pow);
  end
end;
if (t < tfinal)
  disp('SINGULARITY LIKELY.')
  t
end
```