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The central focus of this thesis is the design, fabrication and characterization of amorphous oxide semiconductor (AOS) thin-film transistor (TFT) current mirrors. The thin-film deposition and circuit fabrication methods used to realize zinc tin oxide (ZTO) TFT current mirrors are addressed in order to elucidate the processing challenges for this material system. Accurate current mirror behavior is demonstrated for current mirrors with small mirroring ratios. Deviations from the ideal mirroring ratio are attributed to three primary sources: TFT geometric mismatch, threshold voltage mismatch, and finite output resistance. The most significant source of mirroring error for the current mirrors fabricated is geometric mismatch associated with processing. Variations in TFT size leading to mirroring error arise from the use of mylar masks, inconsistent channel etching, and lift-off patterning of source-drain contacts. Geometric mismatch must be reduced before the effects of threshold voltage mismatch and finite output resistance on mirroring error can be unambiguously assessed. TFT size variation, and thus mirroring error, can be reduced by using chrome masks, developing an improved channel etch, avoiding lift-off processing and utilizing more sophisticated circuit layout.

The work of this thesis continues to support the use of AOS for a variety of applications. Current mirrors are a vital analog circuit building block, used in a multitude of circuits, without which the scope of AOS-based electronics will be limited. The successful realization of such a circuit in ZTO, despite the processing challenges, bolsters the case that AOS can be used in the next stage of large-area electronics.

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Zinc Tin Oxide Thin-Film Transistor Current Mirror Circuits

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Layannah Elizabeth Feller, Author

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1. INTRODUCTION

Amorphous oxide semiconductors (AOS) have garnered interest as possible material systems for a wide range of novel applications. AOS demonstrate two useful attributes for the development of novel technology: optical transparency and high electron mobility (compared to other amorphous materials). Materials possessing both of these qualities may usher in a new era of transparent electronics in which the possibilities for unique and exciting applications are endless [1]. In order for this technology to become a reality, the development of high performance AOS thin-film transistors (TFTs) and AOS TFT circuits must be achieved. Three examples of AOS used as successful channel layers in TFTs are indium gallium oxide (IGO), indium gallium zinc oxide (IGZO), and zinc tin oxide (ZTO). While each material system has been used to realize high performance TFTs and functioning circuitry, ZTO may be the wisest long-term choice for further development and commercialization because it lacks the expensive indium and gallium components but maintains good electrical performance.

In order for AOS semiconductors to be commercially viable there are several circuit blocks that must be developed. An important example of such a circuit block is the current mirror. In the display industry, current mirrors are used in active-matrix organic light-emitting diode (AMOLED) display pixel circuits to combat the effects of mobility variation between transistors and threshold voltage shifting [2]. Additionally, current mirrors are important blocks in operational amplifiers (opamps) and other complex analog circuitry. Opamps are ubiquitous in current state-of-the-art electronics and are vitally im-

portant for amplification and filtering processes. Without opamps, the scope of transparent electronics will be significantly limited. Work presented in this thesis demonstrates that ZTO can be used to successfully fabricate current mirrors with accurate mirroring performance, in an attempt to further the advancement towards a transparent operational amplifier and ZTO pixel drivers for AMOLED displays.

The structure of this thesis is as follows. Chapter 2 provides background information on the operation of TFTs and current mirrors and a review of the pertinent literature regarding AOS TFTs and circuits. Chapter 3 discusses the processing and characterization methods used to construct and evaluate the TFTs presented in this thesis. Chapter 4 presents the results obtained in the fabrication of a ZTO current mirror. Chapter 5 provides a summary of the conclusions drawn from the research presented, as well as recommendations for future work.

2. LITERATURE REVIEW

This chapter contains the background information needed to provide a framework for the results presented in this thesis. An introduction to amorphous oxide semiconductors is presented first. Thin-film transistor structure and operation is discussed next, followed by an overview of current mirror operation. A summary of previously reported AOS TFTs and AOS circuits is presented. Finally an overview of the operation of AMOLED pixels employing current mirrors and a review of fabricated analog circuits in competing technologies is presented.

2.1 Amorphous Oxide Semiconductors

Development of amorphous oxide semiconductors has its foundation in the report by Hosono et al. of a "working hypothesis" for creating transparent conducting oxides [3], [4]. Hosono proposed that transparent conducting oxides, which were traditionally difficult to create due to the conflicting requirements of transparency and high conductivity, could be realized by use of heavy metal cations (HMCs) with electron configurations of $(n-1)d^{10}ns^0$. These materials have a large degree of direction-independent s-orbital overlap which contributes to a wide conduction band and therefore high mobility, despite the amorphous structure. The AOS herein are composed of multi-component HMCs that are abundant, non-toxic and inexpensive. The use of multiple HMCs serves to frustrate crystallization and keep the material amorphous. The application of cheap, environmentally benign materials make AOS an attractive candidate for large-area electronics applications.

2.2 Thin-film Transistor Structure

Thin-film transistors (TFTs) are constructed by means of depositing thin films of material onto an insulating substrate to create the gate, channel, insulator, and source-drain contacts needed for field-effect transistor (FET) operation. TFTs differ from the traditional metal-oxide-semiconductor-field-effect transistor (MOSFET) structure, in which the semiconductor channel material is embedded in the substrate itself, by having the semiconductor channel material deposited on top of the substrate. Figure 2.1 shows the four common structures for TFTs [5]. The TFT structures are classified by the location of

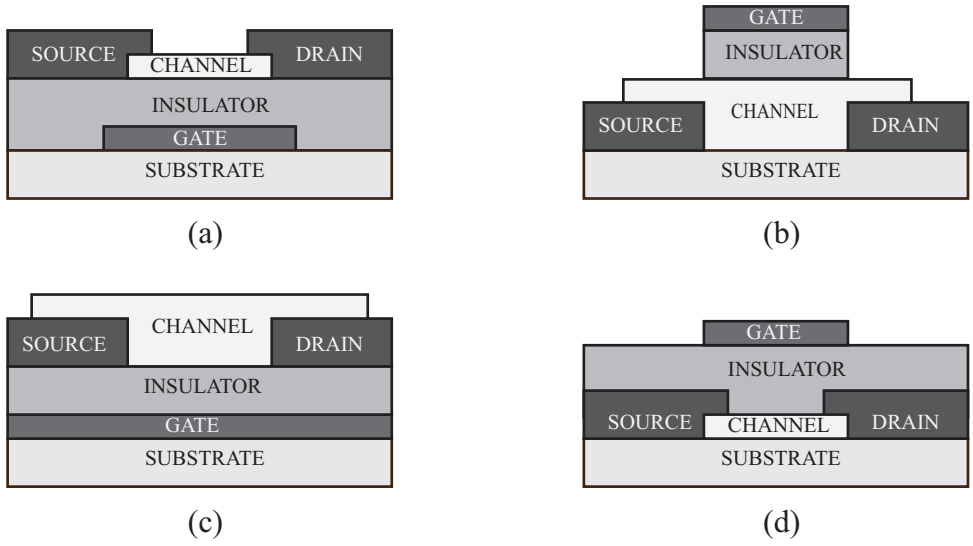


Figure 2.1: The four general TFT configurations: (a) staggered bottom-gate, (b) staggered top-gate, (c) coplanar bottom-gate, and (d) coplanar top-gate.

the gate electrode, either top-gate or bottom-gate, and whether the TFT is in a staggered or coplanar configuration. The staggered TFT is distinguished by having the source and drain contacts on the opposite side of the channel from the insulator. In a coplanar structure the source and drain contacts reside on the same side of the channel as the insulator.

2.3 Thin-film Transistor Operation

TFTs are insulated gate field-effect devices. The current flowing from source to drain is modulated by a gate electrode in the same manner as a MOSFET [6]. To explain how current is modulated in a TFT, one can examine the behavior of a simple MOS capacitor, that constitutes the material stack under the gate electrode of a TFT, which is the transistor control mechanism. Energy band diagrams for the different biasing conditions of the gate control capacitor are shown in Fig. 2.2 [7].

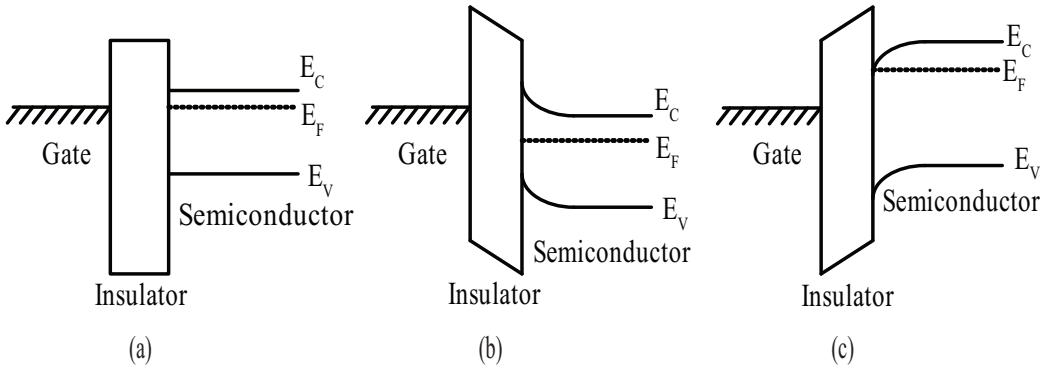


Figure 2.2: Energy band diagram of MOS capacitors under different bias conditions: (a) equilibrium $V_G = 0$ V, (b) depletion $V_G < 0$ V, and (c) accumulation $V_G > 0$ V.

The first condition, depicted in Fig. 2.2(a), is the idealized equilibrium, or flat-band condition. In this state, no bias is applied to the gate electrode, and the device is in equilibrium. A negative bias applied to the gate repels electrons from the semiconductor-insulator interface, thus depleting the region of electrons. This biasing condition, known as depletion, creates a build-up of positive charge at the interface and results in the upwards band bending at the interface seen in Fig. 2.2(b). Conversely, a positive bias to the gate attracts electrons, creating an abundance of negative charge at the interface, leading to the downward band bending depicted in Fig. 2.2(c). This mode of operation is known as accumulation. It is the accumulation of electrons at the semiconductor-insulator in-

terface that provides a conductive path, or a channel, from source to drain in the TFT. Transistor action comes from the modulation of the gate bias that leads to a modulation in the conductivity of the semiconductor channel. The application of a positive voltage to the drain contact, when the channel is in accumulation mode, leads to the extraction of carriers from the channel, via the drain, and thus current flow through the TFT.

With an understanding of the physical mechanisms underlying TFT operation in place, it is now possible to investigate TFT current-voltage relationships. Current flow through the TFT can be classified in one of three categories: cut-off, pre-saturation, and saturation [8]. In cut-off mode, the voltage applied to the gate is less than the voltage required to create a conductive channel, $V_{GS} < V_{ON}$, and no current flows. The device is off. In the pre-saturation regime there is enough bias on the gate to achieve a conductive channel. The conditions for the pre-pinch-off regime are $V_{GS} > V_{ON}$, where V_{ON} is the minimum voltage necessary to achieve a conductive channel and non-negligible drain current, and a small positive drain voltage, $V_{DS} < V_{GS} - V_{ON}$, to set up current flow [9]. Under this condition the drain current can be modeled as,

$$I_D = \frac{W}{L}\,\mu\,C_{ox}\left[(V_{GS} - V_{ON})V_{DS} - \frac{{V_{DS}}^2}{2}\right], \tag{2.1}$$

where C_{ox} is the gate capacitance density, μ is the mobility of electrons in the channel, and W and L are the gate width and length, respectively.

The last mode of operation is saturation. In TFTs, saturation occurs via pinch-off when the channel becomes depleted of carriers in the vicinity of the drain. When pinch-off occurs, the current through the TFT no longer increases with increasing V_{DS} and the current saturates. The saturation current is independent of drain voltage and can be obtained by substituting in the minimum drain voltage necessary to achieve pinch-off,

$V_{DSAT} = V_{GS} - V_{ON}$, into the pre-saturation expression for drain current given by Eq. 2.1

$$I_D = I_{DSAT} = \frac{1}{2}\frac{W}{L}\,\mu\, C_{ox}(V_{GS} - V_{ON})^2. \tag{2.2}$$

Note the use of V_{ON} to define the TFT operation regimes. While many formulations of transistor operation use the more common threshold voltage parameter, V_{TH}, for AOS TFTs the turn-on voltage, discussed in greater detail in Sec.3.6.2 is preferred. The turn-on voltage is a less ambiguous physical, instead of model, parameter that correlates to the onset of non-negligible drain current.

2.3.1 Thin-Film Transistor Channel Length Modulation

A more thorough discussion of pinch-off and the associated channel length modulation effect is presented in order to provide context for the estimation of TFT output resistance. Consider a TFT biased with $V_{GS} > V_{ON}$ and $V_{DS} < V_{GS} - V_{ON}$, i.e the pre-saturation condition. The voltage between the source and the drain is 0 V at the source increasing across the length of the channel until it reaches V_{DS} at the drain. In this case the voltage developed between the gate and the channel at a location near the grounded source is $V_{GS} - 0V$. The voltage developed between the gate and the channel at a location near the drain however, is $V_{GS} - V_{DS}$ which is less than the voltage in the channel near the source. The electric field extending between the gate and the channel that attracts electrons to create an accumulation layer is stronger at the source than at the drain as depicted in Fig. 2.3.

As V_{DS} increases, the concentration of electrons in the accumulation channel near the drain decreases until the accumulation layer is extinguished and the channel is depleted near the drain. Under ideal operation, the spatial extent of the depleted portion of the electron accumulation layer is much less than the gate length. For this case an

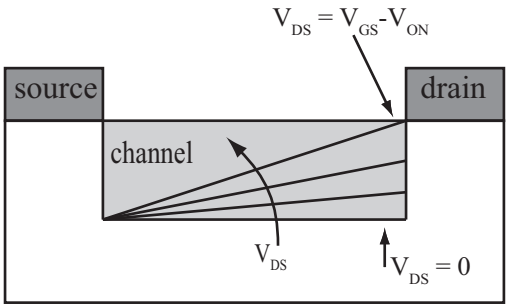


Figure 2.3: Channel profile as the drain-to-source voltage increases. Once $V_{DS} > V_{DSAT} - V_{ON}$ pinch-off occurs and there is no channel accumulated next to the drain.

$I_D - V_{DS}$ curve will exhibit hard saturation in which I_{DS} is always constant with respect to increasing V_{DS}.

Ideal hard saturation is rarely observed in ZTO TFTs. Only at small applied gate voltages is nearly ideal behavior seen. At larger applied gate voltages ZTO TFTs typically exhibit softer saturation, in which I_D increases slightly with increasing V_{DS}, even though $V_{DS} > V_{DSAT}$. As V_{DS} increases, the pinch-off point moves towards the source [10]. The excess applied voltage of $V_{DS} - V_{DSAT}$ drops across the depleted portion of the channel between the pinch-off point and the edge of the drain. This depletion region encroaches into the channel and reduces L by ΔL. The shrinking channel length with the application of V_{DS} in excess of V_{DSAT} leads to an increase in current since I_D is inversely proportional to the effective channel length defined by the edge of the source and the pinch-off point. Quantitatively, this soft saturation associated with channel length modulation can be accounted for by replacing the channel length L with $L - \Delta L$ in the saturation current

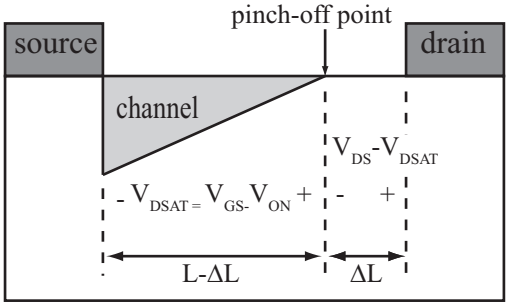


Figure 2.4: Channel profile of the accumulated carriers as the drain-to-source voltage increases past the saturation value, creating a depletion region near the drain which reduces the channel length by ΔL.

expression [11],

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L-\Delta L}(V_{GS}-V_{ON})^2 \tag{2.3}$$

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_{ON})^2\left(\frac{1}{1-\frac{\Delta L}{L}}\right) \tag{2.4}$$

because $\Delta L/L$ is < 1, a series expansion can be used on the final term of Eq. 2.4. Keeping the first two terms of the expansion,

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_{ON})^2\left(1+\frac{\Delta L}{L}\right). \tag{2.5}$$

Assuming that ΔL is proportional to V_{DS} then $\Delta L = \lambda' V_{DS}$ where λ' is the proportionality constant,

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_{ON})^2\left(1+\frac{\lambda'}{L}V_{DS}\right). \tag{2.6}$$

Defining λ'/L as the process parameter λ,

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_{ON})^2(1+\lambda V_{DS}), \tag{2.7}$$

The parameter λ has units of V^{-1} and is proportional the the degree of channel shortening induced by channel length modulation. Equation 2.7 describes the linear dependence of I_D on V_{DS}, for voltages greater than V_{DSAT}, that leads to a non-saturating current.

The Early voltage is sometimes specified instead of λ in defining transistor process parameters. If the straight-line current-voltage characteristics are extrapolated backwards from the output curves, ideally the lines will converge to a point on the negative voltage axis, as seen in Fig. 2.5. This point is the negative Early voltage, $-V_A$. At the Early voltage $I_D = 0$. Based on Eq. 2.7 this condition occurs when $V_{DS} = -1/\lambda$. The Early voltage is the inverse of the channel length modulation parameter,

$$V_A = 1/\lambda. \tag{2.8}$$

Early voltage, V_A, is proportional to the effective length of the channel, i.e., as the channel

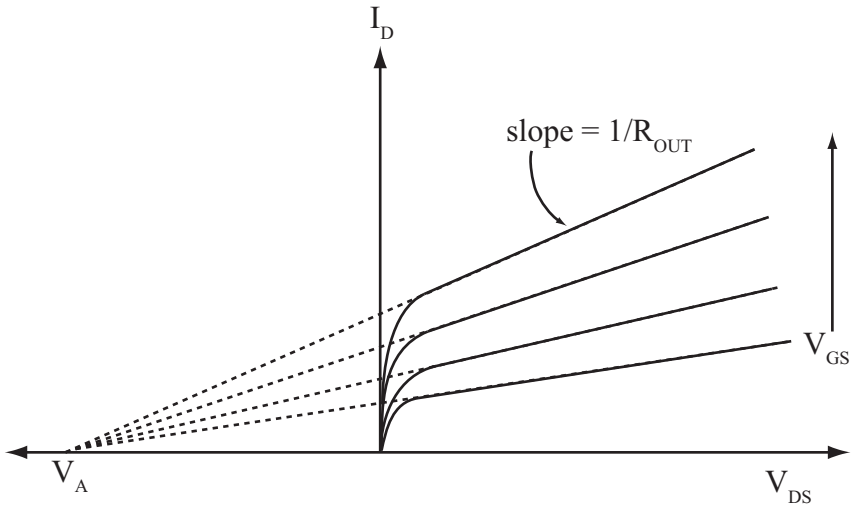


Figure 2.5: The parameter V_A can be extracted from the TFT output curves by extrapolating the straight-line portion of the curves back to the x-axis. The voltage they converge at is the Early voltage, V_A and is a parameter describing channel length modulation.

shrinks so does the Early voltage, so larger values of V_A are desired. TFT output resistance r_o is generally defined as the Early voltage divided by the ideal drain current [12],

$$r_o = \frac{V_A}{I_D}. \tag{2.9}$$

2.4 Current Mirror Operation

Current mirrors are used extensively in analog circuit applications to bias the multiple amplification stages needed for IC design [11]. A reference current is generated at one point in the circuit and is then reproduced, or mirrored, to the amplification stages requiring bias currents. Figure 2.6 is a schematic of the typical 2-TFT current mirror. The

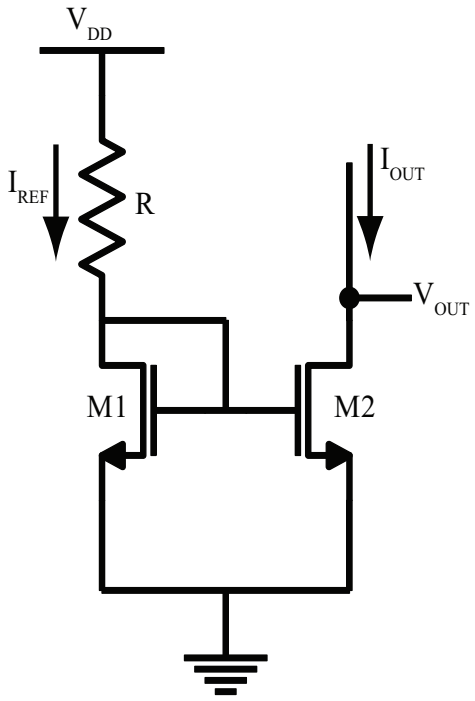


Figure 2.6: 2-TFT current mirror circuit. The saturation current of M1, set by V_{DD} and R is mirrored in the transistor M2 to create the output current.

transistor M1 is diode-tied, characterized by the connection of the gate and drain. A diode tied transistor is forced to operate in saturation. The saturation current through M1 is

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}(W/L)_1(V_{GS} - V_{TH})^2, \tag{2.10}$$

where μ_n is the electron mobility, C_{ox} is the gate capacitance density, W and L are the transistor width and length respectively, and V_{TH} is the threshold voltage. The threshold

voltage is used in the discussion of current mirror operation, rather than turn-on voltage, because it is the more common circuit design parameter. The current through M1 is set by an independent current source or the resistor R and the supply voltage V_{DD} by the relationship

$$I_{D1} = I_{REF} = \frac{V_{DD} - V_{GS}}{R}. \tag{2.11}$$

The voltage between the gate and source for both M1 and M2 is equal, therefore, if M2 is forced to operate in saturation by setting the voltage V_{OUT} to be sufficiently high, $V_{OUT} > V_{GS} - V_{TH}$, then the saturation current of M2 is given by

$$I_{D2} = I_{OUT} = \frac{1}{2}\mu_n C_{ox}(W/L)_2(V_{GS} - V_{TH})^2. \tag{2.12}$$

Relating Eqs. 2.10 and 2.12 the relationship between the reference current and the output current can be established as

$$\frac{I_{OUT}}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1}. \tag{2.13}$$

From Eq. 2.13 it is evident that, by varying the sizes of M1 and M2, any value of output current can be generated from the input current, and the output current can then be used to bias different parts of the analog circuit.

The output resistance of this simple current mirror is equal to the intrinsic output resistance of the transistor M2. The output resistance of a transistor is determined by the channel length modulation effect. The resistance is shown to be,

$$R_{OUT} = r_{o2} = \frac{V_{A2}}{I_{OUT}}, \tag{2.14}$$

where V_{A2} is the Early voltage of M2, related to channel length modulation, and I_{OUT} is the output current through M2.

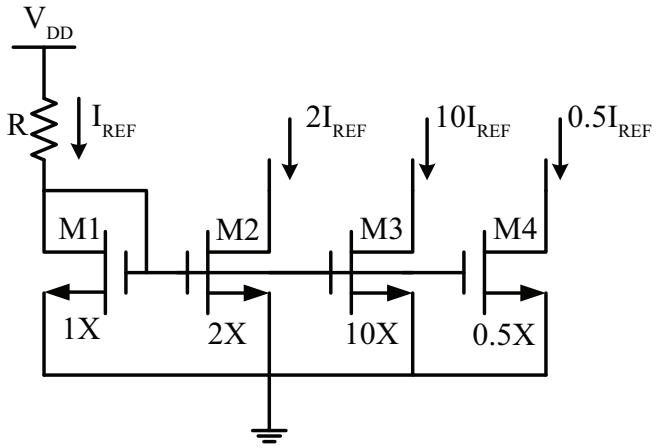


Figure 2.7: A multiple branch current mirror, illustrating how many currents can be mirrored at different values off one reference transistor.

The minimum output voltage needed to keep transistor M2 in saturation can be found by rearranging the saturation current for M2,

$$V_{OUT,min} = V_{GS} - V_{TH2} = \sqrt{\frac{2I_{OUT}}{\mu C_{ox}(W/L)_2}}. \tag{2.15}$$

More output transistors can be connected in parallel to M2 to create many branches of mirrored current from the one reference current, as shown in Fig. 2.7. The nomenclature for current mirrors is to label the reference W/L ratio of M1 with a 1X. Subsequent mirroring transistor W/L ratios are then specified as multiples of the reference ratio. Therefore the mirroring ratio can be expressed as a multiplication of the input current, i.e., 1X, 2X, 5X. This clarifies that the current through each mirror branch is equal to the reference current times the multiplication factor, as shown in Eq. 2.13.

2.4.1 Variations on the Current Mirror

There are several variations of the simple current mirror presented in section 2.4. This section presents a brief overview of two common types of advanced current mirrors, the cascode current mirror and the Wilson current mirror, attempted in this research.

2.4.1.1 Cascode Current Mirror

In IC design there are many types of amplification circuits. One such circuit is the cascode amplifier. This amplifier combines the high input resistance and large transconductance of a common-source amplifier with the high-frequency response of a common-gate amplifier [11]. Such an amplifier requires a cascode current source to maintain the correct output resistance needed to achieve high gain. Therefore a cascode current mirror is implemented to provide current to the amplifier. The operation of the cascode current mirror is essentially the same as the traditional current mirror with the exception that the required voltage to keep transistor M2, and now M4, in saturation is increased from $V_{GS} - V_{TH}$ to $V_{OUT} > V_{TH} + 2(V_{GS} - V_{TH})$. The addition of the cascode transistor, M4, increases the output resistance of the current mirror by the intrinsic gain of M4,

$$R_{OUT} \cong g_{m4} r_{o4} r_{02}. \tag{2.16}$$

Increased output resistance is an important advantage of the more complicated current mirror designs. The output resistance has an effect on the performance of the circuits that utilize current mirrors. The higher the output resistance, the less dependance the output current has on output voltage. This is desirable so that the current mirror will always deliver the correct current to the load.

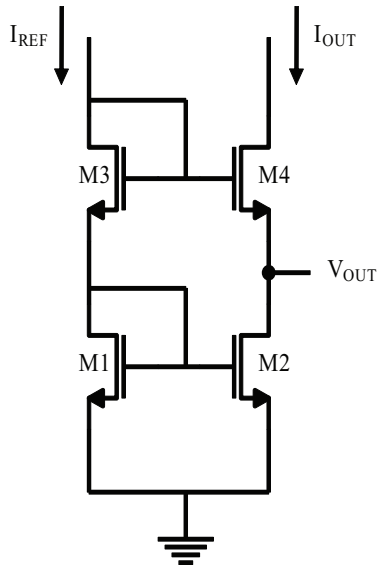


Figure 2.8: The cascode current mirror

2.4.1.2 Wilson Current Mirror

A second variation of the current mirror is the Wilson current mirror. Like the cascode current mirror, the Wilson current mirror has an increased output resistance over the traditional 2-TFT configuration. The output resistance of the Wilson mirror is $R_{OUT} \cong g_{m4}r_{o4}r_{o2}$, the same as that of a cascode current mirror [11]. A second benefit of the Wilson current mirror is the built-in feedback that resists changes to the output current due to changes in the load. To illustrate this point, suppose the output current I_{OUT} in Fig. 2.9 were to rise due to a changing load condition. This would cause the drain-to-source voltage of transistor M1, V_{DS1}, to rise as well. Since the gate of M2 is tied to the drain of M1 V_{GS2} also rises. The increase in gate voltage would normally lead to an increase in drain current. However, the drain current for M2 is set by the current source I_{REF} which cannot change. Therefore, V_{DS2} must fall to compensate, and with it V_{GS3} which is tied

to the drain of M2. With the gate voltage of M3 lowered, I_{OUT} is also lowered and the original increase in I_{OUT} is compensated for. The same analysis can be undertaken in the situation of a falling output current. A Wilson current mirror establishes a negative feedback loop which maintains a constant output current despite changes to the load.

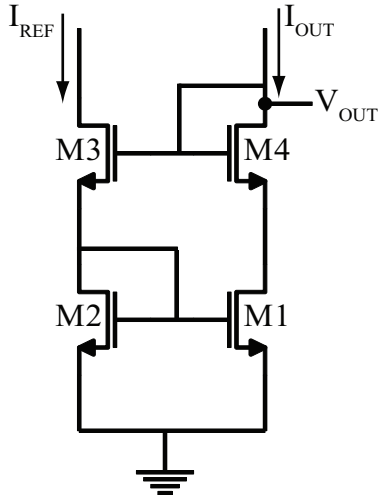


Figure 2.9: The Wilson current mirror has improved output resistance and feedback that resists changes in output current due to output voltage.

Like the cascode, the minimum output voltage needed to keep transistors M2 and M4 in saturation is $V_{TH} - 2(V_{GS} - V_{TH})$. Plugging Eq. 2.15 in to the minimum output voltage yields,

$$V_{OUT,min} = V_{GS} - V_{TH2} = V_{TH} - 2\sqrt{\frac{2I_{OUT}}{\mu C_{ox}(W/L)_2}}. \tag{2.17}$$

2.5 Previously Reported Amorphous Oxide Semiconductor Circuits

The focus in amorphous oxide semiconductor circuitry has been on digital circuit applications. To this date, inverters and ring oscillators make up the majority of reported AOS circuit work.

In 2006 Presley *et al.* fabricated the first fully transparent circuit based on amorphous oxide semiconductors [13]. Indium gallium oxide (IGO) was used as the channel material for the fabrication of transparent inverters and ring oscillators. The gate electrodes were 200 nm of ITO, deposited using RF magnetron sputtering and patterned using standard photolithography. The gate dielectric was 100 nm of plasma-enhanced chemical vapor deposition (PECVD) deposited silicon dioxide (SiO_2). The channel material was 40 - 50 nm of IGO deposited using RF magnetron sputtering and patterned using photolithography and a wet chemical etch. The ITO source drain electrodes were again RF-sputtered ITO patterned this time via lift-off. All constituent layers are transparent, rendering the resulting circuits transparent with $\sim$75 % optical transmittance. The TFTs exhibit a turn-on voltage of $\sim$2 V and a peak incremental mobility of $\sim$7 $cm^2V^{-1}s^{-1}$. The five-stage ring oscillator exhibits an oscillation frequency of $\sim$2.2 kHz at a 30 V bias and 9.5 kHz at an 80 V bias.

In 2007 Ofuji *et al.* published a report of a five-stage ring oscillator utilizing IGZO for the TFT channel material [14]. These circuits used electron beam deposition to deposit trilayer Ti/Au/Ti gate contacts patterned via lift-off. The gate dielectric was 100 nm of SiO_2 and both the dielectric and the IGZO channel, of unspecified thickness, were deposited using RF sputtering and patterned using standard photolithography. The Ti/Au source and drain contacts were deposited using the same method as the gate electrodes. The TFTs reported had a saturation mobility of 18.2 $cm^2V^{-1}s^{-1}$ with a turn-on voltage of -2 V. The five-ring oscillator had an operating frequency of 410 kHz at 18 V with a propagation delay of 240 ns. The circuits fabricated were faster than those of Presley *et al.*; this difference in speed is most likely due to a decreased gate-to-source overlap which decreased the parasitic capacitance and thus the RC time constant.

Also in 2007, Sun *et al.* reported 5, 7, and 15 stage ring oscillators [15]. These circuits used Cr bottom gates patterned and wet etched with photolithography. The gate insulator was 100 nm of Al_2O_3 deposited by atmospheric pressure chemical vapor deposition (APCVD). The channel material was 20 nm of ZnO, also deposited using APCVD and patterned using photolithography. The TFTs reported exhibited a near zero turn-on voltage, and a field effect mobility of 15 $cm^2V^{-1}s^{-1}$. The five-stage ring oscillator had a reported output frequency of 1.04 MHz with a propagation delay of 75 ns.

In 2009 Lee *et al.* fabricated a full-swing IGZO inverter using a depletion-mode load transistor [16]. The use of a depletion-mode transistor allows for higher performance logic circuits when no p-type transistor is available. The circuits were fabricated on a heavily doped p-type silicon substrate that was used as the gate electrode. Silicon dioxide was used as the gate dielectric and the IGZO channel was deposited by RF magnetron sputtering. The source drain contacts were deposited via electron beam evaporation and were Ti/Au. The depletion or enhancement characteristic of the TFT was determined by channel thickness. TFTs with channels of 200 nm were depletion-mode TFTs and those with a channel thickness of 20 nm were enhancement-mode TFTs.

The TFTs exhibited a saturation mobility of 11.4 $cm^2V^{-1}s^{-1}$ and 7.4 $cm^2V^{-1}s^{-1}$ for enhancement and depletion-mode devices, respectively. The enhancement-mode TFTs had a turn-on voltage of $\sim$0 V and the depletion-mode TFTs had a turn-on voltage of $\sim$-20 V. Inverters were fabricated using the enhancement device as the driver and the depletion mode device as the load. The inverters exhibited a high gain of 37.4 V/V with a supply voltage of 20 V. The swing range was wider than inverters made with enhancement-mode loads, and the transition between high and low state was well centered at half the supply voltage, 10 V.

In April 2010 Suresh *et al.* reported the fastest fully transparent circuits [17]. Five stage and 7-stage ring oscillators were built using IGZO transparent TFTs. The circuits were fabricated on glass substrates. Gate electrodes were created by sputtering 60 nm of ITO patterned with photolithography and dry etching. The gate insulator was 120 nm of Al_2O_3 deposited by atomic layer deposition (ALD) at 200 °C. The IGZO channel layer was deposited by PLD and was 40 nm thick. The ITO source and drain were 200 nm thick and deposited by PLD. The TFTs exhibited a saturation mobility of 15 $cm^2V^{-1}s^{-1}$, a turn-on voltage of $\sim$0 V, a subthreshold slope of 130 mV/decade, and an I_D on-to-off ratio of greater than 10^8. The fabricated 5-stage ring oscillators had an operating frequency of 645 kHz at a source voltage of 25 V, with a propagation delay of 155 ns/stage. The 7-stage ring oscillators were even faster at 2.1 MHz and a propagation delay of 48 nsec/stage at a source voltage of 25 V. At the time of publication these were the fastest AOS circuits reported, transparent or otherwise.

The applications for AOS circuits are not limited to inverters and ring oscillators. Display applications is an area in which AOS TFTs are regarded as being competitive with the predominant technology of amorphous silicon TFTs. In 2008 Jeong *et al.* used amorphous IGZO TFTs in an active-matrix organic light emitting-diode (AMOLED) display [18]. AOS TFTs have advantages over the a-Si TFT materials because they have better mobility and threshold voltage uniformity with a comparatively higher mobility of $>$10 $cm^2V^{-1}s^{-1}$.

The TFTs were fabricated in an inverted staggered bottom-gate structure. SiO_x was deposited on glass substrates and Mo gates were patterned on top of the SiO_x layer. The gate dielectric was SiO_x or a stack of SiO_x/SiN_x deposited by PECVD. The IGZO channel was deposited via sputtering and was protected from the Mo or Ti/Al/Ti source/drain layer

sputtering and dry etching with an unspecified etch stop layer (ESL). The TFTs had a field effect mobility of 8.2 $cm^2V^{-1}s^{-1}$ and turn-on voltage of $\sim$-2 V. The subthreshold slope was 0.58 V/decade with the ESL layer and the drain current on-to-off ratio was greater than 10^8. The AMOLED display was a 12.1 inch display with 1280 x RGB x 768 and a resolution of 123 ppi.

In 2009 Görrn *et al.* fabricated ZTO pixel drivers for use in AMOLED displays [19]. Görrn observes that ZTO has advantages for use as pixel drivers because it shows high stability under bias stress, and is less sensitive to visible light than other AOS. The pixel drivers fabricated were of the 2 TFT, 1 capacitor (2T1C) architecture. The pixel drivers were fabricated on glass coated with ITO. The gate dielectric was a 100 nm thick Al_2O_3 deposited by ALD. The 50 nm thick ZTO channel layer was deposited by plasma-assisted pulsed laser deposition (PA-PLD) with the substrate at 350 °C. The source and drain contacts were Al doped ZnO (AZO) deposited by PLD. The fabricated TFTs had a turn-on voltage of -4 V and a saturation mobility of 5 $cm^2V^{-1}s^{-1}$. The pixels fabricated were 180 x 240 μm^2 which is small enough to realize a high resolution display, though the fabrication of such a display was not attempted in the report. The desired switching speed of 10 μs was realized with input pulses of 10 μs without any cross-talk. Using data levels between -2 V and 10 V the pixel was variable between 0 and 4.8 μA corresponding to a possible pixel brightness of 2200 cd/m^2. Görrn asserts that the pixel drivers have "excellent performance in terms of resolution, pixel cross-talk, refresh rate and maximum display brightness". This pixel circuit shows a promising start to display work utilizing ZTO.

2.6 Analog Circuits in Competing Technology

As in the reviewed work in Sec. 2.5, most of the circuit fabrication work using amorphous oxide semiconductors has been in the field of digital circuits. Researchers have reported AOS inverters and ring-oscillators. Simple pixel drivers have also been fabricated using IGZO and ZTO AOS. At this time, there have been no reported analog circuits using AOS channel materials. AOS have three distinct disadvantages that hamper their use in analog circuitry. First, the instability of AOS TFT turn-on voltage can cause analog circuit biasing to be made insufficient when the turn-on voltage shifts [20]. Second, low TFT mobility compared to that of a conventional MOSFET, results in transistors with low intrinsic gain, g_m. Thus, AOS TFTs struggle to provide sufficient gain for complex analog circuits. Lastly, the lack of a p-type AOS channel material limits circuit design to the use of n-TFTs only.

The downsides of using AOS in analog circuits, while formidable, are nothing new to those working with the dominant material for TFTs in display applications, amorphous silicon (a-Si). Amorphous silicon also suffers from turn-on voltage instability, low mobility, and lack of sufficient p-type behavior [21]. Nathan *et al.* and Sambandan *et al.* have outlined possible analog circuits that are functional and crucial for OLED back-plane electronics. These circuits can overcome the drawbacks of a-Si for analog circuit applications. The discussed analog circuits include voltage adders, subtractors, and current mirrors.

The presented a-Si circuits are equally realizable using ASO TFTs. In fact, AOS have higher mobility and better stability than those of a-Si TFTs. Therefore, AOS TFTs should result in higher performance circuits than a-Si [22], [23]. The analog circuits

presented in the two papers could be fabricated using AOS-based TFTs and demonstrate the usefulness of these material systems in OLED back-plane electronics.

Of the circuits discussed, the current mirror is one of the most interesting. Current mirrors can be used in pixel drivers to combat the effects of turn-on voltage instability which causes changes in OLED current. The change in OLED current leads to a decrease in pixel brightness over time. The main advantage of using a current mirror in pixel driver design is that the current mirror circuit itself is less sensitive to turn-on voltage shifts because the gate voltage tracks with the turn-on voltage shift in both of the TFTs in the circuit [21]. A current mirror can be utilized in an AMOLED pixel circuit to compensate for the decrease in pixel brightness that occurs when turn-on voltage shifts in the 2T1C circuit. Figure 2.11 shows one version of a turn-on voltage-shift independent

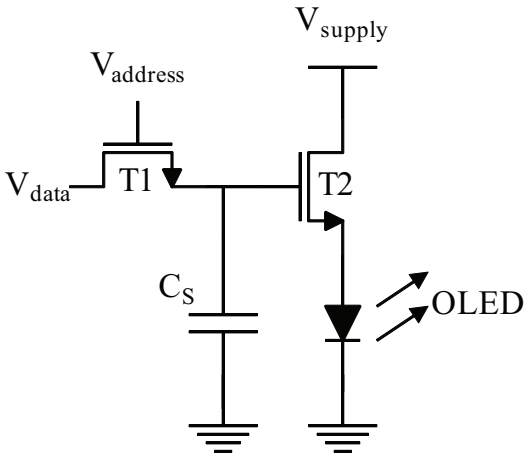


Figure 2.10: A two-transistor one-capacitor pixel driver circuit. This circuit is suspectable to pixel dimming due to turn-on voltage shifting.

four transistor one capacitor (4T1C) pixel driver, implemented with a current mirror [20]. When the pixel is selected by the gate drivers and $V_{address}$ goes high, transistors T1 and T2 turn on creating a path diode tying the gate and the drain of T3 together. The gates of T3 and T4 are connected, so it is apparent that T3 and T4 constitute a current mirror.

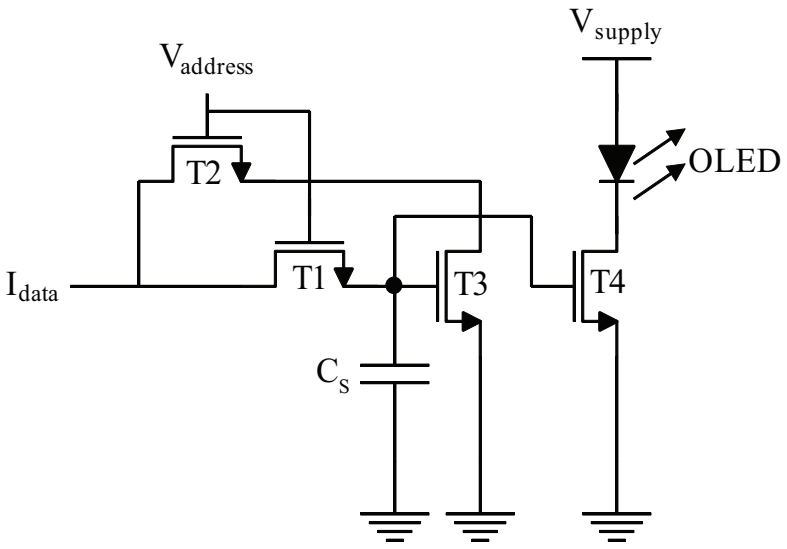


Figure 2.11: A four-transistor one-capacitor pixel driver circuit. This circuit utilizes a current mirror to compensate for variations in turn-on voltage.

Initially, the current I_{data} flows through T1 and charges the storage capacitor C_s. When C_s is charged, all of I_{data} flows into the drain of T3 acting as the reference current for the current mirror, and I_{data} is transferred to the OLED. The gates of T3 and T4 are tied together, so the data stored in C_s programs the data signal on T4 and thus the OLED gets the desired current until the next piece of data is programmed [24]. From the discussions of Nathan *et al.* it is apparent that the current mirror has the potential to be a vital piece of circuitry for AMOLED back-plane electronics.

3. EXPERIMENTAL TECHNIQUE

This section reviews the thin-film deposition and processing methods used to fabricate AOS thin-film transistors and subsequent AOS circuits. The fabrication methods used in this research include physical and chemical vapor deposition, photolithographic patterning, and film etching. Device and circuit measurement and characterization techniques are also presented.

3.1 Sample Preparation

The substrates upon which the TFTs or circuits are to be fabricated must be prepared and cleaned before deposition of the thin-film layers. Samples are subjected to a thorough acetone rinse to remove organics on the substrate surface. Before the acetone has dried on the sample surface, it is generously rinsed off with isopropyl alcohol (IPA). The final step is a deionized (DI) water rinse to remove the IPA before it dries on the surface. The DI water is then removed from the substrate with a filtered nitrogen blow dry. Once the large droplets of water have been removed from the surface, the sample is placed in a drying oven at 35 $^{\circ}C$ for 1 hour to dehydrate it and remove any remaining water. Alternatively, the sample may be placed on a 200 $^{\circ}C$ hotplate for 15 min to achieve dehydration.

3.2 Physical Vapor Deposition

3.2.1 Thermal Evaporation

Thermal evaporation is a physical vapor deposition (PVD) technique used to deposit thin films of material onto a target substrate. PVD is often carried out at a low pressure to decrease contaminants and increase the mean free path of the source particles to be

deposited. The mean free path of particles in a vacuum is determined by,

$$\lambda = \frac{1}{\sqrt{2}\pi {d_o}^2 n}, \tag{3.1}$$

where d_o is the molecular diameter and n is the gas concentration [25]. Pressure and gas concentration are related via

$$P = \frac{nmc^2}{3}, \tag{3.2}$$

where m is the mass of the gas molecule and c is the average speed of the particle determined from the Maxwell-Boltzmann distribution. Therefore, the mean free path, for air, may be simplified and expressed as

$$\lambda = \frac{0.05}{P}, \tag{3.3}$$

where pressure, P, is expressed in torr and λ is the mean free path in mm. From this formulation it is evident that as pressure decreases, mean free path increases. It is advantageous to have a long mean free path for deposition in order to decreases the likelihood that the source particle collides before it reaches the target substrate. Such collisions can result in a lower quality films due to the deposition of impure source material.

To complete thermal evaporation the source material is placed in a crucible, or filament boat, inside a vacuum chamber, as illustrated in Fig. 3.1. The chamber is evacuated and pumped to a sufficiently low pressure to remove contaminants and to increase the mean free path of the source material. Electric current is passed through a heating element attached to the crucible, or the filament boat itself, resulting in resistive heating [26]. The heat causes the source material to melt and evaporate; alternatively the material may sublime and skip the melting phase all together. The vapor phase source material travels to the substrate and condenses on the surface creating a film. The thermal evaporator

used in this research was a Polaron single source evaporation system. The material deposited by this equipment was aluminum and was used for TFT source, drain, and circuit contacts.

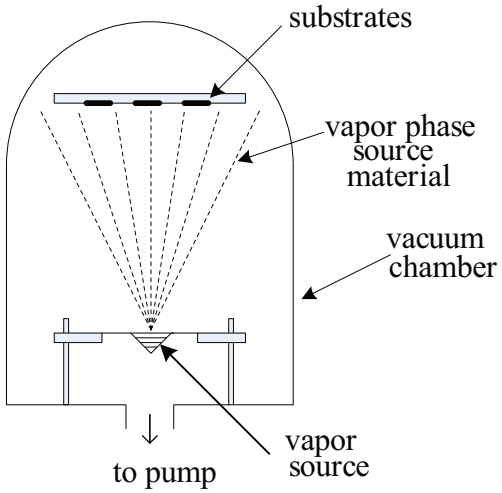


Figure 3.1: Schematic of a thermal evaporation system.

3.2.2 Sputtering

Sputtering is a physical vapor deposition processes in which thin films are deposited onto a substrate when atoms are ejected from a target material via bombardment by energetic particles. Sputtering has many advantages, especially with respect to other PVD techniques such as evaporation, which make it attractive for displays and large-area electronics. The use of AOS for such applications is bolstered by the easy deposition of channel materials via sputtering. Some of the advantages that make sputtering so vital are the ability to cover large areas, easy control of film thickness and composition, and the availability of *in situ* sputter cleaning of substrate surfaces [25].

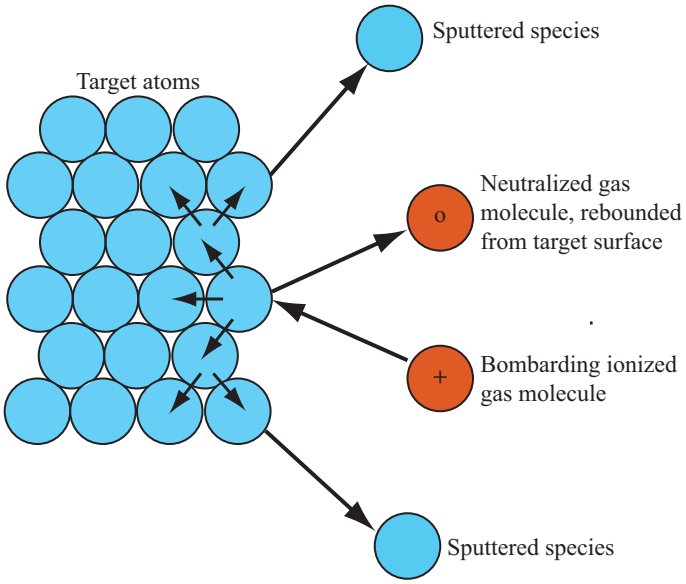


Figure 3.2: Energetic particles bombard target surface ejecting target material to be condensed onto substrate surface.

Sputtering can be used to deposit metals, which conduct, and insulating materials, such as oxides. Deposition of metals is achieved via DC diode sputtering, while insulators require the slightly more complicated method of radio frequency (RF) sputtering. To fully understand how each type of sputtering works, it is first necessary to discuss the basics of a glow discharge.

3.2.2.1 Glow Discharges

In order to sputter it is necessary to create the energetic particles used to strike the target surface and eject atoms to be condensed into a film. These particles come from a plasma, a partially ionized gas containing neutral species, as well as an equal number of positive and negative charge species. A glow discharge is the self-sustaining plasma from which energetic particles for sputtering are drawn. The simplest way to create a glow

discharge is to use a DC diode system. In this configuration two electrodes are placed in a vacuum chamber which has been evacuated and refilled with a particular sputter gas, typically argon, to be ionized. A potential is applied between the two electrodes, such that one becomes the positively charged anode and the other the negatively charged cathode. When the voltage is first applied, little or no current flows, as most of the Ar is neutral. Eventually an ionization event occurs (due to an outside force such as cosmic radiation) creating an Ar^+ ion and a free electron. This electron is accelerated in the electric field created by the potential between the electrodes.

As the electron travels between the electrodes it has a chance to collide with another particle. The two types of collisions that can occur are elastic and inelastic collisions. The more common collision between an electron and an atom, an elastic collision, is one in which a negligible amount of energy is transferred from the electron to the atom. These collisions occur readily because the mass of the electron is far less than that of the atom. The less likely, inelastic collision is characterized by an energy transfer. When this collision occurs, some of the energy that the electron gained from the field is transferred to the Ar atom. If this energy is below the ionization potential of the atom, one of the Ar orbital electrons is excited to a higher state briefly, and then relaxes back to its ground state. This relaxation is accompanied by photon emission. These collisions occur frequently and are what give the glow discharge its characteristic color.

If the energy of the incoming electron is higher than the ionization potential, then the collision results in the removal of an electron from the Ar atom. This creates an additional free electron. The original electron and the newly freed electron are now both accelerated by the field and participate in more collisions which, in turn, create a cascading number of electrons, a condition known as gas breakdown. When gas breakdown has

been achieved, a significant current can now travel between the electrodes and the electrons generated by the collision cascade are collected at the anode. Therefore, in order to sustain current flow, and the plasma, a method of creating more free electrons is needed. The electrons needed to sustain the plasma come from the bombardment of the cathode with energetic neutral and ionized Ar atoms. These collisions are of high enough energy to cause the cathode to emit secondary electrons, thus sustaining the glow discharge.

3.2.2.2 DC Sputtering

In a DC sputter configuration the cathode is the target material to be sputtered. The gas species in the glow discharge impinge onto the target surface. Some of these ions, atoms, or molecules have sufficient energy to dislodge atoms from the target surface which travel, in the gas phase, to condense onto the substrate as seen in Fig. 3.2. This method is viable only for conductive targets. As the negatively charged cathode is bombarded by positive ions, an electron is stripped from the target surface. In DC diode sputtering these electrons are replenished via the electrical conduction of the circuit, so the cathode remains negatively charged and the plasma is sustained. This electron replenishment is not available when sputtering non-conductive insulators.

3.2.2.3 RF Sputtering

When the target is an insulating material, the electrons stripped from the target surface cannot be replenished through electrical conduction as in the dc diode configuration. Impinging ions would lead to a buildup of positive charge on the target which in turn would lead to the glow discharge being extinguished. Therefore, a different sputtering configuration is needed. RF sputtering uses an ac voltage to remove the buildup of positive charge from the target surface. During the negative half cycle of the applied

waveform, positive ions are attracted from the glow discharge to the target surface, resulting in sputtering. The target builds up a net positive charge during this portion of the waveform. When the waveform switches to the positive half cycle, electrons are drawn to the target, neutralizing the positive charge, and creating a net negative charge. Electrons, having less mass than ions, are accelerated to the target faster. Therefore, there are more electrons gathered onto the target surface during the positive half cycle than ions during the negative half cycle. This establishes a negative self bias near the target, also known as the DC offset. The system used in this research is an AJA Orion 5 RF magnetron sputter deposition system.

3.3 Chemical Vapor Deposition

Chemical vapor deposition (CVD) is a thin-film deposition process in which desired chemical components are introduced, in the gas phase, into the reaction chamber. The constituent gases are then decomposed and/or reacted at the substrate to form the desired film [25]. CVD is an advantageous method of film deposition for thin-film transistor work because the surface is not involved with, or consumed in the reaction. This allows for CVD deposition of pure films onto almost any type of surface or substrate. CVD films are deposited by first introducing a given composition of gas into the reaction chamber. CVD uses a continuous flow system, and gas is fed from the inlet to the outlet constantly. Once in the reaction chamber the reactant gas species travel to the substrate surface. The reactant gasses are adsorbed onto the substrate surface, where they then migrate across the surface to film growth sites. It is at these sites that the film forming reaction occurs, as depicted in Fig. 3.3. The gaseous by-products of the reaction are then desorbed from

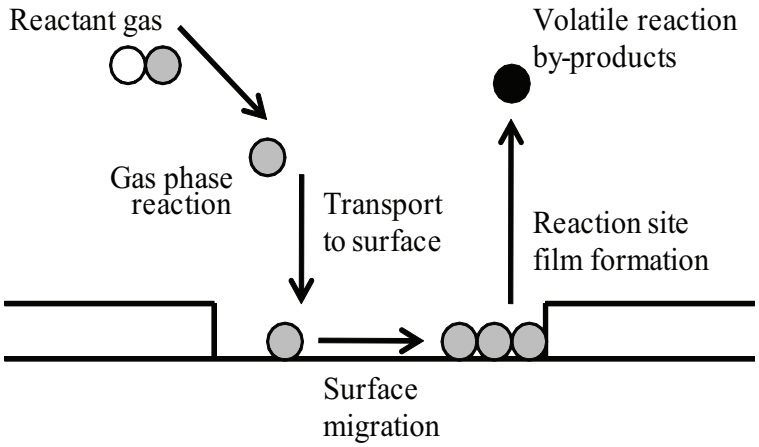


Figure 3.3: Film formation of a CVD film. Reactant gas species decompose and transport to the surface where they are adsorbed and migrate to reaction sites to form the film, and volatile reaction by-products are desorbed from the surface and removed through the gas outlet.

the surface and removed via gas flow to the outlet. It is in this manner that CVD films are deposited.

3.3.1 Plasma-Enhanced Chemical Vapor Deposition

In conventional CVD the energy to drive the reaction is thermal energy, often generated from a heated stage. This presents a challenge, however, when the previous layers of a process stack lack the thermal stability to withstand the temperatures necessary to drive the reaction. Such is the problem for amorphous oxide semiconductors, where high temperatures can cause unwanted crystallization of the channel material. Plasma-enhanced chemical vapor deposition (PECVD) uses an RF glow discharge to provide the reaction energy. An RF glow discharge is generated in the reaction chamber, Fig. 3.4, by the application of an RF field to the low pressure reactant gas in the chamber. The glow discharge, as described in Sec. 3.2.2.1, creates free electrons, which gain energy from the

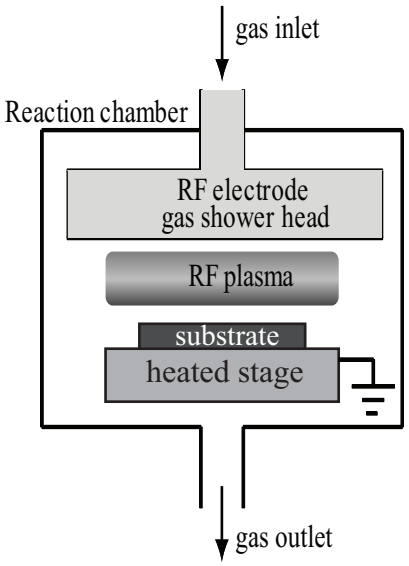


Figure 3.4: A PECVD reactor. The substrates are placed onto the heated stage, which serves as the cathode for the rf bias. The gas is introduced via a shower head which serves as the anode. An RF plasma is created between the two electrodes to aid in film deposition.

field and collide with the reactant gas molecules. These collisions cause decomposition of the reactants and formation of energetic species to be adsorbed on the film surface, thus depositing a thin-film on the substrate at low temperature.

3.4 Photolithography

Photolithography is used to define windows and structures in thin-films. The desired pattern is transferred from a mask to a light-sensitive chemical, called photoresist (PR), by the application of high intensity ultra-violet (UV) light. Once the pattern is transferred, the photoresist protects areas of the film that should not be removed during etching and allows for selective etching in desired locations. The ZTO circuits presented in this thesis were patterned using photolithography.

Photolithography consists of 9 primary steps illustrated in Fig. 3.5.

1. **Surface preparation.** The sample must be free of surface contaminants for proper adhesion and pattern transfer. Even very small particles of contamination, such as dust or hair, can create massive defects in a patterned structure, as the mask structures are only microns wide. It is therefore vitally important to thoroughly clean the surface before application of PR. Surface cleaning is discussed in greater detail in Sec. 3.1

2. **Application of PR.** Liquid PR is applied to the sample and spun at high speed to create a thin, uniform layer. At this stage, adhesion of the PR to the sample surface is extremely important. To promote adhesion, a chemical primer, such as HMDS, may be used.

3. **Soft bake.** The sample is baked at a temperature of 60 $^{\circ}C$ to 100 $^{\circ}C$ to remove the solvent and improve adhesion.

4. **Alignment.** The sample is aligned to the mask so that the pattern on the previous layer lines up with the mask. Alignment marks are used to facilitate the alignment of each new mask to the previous layer.

5. **Exposure.** The sample is brought into contact with the mask and high-intensity UV light is shone through the mask.

6. **Development.** After exposure, the sample is placed in a development solution. If positive resist is used, the pattern of the mask is transferred to the PR. The bonds of the organic compounds in positive PR are weakened by exposure to UV light and wash away easily when placed in developer. If negative resist is used, a negative

image of the mask is transferred to the PR. In negative PR, the bonds exposed to UV light become stronger and remain after development while those areas shielded from UV light are washed away, Fig 3.6.

7. **Hard bake.** The sample is subjected to a higher temperature (100 $^{\circ}C$ - 200 $^{\circ}C$) bake step to harden the PR in preparation for etching.

8. **Etching.** Samples are etched in a suitable wet or dry environment to remove the areas of the film unprotected by photoresist.

9. **PR removal and cleaning.** The photoresist is removed with the appropriate chemical and the sample is cleaned thoroughly to insure no PR residue remains on the surface.

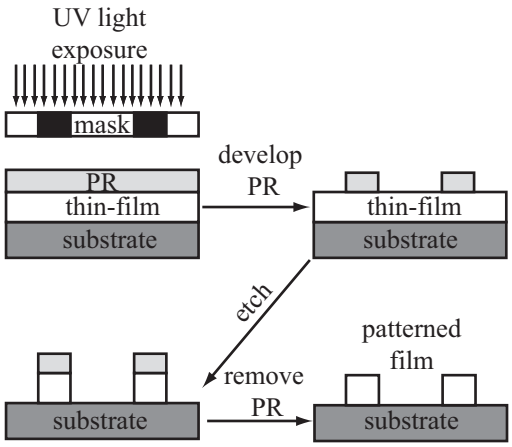


Figure 3.5: Photoresist is applied to the thin-film surface. A pattern is defined in the photoresist layer by the application of ultra-violet light through a mask. Etching removes material not protected by the photoresist layer leaving behind a patterned film.

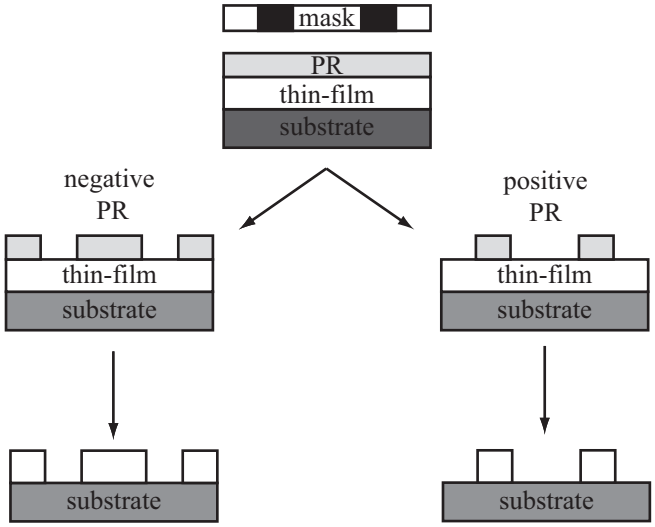


Figure 3.6: Final film pattern created when using positive or negative photoresist

3.5 Etching

Etching is a subtractive process in which material is removed from the substrate. Most often, it is used to remove the unprotected regions exposed by photolithography. There are two common methods of etching, wet and dry etching. In each method the distinguishing characteristics are isotropy and selectivity. Isotropy refers to the profile of the etch process. In a fully isotropic etch the film removal occurs, at an equal rate, in all directions. In an anisotropic etch the etching occurs preferentially in one direction as illustrated in Fig. 3.7. Ideally, an anisotropic etch is preferred. In practice, etches are rarely entirely anisotropic and instead exhibit some degree of isotropy. The selectivity of an etch is a measure of the preferential removal of one material over the others. A high selectivity is preferred so that only the desired material is removed and not the material underneath or above it, Fig. 3.8.

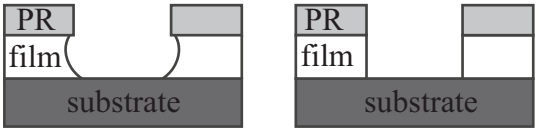


Figure 3.7: (a) An isotropic etch, etching occurs both vertically and laterally. (b) An anisotropic etch, etching occurs only vertically.

In wet etching the sample is immersed in a liquid acid or base solution that reacts with the film to disassociate the film constituents and remove the film. A wet etch can be highly selective and etch the desired film without harming the film below. The downside to a wet etch is the isotropic etch profile, which limits the minimum dimension of patterned features. Circuits reported herein use wet chemical etching to define the gate metal, semiconductor channel, and vias in the dielectric layer.

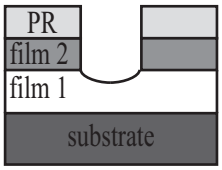


Figure 3.8: A non-selective etch. Film 2 is removed as desired, however poor selectivity leads to the removal of part of film 1 as well.

A dry etch can be accomplished using either a strictly physical mechanism or can incorporate a chemical interaction as well. Ion bombardment in a plasma can be used to physically remove a film. This etch process is anisotropic, but has poor selectivity because the film underneath the one to be removed may be damaged by the ion bombardment. When ion bombardment is used in conjunction with a reactive gas, the resulting etch process is denoted as a reactive ion etch. The reactive gas is dissociated by a glow discharge and the reactive ions bombard the surface where they react with the film, and

chemically and physically remove the film, this dual mechanism yields an efficient and anisotropic etch.

3.6 Electrical Characterization of Thin-Film Transistors

There are two types of current-voltage measurements used to evaluate TFT performance: the output curve and the transfer curve. An output curve is a measurement of TFT output voltage versus output current (V_{DS}-I_D). From this plot the output resistance and associated channel length modulation parameter can be estimated. The transfer curve is a measurement of TFT input voltage versus output current (V_{GS} vs. I_D). This measurement allows for the determination of the turn-on and threshold voltages, the mobility, the subthreshold slope, and the drain current on-to-off ratio.

3.6.1 TFT Output Resistance

Ideally, a transistor has infinite output resistance, causing it to reach a hard saturation, where the TFT maintains the saturation current value, after the application of a drain-to-source voltage in excess of V_{DSAT}. In practical application however, the TFT possesses a finite output resistance caused by channel length modulation. This channel length modulation effect is evidenced by the lack of hard saturation in the output curves and an increasing drain current with respect to drain voltage, or soft saturation as seen in Fig. 3.9 [9].

The saturation equation for a TFT in soft saturation can be described by including an additional V_{DS} dependant term.

$$I_D = I_{DSAT} = \frac{W}{2L}\,\mu\, C_G(V_{GS} - V_{ON})^2(1 + \lambda V_{DS}) \tag{3.4}$$

where μ is the TFT mobility, W/L is the TFT size, V_{ON} is the TFT turn-on voltage and λ is the channel length modulation parameter equal to the inverse of the output resistance.

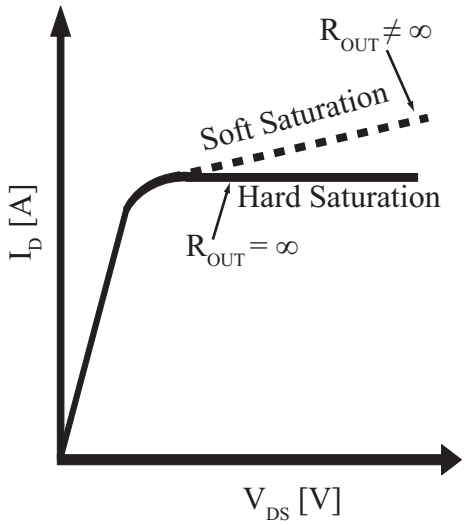


Figure 3.9: Output curve for a TFT showing hard and soft saturation. The slope of the curve in soft saturation can be used to calculate TFT output resistamce.

The slope of the output curve in soft saturation for a given V_{GS} can be used to calculate the output resistance,

$$R_{OUT} = \left[\frac{\partial I_D}{\partial V_{DS}}\right]^{-1}\Big|_{V_{GS}=const}. \tag{3.5}$$

Output resistance can be used to estimate λ,

$$\lambda = \frac{1}{R_{OUT} I_D}. \tag{3.6}$$

Therefore, if the slope of the output curves is known, as well as the ideal value of the drain current (without channel length modulation), then the channel length modulation parameter λ can be estimated.

3.6.2 Turn-on and Threshold Voltages

The turn-on voltage, V_{ON}, is the gate-to-source voltage at which the drain current begins to appreciably increase. This corresponds to the onset of channel conduction and the flat-band condition, just before channel accumulation occurs. It should be noted that the turn-on voltage is different than the more commonly discussed threshold voltage, V_{TH}. Threshold voltage, as discussed in the context of the silicon MOSFET, is a model parameter with a certain amount of inherent ambiguity in its determination. It is however, the dominant parameter used in the discussion and design of analog circuits.

The threshold voltage can be found by taking the transfer curve and plotting it on a linear scale [27]. The linear portion of the transfer curve is then extrapolated downward to the x-axis as seen in Fig. 3.10. The intercept of this line and the x-axis yields an estimation the threshold voltage.

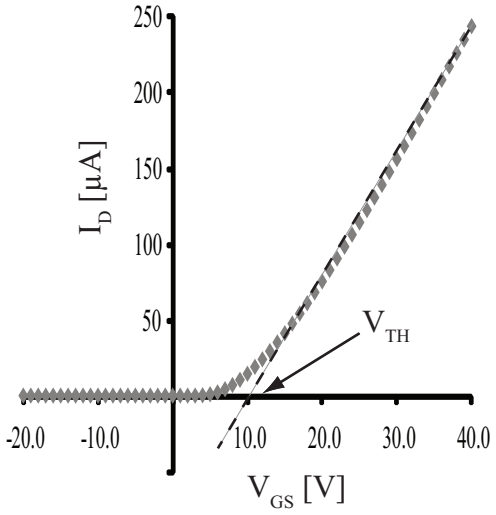


Figure 3.10: Transfer curve of a ZTO TFT with a silicon dioxide gate dielectric. The threshold voltage can be extracted by determining where the linear portion of the curve crosses the x-axis at $\sim$10 V.

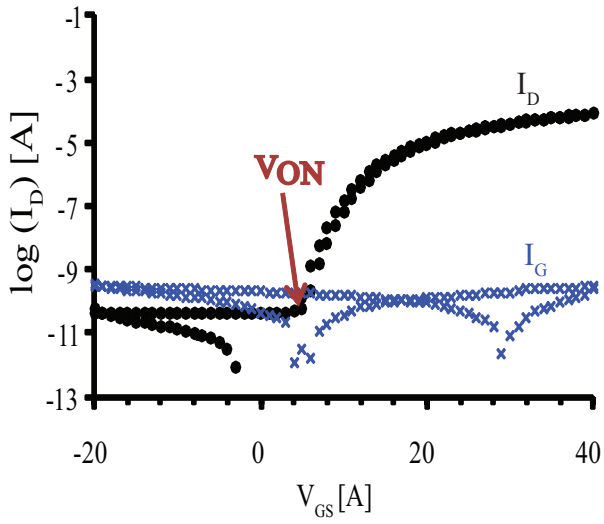


Figure 3.11: Log(I_D) - V_{GS} transfer curve of a ZTO TFT with a silicon dioxide gate dielectric. Turn-on voltage occurs when the drain current begins to increase at a V_{GS} value of 5 V.

This method of threshold voltage extraction has inherent variability based on the estimation of the slope, and as such can be inaccurate for TFTs with gradual turn-on behavior. That is why the turn-on voltage is preferred in the assessment of TFTs as it is a physical device parameter that can be easily determined from a transfer curve. The drain current is plotted on a logarithmic scale versus gate voltage, and the turn-on voltage is the point where drain current begins to increase above the negligible off-current value, as seen in Fig. 3.11.

3.6.3 Mobility

Transistor mobility is of utmost importance when evaluating a TFT as it allows investigation of the charge transport properties of the channel material directly. Mobility is

extracted from the channel conductance, calculated from the transfer curve. The transfer curve sweep is obtained at a low drain-to-source bias of 1 V in order to keep the TFT in the pre-saturation regime so that it can be assumed that channel charge density is uniform and all of the current is drift-dominated. This assumption simplifies the mobility assessment.

In 2004, Hoffman discussed two methods for assessing the channel charge in a mobility calculation. This led to two ways of determining the gate voltage dependant mobility [28]. The first is average mobility,

$$\mu_{avg}(V_{GS}) = \frac{G_{CH}(V_{GS})}{\frac{W}{L}C_{ins}[V_{GS} - V_{on}]}\Big|_{V_{DS}\to 0} \tag{3.7}$$

where $G_{CH}(V_{GS})$ is the gate voltage dependant channel conductance, W and L are the TFT width and length respectively, and C_{INS} is the gate capacitance density. This mobility formulation provides the average mobility of all carriers cumulatively induced in the channel by the gate voltage. The second mobility used is incremental mobility,

$$\mu_{inc}(V_{GS}) = \frac{G'_{CH}(V_{GS})}{\frac{W}{L}C_{ins}}\Big|_{V_{DS}\to 0} \tag{3.8}$$

where $G'_{CH}(V_{GS})$ is the derivative of the gate conductance with respect to V_{GS}, W and L are the TFT width and length respectively, and C_{INS} is the gate capacitance density. This mobility formulation quantifies the mobility of incremental additions of charge into the channel with incremental increases in gate voltage. The two mobilities are plotted as a function of the gate voltage in Fig. 3.12.

The average mobility is useful when characterizing device performance, as it reflects the overall current drive of the TFT as a function of gate voltage, whereas the incremental mobility allows for insight into device operation [28].

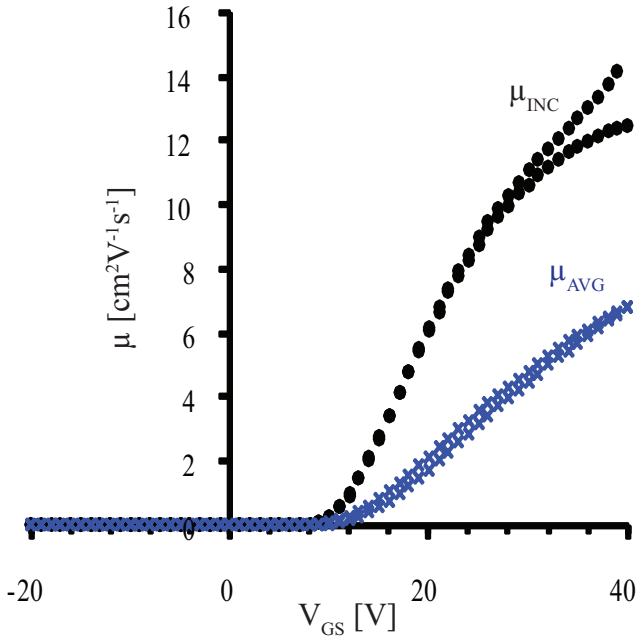


Figure 3.12: Incremental and average mobility as a function of gate voltage for a 3:1 ZTO TFT with SiO_2 gate dielectric and aluminum source-drain contacts.

3.6.4 Drain Current On-to-Off Ratio

The ratio of the current drive of a TFT when it is fully on, to the current drive when the device is off, is known as the drain current on-to-off ratio and can be seen in Fig. 3.13. A high on-to-off ratio is desired so that the device consumes less power when off and has sufficient current drive capability when on. Ratios of greater than 10^8 are generally considered sufficient to provide adequate TFT switching performance.

3.6.5 Subthreshold Swing

Subthreshold swing is a measure of the how sharply the TFT is turned off or on by the application of a gate voltage and can be seen in Fig. 3.14. Ideally the application of a voltage slightly in excess of V_{ON} would be sufficient to abruptly turn the TFT fully on. In

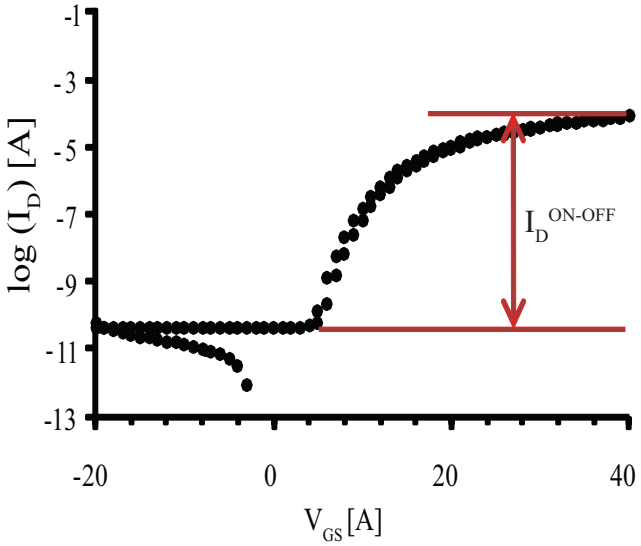


Figure 3.13: Drain current on-to-off ratio is the ratio of the current when the TFT is on to the current level when the TFT is off. The device under test is a 3:1 ZTO TFT with SiO_2 gate dielectric and aluminum source-drain contacts.

reality, however, a TFT turns on gradually with an increase of gate voltage, as the channel becomes fully formed and maximum conduction occurs. The abruptness of the turn-on characteristic is quantified by the subthreshold swing, S, expressed as

$$S = \left[\frac{\partial log I_D}{\partial V_{GS}}\right]^{-1} [mV/Decade]. \tag{3.9}$$

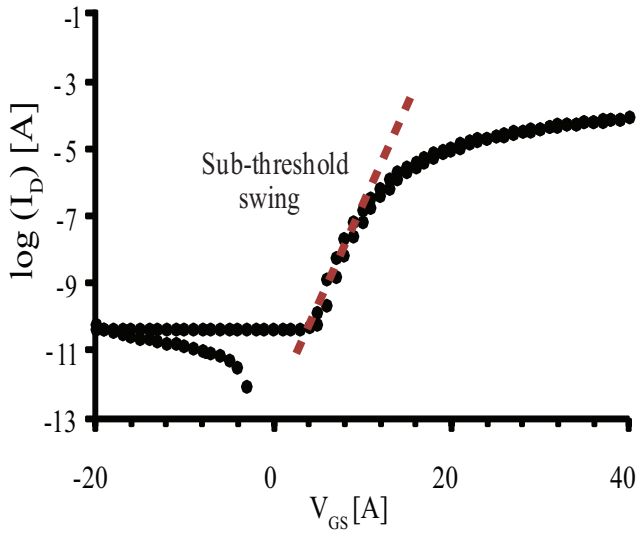


Figure 3.14: Subthreshold swing of a TFT is a measure of how sharply the TFT can be turned on. The device under test is a 3:1 ZTO TFT with SiO_2 gate dielectric and aluminum source-drain contacts

4. RESULTS AND DISCUSSION

4.1 AJA Orion V Sputter System Characterization

The sputter deposition system used to deposit channel material in this work is an AJA International Orion V. This tool is set up for RF magnetron sputtering in the sputter-up configuration. Current tool capabilities include 5 two-inch sputter sources, 2 RF supplies, allowing for a plasma to be generated at the substrate as well as the sputter target, argon and oxygen sputter gasses and substrate heating. The tool was purchased new by the advanced materials group at Oregon State University. As part of the initial setup for this system, characterization of the films, and devices, deposited using the Orion V sputter system was necessary. Investigation of TFTs using a commercial ZTO target (from AJA international) was undertaken. At the onset of TFT fabrication the stoichiometry of the target was thought to be 2:1 ZnO:SnO_2. The TFTs did not behave as previously fabricated 2:1 ZTO TFTs so further investigation into sputter parameters was conducted. The deposition rate and film uniformity are investigated first, then TFT performance of devices with channel layers deposited in the Orion V is evaluated.

4.1.1 Film Characterization

The deposition rate and film uniformity of the TFT channel material ZTO was obtained over a range of power and pressure. All depositions used a minimum substrate-to-target distance and a maximum substrate rotation as set by the tolerances of the tool. The substrate-to-target distance was approximately 6 inches, though accurate measurement of the distance is hard to gauge due to the off-axis sputter-up configuration of the tool. A

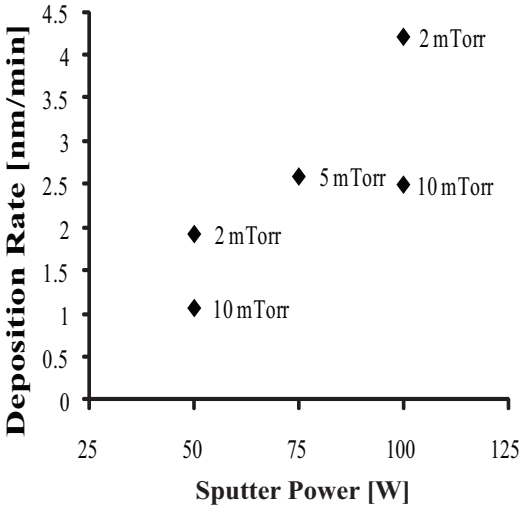


Figure 4.1: Deposition rate for films deposited over a range of power and pressure. Films deposited at high power and low pressure had the highest deposition rate.

longer substrate-to-target distance results in more uniform films, however, the deposition rate for such films is very low. The shortest available substrate-to-target distance is chosen to increase the deposition rate to a reasonable value. The maximum substrate rotation of 40 RPM is used to increase film uniformity. The maximum rate of substrate rotation is recommended by the manufacturer to provide optimal film uniformity.

With substrate-to-target distance and rotation fixed, the RF power and chamber pressured were varied and film uniformity and deposition rate were monitored. All films are deposited with an argon gas flow of 9 sccm and an oxygen flow of 1 sccm, establishing a 90 % argon 10 % oxygen atmosphere. The RF power was varied from 50 - 100 W and the pressure from 2 - 10 mTorr. Film thickness was measured using a single wavelength, fixed angle ellipsometer. Ellipsometer accuracy was independently confirmed using a spectroscopic ellipsometer, and a physical thickness measurement via profilometer. The

two secondary thickness measurements agreed well with the results obtained from the single wavelength ellipsometer and all further measurements were made using the single wavelength ellipsometer. Due to substrate rotation the significant thickness variation occurs radially across the wafer. Thickness measurements were taken from the outside edge radially inward at 7 locations separated by increments of approximately 8 mm along the radius of a 100 mm wafer, which is the largest size substrate that can be accommodated in the Orion V. Figure 4.1 shows the deposition rate for various sputter powers. As power increases, deposition rate increases. Runs performed at the same power but at a lower pressure result in a higher deposition rate. Fig. 4.2 shows the measurement locations

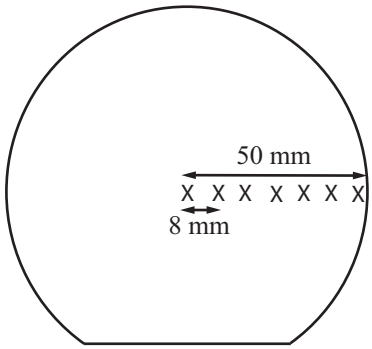


Figure 4.2: Measurement locations across a 100 mm wafer used to validate film uniformity and deposition rate.

used. A plot of normalized film thickness versus radial location, Fig. 4.3, shows that all films have less than 12 % thickness variation from edge to center across a 100 mm wafer. Films deposited at the lower pressures (i.e., 2 mTorr and 5 mTorr) showed less thickness variation. The processing parameters of 5 mTorr and 75 W were chosen for further investigation, with respect to TFT performance, because they provide a realistic trade-off between uniformity and deposition rate. Furthermore, these processing parameters have been shown to provide reliable, high-performance TFTs in comparable sputter systems.

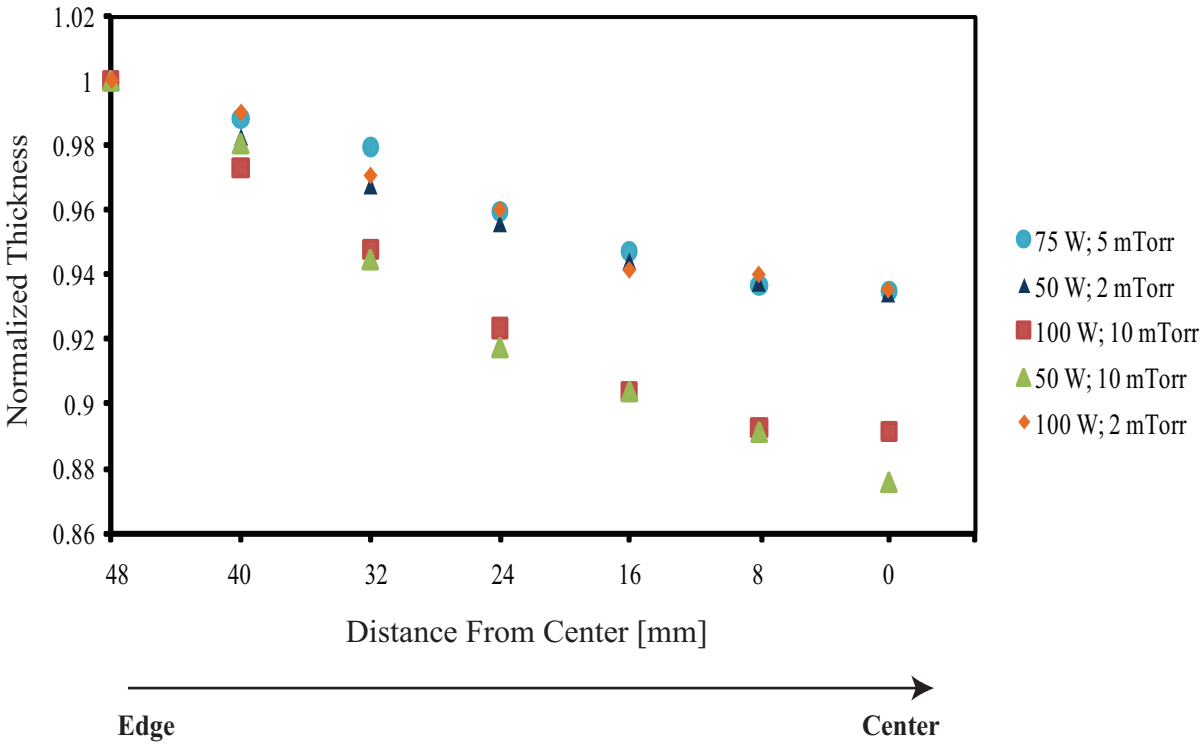


Figure 4.3: Thickness variation as a function of radial position along a four inch wafer for films deposited over a range of powers and pressures.

4.1.2 Thin-Film Transistor Characterization

After characterizing the ZTO films over a range of power and pressure, analysis and characterization of TFTs with ZTO channel layers, deposited in the Orion V at a pressure of 5 mTorr and an RF power of 75 W, are investigated. The TFT channels are defined by a shadow mask with a transistor width-to-length ratio of 10 and a desired channel thickness of 50 - 60 nm. Transistors are fabricated on 10 x 15 mm substrates of heavily doped p-Si with a Ta/Au back gate contact and 100 nm of thermal SiO_2 provided by Hewlett Packard. All substrates are cleaned using the standard substrate cleaning procedure outlined in Sec. 3.1. All shadow mask transistors are fabricated using the following process flow.

1. Substrate cleaning and dehydration.

2. ZTO channel sputter deposition; channel defined via shadow mask.

3. Channel anneal in air.

4. Aluminum source-drain contacts deposited by thermal evaporation; source and drain defined via shadow mask.

During the initial TFT characterization phase, devices were annealed at 400 °C for one hour. These channel deposition and annealing parameters have been investigated previously and are known to result in high-quality devices for similar sputter systems.

Figure 4.4 shows the transfer curve of a TFT fabricated using the AJA Orion V for channel deposition compared to a known good transistor from a comparable sputter system, the CPA.

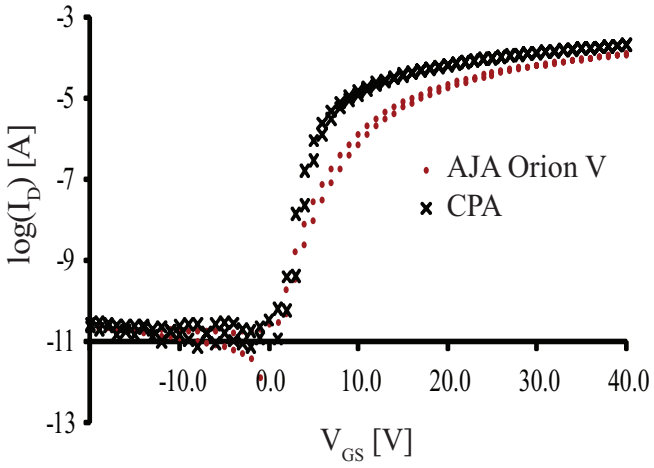


Figure 4.4: ZTO TFTs fabricated on thermal SiO_2 in the AJA Orion V sputter system and the CPA sputter system. Both TFTs have a W/L of 10. The TFT fabricated in the AJA exhibit a reduced subthreshold slope compared to the TFT fabricated in the CPA

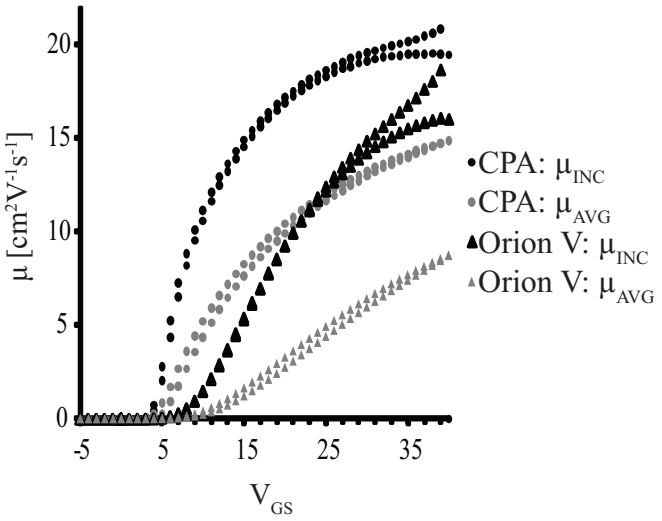


Figure 4.5: ZTO TFTs fabricated on thermal SiO_2 in the AJA Orion V sputter system and the CPA sputter system. Both TFTs have a W/L of 10. The TFT fabricated in the AJA exhibited lower incremental and average mobility than the transistor fabricated in the CPA.

TFTs fabricated using the Orion V show reduced transistor performance associated with a larger, more gradual subthreshold swing and decreased mobility compared to transistors fabricated in the CPA. This degraded transistor performance was unexpected and undesirable. An investigation into the effects of sputter parameters (power and pressure), and annealing temperature on TFT performance was therefore necessary in order to determine the origin of this difference in performance. The goal of this study was to find a set of parameters that yield transistor performance equal to that of transistors fabricated in the CPA.

A series of TFTs were fabricated over a range of different sputter pressures and powers in order to determine the optimal set of parameters to fabricate TFTs with smaller subthreshold swing and higher mobility. TFTs were fabricated at 75, 100, and 125 W.

The high power, 125 W, depositions were done at high and low pressures, 10 mTorr and 2 mTorr respectively. The low power 75 W run is carried out at a pressure of 2 mTorr. High pressure deposition was not attempted for the 75 W run because the low deposition rate is impractical for TFT fabrication. The 100 W run was used as a center point for the experiment and was carried out at a pressure of 5 mTorr.

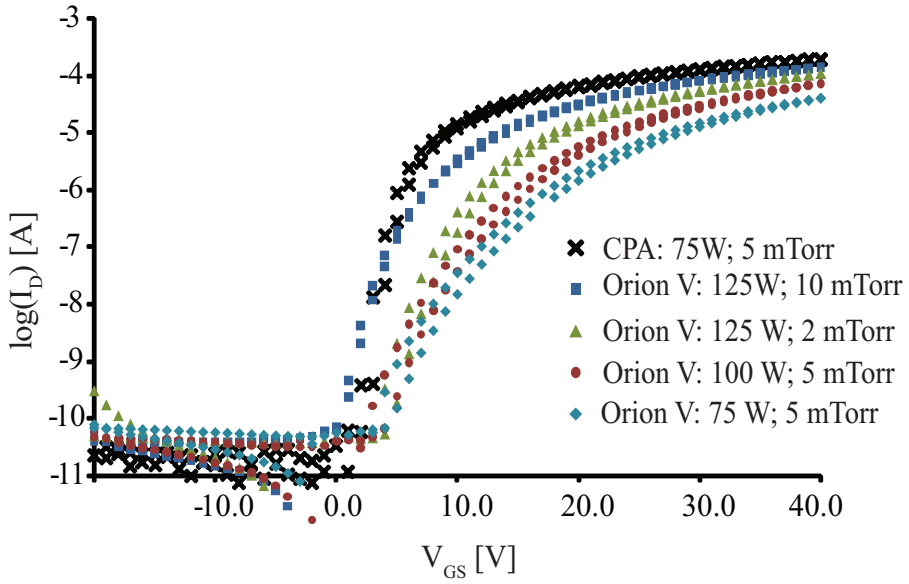


Figure 4.6: ZTO TFTs fabricated on thermal SiO_2 in the AJA Orion V sputter system over a range of powers and pressures. All TFTs fabricated in the Orion V had reduced performance compared to the TFT fabricated in the CPA

The results of TFT fabrication in the Orion V over a range of powers and pressures show that in the reasonable workspace of 75 - 125 W and 2 - 10 mTorr, there was no set of parameters that yielded TFT performance equal to that of TFTs fabricated in the CPA. The 125 W and 10 mTorr run shows improved TFT performance that comes close to the CPA standard. However, the subthreshold swing was still larger than desired.

No set of deposition conditions resulted in high quality TFTs so further investigation into anneal temperature was undertaken. TFTs were fabricated at 75 W and 5 mTorr the channels were then annealed at 400, 500, and 600 °C. Figure 4.7 shows that the 600 °C anneal came closest to providing TFT performance equal to that of TFTs fabricated in the CPA. However, a processing temperature of 600 °C is higher than desired and severely limits substrate choice for future TFT applications. Additionally, this temperature yielded very few working devices.

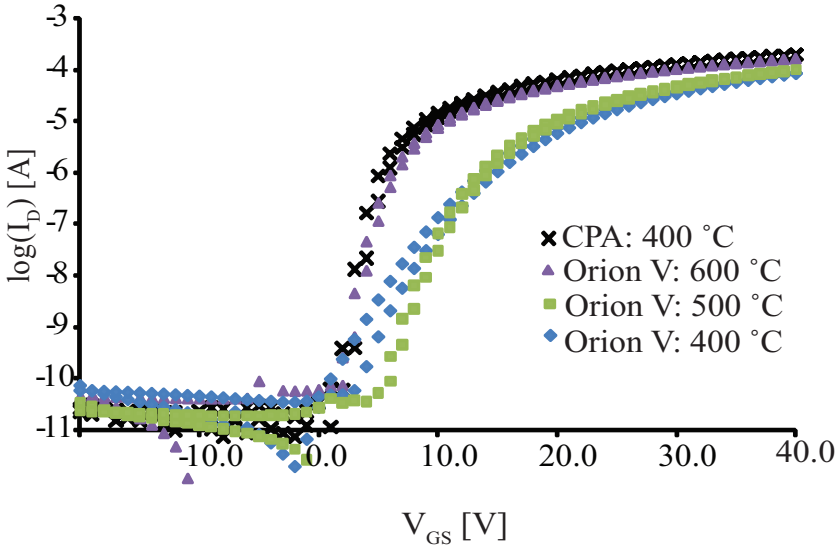


Figure 4.7: ZTO TFTs fabricated on thermal SiO_2 in the AJA Orion V sputter system. Each sample was annealed at a different temperature. The 600 °C annealed sample comes closest to achieving TFT performance equal to TFTs fabricated in the CPA

The exploration of the effects of processing pressure, power, and anneal temperature on TFT performance show that there is a fundamental difference between TFTs fabricated in the Orion V and those fabricated in the CPA. This difference cannot be overcome by modulating process parameters. It is therefore probable that the difference in devices stems from a fundamental material difference between the target materials in-

stalled in the Orion V and CPA. Electron probe micro-analysis (EPMA), provided by John Donovan at CAMCOR, was used to determine the composition of films deposited by the CPA and the Orion V. These results show the zinc-to-tin atomic ratio is $\sim$2:1 in samples from the CPA, this is as expected given the target stoichiometry. Samples from the Orion V however, reveal a zinc-to-tin atomic ratio of $\sim$3:1. Thus, films from the Orion V were found to be zinc rich, which accounts for the differences in TFT performance observed. As detailed by Hoffman in 2006, transistors with a zinc-to-tin ratio greater than 2:1 have a larger subthreshold swing and a lower mobility than those with a 2:1 zinc-to-tin ratio [29].

A target of 2:1 Zn:Sn (atomic %) composition (the same as the target composition in the CPA) was acquired and TFTs were fabricated at 75 W and 5 mTorr. These transistors were then compared to transistors fabricated in the CPA. Figure 4.8 shows that, with the same target composition, TFTs fabricated in the Orion V are of comparable quality to those fabricated in the CPA.

Additionally the mobilities of TFTs fabricated in the Orion V are 25% higher than those made in the CPA. This analysis has shown that high quality TFTs fabricated in the Orion V can be achieved at 75 W and 5 mTorr. These TFTs are of sufficient quality to be used in circuit fabrication, specifically the fabrication of ZTO current mirrors. Details of the fabrication and results of these circuits can be found in Sec. 4.2.

4.2 Zinc Tin Oxide Thin-Film Transistor Current Mirrors

The fabrication of current mirrors using zinc tin oxide thin-film transistors is undertaken. Discussion of the fabrication methods used to realize operational circuits is presented, followed by electrical characterization of discrete transistors fabricated on the

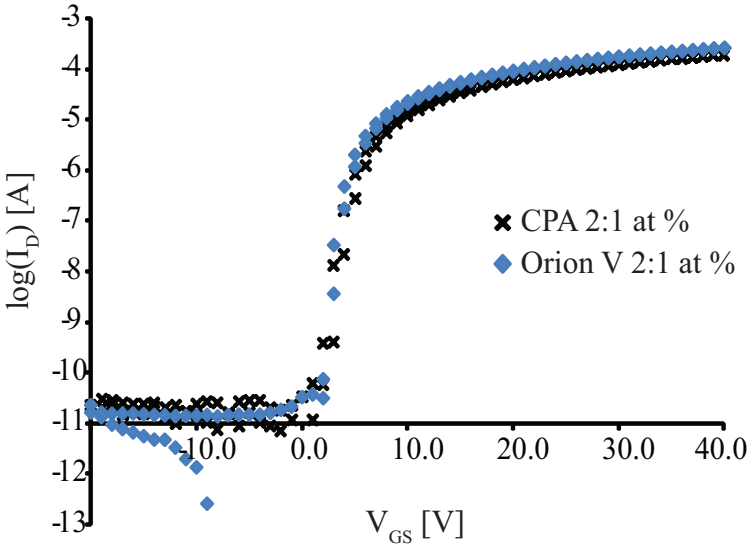


Figure 4.8: ZTO TFTs fabricated on thermal SiO_2 in the AJA Orion V sputter system using a 2:1 at% target compared to TFTs fabricated in the CPA. Both devices show good subthreshold swing and reasonable turn-on voltage.

same substrate as the circuits. Analysis of the current transfer and output characteristics of current mirrors and the sources of mirroring error are presented last. Results for circuits with both the 3:1 ZTO and 2:1 ZTO as the channel layer are presented. The 3:1 ZTO is investigated for use in circuits, despite the reduced transistor performance, for ease of processing. The 3:1 ZTO is more readily etched than 2:1 ZTO making process integration easier. However, the 2:1 ZTO is more physically robust which is important for many applications. The 2:1 ZTO is also more favorable electrically due to enhanced mobility and subthreshold swing. Therefore, both stoichiometries of channel material are used in the current mirror circuits.

The mask set for the substrate includes: discrete transistors with drawn W/L ratios, i.e., the ideal size determined by the mask, of 50 μm / 15 μm (1X), 100 μm / 15 μm

(2X), 250 μm / 15 μm (5X) and 500 μm / 15 μm (10X). These individual transistors are the same size as those used in the current mirror circuits. The current mirrors included on the masks are two-transistor current mirrors of mirroring ratio 1X, 2X, 5X and 10X, with transistor lengths of 15 μm and 30 μm, as well as four-transistor cascode and Wilson current mirrors with mirroring ratios of 1X.

4.2.1 Current Mirror Circuit Fabrication

Current mirror circuits are fabricated utilizing staggered bottom-gate TFTs. The fabrication employs seven primary steps and 4 mylar masks (from CAD/Art Services, Inc.) All circuits are fabricated on 25 x 25 mm Corning 1737 substrates coated with $\sim$150 nm of ITO (from Delta Technologies). The ITO serves as the bottom gate electrode. The gate dielectric is SiO_2 deposited by PECVD. The TFT channel material is either 3:1 or 2:1 sputtered ZTO, processed at minimum substrate-to-target distance and maximum substrate rotation. Source-drain contacts are aluminum deposited by thermal evaporation and patterned using lift-off. All circuits are fabricated using the following process flow.

1. Mask 1: Gate electrodes are defined in the ITO using standard photolithography. The ITO is etched using a 11.8M HCl wet etch for 6 min.

2. The SiO_2 gate dielectric layer of $\sim$100 nm is deposited via PECVD using SiH_4 + He and N_2O precursors.

3. The ZTO channel layer of $\sim$50 nm is deposited using RF magnetron sputtering from a two inch target (from AJA International) of either 3:1 or 2:1 composition. Process pressure, process ambient and RF power are 5 mTorr, Ar/O_2 (90% / 10 %) and 75 W, respectively.

4. Mask 2: The channel layer is patterned using standard photolithography and a 5:1 H_2O:HCl wet etch for 5 s for 3:1 ZTO channels and a 1:1 H_2O:HCl wet etch for 10 s for 2:1 ZTO channels.

5. Mask 3: Contact to the gate electrodes is made through vias opened in the dielectric layer using standard photolithography and a buffered oxide HF wet etch for 1 min.

6. The sample is subjected to a 400 °C furnace anneal for 1 h in air.

7. Mask 4: Aluminum is thermally evaporated for source-drain contacts of ∼200 nm which are patterned via lift-off.

4.2.1.1 Current Mirror Processing Challenges

The 2:1 ZTO, while mechanically and electrically robust, is also very difficult to etch. Wet etching was attempted to pattern the channels of TFTs. All samples were cleaned thoroughly prior to channel patterning, and hexamethyldislazane (HMDS) is used to improve adhesion of photoresist to the ZTO film surface. Improved adhesion helps prevent undercutting of the film during the etch [30]. Undercutting occurs when the etch acid is able to attack the edges of the film under the photoresist and results in features that are smaller than desired. This effect decreases feature size and can have a significant impact on channel width. After the application of HMDS and PR, samples are subjected to a diluted HCl etch for the desired amount of time. A balance must be struck between etch concentration and time to reduce the effects of undercutting. The acid must be concentrated enough to etch the entire film, but not so concentrated that it attacks the edges of the PR pattern resulting in undercutting. The sample must be etched long enough for the entire thickness of film to be removed. The longer the substrate remains submerged in

the wet etch the greater the effects of undercutting. For the 3:1 ZTO, an acid etch dilution of 5:1 H_2O:HCl for 5 s was sufficient to etch the ZTO film with minimal undercutting. For the 2:1 ZTO, an acid etch dilution of 1:1 H_2O:HCl for 10 s was able to etch the film, although undercutting was present.

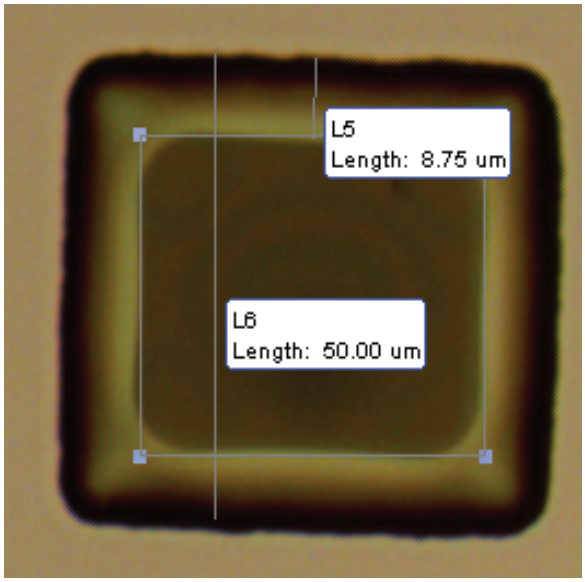


Figure 4.9: Observed undercutting of the 2:1 ZTO channel layer.

Figure 4.9 shows a 2:1 ZTO channel with the PR pattern over top. Undercutting of approximately 9 μm is observed in all directions. The mask set has a built in overlap between the channel and the source or drain contact of 20 μm so the effect of this undercutting on the channel length is insignificant. The effect on the channel width, however, is non-negligible as the overlap on each side is only 5 μm. Therefore, the undercutting of the ZTO channel layer could have an impact on the sizing of the transistors. Moving forward, a consistent etch for ZTO with minimum undercutting is needed.

4.2.2 Discrete Thin-Film Transistor Performance

The mask set used to fabricate current mirror circuits contains discrete TFT arrays that are processed in parallel with the current mirror circuits in order to help characterize the performance of devices that have undergone the entire circuit process flow. These individual transistors allow for the extrapolation of parameters for the TFTs in the circuits, for which individual transfer curve measurement is not possible. Figure 4.10 shows the typical performance of a 3:1 ZTO TFT processed in parallel with the current mirror circuits. The TFTs exhibit a turn-on voltage of $V_{ON} \approx 0$ V, a subthreshold swing (taken at V_{DS} = 1 V) of 1.6 V/decade, a drain current on-to-off ratio (taken at V_{DS} = 10 V) of 10^8, and a maximum average mobility of 6-10 $cm^2V^{-1}s^{-1}$. The gate leakage current increases from its nominal value, to a non-negligible value, at high fields. This increase in gate current is undesirable, as it can lead to increased power consumption and poor device performance. This effect is most likely due to defects in the PECVD deposited gate dielectric as it is not observed in TFTs with thermal SiO_2 investigated in Sec. 4.1.2. A discussion of non-ideal PECVD dielectric effects is presented in Eric Sundholm's M.S. Thesis [31]. The performance of the 3:1 ZTO TFT, while diminished compared to shadow mask processed TFTs reported in Sec. 4.1.2, are still of sufficient quality for use in current mirror circuits.

Figure 4.11 shows the typical performance of 2:1 ZTO TFTs processed in parallel with the current mirror circuits. The transistors exhibit a turn-on voltage of $V_{ON} \approx -1.5V$, a subthreshsold swing of 1 V/decade (taken at $V_{DS} = 10V$), a drain current on-to-off ratio of 10^8 (taken at $V_{DS} = 10V$), and a maximum average mobility of 13-15 $cm^2V^{-1}s^{-1}$. This TFT shows the same gate leakage characteristics as the 3:1 ZTO TFT, further supporting that the effect is a dielectric defect.

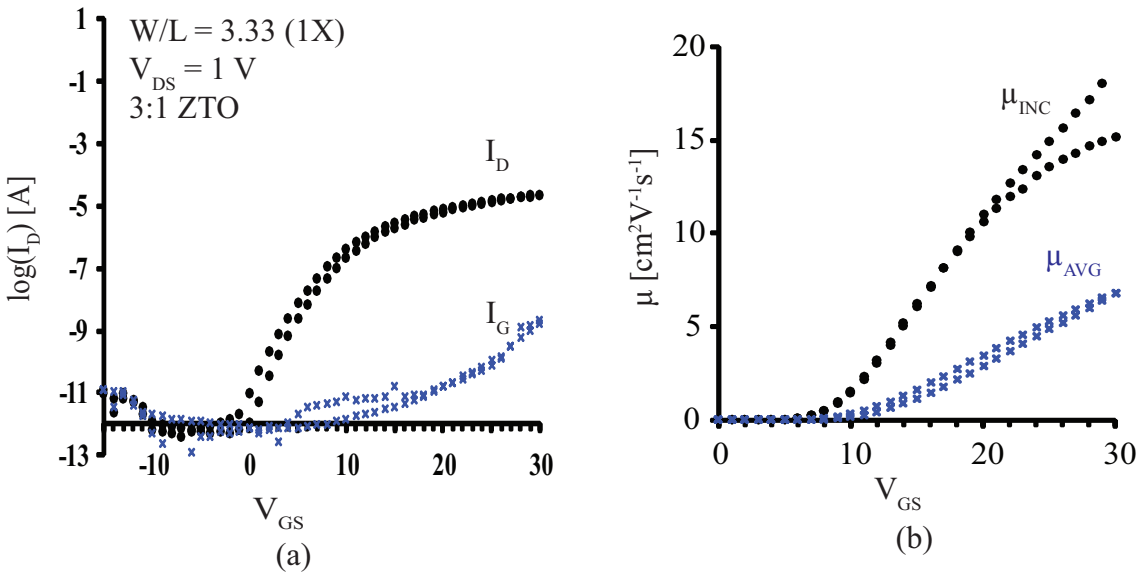


Figure 4.10: (a) $log(I_D) - V_{GS}$ transfer curve and (b) extracted mobility curves for a 3:1 ZTO TFT processed in parallel with current mirror circuits. The device under test is a TFT with a 3:1 ZTO channel layer, a gate dielectric of PECVD SiO_2, a gate electrode of ITO and source-drain contacts of aluminum. This is a 1X transistor with a size of 50 μm /15 μm (W/L =3.33). This transistor shows a larger subthreshold swing, some clockwise hysteresis, and an undescribable gate current increase at high V_{GS}.

The 2:1 ZTO TFT has improved subthreshold swing and mobility and is therefore of higher electrical quality than the 3:1 TFT in Fig. 4.10. However, the 2:1 ZTO TFT has a slightly negative turn-on voltage which is undesirable. All TFTs across the substrate show a similar characteristic, and because the turn-on voltage is matched between transistors, it is expected that the current mirrors will function as desired.

4.2.3 2-TFT Current Mirror Performance

There are two key parameters used to characterize current mirror behavior in this work: the current transfer characteristic and output characteristic. The current transfer characteristic is a measure of output current versus input current, and verifies that the

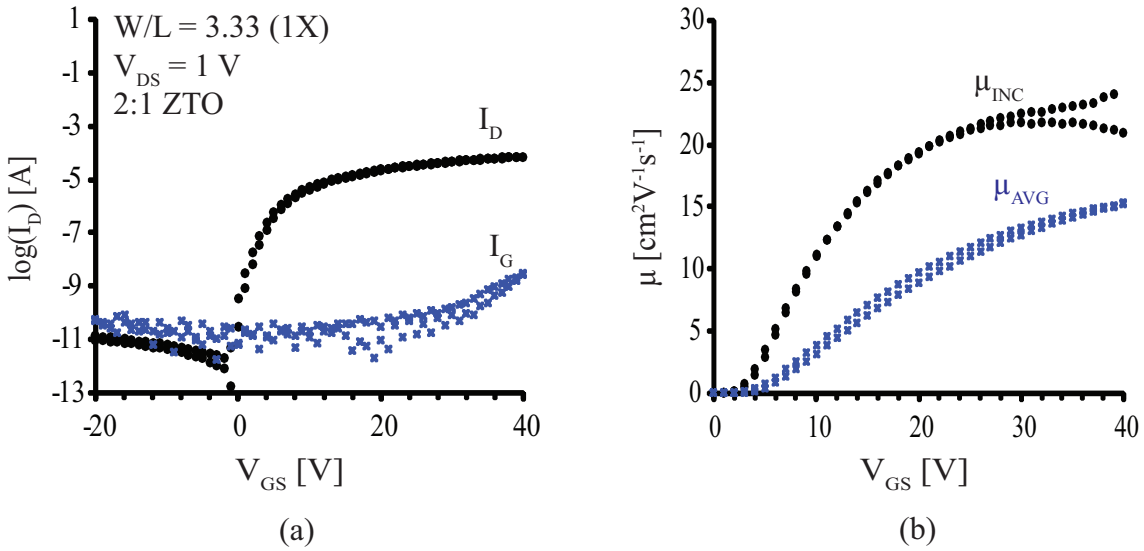


Figure 4.11: (a) $log(I_D) - V_{GS}$ transfer curve and (b) extracted mobility curves for a 2:1 ZTO TFT processed in parallel with current mirror circuits. The device under test is a TFT with a 2:1 ZTO channel layer, a gate dielectric of PECVD SiO_2, a gate electrode of ITO and source-drain contacts of aluminum. This is a 1X transistor with a size of 50 μm /15 μm (W/L =3.33). This transistor shows better subthreshold swing, very little clockwise hysteresis, and an undesirable gate current increase at high V_{GS}.

current mirror is working as detailed in Sec. 2.4. The current mirror output characteristic is a measure of output current versus output voltage, and gives the range of output voltages for which the current mirror provides the correct output current, as well as provides insight into output resistance of the circuit.

4.2.3.1 2-TFT Current Mirror Transfer Characteristic

Figure 4.12 shows the current transfer characteristic for a 1X, current mirror fabricated using a 3:1 ZTO channel material. In a 1X current mirror both transistors have the same W/L ratio. Revisiting Eq. 2.13,

$$\frac{I_{OUT}}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1}, \tag{4.1}$$

in the 1X case the output current should equal the input current when both transistors are the same size.

For the transfer characteristic, the input current of the current mirror is swept from 0 - 200 μA while the output current is monitored. The output voltage is set at 20 V to ensure the output transistor remains in saturation and correct mirroring performance is attained. The minimum output voltage necessary to keep M2 in saturation can be estimated from Eq. 2.15. Using the maximum output current in the transfer characteristic, 300 μA, a mobility of $\mu = 15\ cm^2V^{-1}s^{-1}$, and a 1X transistor size of $W/L = 3.33$, the minimum output voltage necessary is $V_{OUT,min} = 18.3$ V. This voltage is very near the 20 V used as the output voltage in the transfer characteristic. There is a possibility that at the highest currents (i.e. 200 - 300 μA) the transistor M2 could fall out of saturation. Based on the transfer characteristic, however, this does not appear to have a significant effect on the current transfer characteristic and mirroring behavior of the current mirror.

The output current matches the input current exceptionally well through the range of input currents, with an average mirroring ratio of .99X. Figure 4.13 shows the output characteristics of a 1X, 2X, 5X, and 10X branched current mirror, as depicted Fig. 2.7. The 1X and 2X ratios match very well, whereas the 5X and 10X ratios begin to stray from the expected value of 5 and 10 times the input current, respectively. Current mirror gain error is discussed further in Sec. 4.2.4.

4.2.3.2 2-TFT Current Mirror Output Characteristic

The output characteristic measures the ability of the current mirror to accurately transfer the input current to the output over a range of output voltages. Figure 4.14 shows

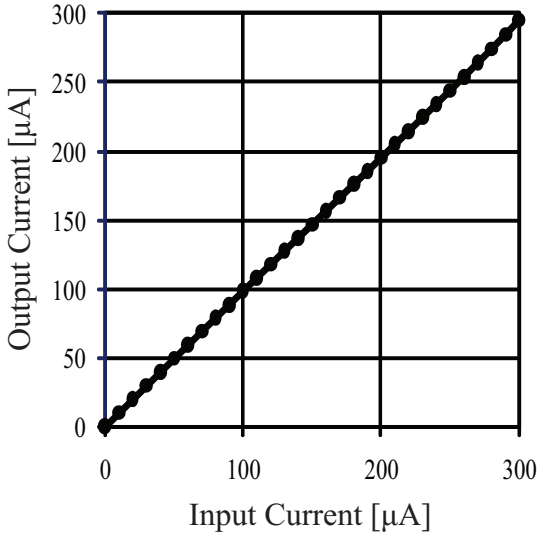


Figure 4.12: The transfer characteristics of a 1X current mirror fabricated using TFTS with a 3:1 ZTO channel layer, a gate dielectric of PECVD SiO_2, a gate electrode of ITO and source-drain contacts of aluminum. This circuit shows excellent matching between the input current and the output current.

that the voltage at which the current stabilizes is the minimum output voltage necessary to assure the output transistor is in saturation, and the current mirror operates as expected: transferring current to the output independent of output voltage. This minimum voltage, $V_{OUT,min}$, depends on the type of current mirror and is specified for each current mirror realized in Sec. 2.4. For the 2-TFT current mirror the minimum output voltage necessary is just the voltage required to keep the output TFT M2 in saturation $V_{OUT,min} = V_{GS} - V_{TH}$.

In addition to specifying the range of useful output voltages, the 2-TFT current mirror output characteristic, being equivalent to the output curve of a single TFT, can also be used to determine the output resistance of the current mirror. Due to channel length modulation, a change in V_{OUT} leads to a change in I_{OUT} even when the output voltage is greater than $V_{OUT,min}$. The output resistance of the current mirror therefore cannot be

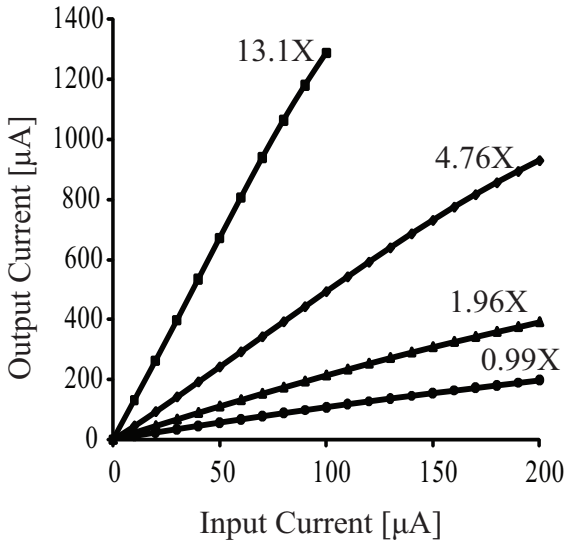


Figure 4.13: Output characteristic of a branched 3:1 ZTO current mirror showing good matching of the 1X, and 2X ratios with matching error becoming larger at the 5X and 10X ratios.

infinite when the output TFT is in saturation, as expected in the ideal case. The output resistance of the current mirror is the inverse of the change in current over the change in voltage,

$$R_{OUT} = \left[\frac{\partial I_{OUT}}{\partial V_{OUT}}\right]^{-1}. \tag{4.2}$$

The output resistance of the current mirror at a given input current, can be found by taking the inverse slope of the straight-line saturation portion of the output characteristic curves. The output resistance of the 1X current mirror, as a function of output current, is plotted in Fig. 4.15. For comparison, the output resistance of a single TFT (extracted from the output curve of an individual transistor on the substrate) is plotted along-side the 2-TFT current mirror output resistance. This plot shows that the output of the 2-TFT current mirror is equal to the output resistance of a single transistor, as expected based on Eq. 2.14.

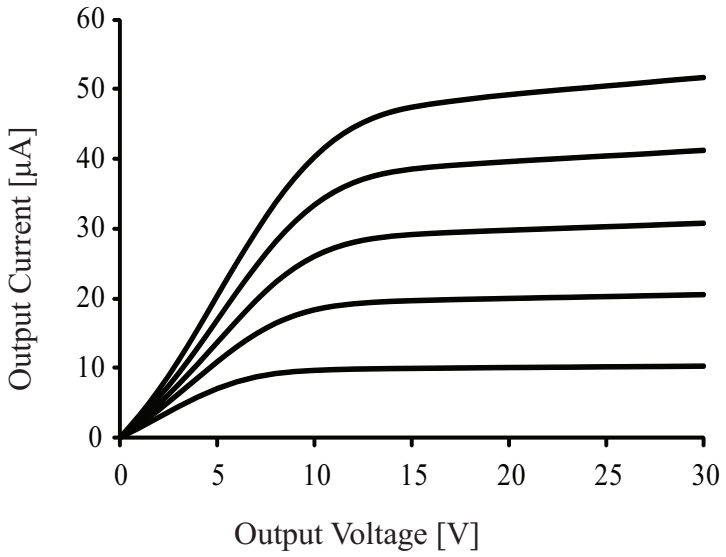


Figure 4.14: The output voltage compliance of a 3:1 ZTO 1X current mirror for input currents from 10 - 50 μA.

Examination of the current mirror output characteristic shows that the current mirror deviates most from ideal behavior when the output current is high. This is exhibited by the increasing slope of the output curves which is more severe for higher output currents. A larger slope of the output curve, correlates to a smaller output resistance, as seen at high currents in Fig. 4.15.

High output resistance is desired in a current mirror so that the circuit accurately delivers current to the load, regardless of output voltage. To illustrate this point, the Norton equivalent circuit of a current mirror is shown in Fig. 4.16. The current mirror can be represented as a current-controlled current source, for which the control current (not shown) is the current mirror input current. This current source is in parallel with the current mirror's output resistance R_{OUT}.

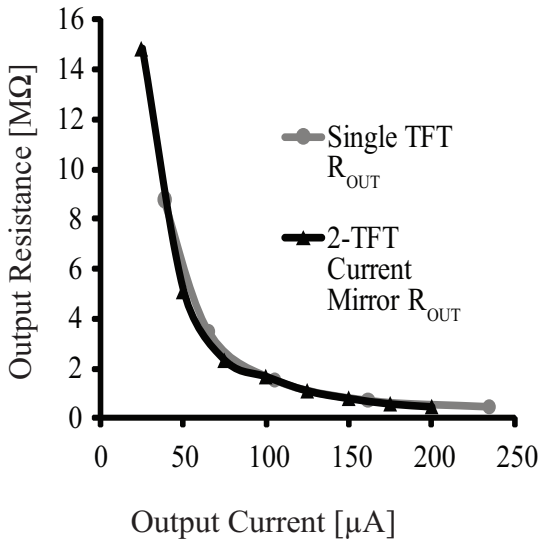


Figure 4.15: Output resistance of a 3:1 1X current mirror as a function of desired output current. The output resistance decreases as the current increases.

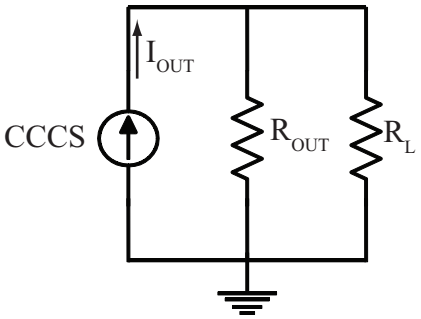


Figure 4.16: Current mirror equivalent circuit. A higher output resistance allows more of the output current to be transferred to the load.

From this equivalent circuit, it is apparent that a higher output resistance results in more of the output current delivered to the load. In practice, a balance must be struck between decreasing current levels to benefit from the higher output resistance at lower current levels, and increasing current levels to increase the speed of the circuit [12]. The basic 2-TFT current mirrors fabricated for this project have an output resistance equal

to the intrinsic resistance of the transistor, r_{o2}, a trend that is observed in Fig. 4.15. As discussed previously, it is advantageous to use other current mirror topologies with a higher output resistance, such as the Wilson and cascode. Circuits with increased output resistance were fabricated and are presented in Sec. 4.2.5.

4.2.4 Current Mirror Error

Through the current transfer and output characteristics of the fabricated circuits, successful current mirror operation has been confirmed. However, not all circuits mirror at the correct ratio throughout the range of operational currents. Figure 4.17 shows the mirroring ratio, α, as a function of input current for 2:1 ZTO current mirrors with desired α values of 1, 2, 5 and 10. The mirroring ratio is expressed as the ratio of output current to input current,

$$\alpha = \frac{I_{OUT}}{I_{IN}}. \tag{4.3}$$

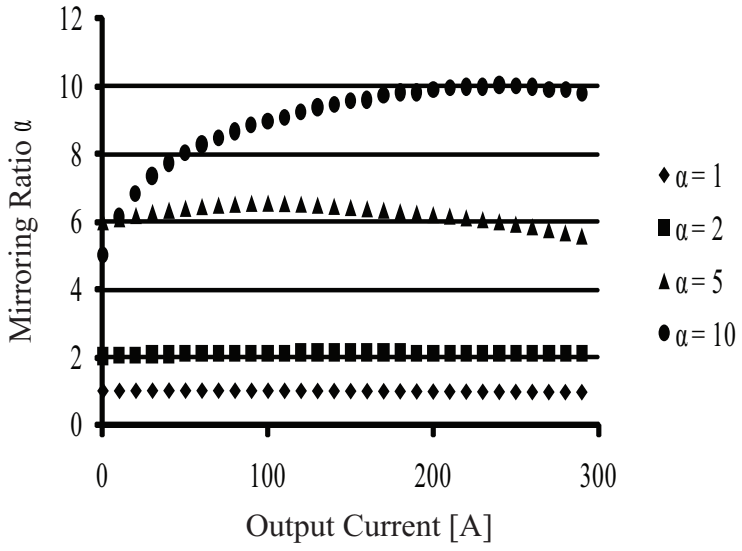


Figure 4.17: The mirroring ratio of 1X, 2X, 5X and 10X 2:1 ZTO current mirrors showing fluctuations in α across the range of operating currents.

The accuracy of a current mirror in transferring the input current to the output current, at the correct ratio, depends on how well matched the TFTs in the circuit are. Mismatches between TFTs can cause the output current to deviate from the ideal value, resulting in a mirroring ratio, α, that is non-ideal. This difference between ideal α and actual α is known as mirroring error. There are several factors that can contribute to mirroring error: geometric mismatch, in the form of TFT device size variation, threshold voltage mismatch between TFTs, and finite output resistance of the TFT due to channel length modulation [32]. Each of these possible sources of error will be examined in detail and evaluated to determine their effect on the current mirror circuits reported herein. Another, more subtle, source of mirroring error is circuit processing variations and non-ideal processing conditions that have a profound and random effect on mirroring performance. Such sources of processing error are: improper substrate cleaning, incomplete removal of photoresist, deposition of unpure source material in thermal evaporation and surface contaminants. These sources of error are difficult to pinpoint and impossible to model accurately. Therefore, they will not be discussed in detail, but their existence should be noted because they can have a significant impact on device performance.

To investigate the effect of geometric mismatch, threshold voltage mismatch, and finite output resistance on current mirror error, the ratio of the input and output saturation currents, including the channel length modulation effect, is elucidating,

$$\alpha = \frac{I_{OUT}}{I_{IN}} = \frac{1/2\mu C_{OX}(W_2/L_2)(V_{GS}-V_{TH2})^2(1+\lambda V_{DS2})}{1/2\mu C_{OX}(W_1/L_1)(V_{GS}-V_{TH1})^2(1+\lambda V_{DS1})}, \tag{4.4}$$

where μ is transistor mobility, C_{OX} is the gate capacitance density, W/L is the transistor width-to-length ratio, V_{TH} is the threshold voltage, and λ is the channel length modulation parameter. Based on measurements of individual TFT transfer curves and capacitance structures across the substrate, mobility, and gate capacitance density are assumed to be

well matched between devices. The effect of the remaining three device parameters can then be investigated individually via the isolation of terms in Eq. 4.5.

$$\alpha = \frac{I_{OUT}}{I_{IN}} = \left(\frac{(W/L)_1}{(W/L)_2}\right)\left(\frac{V_{GS}-V_{TH2}}{V_{GS}-V_{TH1}}\right)^2\left(\frac{1+\lambda V_{DS2}}{1+\lambda V_{DS1}}\right). \tag{4.5}$$

4.2.4.1 Geometric Mismatch Error

Differences in drawn TFT width and length and the actual TFT dimensions may occur due to the processing steps used to fabricate the current mirrors. Possible sources of TFT size error are: mask variation, misalignment of the mask to the previous layers, etching variations, and lift-off effects. These effects are highly random, possibly affecting one transistor differently than a neighboring transistor, and one substrate differently than a previous substrate. These random variations have a direct impact on transistor sizing and thus the mirroring ratio. Assuming geometric mismatch is the only source of error, Eq. 4.5 becomes,

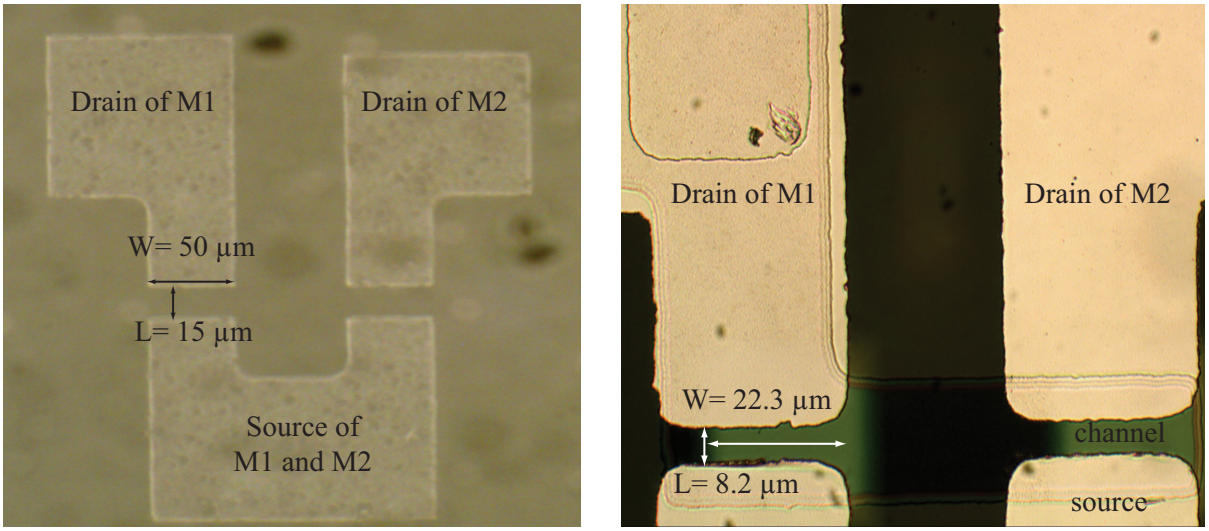
$$\alpha = \frac{I_{OUT}}{I_{IN}} = \frac{(W/L)_2}{(W/L)_1}. \tag{4.6}$$

Equation 4.6 expresses the mirroring ratio assuming geometric TFT mismatch is the only parameter that is not well matched. If the W/L ratio of TFT 1 or TFT 2 changes then the ratio between them changes and modulates α. Geometric errors can contribute greatly to current mirror error, particularly in processing conditions that are difficult to control.

The geometric error is a significant factor in current mirror error for large mirroring ratios (i.e. 5X and 10X). A TFT with a geometric width sizing error of 5 % in a 1X device leads to a mirroring ratio of $\alpha = 1.04$, instead of $\alpha = 1$, for a 10X current mirror the ratio becomes $\alpha = 10.4$. Assuming an input current of 100 μA the output current of the 1X current mirror could vary by $\sim$4 μA. In the 10X case, the output current, ideally 1mA,

could vary as much as ∼40 μA. Geometric mismatch error affects current mirrors with higher mirroring ratios more than those with small mirroring ratios.

It is very difficult to determine the actual device sizes of current mirrors due to the use of lift-off patterning for the source-drain contacts. Figure 4.18(a) is a photograph of the mylar lithography mask used in fabrication. This photograph shows the actual TFT sizes of a 1X current mirror, determined by the width of the drain, and the distance between source and drain of the TFTs. The ideal transistor width is 50 μm and the ideal transistor length is 15 μm as depicted in Fig. 4.18(a). Figure 4.18(b) shows the actual source-drain contacts as imaged by an optical microscope. This photograph shows an



(a) (b)

Figure 4.18: (a) Photograph from a circuit mask of a 1X current mirror showing drawn width and length of the transistors. (b) Photograph of the actual 1X current mirror, showing an apparent reduction in transistor width and length.

apparent reduction in the size of the transistors to from W = 50 μm to W = 22.3 μm, and L = 15 μm L = 8.2 μm after aluminum source-drain processing. The reduction of

TFT size appears to be much larger than expected and the effects of lift-off patterning are investigated to determine if this reduction in TFT length is believable.

The apparent size reduction in gate length can be explained by examining the lift-off processes used to pattern the source and drain contacts in further detail. The development of the photoresist in a wet developer creates sloped side walls on the photoresist structures, as seen in Fig. 4.19. The aluminum is then deposited on top of the photoresist

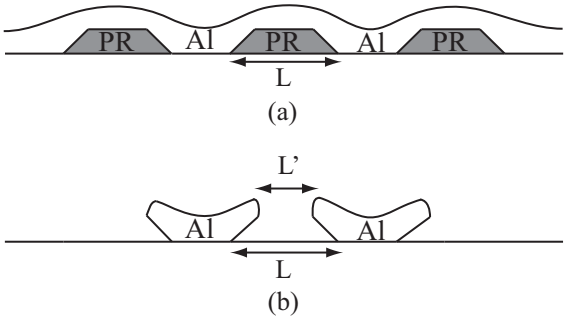


Figure 4.19: (a) Photoresist and aluminum layers for lift-off patterning of source-drain contacts (b) Aluminum structures after photoresist has been removed, showing possible differences in measured gate length from actual length.

structures. When the sample is placed in acetone to remove the photoresist the aluminum remaining has a sloped structure that effects the apparent length, L'. Imaging from the top with an optical microscope will measure the smaller dimension L', instead of the actual device length L. This explains the observed, but most likely false, decrease in TFT gate length. Optical imaging of the TFT to determine the variation of actual device sizes from the drawn device sizes gives an unrealistic estimation of TFT gate length.

The decrease in transistor width can be explained by the misalignment of the channel, which is not evenly centered about the source and drain, but instead offset to the right. This offset can be seen in Fig. 4.18(b) as the light-colored region between the drain and source contacts that is shifted to the right. This offset is due to poor mask alignment

during the source-drain photolithography step. Such misalignment is common, especially when using manual mask alignment, and can significantly decrease the actual gate width.

Determining the actual TFT dimensions is very difficult optically because of the sloped side wall structures that result from lift-off. Without knowledge of the actual TFT dimensions, it is challenging to estimate the effect of geometric mismatch on mirroring error. This source of error, because its effects are not precisely known, obscures the attribution of further error mechanisms such as threshold voltage mismatch and output resistance. This results in an inability to pinpoint the dominant source of error. It can be assumed that the TFTs fabricated for the reported circuits have significant sizing error due to processing conditions. Non-idealities such as manual mask alignment, use of mylar masks, and process variations in etching and cleaning contribute to sizing error. It is a complex task to measure the actual size discrepancies between ideal TFT size (as defined by the mask) and actual TFT size. Improved processing conditions and circuit layout techniques would help decrease TFT size error by making the circuits less dependant on process variation and TFT size. If geometric error was reduced, more insight into the remaining error mechanisms would be possible.

4.2.4.2 Threshold Voltage Mismatch Error

Transfer curves were obtained for the individual transistors at variations locations across the substrate. From these measurements threshold voltage was estimated using the method outlined in Sec. 3.6.2. Threshold voltage was found to be 8.5 V on average with a standard deviation of 0.5 V and a maximum variance of 1.2 V. The threshold voltage information gathered is from a small sample set across the substrate and is not meant to

be statistically complete, but instead gives a starting point from which to do analysis on threshold voltage mismatch error.

Assuming all other aspects of the transistor are well matched, the mirroring ratio due to the effects of threshold voltage mismatch can be distilled from Eq. 4.5 as,

$$\alpha = \frac{I_{OUT}}{I_{IN}} = \left(\frac{(W/L)_1}{(W/L)_2}\right)\frac{(V_{GS}-V_{TH2})^2}{(V_{GS}-V_{TH1})^2}. \tag{4.7}$$

If average threshold voltage is defined as $V_{TH} = \frac{1}{2}(V_{TH1}+V_{TH2})$ and the threshold voltage difference is $\Delta V_{TH} = V_{TH1} - V_{TH2}$ then assuming all other parameters are well matched, Eq. 4.7 may be recast as,

$$\alpha \cong \left(\frac{(W/L)_1}{(W/L)_2}\right)\left(1 - \frac{2\Delta V_{TH}}{V_{GS}-V_{TH}}\right). \tag{4.8}$$

The effect of threshold voltage variation on mirroring ratio decreases with increasing current. Increased current is provided by an increase in V_{GS}, as V_{GS} becomes larger the change in threshold voltage is a smaller percentage of V_{GS} and affects the error less as seen in the denominator of Eq. 4.8.

Figure 4.17 shows that the 10X current mirror ($\alpha = 10$) has a significant amount of error at low currents but stabilizes at higher currents. Therefore, it is possible that threshold voltage mismatch could be a source of error. The distance between the two TFTs of the 10X current mirror is greater due to the size of M2, so it is more likely that the two TFTs would suffer from threshold voltage mismatch. Using the average V_{TH} (8.4 V) and maximum V_{TH} variation (1.2 V) extracted from individual TFT curves, Fig. 4.20 shows the actual mirroring ratio (circles) for a 10X current mirror and the calculated ratio (diamonds) assuming threshold voltage mismatch is the only source of error.

The shape of the curve agrees well with that of the observed mirroring ratio, although the calculated value of α never reaches the correct value. This is a sign that there

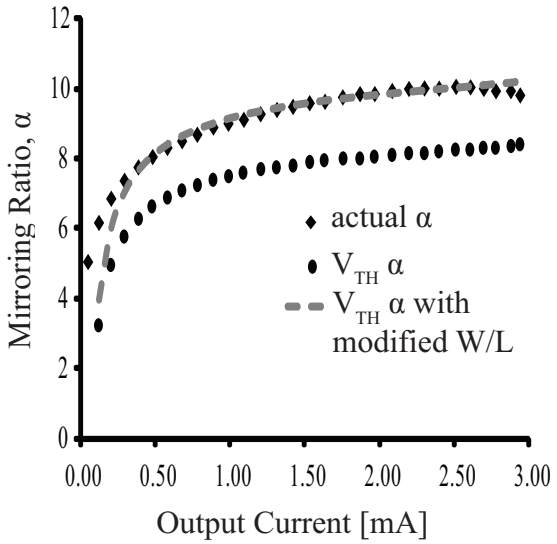


Figure 4.20: Actual measured mirroring ratio, α, as a function of output current and α determined only by threshold voltage mismatch.

is another error effect present. The actual and calculated curves seem to differ from each other by a rigid offset. Geometric error could account for this rigid shift in the mirroring ratio as it is the only error mechanism resulting in a voltage- and current-independent modification of α. If the W/L ratio in Eq. 4.8 is modified to be 12.2 instead of 10, then the calculated mirroring ratio (dashed line) matches very closely to the actual mirroring ratio. This is evidence that threshold voltage mismatch and geometric mismatch are significant factors in establishing current mirror error, especially for circuits containing large devices and high mirroring ratios.

Process-dependant parameters, such as V_{TH}, are best matched when transistors are close together, larger mirroring ratios force the transistors further apart and exacerbate parameter mismatch, thus incurring more mirroring error [33]. Robust circuit layout can mitigate the effects of random sizing error. The nature of this work, however, is to show

proof-of-concept for working ZTO current mirrors. Therefore, such design practices were not employed.

4.2.4.3 Finite Output Resistance Error

All TFTs have a finite output resistance which is attributed to channel length modulation. The effect of finite output resistance on mirroring ratio can be seen in the output characteristic of the 1X 2:1 ZTO current mirror with output currents ranging from 25 - 300 μA as seen in Fig. 4.21. When channel length modulation is present, the change in output voltage results in a corresponding change in output current which defines a finite output resistance. The effect of finite output resistance on current mirror error can

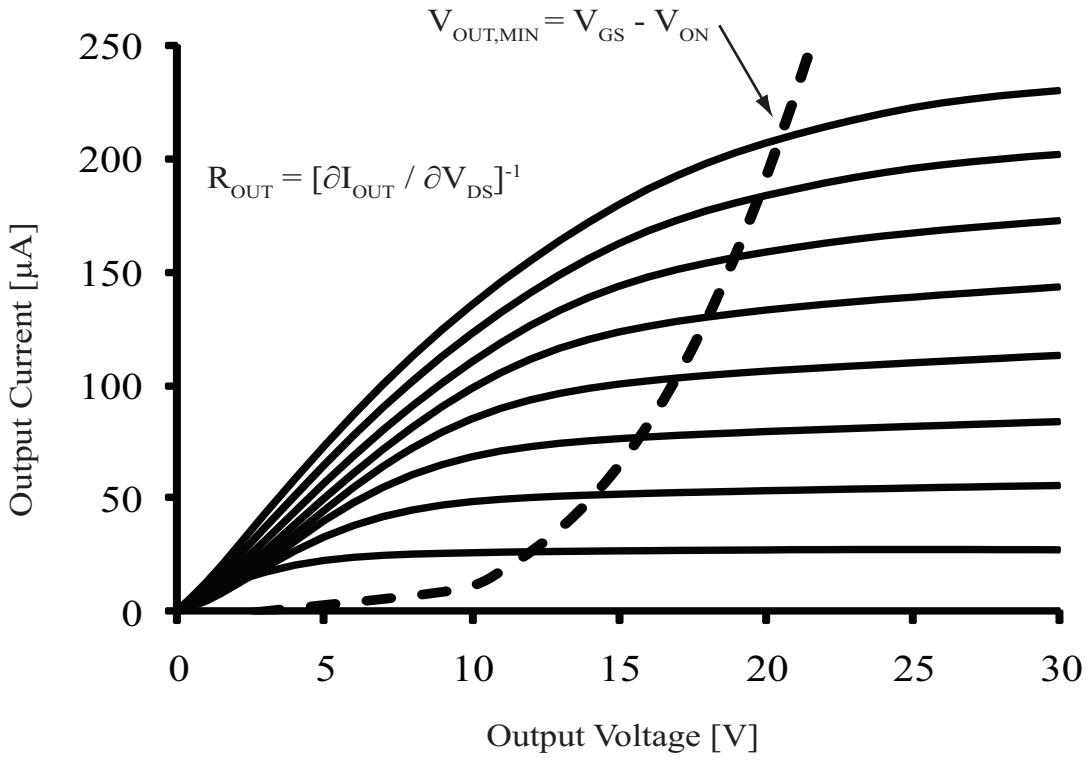


Figure 4.21: The current mirror output characteristic, $I_{OUT} - V_{OUT}$, for a 2:1 ZTO current mirror used to extract output resistance as a function of the output current.

be investigated by assuming the TFTs are well matched geometrically and have identical threshold voltages. Equation 4.5 (assuming a well matched 1X current mirror) is then simplified to,

$$\alpha = \frac{I_{OUT}}{I_{IN}} = \frac{1+\lambda V_{DS2}}{1+\lambda V_{DS1}}, \tag{4.9}$$

where λ is the channel length modulation parameter (discussed in greater detail in Sec. 2.3.1). Equation 4.9 shows that when λ is large enough, the difference in the drain-to-source voltages of each TFT impacts the mirroring ratio. This effect is unavoidable, as all TFTs exhibit some degree of channel length modulation.

In order to investigate whether or not channel length modulation is a significant source of error for the fabricated current mirrors, it is necessary to estimate λ. Output resistance is a product of channel length modulation and can be used to estimate the parameter λ. Starting from the output resistance expression, Eq. 4.2, the partial derivative of the output current with respect to output voltage can be determined using the TFT saturation equation, including the effects of channel length modulation,

$$\frac{\partial I_{OUT}}{\partial V_{OUT}} = \lambda \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2. \tag{4.10}$$

Recognizing that Eq. 4.10 is just the ideal TFT drain current, without the effects of channel length modulation, multiplied by λ, the output resistance can be redefined as,

$$R_{OUT} = \left[\frac{\partial I_{OUT}}{\partial V_{OUT}} \right]^{-1} = \frac{1}{\lambda I_{OUT}}, \tag{4.11}$$

where I_{OUT} is the ideal output current ignoring the effects of channel length modulation, determined by the ideal TFT saturation current expression. Equation 4.11 shows that λ can be estimated if the output resistance is known. The output resistance of the current mirror, for a given output current, can be found by taking the straight-line slope of the sat-

uration portion of the output characteristic in Fig. 4.21. The output resistance estimated via this method is plotted in Fig. 4.22.

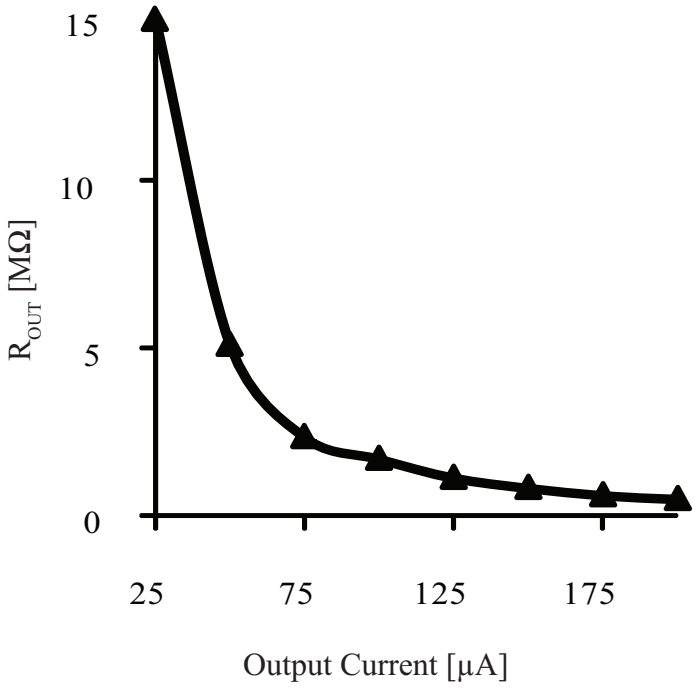


Figure 4.22: Output resistance of a 2:1 ZTO current mirror as a function of desired output current

The channel length modulation parameter, λ, is estimated by plotting the inverse of output resistance versus ideal output current, $1/R_{OUT} = \lambda I_{OUT}$, as shown in Fig. 4.23. The slope of this line yields λ = 0.0091 V^{-1} for a 1X 2:1 ZTO current mirror. Using this value for λ the expected mirroring ratio, when channel length modulation is the only parameter determining mirroring ratio, can be plotted. The same analysis can be done to find λ for the 2X, and 5X current mirrors as well. Figure 4.24 shows the actual mirroring ratio, as well as a calculated mirroring ratio based on channel length modulation effects for a 1X, 2X, and 5X current mirror, assuming all other device parameters are well matched. The actual mirroring ratio and the calculated mirroring ratio have a similar trend at high

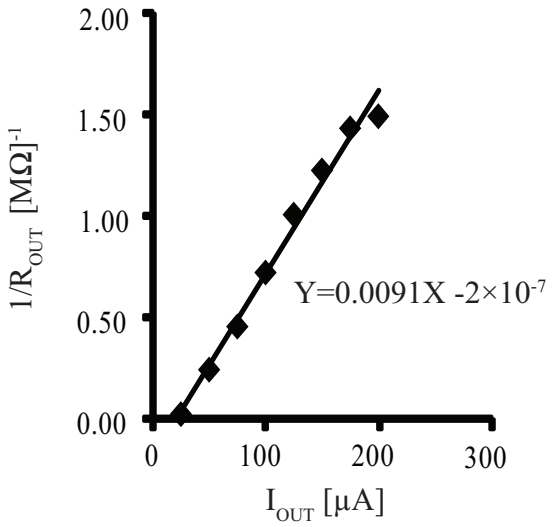


Figure 4.23: Estimation of $\lambda = 0.0091\ V^{-1}$ from the output resistance of a 1X 2:1 ZTO current mirror.

output currents, in that the mirroring ratio decreases with increasing current. However, a rigid shift exists between actual and calculated mirroring ratios. This offset is attributed to geometric mismatch between the TFTs of the current mirror. Geometric mismatch is the only source of error that is independent of output current and output voltage.

Based on the observed current mirror output characteristic in Fig. 4.21, it is likely that channel length modulation effects are most pronounced at high currents when the output resistance is the smallest and the current mirror fails to maintain the output current independent of the output voltage. It is difficult to tell for certain which error mechanism is dominant in the current mirrors, but the agreement between the calculated mirroring ratio, dependent on output resistance effects, and actual mirroring ratio shows that the presence of finite output resistance plays a role in current mirror error. The limitation of

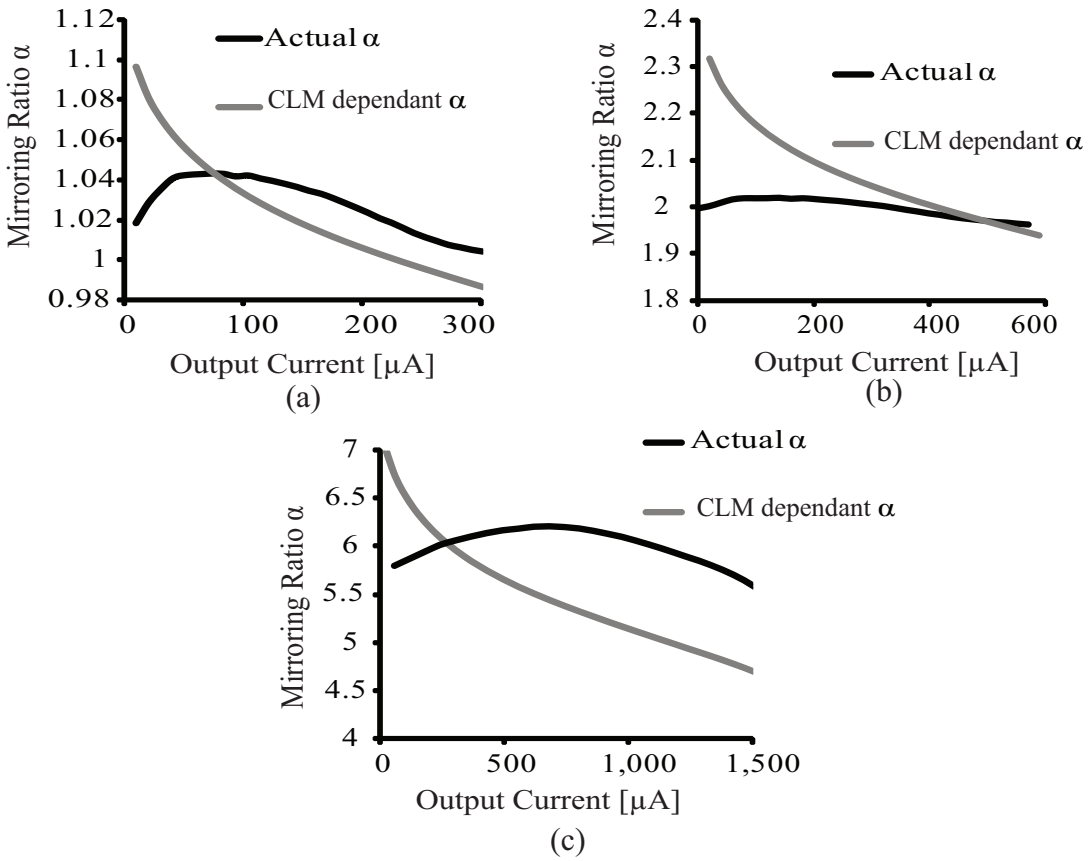


Figure 4.24: Actual measured mirroring ratio, α, as a function of output current and α determined assuming only channel length modulation effects are operative for (a) a 1X current mirror, (b) a 2X current mirror, and (c) a 5X current mirror.

mirroring accuracy based on finite output resistance is unavoidable as it is brought on by the channel length modulation phenomenon which is a natural part of TFT behavior.

There are several ways to overcome the low output resistance and its associated mirroring error. The channel length of the TFTs used can be increased so that the shrinking of the channel length, due to channel length modulation, is minimal compared to overall device length. The operating conditions of the current mirror can be limited to keep the current mirror operating at low current levels. The current mirror output characteristics

show that current levels below $\sim 100\mu$A have relatively invariant output current with respect to output voltage. Finally, more complex current mirror circuits (i.e., the cascode and Wilson), with stacked output transistors have higher output resistance and can be used in situations where a high output resistance is necessary.

4.2.5 Cascode and Wilson Current Mirror Performance

Alternatives to the standard 2-TFT current mirror are commonly employed to increase the output resistance of the circuit, as discussed in Sec. 2.4.1. Results for 1X cascode and Wilson current mirrors are presented. Figure 4.25 shows the mirroring ratio for the 1X current mirrors for each of the three configurations fabricated. The mirroring ratio for the 2-TFT current mirror shows a relatively constant ratio across the range of output currents. The Wilson current mirror also has a relatively constant ratio α, although it is lower than expected. The reduced mirroring ratio, because it is a rigid shift downward, is most likely due to geometric TFT mismatch error, which is the only error to manifest as a rigid shift in α.

The cascode current mirror has a decreasing mirroring ratio with increasing output current, as shown in Fig. 4.25. This decreasing mirroring ratio, is attributed to insufficient output voltage. Both the cascode and the Wilson current mirrors require an output voltage of $V_{OUT,min} = V_{TH} + 2(V_{GS} - V_{TH})$. This voltage is significantly higher than the required output voltage for the 2-TFT current mirror. The minimum output voltage for a cascode or Wilson current mirror, at output currents greater than 200 μA, is in excess of 30 V. Therefore, the steady decrease in α, occurs as the output TFTs drops out of saturation. Unfortunately, voltages in excess of 30 V are likely to cause dielectric breakdown and

circuit failure. The cascode circuit was tested with an output voltage of 20 V to avoid dielectric breakdown and obtain transfer and output characteristic data.

Both the Wilson and cascode circuits fabricated suffered from low yield and poor reliability. The data set was small and broad conclusions are unreliable. The increased complexity of these circuits, along with non-optimal circuit layout, resulting in geometric and other error, is likely to contribute to the mirroring ratio trends observed.

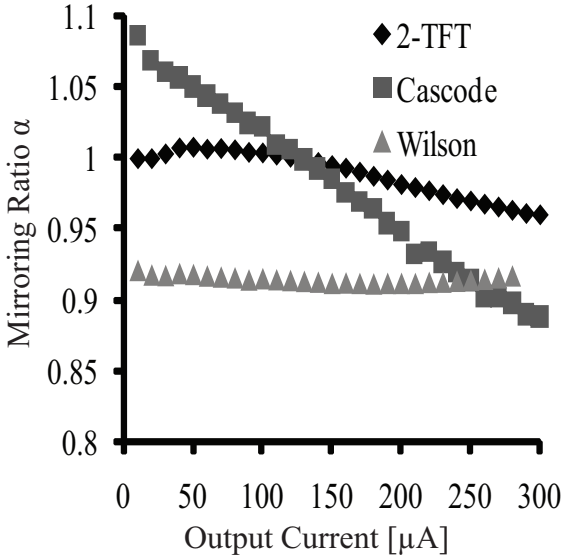


Figure 4.25: Mirroring ratios for 1X 2-TFT cascode and Wilson current mirrors.

Figure 4.26 shows the output characteristic for all three current mirror topologies. All three characteristics agree with the curves presented by Allen and Holberg in [32]. The Wilson current mirror, Fig. 4.26(c), has a unique design which uses feedback to resist changes in output current due to changes in output voltage. This leads to a a different output characteristic shape than observed with the other two current mirrors which should not be confused with series resistance effects.

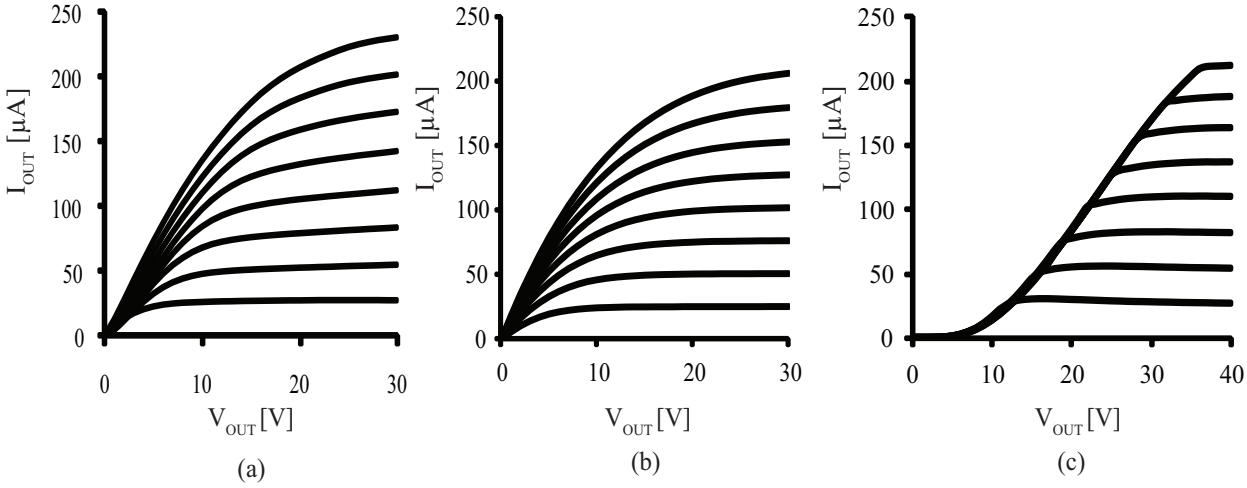


Figure 4.26: Current mirror output characteristics for (a) the standard 2-TFT current mirror, (b) the cascode current mirror, and (c) the Wilson current mirror

From the output characteristics of the cascode and Wilson current mirrors, the output resistance of each of the current mirrors can be calculated. Figure 4.27 shows the output resistance of all three current mirror circuits as a function of desired output current. As expected the cascode and Wilson current mirrors have increased output resistance when compared to the 2-TFT current mirror. Ideally, the output resistance of the cascode and Wilson current mirrors should be equivalent. As seen in Fig. 4.27, the output resistances of the Wilson current mirror is similar to that of the cascode. However, the output resistance of both the cascode and Wilson are lower than predicted by the output resistance expression for the circuits,

$$R_{OUT} \cong g_{m4} r_{o4} r_{02}, \tag{4.12}$$

if g_{m4} is estimated as [12],

$$g_{m4} = \sqrt{2\mu(W/L)I_{OUT}}. \tag{4.13}$$

Equations 4.12 and 4.13 predict an output resistance, at 50 μA, of 85 MΩ, which is much higher than the observed output resistance. This is could be attributed to a transconductance, g_m which is lower than calculated due to the gate voltage dependant nature of AOS TFT mobility.

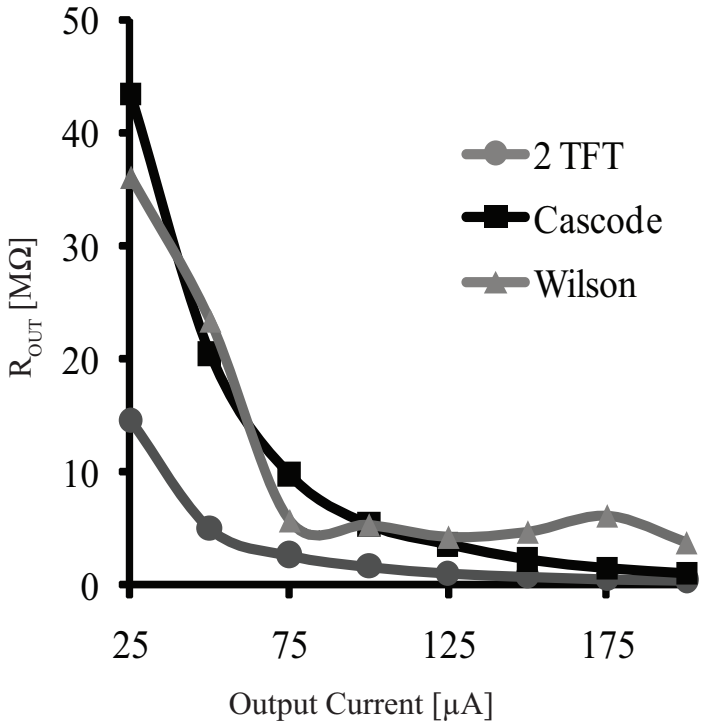


Figure 4.27: Output resistance of the 2-TFT, cascode and Wilson current mirrors. The cascode and Wilson circuits have improved output resistance over the 2-TFT current mirror as expected.

The output resistances of the cascode and Wilson current mirrors are higher than the 2-TFT current mirror, as expected. The extracted output resistances are lower than the calculated output resistances for the cascode and Wilson current mirrors. Unfortunately, this increase in output resistance did not lead to improved current mirror performance due to the increased complexity and decreased reliability of the circuits. The effects of

processing non-idealities and TFT size mismatch greatly influenced the current mirrors due to the increased size and complexity of the circuits. These problems could be mitigated through use of a more robust circuit layout. For relatively simple applications such as AMOLED pixel drivers the 2-TFT configuration may be sufficient. In order to move beyond proof-of-concept circuits better processing and circuit layout is required.

5. CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

This chapter is a summary of the conclusions drawn from the successful fabrication of zinc tin oxide thin-film transistor current mirror circuits. Insights gained from the results presented lead to a discussion of the possibilities for future work.

5.1 Conclusions

Current mirrors are an integral part of analog circuitry and the current mirrors presented herein represent a first step towards using AOS in analog circuit applications. Furthermore, the use of current mirrors in pixel drivers for AMOLED displays is an intriguing application for the circuits presented. The characterization of ZTO TFTs in Sec. 4.2.2 shows strong electrical performance, with mobility greater than the competing technology, a-Si. Therefore, these TFTs are suitable for use in AMOLED pixel drivers and other analog circuit applications that have not yet been realized by TFTs.

The successful fabrication of current mirrors with different mirroring ratios and architectures was presented. The current mirrors fabricated exhibit good matching at the 1X and 2X ratios with minimum mirroring error. As the mirroring ratio increases, and concomitantly the size of the output transistor M2, geometric mismatch and threshold voltage mismatch contribute to the mirroring error. Current mirrors with mirroring ratios of 5X and 10X exhibit significant variations in the mirroring ratio, across the range of output currents.

There are three primary contributions to the mirroring error in the current mirrors fabricated: geometric mismatch between TFTs, threshold voltage between TFTs and the finite output resistance of TFTs.

Geometric errors due to TFT size mismatch stem from imperfect processing, i.e., the use of mylar masks, mask misalignment, etching inconsistencies (e.g., undercutting and/or insufficient etching), and lift-off effects (e.g., source-drain contacts with sloped sidewalls, and jagged pattern edges). These fluctuations in TFT size are difficult to quantify. Thus, the extent to which geometric mismatch contributes to mirroring error cannot be independently established. However, geometric mismatch is likely the primary source of mirroring error because processing variations introduce the majority of non-idealities into current mirrors and have a direct impact on TFT size. Geometric mismatches must be reduced in order to improve current mirror performance so that secondary sources of current mirror error can be evaluated. Geometric mismatch can be minimized by employing careful processing techniques, robust circuit layout, developing a ZTO etch with minimal undercutting, and by using of chrome lithography masks.

The effects of threshold voltage mismatch on current mirror error are most important for a current mirror with a large mirroring ratio. The physical size of the output TFT of a current mirror with a large mirroring ratio is much bigger and therefore further away from the input TFT . Physical proximity is an important factor in attaining circuits with well matched TFTs. The effects of threshold voltage variation between TFTs can be diminished through establishing tight process control and starting with robust circuit layout that groups TFTs as closely together as possible.

All current mirrors have a finite output resistance that decreases as the output current increases. The effect of a finite and decreasing output resistance makes the current

mirror more susceptible to variations in the output voltage, especially when the desired output current is large. This can result in a deviation of the output current from the ideal value which creates mirroring error. Output resistance is the result of channel length modulation, an unavoidable characteristic of the TFT. The effects of finite output resistance and channel length modulation are most pronounced in the 2-TFT current mirror configuration because the output resistance of the circuit depends solely on the output resistance of the single output TFT. The decreased output resistance at high current levels restricts the operation of these current mirrors to a maximum output current level. Operational currents below 100 μA yield an output resistance that is sufficiently high to keep the output current relatively invariant to a change in output voltage.

While channel length modulation is inescapable in a TFT and will always result in a finite output resistance, there are steps that can be taken to reduce its effect on mirroring ratio. Designing circuits with TFTs of longer channel length would yield circuits that are less affected by channel length modulation. Additionally, improved layout technique (e.g, transistor fingering where multiple smaller transistors are connected in parallel to yield one larger transistor, and use of a common centroid design [33]) and alternative current mirror topologies with enhanced output resistance can be implemented in order to mitigate low output resistance problems. For many low current applications the 2-TFT current mirror should have an acceptable output resistance.

More complex current mirror architectures, i.e., the cascode and the Wilson, were attempted because they utilize stacked output TFTs that amplify the output resistance. These more complex current mirrors were realized using a 1X mirroring ratio. Results showed that both circuits had improved output resistance compared to the 2-TFT current mirror. Both the cascode and Wilson showed variation in the mirroring ratio across the

range of output currents, and had a mirroring ratio that was non-ideal. The larger required substrate area and the increased circuit complexity associated with these circuits, caused the current mirrors to be more susceptible to mirroring error, especially in the form of processing non-idealities leading to geometric mismatch. The reliability and yield of these circuits was very low, and a large sample size from which to draw conclusions was not available. Possible causes for the low yield are dielectric failure and inconsistent etching. As with the 2-TFT current mirrors, gaining control of geometric error and implementing the best possible process control will help increase circuit yield and performance.

5.1.1 Recommendations for Future Work

The circuit layout and processing methods used to fabricate current mirror circuits were sufficient to provide a proof-of-concept that ZTO TFTs could be used in an analog circuit application. Mirroring error must be addressed in order for ZTO current mirror circuits to be implemented as fully functional AMOLED pixel drivers and as components in more complex analog circuits such as amplifiers. In future work, there are several steps that should be taken. Collaboration with an analog circuit designer to provide a more robust circuit layout and decrease the effects of geometric and threshold voltage mismatch is needed. The use of a more accurate lithography mask, perhaps a direct write laser chrome mask, would also serve to decrease the amount of error by providing more accurate pattern transfer to the substrate. There are several processing issues that must also be addressed in order to help reduce the amount of mirroring error. A successful etch for 2:1 ZTO, with minimal undercutting, must be developed. Lift-off processing of the source-drain contacts is not ideal for the realization of clean pattern transfer, and can lead to geometric error. Moving forward, it would be advantageous to avoid lift-off patterning.

This could be accomplished by using a different TFT configuration (i.e. staggered top-gate) although this would result in a new set of processing concerns. One of the main conclusions drawn from the fabrication of ZTO TFT current mirrors is that control of the mirroring error depends greatly on control of process integration issues. Precise control of TFT size and threshold voltage is vital to the success of ZTO circuits.

The future of this work should continue to advance the case for the implementation of AOS in many facets of large area electronics. The current mirror is a foundation piece in the analog circuit toolbox; therefore, the work presented should be leveraged to create more complex circuitry that is necessary in large area electronics. Examples of such circuitry are: a full AMOLED pixel driver, an AMOLED source driver [20], and signal conditioning or amplification circuits including the long term goal of an all enhancement-mode N-TFT operational amplifier [34]. Regardless of the form the next AOS circuits take, it is clear that processing control will be necessary to ensure that transistors in the current mirror are well matched and therefore reduce mirroring error.

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