AN ABSTRACT OF THE THESIS OF

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in Electrical and Electronics Engineering (Major) presented on April 16, 1971 (Date)

Title: DESIGN OF HIGH SPEED PAPER TAPE READER INTERFACE FOR PDP-8/L COMPUTER SYSTEM

Abstract approved: Redacted for privacy

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This thesis is concerned with the design of the high speed tape read-out and tape feed control circuits and interface to the PDP-8/L Computer system. The system was designed to operate under the programmed data transfer mode of the computer, and is compatible with the computer manufacturer's system.

The circuit components of the tape read-out circuits were experimentally determined for the best performance and the cost of the major units of the system, excluding the labor cost, was estimated. This paper indicates how a simple, inexpensive and reliable interface can be developed by using commercially available integrated circuits.

Design of High Speed Paper Tape Reader Interface for PDP-8/L Computer System

by

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A THESIS

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Master of Science

June 1971

APPROVED:

Redacted for privacy

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Date thesis is presented April 16, 1971

Typed by Barbara Eby for Chansak Laoteppitaks

ACKNOWLEDGEMENT

The author wishes to express gratitude to Professor D. L. Amort for his patience, advice, suggestion, and assistance in directing the design and writing of this thesis.

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LIST OF TERMS

Term	Description	Dimension
I_1	Total base circuit current	ma
I_b	Base current	ma
$I_{b(min)}$	Minimum base current required to drive the transistor into saturation	ma
I_c	Collector current	ma
I_2	By-pass current to ground in the base circuit	ma
$V_{ce(sat)}$	Collector-emitter saturation voltage	volt
V_o	Output voltage	volt
$V_{be(sat)}$	Base-emitter saturation voltage	volt
$V_{be(cutin)}$	Base-emitter cutin voltage	volt
$h_{fe(min)}$	Minimum forward current gain	dimensionless

DESIGN OF HIGH SPEED PAPER TAPE READER INTERFACE FOR PDP-8/L COMPUTER SYSTEM

I. INTRODUCTION

Loading information into the PDP-8/L Computer via the standard Teletype Model 33 ASR (10 characters/sec) is slow and time consuming. In order to speed up the read-in operation, a high speed paper tape reader and interface were developed.

The cost of the system was minimized by making use of the existing unused seven-channel Ferranti High Speed Tape Reader. Some mechanical modifications were made to read an eight-channel tape and nine sets of tape read-out circuits and a tape feed control circuit were developed. The tape reader is able to read several types of the commercial paper tape: the black, gray and green paper tape.

The interface was designed to keep the reader operating at its maximum speed (250 characters/sec) and to realize full benefit of the built-in control features of the PDP-8/L Computer programmed input/output (I/O) transfer (1). All requirements imposed by the computer bussed system are met (1).

The high speed paper tape reader and interface which have been commercially available are expensive. Therefore, the development of this system is based on low cost as well as reliability and simplicity.

II. SYSTEM ORGANIZATION

The high speed paper tape reader and interface system consist of three major functional units as shown in Figure 1 are:

1. tape reader unit
2. device selector
3. reader control

The tape reader unit will be discussed in detail in the next chapter. The reader is assigned the device code or I/O device address 01_8. Bit 3 through 8 of an I/O transfer instruction serve as a device code, and once the reader is enabled it regenerates the computer generated programmed I/O pulse (IOP) as IOT command and transmits these pulses to the reader control unit. Figure 2 shows the logic of the device selector. Instruction bit, IOP pulse, IOT pulse and event time correspondence is as follow (1):

Instruction Bit	IOP Pulse	IOT Pulse	Event Time	Used For
11	IOP1	IOT1	1	Sampling Reader Flag, Skipping
10	IOP2	IOT2	2	Clearing Flag, Loading Accumulator
9	IOP4	IOT4	3	Clearing Buffer and Reading

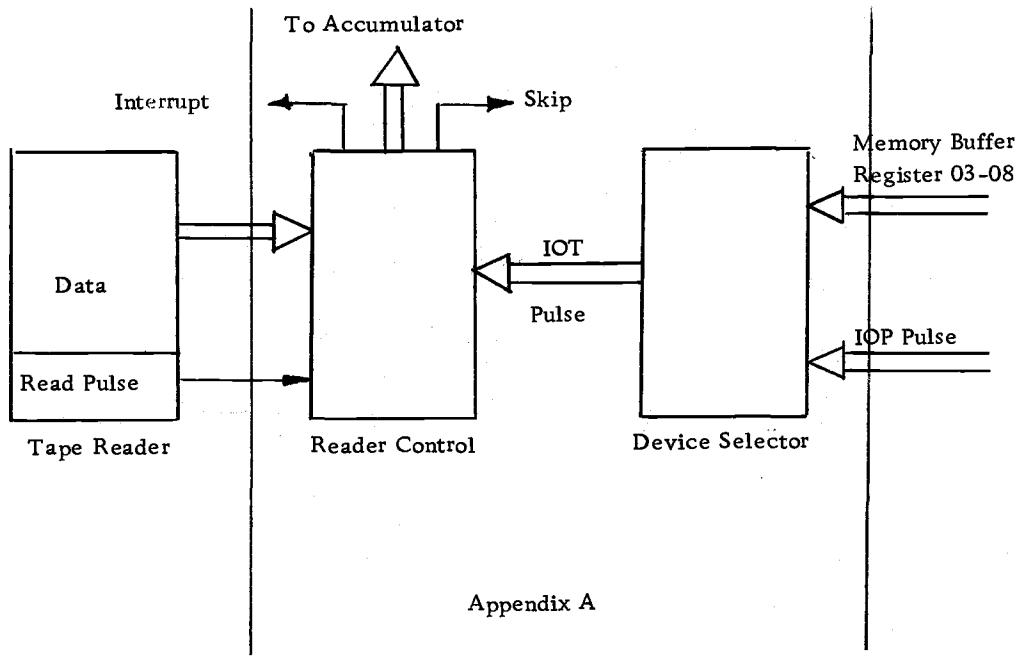

Figure 1. System organization of the high speed tape reader and interface.

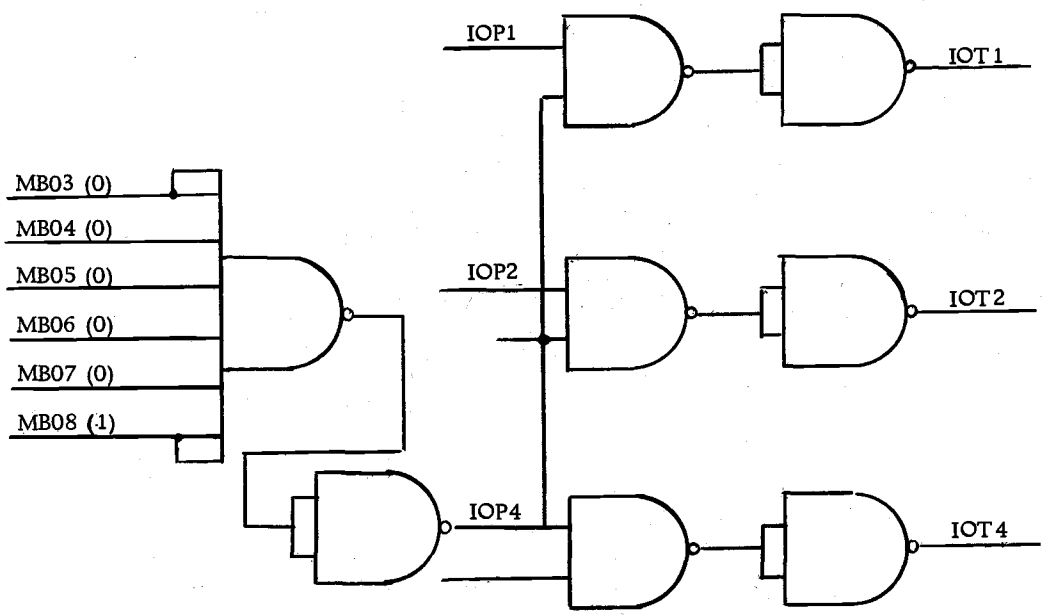

Figure 2. Device selector.

The reader control (see Appendix A) is composed of the following functional sub-units:

a. 8-bit buffer register (BUFFER)

b. output gating

c. buffer status flip-flop (FLAG)

d. reading control flip-flop (READ)

e. reader running control flip-flop (RUN)

f. clock pulse generator (CLOCK)

The BUFFER provides temporary storage for the data from the tape reader; its contents are gated into the Accumulator by the IOT2 and the FLAG is cleared simultaneously. Eight open collector gates were used as the gates, unless the reader is enabled the gates are disabled.

The IOT4 clears the BUFFER and FLAG, it sets the READ and RUN. Whenever the READ is set, it allows the data from tape read-out circuits to be loaded into the BUFFER. Once the BUFFER is loaded, the READ is cleared and the FLAG is set to indicate a busy state.

The IOT1 samples the FLAG and transmits an I/O Skip Pulse to the computer to skip the next instruction.

The RUN controls the tape feed operation and the tape is stopped when it is cleared; it will be cleared only at the initializing state and the coincidence of a "0" state of the READ and the Read Pulse from the tape reader.

Information is strobed into the BUFFER, READ, and FLAG by the CLOCK pulse that is generated by a 200-nsec monostable multivibrator which is triggered by:

$$\overline{\text{(Read Pulse) AND (READ) AND } \overline{\text{(IOT4)}}}$$

The $\overline{\text{IOT4}}$ is used in generating the CLOCK pulse in order to prevent the coincidence of the IOT4 which clears the BUFFER and the CLOCK which strobes data into the BUFFER.

The period of the Read Pulse is 4 msec (250 characters/sec) and the rate of programmed data transfer for PDP-8/L Computer is 134 KHz. Therefore it is obvious that, in normal operation, the RUN will be set before a Read Pulse is generated and the reader will operate at its maximum speed continuously. Figure 3 shows the timing diagram of the interface.

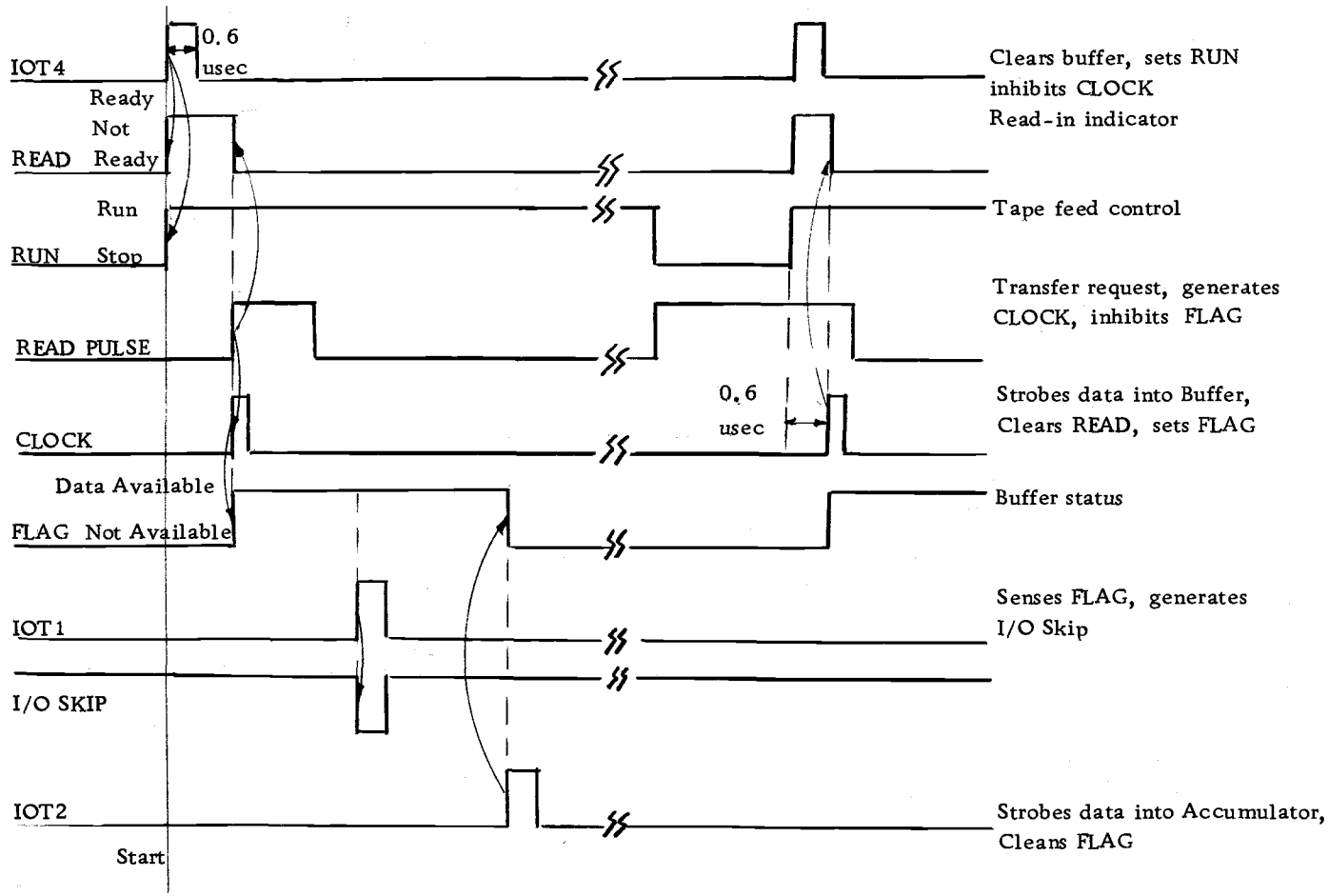

Figure 3. Timing diagram of the interface.

III. HIGH SPEED PAPER TAPE READER

The reader consists of four major components:

1. tape feed mechanism
2. optical projection system
3. photodiode circuits (tape read-out)
4. tape feed control circuit

Tape feed mechanism: The tape feed mechanism is as described in the tape reader instructional manual (5).

The optical projection system: the system is based on the "pinhole projection" principle in that an image from the projection lamp filament is produced by the light from this lamp being passed through the hole in the tape and each image is arranged to cover the area of the photodiode. A single light source is used: a 12 volt, 36 watt, prefocused lamp. The light from this source passes through the holes in the tape masking plate onto a row of photodiodes mounted under the plate.

Photodiode circuits: the circuit diagram and the design procedure of the tape read-out are shown in Appendix B and C, respectively. The eight photodiodes (1N2175) D0-D7 are associated with character elements on the tape and are known as "digit" photodiodes. Photodiode D8 is associated with the sprocket holes on the tape and is known as location photodiode. The output from each digit photodiode

is connected to a single stage switching transistor (2N5134). Each digit photodiode produces, at the output of the transistor, either 0.3 volt or 5 volts depending on whether a "hole" or "no hole" on the tape is being read. The location photodiode is used to produce a Read Pulse which is transmitted to the reader control unit indicating a character is being read. The photodiode circuits were tested by running the tape which had all character elements punched at every other character position and the output waveforms of each digit photodiode and location photodiode circuits were observed in pairs. All output waveforms of the tape read-out were superimposed in Appendix D.

Tape feed control circuit: Two power switching circuits are in the tape feed control as shown in the circuit diagram in Appendix E, and designing procedure is shown in Appendix F. One circuit is connected to the clutch electromagnet and the other to the brake electromagnet. The "0" and "1" output of the reader control flip-flop (RUN) in the tape reader control are connected through an inverter-driver to the clutch (P1) and the brake (P2) power switching circuits respectively. Each time the RUN is cleared, P1 will be cut off and the current in the clutch electromagnet coil will be rapidly reduced to zero, thus releasing the clutch shoes. At the same time, P2 will be driven into saturation and the current in the brake electromagnet coil will be increased from 0 to 60 ma in 0.7 msec, thus applying the brake shoes to the brake drum to halt the tape drive drum and stop the tape. When

the RUN is set, P2 is cut off causing release of the brake shoes on the brake drum; P1 is in saturation causing the application of the clutch shoes to the clutch drum, thereby allowing the tape to move forward.

The tape feed control system can stop the tape within 0.03 inch of the point where braking begins. Therefore, if it is desired to halt the tape at any particular character, braking action can be applied immediately as the character enters the reading position and the tape will be halted while the character is still in the reading position.

IV. SYSTEM OPERATION AND EVALUATION

The tape reader and interface should be turned on before the "START" key of the computer is pressed to start an input operation via the tape reader in order to enable the Initialize Pulse to clear the buffer, the status and control flip-flop in the interface and to stop the reader. The program for testing the tape reader is listed in Appendix G., the program allows the reader to read one character then the computer prints it out via the Teletype and so on until the end of the testing tape. The computer print out is then checked with what has been coded on the tape to see if there is any error. The testing tape should include a leader-trailer code which is simply generated by striking the "HERE IS"key on the Teletype key board with the Teletype control switched to LOCAL.

The designed system operates under program control and is compatible with the software provided by the computer manufacturer for the high speed tape reader including the program interrupt facility. The RIM (Read-in Mode) Loader for the high speed tape reader is listed in Appendix H, and more information about programming the tape reader can be obtained from the PDP-8/L Computer Manuals (1, 2, 3).

Cost Estimation

The cost of the electronic components of the system is very low especially for the interface. The cost of the major units excluding labor cost are:

Tape Reader

Unit	Price $
Tape read-out circuits	46
Tape feed control circuit	10
Total	$ 56

Interface

Logic circuits	9
Connector boards	16
Total	$ 25

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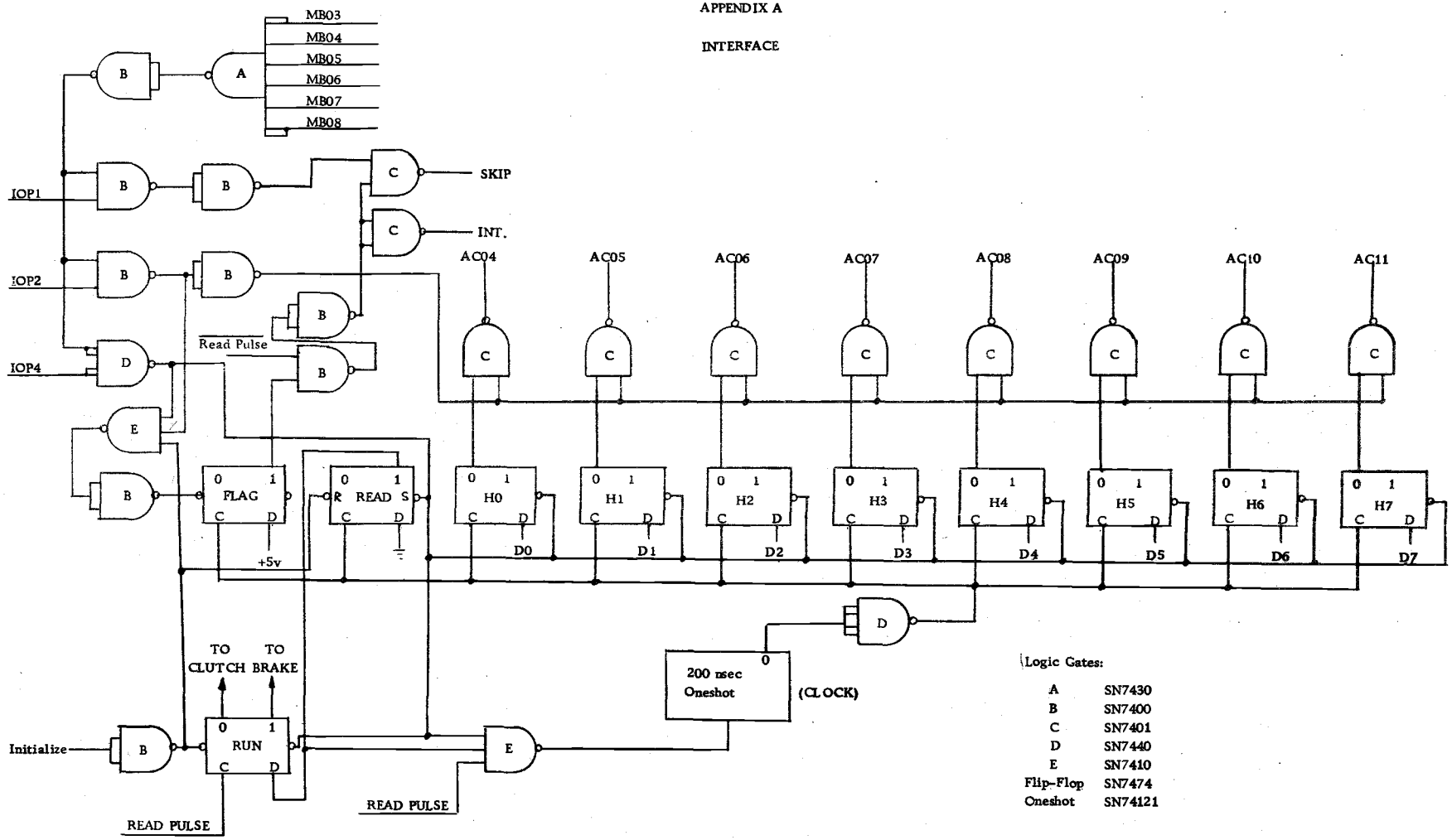
APPENDICES

APPENDIX A

INTERFACE



Logic Gates:

A	SN7430
B	SN7400
C	SN7401
D	SN7440
E	SN7410
Flip-Flop	SN7474
Oneshot	SN74121

Figure 4. Logic diagram of the interface.

APPENDIX B

TAPE READ-OUT CIRCUITS

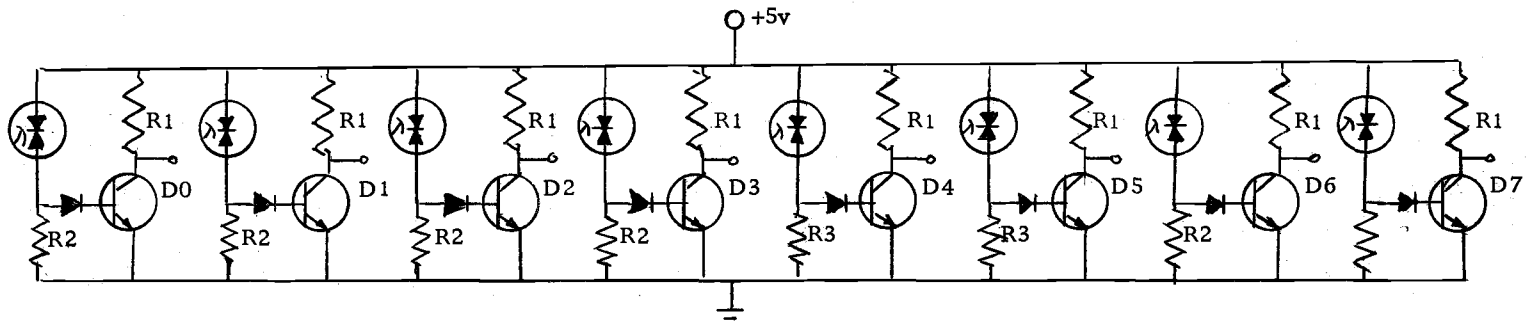


Figure 5. Digit photodiode circuits.

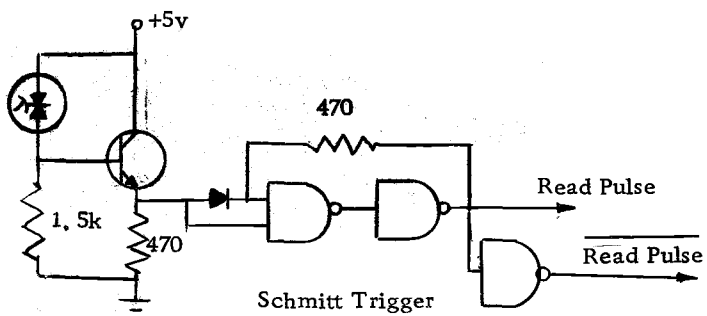


Figure 6. Location photodiode circuit.

Note: Photodiodes are 1N2175
Diodes are 1N3064
Transistors are 2N5134
Resistors: R1 4.7 k ohms
R2 3.3 k ohms
R3 680 ohms
Logic gates are SN7400

APPENDIX C

PHOTODIODE CIRCUITS DESIGN

The current in each photodiode circuit was measured by using a 5-volt dc power supply and a 100-ohm sensing resistor with the green and gray paper tape in the reading position and only the minimum light current and the maximum dark currents in each photodiode were recorded in Table 1. The light and dark currents are defined as the current that flows through the photodiode when a "hole" and "no hole" on the tape is being read respectively.

Table 1. Photodiode current measurement.

Photodiode	Light Current (ma)	Dark Current (ma)
D0	1.49	0.13
D1	0.90	0.11
D2	1.98	0.21
D3	1.88	0.18
D4	3.20	0.28
D5	4.30	0.41
D6	0.95	0.18
D7	1.80	0.14
D8	3.43	0.42

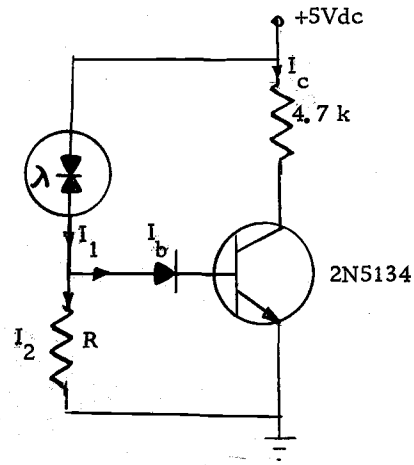


Figure 7. Photodiode circuit calculation.

Because of using a single light source the light intensity and incident angle to each photodiode are different, causing a different amount of current flowing through each circuit. Therefore the photodiode circuits are divided into two groups, high current group D4, D5, D8 and low current group D0, D1, D2, D3, D6 and D7. From Figure 7 the minimum base current, I_b required to drive the transistor into saturation is:

$$I_{b(min)} = \frac{I_c}{h_{fe(min)}}$$

For silicon transistor 2N5134, $h_{fe(min)}$ is 20, $V_{ce(sat)}$ is 0.3 volt.

$$I_{b(min)} = \frac{(5 - 0.3)}{4.7 \times 20} = 0.05 \text{ ma}$$

High current group: Let R = 680 ohms.

The minimum photodiode current required to turn the transistor on is:

$$I_1 = I_{b(min)} + I_2$$

$$= 0.05 + \frac{1.4}{680} \times 10 = 2.08 \text{ ma}$$

From Table 1 the minimum light current in the group is produced by D4:

$$I_{1(light)} = 3.2 \text{ ma}$$

Since

$$I_1 > I_{1(min)},$$

hence the transistor is on and

$$V_{o(light)} = V_{ce(sat)} = 0.3 \text{ volt}$$

The maximum dark current is produced by D5:

$$I_{1(dark)} = 0.41 \text{ ma}$$

Since

$$I_{1(dark)} << I_{1(min)},$$

therefore the transistor is cut off and:

$$V_{o(dark)} = 5 \text{ volts.}$$

Low current group: Let R = 3.3 K ohms

$$I_{l(min)} = 0.05 + \frac{1.4}{3.3} = 0.43 \text{ ma}$$

The minimum light current is produced by D7:

$$I_{l(light)} = 0.95 \text{ ma} \quad .$$

$$I_l > I_{l(min)} ,$$

hence the transistor is on.

The maximum dark current is produced by D2:

$$I_{l(dark)} = 0.21 \text{ ma} .$$

$$I_{l(dark)} << I_{l(min)} ,$$

therefore the transistor is off.

APPENDIX D

PHOTODIODE CIRCUIT OUTPUT WAVEFORMS
(Inverted)

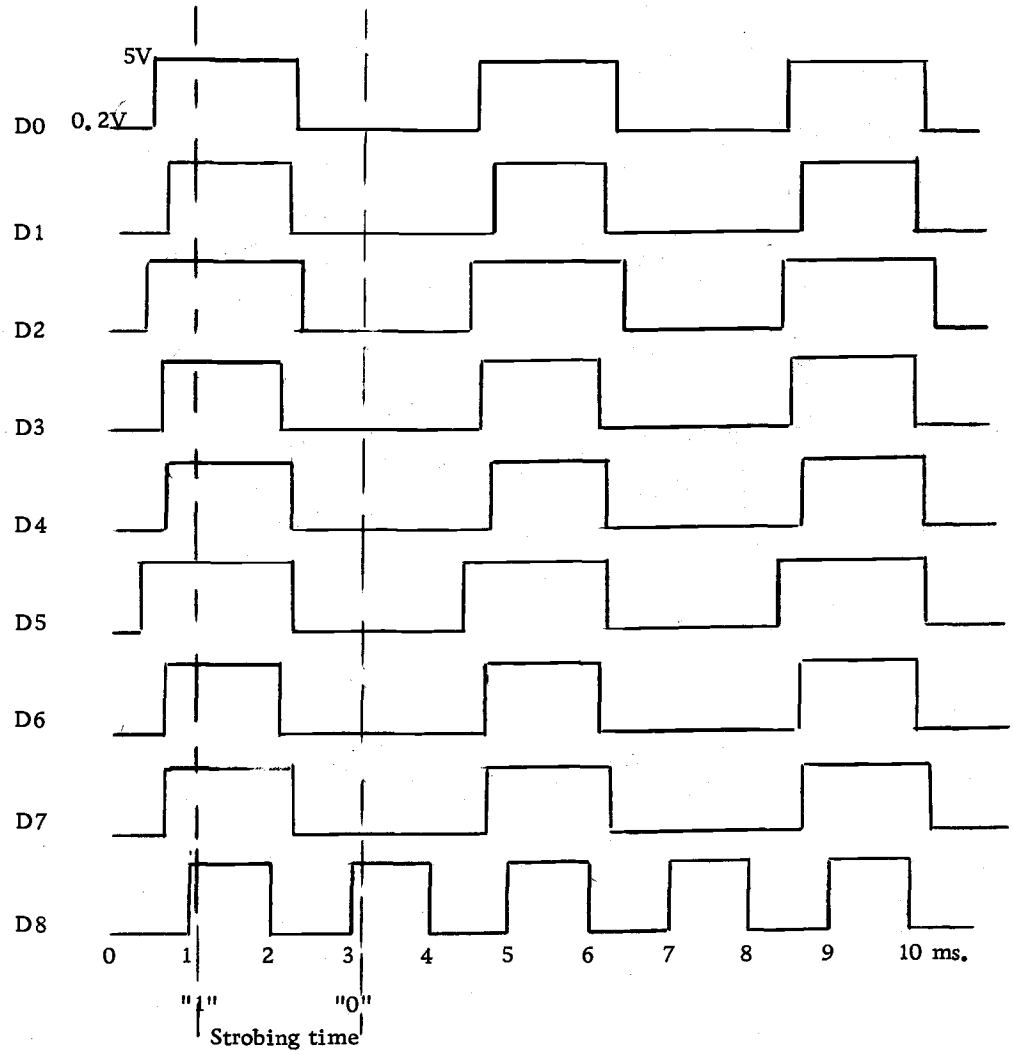


Figure 8. Output waveforms.

APPENDIX E

TAPE FEED CONTROL CIRCUIT

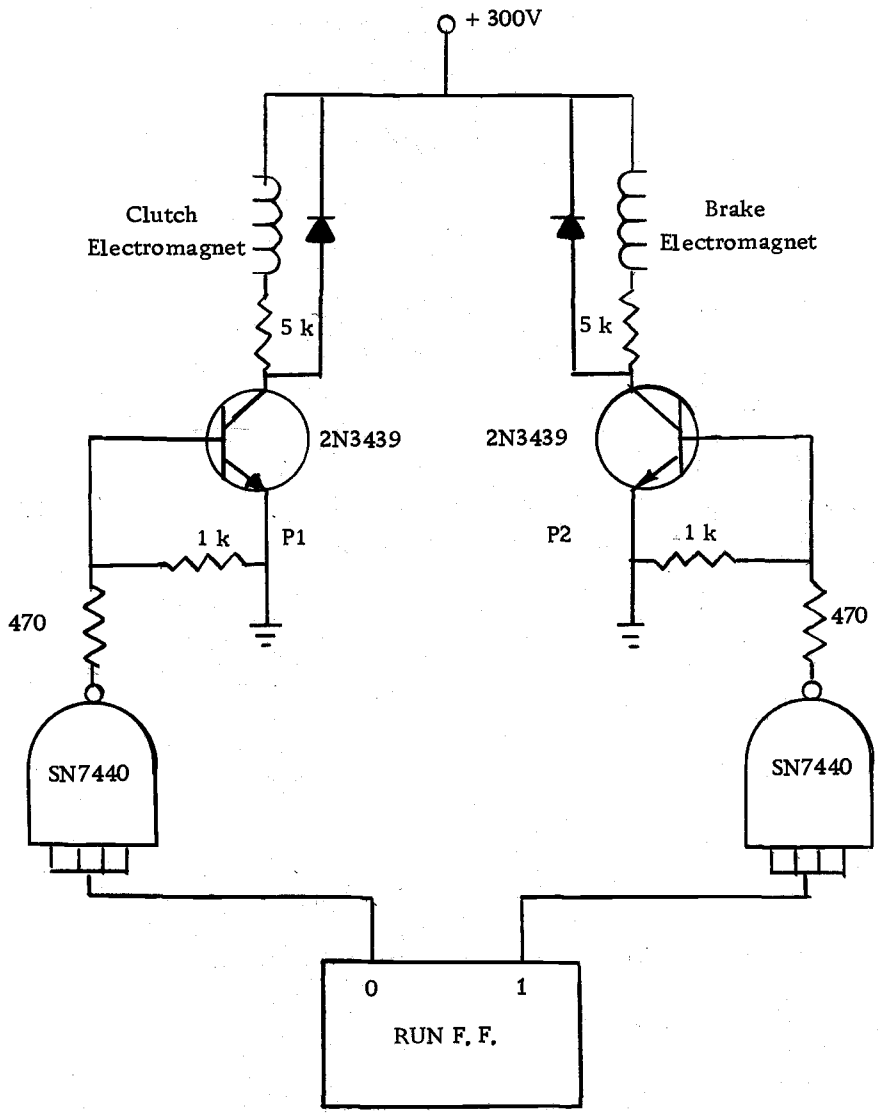


Figure 9. Tape feed control circuit.

APPENDIX F

TAPE FEED CONTROL CIRCUIT DESIGN

Two silicon power transistors 2N3439 are used in the circuit. The transistors ratings are:

Collector-emitter brake down voltage (BV_{CEO}) = 350 volts

Maximum power dissipation = 1 watt

$V_{ce(sat)}$ (measured) = 0.3 volt

$V_{be(cutin)}$ = 0.5 volt

$V_{be(sat)}$ = 0.7 volt

$h_{fe(min)}$ = 40

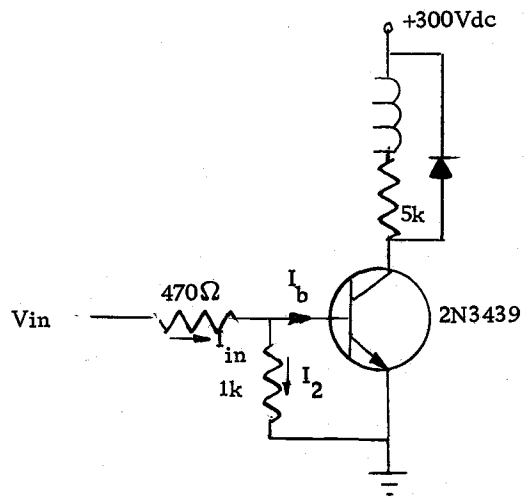


Figure 10. Tape feed control circuit calculation.

The transistor operates as a switch, in order to turn it on the minimum base current is:

$$I_{b(min)} = \frac{I_c}{h_{fe(min)}} = \frac{300 - 0.5}{5 \times 40} \text{ ma}$$

$$= 1.5 \text{ ma}$$

For the "ON" condition, the minimum input voltage at the base circuit is 2.4 volts. Hence

$$I_{in} = \frac{2.4 - 0.7}{470} = 3.62 \text{ ma}$$

$$I_b = I_{in} - I_2$$

$$= 3.62 - 0.7 = 2.92 \text{ ma}$$

Since

$$I_b >> I_{b(min)} ,$$

therefore the transistor must be on.

For the "OFF" condition, the maximum V_{in} is 0.4 volt and:

$$V_{in} < V_{b(cutin)} .$$

Therefore the transistor is off.

APPENDIX G

TAPE READER TESTING PROGRAM

Location	Instruction	Mnemonic Code
0200	6046	TLS
0201	6014	RFC
0202	6011	A, RSF
0203	5202	JUMP A
0204	6016	RRB RFC
0205	7450	SNA
0206	5202	JMP A
0207	6041	B, TSF
0210	5207	JMP B
0211	6046	TLS
0212	7300	CLL CLA
0213	6011	RSF
0214	5213	JMP . -1
0215	6016	RRB RFC
0216	7450	SNA
0217	7402	HLT
0220	5207	JMP B

APPENDIX H

RIM LOADER PROGRAM FOR HIGH SPEED READER

Location	Instruction	Comments
7756	6014	Clear FLAG and BUFFER, Set READ and RUN
7757	6011	Skip if FLAG is 1
7760	5357	Looking for character
7761	6016	Reads contents of BUFFER into AC, clear FLAG, sets READ and RUN
7762	7106	Clear Link, rotate two left
7763	7006	Rotate two left, channel 8 in ACO
7764	7510	Checking for Leader
7765	5374	Found Leader
7766	7006	Channel 7 in link
7767	6011	
7770	5367	
7771	6016	Load AC do not clear
7772	7420	Checking for address
7773	3776	Store content, clear AC
7774	3376	Store address, clear AC
7775	5357	Read next word
7776	0	Temporary storage