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Title: AN INTEGRATED MOS ADDRESSING CIRCUIT

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James C. Looney

This paper is a study of the design of an integrated MOS addressing circuit by using the modified two-phase dynamic shift register. This modified circuit is compared to the conventional two-phase dynamic SR and discussed briefly. The resulting circuit shows several advantages to improve the essential conditions of integrated circuit design and fabrication.

Four stages of this dynamic SR are designed on a single monolithic chip. Each stage consists of seven devices and two intentionally added capacitors. A suggestion to imply that more stages can be used in any sequential digital system is given.

It is shown that the operation is at AC and the operating frequency is ranged between 200 KHz and 1 MHz clock rates.

An Integrated MOS Addressing Circuit

by

Ki Suk Chang

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Associate Professor of Electrical and Electronics Engineering

in charge of major

Redacted for privacy

Head of Department of Electrical and Electronics Engineering

Redacted for privacy

Dean of Graduate School

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Typed by Clover Redfern for Ki Suk Chang

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I. INTRODUCTION

Multiphase metal-oxide semiconductor (MOS) integrated circuits have been developed in digital circuit fields. The development of large scale integration has put added emphasis on the development of new circuit techniques which makes it possible to build circuits of small size, high initial yield, and low power dissipation (18). Several advantages were obtained by using a dynamic shift register (SR) in an addressing circuit.

The circuit approach used in this SR is somewhat similar to that of an earlier type of two-phase dynamic shift register. The modification is that the external clock pulses drive a coupling device in addition to the load resistor, of the following inverter stage, rather than the previous load device (14). By this simple change, the circuit is able to function with the use of all minimum geometry devices. This allows substantial reduction of both the size of the inverter and the load device and the intrinsic capacitance of each node, thus allowing the cell to operate at a higher frequency. In addition, the power dissipation is much lower than in most two-phase systems.

This paper is primarily concerned with the theoretical analysis, design methods, and fabrication process and results of the integrated MOS addressing circuit. A general discussion of the existing MOS techniques is also included for background and prospective.

II. THEORETICAL ANALYSIS

Operating Principles of the MOS Transistor

The MOS transistor shown in Figure 1a, operates as follows: when the source, substrate and gate are grounded and the drain is at some $-V_{DD}$ level, no current will flow between the source and the drain, since the drain to the body P-N junction is reverse-biased.

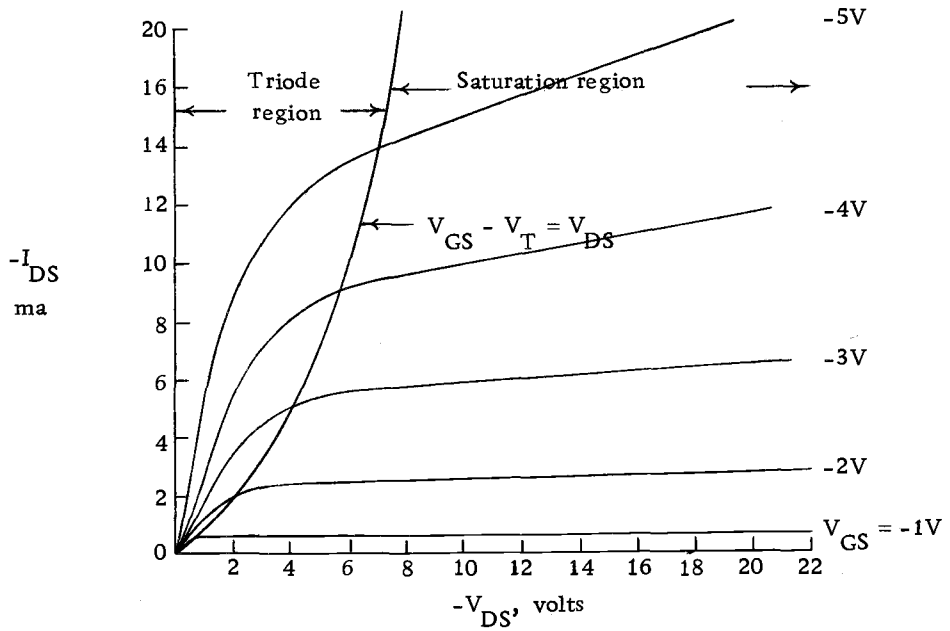
When a negative bias greater than the threshold voltage is applied to the gate, the surface of the N-type silicon inverts. That is, it changes from an N-type to a P-type region, thus forming a channel from the source to the drain. The formation of this channel provides an ohmic path for the majority of carriers to flow between the source and the drain. A typical V-I characteristic curve is also illustrated in Figure 1b, which shows two different regions of operation.

Electrical Characteristics of MOS Devices

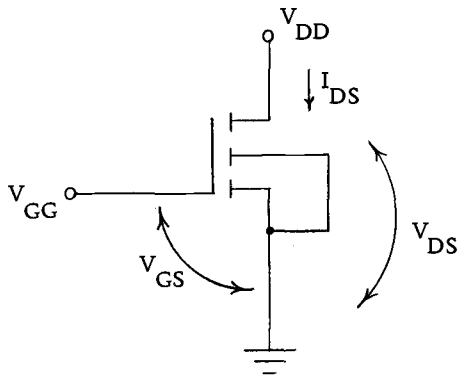
There are several pertinent electrical characteristics of an MOS transistor which make it particularly suitable for both digital and analog applications. These are:

High Input Impedance

The MOS transistor has virtually an infinite impedance (10^{14} ohm) at the gate input due to the characteristics of the "no-



(a)



(b)

Figure 1. Typical V-I characteristics (a) and notation of an MOS device (b).

junction input" terminal, i. e., the gate is completely isolated from the drain and source region by a thin layer of silicon dioxide. The drain and source input terminals exhibit an impedance characteristic in the order of 10^{10} ohm when the transistor is in the "OFF" state. This result is due to the reverse biased P-N junction.

Bilateral Current Flow

Since the MOS transistor is a symmetrical device, i. e., the physical construction of the drain and source are identical and therefore interchangeable, the current can flow in either direction in the channel. Therefore the device can be used as an ideal switch, providing in the "ON" state, current flow in either direction or, in the "OFF" state, virtually an infinite resistance.

Coupling Device

Because of the bilateral nature of an MOS device, it can be used as an ideal switch or coupling device. The use of a coupling device is one of the essential elements which make possible the implementation of an extremely simplified static or dynamic register cell.

Temporary Storage

The gate-to-source capacitance of an MOS device can be used as a temporary memory-storage element. The storage time is

dependent directly on the capacitance and the leakage characteristics of the gate oxide, and the drain or source to the body junction of its preceding coupling stage.

MOS Resistor

The most dramatic characteristic of an MOS device is its ability to act as an active load resistor. Although the resistance characteristic is nonlinear, i. e., the resistance varies as a function of the gate to source bias, large resistance values in the order of 100 Kohm to 400 Kohm can be fabricated within an area of less than 1 mil^2. Coupled with its ability to exhibit large resistance values in an extremely small area, the MOS load device can be turned "ON" and "OFF" by applying a negative clock pulse to its gate. Power dissipation now becomes a function of the duty cycle of the clock. For very low duty cycles, extremely low power dissipation is obtainable even in the most complex circuits.

MOS Current Equation

The basic current equations for the non-saturated and saturated regions of operation are (4):

Non-saturated region

$$|V_{GS}-V_T| \geq |V_{DS}|$$

$$I_{DS} = \frac{\bar{\mu}_p \epsilon_{ox}}{2t_{ox}} [2(V_{GS}-V_T)V_{DS}-V_{DS}^2] \quad (1)$$

Saturated region

$$|V_{GS}-V_T| \leq |V_{DS}|$$

$$I_{DS} = \frac{\bar{\mu}_p \epsilon_{ox}}{2t_{ox}} (V_{GS}-V_T)^2 \quad (2)$$

where

V_{GS} is the voltage from gate to source

V_T is the threshold voltage

V_{DS} is the voltage from drain to source

I_{DS} is the current from drain to source

$\bar{\mu}_p$ is the average surface mobility of holes and units are in $cm^2/V\text{-}sec$

ϵ_{ox} is the oxide dielectric constant; assumed as 1/3pf/cm

t_{ox} is the oxide thickness (1200 Å)

W is the channel width (perpendicular to current flow)

L is the effective channel length in the direction of current flow

Defining two parameters K and K' such that

$$K = K' \frac{W}{L}$$

$$K' = \frac{\bar{\mu}_p \epsilon_{ox}}{2t_{ox}}$$

The above Eqs. (1) and (2) become

$$I_{DS} = K[2(V_{GS}-V_T)V_{DS}-V_{DS}^2] \tag{3}$$

for a non-saturated region, and

$$I_{DS} = K[V_{GS}-V_T]^2 \tag{4}$$

for a saturated region.

The value of K in the above equation is determined by certain process constants which may be lumped together and called K', and the ratio of the width W and the length L of the device channel. Since the resistance of a device is inversely proportional to its K value, a large ratio of

$$\frac{K_I}{K_L} = (W_I/L_I)/(W_L/L_L) \tag{5}$$

(where K_I and K_L are the process constants of the inverter and the load, respectively) is equivalent to a large load resistance. Most of the voltage is then dropped across the load, and the output zero level is low. In general, the lower the output zero level requires for given "1" input, the larger the ratio of K_I/K_L must be.

The "gain" parameter of the MOSFET is the forward transfer-conductance ratio. This expresses the output-current variation for an input voltage variation. Therefore, transconductance is defined as the ratio of a small variation in the drain current to the variation in gate voltage which produces the current, and is symbolized as g_m.

Mathematically, this can be written as (4, p. 53)

$$g_m = \frac{\partial I_D}{\partial V_G} \Big|_{V_D} \tag{6}$$

which is determined in the active operating region, the saturated region.

Differentiating the Eq. (6) yields

$$\frac{\partial (I_D)}{\partial V_G} = \frac{\partial K(V_{GS}-V_T)^2}{\partial V_{GS}} = 2K(V_{GS}-V_T) \tag{7}$$

where

$$I_D = K(V_{GS}-V_T)^2$$

This expression tells that g_m is directly proportional to the ratio of W/L, and also to the voltage $(V_{GS}-V_T)$. Thus g_m can be varied in one of two ways. First, the gate bias V_G may be varied, or second, the geometry of the device may be varied. Another

parameter which is of interest to the switching device application is the resistance R_{on} of the device when it is turned on and operated in the non-saturated regions.

$$R_{on} = \frac{\partial V_D}{\partial I_D}\Big|_{V_{GS}} = \frac{1}{K[2(V_{GS}-V_T)-2V_{DS}]} \tag{8}$$

In the non-saturated region, the characteristic curves of MOS are nearly linear, thus this expression can be approximately rewritten when V_{DS} goes to 0.

$$R_{on} \approx \frac{1}{2K(V_{GS}-V_T)} = \frac{1}{g_m} \tag{9}$$

And for load device, R_L is expressed as (4, p. 90)

$$R_L = \frac{2}{g_{mL}} \tag{10}$$

Threshold Voltage

The threshold voltage expression is as follows (4):

$$V_T = \frac{Q_{SS}+Q_D}{C} \tag{11}$$

where

Q_{SS} = effective surface-state charge density per unit area.

Q_D = bulk charge per unit area associated with the channel

depletion region.

C = capacitance of the gate to channel per unit area

ϵ_{ox}/t_{ox}.

Physically, V_T is the gate voltage required to neutralize, in effect, the immobile charge above and below the channel region. The charge above the channel is Q_{SS}, while the charge below the channel consists of that within the depletion region located in the bulk.

Depletion-region charge Q_D is derived from an application of the simple P-N junction theory, where the number of charge carriers in the channel is much greater than that of the substrate.

Q_D = depletion-region thickness (X_D) substrate charge density

$$= \sqrt{\frac{2\epsilon_S \phi_S}{qN}}\, qN$$

where

ϕ_F = Fermi function; the amount of the fermi level which is displaced from the intrinsic level, and the unit is expressed in volts.

ϕ_S = surface potential

$\phi_S = 2\phi_F \quad Q_D = \sqrt{q\epsilon_S N}\,\sqrt{2\phi_F}$

where

$N = N_D$ for an N-type substrate device (P-channel)

$N = N_A$ for a P-type substrate device (N-channel)

The voltage on the gate necessary to support this charge from Eq. (11) is

$$V_{I_T} = + \frac{Q_D}{C} = -K_1 \tag{12}$$

where $K_1 = \pm (t_{ox}/\epsilon_{ox})\sqrt{q\epsilon_S N}$ (+ for P-channel, - for N-channel)

Equation (12) might be considered an "intrinsic" threshold voltage for a "perfect" device with zero surface-state charge density ($Q_{SS} = 0$). This will be of the enhancement-mode type with a low threshold voltage equal to V_{IT}.

The surface-state charge Q_{SS} is assumed to be constant and to lie close to the silicon-oxide interface. The bulk charge V_{SS} is

$$V_{SS} = - \frac{Q_{SS}}{C} = - \frac{t_{ox}}{\epsilon_{ox}} Q_{SS} \tag{13}$$

Q_{SS} is generally an ionized donor and thus acts as a positive charge center, giving V_{SS} a negative sign in Eq. (13).

The total threshold voltage is the algebraic sum of the intrinsic threshold voltage and that due to surface states. From Eqs. (12) and (13)

$$V_T = V_T + V_{SS} \tag{14}$$

$$V_T = - K_1 \sqrt{\phi_S} + V_{SS} \tag{15}$$

where

$$K_1 = \pm (t_{ox}/\epsilon_{ox})\sqrt{2q\epsilon_S N}$$

$$\phi_S = 2\phi_F$$

For typical values where $N_D = 10^{15}$, $t_{ox} = 1500$ Å, $\epsilon_{ox} = 1/3$ pf/cm Fermi potential.

$$V_{IT} = -0.6 \text{ V},$$

and

$$V_{SS} = -2.88 \text{ V}.$$

Therefore, the resultant total threshold voltages for a P-channel device and for an N-channel device are -3.48 V and -2.28 V, respectively.

In this paper, the threshold voltage will be assumed to be -5 V.

Back Gate Bias

When a bias is applied to the substrate, modulation of the channel conductance results. Thus the substrate can act as a second gate, and in fact, is sometimes referred to as the back gate. Because a P-N junction is formed with the source and drain diffusions to the substrate, some of its characteristics tend to be more like the gate of a junction FET than the gate of an insulated device.

The theory of operation of the back-gate bias can be explained by an extension of the insulating depletion region layer into the

substrate. As the reverse bias on the substrate increases, the depletion region extends further into the substrate as mobile electrons are depleted and imobile holes are decreased, just as in the P-N junction theory. For a fixed gate voltage, there will now be less mobile channel charge, and therefore a decrease in conduction.

The expression for the threshold voltage as a function of the back-gate bias can be written directly from Eq. (15). It is assumed that all the applied voltage will appear across the depletion region and none across the bulk semiconductor. A polarity of back gate bias V_{BG} is assumed such that when the substrate is reverse-biased with respect to the source, V_{BG} and ϕ_S have the same polarity. These will give the following results (4):

$$V_T = -K_1 \sqrt{\pm(\phi_S - V_{BG})} + V_{SS} \tag{16}$$

where

$$\phi_S = 2\phi_F$$

It is often convenient to express V_T in terms of a fixed value (where $V_{BG} = 0$) plus a variable term ΔV_T, which is a function of V_{BG}. The following analysis derives ΔV_T by starting with Eq. (15)

$$V_T(V_{BG}) = V_{SS} - K_1 \sqrt{2\phi_F + V_{BG}}$$

$K_1 \sqrt{2\phi_F}$ is added and subtracted to the right-hand side of the equation:

$$V_T(V_{BG}) = V_{SS} - K_1\sqrt{2\phi_F} + K_1\sqrt{2\phi_F} - K_1\sqrt{2\phi_F+V_{BG}}$$

$$V_T(V_{BG}) = V_T + \Delta V_T \tag{17}$$

so that

$$\Delta V_T = - K_1(\sqrt{2\phi_F+V_{BG}} - \sqrt{2\phi_F}) \tag{18}$$

This result is plotted in Figure 2.

Capacitance

Two kinds of capacitance will be associated with the MOS device. One is the oxide capacitance, and the other is the capacitance of the silicon P-N junction which is due to the depletion region.

The oxide capacitance is due to evaporating a metal electrode over the oxide and using this electrode and the semiconductor as the parallel plates of a capacitor whose dielectric is the oxide. It may be determined solely from geometry, and is given by (4)

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \cdot A \tag{19}$$

where ϵ_{ox} is the dielectric constant of silicon oxide, and t_{ox} is the thickness of the silicon oxide.

The overlap thick oxide capacitance due to the gate overlapping into the drain and source areas will be considered by the above expression.

$$\Delta V_T = -K_1 (\sqrt{2\phi} + V_{BG} - \sqrt{2\phi})$$

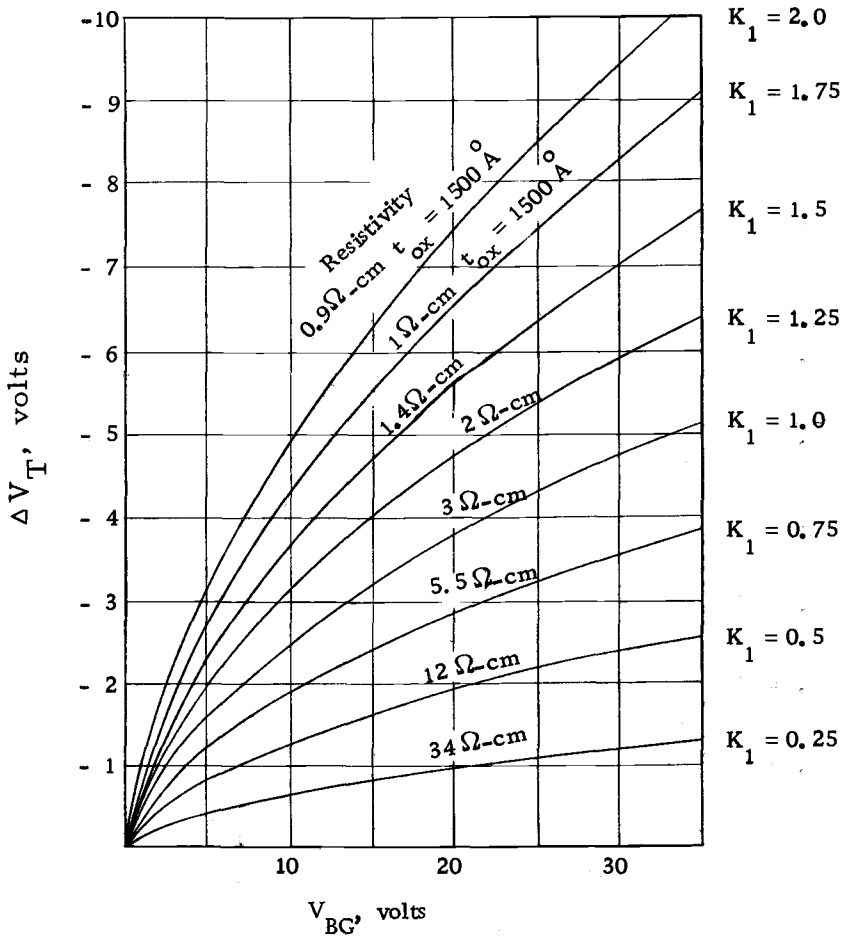


Figure 2. Threshold voltage variation vs. back-gate bias (4).

The P-N junction capacitance is related to the back-bias diffused junctions of the drain and source. With increasing voltage the depletion region widens, resulting in a decrease in the depletion capacitance. Its reverse bias voltage vs. capacitance relation is given by the formula (1).

$$C = \frac{0.08}{\sqrt[3]{0.6+V_R}} \text{ pf/mil}^2 \tag{20}$$

where V_R is the amount of the reverse bias voltage. The above expression is plotted in Figure 3.

MOS Inverter

The MOS inverter circuit is a basic building block of digital subsystem. A common inverter circuit with an MOS as a load resistor configuration is shown in Figures 4 and 5 (10).

The basic DC inverter consists of a switch tied to the ground and a load-resistor tied to the power supply. The negative voltage above the threshold voltage V_T to the P-channel device applied to the gate turns the device on and pulls the output voltage V_{DD} near to the ground. In the 2ϕ technique, the resistor is clocked on for a convenient period of time. The clock can also be used to sample and hold the inverter information onto a storage capacitor.

The theoretical expression for the voltage characteristics of an

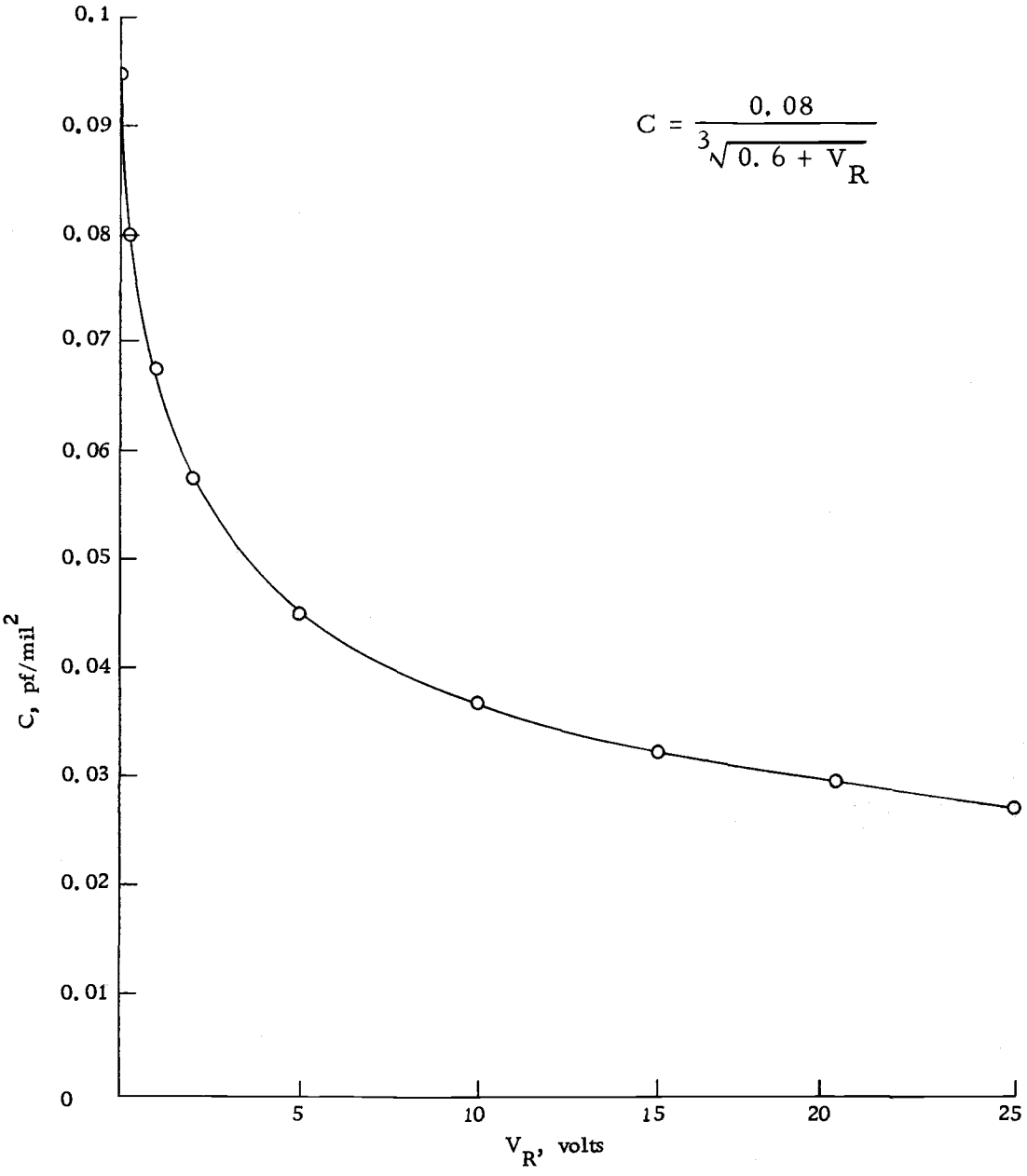


Figure 3. P-diffusion capacitance vs. reverse bias voltage (1).

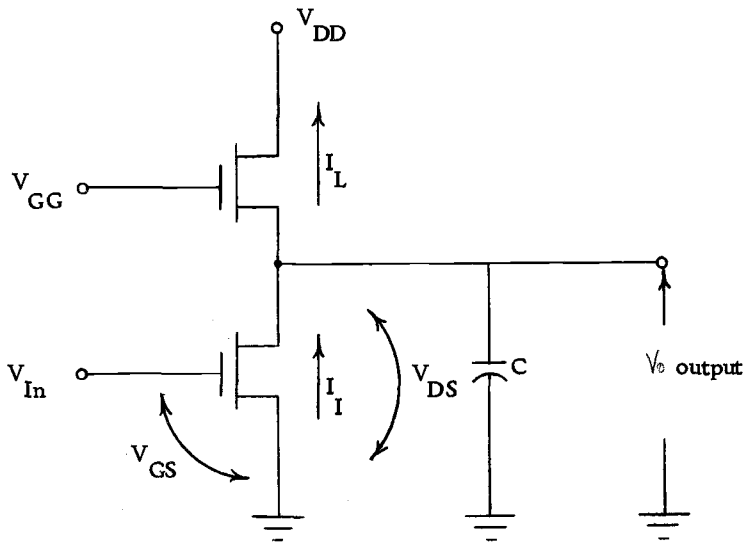


Figure 4. Turn-on case of an MOS inverter.

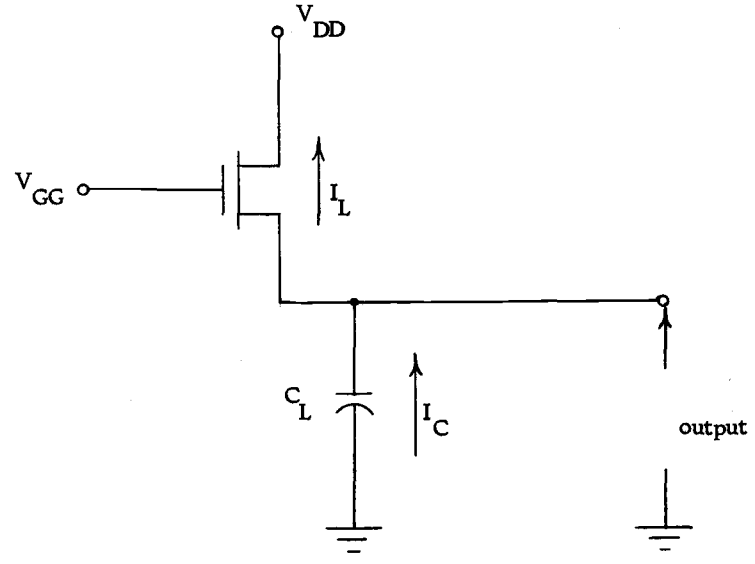


Figure 5. Turn-off case of an MOS inverter.

MOS inverter device and its associated load will be developed.

The analysis will be progressed for two different types of loads: (1) an MOS device biased in the saturated mode; and (2) an MOS device biased in the non-saturated mode.

From Figure 4 it is obvious that

$$V_{GS} = V_{IN}$$

$$V_{DS} = V_o$$

The current in the inverter can be found by substituting the above equations into equations (3) and (4)

$$I_I = K_I(V_{IN}-V_T)^2 \tag{21}$$

for the condition of the saturated region, and

$$I_I = K_I[2(V_{IN}-V_T)V_o - V_o^2] \tag{22}$$

for the condition of the non-saturated region.

Power Consumption of the MOS Inverter

The DC power consumption of the MOS inverter in each stage is associated with the drain current flow I_D. Therefore, the expression in the saturation region is

$$p = V_{DD} \cdot I_D$$

$$= V_{DD}K(V_{GS}-V_T) \quad \text{watts.} \tag{23}$$

In the non-saturated region, the DC power expression is

$$p = V_{DD}K(2(V_{GS}-V_T)V_{DS}-V_{DS}^2) \tag{24}$$

When the complementary MOS devices are used, power is dissipated only during the switching interval.

Transient Response and Switching Time Consideration

The following discussion for an MOS load device whose substrate is returned to the source terminal can be used to determine the "worst case" conditions of a grounded substrate in an actual IC case. They are as follows:

Load Device, Substrate Common to Source, Saturation Region

It is generally desirable to use an MOS as a load resistor in ICs. Figures 6 and 7 show how a device can be biased as a load, and illustrate the load's non-linear characteristics superimposed upon the output curves of the driver device (4, p. 78-83).

Figure 6 is arranged to discuss the switching time of these load devices. The driver device is turned on, allowing C_L to discharge completely. T1 is then switched off, thus effectively removing it

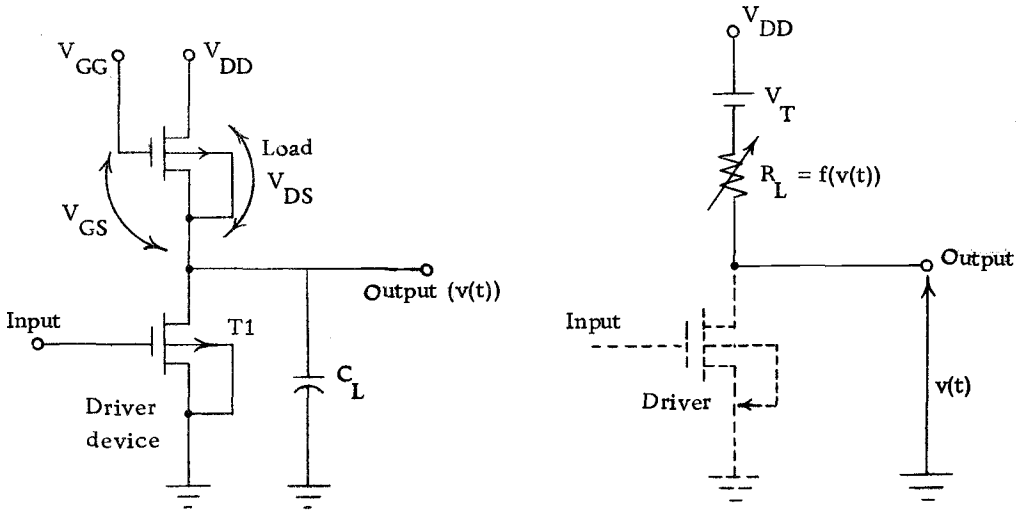


Figure 6. Inverter circuit using an MOS load and its equivalent circuit (4).

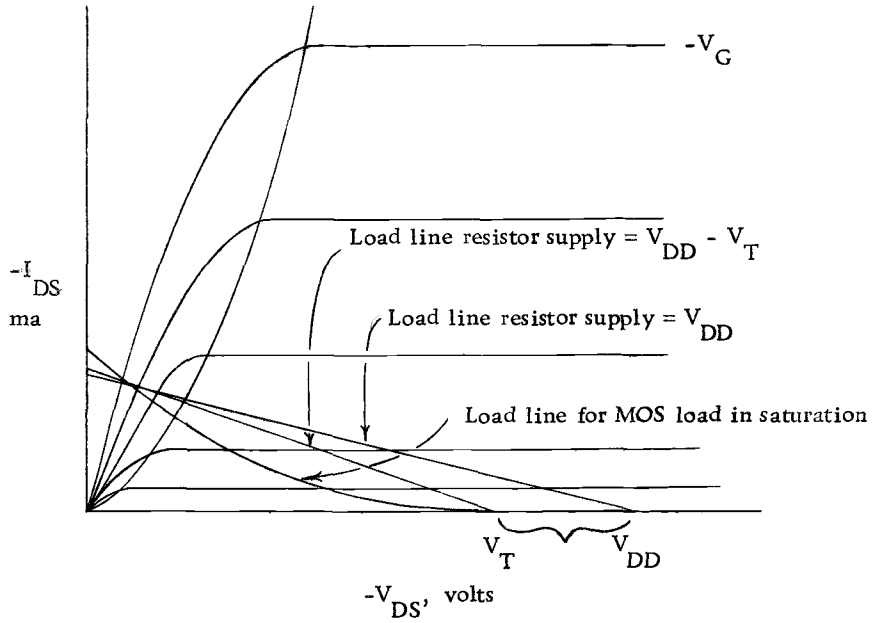


Figure 7. MOS load line and linear-resistor characteristic superimposed upon the driver characteristic (4).

from the circuit and allowing the MOS load to charge C_L. T1 is assumed to have zero storage time. The current charging i_{C_L} is not a constant, and is a function of the voltage across C_L. Because the load gate is returned to the drain and the device is assumed to be an enhancement-mode device, the operation is in the saturation region, and the biasing must satisfy the condition that

$$|V_{GG}-V_T| \leq |V_{DD}|$$

From Figure 6,

$$V_{GS} = V_{GG} - v(t) \tag{25}$$

$$V_{DS} = V_{DD} - v(t) \tag{26}$$

The theoretical expression for the current in the saturated device is

$$I_L = K_L(V_{GS}-V_T)^2 \tag{27}$$

and the capacitor current i_{C_L} is

$$i_{C_L} = C_L \frac{dv(t)}{dt} \tag{28}$$

The drain and capacitor C_L current are equated and yield

$$C_L \frac{dv(t)}{dt} = K_L[V_{GG}-v(t)-V_T]^2 \tag{29}$$

where $v(t)$ is the capacitor output voltage.

Solving the equation for $v(t)$ gives the time response for the MOS load and capacitor combination:

$$\frac{v(t)}{V_1} = \frac{t/\tau}{2+ t/\tau} \tag{30}$$

where

$$V_1 = V_{GG} - V_T$$

$$\tau = C/g_m$$

$$g = -2K(V_{GG}-V_T)$$

Equation (30) is plotted in Figure 8.

This result is not an exponential the same as an R-C network, but it is still comparable.

This is an expected characteristic for the MOS, since as the output voltage across C_L increases toward $V_{GG} - V_T$, the MOS delivers less and less charging current to C_L. When the $v(t)$ increases, the voltage across R decreases, thus naturally decreasing the current across C_L. This is analogous to a capacitor being charged by a nonlinear resistor whose resistance value increases as a function of capacitor voltage (see Figure 6). The speed of the circuit in Figure 8 is calculated to be approximately $18\ \tau$.

Load Device, Substrate to Source, Triode Region

The higher the gate voltage, the more linear the load V-I

characteristics become, as shown in Figure 7. In the limit as V_{GG} approaches to infinity, the switching characteristic of a fixed resistor will be 2.2T, whose speed is that of the R-C network.

This result will be analyzed by equating the capacitor and device current, which is in the non-saturated region. The biasing parameter must satisfy the condition that

$$|V_{GG}-V_T| \geq |V_{DD}|$$

The theoretical expression for the current in this region is

$$I_L = -K_L[2(V_{GS}-V_T)V_{DS}-V_{DS}^2] \tag{31}$$

and the capacitor current i_{C_L} is

$$i_{C_L} = C_L \frac{dv(t)}{dt} \tag{32}$$

Substituting Eqs. (25) and (26) into Eq. (31) yields

$$I_L = -K_L[2(V_{GG}-v(t)-V_T)(V_{DD}-v(t))-(V_{DD}-v(t))^2] \tag{33}$$

Equating Eqs. (32) and (33), then it becomes

$$C_L \frac{dv(t)}{dt} = -K_L[2(V_{GG}-v(t)-V_T)(V_{DD}-v(t))-(V_{DD}-v(t))^2] \tag{34}$$

Rearranging the terms yields

$$-\frac{C_L}{2K_L(V_{GG}-V_T)}\frac{dv(t)}{dt} = V_{DD} - v(t) + \frac{v(t)^2 - V_{DD}^2}{2(V_{GG}-V_T)} \tag{35}$$

By dividing both sides by V_{DD}, using $g_m = -2K(V_{GG}-V_T)$, and introducing parameter $m = V_{DD}/V_{GG} - V_T$, which is the biasing parameter, the following normalized differential equation is obtained:

$$\frac{C}{g_m}\frac{d[v(t)/V_{DD}]}{V_{DD}} = 1 - \frac{v(t)}{V_{DD}} + \frac{1}{2}\left[\left(\frac{v(t)}{V_{DD}}\right)^2 - 1\right]m \tag{36}$$

Letting $C/g_m = \tau$ and separating the variables yield

$$\int_0^t \frac{dt}{\tau} = \int_0^{v(t)/V_{DD}} \frac{d[v(t)/V_{DD}]}{\frac{1}{2}m[v(t)/V_{DD}]^2 - [v(t)/V_{DD}] + (1-\frac{1}{2}m)} \tag{37}$$

The integration of Eq. (37) is the relation between the normalized output voltage and the normalized time. The final result becomes

$$\frac{v(t)}{V_{DD}} = \frac{(2-m)\left[1-e^{-(\frac{t}{\tau})(1-m)}\right]}{2-m\left[1+e^{-(\frac{t}{\tau})(1-m)}\right]} \tag{38}$$

The above equation is plotted in Figure 9, where the normalized voltage parameter m results in a family of curves. The parameter m varies from 0 to 1 for the case which V_{GG} approaches infinity and $V_{DD} \geq V_{GG} - V_T$, respectively. When $m = 1$,

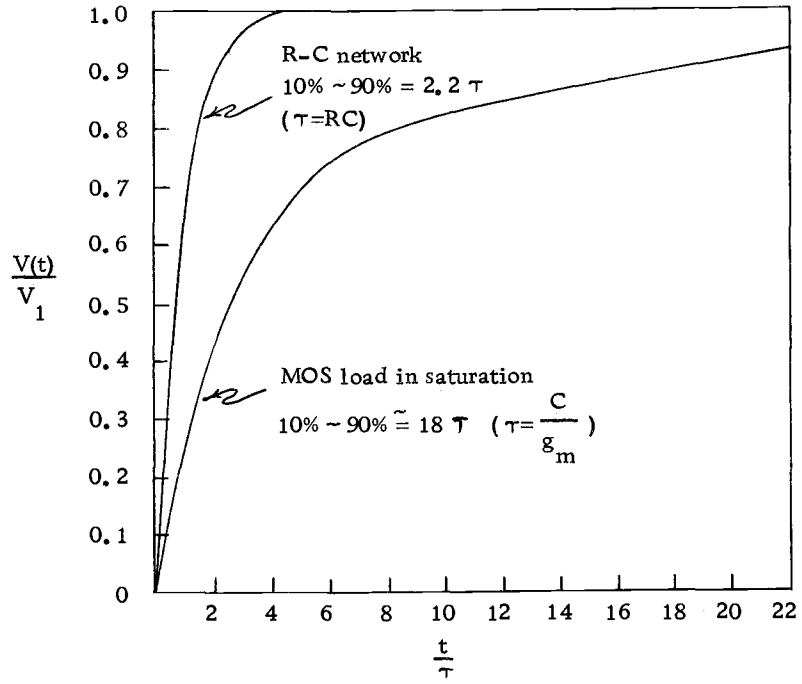


Figure 8. Switching time response of an MOS in the saturation region, with an R-C network for comparison (4).

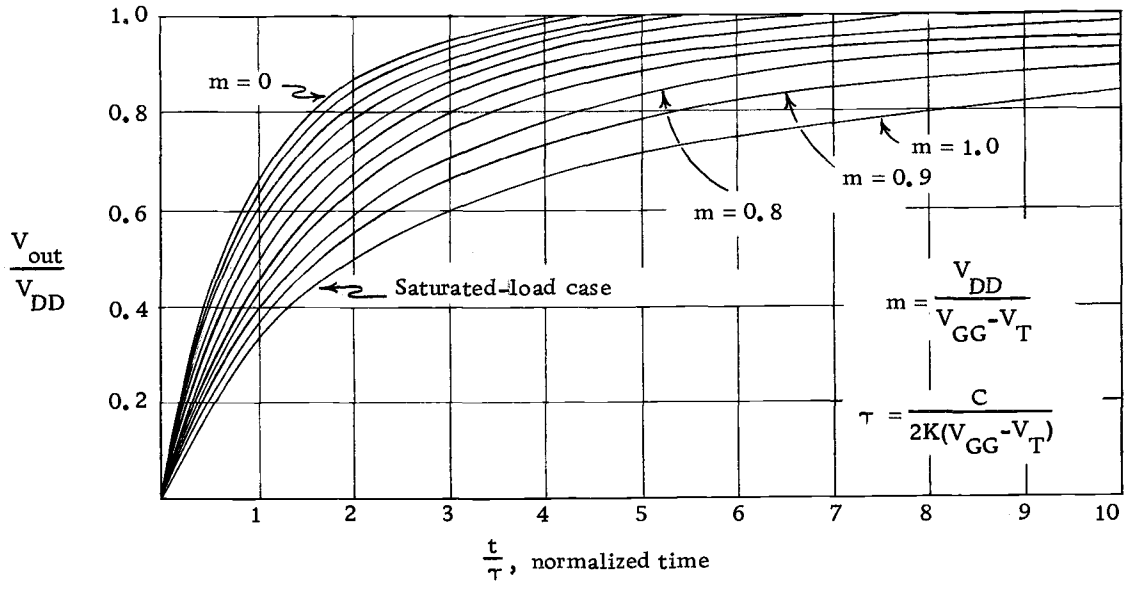


Figure 9. Switching time response of an MOS load in the triode region (m = 0 to m = 1) (4).

Eq. (38) can be reduced by the use of L'Hospital's rule to Eq. (30).

$$\lim_{m \to 1} \frac{(2-m)\left[1-e^{-\left(\frac{t}{\tau}\right)(1-m)}\right]}{2-m\left[1+e^{-\left(\frac{t}{\tau}\right)(1-m)}\right]}$$

$$= \lim_{m \to 1} \frac{(-1)(1-e^{-\left(\frac{t}{\tau}\right)(1-m)}) + (2-m)(-e^{-\left(\frac{t}{\tau}\right)(1-m)})\left(\frac{t}{\tau}\right)}{1-e^{-\left(\frac{t}{\tau}\right)(1-m)} - me^{-\left(\frac{t}{\tau}\right)(1-m)}\left(-\frac{t}{\tau}\right)(-1)}$$

$$= \frac{-\frac{t}{\tau}}{-2-\frac{t}{\tau}} = \frac{\frac{t}{\tau}}{2+\frac{t}{\tau}} \qquad (39)$$

Above results come out the same as those of Eq. (30), which say that the device is now operating in the saturation region with a 18 τ switching time.

Load Device, Substrate Common to Ground

This is the actual transient case for the IC case. Eq. (38) shows the switching characteristic to be dependent upon τ and m both of which are functions of V_T. Also, the variation of V_T is due to the output voltage (back gate bias) for the ground substrated configuration. Therefore, in this case, m and τ must be rearranged to represent the threshold voltage variation.

$$m = \frac{V_{DD}}{V_{GG}-(V_T+\Delta V_T)}$$

$$\tau = \frac{C_L}{-2K[V_{GG}-(V_T+\Delta V_T)]} \qquad (40)$$

and

$$g_m = 2K[V_{GG}-(V_T+\Delta V_T)]$$

Notice in Eq. (40) that as ΔV_T increases, the terms m and τ also increase. By using these properties, one can approach the "worst-case" design.

This result is particularly evident at the lower gate voltage, where ΔV_T causes a larger percentage of change in m and τ than at the higher voltages.

Comparison of Two Types of 2φ Dynamic Shift Register

There are two types of dynamic shift register circuits. These are: the ratio type, which has a large geometry ratio between load and inverter devices and the ratioless type, which has the same geometry size on both load and inverter devices. The following explanation tells the differences.

Ratio Type Circuit Operation

The earliest ratio type of the two-phase delay stage is shown in Figure 10 (4). This circuit functions as follows: with a logic "1" fed

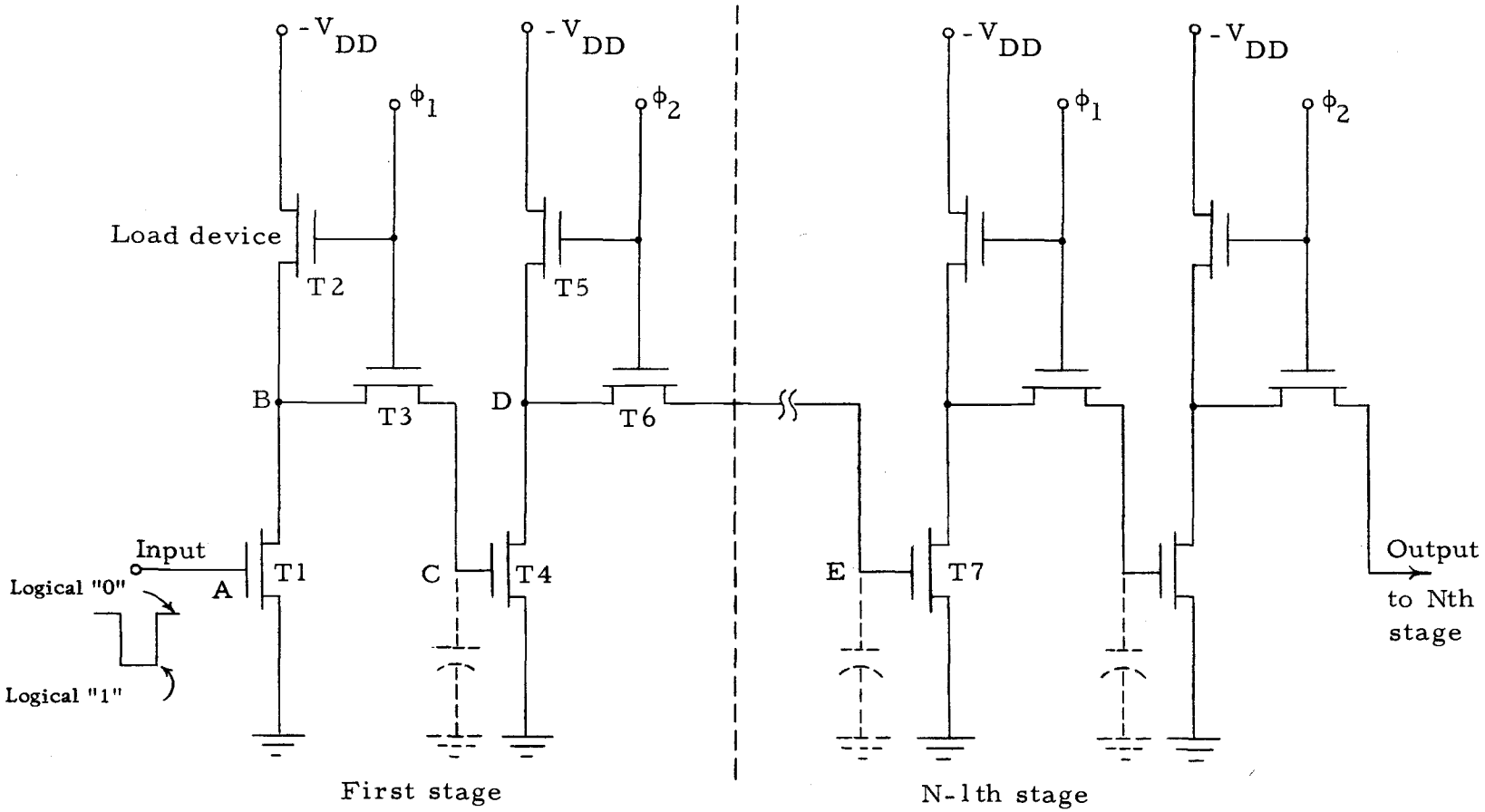


Figure 10. Two-phase dynamic shift register schematic (ratio type).

into the input at node A, transistor T1 turns "ON" allowing node B to discharge to ground. During clock ϕ_1, T2 and T3 turn "ON", allowing the charge that was previously stored on the node C to discharge through T1 and T3. It must be pointed out that, in order for node B to obtain an adequate logic "0" level, a resistance ratio of at least 10 to 1 is required between transistors T1 and T2. This implies that the physical geometry of T1 must be much larger than that of T2, which in turn greatly increases the physical size of these two elements. Furthermore, when ϕ_2 goes negative, T5 and T6 turn "ON"; however, since the gate of T4 is at a logic "0" level, nodes D and E are allowed to charge to a logic "1" level. If, however, node C was at a logic "1" level and clock ϕ_2 goes negative, T4, T5 and T6 turn "ON", allowing the charge stored on nodes D and E to discharge to a logic "0" level. To insure an adequate "0" level at node D and E, the resistance ratio of T4 and T5 must be at least 10 to 1 or greater for the circuit to operate correctly. The need for a resistance ratio between load and inverter devices of T2, T3 and T5, T6 greatly increases the cell area and in turn effectively reduces the maximum operating speed of the devices.

The Ratioless Type Circuit Operation

The ratioless type circuit which is shown in Figure 11 is somewhat similar to that of Figure 10 (14).

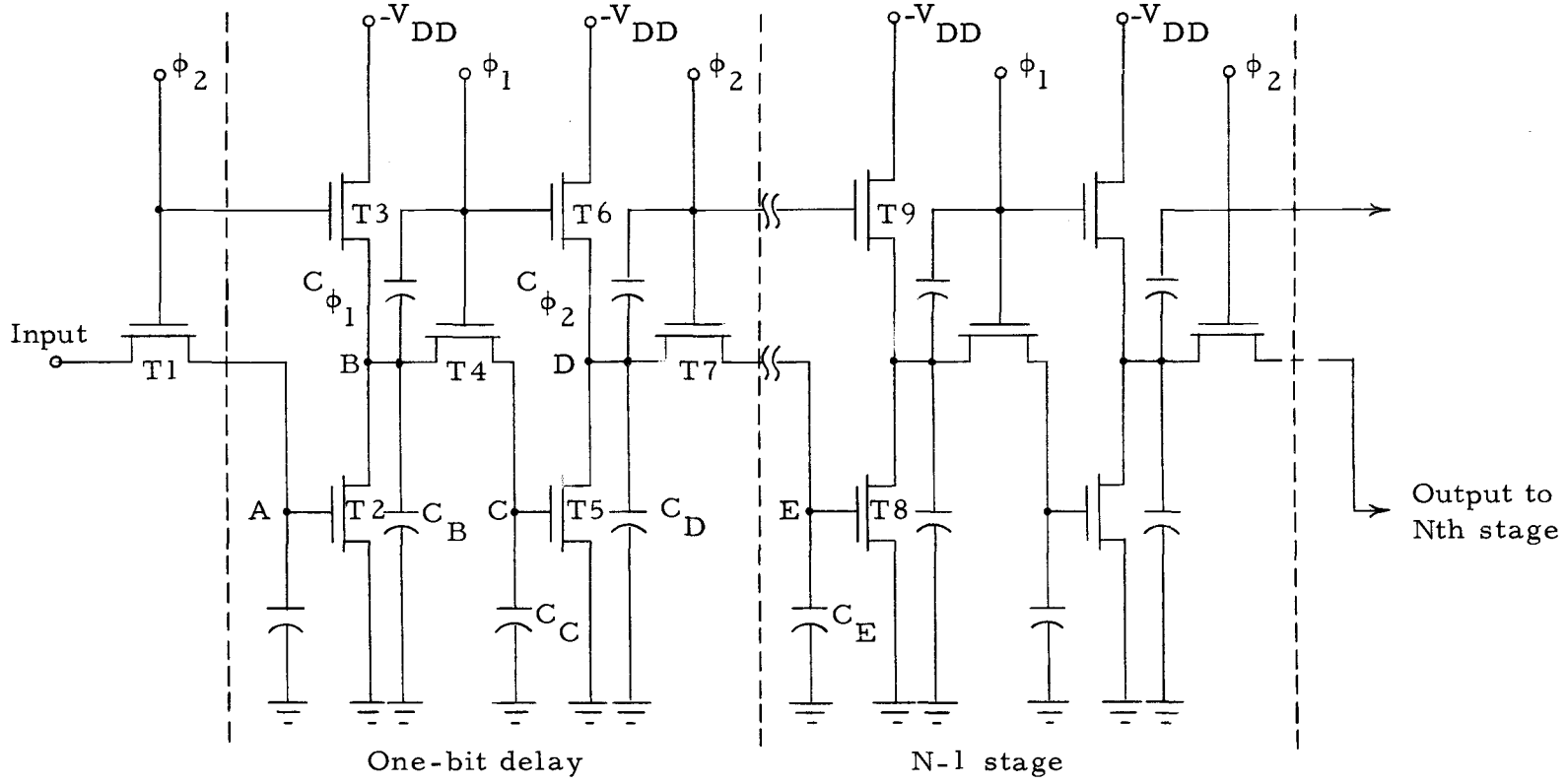


Figure 11. Two-phase dynamic shift register schematic (ratioless type).

The difference is that clock ϕ_1 drives a coupling transistor T4 in addition to the load resistor of the following inverter stage T6, rather than the previous load devices as in Figure 10. Likewise, ϕ_2 drives coupling transistor T7 and the load of the following inverter stage T9. Each delay stage consists of two inverters T2 and T5 in conjunction with a clocked load register T3 and T6, followed by two coupling devices T4 and T7. The concept of operation is such that information is clocked from one stage to the next, where it is temporarily stored on the inherent nodal capacitance associated with each MOS transistor. Alternate stages are clocked by clock ϕ_1 and ϕ_2, respectively. As can be seen from the timing diagram, Figure 12, the sequence of operation is as follows: if a logic "1" level is present at the input during ϕ_2 time, both T1 and T3 turn "ON", allowing the voltage at node B to assume a value which is determined by the ratio of the load and inverter devices T3 and T2, respectively. Since both T2 and T3 are almost the same minimum geometry devices, the "ON" resistance of the load and inverter are approximately equal, thus placing node B at $V_{DD}/2$. However, when clock ϕ_2 returns to ground (logic "0" level), T1 and T3 turn "OFF", storing a "1" level at node A, allowing T2 to remain in the "ON" state, thus continuing to discharge node B to a logic "0" level. When clock ϕ_1, goes negative (logic "1" level), T4 and T6 turn "ON", allowing previous information stored at

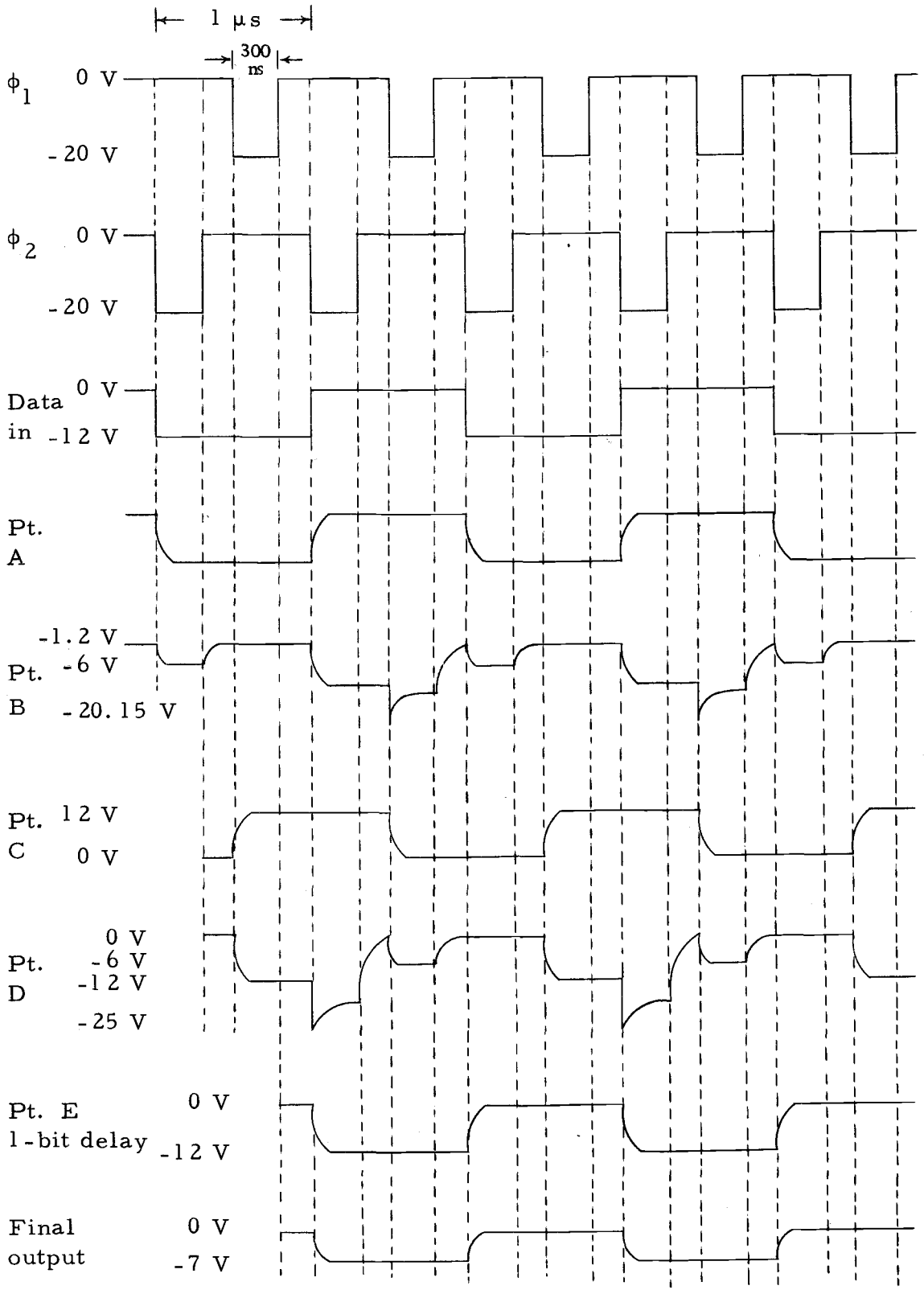


Figure 12. Timing diagram of each mode point for the ratioless type of dynamic shift register.

node C to discharge through T4 and T2, placing it at a logic "0" level. The energy coupled into node B through the intentionally added capacitance C_{ϕ_1} is discharged to the ground through T2. Because the logic level at node C is "0", T5 is in the "OFF" state, allowing T6, which is in the "ON" state, to charge node D to V_{DD}. When clock ϕ_1 returns to the ground (logic "0" level), T4 and T6 turn "OFF", allowing node C to remain at a logic "0" level. Likewise, the "1" level developed at node D is temporarily stored on the node capacitance (C_D). Again, when clock ϕ_2 goes negative (logic "1" level), T7 and T9 turn "ON", electrically connecting nodes D and E, allowing the voltage at node D to seek a level determined by the ratio of C_D and C_E.

Simultaneously, the energy which is coupled through the overlap capacitance C_{ϕ_2} during ϕ_2 increases the voltage level at node E by a capacitance ratio established by C_D, C_E and C_{ϕ_2}. Note that the capacitance C_B, C_C and C_{ϕ_1} and C_D, C_E and C_{ϕ_2} will be chosen such that the resultant voltage at its respective nodes exceeds the threshold voltage level of each inverter stage. The signal at node E is used to drive another stage or several stages to produce a series of shift register cells.

To summarize the circuit operation: during the time that ϕ_2 is negative, each stage will read its input and store that input (inverted) at its respective nodes. When ϕ_1 is negative, the stored

information from the previous stage is inverted and transferred to the following stage, thus providing a one-bit delay. In other words, information at A appears at E delayed by one clock period.

According to the above explanation for the two types of circuit, the ratioless type circuit is able to function with the use of all minimum geometry devices, since its driver-device geometry size is almost the same as its load size. This similarity allows a substantial reduction of both the cell size and the intrinsic capacitance of each node, thus permitting the cell to operate at a higher frequency. The power consumption is much lower than in most two-phase systems, since the smaller the size, the larger the turn-on resistance, allowing less current flow during the transition period.

Addressing Circuit Using Dynamic Shift Register

An addressing circuit was designed and is shown in Figure 14. Operation is as follows: according to the above operation of the dynamic shift register chain in which the first is coupled to the second, the second to the third, and so on, the logical input information will be delayed a certain amount of time.

Consider a chain with N stages. If the time interval between pulses is T, then the output from any stage is a pulse train of period NT, with each pulse of duration T. The output pulse of one stage is delayed by a time T from a pulse in the preceding stage.

In other words, the information is addressed in a certain specific location where the data should be stored in a memory.

By connecting the amplifying device at the end of each stage, the delayed information can be ready to be used in a certain location. When the ϕ_3 is clock pulses, which are different from those of the ϕ_1 and ϕ_2 clock, it may control the only desired address line during its delay function. Otherwise, the information is delayed on all output lines. The functional clock diagram is presented in Figure 13.

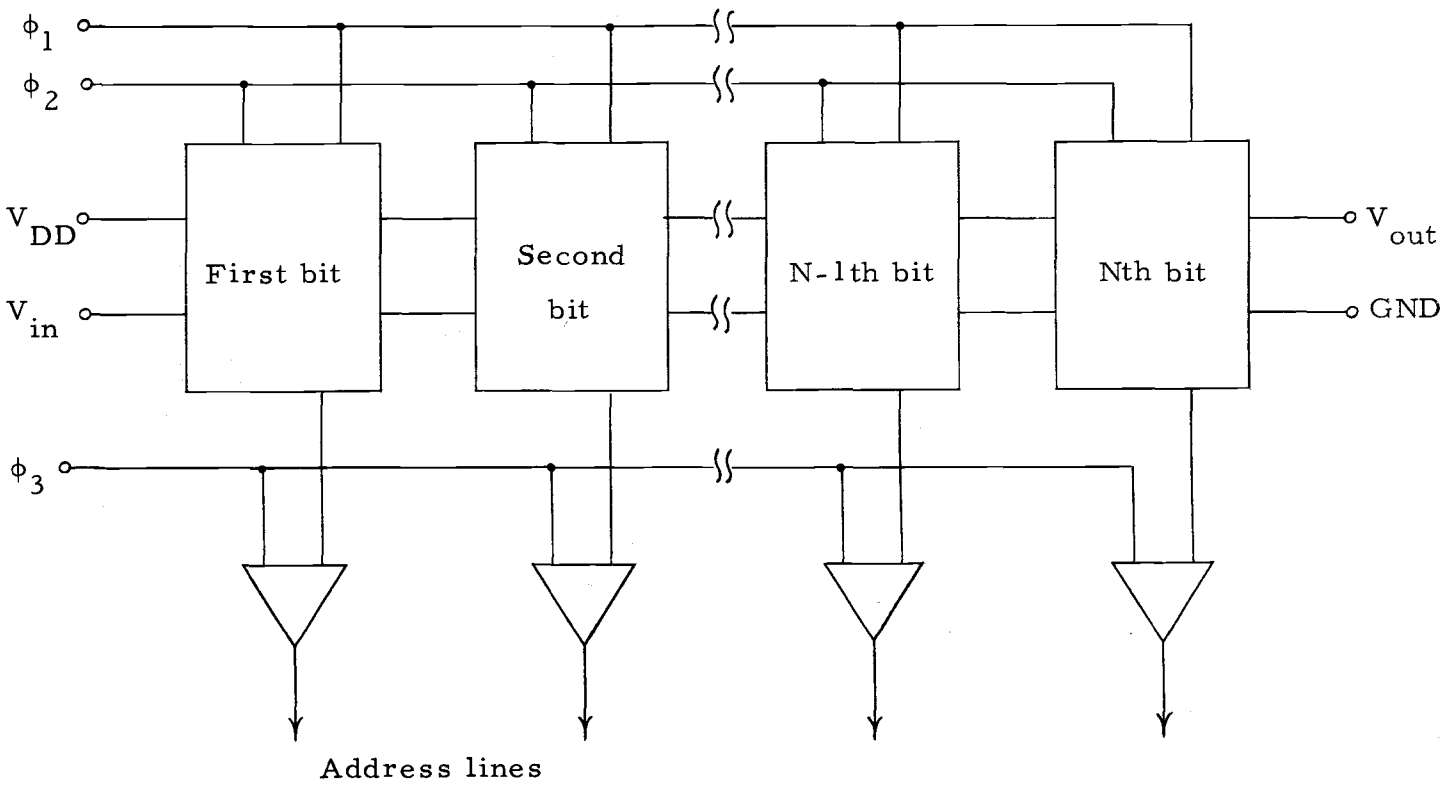


Figure 13. Functional block diagram showing address line connections.

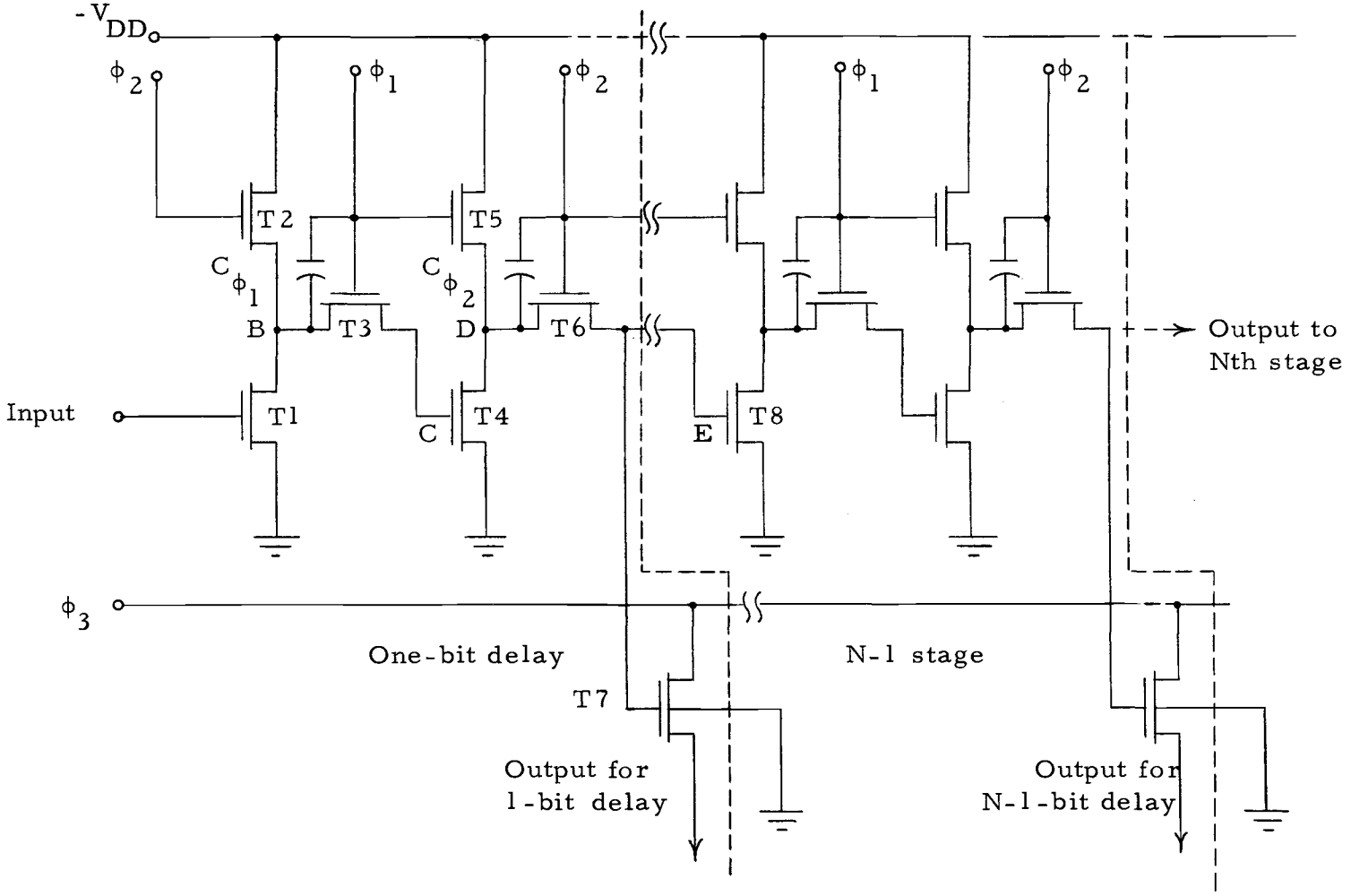


Figure 14. Two-phase, N-bit delay, addressing circuit.

III. DESIGN METHODS

Design Calculations

This circuit will be designed for "worst-case" conditions. The conditions are:

High Temperature

The hole mobility μ_p is a function of temperature which decreases with increasing temperature; therefore I_L decreases with increasing temperature. A lower charge current results in lower speed.

Low V_{DD}

With a lower V_{DD}, C_L charges to a smaller final voltage, and therefore takes longer to reach the voltage to turn on the next device.

Low V_{GG}

From Eq. (40), a low V_{GG} means a higher value of m, and therefore switching time will be slower.

High V_T

High V_T means less effective gate drive voltage, and again, less speed.

The design parameters are determined as follows:

$$V_{DD} = -12 \text{ V}$$

$$V_T = -5 \text{ V}$$

$$V_{in} = -11 \text{ V}$$

$$\phi_1 = \phi_2 = -20 \text{ V}$$

$$\phi_3 = -12 \text{ V}$$

$$t_{oxide} = 1200 \text{ Å (gate area)}$$

$$F_\phi = 1 \text{ MHz}$$

$$V_o = -6 \text{ V}$$

$$I_o = 3 \text{ ma}$$

where

V_{DD} is drain supply voltage

V_{GG} is gate supply voltage

V_T is threshold voltage

V_{in} is data input voltage

ϕ is clock input voltage

t_{oxide} is the thickness of oxide under the gate

V_o is final out-put voltage

I_o is output current level

As the voltage range for a logic "1" is from -8 V to -12 V, any input voltage within this range will turn on an inverter. Because the voltage range for a logic "0" is 0 V to -3 V, any input voltage within this range will turn off an inverter (see Appendix B).

Also, it may be assumed that the threshold voltage range is from -3 V to -5 V to satisfy the above input voltage ranges.

Thus the capacitance values from Eq. (19) are

1) Thin oxide (oxide thickness 1200 Å)

$$\frac{\epsilon_{ox}}{t_{ox}} = 0.19 \text{ pf/mil}^2 \simeq 0.2 \text{ pf/mil}^2$$

2) Thick oxide (oxide thickness 8000 Å)

$$\frac{\epsilon_{ox}}{t_{ox}} = 0.03 \text{ pf/mil}^2$$

3) Junction capacitance $C_{diff} = 0.05 \text{ pf/mil}^2$.

The threshold voltage variation ΔV_T is -2 V, since the starting material resistivity is 7 ~ 10 Ω cm (see Figure 3).

The geometrical size will be determined from the output device T7, whose substrate is grounded. It is assumed that the output current is needed 3 ma; therefore the turn-on resistance for the output device is approximately 2.5 KΩ. The resultant transconductance for the output device will be 400 μmhos.

From Eq. (40)

$$g_m = 2K(V_{GG}-(V_T+\Delta V_T))$$

$$\frac{W}{L} = \frac{2\frac{\epsilon_{ox}}{t_{ox}}\mu_p[V_{GG}-(V_T+\Delta V_T)]}{g_m}$$

$$= \frac{(5)(10^{-6})\ (11-7)}{(400)(10^{-6})}$$

$$\cong 20$$

And this device is in the saturated region, since it satisfies the condition $V_{GS} - V_T < V_{DD}$, $11 - 7 < 12$.

Capacitance calculation over the thin oxide gate area will be developed as follows:

1) Geometrical channel length is 0.4 mil

2) Side diffusion is 0.1 mil for both diffused areas

3) Actual device channel length is 0.3 mil.

Using an actual length of 0.3 mil yields a width of 6 mil for a W/L ratio of 20.

From Eq. (19) and Eq. (20), the sum of the capacitance for the output device which is due to the gate area, the diffused area and the thick oxide region for the output terminal is approximately 1.38 pf, since the gate area capacitance is

$$0.2\ \text{pf/mil}^2 \times 0.4\ \text{mil} \times 6\ \text{mil} = 0.48\ \text{pf},$$

the diffused junction capacitance is

$$0.05 \text{ pf/mil}^2 \times 6 \text{ mil}^2 = 0.3 \text{ pf}$$

and the thick oxide capacitance is

$$0.03 \text{ pf/mil}^2 \times 20 \text{ mil}^2 = 0.6 \text{ pf}$$

Charging node D with C_{ϕ_2} added at $t = 0$ when the ϕ_1 clock has just turned on, $V_D(0)$ float -12 V, and $V_D(0^+)$ will be

$$V_D(0^+) = -12 \text{ V}\left(\frac{C_{\phi_2}}{C_D+C_{\phi_2}}\right)(-20)$$

Choosing $C_{\phi_2} = 1.2$ pf, $C_D = 0.6$ pf, since the $C_{\phi_2} + C_D$ should be greater than C_E, so that the final voltage for node D should be great enough to turn on the next device.

Then

$$V_D(0^+) = -12 \text{ V} + \left(\frac{(-20)(1.2)}{1.8}\right) = -12 - 12.5 \text{ V} = -24.5 \text{ V}$$

From Eqs. (13) and (14) in Appendix A

$$V_E(t) = V_D(0^+)\frac{C_D+C_{\phi_2}}{C_D+C_{\phi_2}+C_E}\left[1-e^{-\frac{C_D+C_{\phi}+C_E}{RC_E(C_D+C_{\phi_2})}t}\right]$$

$$V_D(t) = -V_D(0^+)\frac{C_D+C_{\phi_2}}{C_D+C_{\phi_2}+C_E} + V_D(0^+)\left(\frac{C_D+C_{\phi_2}}{C_D+C_{\phi_2}+C_E}-1\right)e^{-\frac{C_D+C_{\phi_2}+C_E}{RC_E(C_D+C_{\phi_2})}t}$$

$$V_E(t) = (-24.5)(0.6)(1-e^{-\frac{t}{0.6RC_E}})$$

since

$$\frac{C_D+C_{\phi_2}}{C_D+C_{\phi_2}+C_E} = \frac{1.8}{3} = 0.6$$

$$= -15(1-e^{-\frac{t}{0.6RC_E}})$$

Solving for the time t which is required to charge up the node E to -11 V,

$$-11 = -15(1-3^{-\frac{t}{0.6RC_E}})$$

$$t = 0.78RC_E$$

At this time $V_D(t)$ is

$$V_D(t) = (-25)(0.6) + 25(0.4)e^{-\frac{t}{0.6RC_E}}$$

$$= -15 - 10(e^{-1.3}) = -17.7 \text{ V}$$

R_{on} for T6 device will be derived from this t value, which is 10 nsec or less because of necessity of faster switching time.

Choosing $t = 3$ nsec, R_{on} will be

$$R_{on} = \frac{3 \times 10^{-9}}{0.78 \times 1.4^{-12}} = 2.7 \text{ K.}$$

T6 is saturated since it satisfies the condition

$$V_{GG} - (V_T + \Delta V_T) < V_{DD}, \quad -20 + 7 < 17.7$$

Therefore

$$\left(\frac{W}{L}\right)_{T6} = \frac{1}{2K(V_{GG} - (V_T + \Delta V_T)(R_{on})}$$

$$= \frac{1}{(5)(10^{-6})(13)(2.7)(10^{3})}$$

$$= 6$$

To make g_m large enough to ensure faster switching and better conduction, a somewhat larger value was used in this design. Therefore,

$$\left(\frac{W}{L}\right)_{T6} \cong 10$$

From Eq. (40) g_m will be

$$g_m = 2K(V_{GS} - (V_T + \Delta V_T)$$

$$= 150 \ \mu\text{mhos} \quad \text{at} \quad V_{GS} = -10 \text{ V}$$

The load device T5 is non-saturated, since it satisfies the condition $V_{GG} - (V_T + \Delta V_T) > V_{DD}, \quad 20 - 7 > 12$. And from Eq. (40) the

biasing parameter m will be

$$m = -\frac{-12}{(-20+6)} = \frac{-12}{-14} = 0.9$$

Therefore, eight time constants are required to reach 90% charge for $C_{\phi_2} + C_D = 1.6$ pf from Figure 9.

$$t = 8RC_E$$

Choosing t = 200 nsec or less, since the clock pulse width is 300 nsec, R_L will be

$$R_L = \frac{(200)(10^{-9})}{(12.8)(10^{-12})} \cong 16 \text{ K}$$

where R_L is resistance for load device T5 from Eq. (9)

$$g_m = \frac{2}{R_L}$$

Therefore

$$(\frac{W}{L})_{T5} = \frac{2}{2K(V_{GG}-(V_T+\Delta V_T))R_L}$$

$$= \frac{2}{(16)(10^3)(13)(5)(10^{-6})} = 1.0 \cong 2$$

$$g_m \cong 30 \text{ } \mu\text{mhos}$$

when the gate voltage is -10 V. The inverter device T4 changes

from saturated into non-saturated operation. t_f is the time required to discharge $C_L = C_\phi + C_D$ to 10% of v_o, the off-level voltage and t' is the time required that the T4 device changes from saturated into non-saturated operation.

For $0 < t < t'$, T4 is saturated. Combining Eqs. (27) and (28), then

$$C_L \frac{dv_o}{dt} = K(V_{GS} - V_T)^2$$

$$\frac{C_L}{K(V_{GG} - V_T)^2} \int_{-11}^{-5} dv_o = \int_0^{t'} dt$$

$$t' = \frac{C_L}{6^2 K} \quad (11\text{-}5)$$

$$= \frac{6C_L}{36K}$$

For $t' < t < t_f$, T4 is non-saturated.

Combining Eqs. (31) and (32), then

$$C_L \frac{dv_o}{dt} = K[2(V_{GS} - V_T)v_o - v_o^2]$$

$$\int_{-6}^{-1.2} \frac{dv_o}{-v_o^2 + 12v_o} = \frac{L}{C_L} \int_{t'}^{t_f} dt$$

$$t_f - t' = -\frac{C_L}{6K}\tanh^{-1}\left(\frac{-v_o-6}{6}\right)\Bigg|_{-6}^{-1.2}$$

$$= -\frac{C_L}{6K}(-1.1)$$

$$t_f = \frac{1.1C_L}{6K} + \frac{6C_L}{36K}$$

$$= \frac{12.6\,C_L}{36K}$$

Assuming $t_f = 100$ nsec for a faster fall time, then W/L ratio of T4 is

$$\left(\frac{W}{L}\right)_{T4} = \frac{(1.8)(10^{-12})(12.6)}{(36)(2.5)(10^{-6})(100)(10^{-9})}$$

$$= 2.5$$

$$g_m = 40\ \mu\text{mhos}$$

From Eq. (19), the capacitance for this device which is due to the gate area is approximately 0.05 pf, the diffusion capacitance due to the diffused junction 0.02 pf and aluminum contact thick oxide capacitance 0.03 pf. Therefore total capacitance will be approximately 0.1 pf.

Performing the same procedure as the nodes D and E, the capacitances C_{ϕ_1} and C_B may be calculated to be 0.4 pf and 0.35 pf, respectively.

Then

$$V_B(0^+) = -12\ V + \frac{0.4}{0.75}(-20) = -22\ V,$$

since

$$\frac{C_{\phi_1}}{C_B + C_{\phi_1}} = \frac{0.4}{0.75}$$

and

$$V_C(t) = -22 \times 0.87\left(1 - e^{-\frac{t}{0.87RC_C}}\right),$$

since

$$\frac{C_B + C_{\phi_1}}{C_B + C_{\phi_1} + C_C} = \frac{0.75}{0.85} = 0.87$$

when

$$V_C(t) = -11\ V$$

$$-11 = (-22)(0.87) + (10)e^{-\frac{t}{0.87RC_C}}$$

Therefore

$$t = 0.76\ RC_C$$

and V_B at the time $t = 0.76RC_C$ is

$$V_B(t) = -19 - \left(2.86\ e^{-\frac{0.76RC_C}{0.87RC_C}}\right)$$

$$= -19 - (2.86\ e^{-0.87})$$

$$= -19 - 1.15\ V$$

$$= -20.15\ V.$$

T3 is saturated since it satisfies the condition

$$V_{GG} - (V_T + \Delta V_T) < V_{DD}, \quad 20 - 7 < 20.15$$

R_{on} for T3 device will be derived from this t, for which a faster switching time is required. The t may be calculated as 0.3 nsec.

Therefore

$$R_{on} = \frac{(0.3)(10^{-9})}{(0.76)(10^{-13})} = 4K$$

and

$$\left(\frac{W}{L}\right)_{T3} = \frac{1}{(5)(10^{-6})(4)(10^{-3})(13)}$$

$$\cong 4$$

A somewhat larger (W/L) ratio was needed for this coupling device to ensure faster switching speed and better conduction.

(W/L) ratio was increased as 10. The load device T2 is non-saturated. The condition is $V_{GG} - (V_T + \Delta V_T) > V_{DD}$, $20 - 7 > 12$. The biasing parameter from Eq. (40) m is

$$m = \frac{-12}{(-20+7)} = 0.9$$

Therefore, eight time constants are required to reach 90% charge for $C_{\phi_1} + C_B = 0.75$ pf from Figure 9. Therefore $t = (8)(0.75\,\text{pf})R_L$. Choosing $t = 100$ nsec, since the clock pulse width is 300 nsec, R_L will be

$$R_L = \frac{(100)(10^{-9})}{(6)(10^{-12})} = 17K$$

where this R_L is the resistance for the load device T2. From Eq. (9)

$$g_m = \frac{2}{R_L}$$

Therefore,

$$(\frac{W}{L})_{T2} = \frac{2}{(17)(10^3)(65)(10^{-6})} = 1.8 = 2$$

T1 changes from saturated into non-saturated operation. Similar to the T4 calculation, T1 is saturated for $0 < t < t'$. Combining Eqs. (27) and (28)

$$C_L \frac{dv_o}{dt} = K(V_{GS}-V_T)^2$$

where C_L is $C_{\phi_1} + C_B$

$$\frac{C_L}{K(V_{GS}-V_T)^2} \int_{-11}^{-5} dv_o = \int_0^t dt$$

$$t = \frac{C_L}{36K}(11-5) = \frac{6C_L}{36K} = \frac{C_L}{6K}$$

For $t' < t < t_f$, T1 is non-saturated. Combining Eqs. (31) and (32)

$$C_L \frac{dv_o}{dt} = K[2(V_{GS}-V_T)v_o - v_o^2]$$

$$\int_{-6}^{-1.2} \frac{dv}{-v_o^2+12v_o} = \frac{K}{C_L} \int_{t'}^{t_f} dt$$

$$t_f - t' = \frac{C_L}{6K} \tanh^{-1}\left(\frac{-v_o-6}{6}\right) \Bigg|_{-6}^{-1.2}$$

$$t_f = t' + \frac{1.1C_L}{6K}$$

$$= \frac{C_L}{6K} + \frac{1.1C_L}{6K}$$

$$= \frac{2.1C_L}{6K}$$

Assuming that $t_f = 50$ nsec for a faster response, then (W/L) ratio will be

$$\left(\frac{W}{L}\right)_{T1} = \frac{(0.75)(10^{-12})(2.1)}{(6)(2.5)(10^{-6})(50^{-7})(10^{-8})}$$

$$\cong 2$$

Power consumption for each stage will dissipate in one inverter where both the load and driver device turn on simultaneously. From Eq. (23) and (17)

$$P = -V_{DD}K[V_{GS}-(V_T+\Delta V_T)]^2$$

$$= (12)(2.5)(10^{-6})(13^2)$$

$$= 6.06 \text{ m W}$$

The resultant W/L ratios of the devices of this dynamic shift register basic stage are summarized in Table 1. The actual widths and lengths shown in this table are the dimensions of the first oxidation removal patterns on the fabrication mask to diffuse P type material. The calculated R_{on} and g_m which are determined at the gate voltage -10 V are shown in Table 1. Each capacitance of the devices is also shown in Table 2.

Table 1. W/L ratios of each device.

Devices	W/L	W	L	g_m	R_{on}
T1	2	0.6	0.3	30 μmhos	33K
T2	2	0.6	0.3	30 μmhos	33K
T3	10	3	0.3	150 μmhos	7K
T4	2.5	0.75	0.3	40 μmhos	25K
T5	2	0.6	0.3	30 μmhos	33K
T6	10	3	0.3	150 μmhos	7K
T7	20	6	0.3	400 μmhos	2.5K

Table 2. Capacitance values.

C_{ϕ_1}	C_{ϕ_2}	C_B	C_C	C_D	C_E
0.4 pf	1.2 pf	0.35 pf	0.1 pf	0.6 pf	1.4 pf

Fabrication Process and Results

The MOS fabrication process is simpler and inherently more reliable than conventional triple--diffused junction--transistor integrated circuitry. The MOS also has a size advantage over conventional

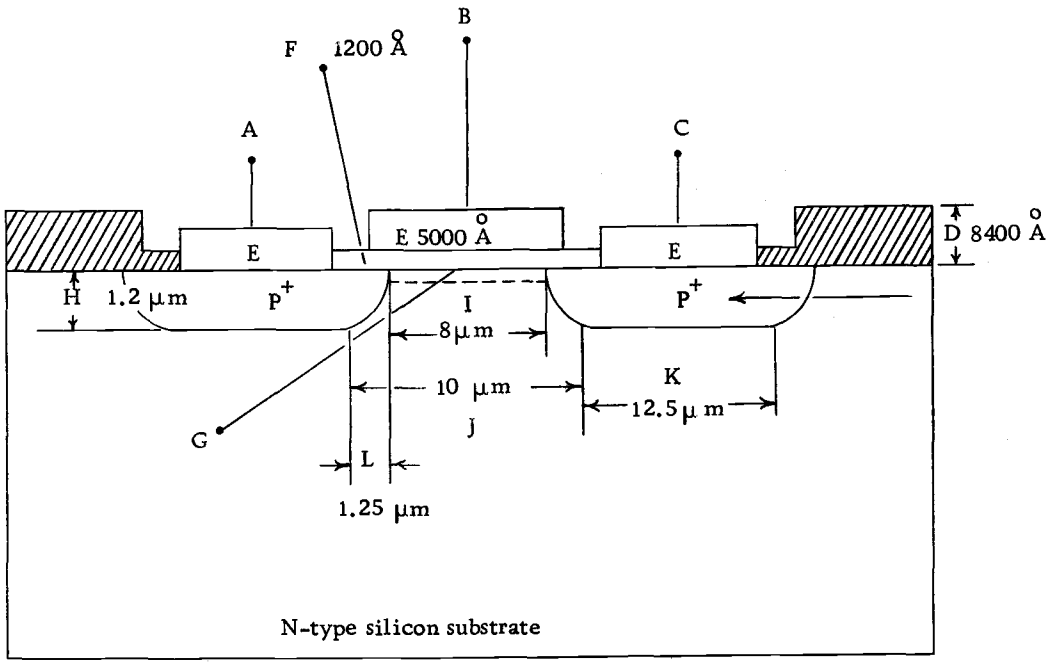
integrated circuits. The use of the active load resistor in place of conventional diffused resistors also further reduces the size of MOS integrated circuits. Because of this smaller size, and of the higher yields of the MOS process, the complexity of integrated circuits can be increased by an order of magnitude (17).

This paper, however, presents larger scale of designing parameters in order to have some flexibility for experimental purposes. Design parameters are listed below:

1. Geometry parameters
   a. Chip size is 1000 x 1000 μm (40 mils x 40 mils).
   b. All interconnecting leads are 25 μm (1 mil) with 12.5 μm ~ 50 μm (0.5 mil ~ 2 mil) spacings.
   c. Bonding pads are 100 μm x 100 μm (4 mils x 4 mils).
   d. P to P spacings are 10 μm (0.4 mil) long.
   e. Contact holes are 12.5 ~ 25 μm^2 (0.5 ~ 1 mil^2).
   f. Gate mask overlaps are 6.25 μm (0.25 mil).
2. Oxide thickness
   a. Thick oxide is 8400 Å thick.
   b. The oxide over the diffusions is 1200 Å thick.
   c. The gate oxide is 1200 Å.
3. The crystal orientation <100>.
4. The junction depth is 1.2 μm.
5. The implied starting-resistivity is 7 ~ 10 ohm - cm.

6. Sheet resistance after diffusion is 18 Ω/□.

The expected cross-sectional structure of this design is presented in Figure 15 and the total physical layout for the basic 1-bit cell is shown in Figure 16. The gate area, contact holes and metal mask are superimposed upon the diffusion area mask. This basic cell is repeated by using the photo-mask making technique to get a desired nth-bits delay stage mask.



A) Drain terminal
B) Gate terminal
C) Source terminal
D) Thick oxide
E) Metal electrodes
F) Gate region thin oxide
G) Channel
H) Junction depth
I) Actual channel length
J) Geometry channel length
K) Diffusion region width
L) Side diffusion

Figure 15. Cross-sectional structure of the device.

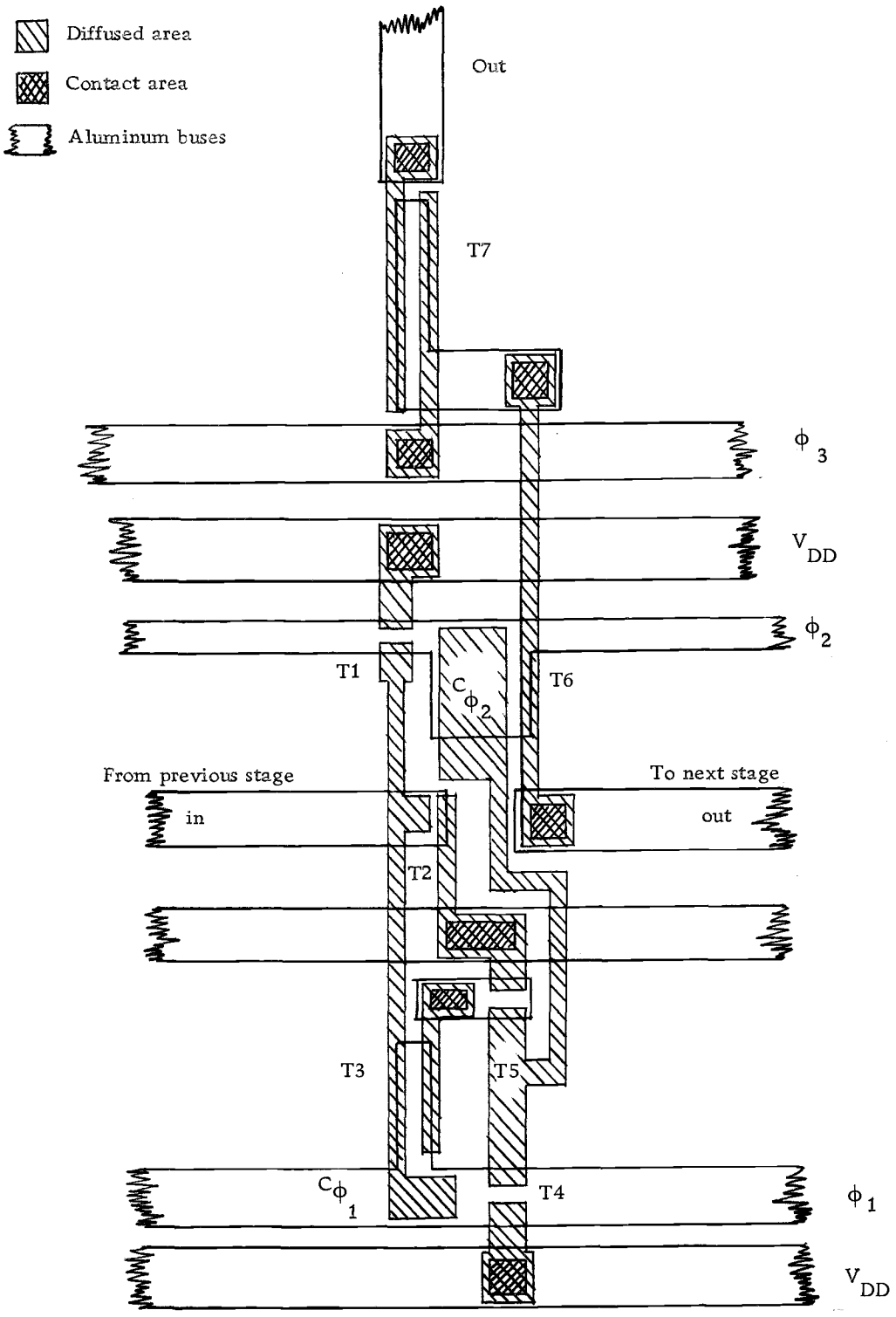


Figure 16. Layout of the dynamic SR basic one-bit cell.

IV. EXPERIMENTAL RESULTS

Characteristics of Devices Used for Tests

The characteristics of the four devices whose geometry sizes are different from each other were measured and listed in the following table.

Table 3. Device characteristics.

Parameter	T1($\frac{W}{L}$=2)	T4($\frac{W}{L}$=2.5)	T3($\frac{W}{L}$=10)	T7($\frac{W}{L}$=20)	Units
V_T	-4.2	-4.1	-3.1	-3.56	V
g_m	50	40	220	420	μmho
BV_{DS}	-55	-50	-45	-45	V

The photographed characteristics of the T7 device are shown in Figure 17.

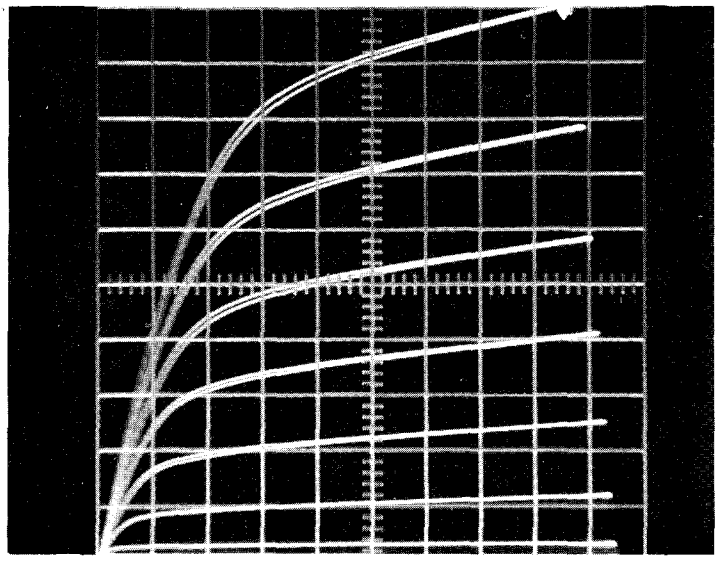


Figure 17. Characteristic curve of T7 device (W/L = 20). Vertical 200 μa/major division, horizontal 2V/major division, V_{GG} 1 V/step (V_G levels are also shown).

The Results of the Circuit

Table 4. Operating conditions.

Parameters	Designed value		Lab measurement			Unit
	Min	Max	Min	Typ	Max	
Supply voltage V_{DD}	-8	-12	-11	-14	-17	V
Supply voltage V_{GG}	-16	-20	-16	-18	-23	V
Supply voltage V_{ϕ_3}	-8	-12	-11	-14	-17	V
Width of data pulse, t_p (data) (see Figure 18)		1	.2	.6	.85	μs
Width of clock pulses, $t_p(\phi_1)$ (see Figure 18)	.3	3	.2	.4	2	μs
, $t_p(\phi_2)$ (see Figure 18)	.3	3	.2	.6	2	μs
Rise time of clock pulse, $t_f(\phi)$ (see Figure 18)			0.1			μs
Fall time of clock pulse, $t_f(\phi)$ (see Figure 18)			0.1			μs
Clock repetition rate	.2	1	.01	0.22	1.2	MHz
Temperature variation			25°C	25°C	120°C	°C

Table 5. Electrical characteristics.

Parameters	Test conditions	Lab measurement Min	Typ	Max	Unit
$V_{in}(1)$ input voltage (logical 1)		- 9	-10	-15	V
$V_{in}(0)$ input voltage (logical 0)		0		- 2	V
$V_{in}(1)\phi$ input voltage (logical 1) at either clock input		-16	-18	-25	V
$V_{in}(0)\phi$ input voltage (logical 0) at either clock input		0		- 2	V
$V_{out}(1)$ logical 1 output voltage	f_{clock} = 500 KHz	-11	-12	-14	V
$V_{out}(0)$ logical 0 output voltage	f_{clock} = 500 KHz			- 1	V
V_{out} out voltage at each stage	R_L = 20 KΩ to GND	- 3	- 5	- 7	V
C_{in} capacitance of data	V_{in} = -10V f = 500 KHz TA = 25° C			0.1	pf
$C_{in}\phi_1$ capacitance of clock ϕ_1 input	$V_{in}\phi_1$ = -18 V f = 500 KHz TA = 25° C			0.4	pf
$C_{in}\phi_2$ capacitance of clock ϕ_2 input	$V_{in}\phi_2$ = -18 V f = 500 KHz TA = 25° C			1.2	pf
I_{DD} supply current into V_{DD} terminal	V_{DD} = -14 V, V_{GG} = -18 V	.43	.6	.9	ma
I_{GG} supply current into V_{GG} terminal	V_{DD} = -14 V, V_{GG} = -18 V			1.2	ma
Power dissipation/stage	V_{DD} = -14 V, V_{GG} = -18 V		8.4	13.5	mW

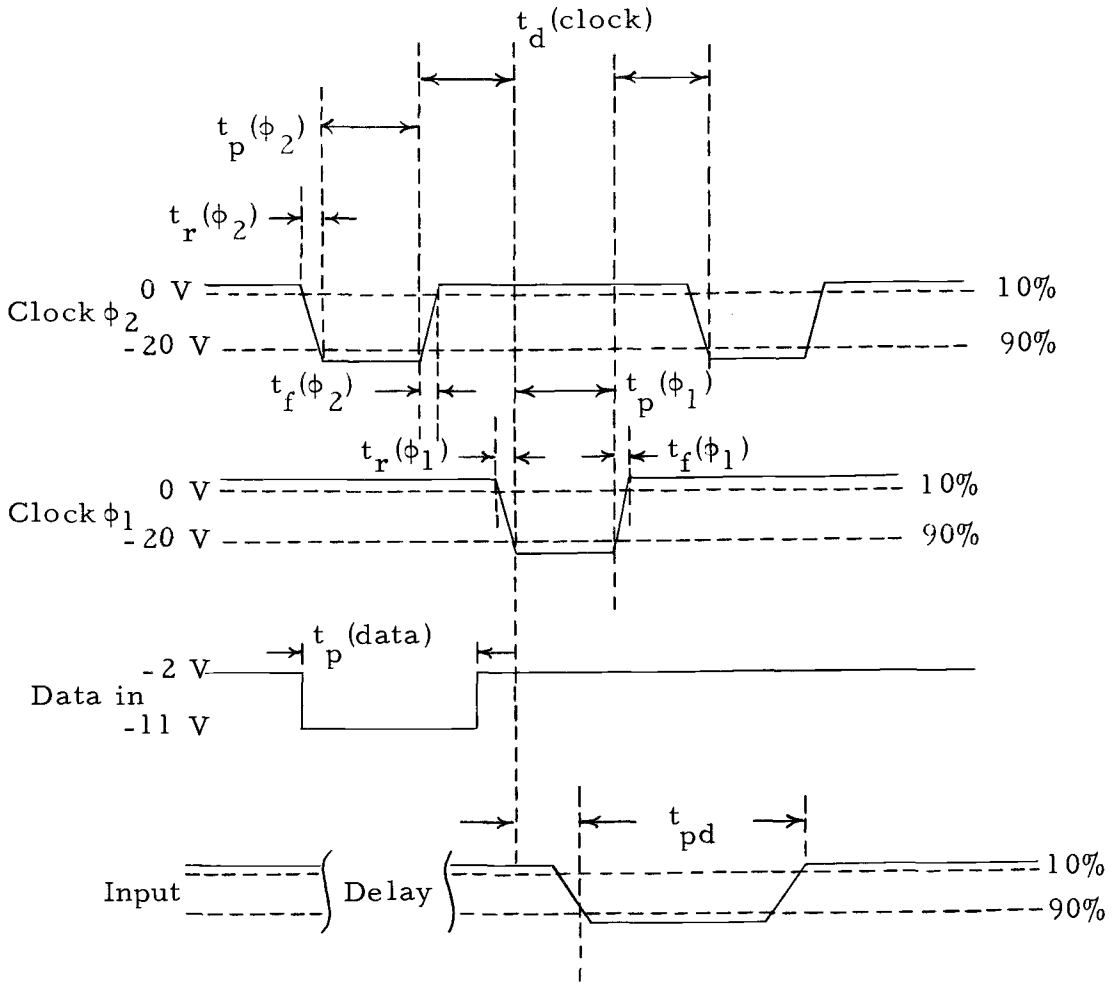


Figure 18. Analysis of voltage waveforms.

The photographed output waveforms are shown in Figures 19, 20, 21, and 22 for a one-bit delay, a two-bit delay, a three-bit delay and a four-bit delay, respectively.

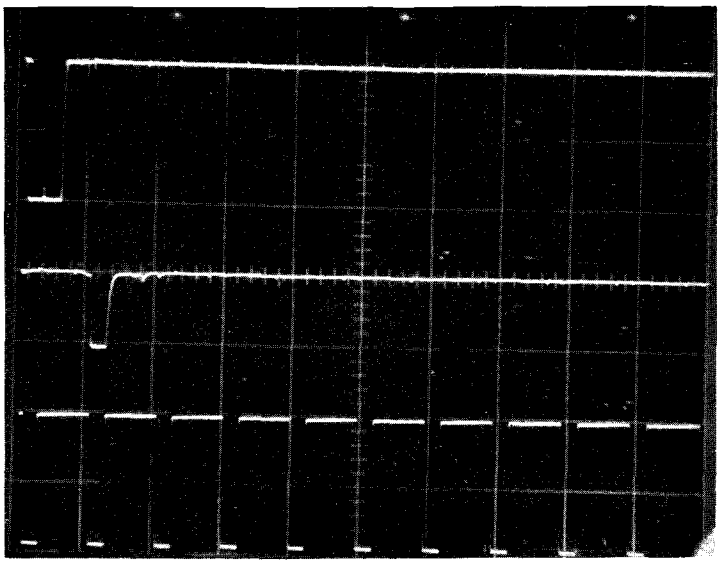


Figure 19. One-bit delay waveform. (Top, data input; center, output; bottom, clock; Vertical: 5V/division for top and center, 10V/division for bottom; Horizontal: 2 μsec/division.)

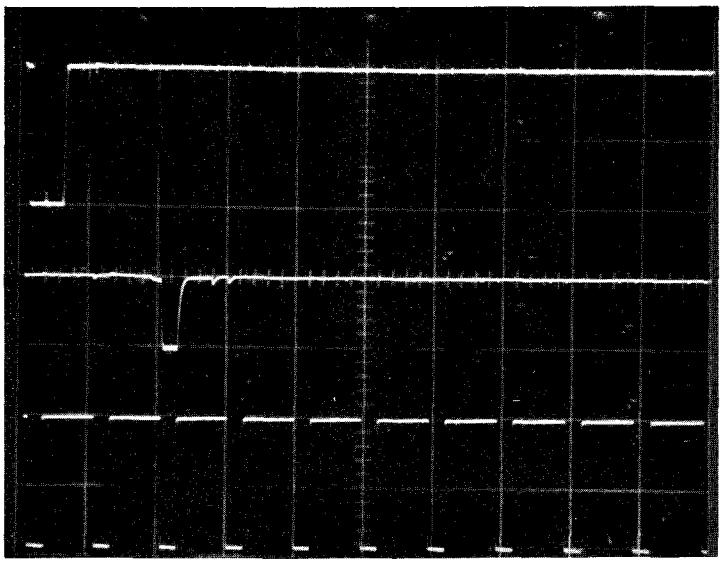


Figure 20. Two-bit delay waveform. (Vertical: 5V/division for top and center, 10V/division for bottom; Horizontal: 2 μsec/division.)

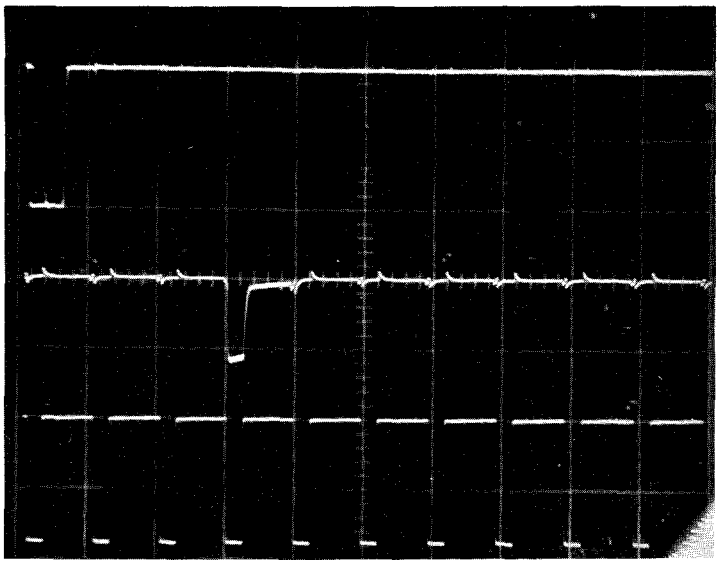


Figure 21. Three-bit delay waveform. (Vertical: 5V/division for top and center, 10V/division for bottom; Horizontal: 2 μsec/division.)

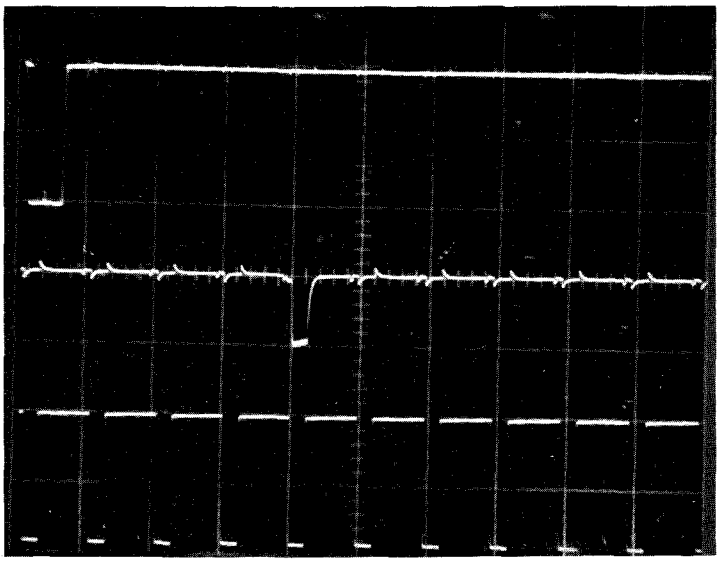


Figure 22. Four-bit delay waveform. (Vertical: 5V/division for top and center, 10V/division for bottom; Horizontal: 2 μsec/division.)

V. CONCLUSION

An integrated addressing circuit has been designed. It has been shown that the ratioless type technique offers several advantages in certain circuit applications which cannot be equaled by any of the other types of techniques. In particular, the final results show that the ratioless type circuit can have a smaller geometry size and less nodal capacitance over the ratio-type technique in a two-phase dynamic shift register circuit. The power-dissipation is also lower than that of the others.

The performance of this circuit was also enhanced by the presence of a low threshold voltage (V_T = -3.1 V). This explains why the clock and supply voltage amplitudes are required to be only -16 and -8 volts, respectively. The intentionally added capacitors assured a higher voltage on the gate at node B.

In regard to applicability of this ratioless technique in this addressing circuit, it appears that the sequentially added stage may be used in digital systems.

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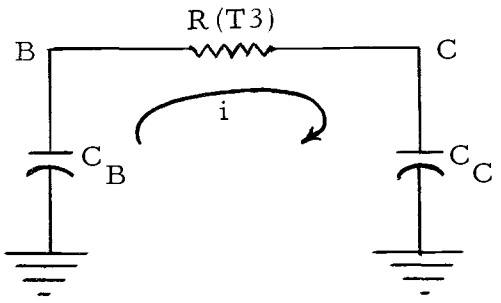
APPENDICES

APPENDIX A

Charging Node B Without C_ϕ Added

The equivalent circuit diagram when ϕ_2 has just turned on is shown below.



At $t = 0$ when ϕ_1 turns on

$$V_F(0^+) = V_F(0^-) = -12 \text{ volts}$$

where $V_F(0^+)$ is the voltage that ϕ_1 just turns on and $V_F(0^-)$ is the voltage that node B was at -12 volts and T2 has just turned off.

The voltage equation for the circuit becomes

$$V_B = V_C + iR \tag{A-1}$$

$$\frac{1}{C_B}\int idt + V_B(0) = \frac{1}{C_C}\int_0^t idt + i(t)R \tag{A-2}$$

By using the Laplace transforms, the above Eq. (A-2) will be

$$-\frac{1}{C_B}\frac{I(s)}{s}+\frac{V_B(0)}{s}=\frac{1}{C_C}\frac{I(s)}{s}+I(s)R$$

$$i(s)\left[-\frac{1}{sC_B}-\frac{1}{sC_C}-R\right]=\frac{-V_B(0)}{s}$$

$$i(s)=\frac{\frac{V_B(0)}{s}}{\frac{1}{sC_B}+\frac{1}{sC_C}+R}=\frac{V_B(0)sC_BC_C}{(C_C+C_B+RC_CC_Bs)}$$

$$=\frac{\frac{V_B(0)C_BC_C}{RC_CC_B}}{s\frac{RC_CC_B}{RC_CC_B}+\frac{C_C+C_B}{RC_CC_B}}$$

$$=\frac{V_B(0)}{s+\frac{C_C+C_B}{RC_CC_B}} \qquad \text{(A-3)}$$

Its inverse is readily recognized as

$$i(t)=\frac{V_B(0)}{R}\,e^{-\left(\frac{C_C+C_B}{RC_CC_B}\right)t} \qquad \text{(A-4)}$$

And $V_c(t)$ will be

$$v_c(t) = \frac{1}{C_C}\int_0^t i(t)dt = \frac{V_B(0)}{C_C R}\int_0^t e^{-\left(\frac{C_C+C_B}{RC_CC_B}\right)t}\,dt$$

$$= -\frac{V_B(0)}{C_C R}\,\frac{RC_CC_B}{C_C+C_B}\,e^{-\left(\frac{C_C+C_B}{RC_CC_B}\right)t} + \frac{V_B(0)}{C_C R}\,\frac{RC_CC_B}{C_C+C_B} \qquad \text{(A-5)}$$

Let $t = \infty$; for the final V_C value

$$v_c(\infty) = V_B(0)\,\frac{C_B}{C_C+C_B} = -12\left(\frac{0.35}{0.45}\right) = -9.3 \quad \text{volts}$$

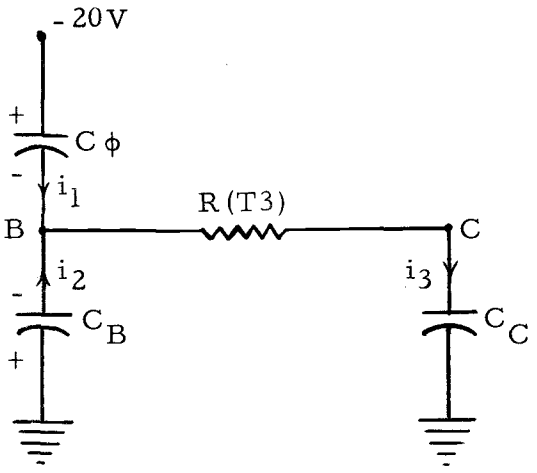
This is the voltage for the final value at node C.

Charging Node B With C_ϕ

The purpose of the added capacitance, C_ϕ is to determine a final value of V_C after node C is changed to -11 volts.

The equivalent circuit diagram when the clock ϕ_2 has just turned on is shown below. From the following equivalent circuit, the current equation will be

$$i_1 + i_2 = i_3 \qquad \text{(A-6)}$$



The differential equations between current and voltage for each capacitance, and their transforms are

$$i_1 = C_\phi \frac{d(-20-V_B)}{dt} = -C_\phi \frac{d(V_B)}{dt} \qquad \text{(A-7a)}$$

$$i_2 = -C_B \frac{d(V_B)}{dt} \qquad \text{(A-7b)}$$

$$i_3 = C_C \frac{dV_C}{dt} \qquad \text{(A-7c)}$$

$$i_1(s) = -C_\phi (sV_B(s) - V_B(0)) \qquad \text{(A-8a)}$$

$$i_2(s) = -C_B (sV_B(s) - V_B(0)) \qquad \text{(A-8b)}$$

$$i_3(s) = C_C (sV_C(s) - V_C(0)) \qquad \text{(A-8c)}$$

Substituting the Eqs. (A-8a, b, c) into Eq. (A-6), then

$$-(C_B+C_\phi)(sV_B(s)+V_B(0)) = C_C(sV_C(s)) \qquad \text{(A-9)}$$

and the voltage relation is

$$V_B(s) = V_C(s) + Ri_3(s)$$

$$V_B(s) = V_C(s) + RC_C(s)V_C(s) \qquad \text{(A-10)}$$

By simultaneous solution of Eqs. (A-9) and (A-10)

$$V_C(s) = \frac{-V_B(0)(C_B+C_\phi)}{s(C_B+C_\phi)(RC_Cs)+s(C_B+C_\phi)+C_Cs} \qquad \text{(A-11)}$$

After some algebraic manipulation, then

$$V_C(s) = \frac{-V_B(0)}{RC_C} \frac{1}{s[s+\frac{C_B+C_\phi+C_C}{RC_C(C_B+C_\phi)}]} \qquad \text{(A-12)}$$

And its inverse will be

$$V_C(t) = -V_B(0)\frac{C_B+C_\phi}{C_B+C_\phi+C_C}\left[1-e^{-(\frac{C_B+C_\phi+C_C}{RC_C(C_B+C_\phi)})t}\right] \qquad \text{(A-13)}$$

Solving for the $V_B(t)$ by the same procedure:

$$V_B(t) = -V_B(0^+)\frac{C_B+C_\phi}{C_B+C_\phi+C_C} + V_B(0^+)(\frac{C_B+C_\phi}{C_B+C_\phi+C_C}-1)e^{-\frac{C_B+C_\phi+C_C}{RC_C(C_B+C_\phi)}t}$$

(A-14)

the final V_B voltage will be determined when $t = \infty$

$$V_B(\infty) = -V_B(0^+) \frac{C_B+C_\phi}{C_B+C_\phi+C_C}$$

$$= (-22V)(0.87) = -19\,V$$

since

$$\frac{C_B+C_\phi}{C_B+C_C+C_\phi} = 0.87$$

Therefore, the intentionally added capacitor C_ϕ assures -11 volts at node B, instead of the -9.3 volts.

APPENDIX B

In order to determine the operating input voltage level, the threshold voltage, V_T variation during the fabrication process should be considered.

Considering $V_T = -3.5V$ from the theoretical calculation (see page 12), the typical values of the threshold voltage variation may be assumed from $-3V$ to $-5V$ with which the calculation will be started.

In case V_T is $-3V$ and both the load and the driver devices are turned on, the voltage on node B in Figure 14 is $V_{DD}/2$ which this must be at least $-3V$ to turn on the next device. And supply voltage V_{DD} must be at least $-6V$ since the geometry of the load and the driver device is approximately the same.

To verify that the voltage on node B, $-3V$ can turn on the next device T4, the following calculations will be done.

When the ϕ_1 clock has just turned on, $V_B(0^-)$ is floating at $-6V$, and $V_B(0^+)$ will be

$$V_B(0^+) = -6 + (-6)(\frac{0.4}{0.75}) = -9.5\,V$$

since

$$\frac{C_{\phi_1}}{C_B + C_{\phi_1}} = \frac{0.4}{0.75}.$$

And substituting the above values into Eq. (13) in Appendix A yields

$$V_C(t) = -9.5 \times 0.87\left(1-e^{-\frac{t}{0.87RC_C}}\right)$$

since

$$\frac{C_B+C_{\phi_2}}{C_B+C_{\phi_2}+C_C} = \frac{0.75}{0.85} = 0.87.$$

When

$$V_C(T) = -3V$$

$$-3 = -9.5 \times 0.87\left(1-e^{-\frac{t}{0.87RC_C}}\right)$$

Therefore,

$$t = 0.07RC_C.$$

From Eq. (14) in Appendix A $V_B(t)$ at the time $t = 0.07RC_C$ will be

$$V_B(t) = -6 \times (0.87) + (-6) \times (0.13) \times \left(e^{-\frac{0.07RC_C}{0.87RC_C}}\right)$$

$$= -5.2 - 0.4 = -5.6\,V$$

when $t = \infty$, the $V_B(\infty)$ will be

$$V_B(\infty) = -5.2V$$

This is the final voltage for the node B, which can of course, turn on the next device. To avoid the noise margin, V_{DD} may be chosen as $-8V$ as its minimum operating value. Naturally voltages

less than $-3V$ will not be able to turn on the driver device.

The clocks ϕ_1 and ϕ_2, which are the gate input voltages for both the load and the coupling device in this circuit, can be determined from the following.

The load device should be in non-saturated condition, that is, $V_{GG} - (V_T + \Delta V_T) > V_{DD}$ (Eq. 40). Therefore

$$V_{GG} > -8V - 5V = -13V$$

since $V_T = -3V$ and ΔV_T due to the back gate bias effect is approximately $-2V$ from Figure 3.

However, from Eq. (40), the biasing parameter m will be

$$m = \frac{V_{DD}}{V_{GG} - (V_T + \Delta V_T)} = \frac{-8}{-13.5} = 1$$

When $m = 1$, the switching time constant must be at least 18τ from Figure 8. Therefore V_{GG} should be at least $16V$ to make m smaller, thus improving the operation of the circuit.

When the threshold voltage is $-5V$, which is the "worst case", V_{DD} and V_{GG} will be determined as $-12V$ and $-20V$, respectively, by a similar procedure as above.

As far as the clock pulse rates are concerned, it has been assumed that the desired operating frequency range is from 200 KHz to 1 MHz and the two clock pulses, ϕ_1 and ϕ_2, do not overlap

each other. Therefore, the minimum time interval becomes 1 μ second for each clock cycle and the allowed pulse width could be at most 0.3 μsec for 1 MHz clock repetition rate.

In case of a 200 KHz clock rate, the allowable pulse width will be 3 μsec. And the pulse width for the data input may be the same as the clock cycle.

The voltage level for ϕ_3 is chosen in the same way as the V_{DD} level, to turn on the output device. All the values determined in this fashion are listed in Table 4.