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John G. Kenney

Multi-level decision feedback equalization (MDFE) is a sampled signal processing technique for data recovery from magnetic recording channels which use the 2/3(1,7) run length limited code. The key adaptive feedback loops in MDFE are those which perform the timing recovery, gain recovery, dc offset detection, and adaptive equalization of the feedback equalizer. The algorithms used by these adaptive loops are derived from the channel error which is the deviation of the equalized signal from its ideal value. It is advantageous to convert this error signal to a digital value using a flash analog-to-digital converter (flash ADC) to simplify the implementation of the adaptive loops.

In this thesis, a scheme to place the thresholds of the flash ADC is presented. The threshold placement has been optimized based on the steady-state probability density function (pdf) of the signal to be quantized. The resolution constraints imposed by this quantization scheme on the adaptive loops has been characterized. As the steady-state assumption for the signal to be quantized is not valid during the transient state of the adaptive loops, the loop transients with this quantization scheme have been analyzed through simulations. The conditions under which the channel can recover from a set of start-up errors and converge successfully into steady-state have been specified. The steady-state channel performance with the noise introduced by the iterative nature of the adaptive loops along with this quantization scheme has also been verified.

Optimum Quantization for the Adaptive Loops in MDFE

by

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CHAPTER 1

INTRODUCTION

1.1 Introduction to magnetic recording

Magnetic storage of digital data is a booming industry with the advent of the information age. Vast improvements have been made in the design of the magnetic head, storage media and servo accuracy resulting in higher densities, greater operating speeds and more reliable storage systems. In order to extend the storage system performance without straining its physical and mechanical components, attention has been focused on exploiting signal processing techniques for improved data recovery from the read head. This has been further aided by the fact that the disk write and read processes are very similar to the data transmission and detection in digital communication channels.

Multilevel decision feedback equalization (MDFE) developed by Kenney et al., [1993] is a sampled signal processing technique for data recovery from storage channels. In order to highlight its salient features, the general hierarchy in a magnetic recording system is introduced. Fundamental to any magnetic recording system is the write and read processes shown in Figure 1.1 and described below:

The write head stores the digital data on the storage medium using saturation recording. In saturation recording, the current that flows through the write head induces a flux on the storage medium to store digital data. The non-return to zero inverse modulation (NRZI) is the scheme used to translate the data bit stream to a two level write current signal for the recording head. As seen in Figure 1.1, symbols '1' generate a transition in the write current causing the magnetization polarity to change. Symbols '0' cause no change in the direction of the write current and hence the magnetization polarity is left unchanged. NRZI modulation is performed by a component of the storage channel

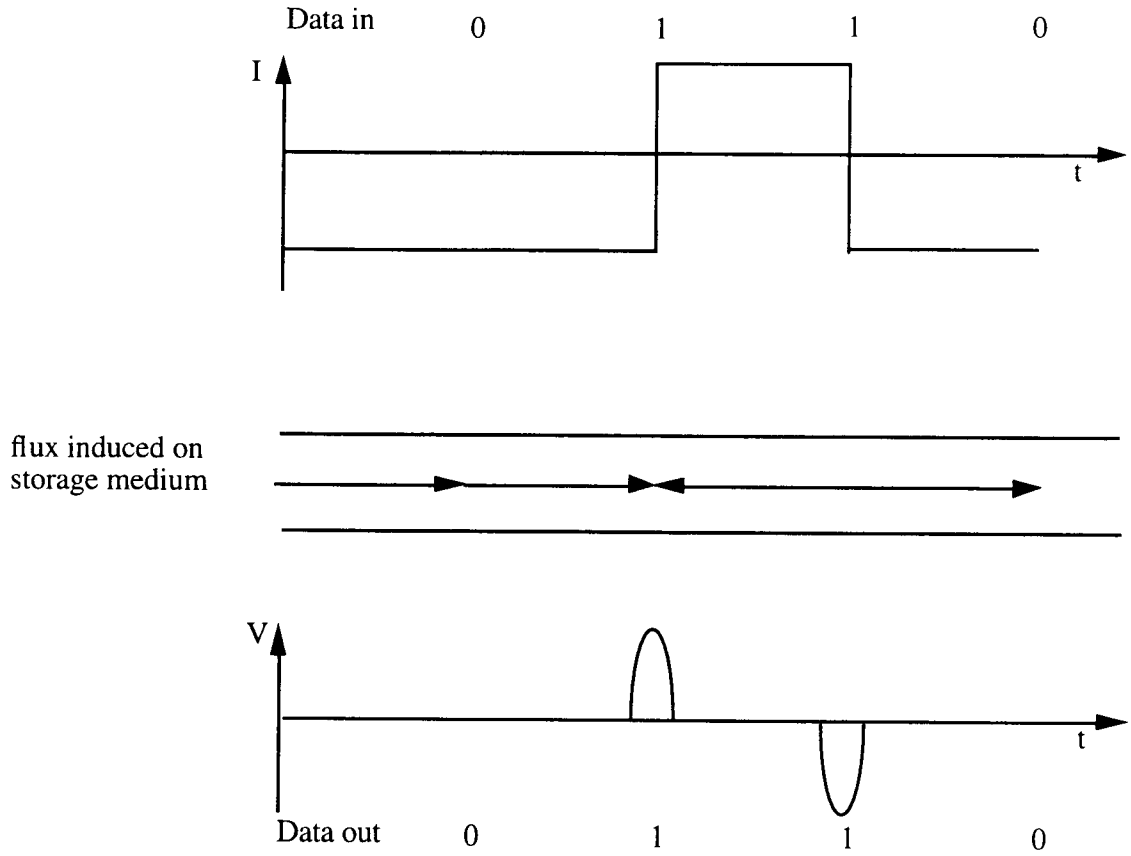


Figure 1.1 Fundamentals of write/read processes in saturation recording

called the precoder and ensures that the write current has no dc content before passing through the inductive write head.

During the read back process, the read head transforms the sequence of transitions to a stream of pulses of alternating polarity (Figure 1.1). The response of the read head to a transition or a step is modeled as a 'modified Lorentzian' defined as

$$s(t) = \frac{1}{1 + (\frac{2t}{PW50})^2} \tag{1.1}$$

where $PW50$ is the width of the step response at 50% amplitude level as shown in Figure 1.2. The value of $PW50$ is determined by the characteristics of the medium, the read/write heads, and the distance of the head to the medium. Hence the response of the

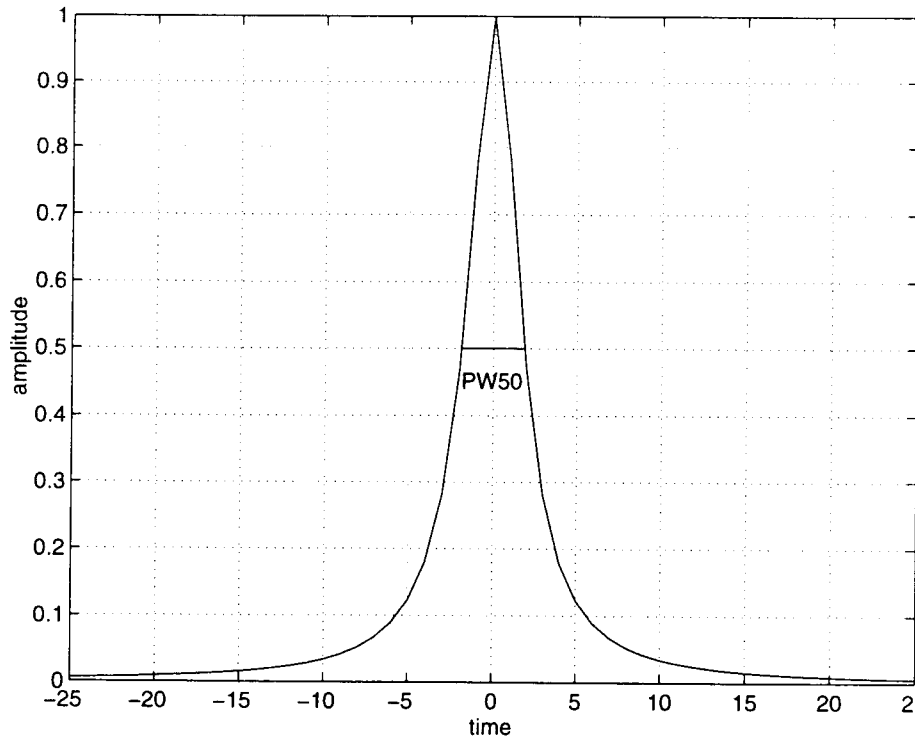


Figure 1.2 The Lorentzian impulse response

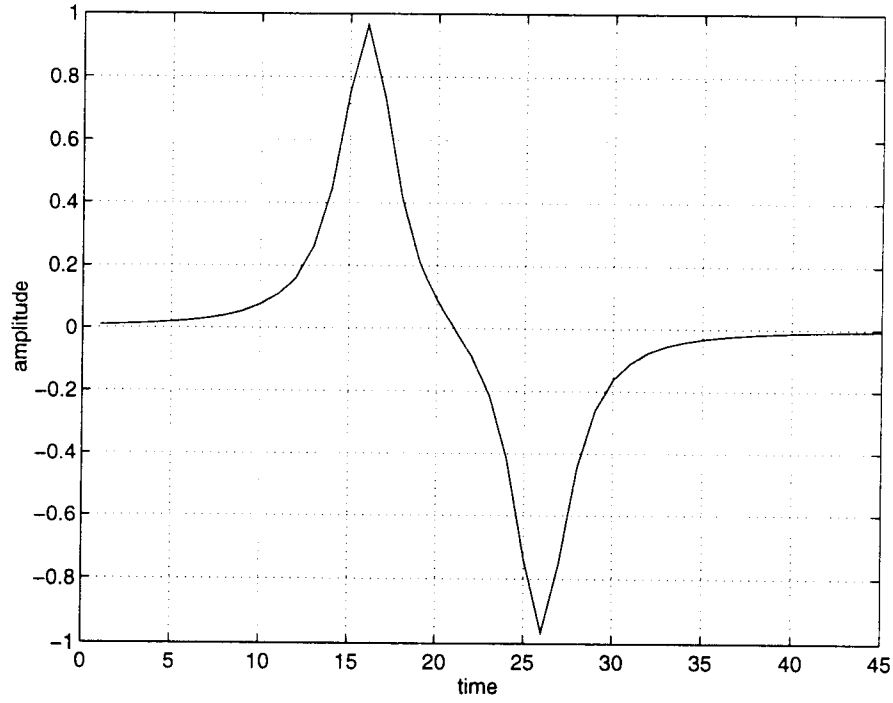


Figure 1.3 The dibit response

read head to a pulse (or two successive transitions) also called the 'dibit response' (Figure 1.3) is defined as

$$p(t,T) = s(t) - s(t-T) \tag{1.2}$$

where T is clock period. Equation 1.2 highlights the dependence of the read head pulse response on the clock period which is important in storage channels. This is because the dibit response indicates that an increase in storage density means decreasing T which in turn reduces the channel output signal energy per bit. The signal energy per bit E_b is given by:

$$E_b = \int_{-\infty}^{\infty} | p(t,T) |^2 dt \tag{1.3}$$

The general hierarchy in a storage channel is shown in Figure 1.4. The function of each component along with the principle it has borrowed from communications is discussed below:

The data encoder first interleaves or specifically rearranges the original data sequence and encodes it using the Reed Solomon error correcting code (ECC). The ECC adds redundancy to the data as a mechanism to locate and correct a small number of multi-byte errors per track with a high probability of success. As the ECC can correct only a small number of errors, interleaving the data before encoding improves its performance during a succession of errors.

The RLL (run length limit) coder [Siegel, 1985] is used to alleviate two problems that arise in storage channels. The first problem is intersymbol interference (ISI). ISI is the loss in the signal energy of a data symbol due to interference from its neighbors caused by reduced symbol spacing at high storage densities. The second problem is due to the fact that when dealing with digital data, precaution has to be taken to ensure sustained bit synchronization. Hence the RLL coder can be characterized by its parameters $R(d,k)$. 'd ' specifies the minimum number of 0's that can occur between two consecutive 1's thereby controlling the high frequency data content and reducing the effect of ISI.

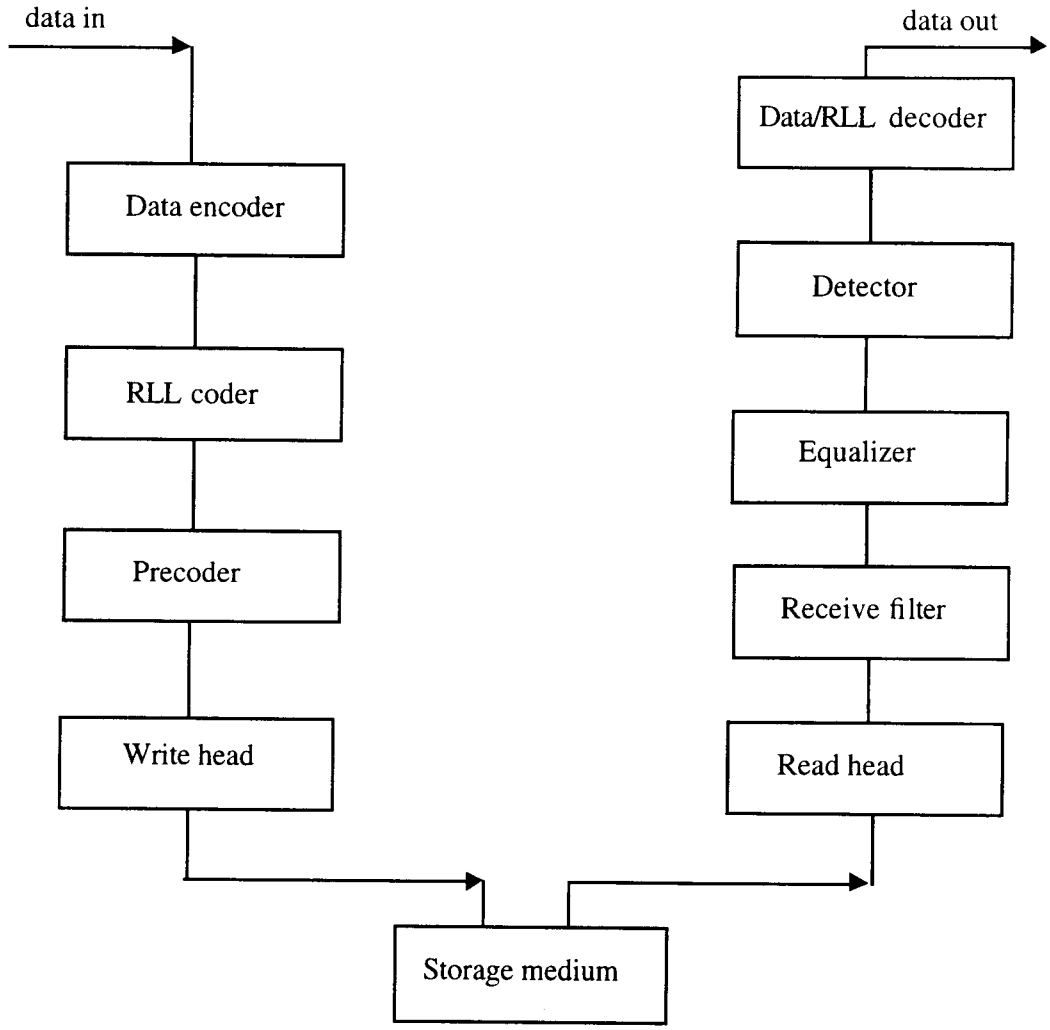


Figure 1.4 Hierarchy in a storage channel

'k ' specifies the maximum number of 0's that can occur between two consecutive 1's controlling the low frequency data content and ensuring that the clocking circuits do not lose synchronization with the incoming data. Thus the RLL code introduces significant redundancy which reduces the information content of the bits stored on the disk. The amount by which this reduction occurs is specified by the other parameter called the code rate R - the ratio of the input word length to the output word length. This parameter determines the increase in speed on the associated electronics for a given output data rate.

There are two prevalent RLL codes used in storage systems. The rate 8/9 code is used to cope with the data synchronization problem (k = 4) and has been specifically designed for a data recovery scheme referred to as partial response IV (PR IV) signaling used with the Viterbi algorithm [Cideciyan et al., 1992]. No constraint is imposed to tackle the ISI (d = 0), thereby the redundancy introduced by the RLL coder is minimized and the code rate is kept closer to unity. The 2/3(1,7) code is the other widely used RLL code in storage channels. The run length constraint of 1 provides a wide detection window for each symbol at high densities and has been exploited in MDFE to simplify high performance but complicated data recovery techniques as will be seen shortly. As the constraint of 7 on the 0's shows, the 2/3(1,7) RLL code also contributes to maintaining bit synchronization. The significant drawback of this code is its rate of 2/3, which means that the disk drive electronics have to operate 3/2 faster for a given output information rate.

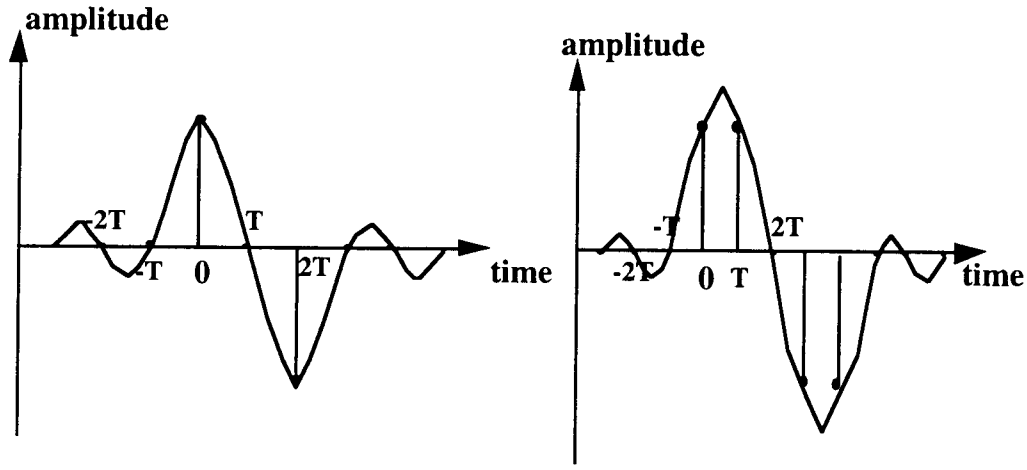
The components following the read head perform the signal processing for data recovery and hence are referred to as the 'read channel' of the disk drive, the first of which is the receive filter. The receive filter is a low pass filter which passes signal energy, and reduces channel noise at frequencies where there is no signal. The frequency response or the spectrum of the receive filter is matched to the spectrum of the incoming signal, ideally it has a flat magnitude and linear phase. This is the concept of the 'matched filter' in digital communication channels. Use of a matched filter maximizes the signal to noise ratio (*SNR*) of the signal at the input to the detector.

As it is difficult to achieve the ideal *SNR* of a matched filter using the practical receive filter alone, an equalizer shapes the time domain response of the output of the receive filter to a form that is suitable for the detector. Techniques to optimize the equalizer setting to a given environment have become imperative for disk drive channels. The optimization is done by making the equalizer coefficients programmable (during manufacturing) or adaptive. By doing so, channel variations due to different head and media, varying amounts of ISI from the inner to outer diameter of a hard disk, fluctuations

in the read head position, and data corruption due to noise from the electronic circuits are all compensated [Cioffi et al., 1990]. Simple adaptive algorithms are available [Qureshi, 1985] to update the equalizer coefficients.

The detector is the component which makes decisions for the digital data using the output of the equalizer. Maximum likelihood sequence detection (MLSD) is the optimum technique for detecting digital data ridden with noise and ISI [Forney, 1972]. The principle of MLSD is to make decisions after considering a sequence of data from the equalizer output thereby using more of the signal energy to perform reliable data detection. MLSD is often used with some form of partial response (PR) equalization preceding the equalizer.

PR signaling schemes shape the signal to match its spectrum to that of the storage channel at high densities. The general form of a PR polynomial is $(1-D)(1+D)^n$ where D is the delay operator and n is a non-negative integer [Thapar and Patel, 1987]. PR IV (n =1) and EPR IV (extended PR IV, n = 2) are the two commonly used PR techniques used with MLSD and they shape the main impulse with two and four terms of ISI respectively as shown in Figure 1.5. More terms of ISI or higher values for n are needed to



(a) PR 4 Signaling

(b) EPR 4 Signaling

Figure 1.5 Examples of PR signaling

approximate the storage channel spectrum at increased densities. As the complexity of MLSD increases exponentially with the number of terms of ISI, this type of a detection scheme becomes very impractical to implement in storage channels.

Another drawback of MLSD is that the Viterbi algorithm with which it is implemented results in decisions that are bursty and not available with every clock cycle. This lag in the decisions affects the performance of the timing and gain recovery control sections (not shown in Figure 1.4) of the read channel which function using decision-directed schemes. Hence an auxiliary multi-level threshold detector is used [Cideciyan et al., 1992] to perform symbol-by-symbol detection for the timing and gain recovery circuits. This detector is likely to make more decision errors than the MLSD detector. As an important digression, control circuits are vital in keeping signals within their optimum bounds. If not, there will be significant performance degradation and stability of the channel cannot be guaranteed.

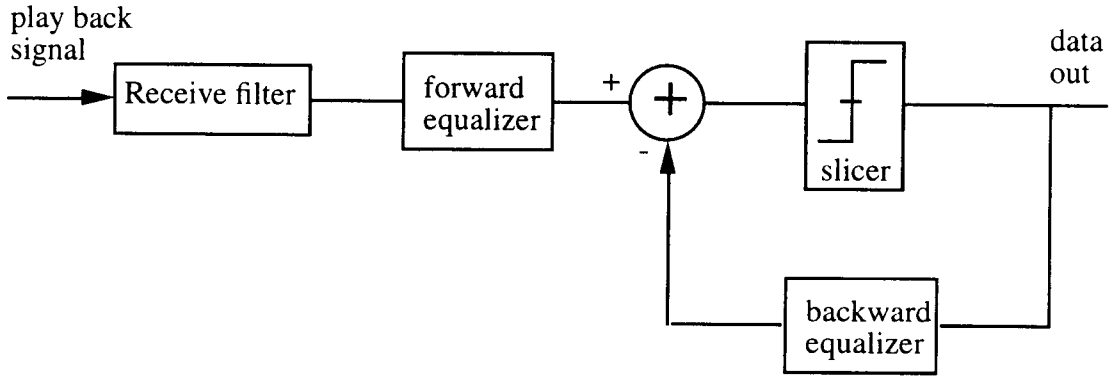


Figure 1.6 Block Diagram of decision feedback equalization

The concept of decision feedback equalization (DFE) used in communication channels to cancel ISI is an increasingly popular detector architecture for read channels due to its implementation simplicity and is shown in Figure 1.6. The forward equalizer cancels the ISI that occur due to future data symbols referred to as 'pre-cursor ISI'. Hence it shapes the time domain response into a causal form. The feedback equalizer cancels the

ISI due to the past data symbols referred to as 'post-cursor ISI'. The complexity of DFE increases linearly with ISI. A simple single threshold detector (also referred to as the slicer) following DFE works on a symbol-by-symbol basis. Symbol-by-symbol detection uses less signal energy to perform the detection when compared to MLSD but provides decisions with every clock cycle which can be used directly by the control sections.

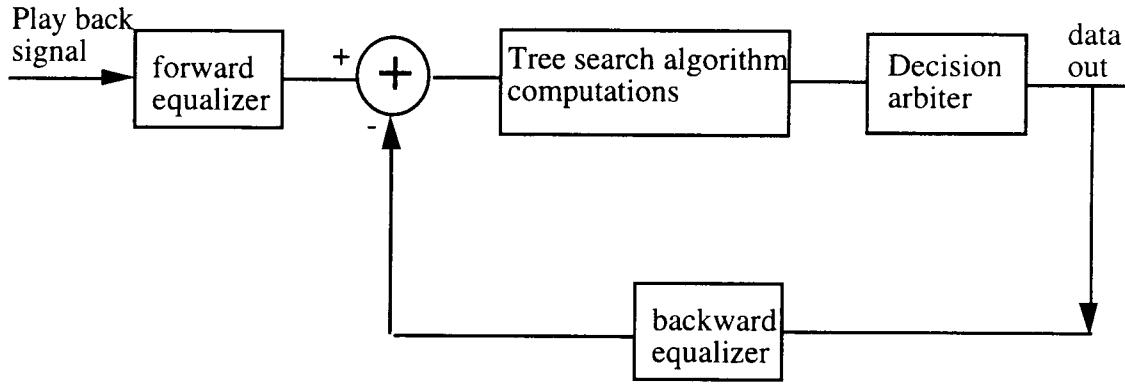


Figure 1.7 Block diagram of FDTS/DF

Fixed delay tree search with decision feedback (FDTS/DF) [Moon and Carley, 1990] is a detection technique for read channels that combines DFE with MLSD. By doing so, an architecture almost as simple as DFE with nearly the performance gains of MLSD is achieved. A block diagram of FDTS/DF is shown in Figure 1.7. As seen in Figure 1.7, arithmetic computations have to be completed within one clock cycle before the decision is fed back. As this is a severe implementation constraint at high operating speeds, the MDFE detector is derived from FDTS/DF when a run length constraint of 1 imposed on the input data symbols to minimize the computations in the feedback path. This results in an architecture identical to DFE [Kenney, 1991]. The performance gains of MDFE in terms of *SNR* is identical to FDTS/DF and has been demonstrated to be within 2 dB of the matched filter bound [Moon and Carley, 1990], [Carley and Kenney, 1991]. The matched filter bound (MFB) is the theoretical upper bound for the detector output *SNR* which corresponds to the performance level that can be obtained with optimum

detection when only one bit is stored in the channel. It can be easily computed as the output signal power when the effects of ISI and noise are eliminated (the undistorted output signal power).

1.2 Introduction to MDFE

A block diagram of the MDFE system is shown in Figure 1.8. The RLL coded data a_k is in terms of '+1' and '-1'. The differentiator block models the read head. The input data is convolved with the impulse responses shown in the Figure 1.8. *s(t)* is the Lorentzian impulse response introduced in section 1.1. The user *PW50* ranges from 2.0 to 3.0. Due to the 2/3 code rate this translates to a 3/2 increase in the *PW50* in Eqn. 1.1 for the Lorentzian response. Additive white Gaussian noise with variance σ^2_n is added at the read head . *g(t)* is the impulse response of a first-order all pass filter which is the forward equalizer. *f(t)* is the impulse response of the receive filter of Section 1.1. A fourth-order Butterworth filter is used to approximate a matched filter. The impulse response of the forward section *l(t)* can be written as

$$l(t) = f(t) * g(t) \tag{1.4}$$

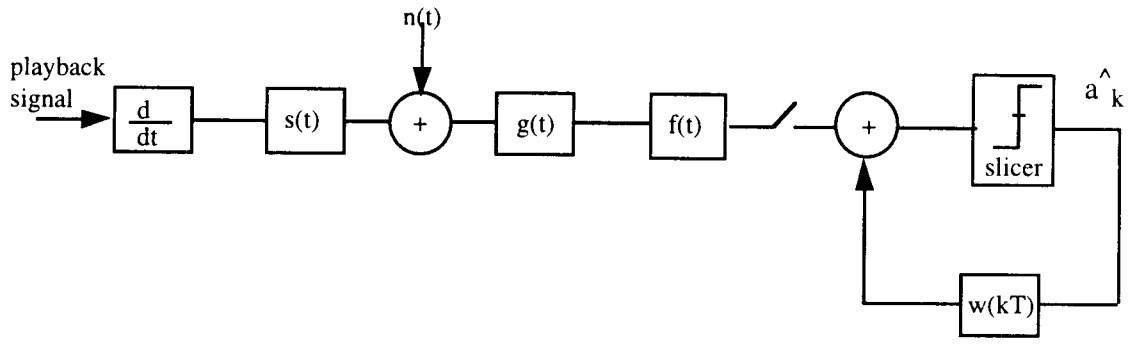


Figure 1.8 Block diagram of MDFE

where '*' is the convolution operator. The positioning of the poles and zeros of *f(t)* and *g(t)* is done off-line. Non-linear optimization techniques are used to place the poles and zeros such that the total noise power (ISI + noise) is minimized [Kenney and Wood, 1995]. This results in *f(t)* having a corner frequency at $0.3/T$ at a user *PW50* of 2.5. *l(t)*

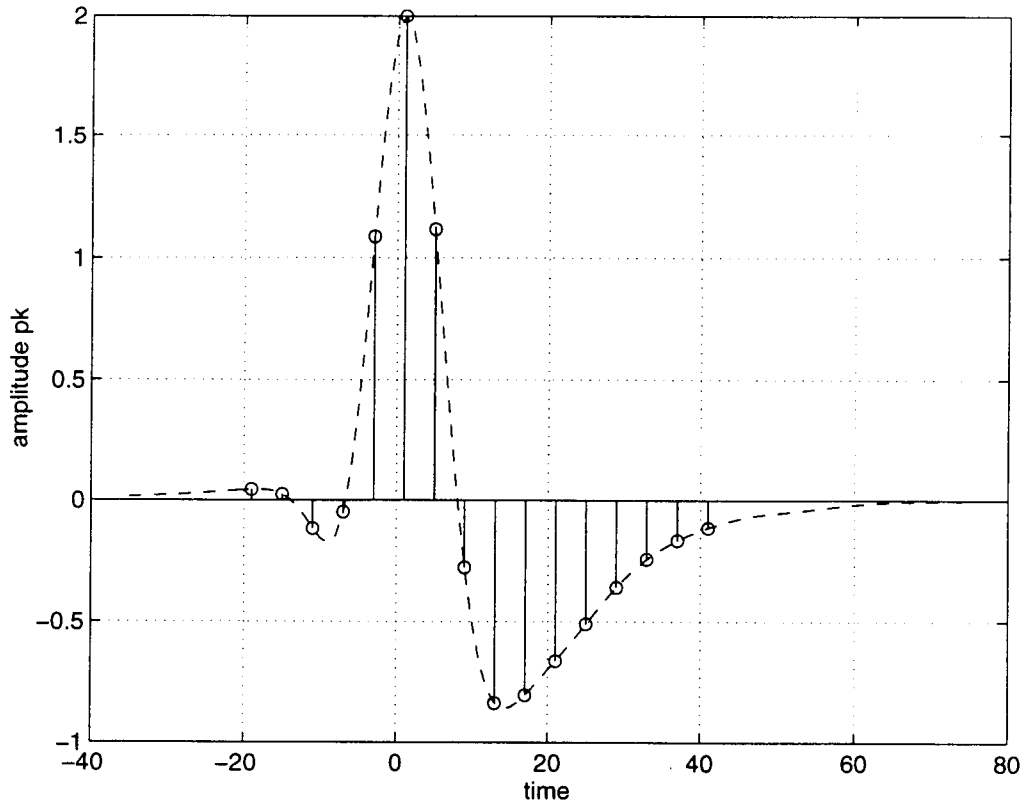


Figure 1.9 The equalized dibit

is referred to as the 'equalized dibit' shown in Figure 1.9. The impulse at discrete-time instant '1' corresponds to the current decision that has been normalized to a peak amplitude of 2.0. The time axis to the left of time '1' is for the pre-cursor ISI or the non-causal terms. The right side of time '1' is for the post-cursor ISI or causal terms.

The function of the forward equalizer is to minimize the pre-cursor ISI and concentrate the signal energy near the current decision of the equalized dibit. This is the reason for choosing an all pass filter for the forward equalizer. An all pass transfer function ensures that the forward path transfer function is minimum-phase. A minimum-phase transfer function has its poles and zeros within the unit circle. This results in a stable and causal system which has the property of minimum energy delay [Oppenheim and Schafer, 1989]. Minimum energy delay means the signal energy is concentrated near the main impulse (time '1') which is one of the motives behind forward path equalization.

The feedback equalizer functions in discrete-time with an impulse response $w(kT)$ (T is the sampling clock period). The coefficients or taps of $w(kT)$ are chosen as shown in equation 1.5 (also refer to Figure 1.9):

$$w_1 = p_2 - p_0$$
$$w_k = p_k; \qquad k \geq 2 \tag{1.5}$$

Hence the feedback equalization results in one term of ISI on either side of the main impulse (one causal, one non-causal) to appear at the input of the threshold detector or slicer. These two extra terms of ISI account for the improved performance of MDFE over regular DFE as they increase the detection signal energy. Hence the ideal slicer input can be written as

$$v_k = p_0(a_{k-1} + a_{k+1}) + a_k \tag{1.6}$$

where p_0 is the equalized dibit amplitude at time '0', a is the decision and its subscript denotes the time with respect to the current decision at time k. The Equation 1.6 is useful in reducing the MDFE system to the discrete-time representation shown in Figure 1.10 which clearly illustrates the equalization in MDFE. The operator D is a delay of one clock cycle and is equivalent to the Z-transform operator z^{-1}.

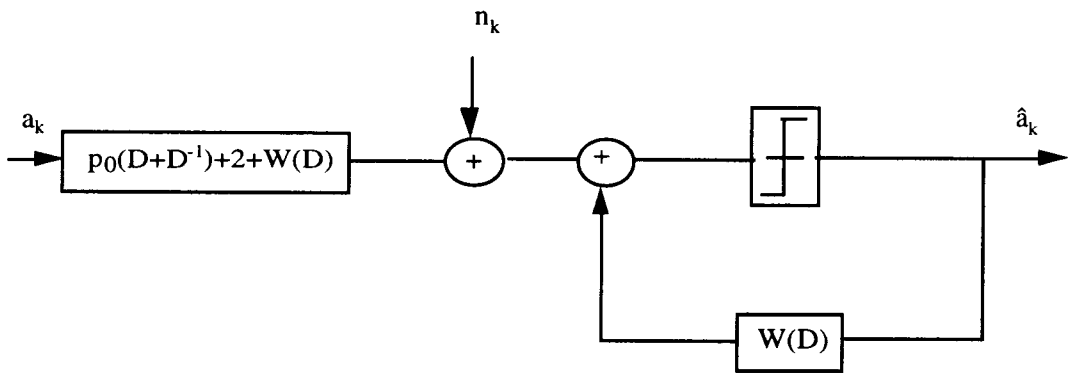


Figure 1.10 MDFE in the discrete domain

As a run length constraint of 1 is imposed on the incoming data, sequences such as (-1,+1,-1) with consecutive transitions are not permitted. Hence using Equation 1.6, the possible ideal values of the slicer input are listed in Table 1.1. This can be summarized as:

$$v_k \in \{-2p_0 - 2, -2, +2, +2p_0 + 2\} \tag{1.7}$$

Table 1.1 Ideal values of slicer input in MDFE

a_{k-1}	a_k	a_{k+1}	v_k
-1	-1	-1	$-2p_0+2$
-1	-1	+1	-2
-1	+1	-1	not allowed
-1	+1	+1	+2
+1	-1	-1	-2
+1	-1	+1	not allowed
+1	+1	-1	+2
+1	+1	+1	$2p_0+2$

Equation 1.7 indicates that the slicer or the threshold detector in MDFE can have a threshold at zero. Any value of $v_k < 0$ translates to a decision of '-1' and if $v_k > 0$, the decision is a '+1'. The two terms of ISI in v_k are hence used to provide excess amplitude or more signal energy to the slicer in making a decision.

1.3 The timing and gain recovery loops in MDFE

A block diagram for the timing recovery control section is shown in Figure 1.11 and the gain recovery section is shown in Figure 1.12. Both of these control sections estimate the timing/gain error using the decisions from the output of the slicer and the sampled slicer input such that the value of minimum mean-squared error (MMSE) is obtained. The reason for using decision-directed timing recovery schemes operating at symbol rate is that there is little high frequency signal power in storage channels at high densities. Hence timing recovery techniques which operate using higher harmonics of the average input frequency are not feasible in storage channels [Raghavan and Thapar, 1991].

The loop filter of the timing recovery control section has one pole (an ideal integrator) and a zero. The gain recovery loop filter is a first-order integrator. Both of the loop filters in the control sections smooth out the error estimates to provide a steady

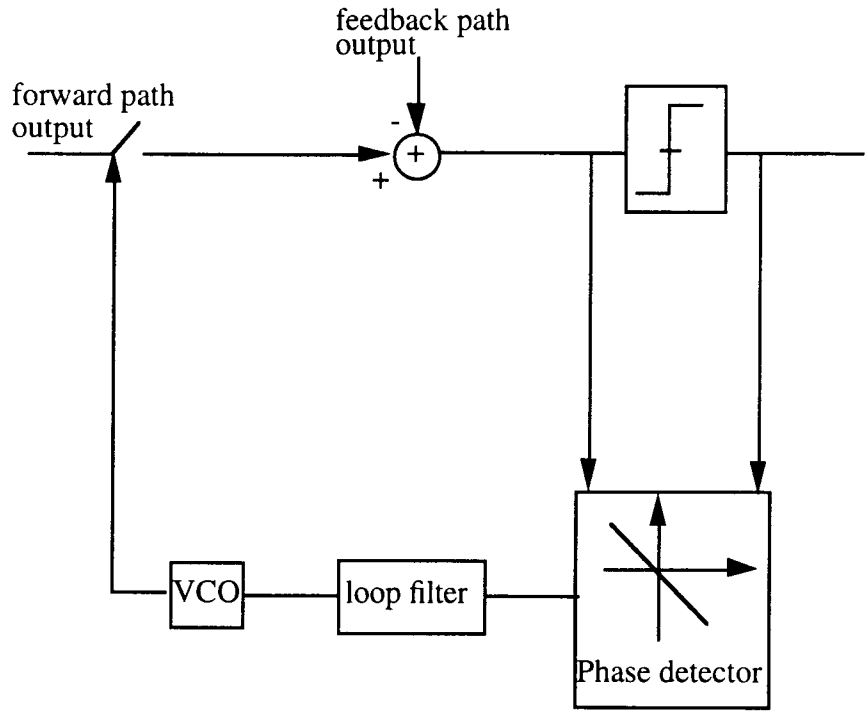


Figure 1.11 Block diagram of the timing recovery scheme in MDFE

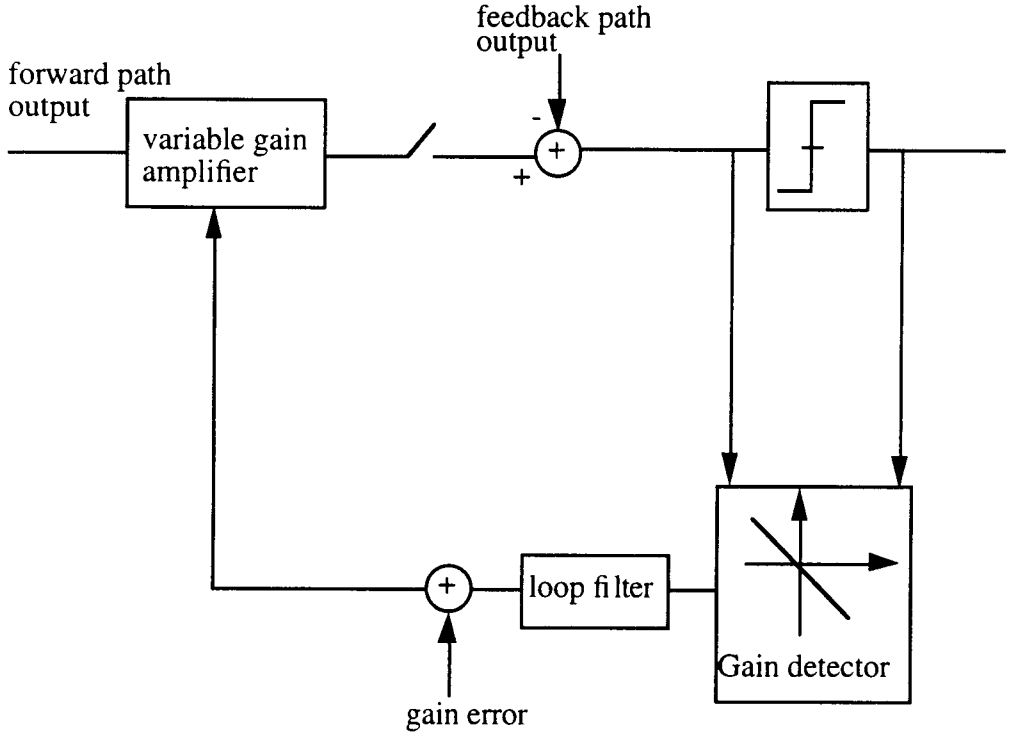


Figure 1.12 Block diagram of the gain recovery scheme in MDFE

control signal. The filter gain values and the location of the zero are chosen such that a compromise between fast convergence and reduced steady-state jitter is obtained. The voltage controlled oscillator (VCO) in the timing recovery circuit is the sampling clock generator. The VCO uses the loop filter output as a control signal to change the frequency and phase of the clock for the next sampling instant and is modeled as a first-order integrator.

1.4 Implementation issues in MDFE

The entire forward section is implemented in continuous-time using analog circuits. An analog implementation achieves a compact, low- power and high-speed front end. The filter design mentioned in Section 1.2 is done in discrete-time with an oversampling ratio of 4 to emulate continuous-time. The pole/zero location in the continuous-time domain is obtained through suitable mappings from the discrete-time domain [Oppenheim and Schafer, 1989].

The feedback equalizer is implemented in discrete-time as a finite impulse response (FIR) filter using a mix of analog and digital circuits. The number of taps used is 10 which is a value decided by simulations that check for its impact on channel error-rates. The digital sections of the feedback equalizer are used to facilitate its adaptation.

The design of the equalized dibit is done under the constraint that the first tap of the feedback filter w_1 (equation 1.4) is zero [Kenney and Melas, 1996]. Hence the feedback filter has 9 non-zero taps. As the first tap has been set to zero, an extra clock cycle is available before the decisions are fed into the feedback equalizer. This free clock cycle has been utilized to split the feedback section into two parallel detector sections (Figure 1.13) that operate at half the original speed. Hence the factor of 3/2 introduced by the RLL code is reduced to 1/2(3/2) = 3/4. In regular DFE architectures, in order to perform this ping-pong feedback detection, look-ahead operations have to be used to pre-calculate decisions [Bednarz et al. 1994]. These operations have to be performed within one clock cycle which is a strain on the circuits. This has been successfully avoided in MDFE.

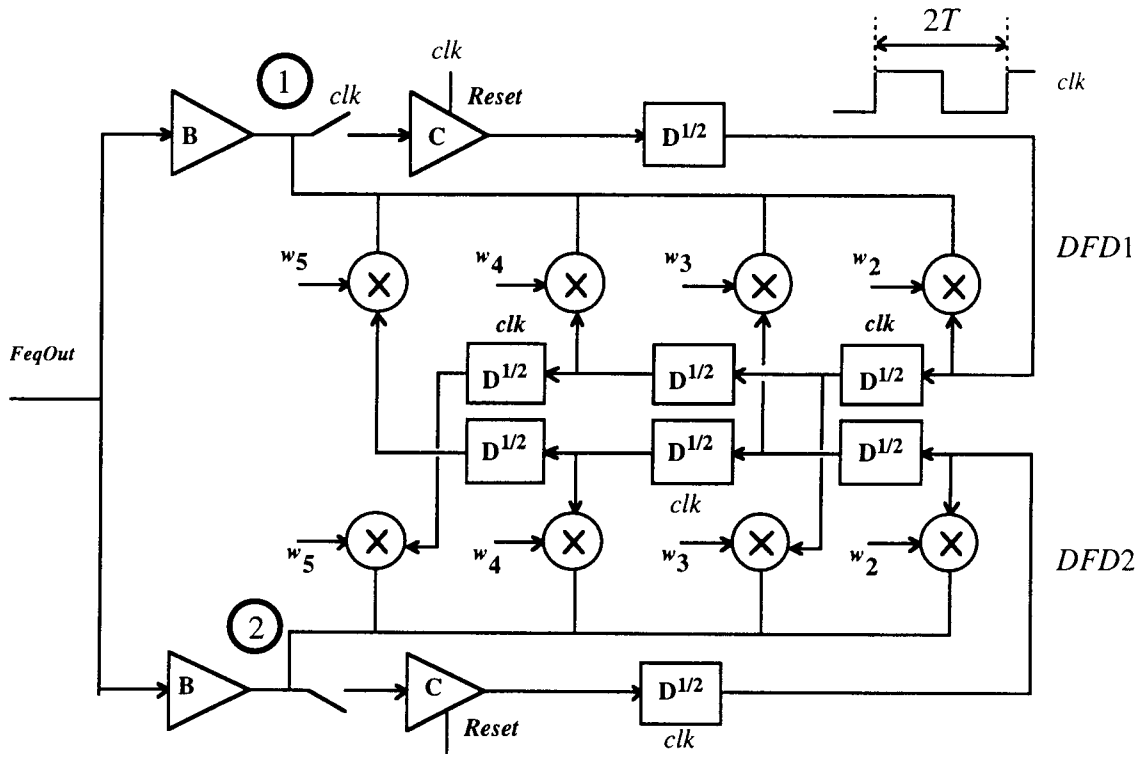


Figure 1.13 The ping-pong feedback equalizer in MDFE

Another advantage from performing continuous-time equalization in the forward path is that the sampling is done before the slicer. Hence group delays amounting to a finite number of clock cycles caused by a discrete-time front end filter have been avoided. Thereby, the data symbols take less time to propagate to the slicer input and do not cause the undesirable lag associated with a discrete-time filter. This is a significant advantage to the the decision-directed timing and gain recovery control sections.

The equalized signal following the sampler entering the slicer is converted to a digital value using a flash analog to digital converter (ADC). The purpose of analog to digital conversion of the steady-state equalized signal is two fold: (i) to perform the fundamental fuction of the read channel in making decisions on the play-back signal and (ii) to encode the output of the flash ADC using a finite number of bits to represent the error, which is the deviation of the slicer input from its ideal value. The feedback loops in

MDFE use this digital error signal to perform updates that adapt to channel variations, and hence are referred to as adaptive loops. The timing and gain recovery control sections and the loop to update the feedback equalizer's coefficients are the three adaptive loops in MDFE.

A digital control error signal makes the phase and gain detector block (introduced in Figures 1.11 and 1.12) fully digital. A digital phase/gain detector simplifies the circuit implementation of the timing and gain recovery circuits and offers greater precision in their performance. In addition to this, as will be introduced in Chapter 3, the timing and gain updates require information spread over two clock cycles. Hence storage of information in the circuit is also made easier by using a digital control input signal.

1.5 An outline of this thesis

The objective of this thesis is to present an optimum method to perform the A/D conversion of the equalized signal. A scheme for performing quantization on the steady-state equalized signal is presented in Chapter 2. The relavent issues this quantization scheme should be capable of withstanding are: is it a valid scheme during the transient states of the adaptive loops? Under what conditions will the channel be able to recover from start up phase offsets, frequency offsets and gain errors and achieve lock into steady-state? During steady-state, the adaptive loops are noisy by nature as they track the channel variations in an iterative manner. Hence if quantization is introduced in the system, how much noise will it add to the existing steady-state jitter? Chapter 3 addresses these issues after characterizing the adaptive algorithms for timing error detection, gain error detection, and adaptive equalization of feedback equalizer which includes dc offset detection.

CHAPTER 2

QUANTIZATION SCHEME FOR THE STEADY-STATE EQUALIZED SIGNAL

2.1 Defining the density function of the signal to be quantized

As introduced in Chapter 1, MDFE ideally has four possible equalized levels at the input to the slicer. At high densities, (2.5 user *PW50*), the outer levels are 100% larger in amplitude or 6 dB greater in energy than the inner levels and due to the run length constraint of 1 they occur only about one third of the time. Both of these features render the outer levels more robust to timing, gain and adaptation errors. Hence these errors are computed and used only on the inner levels and are set to zero otherwise as will be elaborated in Chapter 3. Therefore, in quantizing the input to the slicer, attention is paid only to the inner levels in MDFE.

Figure 2.1 shows a histogram of 1000 data points to illustrate the four equalized levels in MDFE. The equalized dibit has been normalized to a peak value of 2.0 and for a user *PW50* of 2.5, the tap $p_0 \equiv 1$. Hence the four main impulses or levels shown in the histogram are at -4, -2, +2, +4. These levels are centered around the channel noise. Additive white Gaussian noise is added after the read head with variance σ^2_n. The value of σ^2_n is derived from the input *SNR* defined as

$$SNR = 10\log_{10}\left[\sum_k \frac{h_k^{\,2}}{\sigma_n^{\,2}}\right] dB \qquad (2.1)$$

where h_k is the equalized dibit sampled at the best phase (as was illustrated in the equalized dibit in Figure 1.9 of Chapter 1). The white noise gets colored by the channel as it is filtered through the forward path. Figure 2.2 shows this colored Gaussian noise around an inner level with the mean value (+2 or -2) removed at an user *PW50* of 2.5 and input *SNR* of 20 dB. This is defined as the random variable X to be quantized with variance σ^2_x whose steady-state pdf is Gaussian defined as:

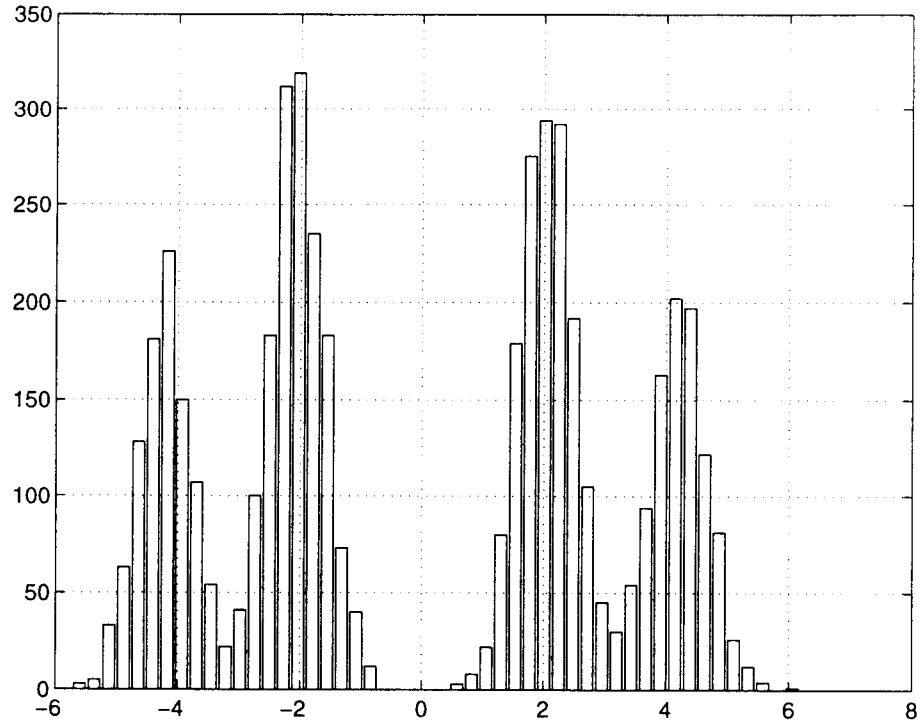


Figure 2.1 Histogram showing the equalized levels in MDFE

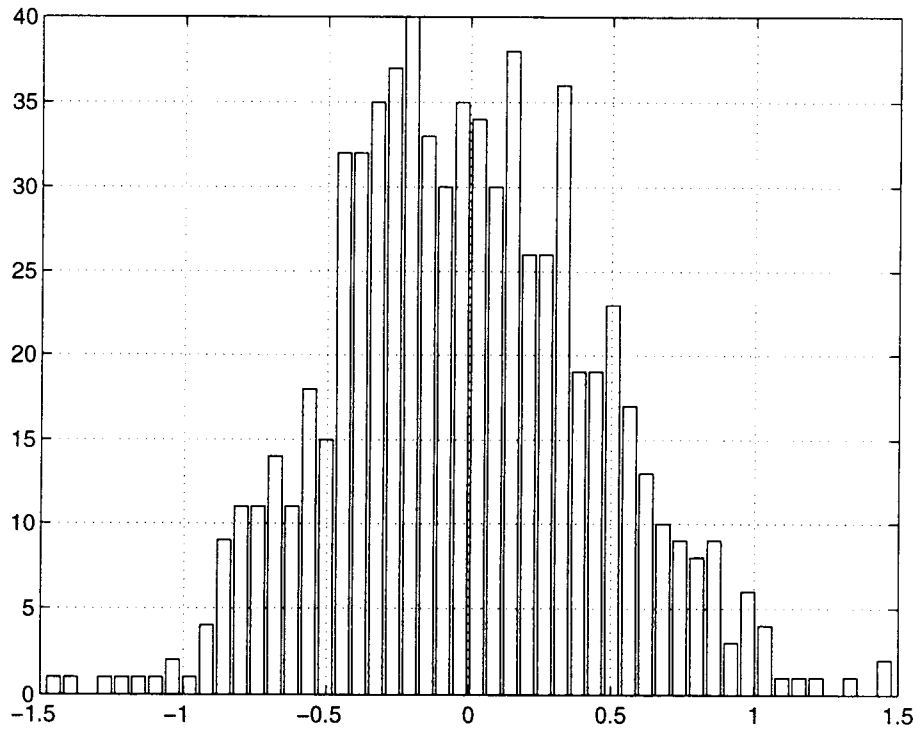


Figure 2.2 The random variable X to be quantized

$$p_x(x) = \frac{1}{\sigma_x \sqrt{2\pi}} e^{-x^2/2\sigma_x^2} \tag{2.2}$$

The standard deviation of X for the defined channel conditions was measured using Matlab and was found to be 0.46. After quantization, the corresponding inner level value (or the mean) is added to the quantized signal.

2.2 Quantizer design

Figure 2.3 shows the four different quantizer transfer characteristics. Figures 2.3a and 2.3b are both uniform quantizers. The transfer characteristic of a uniform quantizer is defined by a constant step size Δ which is the spacing between each of its input or output thresholds. Figures 2.3c and 2.3d are non-uniform quantizers. The non-uniform quantizer has a variable step size that has been optimized to obtain the best possible dynamic range for a given number of thresholds. A uniform quantizer is simple to implement using circuits as the step sizes defining the quantizer transfer characteristic determine the values of the resistors which provide the voltage reference to the comparators in the flash ADC. Thus if the step size is a constant, the resistor values are scaled by integer factors unlike in non-uniform quantization thereby simplifying an implementation issue.

Figure 2.3 illustrates one other classification of the quantizer transfer characteristic based on the values of the output threshold. If a quantizer has an output threshold at the origin, as in Figures 2.3b and 2.3d, it is referred to as a 'mid-tread' quantizer. In the absence of an output threshold at the origin as in Figures 2.3a and 2.3c, the quantizer is referred to as the 'mid-rise' quantizer. The mid-tread quantizer is characterized by an odd number of output thresholds symmetric about a threshold at the origin, which in MDFE ensures errors of both polarities are handled symmetrically. The mid-rise quantizer has an even number of output thresholds none of which are placed at the origin.

The application in MDFE requires the flash ADC to be a mid-tread quantizer. By using a mid-tread quantizer, and the signal values corresponding to the quantizer input interval near the origin are encoded to zero. This zero error value is not to be interpreted as

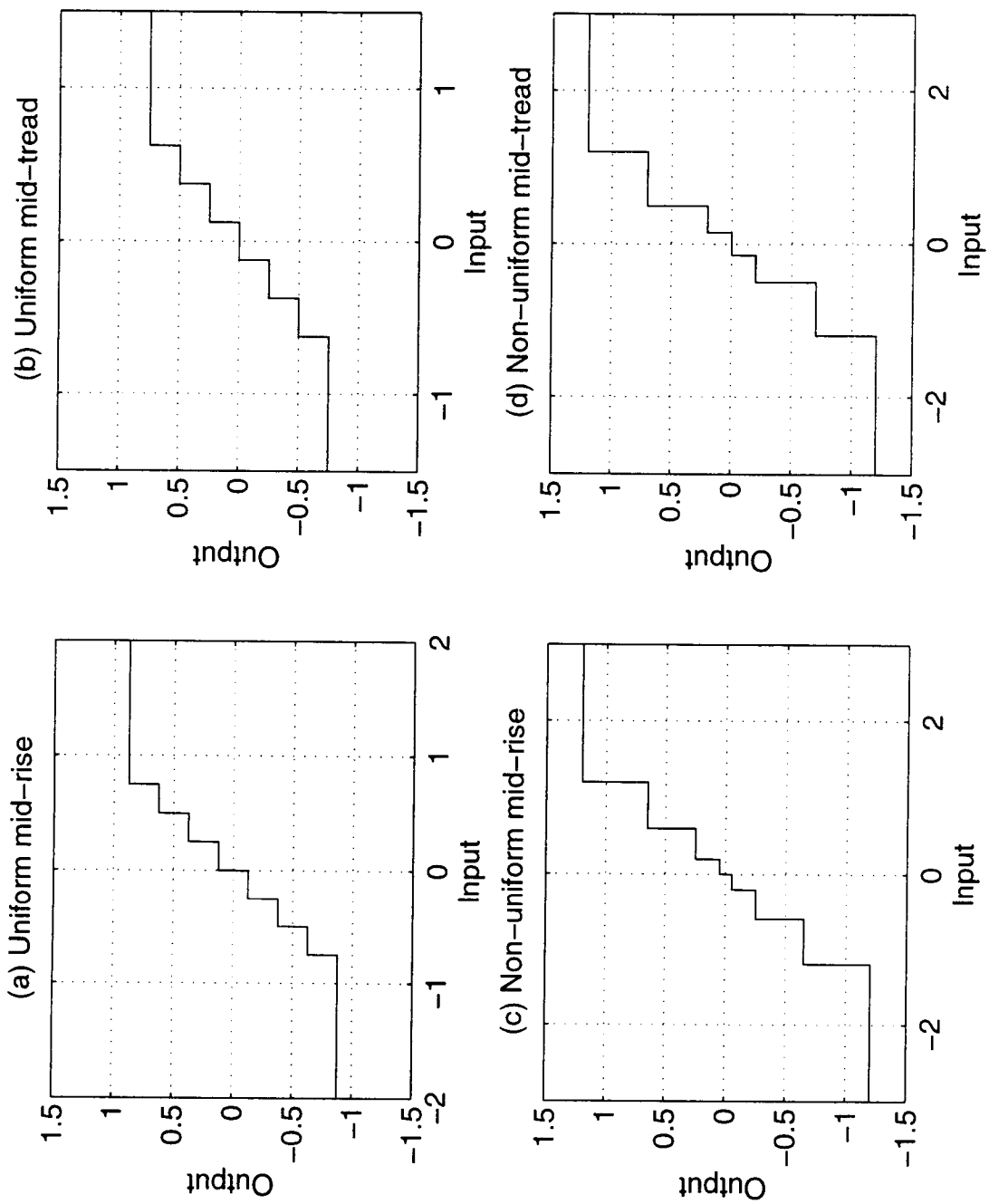


Figure 2.3 Quantizer transfer characteristics

the actual channel error determined by the output signals from the adaptive loops. As will be elaborated in the next Chapter, the adaptive loops function in a stochastic or iterative environment and this ideal state of zero error is approximated by an average over time. By placing an output threshold corresponding to zero error in the flash ADC, the channel error has been sliced to zero ignoring the existing jitter in that input interval. If a mid-tread quantizer were instead used, the channel error is always a quantized non-zero value which increases jitter from the adaptive loops and degrades the steady-state channel performance.

A quantizer $Q(x)$ maps a stationary random variable X with a variance σ_x^2, and pdf $p_x(x)$, in a given interval I_k to $Q(x) = y_k$. The quantization error is given by x-$Q(x)$ and has the same pdf as X. If the quantizer has L input intervals, the quantizer error variance [Jayant and Noll, 1984] is given by:

$$\sigma_q^2 = \sum_{k=1}^{L} \int_{x_k}^{x_{k+1}} (x - y_k)^2 p_x(x) dx \tag{2.3}$$

The error variance is also referred to as the average distortion or the mean-squared error and is a popular performance measure for quantizers due to its simplicity and analytical tractability. The uniform and the non-uniform quantizers are designed to minimize this quantizer error variance by optimizing the threshold placement based on the input pdf to be quantized.

2.2.1 The pdf-optimized uniform quantizer

The input thresholds x_k and output thresholds y_k of an uniform quantizer are defined as

$$\begin{aligned} x_k &= \left[k - \frac{L+2}{2}\right]\Delta; \qquad && k = 1,2,3,\ldots,L \\ y_k &= \left[k - \frac{L-1}{2}\right]\Delta; \qquad && k = 2,3,4,\ldots,L \end{aligned} \tag{2.4}$$

Equation 2.3 for the quantizer error variance can be expanded for all L intervals and the limits of the integral can be expressed in terms of Δ using Equation 2.4. As an explicit

solution for the optimum step size Δ_{opt} cannot be obtained, numerical techniques are used to find Δ_{opt} that minimizes σ^2_x. The Δ_{opt} for different number of mid-tread quantizer thresholds is shown in Table A.1 [Proakis and Salehi, 1994] of Appendix A. These values are for a Gaussian source of unit variance, hence the step sizes are scaled by the standard deviation of the input σ_x to be used in the flash ADC.

2.2.2 The pdf-optimized non-uniform quantizer

As the pdf of X is known, it can be used to calculate the probabilities of occurrence of X. Smaller decision intervals are placed where the probability of X is high, and larger decision intervals otherwise. This scheme minimizes the quantization error variance and obtains the best possible dynamic range for a given number of thresholds. The conditions for defining optimal input and output thresholds using the input pdf are explained below and such an optimal quantizer is also referred to as the Lloyd-Max or the non-uniform quantizer.

2.2.2.1 *Minimizing σ^2_q with respect to input intervals x_k*

Any value of X that minimizes the mean-squared error $E[(x - y_k)^2]$ in a given interval I_k is given by $E[y_k]$ where $E[.]$ is the expected value of [.]. If $E[y_k] = \overline{y}$, this can be justified as

$$\begin{aligned} E[(x-y_k)^2] &= E[(x-\bar{y}+\bar{y}-y_k)^2] \\ &= E[(x-\bar{y})^2] + (y_k-\bar{y})^2 \\ &>= E[(x-\bar{y})^2] \end{aligned} \qquad (2.5)$$

as both X and Y are zero mean random variables and using the fact that y_k is a constant for a given input interval. Hence Equation 2.5 demonstrates that minimum variance is obtained when X = the mean of Y in any given interval. This is the first necessary condition for MMSE referred to as the 'nearest neighbor condition' and can be stated as:

$$x_{1,opt} = -\infty;\ x_{L+1,opt} = \infty;\quad x_{k,opt} = \frac{y_{k-1,opt} + y_{k,opt}}{2};\qquad k = 2,3,...,L \qquad (2.6)$$

2.2.2.2 *Minimizing σ_q^2 with respect to output intervals y_k*

For a given interval I_k, σ_q^2 can be written as shown in equation 2.7 where $p_x(x / x \in I_k)$ is the conditional pdf of X occurring in interval I_k. As shown in the nearest neighbor condition, the value of y_k that minimizes this integral is the mean of the conditional pdf $p_x(x / x \in I_k)$ also referred to as the conditional mean or the 'centroid'. Hence,

$$\begin{aligned}\sigma_q^2 / x \in I_k &= \int_{x_{k,opt}}^{x_{k+1,opt}} (x - y_{k,opt})^2 p_x(x)dx \\ &= P_x(x \in I_k) \int_{-\infty}^{\infty} (x - y_k)^2 p_x(x / x \in I_k)dx \\ &= P_x(x \in I_k) E[(x - y_k)^2 / x \in I_k]\end{aligned} \tag{2.7}$$

Thus, using Bayes rule for conditional probabilities, the centroid or second necessary condition for MMSE is stated as:

$$\begin{aligned}y_k &= \int_{x_{k,opt}}^{x_{k+1,opt}} x p_x(x / x \in I_k)dx \\ &= \frac{\int_{x_{k,opt}}^{x_{k+1,opt}} x p_x(x)dx}{\int_{x_{k,opt}}^{x_{k+1,opt}} p_x(x)dx}; k = 1,2...L\end{aligned} \tag{2.8}$$

Table 2.1 - The Lloyd II algorithm

Step I	Pick an initial value for input thresholds $\{x_k,\ k = 2,3,...L\}$; $x_1 = -\infty$
Step II	Find the output thresholds y_k = centroid(x_{k-1}, x_k), $k = 2,3,...L$
Step III	Find x_k = mean(y_k, y_{k+1}), $k = 2,3,...L$
Step IV	Compute c = centroid(x_L, ∞). If $\lvert y_L - c \rvert < \varepsilon$, stop else goto step V
Step V	Let $y_L = y_L - \alpha (y_L - c)$. Goto step II

* ε and α are design parameters which determine algorithm convergence

The Lloyd II iterative algorithm [Gersho and Gray, 1992] gives a non-explicit solution for the Lloyd-Max quantizers based on these two conditions for optimality. The algorithm is listed in Table 2.1. The results of the algorithm (Table A.2) along with the Matlab code are listed in Appendix A.

2.3 Quantizer design results in MDFE

Figure 2.4 performs a comparison between the uniform and non-uniform quantizer error distortions [Proakis and Salehi, 1994]. The less uniform the shape of the input pdf is, the greater is the performance gain of a non-uniform quantizer compared to its uniform counterpart [Jayant and Noll, 1984]. As seen in Figure 2.4, for a Gaussian pdf, the non-uniform quantizer shows only about a 1.5 dB gain over the uniform quantizer for the maximum number of thresholds shown.

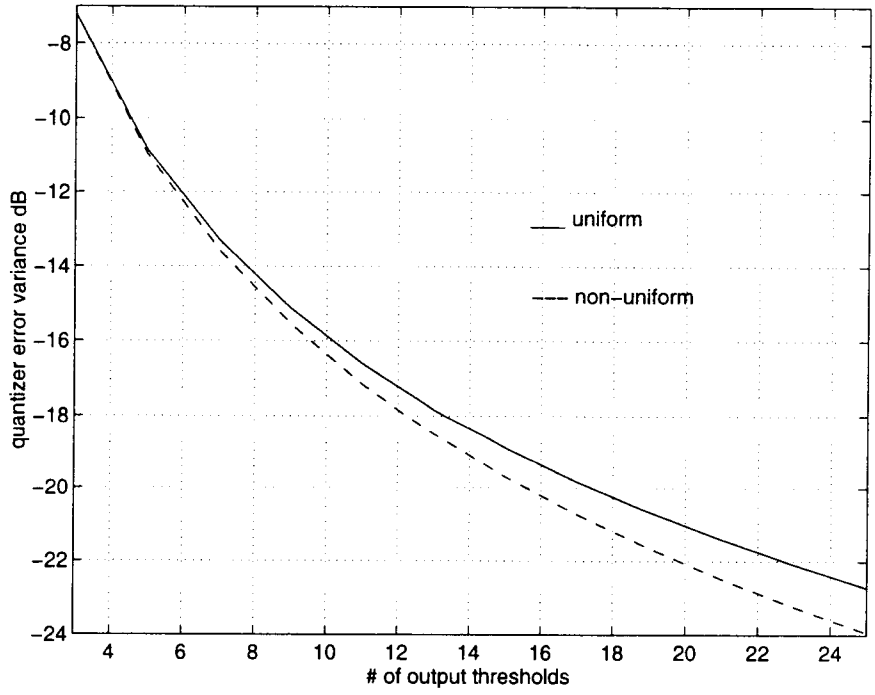


Figure 2.4 Distortion comparison between uniform and non-uniform quantizers

Steady-state conditions in MDFE are robust to quantizer distortion as the application focuses on retrieving the equalized impulses (the mean of X) and not perfect

reconstruction of the input signal X. Hence it is sufficient to proceed with the uniform quantization scheme. During the channel transients, the timing and gain recovery loops work to recover phase offsets, frequency offsets and gain errors and hence the stationarity assumption of the steady-state Gaussian introduced Figure 2.2 is questionable. The number of thresholds for the quantization scheme is thus dictated by the timing and gain recovery loop transients.

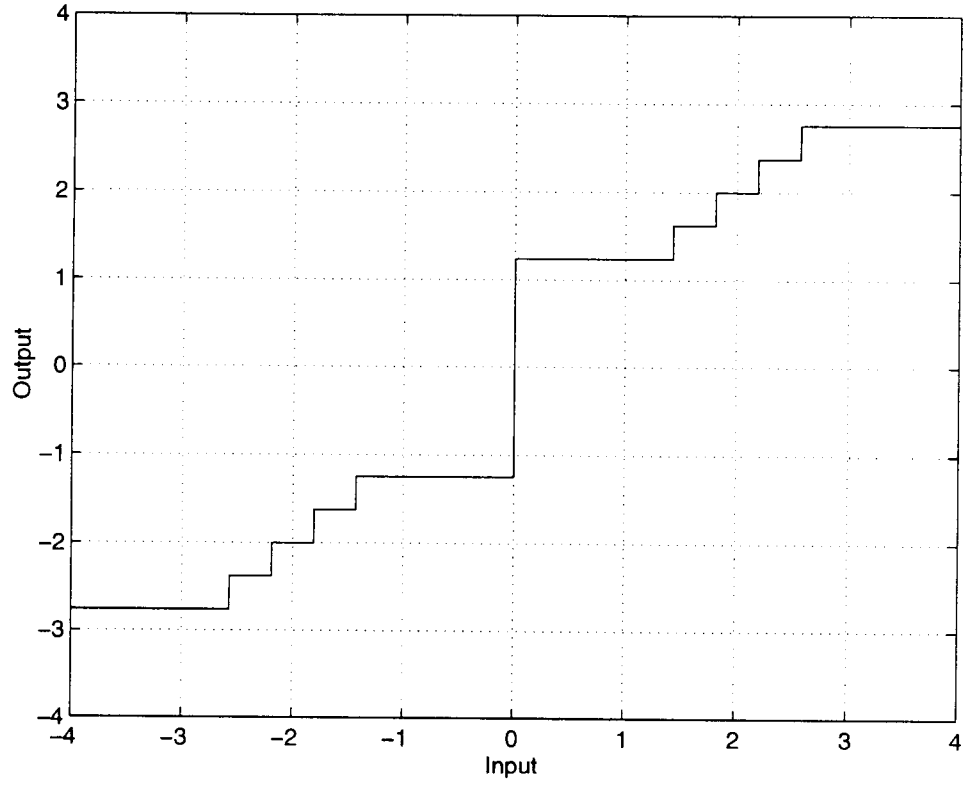


Figure 2.5 Transfer characteristic of flash ADC

In applying the quantizer design results to MDFE, the fact that the Gaussian distribution is symmetric can be used to bound the input between (0, ∞). If L output levels are used in performing the quantization, these levels can be mirrored into $2L-1$ levels for an input between (-∞,∞). For example, if a value of $L=3$ is chosen as in Figure 2.5, this is translated to each inner level having five output thresholds in the flash ADC one of which includes the quantizer mean. As the two inner levels are symmetric about the origin

as introduced in the histogram of Figure 2.1, the same transfer characteristic is replicated for the inner level on the other side of the origin. The transfer characteristic shown in Figure 2.5 is the proposed quantization scheme for the flash ADC. Results from simulations are used to analyze the performance of the adaptive loops with this simple to implement quantization scheme during channel transients and steady-state and are presented in the next chapter.

CHAPTER 3 - THE ADAPTIVE LOOPS IN MDFE

3.1 Introduction

The purpose of this chapter is to (i) characterize the algorithms for timing recovery, gain recovery and adaptive equalization of the feedback equalizer (which includes dc offset detection) and study the impact of the flash ADC on their characterization; (ii) analyze the loop transients with this steady-state quantization scheme; (iii) specify the conditions under which the channel can recover from transient errors and lock into steady-state; (iv) verify the steady-state channel performance with the adaptive loops and the flash ADC. All simulations have been done assuming a channel *SNR* of 20 dB (with the exception of channel error-rate Vs *SNR* curves) and a user *PW50* of 2.5. The parameter L is used to refer to the resolution of the flash ADC, where L denotes the number of output thresholds for each inner level. The scheme proposed for MDFE has a resolution of $L = 5$.

3.2 Timing recovery

The sampling in MDFE is performed at the data-rate. Baud-rate or data-rate sampling is possible as the spectrum of the Lorentzian impulse response has very little energy beyond the Nyquist frequency. The RLL constraint of 1 in MDFE further helps in band-limiting the high frequency content of the data and thus aliasing is not an issue of concern despite data-rate sampling. This facilitates the use of decision-directed timing recovery techniques operating at the data rate which use a scheme for timing error detection with minimal increase in circuit complexity. Decision-directed methods are inductive in nature as they estimate the timing error using the available sampled equalized signal and the decisions, and process this error in a feedback loop to perform an update for the next sampling instant.

3.2.1 Phase Detection

An example of a phase error is shown in Figure 3.1 where e_k is the error at time k due to the timing phase offset ϕ. A general method to obtain near minimum variance

estimates of the timing offset with respect to a steady-state sampling criterion using the data has been outlined [Mueller and Muller, 1976]. The most important properties of such a timing function are monotonicity, zero crossing at a good timing phase and odd symmetry about the zero crossing to ensure that offsets of both polarities are handled symmetrically. Relevant forms of this solution to timing recovery have been applied to DFE [Abbot and Cioffi, 1990] and PRML [Cideciyan et al., 1994] detection schemes.

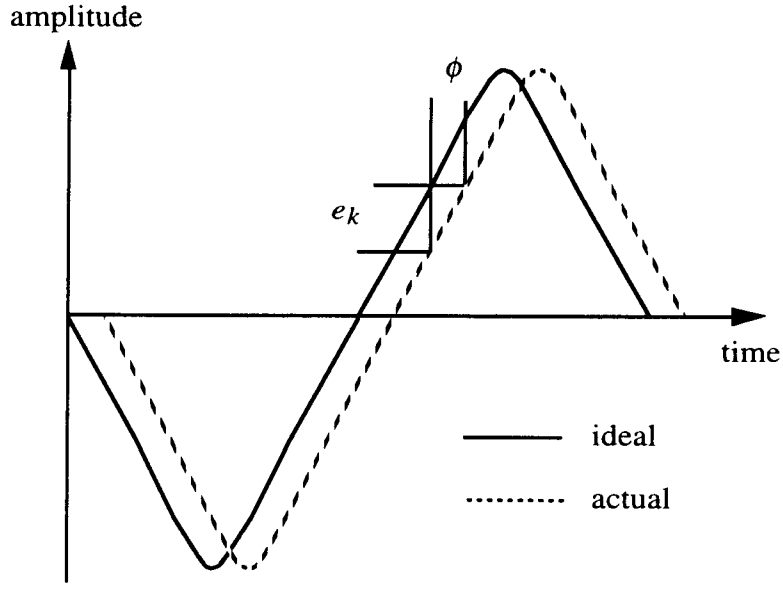


Figure 3.1 Example of a phase error

The suitable choice of timing function in MDFE is a simplified version of the solution to the mean-squared error criterion given by the stochastic gradient algorithm [Lee and Messerschmitt, 1994]. This timing recovery technique selects a sampling phase for MMSE hence called MMSE or least mean-squared (LMS) timing recovery. If τ is the phase offset, the error e_k (ideal slicer input minus the actual value) is given by:

$$e_k = \hat{v}_k - v(kT + \tau) \tag{3.1}$$

The mean-squared error gradient is given by:

$$\nabla_{\tau_k} = \frac{\partial}{\partial \tau}\left[E(e_k^2)\right]$$

$$= -2E\left\{e_k \frac{\partial}{\partial \tau}[v(kT+\tau)]\right\} \tag{3.2}$$

as $\hat{v}_k$ is independent of timing errors. The stochastic gradient is obtained by using the value of the gradient at that timing instant instead of performing an average. A technique to compute the slope by filtering the discrete-time samples using an FIR filter has been outlined [Qureshi, 1976]. A simplification in implementing the stochastic gradient is to use the sign of the slope rather than its actual value. Thus, the approximated phase error gradient is given by:

$$\nabla_{\tau_k} = -e_k sign\left\{\frac{\partial}{\partial \tau}[v(kT+\tau)]\right\} \tag{3.3}$$

In MDFE, the timing update is performed only during the zero crossings [Kenney and Wood, 1995]. A zero crossing is detected by checking if $a_k \neq a_{k-1}$ and the respective slicer input signals v_k and v_{k-1} correspond to the inner levels. The slope of the phase error is positive when a_k = +1 and a_{k-1} = -1 and likewise negative when a_k = -1 and a_{k-1} = +1. Hence the sign of the phase error slope is given by the decision a_k. In the absence of a zero crossing, the signal v_k has 6 dB more energy corresponding to an outer level. Due to this excess energy, the slope of the phase error is approximated to zero during the outer levels. It should be noted that this gradient scheme for timing error detection is specific to the run length constraint of 1 in MDFE and cannot be applied to DFE detection schemes where a constraint of 0 is employed and can be summarized as:

if $a_k \neq a_{k-1}$

$$\nabla_{\tau_k} = (e_k + e_{k-1})a_k$$

else

$$\nabla_{\tau_k} = 0 \tag{3.4}$$

The negative sign dropped off from Equation 3.3 in the estimate of the phase error gradient is included in the direction of the timing gradient update.

3.2.2 Characterizing the phase detector

The phase detector is characterized during the initial acquisition of timing phase. Two periodic input data preamble sequences can be used for timing acquisition: the $4T$ sequence defined as $a_k \in \{+1, +1, -1, -1 \ldots.\}$ and $6T$ sequence defined as $a_k \in \{+1, +1, +1, -1, -1, -1 \ldots\}$. Both of these sequences satisfy the run length constraint of 1. This results in an equalized slicer input wave-form for the two acquisition patterns shown in Figure 3.2. As seen in Figure 3.2, the $4T$ acquisition pattern uses only the two inner levels whereas the $6T$ pattern uses all 4 amplitude levels in MDFE.

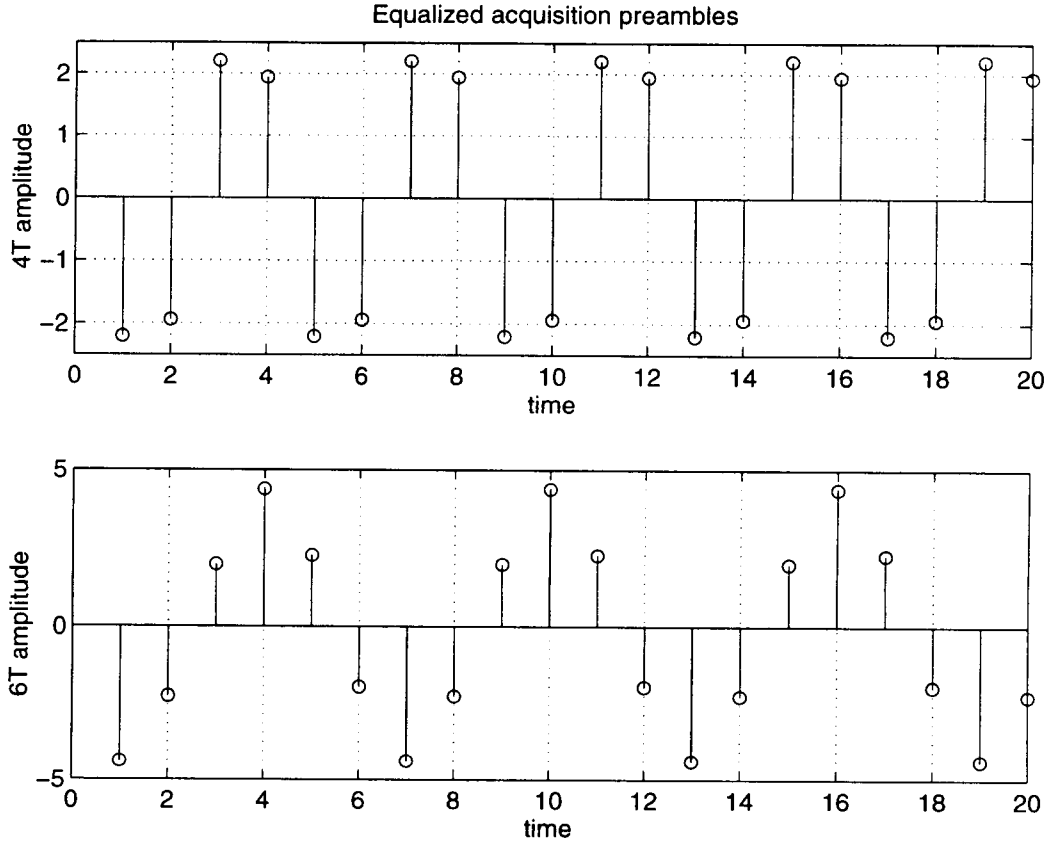


Figure 3.2 Equalized $4T$ and $6T$ acquisition sequence patterns

In order to characterize the phase detector, the first and second order statistics or the mean and standard deviation of the phase error are used. The mean shows the monotonicity and zero crossing of the timing function used to estimate the phase error.

The standard deviation gives an insight into the noise in the timing function which indicates how much the update at every instant is going to cause sampling jitter. This noise is smoothed out by the loop filter in the phase locked loop of the timing recovery circuit. Phase offsets were simulated by linearly interpolating the output samples of the over-sampled equalized dibit of the forward path implemented as a polyphase channel. As colored noise is added to the channel, the statistics were averaged over 10000 points.

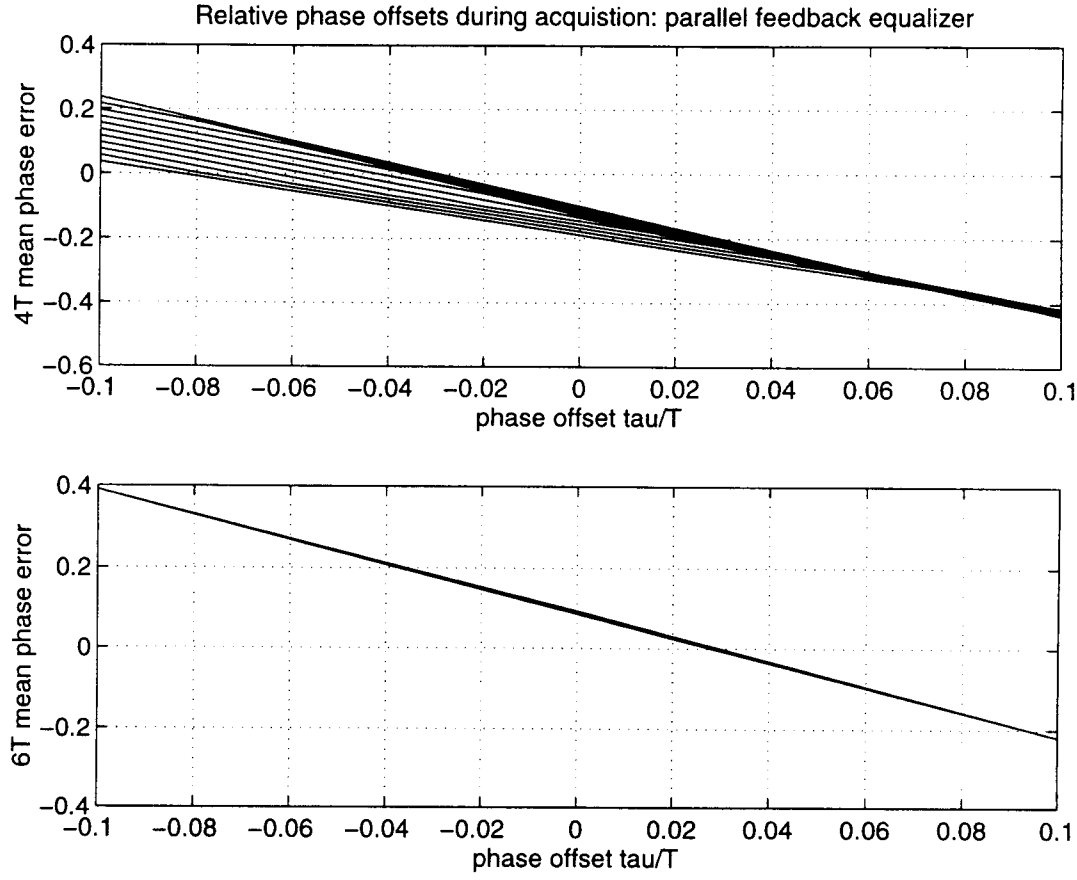


Figure 3.3 Impact of relative phase offsets due to parallel realization of the feedback equalizer on the $4T$ and $6T$ acquisition sequences

The nature of the acquisition sequence used in MDFE has an impact on the two parallel feedback detectors DFD1 and DFD2. The equalized output of the two feedback detectors during acquisition will be the alternate samples of the wave-form shown in Figure 3.2. The $4T$ sequence results in identical equalized wave-forms at the output of

both the feedback paths whereas the $6T$ sequence results in outputs which are 180 degrees out of phase. The presence of device mismatches in the analog components of the two feedback paths cause relative phase offsets between the two parallel paths. In terms of sampling instants, if output of DFD1 is sampled at $kT+\tau+\Delta\tau/2$, the output of DFD2 will be sampled at $kT+\tau-\Delta\tau/2$ where τ and $\Delta\tau/2$ denote the absolute and relative phase offsets respectively. Hence, if the $6T$ pattern is used for acquisition, the relative phase errors average out, in the $4T$ case the phase detector characteristic gets skewed to the relative phase error between the two feedback paths. Relative phase offsets were introduced in the parallel realization of the feedback equalizer and the simulation results showing its impact on the phase detector mean for the two acquisition sequences are shown in Figure 3.3. The results shown in Figure 3.3 are in concurrence with the acquisition pattern used. As the use of the $6T$ pattern solves sampling phase skews due to device mismatches, and makes use of all possible amplitude levels, it is the acquisition sequence used in MDFE.

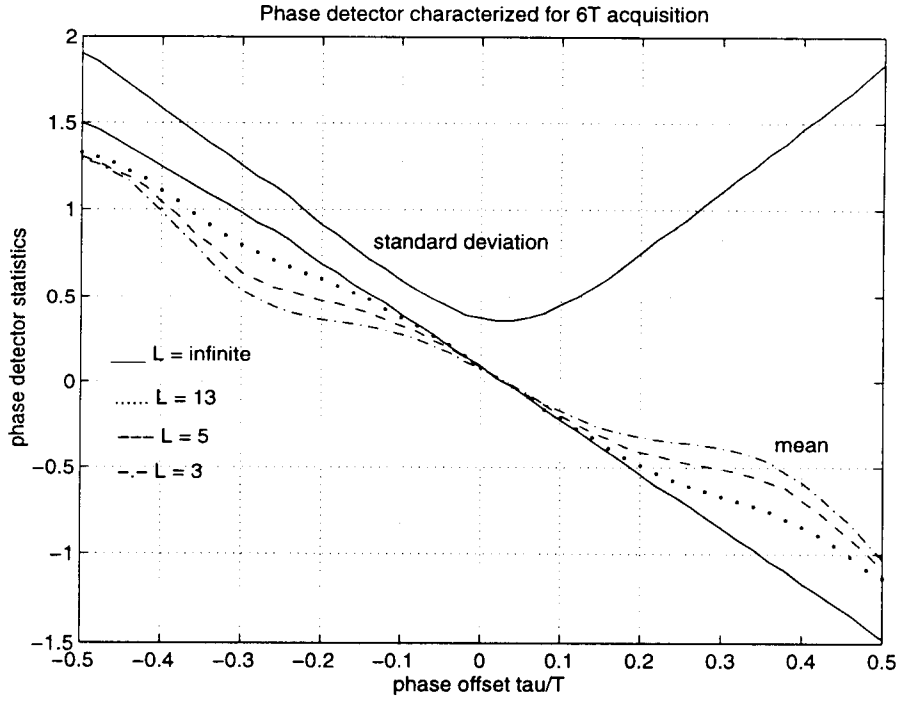


Figure 3.4 Phase detector statistics for 6T acquisition, the mean is characterized with resolution constraints on the flash ADC, the standard deviation is for an infinite resolution channel

Figure 3.4 characterizes the phase detector for offsets within ±0.5 where the phase offset τ is expressed as a fraction of the clock period T, in terms of τ/T. The zero mean phase error occurs at a small sampling phase offset and not exactly at zero phase. This is attributed to the uncanceled pre-cursor ISI from the forward path. As an implementation detail, during acquisition the ideal input data values (a delayed version of the input data accounting for the propagation time through the forward path) are forced into the feedback paths and are also used to estimate the timing function. This is important during channel start-up as large timing errors cause numerous decision errors rendering the estimated phase error meaningless. Once the timing phase has been acquired, the decisions from the slicer are fed back. The standard deviation of the phase error for the same range of phase offsets is shown in Figure 3.4. The minimum value is approximately 0.35 and is attributed to the fact that the equalized dibit has been normalized to a peak value of 2.0 as opposed to 1.0. The impact of quantization of the phase detector mean is also shown in Figure 3.4. Quantization introduces non-linearities in the phase error mean but the monotonicity and zero crossing are maintained.

Figure 3.5 shows the impact of quantization on the standard deviation of the phase error. In order to make a fair comparison, the standard deviation for each resolution of the flash ADC was scaled by the slope of the phase error in the range of offsets where linearity of the mean is maintained (between $\pm\ 0.1T$). As seen in the Figure 3.5, the standard deviation of the phase error increases progressively with decreased resolution in the flash ADC. But the increase in the standard deviation is not substantial and the resolution of $L = 5$ output thresholds for each inner level provides a good trade-off between timing function noise and resolution of the flash ADC.

The tolerance of the step size for the proposed flash ADC was specified to be within ±5% of the step size Δ. This range was decided by checking its impact on the slope of the phase error. The change in the slope of the phase error due to this range of errors in the step-size did not increase the phase error variance appreciably.

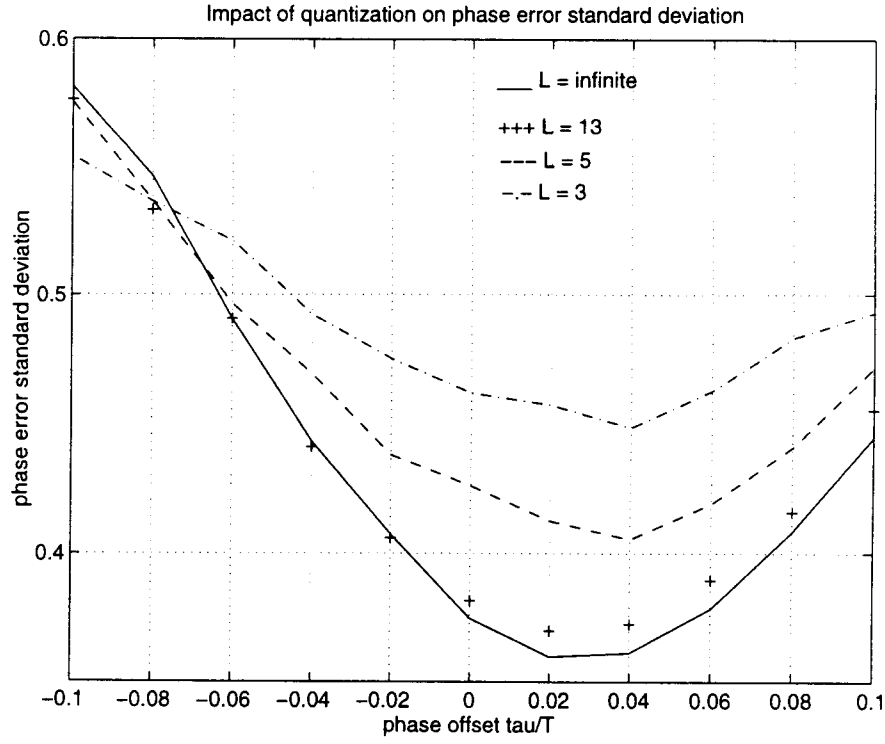


Figure 3.5 To illustrate the increase in phase error noise with quantization

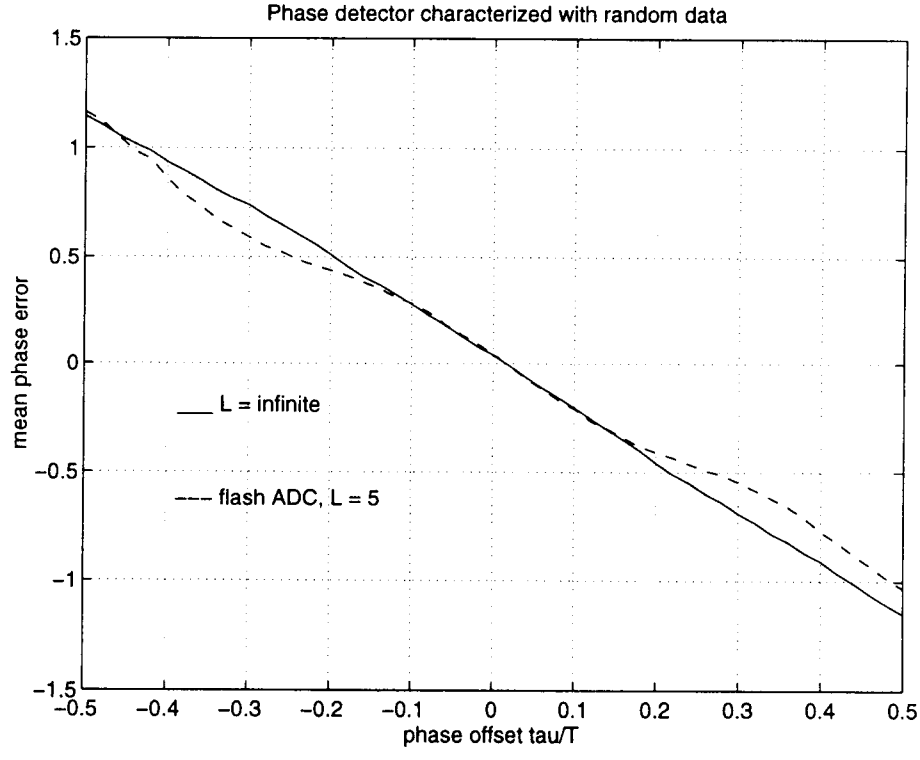


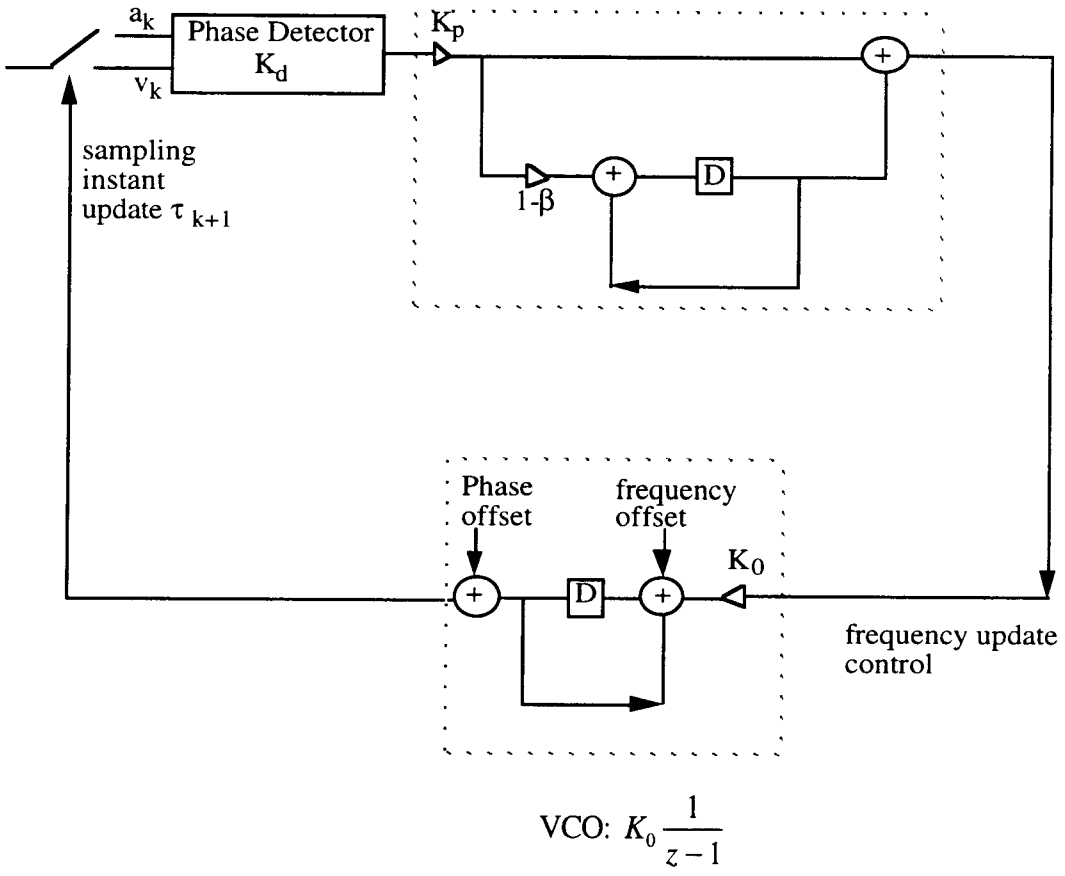
Figure 3.6 Phase detector mean with random data

Figure 3.6 characterizes the mean of the phase detector during the channel tracking mode, with random data. The Figure 3.6 shows the expected decrease in the slope of the mean phase error during tracking as the random data pattern reduces the clocking energy. Information about the slope of the phase error is needed in implementing the phase locked loop as discussed in Section 3.2.3.

3.2.3 Timing gradient update using the phase locked loop (PLL)

A second-order phase locked loop (PLL) is required in MDFE to handle frequency and phase offsets. A block diagram of the PLL is shown in Figure 3.7 and is drawn in the form the simulations were structured.

$$\text{Loop Filter } L(z) = K_p \frac{1-\beta z^{-1}}{1-z^{-1}}$$



$$\text{VCO: } K_0 \frac{1}{z-1}$$

Figure 3.7 Block diagram of second order PLL

An offset in frequency between the incoming data rate and the local clock can be visualized as a consistent change in sampling phase with time i.e., it corresponds to sampling at $T+\delta T$, $T+2\delta T$, $T+3\delta T$, ... time instants. Such an offset in frequency is estimated along with the phase error and can be brought to zero by using an integrator in the loop filter [Lee and Messerschmitt, 1994]. The PLL constantly updates the sampling period T taken at the sampling time τ_{k+1} according to:

$$\begin{aligned} \tau_{k+1} &= \tau_k + K_0 T_k \\ T_k &= T_{k-1} + K_p K_d (\nabla_{\tau_k} - \beta \nabla_{\tau_{k-1}}) \end{aligned} \tag{3.5}$$

where K_0 is the gain of the VCO, K_d is the slope or the gain of the mean phase error, K_p is the loop filter gain and β is the location of the zero in the loop filter. From the phase detector characteristic of Figure 3.4, the value of $K_d = 3/2\pi$ radians^{-1} during acquisition. The gain of the VCO is approximated as $\pi/2$ radians for the simulations. Hence K_p and β are chosen to determine the radius r of the closed loop poles in the z-plane which determines the bandwidth of the PLL. The radius r is solved from the characteristic equation of the PLL which is the denominator of the closed loop phase transfer function:

$$1 - (2 - K_d K_0 K_p) z^{-1} + (1 - K_d K_0 K_p \beta) z^{-2} = 0 \tag{3.6}$$

As the PLL is a two pole system, this is of the form

$$\begin{aligned} &(1 - re^{j\theta} z^{-1})(1 - re^{-j\theta} z^{-1}) = 0 \\ &= r^2 z^{-2} - 2r\cos\theta z^{-1} + 1 \end{aligned} \tag{3.7}$$

Hence,

$$r = (1 - K_0 K_d K_p \beta)^{1/2} \tag{3.8}$$

The zero of the loop filter β was set to 0.99 which gives a good compromise between acquisition speed and low steady-state timing jitter (timing jitter is the standard deviation of the PLL transient response). The value of the loop gain was chosen to be large during acquisition (0.03) and shifted down to 0.01 during tracking. This translates into a radius of 0.9888 during acquisition. From Figure 3.6, the slope of the phase detector with

random data reduces to $2.3/2\pi$ translating to a radius of 0.9972 during tracking. Hence the PLL encloses a wide bandwidth during acquisition which permits faster settling and a narrower bandwidth during tracking to follow slow steady-state timing variations with reduced timing jitter.

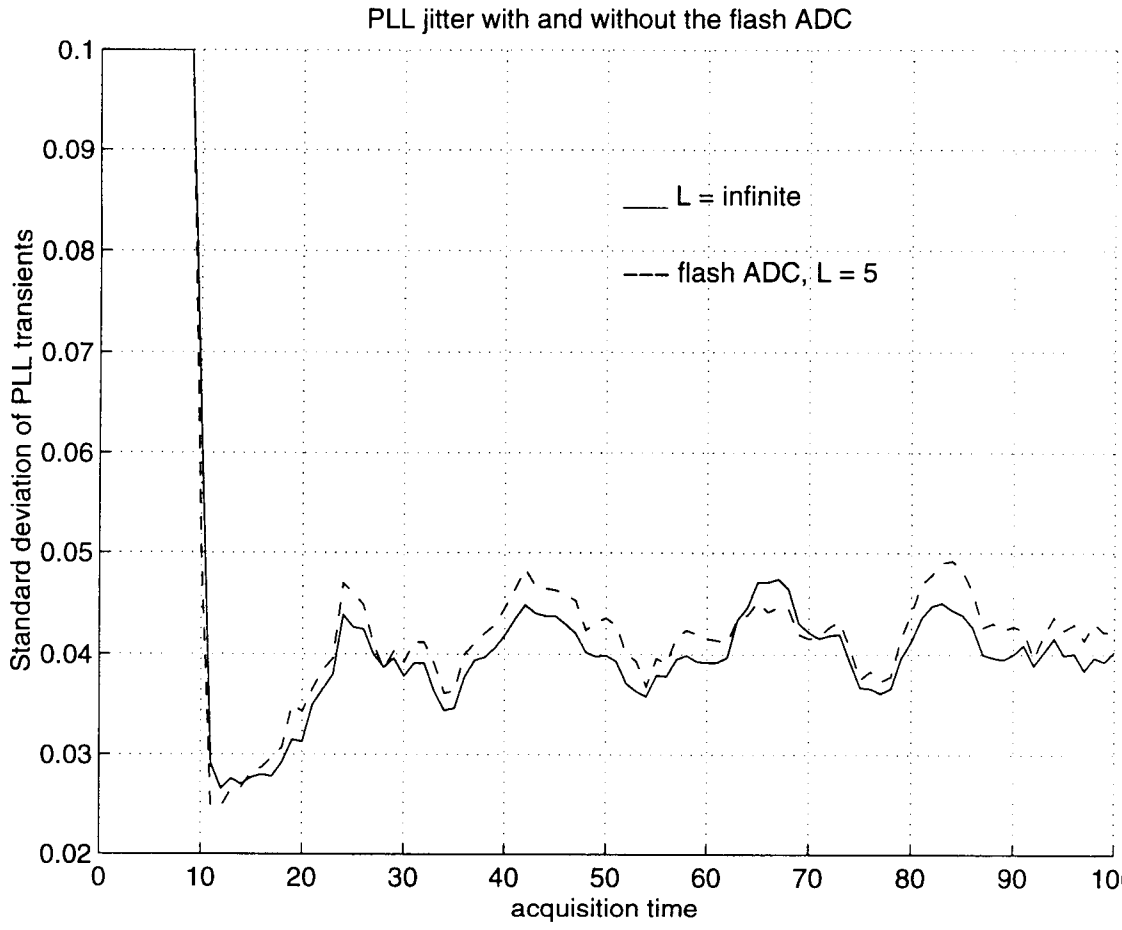


Figure 3.8 To illustrate the increase in timing jitter with the flash ADC

The transient response of the PLL is characterized by its mean and standard deviation over an ensemble of 50 realizations. By observing an ensemble instead of a single realization, the average impact of the colored noise on the PLL transients is seen. Figure 3.8 shows the jitter in the PLL with and without the flash ADC. The mean response of the PLL for a 10% step in phase was first made identical for both cases by normalizing the gain of the phase detector. The results show that the PLL is able to

average the noise introduced in the timing function due to quantization and the incremental timing jitter is negligible. The steady-state channel performance with this amount of jitter has been verified and will be presented in Section 3.4.2.

3.3 Gain recovery

Gain errors result from the random variations in the position of the head with respect to the storage medium, unknown gains of amplifiers preceding the read channel, temperature variations etc., and is analogous to flat fades or amplitude drops in communication channels. The gain recovery scheme employed in MDFE is also based on decision-directed stochastic gradient descent as the timing recovery scheme. An example of a gain error is shown in Figure 3.9 and is estimated at each sampling instant along with the timing error.

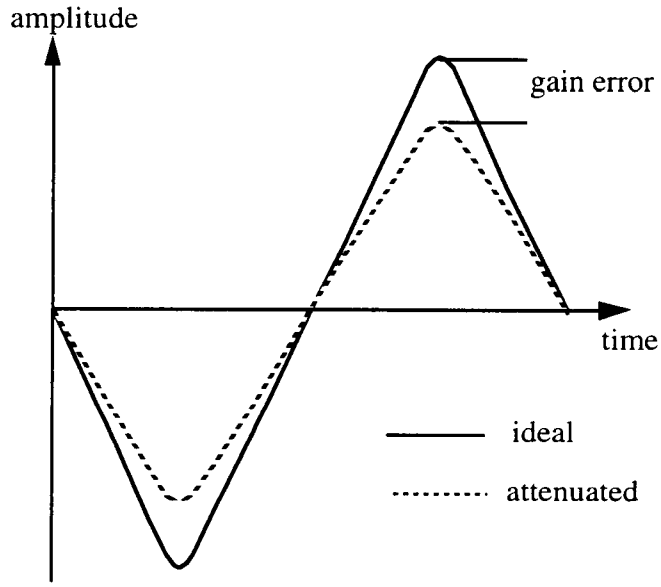


Figure 3.9 Example of a gain error

3.3.1 Gain detection

It is desirable to perform gain updates using gain errors estimated from signals with large amplitudes. The two outer levels in MDFE have large amplitudes making them

attractive for gain detection. Two considerations discourage the use of the outer levels for updating the gain: increased complexity in the flash ADC, and decision errors are very unlikely on these outer levels. Consequently, the gain update is done only on the inner levels and are set to zero otherwise just as in the timing recovery scheme.

Starting with the slicer error e_k (ideal value - actual) defined as:

$$e_k = \hat{v}_k - v(kT) \tag{3.9}$$

The mean-squared gain error gradient is obtained as:

$$\begin{aligned} \nabla_{g_k} &= E\left[\frac{\partial}{\partial g}(e_k^2)\right] \\ &= -2E\left\{e_k \frac{\partial}{\partial g}[v(kT)]\right\} \\ &\cong -e_k sign\left\{\frac{\partial}{\partial g}[v(kT)]\right\} \end{aligned} \tag{3.10}$$

Equation 3.10 gives the stochastic gain error gradient and when used only during zero crossings (or the two inner levels), the decisions at the corresponding time instants give the sign of the slope of the gain error. Thus the gain gradient is summarized as:

$$\begin{aligned} &\textit{if } a_k \neq a_{k-1} \\ &\quad \nabla_{g_k} = e_{k-1}a_{k-1} + e_k a_k \\ &\textit{else} \\ &\quad \nabla_{g_k} = 0 \end{aligned} \tag{3.11}$$

The gain detector has been for $6T$ acquisition similar to the phase detector for gain errors ranging from 0.5 to 1.5 and is shown in Figure 3.10 (the mean is shown with resolution constraints on the flash ADC and standard deviation is shown on an infinite resolution channel). The ideal gain at the zero crossing of the mean gain error should be 1. But uncanceled pre-cursor ISI leads to a bias in the gain error during acquisition. Figure 3.11 shows the impact of quantization on the increase in the standard deviation of the gain error. This comparison was done in the same manner as in the phase detector, by scaling the estimate of the gain error for constant slope.

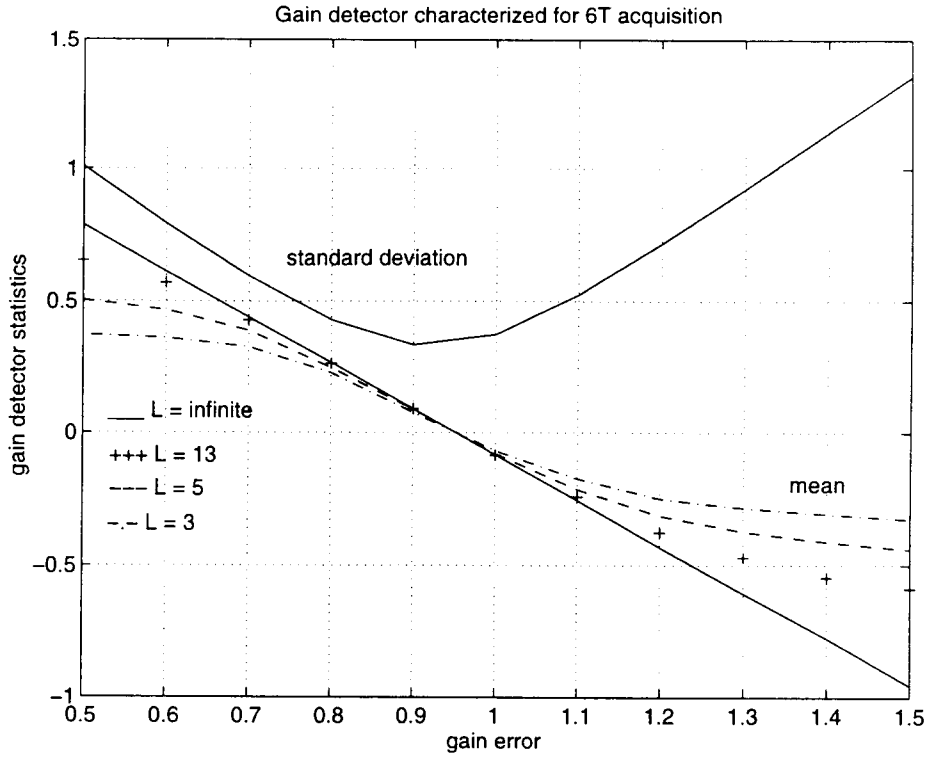


Figure 3.10 Gain detector statistics for 6T acquisition

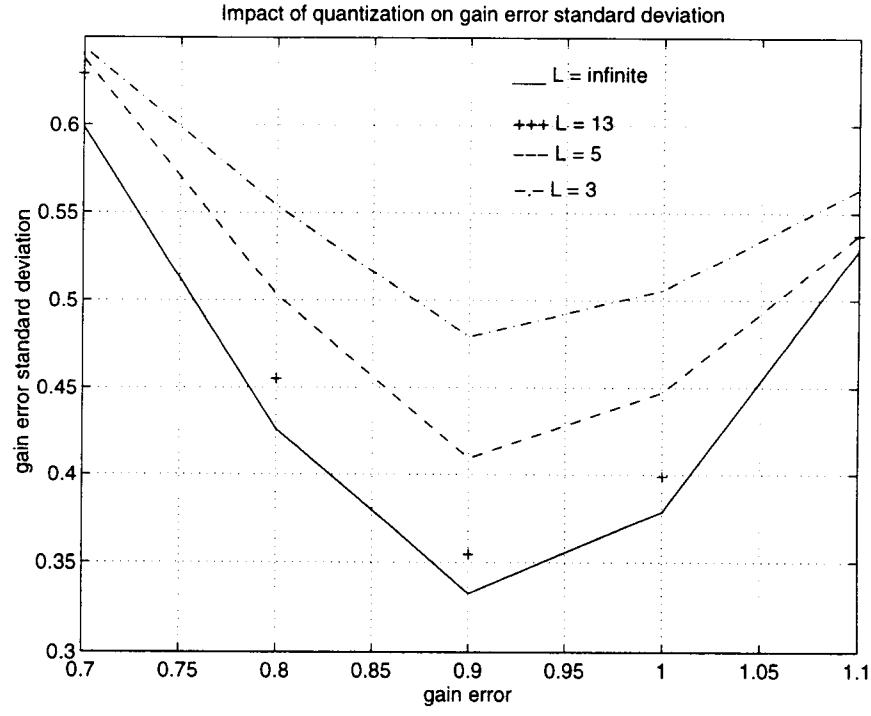


Figure 3.11 To illustrate the increase in gain error noise with quantization

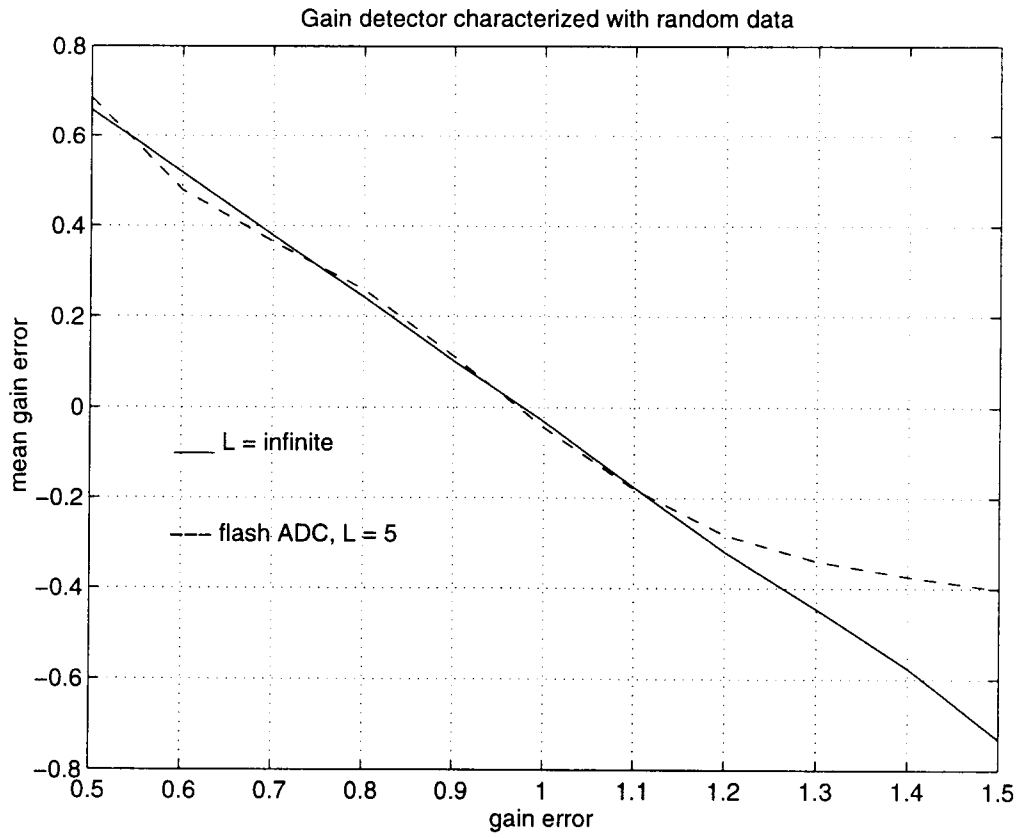


Figure 3.12 Gain detector mean with random data

Figure 3.12 characterizes the gain detector with random data. The slope of the gain detector during acquisition from Figure 3.10 is 1.7435 and reduces to 1.39 during tracking (measured from Figure 3.12).

3.3.2 Automatic gain control (AGC) using the gain gradient

A block diagram of the AGC is shown in Figure 3.13. The gain gradient update g at time k which summarizes the operation of the gain recovery loop can be written as:

$$g_{k+1} = g_k + k_g \nabla_{g_k} \tag{3.12}$$

This update is implemented as a first-order integrator with a gain of k_g. Similar to the PLL, a large loop gain is used during acquisition for quick settling and shifted down to a smaller value during steady-state for tracking slow variations and reducing the gain jitter. The same values of loop gain constants used in the PLL work well with the AGC. The mean

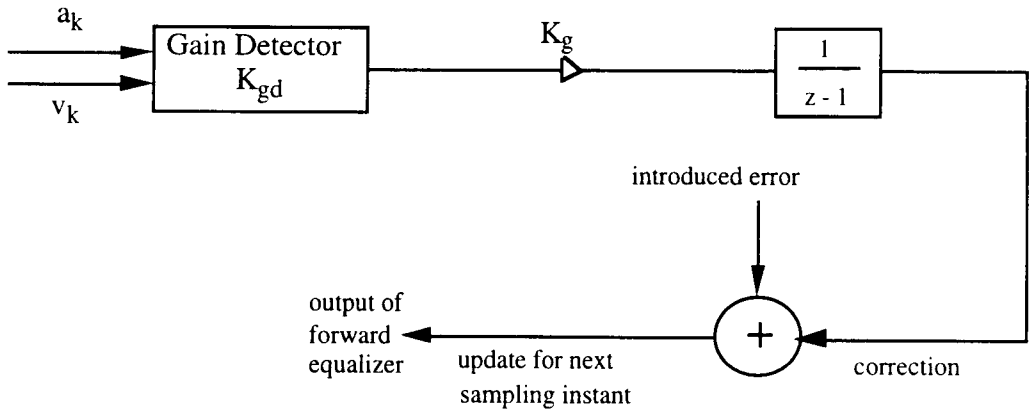


Figure 3.13 Block diagram of AGC

and standard deviation of the gain recovery loop transients are also observed as an ensemble average as in the PLL.

3.4 Results from the joint operation of timing and gain recovery

3.4.1 Channel transients

As the timing recovery and channel equalization are highly inter-related adaptive loops, timing acquisition precedes the adaptation of the feedback equalizer in MDFE. Hence the feedback equalizer is initialized with a reasonable set of start-up coefficients. Once acquisition is complete, the equalizer adapts in the fine tuning mode to track slow channel variations as will be elaborated in Section 3.5.

The first important concern during channel start-up is that the PLL and AGC acquire together successfully and settle quickly. As the estimate of the timing and gain gradient is made at every sampling instant, isolated information about the two errors cannot be conveyed to the PLL and AGC. Hence the settling of the PLL is slowed down by the presence of gain errors and timing errors affect the operation of the gain recovery loop. The joint trajectories of the phase and gain during acquisition for a small range of phase offsets and gain errors has been illustrated [Schmid, 1995]. But the use of the $6T$ acquisition pattern requires a monotonic phase detector for large offsets extending between $-3T$ and $3T$ to ensure successful capture of the PLL into steady-state.

Thus the first step in looking at the channel transients was to characterize the phase detector for offsets extending to three clock cycles during acquisition as seen in Figure 3.14. As this characterization is crucial to the channel start-up scheme, it has been done for user *PW50*'s 2.0, 2.5 (with and without the flash ADC) and 3.0. From the Figure 3.14, monotonicity is retained for offsets within $\pm 1.5T$. A precautionary measure has to be taken to ensure that the start-up offsets stay within the range over which the slope of the phase detector is negative. This is equivalent to having reliable information about where to sample the continuous time $6T$ preamble sequence coming out of the forward equalizer.

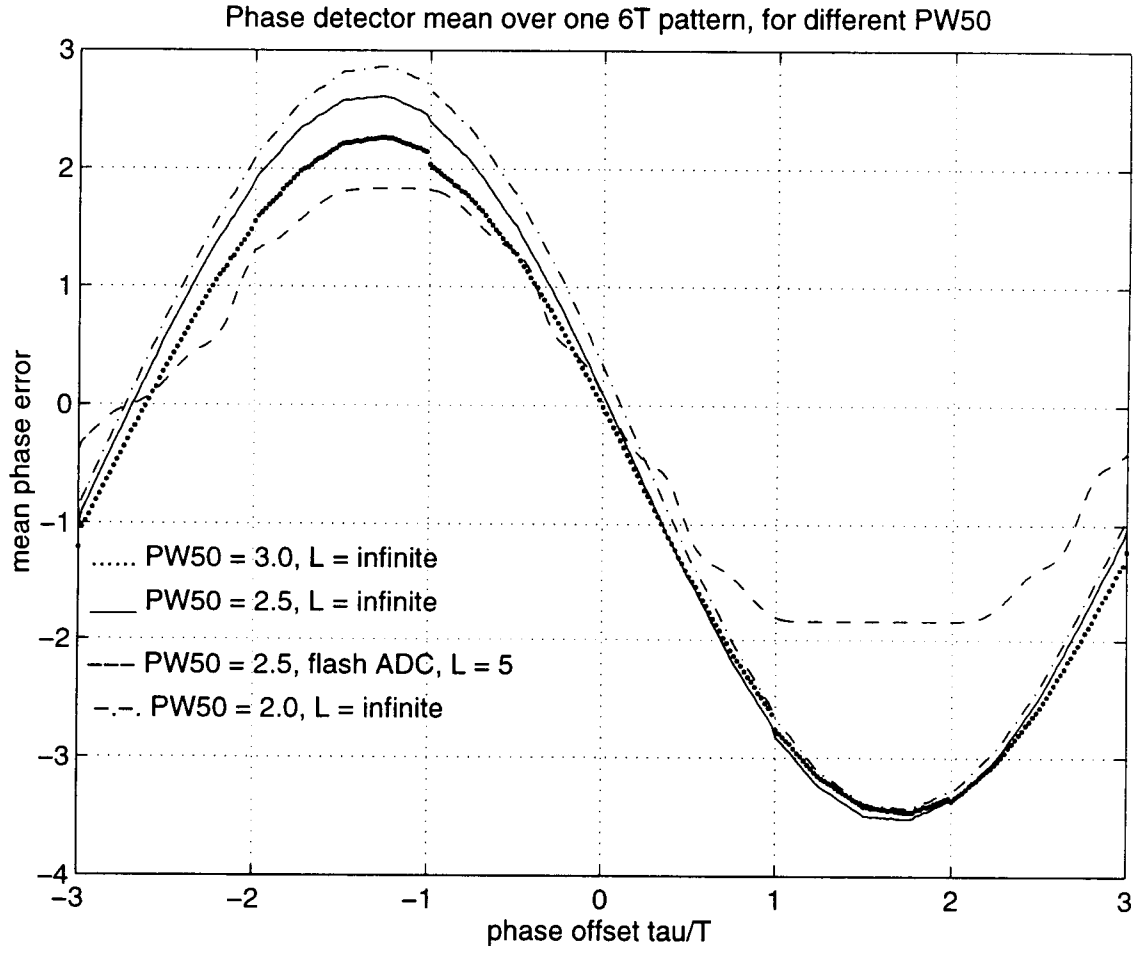


Figure 3.14 Phase detector characterized for offsets containing one $6T$ pattern, for user densities 2.0, 2.5 (with and without the flash ADC), and 3.0

A solution to this problem is to start the channel with the feedback detectors disconnected and make decisions on the unequalized forward path wave-form. As seen in Figure 3.15, when the sequence -1 followed by a +1 is detected, definite information about the location of the sampling point on the sine wave is obtained and the feedback detectors can then be connected to the channel to begin the equalization. If the sequence

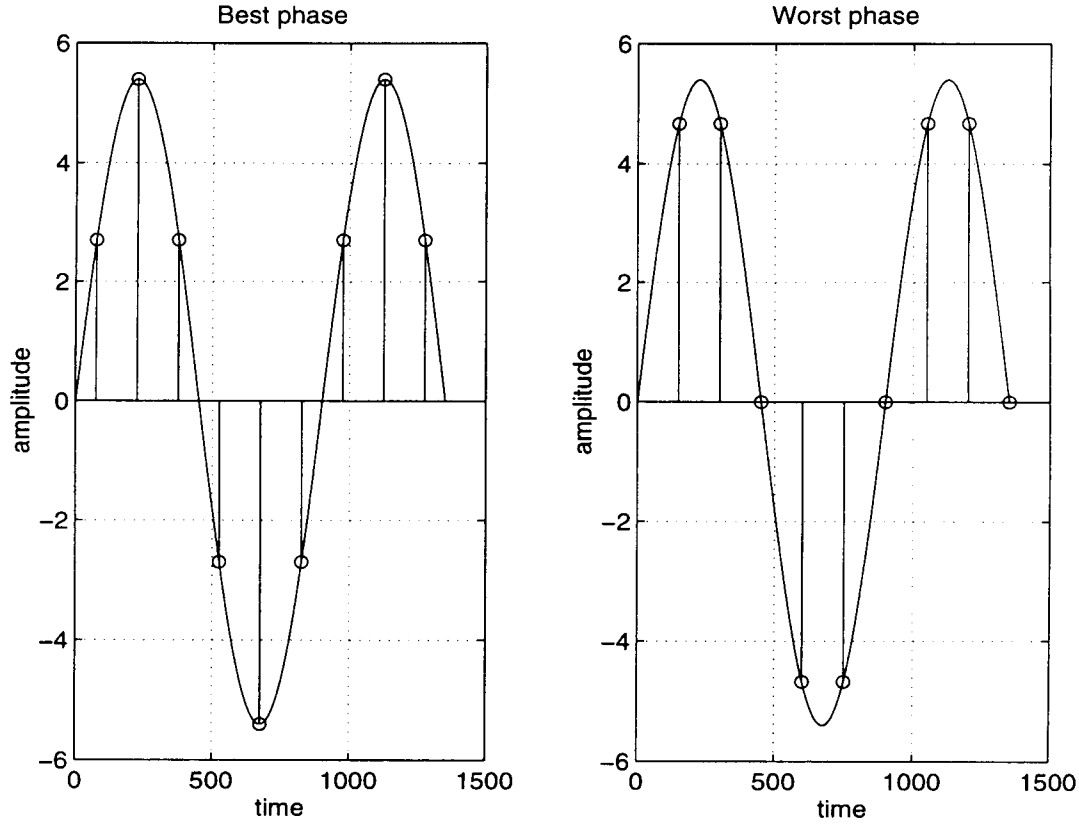


Figure 3.15 Start-up offset boundaries on an ideal continuous-time sine wave from the forward equalizer

-1 followed by a +1 was made correctly as also illustrated in Figure 3.15, the worst case sampling offsets are bounded within ± 0.5T. But during the transient state of the channel, possible sources of decision errors are the dc offsets from the analog components in the system, large gain errors, and noise sources which lead to the following three error cases:

Case(i): If the first decision -1 is in error, the sequence coming into the forward filter is in reality +1, +1, +1, -1, -1, -1 .... whereas the sequence forced into the feedback filter

starting from time instant 3 would instead be +1, +1, -1, -1, -1 .... resulting in a start-up phase error of $-T \pm 0.5T$.

Case(ii): If the second decision alone is incorrect, the forward path preamble is a -1, -1, -1, +1, +1, +1, ... and the corresponding feedback preamble from time instant 3 is a +1, +1, -1, -1, -1, ... causing a start-up phase error of $+2T \pm 0.5T$. This case is a decision error in the middle of the sine wave where the amplitude is expected to be 6 dB larger than near a zero crossing corresponding to the first case decision of -1. But this assumption is more reliable during channel steady-state and such an error is possible during transients.

Case(iii): The third case of decision error would be the one where both -1, and +1 are detected incorrectly and the forward and feedback preambles end up being a whole $3T$ $\pm 0.5T$ apart in phase.

Table 3.1 Error events and Phase errors for the proposed start-up sequence

Possible error combinations	Start-up phase error
a_1	$+T \pm 0.5T$
a_2	$-T \pm 0.5T$
a_3	not allowed in MDFE
a_1, a_2	not allowed in MDFE
a_1, a_3	$+2T \pm 0.5T$
a_2, a_3	$-2T \pm 0.5T$
a_1, a_2, a_3	$+3T \pm 0.5T$

To make sure that the phase offsets are securely bounded within $\pm 1.5T$, it is safer to wait for a sequence -1, +1, +1 to make the occurrence of possible error cases more remote. Table 3.1 illustrates all the error possibilities along with the resulting start-up phase offset where the sequence is denoted as a_1, a_2, and a_3. This start-up scheme was tested over 50 different realizations of a simulated continuous-time sine wave with a resolution of 0.001% of a clock period, corrupted by dc offsets within ±10% of the ideal inner level, gain errors within ±50% and band-limited noise at an SNR of 20 dB. The results are shown in Figure 3.16 and of all the realizations, about 13% of the trials in the random experiment caused decision errors resulting in offsets outside the expected $\pm 0.5T$

but bounded within $\pm 1.5T$. From the simulation results, only the first two error events of Table 3.1 are likely to occur, the other error events are highly improbable showing that this is a reliable start-up scheme.

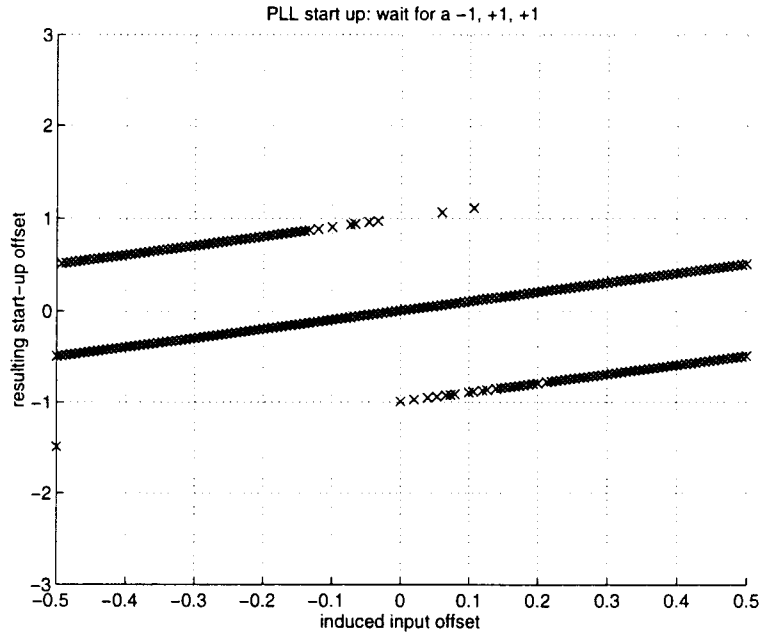


Figure 3.16 Results to verify the channel start-up scheme

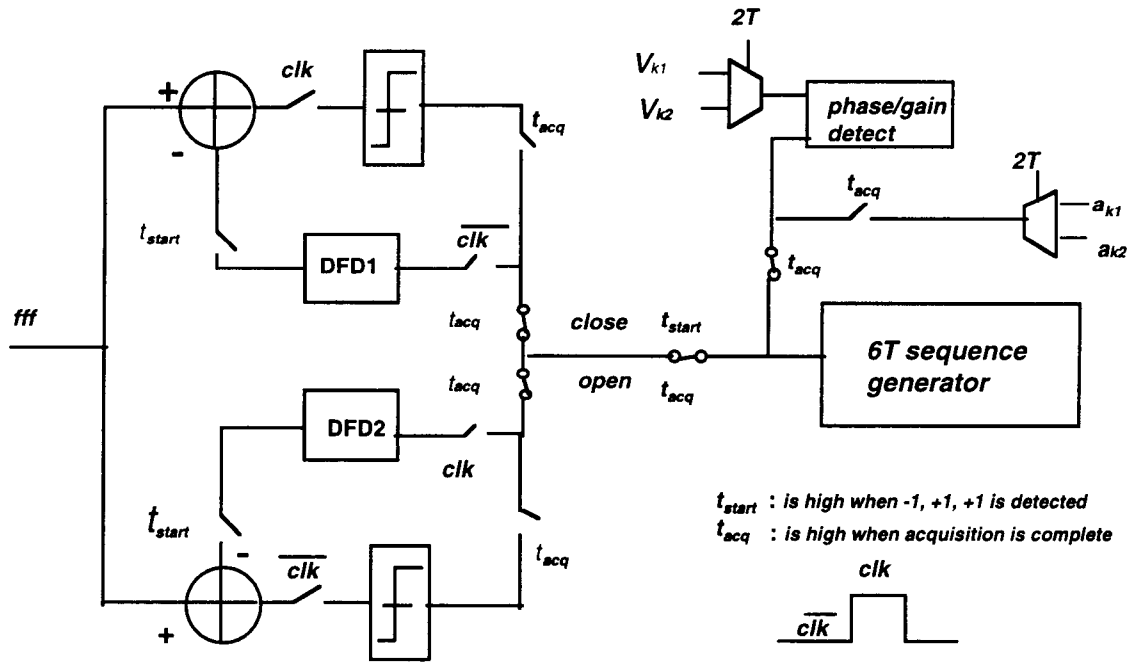


Figure 3.17 Implementing the channel start-up scheme

Figure 3.17 shows a block diagram to illustrate the channel start-up scheme. When the sequence -1, +1, +1 is detected from this continuous-time sine wave, the discrete-time feedback equalizer is connected to the channel. The contents of three shift registers in series are pre-loaded with the pattern consistent with the -1, +1, +1 sequence. When this pattern is detected from the output of the forward equalizer, the timing/gain acquisition begins. The output of the $6T$ preamble generator feeds into the two feedback detectors and is also used to estimate the phase/gain errors during acquisition. Once acquisition is complete, the $6T$ sequence generator is disconnected and the actual decisions from the slicers are fed back and used to estimate the timing and gain gradients.

The range of frequencies the PLL should be able to lock onto is specified to be within $\pm 1\%$ of the clock frequency. This range is sufficient to account for the spindle speed variations in the disk drive. Figures 3.18 and 3.19 show the PLL/AGC transients for two extreme startup errors: phase offset of $\pm 150\%$, frequency offset of $\pm 1\%$ (one-hundredth of the clock) and gain errors of $\pm 50\%$. Both the PLL and AGC are able to successfully recover from these errors and achieve lock into steady-state.

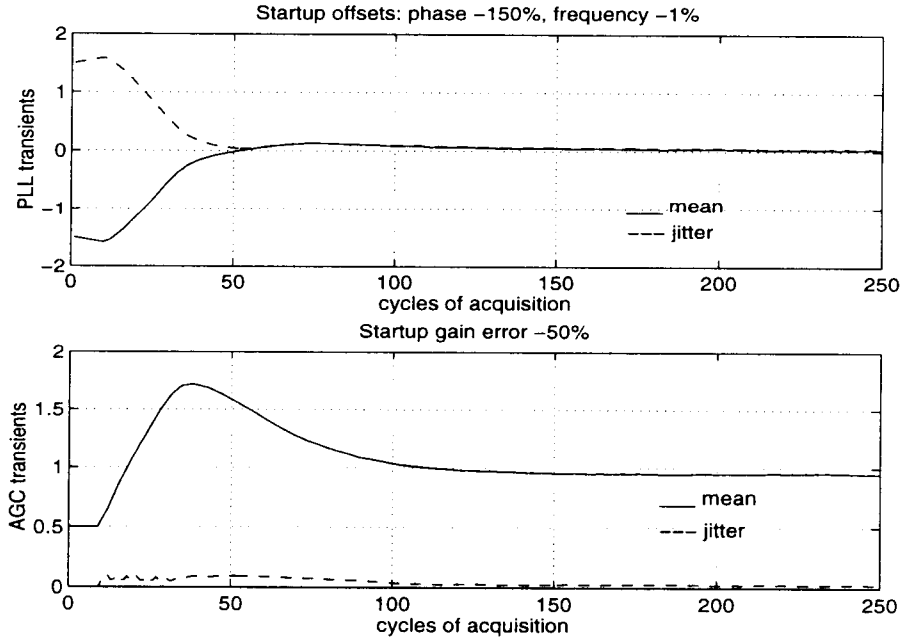


Figure 3.18 PLL/AGC transients for extreme negative start-up errors with the flash ADC

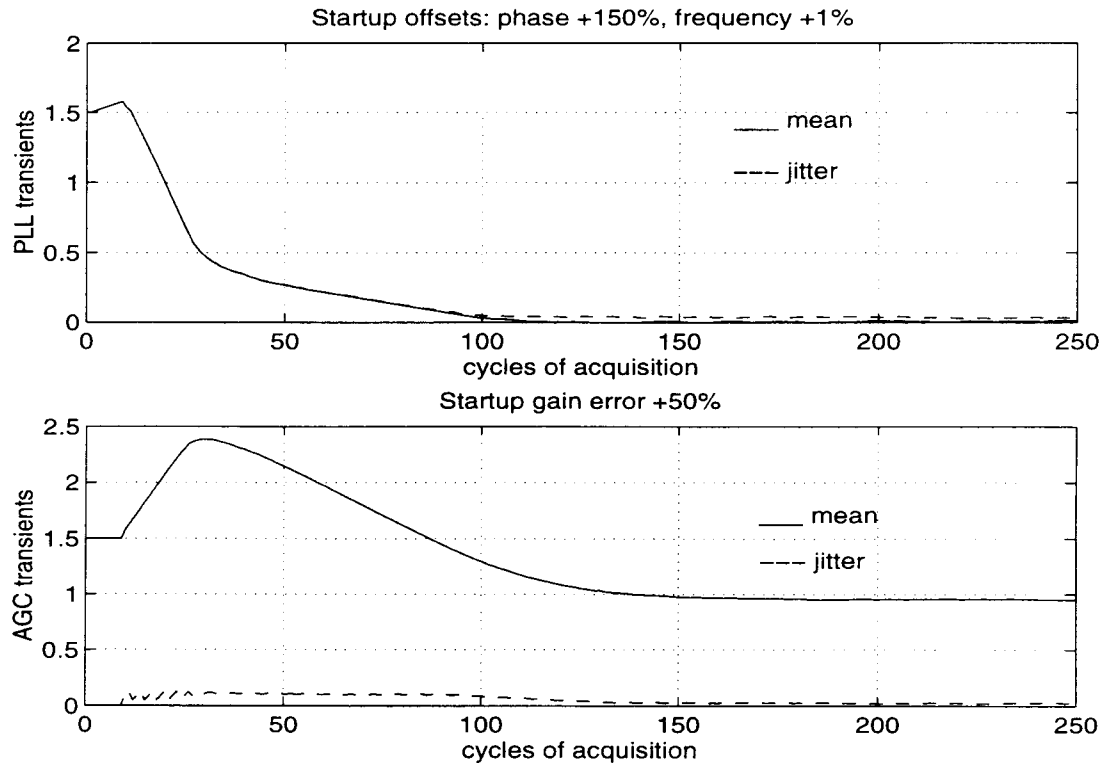


Figure 3.19 PLL/AGC transients for extreme positive start up errors with the flash ADC

Table 3.2 Pull-in time Vs resolution of flash ADC

number of output thresholds for each inner level	3	5	7	9	11	13	infinite
pull-in time	300	250	200	180	160	140	120

The pull-in time of the timing and gain recovery loops is not only influenced by the interaction between the two adaptive loops but also by the resolution of the flash ADC. Acquisition was empirically defined to be complete when the mean of the PLL and AGC transients stayed within 0.005 of their final value for 50 clock cycles. The worst case pull-in time for an infinite resolution channel occurred for the extreme negative start-up error case as determined by simulations. For this worst case, the resolution constraints were imposed on the flash ADC and increase in the pull-in time with decrease in the resolution is tabulated in Table 3.2.

3.4.2 Channel steady state

The steady-state channel performance was assessed by measuring error-rates. The channel error-rate was empirically defined as 200 errors divided by the number of input symbols required to generate them. This value of 200 errors was chosen in order to get a reasonably consistent estimate of the error-rate. As the flash ADC step size was chosen assuming a channel *SNR* of 20 dB, the channel error-rates at this *SNR* were measured with and without the flash ADC including the steady-state jitter from the timing and gain recovery loops. The results are expressed as log_{10} and without the flash ADC the value was -5.7012 and including the flash ADC the value was -5.6056. Thus the additive noise introduced by the uniform quantization is averaged by the PLL loop filter without significant error-rate degradation.

Nevertheless, it is interesting to translate the steady-state jitter from the timing recovery loop into ISI which contributes to the total noise power specifying the *SNR* of the channel. As the forward path output is sampled, timing jitter results in random variations in the position of the forward path impulse response thus contributing to the ISI. Since the timing variations are random, this type of noise cannot be modeled as a constant variance term like the additive noise specified by the channel *SNR*, and dependence on the random data pattern is expected.

Referring to the channel model of MDFE introduced in Figure 1.8 of Chapter 1, the data a_k stored on the medium in terms of +1 and -1 using saturation recording and is translated to a ternary signal b_k in terms 1, 0 and -1 modeling the differentiation of the read head that detects transitions from -1 to +1 and +1 to -1. b_k is convolved with the Lorentzian step response *s(t)* and the forward path impulse response *l(t)* that includes the low pass receive filter and the all pass forward equalizer. If c_k represents the output of the forward path, and *h(t) = s(t)*l(t),* (* is the convolution operator),

$$c_k = \sum_j (b_j + n_j)[h_{k-j} + \nabla t_j h_{k-j}'] \tag{3.13}$$

where the dependence of the entire forward path impulse response h_k on the sampling instant has been approximated by a first order-Taylor series expansion. Hence the forward path impulse response consists of two paths, the sum of the nominal response and a residual component due to the timing jitter. The signal to noise ratio can be written as:

$$SNR = 10\log_{10}\left[\frac{\sum_k h_k^2}{\sigma_x^2 + \sigma_t^2 \sum_j (b_j h_{k-j}')^2}\right] \tag{3.14}$$

where σ^2_x represents the variance of the noise (ISI + additive white Gaussian noise) colored by the nominal channel, and σ^2_t is the variance of the timing jitter. Hence the signal to noise ratio becomes dependent on the transitions or the input data pattern. Extensive analysis of the read channel performance dominated by jitter due to data transitions has been done by Moon [1991 a, b]. In order to make an approximate estimate of the loss in *SNR* due to timing jitter, error-rates were measured with and without the timing recovery loop. A value of -4 was obtained in the absence of timing jitter in the channel for an *SNR* of 18 dB. When timing jitter was included, the same error-rate was obtained for an *SNR* of 18.2 dB and hence an approximate measure of the loss in *SNR* 0.2 dB.

3.5 Adaptive Equalization of feedback equalizer

3.5.1 A brief review of LMS for adaptive equalization

Adaptive equalization is a practical solution to situations as in disk drives where the channel response is initially unknown. The feedback equalizer in MDFE is made adaptive using the LMS algorithm which is a popular choice for adaptive equalizers [Qureshi, 1985]. The LMS algorithm gives an iterative solution to obtain the filter coefficients such that the mean-squared error of the channel ISI + noise is minimized. It is a simplification to the mean-squared error gradient algorithm [Lee and Messerschmitt, 1994] which states that the iterative solution to the optimum coefficient vector $W = [w_0, w_1, \ldots, w_L]$ of an adaptive filter with L taps is given as:

$$W_{k+1} = W_k + \beta \nabla \xi(W_k) \tag{3.15}$$

where k denotes the time index, and $\nabla\xi(W_k)$ is the slope or gradient of the mean-squared error $\xi(W_k)$. The mean squared error is a quadratic surface with respect to the coefficient vector and its gradient is given as:

$$\nabla\xi(W_k) = -E[e_k A_k] \tag{3.16}$$

where e_k is the error (i.e., the difference between the ideal filter output and its actual value), and A_k is the vector of filter input values. Since the gradient gives the direction of the error, the update to the coefficients at every time instant is done in the opposite direction and can be written as:

$$W_{k+1} = W_k + \beta E[e_k A_k] \tag{3.17}$$

The LMS algorithm implements this coefficient update as:

$$W_{k+1} = W_k + \beta e_k A_k \tag{3.18}$$

LMS substitutes the ensemble average of the mean-squared error gradient with an average over time.

In a decision feedback equalization architecture, the output of the feedback equalizer is subtracted from the forward path output. Hence the LMS update for a feedback equalizer is given as:

$$W_{k+1} = W_k - \beta e_k A_k \tag{3.19}$$

When the equalizer begins to adapt (also referred to as the training mode), its coefficients are far from their ideal values. Hence the input vector A is a sequence of delayed ideal input values. Once the equalizer training is over i.e., after it has stopped adapting, the decisions from the slicer are fed back. It is interesting to observe that the feedback equalizer uses the noise-free decisions as its input, hence it adapts only to minimize the ISI and does not contribute to minimizing the noise power. The error e_k is given as:

$$e_k = \hat{v}_k - v_k \tag{3.20}$$

where $\hat{v}_k$ is the ideal slicer input and v_k the actual value.

Further simplifications are made in implementing this LMS algorithm. As seen from the gradient update equation 3.19 for a feedback equalizer, the decisions a_k +1's and -1's, and if the sign of the error is used instead of its actual value, the coefficient update can be done in steps of β [Hayes, 1996]. Also, if β is expressed as a power of 2, the coefficient adaptation can be done digitally as a binary up-down counter. Hence the sign-LMS update for the feedback equalizer can be written as:

$$w_{k+1} = w_k - \beta sign(e_k) A_k \tag{3.21}$$

The sign-LMS algorithm is a noisier estimate of the mean-squared error gradient as compared to the original LMS algorithm, it uses the magnitude of the error instead of its squared value as the error performance surface (also referred to as the cost function):

$$\xi_k = | e_k | \tag{3.22}$$

Hence the gradient is given as:

$$\begin{aligned} \nabla \xi_k &= sign(e_k) \frac{\partial (e_k)}{\partial W} \\ &= sign(e_k) a_k \end{aligned} \tag{3.23}$$

Using the sign of the error instead of its actual value to update W_k does not alter the direction of the error gradient but only its magnitude. If the error is large, the step size is kept small and vice versa. This is a robust approximation to the LMS algorithm and has been verified by simulations as will be presented in the next section and is the scheme used in MDFE.

3.5.2 Results of feedback equalizer adaptation in MDFE

Adaptation is done only on the two inner levels of MDFE and frozen on the outer levels by setting the LMS error to zero. This is a simplification that eliminates the need for additional analog references at the outer levels based on the fact that the inner levels are a more likely source of error distance (referring to the geometric or Euclidean distance between the equalized levels in MDFE) as compared to the outer levels which are spaced

further apart by a factor of 2. Hence channel variations are more likely to affect decisions from the inner levels as compared to those from the outer levels. This was simulated and verified by measuring the channel error-rates after adaptation was complete. As the results of Figure 3.20 show, adapting only on the inner levels does not significantly degrade the channel error-rate. The criterion for completing the adaptation will be explained shortly.

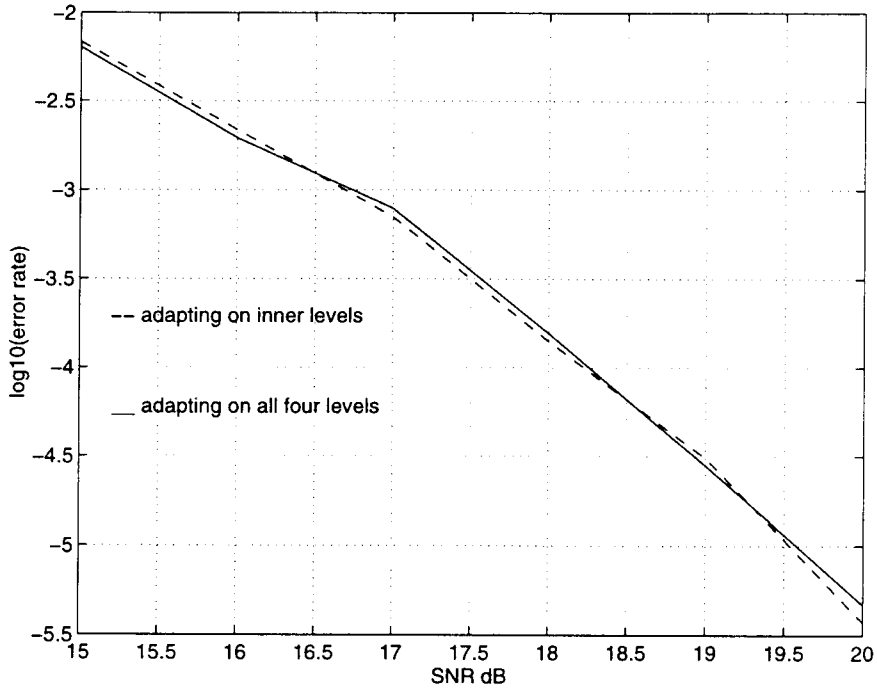


Figure 3.20 Impact of adapting on inner levels on error-rates

In order to study the adaptation in MDFE, the first step was to pick out the value of β [Lee and Messerschmitt, 1994]. A large value of β (not exceeding the bound for stability) ensures fast initial convergence but results large oscillations around the optimum settings. On the other hand, a small value of β attains smaller steady-state mean-squared error with increase in the time for coefficient convergence. It is customary to employ gear shifting algorithms i.e., to start off with a large value of β to come near the optimum value of filter coefficients and then shift it down to a smaller value for fine coefficient tuning. A value of 0.01 to start-up and 0.001 for finer tuning gives a good solution to finite precision

to cover this range for β ($0.01 \cong 2^{-6}$; $0.001 \cong 2^{-10}$). Ten bits are used to store each coefficient update and the six most significant bits are used for the feedback equalization. The feedback equalization is done using analog circuits and the six-bit constraint is the precision of the digital to analog converter (DAC). This was the scheme used in implementing the DFE detection scheme for disk drives [Kajley et al., 1996] where the feedback equalizer has only four taps as opposed to nine in MDFE.

The feedback equalizer coefficient adaptation can be summarized as:

$$
\begin{aligned}
&\textit{If } a_k \neq a_{k-2} && \textit{\% to detect an inner level} \\
&\quad w_k(n) = w_{k-1}(n) - \beta\, sign(e_{k-1}) a_{k-1}(n); && n = 1,2,...,9 \\
&\quad w_k(n) = w_{k-1}(n) - \beta\, sign(e_{k-1}); && n = 0 \\
&\textit{else} \\
&\quad w_k(n) = w_{k-1}(n); && n = 0,1,...,9
\end{aligned}
\qquad (3.24)
$$

where k denotes the time index and n the tap number. The value $n = 0$ is the tap which cancels dc offsets. Device mismatches in the analog circuits of the two parallel feedback paths in MDFE cause dc offsets. This tap integrates the LMS error to zero over time and is independent of the input vector A thereby canceling constant offset errors. DC offsets within $\pm 10\%$ of the inner level were simulated and canceled using this scheme (Figures 3.21 and 3.22). An important implementation detail is the time index of Equation 3.24. The non-causal term in MDFE introduces a delay of 1, hence the appropriate error and input value is used for the coefficient update.

The coefficient convergence for both the original LMS and its sign approximation were simulated. The results for the convergence of the first three feedback taps are shown in Figure 3.21 (original LMS) and Figure 3.22 (sign-LMS). As seen in Figures 3.21 and 3.22, a single realization of the sign-LMS is noisy compared to the original LMS. This is not only due to the sign-LMS approximation but also due to the six-bit precision constraint imposed by the DAC on the final value of the feedback equalizer coefficients.

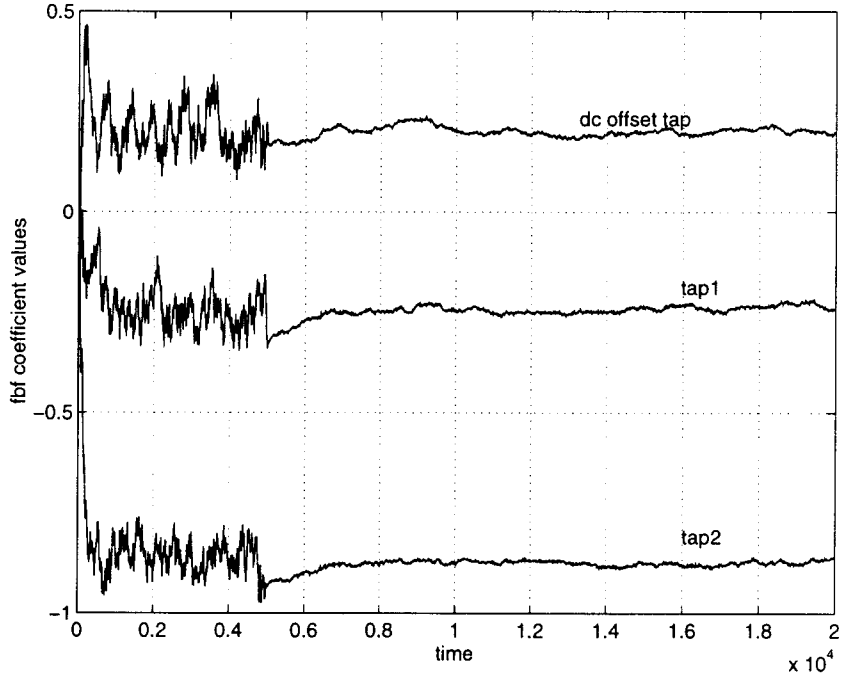


Figure 3.21 Convergence of original LMS algorithm

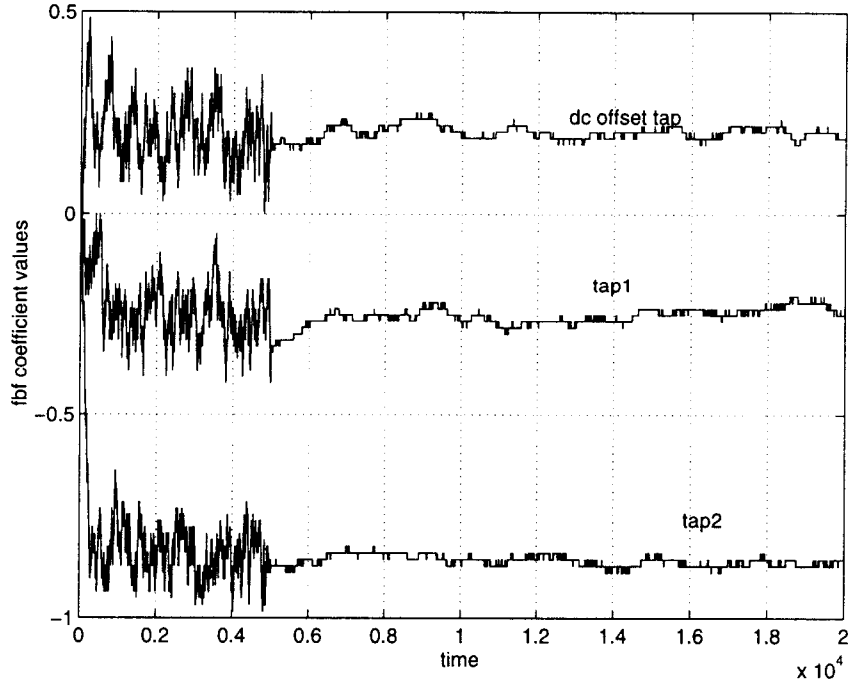


Figure 3.22 Convergence of sign-LMS algorithm

The average value of the first two taps in both the algorithms stay within ±0.005 of its average value over 10000 clock cycles. This was chosen as an empirical specification for steady-state. Adaptation was stopped after this time and error-rates were computed for both the algorithms (Figure 3.23). As seen in the Figure 3.23, use of sign-LMS with the ten-bit precision for coefficient update and six-bit precision for the feedback equalizer coefficients does not degrade the channel performance as compared to the original LMS algorithm on an infinite resolution channel.

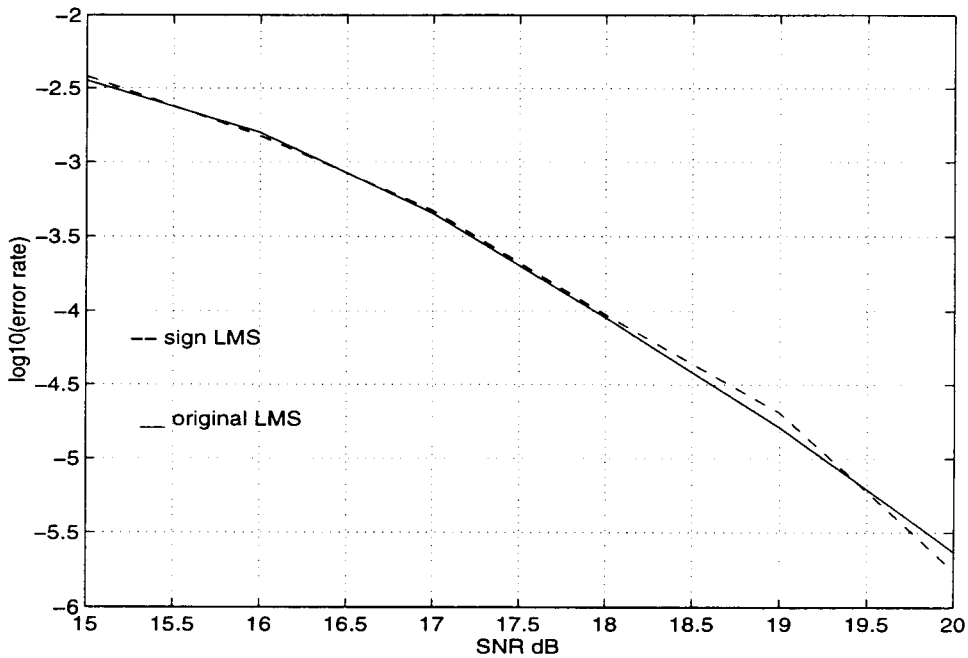


Figure 3.23 Impact of the two LMS algorithms on channel error-rates

Table 3.3 Feedback Equalizer coefficient values after adapting

Tail of equalized dibit	Values after adapting using the sign-LMS	Values after adapting using the original LMS
-0.2774	-0.2403	-0.2344
-0.8367	-0.8591	-0.8594
-0.8032	-0.8049	-0.7969
-0.6616	-0.6623	-0.6406
-0.5103	-0.5135	-0.5156
-0.3594	-0.3669	-0.3750
-0.2432	-0.2496	-0.2500
-0.1662	-0.1702	-0.1562
-0.1140	-0.1069	-0.0938

The precision constraints on the error introduced by the flash ADC does not affect this sign-LMS adaptation scheme. This is because the sign-LMS algorithm requires information only about the sign of the error and not its actual value and is an added advantage to approximating the original LMS by its sign version. Table 3.3 lists the coefficient values after adaptation along with the tail of the equalized dibit which specifies the response the equalizer has to adapt to at an user density of 2.5 PW50.

CHAPTER 4

CONCLUSIONS AND FUTURE WORK

4.1 Conclusions

The mixed-signal implementation of MDFE provides the advantages of low power, high speed and reliable operation at higher user densities. MDFE relies on the run length contraint of 1 which has been exploited fully to split the feedback sections into parallel operating paths thereby relaxing the increase in speed requirements imposed by the RLL code. The run length constraint has also resulted in simple timing, gain and adaptive feedback equalizer error detecting schemes with minimum increase in circuit complexity.

The flash ADC which partitions the continuous-time analog front end from the discrete-time, mixed-signal feedback end has been designed in a robust, easy to implement manner. The adaptive algorithms have been characterized with the impact of quantization. The performance of the adaptive loops which rely on the output of the flash ADC has been exhaustively analyzed in both the transient and steady-state channel conditions. A solution to the channel start-up problem has been provided and tested thoroughly to guarantee channel lock into steady-state. Bounds on the start-up errors have been clearly defined and quick acquisition into steady-state has been demostrated. The steady-state channel performance with the jitter introduced by the adaptive loops has also been verified. The system design has been done assuming a channel SNR of 20 dB and a user $PW50$ of 2.5.

4.2 Future Work

The flash ADC has introduced comparators in the system that add to the power dissipation. In order to reduce the number of comparators used by a factor of 50%, the flash ADC can be preceded by a full wave rectifier. A design technique has been outlined in Appendix B and can be included in a future implementation.

The feedback equalizer utilizes about 20 digital to analog convertors (DAC). Pooling the coefficient adaptation and time sharing the DACs can be investigated. The random access memory (RAM) architecture of the feedback equalizer can also be explored to deal with non-linear ISI effects which arise at high storage densities.

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APPENDICES

APPENDIX A

QUANTIZER DESIGN RESULTS

Table A.1 Optimal mid-tread uniform quantizer for a Gaussian source (zero mean, unit variance)

# of output levels L	Step-size Δ_{opt}
3	1.2240
5	0.8430
7	0.6508
9	0.5338
11	0.4546
13	0.3972
15	0.3534
17	0.3189
19	0.2909
21	0.2678
23	0.2482
25	0.2315
27	0.2171

From Proakis and Salehi, Prentice Hall Publishers, 1994

Table A.2 Optimal mid-tread non-uniform quantizer for a Gaussian source (zero mean, unit variance)

# of output levels L	input thresholds (to be translated to the other side of origin for the negative inner level)	output thresholds (to be translated to the other side of origin for the negative inner level)
3	0.6120	0, 1.2240
5	0.3823, 1.2444	0, 0.7646, 1.7242
7	0.2803, 0.8744, 1.6108	0, 0.5606, 1.1882, 2.0334
9	0.2218, 0.6812, 1.1976, 1.8655	0, 0.4436, 0.9188, 1.4764, 2.2547
11	0.1837, 0.5599, 0.9656, 1.4357, 2.0592	0, 0.3675, 0.7524, 1.1788, 1.6927, 2.4258
13	0.1569, 0.4760, 0.8126, 1.1841, 1.6229, 2.2145	0, 0.3138, 0.6383, 0.9870, 1.3813, 1.8645, 2.5645
15	0.1369, 0.4143, 0.7030, 1.0130, 1.3605, 1.7763, 2.3437	0, 0.2739, 0.5548, 0.8512, 1.1749, 1.5461, 2.0065, 2.6809
17	0.1215, 0.3670, 0.6201, 0.8875, 1.1783, 1.5077, 1.9057	0, 0.2430, 0.4909, 0.7493, 1.0256, 1.3309, 1.6845, 2.1270, 2.7808
19	0.1092, 0.3294, 0.5551, 0.7908, 1.0423, 1.3183, 1.6336	0, 0.2184, 0.4404, 0.6698, 0.9117, 1.1728, 1.4638, 1.8034, 2.2314, 2.8682
21	0.0992, 0.2989, 0.5027, 0.7137, 0.9360, 1.1752, 1.4395, 1.7433, 2.1154, 2.6345	0, 0.1984, 0.3994, 0.6059, 0.8215, 1.0506, 1.2998, 1.5793, 1.9074, 2.3233, 2.9457
23	0.0909, 0.2736, 0.4594, 0.6507, 0.8504, 1.0622, 1.2914, 1.5461, 1.8403, 2.2025, 2.7103	0, 0.1817, 0.3654, 0.5534, 0.7481, 0.9527, 1.1716, 1.4111, 1.6811, 1.9996, 2.4053, 3.0152
25	0.0838, 0.2522, 0.4231, 0.5982, 0.7797, 0.9702, 1.1734, 1.3943, 1.6410, 1.9271, 2.2807, 2.7787	0, 0.1676, 0.3368, 0.5093, 0.6870, 0.8723, 1.0681, 1.2786, 1.5100, 1.7720, 2.0823, 2.4792, 3.0782
27	0.0778, 0.2340, 0.3921, 0.5536, 0.7201, 0.8936, 1.0766, 1.2726, 1.4866, 1.7264, 2.0056, 2.3518, 2.8411	0, 0.1556, 0.3124, 0.4719, 0.6354, 0.8049, 0.9824, 1.1708, 1.3743, 1.5988, 2.1572, 2.5463, 3.1358

```
% OPTIMUM THRESHOLDS FOR THE FLASH ADC using Lloyd II algorithm

% L:      2L-1 is the # of output thresholds for flash ADC
% xl, xu: lower and upper bound on input signal
% stdev:  standard deviation of input signal
% ep, al: convergence parameters of the Lloyd II algorithm
  (all arguments are optional)

% Q = 0.5erfc(x/sqrt(2))
function[x,y] = lm(L,xl,xu,stdev,ep,al)
if nargin == 0
  L = 3;
  xl = 0;
  xu_init = 3.0;
  xu = inf;
  stdev = 0.45;
  ep = 0.000001;
  al = 0.00001;
end
if nargin == 1
  xl = 0;
  xu = inf;
  xu_init = 3.0;
  stdev = 0.45;
  ep = 0.000001;
  al = 0.00001;
end
err = 0.1;
for k = 1:L-1
  x(k) = xu_init/L*k;
end
iter = 1;
while err > ep
  y(1) = 0;
  for k = 2:L-1
    y(k) = centroid(x(k),x(k-1));
  end
  y(L) = centroid(x(L-1),xu);
  for k = 1:L-1
    x(k) = (y(k) + y(k+1))/2;
  end
  c = centroid(x(L-1),xu);
  err = c-y(L);
  err = err*sign(err);
  y(L) = y(L)-(al*err);
  iter = iter+1;
end
```

```
function[c] = centroid(xl,xu)
 % function to compute the centroid of a Gaussian pdf, called by lm.m
tl = xl^2/2;  tu = xu^2/2;  num =  1/((2*pi)^(0.5))*(exp(-tl) - exp(-tu));
denom = 0.5*erfc(xl/2^(0.5)) - 0.5*erfc(xu/2^(0.5));   c = num/denom;
```

APPENDIX B

DESIGN OF THE FULL WAVE RECTIFIER

B.1 Design Approach

The purpose of performing full wave rectification on the equalized signal in MDFE is to achieve a 50% reduction in the number of comparators used by the flash ADC. A full wave rectifier can be realized using two differential transistor pairs as shown in Figure B.1. As the outputs are taken from transistors in the source follower configuration, the use of Pmos input transistors avoids problems due to back gate effect that cannot be overcome in Nmos transistors. The principle of operation is to use one differential pair (diff-pair) to find the common mode voltage of the input signal, and the second diff-pair to pick out the negative going differential input signal. When this negative going output is measured with respect to the common mode signal, a full wave rectified signal is obtained. The resistors connected to the output of the first diff-pair average the differential input signal to compute the common mode voltage.

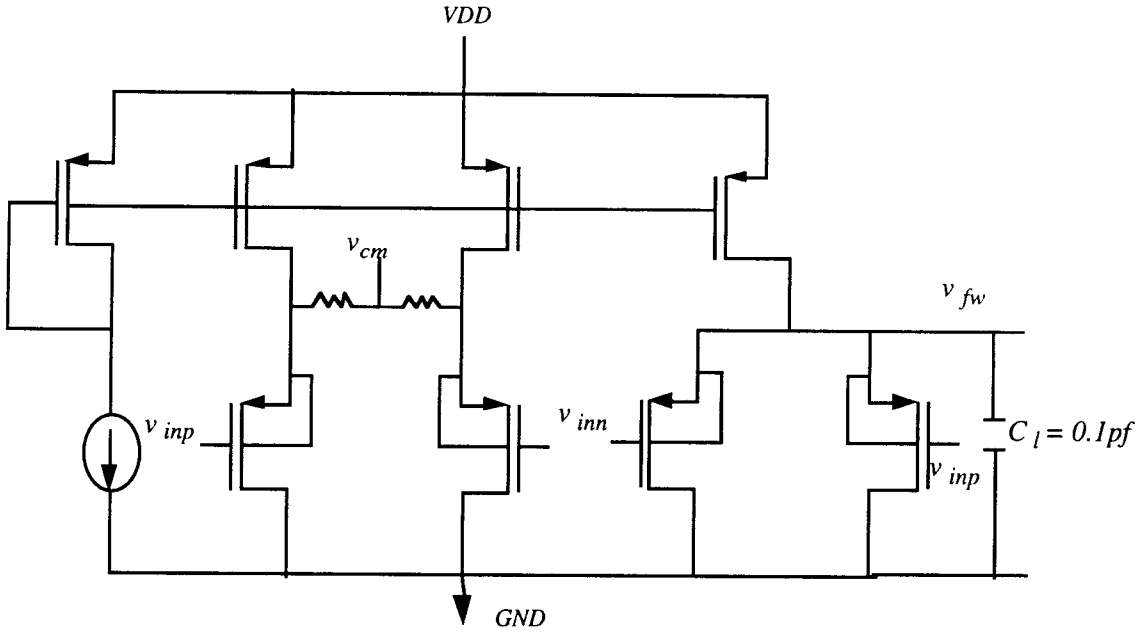

Figure B.1 Full Wave Rectifier

B.2 Results

Due to the symmetry of the circuit, all transistors are of the same size except for the tail current source of the second diff-pair which has to be twice as large to source the same current as into the first diff-pair. The value of the resistors was chosen as 20K to give sufficient linearity in the common mode signal. The voltage power source dissipation of this circuit was 2.3 mW. The simulations performed on this circuit were: (i) the dc transfer characteristic (Figure B.2), (ii) transient response to a sine wave input (Figure B.3), and (iii) transient response to a pulse input (Figure B.4). The results in Figures B.2, B.3 and B.4 show the circuit performance for three different conditions of the 1.2 micron, CMOS n-well process: the nominal(0), fast(1) and slow(2). Two signals are shown in each of the results and referred to Figure B.1, they are: (i) the input signal to the diff-pair with the common mode voltage voltage removed referred to as *vsw* ($vsw = v_{inp} - v_{cm}$) and (ii) the full wave rectified signal referred to as *v(vcm-vfw)* which represents the output of the second diff-pair with respect to the common mode voltage ($v_{cm} - v_{fw}$).

As anticipated, the dc transfer curve in Figure B.2 illustrates the dc level shift inherent to a MOS source follower (for a PMOS source follower the dc shift is positive and given by $v_{sg} = v_t + v_{dsat}$) . As the output voltage of this diff-pair is measured with respect to the common mode voltage, this proposed circuit for full wave rectification will always be smaller than the input signal amplitude by a value of v_{dsat}. As the amplitude loss is approximately 20% of the input voltage, the step size in the flash ADC decreases by the same factor. Hence this increases the resolution requirements of the comparators in the flash ADC which follows the full wave rectifier in the MDFE system.

From the transient response results shown in Figures B.3 and B.4, the rise time is within 2ns, and the circuit introduces non-linearities. Linearity is an important consideration to the feedback equalizer as it implements a linear impulse response. But the signal from the full wave rectifier is used only by the slicer and the input to the timing and gain recovery control sections. As was analyzed in detail in Chapter 3, the stochastic

gradient descent scheme used by the timing and gain recovery loops are robust to non-linearities and hence this issue does not raise a significant concern. One other issue of concern in this circuit is the threshold voltage mismatches that can arise between the transistors of each diff-pair. This adds to the dc offsets due to all the analog components existing in the system. The feedback equalizer has a tap to adapt and cancel these errors as was illustrated in Chapter 3.

B.3 Alternate full wave rectifier

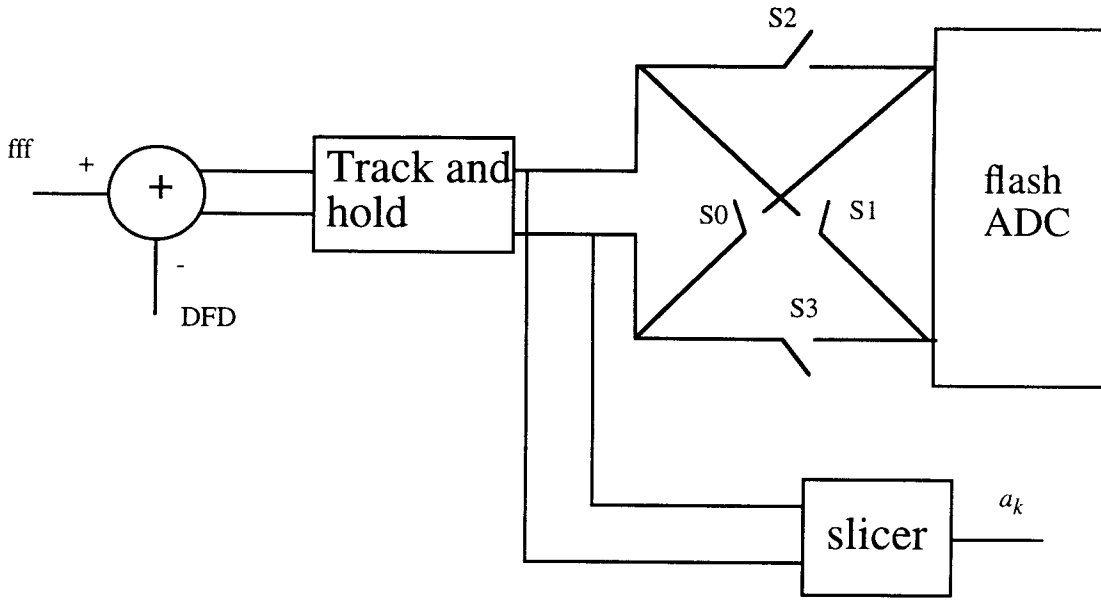

Figure B.5 Rectification without amplitude loss

Figure B.5 proposes a scheme to perform full wave rectification without loss of amplitude. The differential signal from the output of the summing node for each feedback path enters a track and hold before the slicer uses it to make a decision. The decision from the slicer can be used to close switches S2, S3 and open switches S0, S1 if $a_k = 1$ thereby rectifying the differential equalized signal. If $a_k = 0$, the reverse is done i.e., switches S0, S1 are closed and S2, S3 are opened.

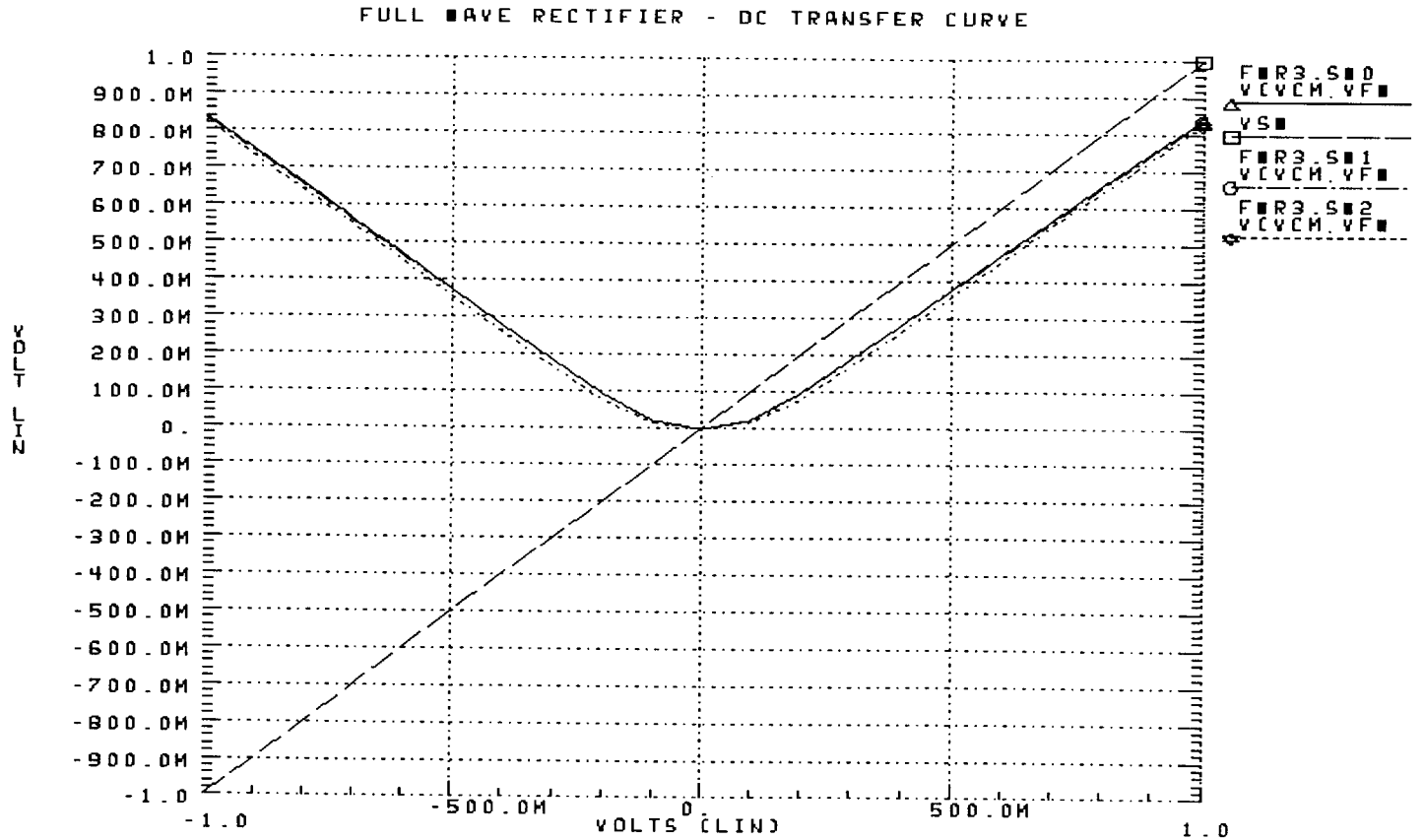

Figure B.2 DC Transfer curve of full-wave rectifier

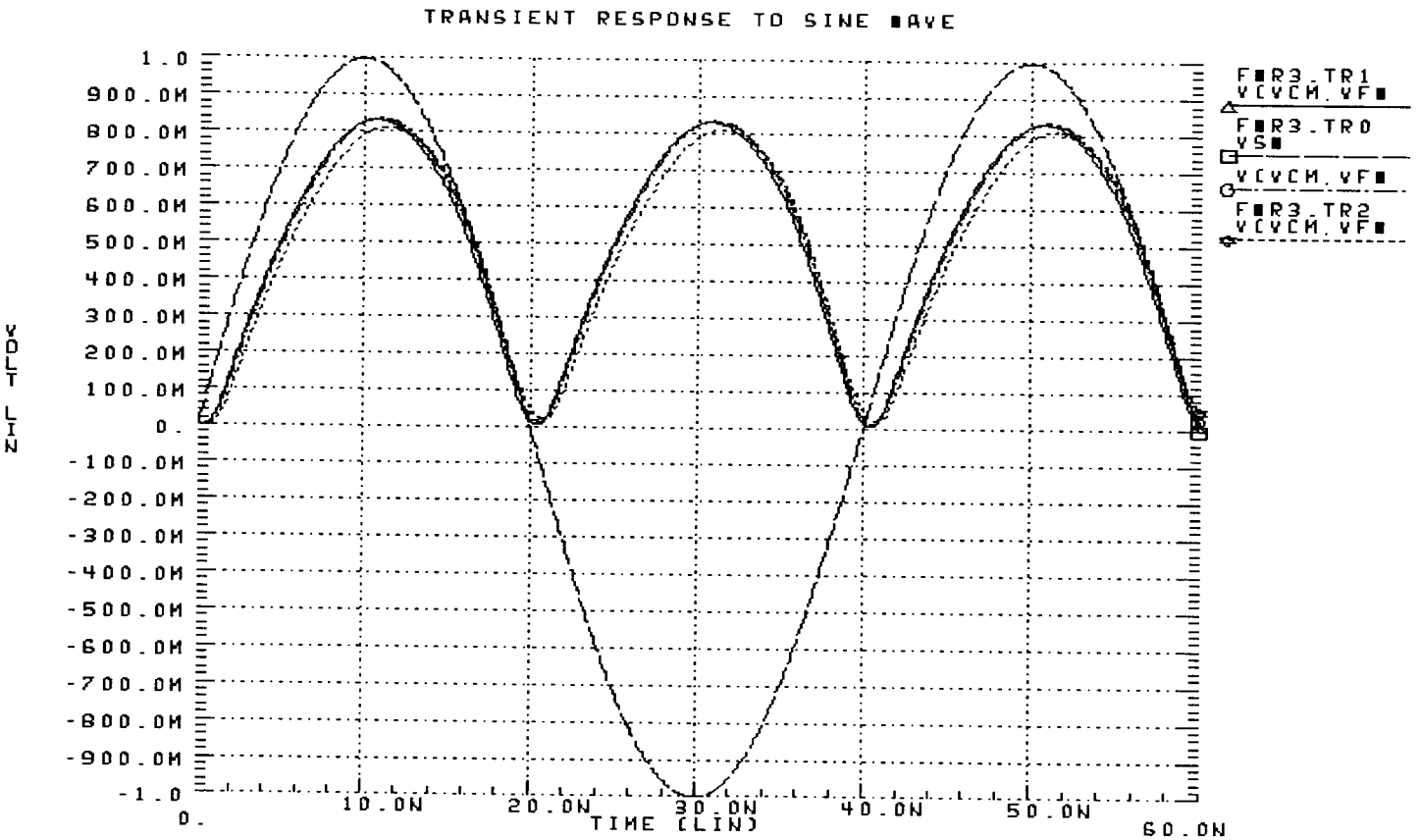

Figure B.3 Full wave rectifier: Transient response to a sine wave input

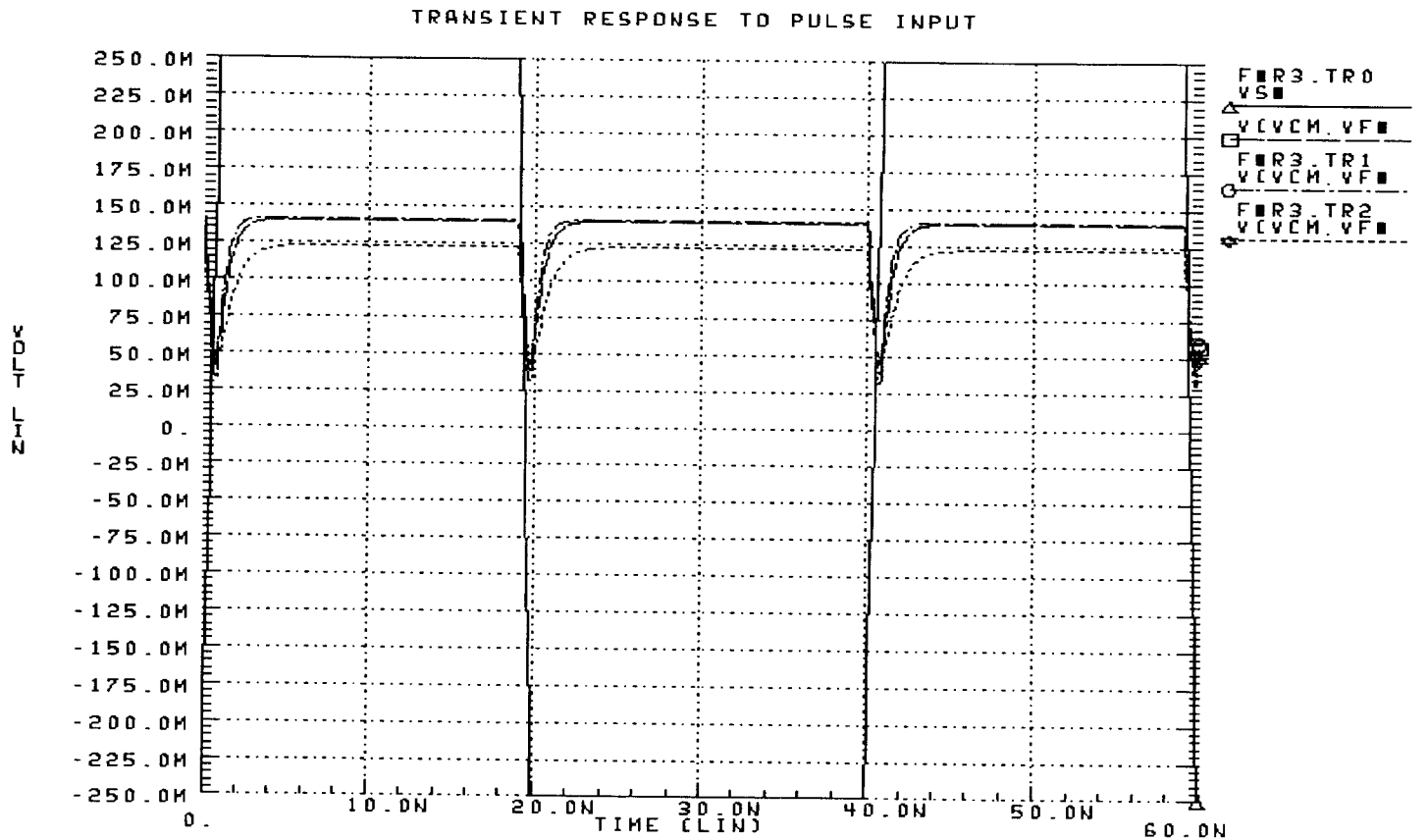

Figure B.4 Full wave rectifier: Transient response to a pulse input