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A current-mode concept for digital integrated circuit design is introduced and is called Switched-Current (SI) Logic. This concept enhances high-performance mixed-mode IC design by reducing power supply noise spikes. The speed of operation is comparable with static CMOS logic gates.

The basic building blocks of digital design are developed and categorized. The operation of these gates, the sources of noise spikes, concepts of noise margin and gate propagation delay are some of the aspects that are investigated. To test the practicality of this method representative digital circuits including a carry look-ahead adder are designed and fabricated in a 2-μm p-well CMOS process. Simulation results show that this technique reduces the associated power supply noise spikes by approximately two orders in comparison to standard static CMOS logic. The power supply noise spikes were measured to be about 15 μA with a gate delay 0.6 ns for a bias current I = 100 μA.

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LIST OF SYMBOLS

K_n	Transconductance of NMOS, μA/V
K_p	Transconductance of PMOS, μA/V
L	Lenth of MOSFET, μ
W	Width of MOSFET, μ
V	Voltage, volts
C_{xx}	Capacitance in fFarad
V_{xx}	Voltage of MOSFET, volts, where x= d = drain s = source g = gate b = bulk
V_T	Threshold voltage, volts
λ	Channel-length modulation, volts
Θ	exclusive-OR
I	Current, A

SWITCHED-CURRENT LOGIC FOR DIGITAL CIRCUIT DESIGN

1. INTRODUCTION

With the improvements in Integrated Circuit (IC) fabrication technology, the integration of electronic circuitry has increased dramatically. A chip that once contained a few hundred transistors may now contain as many as a million or more transistors, with prospects for a billion transistors at the beginning of the next millennium.

In the beginning of this era of Large Scale Integration in the 1960's, the emphasis was on bipolar analog integrated circuits. After the invention of the microprocessor in the late 1970's, there was an explosion of interest in digital IC's fabricated in Metal Oxide Semiconductor (MOS) technology. In recent years, mixed-mode IC's containing both analog and digital circuitry have emerged for system integration applications. Interestingly, technology has also advanced to incorporate both bipolar and MOS capabilities, i.e. BiCMOS technologies.

Advancements have also occurred in the scaling of technologies and the shrinking of the minimum sizes of transistors, accompanied by higher performance processing parameters, reduction in power supply voltages, etc. [1]. These technology changes have necessitated new analog and digital design techniques. For example, noise spikes generated by the switching of MOSFET's in conventional static CMOS digital circuits are propagated to the analog side in a mixed-mode IC and may degrade the performance of the analog circuitry [2]. Due to this noise, there is presently an upper limit on the accuracy of mixed-mode integrated systems.

As mentioned earlier, the advances in IC technology allowing mixed-mode systems have created a need for new logic families that significantly reduce the power

supply noise generation of conventional CMOS static voltage-mode circuits [3]. Though static CMOS logic offers high performance with low static power, high functional manufacturing yield and easy scalability to smaller device sizes, it typically generates power supply noise spikes as large as 1 mA/gate. On a chip where many thousands of transistors may switch synchronously, very large spikes may occur.

To circumvent the problem of noise propagation in mixed-mode IC's, several techniques have been developed. Good layout techniques such as using separate analog and digital power supply lines and minimizing their common impedances are somewhat effective. The use of diffused guard rings to shield noise from analog circuitry is also beneficial.

Statistics show that digital MOS IC's currently dominate and will continue to dominate the IC market. Previously, the of operation of static CMOS logic circuits has been in the voltage-mode domain. In this thesis, digital circuits that work in the current domain are presented. A new concept for digital circuit design is introduced called Switched-Current (SI) Logic. The traditional voltage levels for digital logic high or "1" and logic low or "0", are replaced by current levels. The gates operate with a constant current source and hence there are ideally no noise spikes generated. This SI logic technique increases the performance of digital circuits over those that are voltage controlled. The technique is especially intended for high performance mixed-mode applications.

In chapter 2 the basic building blocks of this new logic family, the SI INVERTER and the SI NOR gate are introduced. This chapter also deals with the issues of maximum fanout and input/output buffers. The translators that convert from voltage to current and vice versa are necessary to make SI compatible to the existing CMOS logic families. Chapter 3 discusses the characteristics of the logic gates

including propagation gate delays, maximum speed and power supply noise spikes. Chapter 4 considers the practical implementation of SI logic in both combinational and sequential digital circuits. Several new SI circuit blocks are described and fabricated. In order to predict the viability of SI for the future, Chapter 5 considers the performance of SI with scaled CMOS technologies using two standard scaling laws - constant voltage (CV) and constant electric field (CE).

2. THE SWITCHED-CURRENT (SI) LOGIC

On-chip digital logic levels have been traditionally defined by voltages. Using a positive logic convention, a high voltage denotes a logic high or "1" and a low voltage denotes a logic low or "0". In the switched-current (SI) technique, the logic levels are defined in terms of currents and are ideally independent of the voltage levels. Thus, if a branch has a high flow of current, it is termed as I_H or a logic "1" state, and if it has a low flow of current, it is called I_L or the logic "0" state.

2.1 A Current Mirror

Before considering the SI logic circuits, the simple current mirror is first reviewed as it is an essential building block of this logic technique. The concept of current mirroring is as literal as its name. Designers of bipolar and CMOS analog and digital circuits often make use of this essential technique.

The basic idea is to replicate the current flowing in a particular branch to other branches in a circuit. Figure 2.1 shows an NMOS implementation of a simple current mirror. M1 is diode-connected and operates in the square-law saturation region when biased with a current I as shown. M1 performs a current-to-voltage conversion on I resulting in [4]

$$V_{GS} = V_{T1} + \sqrt{\frac{2I}{K_n(W/L)_1}} \tag{2.1}$$

The gate of M2 is driven by V_{GS} resulting in a current of

$$I_2 = \left(\frac{K_n}{2}\right)\left(\frac{W}{L}\right)_2\left(V_{GS} - V_{T2}\right)^2 \tag{2.2}$$

if M2 is in saturation for $V_{DS2} > (V_{GS} - V_{T2})$ and a current of

$$I_2 = K_n\left(\frac{W}{L}\right)_2\left[\left(V_{GS} - V_{T2}\right)V_{DS2} - \left(\frac{V_{DS2}^2}{2}\right)\right] \tag{2.3}$$

if M2 is in non-saturation $V_{DS2} < (V_{GS} - V_{T2})$. The output I-V characteristic of the simple current mirror obtained from (2.2) and (2.3) is shown in Fig. 2.2. Assuming that $L_1 = L_2$ and M1 and M2 are both saturated,

$$I_2 = \left(\frac{W_2}{W_1}\right)I \tag{2.4}$$

By varying the ratio of the widths of the transistors, the desired current can be generated with respect to the bias current I flowing into M1.

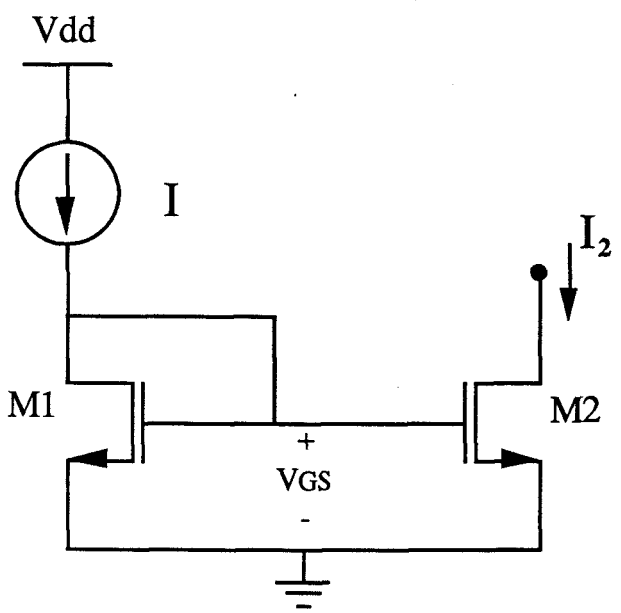


Figure 2.1 A simple current mirror.

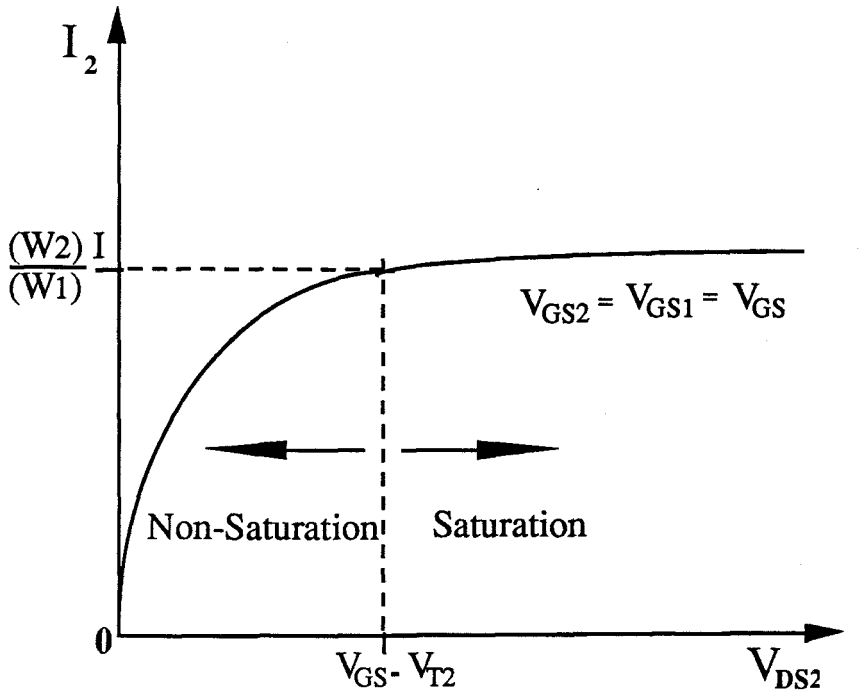


Figure 2.2 Transfer characteristics of a current mirror; $L_1=L_2$.

2.2 The SI Logic Inverter

The inverter is the basic building block for all digital circuits. Figure 2.3 shows a schematic of an SI inverter consisting of M1, M2 and M3 with the corresponding current-mode truth table given in Table 2.1. Recall that I_H represents a logic "1" and I_L a logic "0" and that M3 realizes the constant current source I. Simulated input and output current waveforms are shown in Fig. 2.4, for the SI inverter of Fig. 2.3 assumed driving the input of an identical stage.

INPUT I_{IN1}	OUTPUT I_{OUT}
I_H	I_L
I_L	I_H

Table 2.1 Truth table of an SI current-mode inverter.

At t=0, $I_{IN} = I_H$ and M1 and M2 are both conducting. Hence $I_{OUT} = I_L = 0$ flows into the diode-connected input of the next stage. When $I_{IN}(t)$ changes to I_L, both M1 and M2 turn off and the output current flowing into the input of the next stage increases to $I_H = I$ as shown in Fig. 2.4. Note that I_H is slightly less than I due to channel-length modulation effects of the PMOS current source. If necessary, this effect can be eliminated by replacing M3 by a cascode PMOS current source. A 2-μm p-well CMOS process parameters were used for all the simulation results presented in this thesis.

As mentioned earlier, mirroring produces equal currents if the transistors are identical including their voltages, K factors and dimensions W and L. In practice this does not occur and hence M2 must be made bigger than M1 to achieve current gain to compensate for possible errors, and to provide a sufficient noise margin.

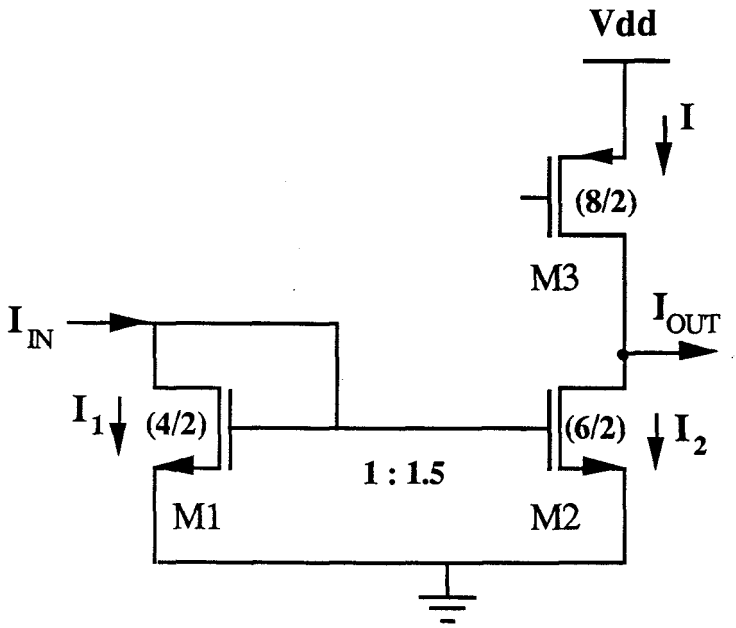


Figure 2.3 A switched-current (SI) inverter.

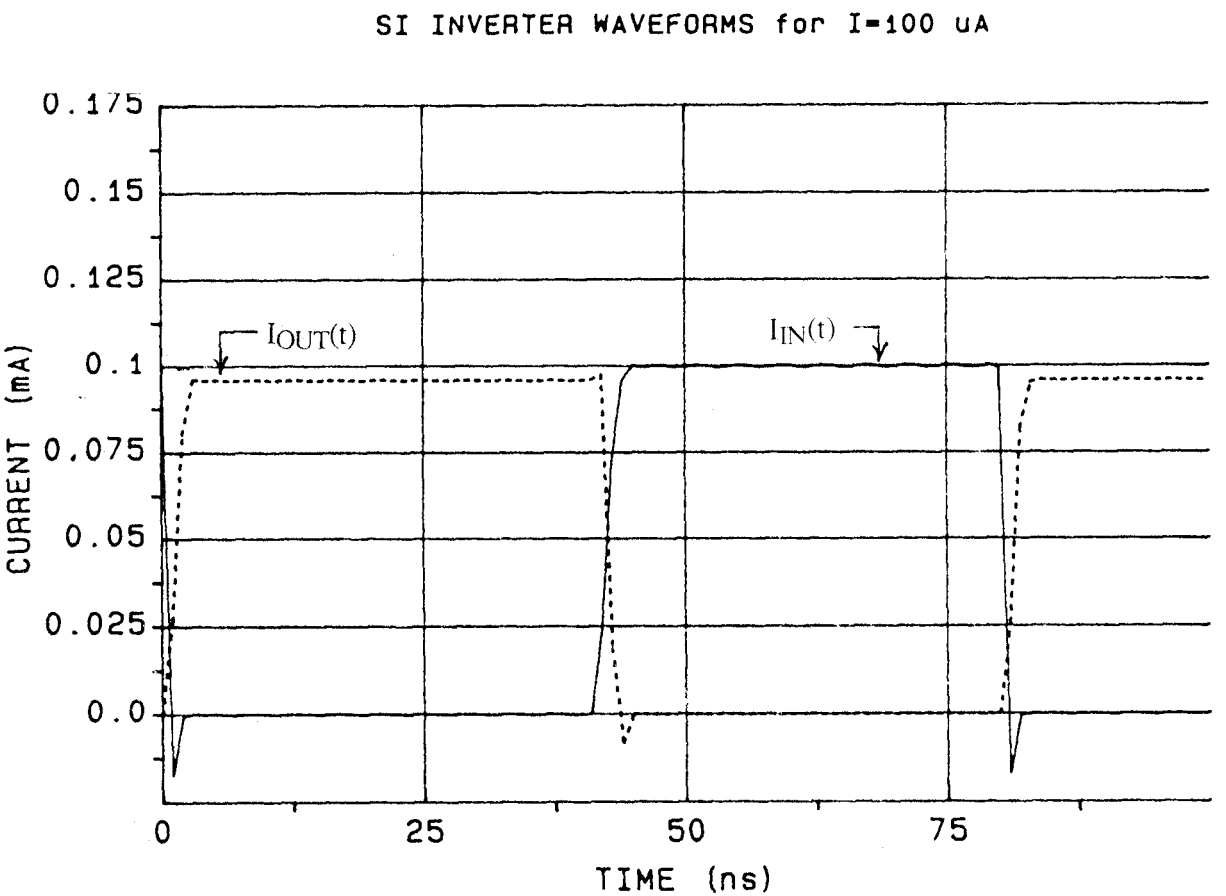


Figure 2.4 The simulated input and output waveforms of a SI inverter for I = 100 μA.

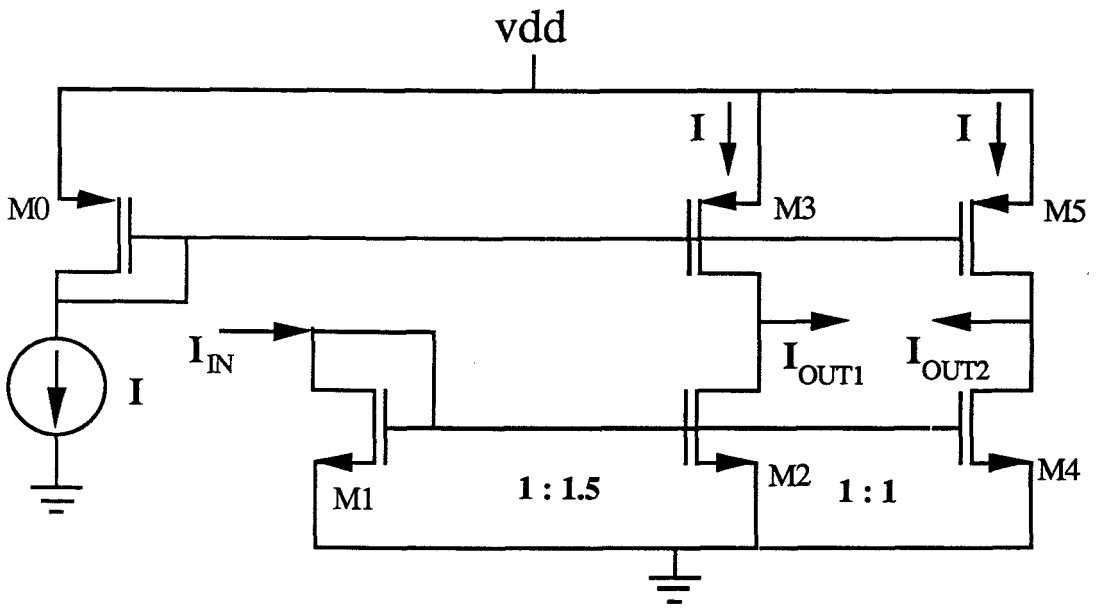


Figure 2.5 A practical implementation of a SI inverter with fanout = 2.

The current sources shown in Fig. 2.5 are implemented using simple PMOS and NMOS current mirrors. The circuit shown is a practical realization of a SI inverter with fanout of two. Unlike static CMOS logic or other voltage-mode circuits where multiple fanouts are driven from the same point, an extra output stage (represented by transistors M4 and M5) is required for each additional fanout with current-mode SI logic. $I_{OUT1} = I_{OUT2}$ is obtained when

$$\left(\frac{W}{L}\right)_5 = \left(\frac{W}{L}\right)_3 \text{ and } \left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_2 \tag{2.5}$$

2.3 The SI Logic NOR

The SI NOR gate is an extension of the SI inverter. Figure 2.6 illustrates the schematic of a two input NOR gate with a fanout capability of one. The operation of

this circuit is similar to that of the SI inverter just discussed. When the inputs I_{IN1} and I_{IN2} are both high, pushing currents $I_H = I$ into M1 and M5 respectfully, then M1, M2, M4 and M5 all turn on. Hence, the bias current I splits evenly between M2 and M4. Thus, the output current is designed to be zero to ensure that the subsequent stage is turned off. If there are "n" input NOR stages and all of them turn on, then the bias current splits into I/n. In the worst case, the circuit is designed so that even if only one input is high then the output current is still zero. Only when all the inputs are low do all of the transistors turn off allowing the output to attain the high level, I_H. An arbitrary number of inputs can be added to the NOR gate, although as mentioned before, each fanout requires an additional output branch.

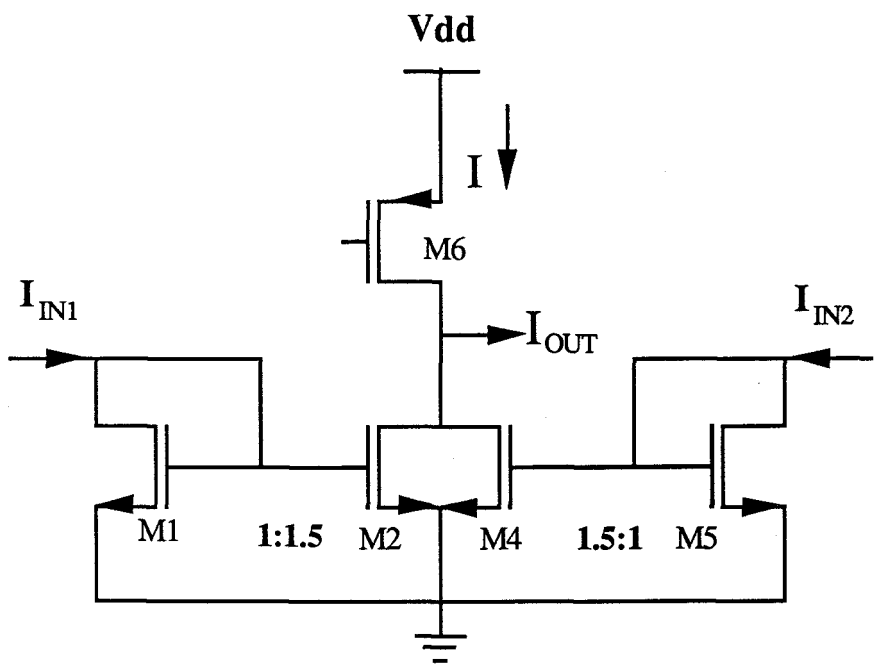


Figure 2.6 A two-input SI logic NOR gate with fanout = 1.

I_{IN1}	I_{IN2}	I_{OUT}
I_L	I_L	I_H
I_L	I_H	I_L
I_H	I_H	I_L
I_H	I_L	I_L

Table 2.2 Truth table of a two-input SI logic NOR gate.

Table 2.2 gives the truth table of a two-input SI logic NOR gate. A suitable technique for realizing NAND gates with SI logic has not yet been found, although it is not needed as a NOR gate is a logically complete set.

2.4 The Input V-I and Output I-V Translators

The current-steering logic circuits discussed so far are intended strictly for on-chip applications as they have their inputs and outputs in terms of currents. In practice, these circuits interface to existing logic families such as CMOS static logic, and thus there is a need for converting from current-to-voltage and vice-versa.

2.4.1 The Input Voltage-to-Current Converter

Figure 2.7 shows the schematic of a simple input V-I converter. When the input V_{IN} is less than V_{T1}, M1 is off and the current available at the output to flow into the next stage is I. Similarly when $V_{IN} > V_{T1}$(e.g., V_{IN} = Vdd), then M1 is on and designed so that all of the bias current I flows to ground, and $I_{OUT} = 0$. The truth table for the V-I

translator is shown in Table 2.3.

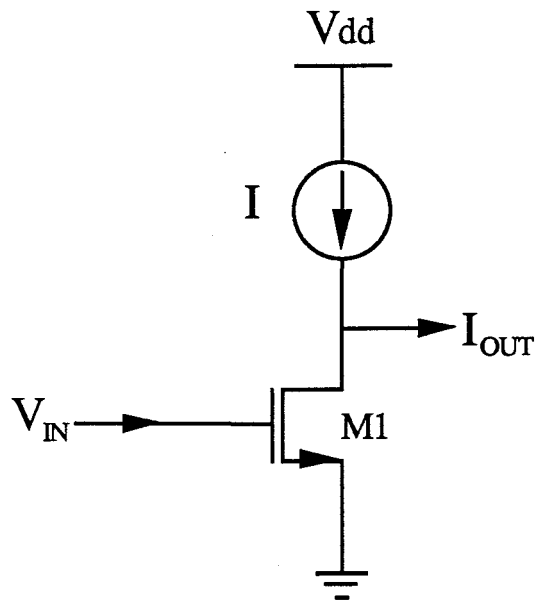


Figure 2.7 A simple input voltage-to-current translator.

INPUT V_{IN}	OUTPUT I_{OUT}
V_{IH}	I_L
V_{IL}	I_H

Table 2.3 Truth table for an input voltage-to-current translator.

2.4.2 The Output Current-to-Voltage Converter

Figure 2.8 shows the schematic of one possible simple output I-V converter. M3 is biased with a multiple of I similar to a standard SI inverter. When $I_{IN} = I_L$, M2 is turned off, and M3 charges the output capacitive load, C_L, to the power supply voltage. When $I_{IN} = I_H$, M1 and M2 are on, and M2 and M3 are properly ratioed so that the voltage at the output node is low, V_{OL}. The truth table is shown in Table 2.4.

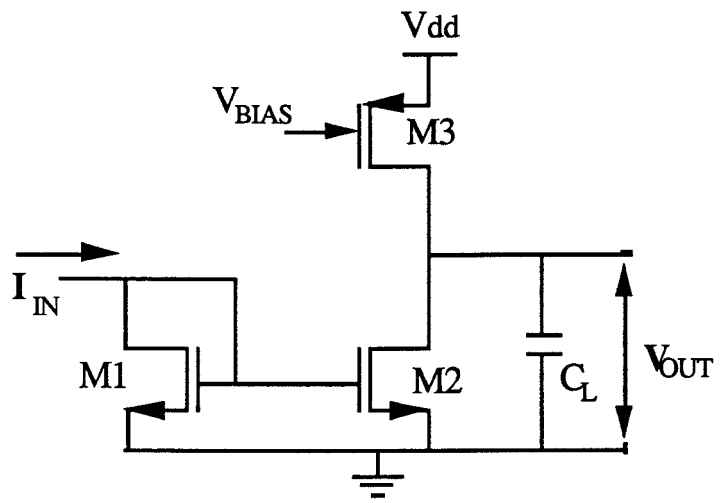


Figure 2.8 A simple output current-to-voltage translator.

INPUT I_{IN}	OUTPUT V_{OUT}
I_H	V_{OL}
I_L	V_{DD}

Table 2.4 Truth table for an output current-to-voltage translator.

2.5 Input/Output Buffers

The input and output variables of SI logic are current signals. In a practical IC design, the voltage outputs of the on-chip gates are connected to IC package pins loaded with large capacitances greater than 10-15 pF. The output stage with such external loading often limits the speed of the overall circuit. Hence, practical output buffers are used which are a series of tapered CMOS gates cascaded together. Size tapering is done to reduce the loading effect of the pin capacitance and to minimize the total load driven by the internal gates. From practical experience, it appears best to include an I-V

translator preceding the tapered buffer to ensure a full logic voltage swing at the output as shown in Fig. 2.9.

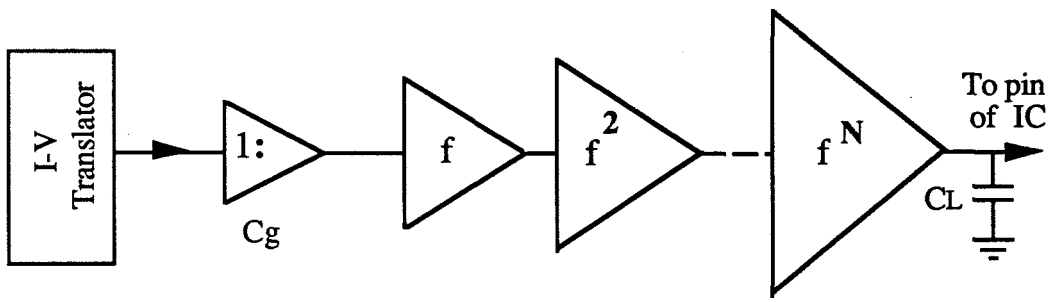


Figure 2.9 A tapered buffer design to reduce the loading effect of pin capacitance.

The buffer is designed by using the following approach. Denote the gate capacitance of the minimum sized inverter as C_G and the load capacitance as C_L. Now

let $y = C_L / C_G$ (2.6)

and $y = f^N$ (2.7)

where N = number of stages and f = e = 2.313 is the optimum upscale factor [5]. Starting with the minimum sized inverter, the (W/L) ratios of the subsequent stages are scaled up by multiplicative factors of f as shown in Fig. 2.9.

3. PERFORMANCE ANALYSIS OF SI LOGIC CIRCUITS

In this chapter, the power supply noise spike generation and speed characteristics of SI logic gates are considered. It is shown that SI logic has a significant advantage over conventional static CMOS logic families in terms of power supply noise generation. This key advantage may be especially important in high-performance mixed-mode applications.

3.1 Power Supply Noise Spikes

Power supply noise is an unwanted signal in the form of a voltage or current that causes deviations from ideal behavior. Noise can originate at the inputs or be generated in the power supply or in the ground lines due to the switching of logic gates.

With the increasing emphasis on combining high-performance analog with high speed digital circuits on the same chip, and with experience that the accuracy of such analog circuits is currently limited by power supply noise, considerable work is going into reducing or eliminating power supply noise. The SI logic technique reduces power supply noise by nearly two orders of magnitude.

In conventional CMOS digital circuits, overlap current pulses are caused by the switching of transistors, and result in power supply and ground noise. Consider the case in static CMOS circuits where the power supply noise spike from a gate could measure as large as 1 mA. On an integrated chip with many thousands of transistors which may be switching synchronously, the total power supply noise spike may be very large. When this happens, the analog circuitry sees this as power supply noise which degrades its performance [6].

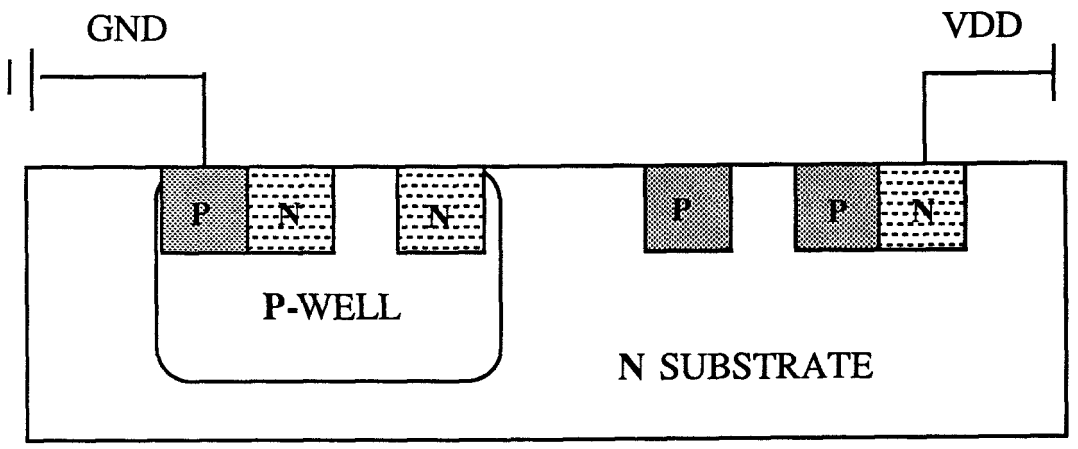


Figure 3.1 A static CMOS inverter in p-well technology.

Figure 3.1 shows a cross-sectional view of a static CMOS inverter. Note that the implementation is in a p-well CMOS technology and hence there is sharing of the common N-type substrate between the analog and digital circuitry. To ensure that latch-up does not occur, the digital power supply Vdd is locally tied to the substrate within each of the digital cells, and the p-wells are connected to ground. Hence, noise generated on the digital power supply (Vdd) lines is directly coupled into and propagated throughout the N-substrate.

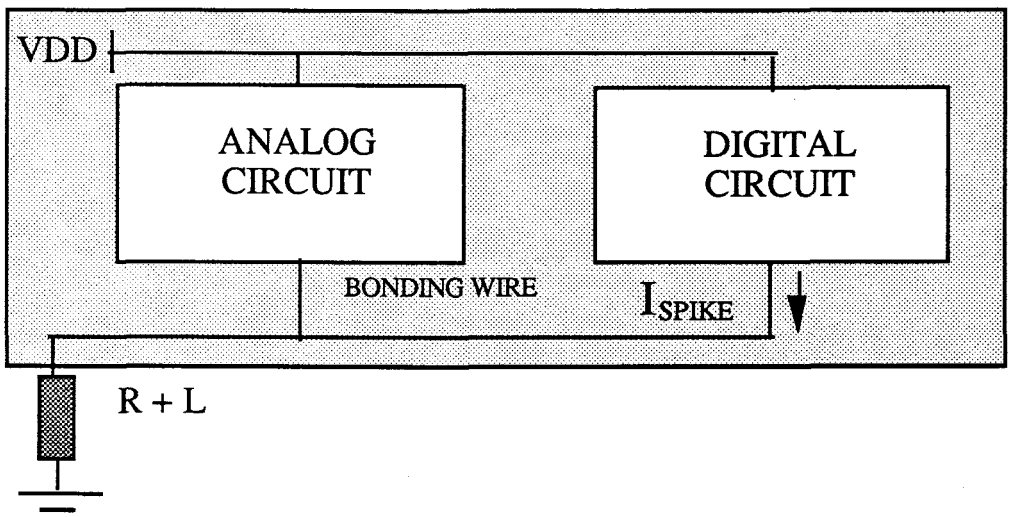


Figure 3.2 A top view of the basic layout of a mixed-mode IC.

Figure 3.2 shows a top view of the layout of a typical mixed-mode chip. The power supply noise due to a power supply current spike, I_{SPIKE}, is given by

$$V_{NOISE} \cong R\, I_{SPIKE} + L \frac{dI_{SPIKE}}{dt} \tag{3.1}$$

Noise spikes directly affect the accuracy of the analog circuitry because the noise is coupled to the analog from the digital part due to the common power supply impedance and the common substrate. The common power supply impedance is minimized by using separate on-chip analog and digital power supply and ground lines and pins.

The main advantage of SI logic is that by using constant current sources, the power supply current is ideally constant and theoretically there is no power supply noise. The non-ideal sources of noise generation are now analyzed. Figure 3.3 shows a pair of SI logic inverters. M3 operates in the saturation region and the current flowing through it is given by

$$I_3 = \left(\frac{K_p}{2}\right)\left(\frac{W}{L}\right)_3 \left(V_{SG3} + V_{T3}\right)^2 \left(1 + \lambda V_{sd3}\right) \tag{3.2}$$

The voltage change at the output node which results in a change in current flowing through M3 is about 1V. Due to the channel-modulation effect the change in current I_3 with respect to V_{ds3} is given by

$$\frac{\partial I_3}{\partial V_{sd3}} = \lambda \left(\frac{K_p}{2}\right)\left(\frac{W}{L}\right)_3 \left(V_{SG3} + V_{T3}\right) \tag{3.3}$$

which is represented as I (λ ΔV). This is the square wave part of the measured power supply noise in Fig. 4.6.

The power supply noise is also caused by the displacement current. The change in the output voltage due to the turn-on and turn-off of diode M4 causes the supply capacitance C_{dd} to charge and discharge. C_{dd} is the capacitance between the power supply and the output node as shown in Fig. 3.3. The change in the output voltage is given by

$$\frac{dV}{dt} = \frac{I}{C_{TOT}} \tag{3.4}$$

where C_{TOT} is the total capacitance at the output node equal to $C_{db2} + C_{gd2} + C_{db3} + C_{gd3} + C_{gb4} + C_{db4} + C_{gs4} + C_{gs5} + C_{gb5} + C_{gd5}$. The power supply displacement current is then given by

$$I_{dd} = C_{dd}\frac{dV}{dt} = C_{dd}\frac{I}{C_{TOT}} \tag{3.5}$$

where neglecting interconnect capacitances, $C_{dd} = C_{db3}$. This is the spike that is seen the in the measured power supply noise in Fig. 4.6.

In a similar way the gate capacitors in M1 and M2 are also charged and discharged to generate noise that in this case flows into ground. This noise spike is given by

$$I_{GND} = \left(C_{db2} + C_{gs4} + C_{gb4} + C_{db4} + C_{gs5} + C_{gb5} \right) \frac{dV}{dt} \qquad (3.6)$$

where the dominant capacitances, C_{gs1} and C_{gs2} are the gate capacitances of M1 and M2. Thus,

$$I_{GND} \cong \left(C_{gs1} + C_{gs2} \right) \frac{I}{C_{TOT}} \qquad (3.7)$$

The ground spike is typically larger than the Vdd power supply spike. However, in a p-well CMOS technology, the wells are isolated from the substrate which is common to the analog circuitry and hence, ground noise does not affect the performance of the analog circuit provided separate analog and digital ground lines are used. It is also assumed that the preceding stage is turned off instantly which is not the case. Hence all the current does not flow immediately into the input node and charge up the capacitances. The result of a simulation for a bias current of 100 μA is shown in Fig. 3.4. From the graph it can be seen that the power supply spike is about 15 μA. Compare this to the 1 mA spike that is obtained from switching a CMOS inverter and a reduction in magnitude by a factor of 70 is achieved. The ground spike is found to be about 40 μA.

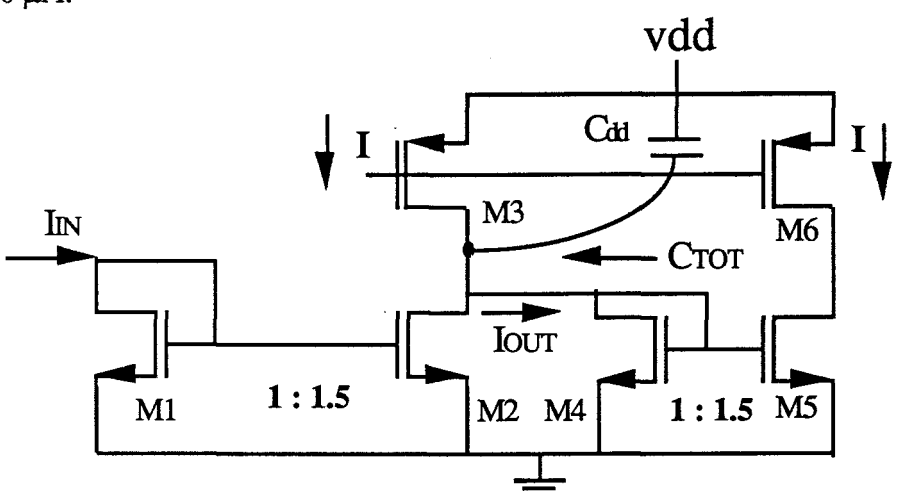


Figure 3.3 Circuit to analyze the sources of noise generation in SI logic.

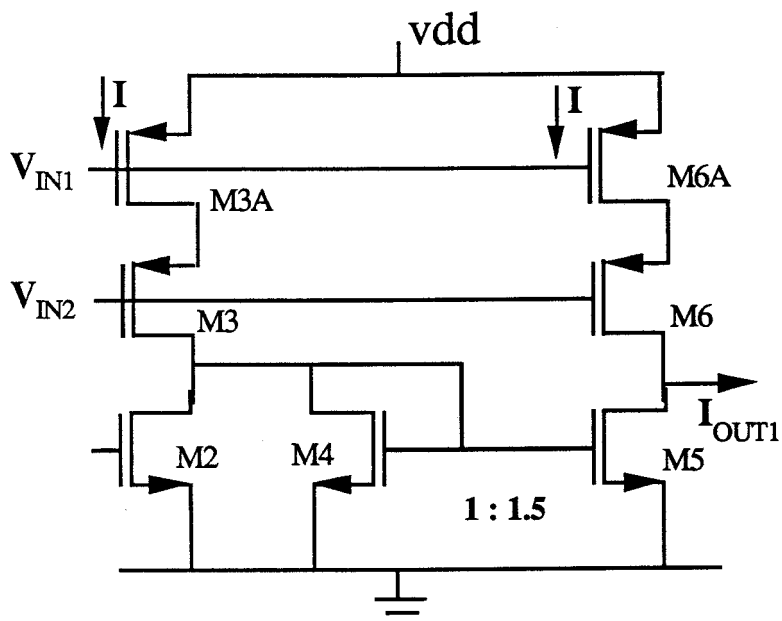


Figure 3.3.b A SI inverter with PMOS cascode current sources.

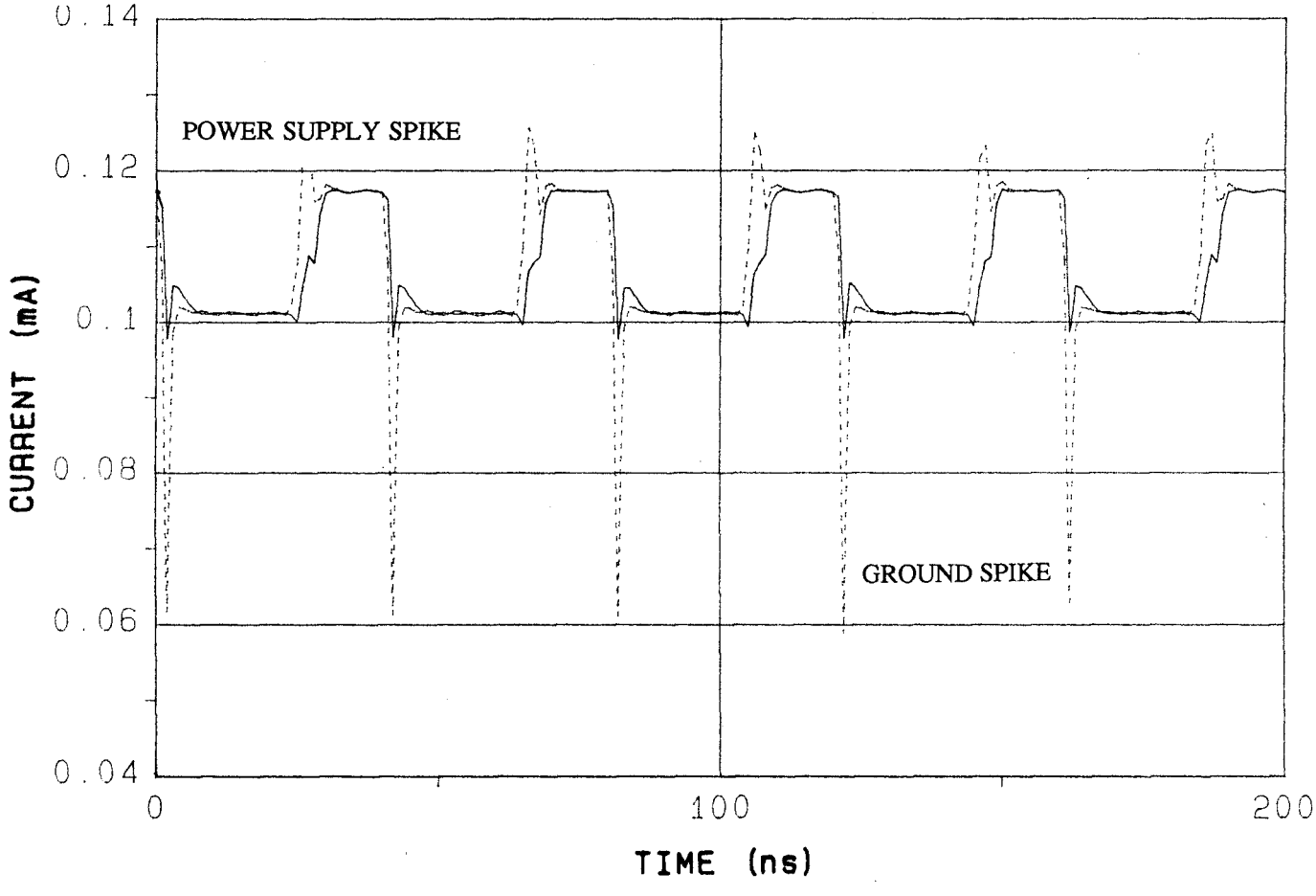


Figure 3.4 The simulated noise spikes of both ground and power supply for I = 100 μA.

3.2 Noise Margin

Large noise signals cause logic errors. However, if the noise amplitude at the input of any logic circuit is smaller than a specified magnitude known as the "noise margin", it is attenuated. Noise margins are defined as the ranges between which the circuit does not mistake noise for a valid input signal; they are important properties of any logic circuit. Due to their regenerative nature, noise in digital circuits does not accumulate from one stage to the next which is a distinct advantage over analog [7]. The transfer characteristic of a voltage driven static CMOS inverter is shown in Fig. 3.5.

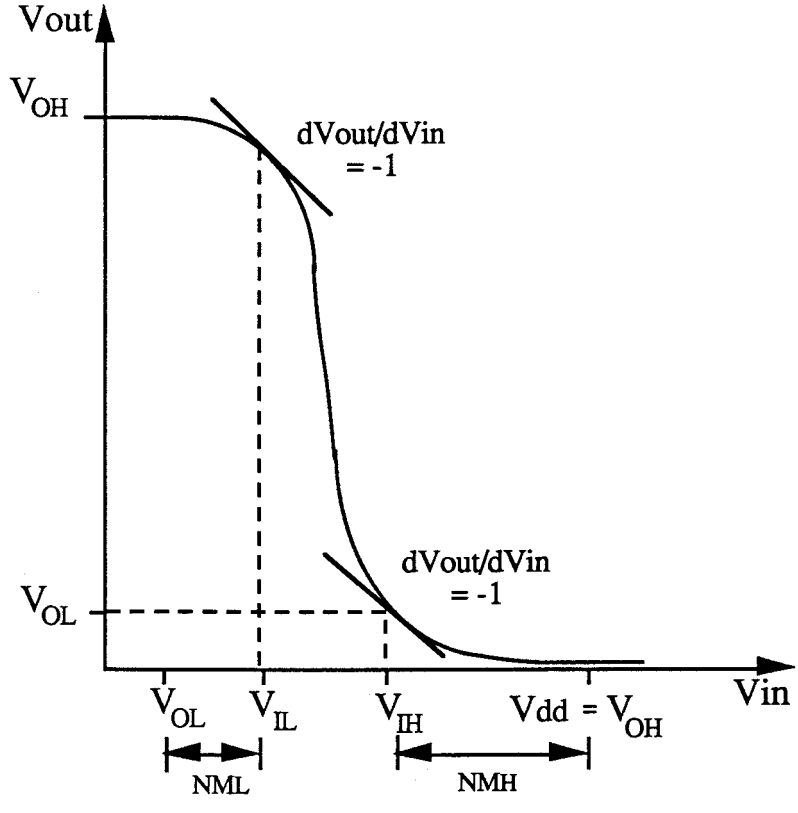


Figure 3.5 Voltage transfer characteristic of a static CMOS inverter.

The static noise margins are defined by

$NM_H = V_{OH} - V_{IH}$ which is the logic-high noise margin, and

$NM_L = V_{IL} - V_{OL}$ which is the logic-low noise margin.

The static transfer characteristic of a SI inverter with current gain = 1 is shown in Fig. 3.6. The inverter has zero NM_H and NM_L noise margins, and is therefore impractical.

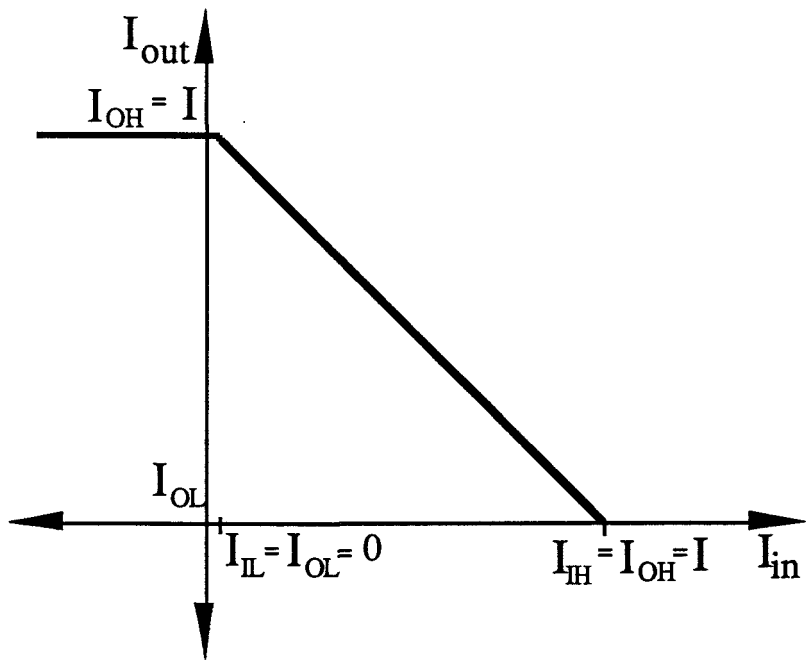


Figure 3.6 The transfer characteristics of a normal SI inverter.

To design a practical SI inverter as in Fig. 3.7, a current gain greater than one (typically 1.5 to 2.0) is needed. This multiplicative factor is called the Shape Factor. The current gain is achieved by increasing the width of the mirroring transistor M2 by the shape factor. Referering to Fig. 3.7, the shape factor ratio of the inverter with gain G is

$$G = \frac{(W/L)_2}{(W/L)_1} = 1.5 = K \tag{3.8}$$

The interpretation of the noise margin in this case is analogous to the CMOS inverter discussed above. Thus the logic-high noise margin is $NM_H = I_{OH} - I_{IH}$ and the logic-low noise margin $NM_L = I_{IL} - I_{OL}$ where the quantities are defined in Fig. 3.8. From Fig. 3.8 the input logic levels are shown to be $I_{IL} = 0$ and $I_{IH} = 0.67I$ and the output

logic levels are $I_{OH} = I$ and the $I_{OL} = -0.5I$. Thus the $NM_H = 0.33I$ and the $NM_L = 0.5I$. With a shape factor of two the logic-low and logic-high noise margins are equal.

To analyze the circuit in Fig. 3.7 to show that is has enhanced noise rejection capability, let the input current change from a logic low level to a high level. The bias current I flows through M1 and establishes a voltage, V_{GS1}. As M1 and M2 share the same gate, $V_{GS1} = V_{GS2}$. Since $(W/L)_2 = 1.5\ (W/L)_1$, a current 1.5I flows through M2 (assuming M2 operates in saturation). On the other hand, the total current available to M2 is only I. M1 operates in saturation and so would M2 if the required current 1.5I was supplied. But since only I is supplied to M2, it operates in the non-saturation region. This ensures that $V_{ds2} < V_T$ and that the next stage is turned off.

Now let the inverter in Fig. 3.7 be driven by an identical stage. M1 is off if the input current is zero. The driving transistor of the previous stage is capable of sinking 1.5I. Thus, even if there is an error in the input current as large as 0.5I, it is sunk into the previous stage and M1 remains turned off.

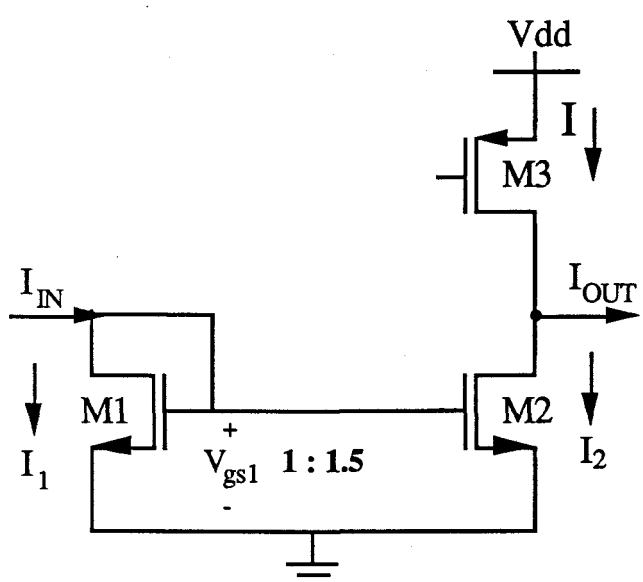


Figure 3.7 A practical SI inverter with enhanced noise margin.

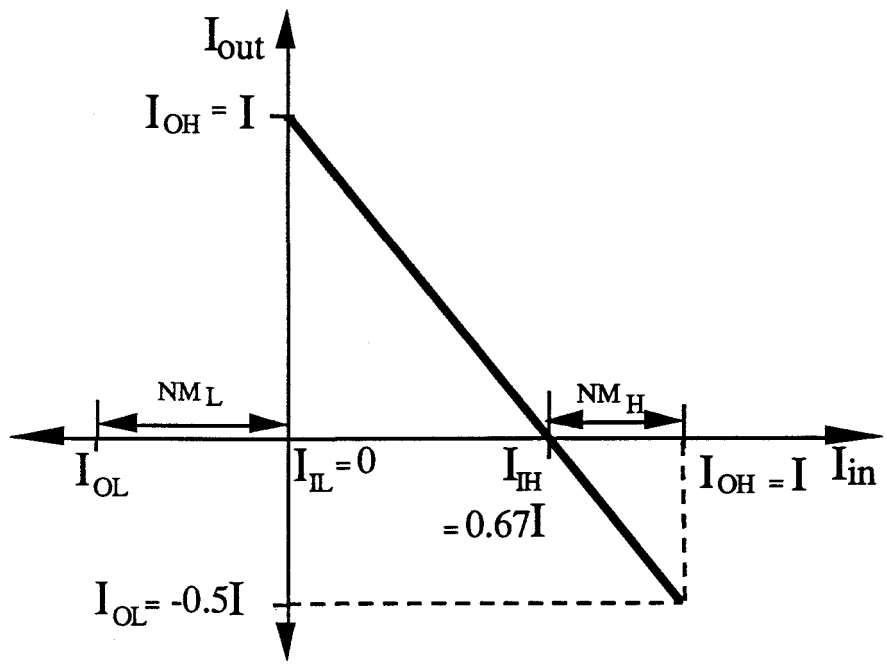


Figure 3.8 The transfer characteristic of a SI inverter with current gain = 1.5.

3.3 Speed Characteristics

Another significant aspect of the SI logic family is its speed of operation. Input and output current waveforms for an SI inverter are shown in Fig. 3.9. The levels of operation are I_H and I_L. The region between these two levels is the transition region. The triggering of an SI logic gate is hence based on a threshold parameter I_T, defined as the minimum current needed to turn it ON. It is defined as the 50 percent point of the transition region. The delays of the inverter are measured between the I_T point of the input and the corresponding output. Simulation results show that the delay is as low as 0.3 ns for I = 300 μA and $(W/L)_1 = (3\mu/2\mu)$, $(W/L)_2 = (6\mu/2\mu)$ in a 2 μm p-well CMOS technology.

The delays are determined by analyzing the switching of the three transistors M1, M2 and M3 of the inverter in Fig. 3.7. Transistor M1 is the input transistor while

the other two are the output devices M1 is diode-connected and operates in either the cutoff or saturation region. The delay involved in switching the SI inverter is analyzed in terms of its rise and fall time. The time required to charge the input capacitance in addition with the time to turn on M1 and M2 (discharge the output node) is the rise time, T_R. The time required to both turn off M1 and M2 (charge the output node) and discharge the input capacitance is the fall time, T_F. When the input is I_L, M1 is off and the output is I_H. The input is next changed to I_H. With $I < I_T$, M1 is off and capacitors $Cin = C_{db1} + C_{gb1} + C_{gs1} + C_{gb2} + C_{gs2} + C_{gd2}$ are charged by M3.

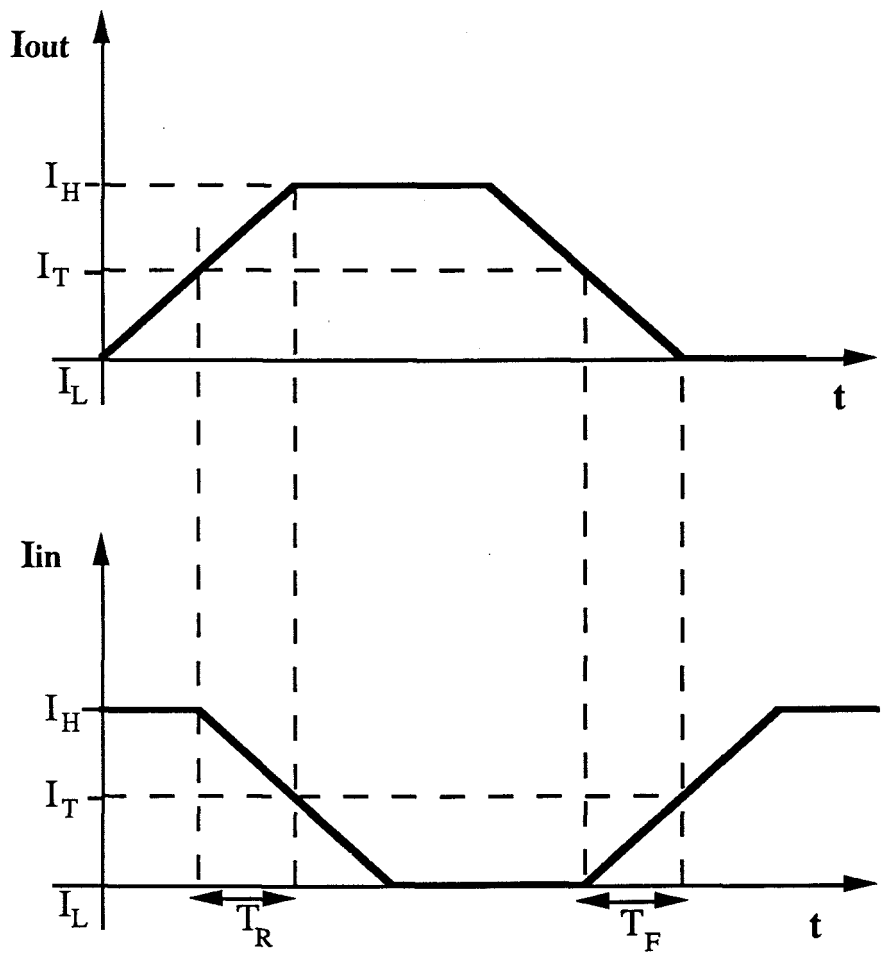


Figure 3.9 Definition of delay characteristics of a SI inverter.

$$I_H = C_{in} \frac{dV_{gs1}}{dt} \tag{3.9}$$

$$T_1 = C_{in} \frac{\Delta V_{gs}}{I} \tag{3.10}$$

where T_1 is defined as the time needed to charge the input capacitors.

When $V_{GS} > V_T$, M1 and M2 turn on, and the output starts to fall towards I_L. The current available to charge the input capacitance is now I_C and is given by

$$I_C = I_H - K_1 \left(V_{GS1} - V_{T1}\right)^2 = C_{in} \frac{V_{gs}}{dt} = C_{in} \frac{\Delta V}{T_2} \qquad \text{where} \tag{3.11}$$

$$T_2 = \frac{C_{in}}{2} \sqrt{\frac{1}{K_1 I}} \ln\left(\frac{\sqrt{K_2} + \sqrt{K_1}}{\sqrt{K_2} - \sqrt{K_1}}\right) \tag{3.12}$$

is the time needed to turn on M2. The total rise time T_R is given by $T_1 + T_2$.

Now when the input changes to I_L, M2 turns off, and then M1 turns off and C_{in} discharges through the input node of diode M1 to the previous stage. The time taken for this is T_F. The charging current is the same as when C_{in} was being charged, but in the opposite direction. Hence,

$$I_C = I_L + K_1 \left(V_{GS1} - V_{T1}\right)^2 = -C_{in} \frac{dV_{gs1}}{dt} \tag{3.13}$$

and

$$T_F = C_{in} \sqrt{\frac{1}{\left(K_2 - K_1\right) I}} \tan^{-1}\left(\sqrt{\frac{K_1}{K_2 - K_1}}\right) \tag{3.14}$$

The propagation delay time T_{delay} is defined as $(T_R + T_F)/2$ and given as

$$T_{delay} = \frac{C_{in}\,\Delta V_{gs}}{2\,I_H} + \frac{C_{in}}{4}\sqrt{\frac{1}{K_1 I}}\,\ln\left(\frac{\sqrt{K_2}+\sqrt{K_1}}{\sqrt{K_2}-\sqrt{K_1}}\right) + \frac{C_{in}}{2}\sqrt{\frac{1}{(K_2-K_1)\,I}}\,\tan^{-1}\left(\sqrt{\frac{K_1}{K_2-K_1}}\right) \quad (3.15)$$

The reasons for high speed of operation of the switched-current inverter are seen by examining the charging current given by

$$I = C\frac{dV}{dt}$$

or

$$t = C\frac{\Delta V}{I} \qquad \text{where t is the delay time.} \quad (3.16)$$

The voltage swing in SI logic is very small, about 500 mV as compared to 5 V for conventional static CMOS logic. Thus, from (3.16), the SI logic gate is potentially very fast. Minimum dimension inverters are used with (W/L) values of (3μ/2μ). By reducing the size of the transistor, the capacitance become smaller. Also note that a constant current is charging a diode-connected transistor. By increasing the current, the delay of the SI logic gates is reduced.

3.4 Power-Delay Product

From the delay time calculations (3.15) the power-delay product (PDP) is determined as

$$PDP = V_{dd} I T_d$$

$$= \frac{V_{dd} C_{in} \Delta V_{gs}}{2} + \frac{V_{dd} C_{in}}{4} \sqrt{\frac{I}{K_1}} \ln \left(\frac{\sqrt{K_2} + \sqrt{K_1}}{\sqrt{K_2} - \sqrt{K_1}} \right)$$

$$+ \frac{V_{dd} C_{in}}{2} \sqrt{\frac{I}{K_2 - K_1}} \tan^{-1} \left(\sqrt{\frac{K_1}{K_2 - K_1}} \right) \qquad (3.17)$$

The power-delay curve is shown in Fig. 4.5. As the current is increased, the time needed to charge the capacitance decreases and hence the gate delay is reduced. But, as the bias current is increased the size of the transistors have to be increased so as to maintain a proper logic swing. With the increase in transistor sizes, the parasitic capacitances also increase. Hence there is a limit to which the current can be increased. Depending on the limit of power dissipation, the bias current is chosen thereby setting the gate delay.

4. DESIGN OF DIGITAL CIRCUITS

Having seen that SI logic gates function as predicted, several basic digital circuits are now implemented. Both combinational and sequential circuits are designed and analyzed.

4.1 Ring Oscillator

A basic digital circuit to study power-delay performance is a ring oscillator. The time period of oscillation is given by

$$T = n\,\tau, \qquad \text{where} \qquad \begin{array}{l} n = \text{number of stages (odd only)} \\ \tau = \text{delay of an inverter} \\ T = \text{Time period of oscillation} \end{array} \qquad (4.1)$$

A ring oscillator is implemented as a series of inverters with the output of the final stage connected to the input of the first stage. To limit the frequency of oscillation below 50 MHz so that it could be easily measured, and assuming a gate delay of 1 to 2 ns per stage, a 49-stage ring oscillator was designed. To study fanout effects, three circuits were designed and implemented with fanouts of 1, 3 and 5. The three ring oscillators were then implemented in the 2 micron p-well process and fabricated by MOS Integration Services (MOSIS). The schematic of the circuit is shown in Fig. 4.1 and a microphotogrpah of the fabricated IC in Fig. 4.2.

For each inverter

(W/L)M1=4μ/2μ -NMOS

M2=6μ/2μ -NMOS

M3=6μ/2μ -PMOS

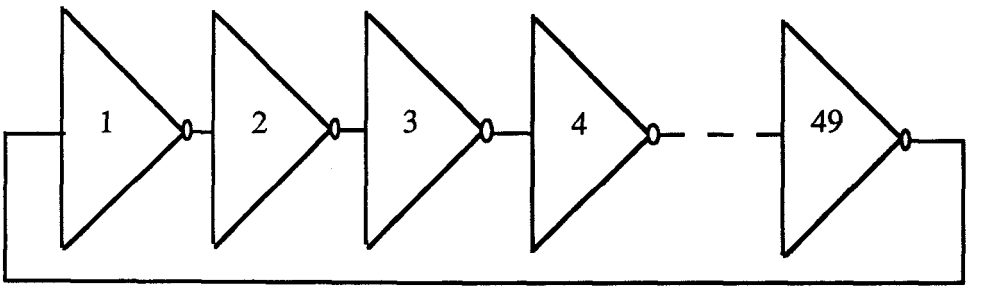


Figure 4.1 Schematic of a 49-stage ring oscillator.

BIAS CURRENT

POWER SUPPLY VOLTAGE (V \ μA)	50	100	150	200	250	300	350
5.0	1.15	0.768	0.586	0.491	0.440	0.396	0.357
4.5	1.18	0.744	0.598	0.512	0.448	0.364	—
4.0	1.24	0.788	0.630	0.512	—	—	—
3.5	1.287	0.841	0.611	—	—	—	—
3.0	1.346	0.813	0.606	—	—	—	—
2.5	1.557	—	—	—	—	—	—

Table 4.1 Simulated gate delay (ns) of an inverter with variations in power supply and bias current for fanout = 1.

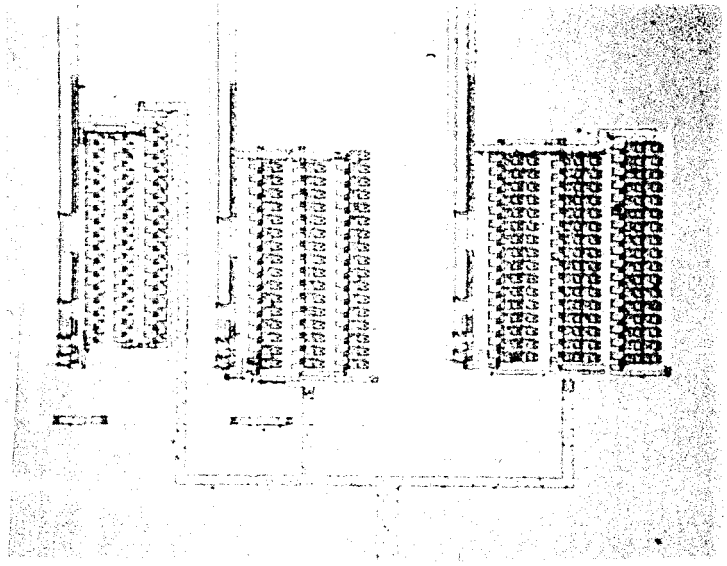


Figure 4.2 The micro-chip photograph of three 49-stage ring oscillators with fanouts of 1, 3 and 5 (left to right) for each inverter.

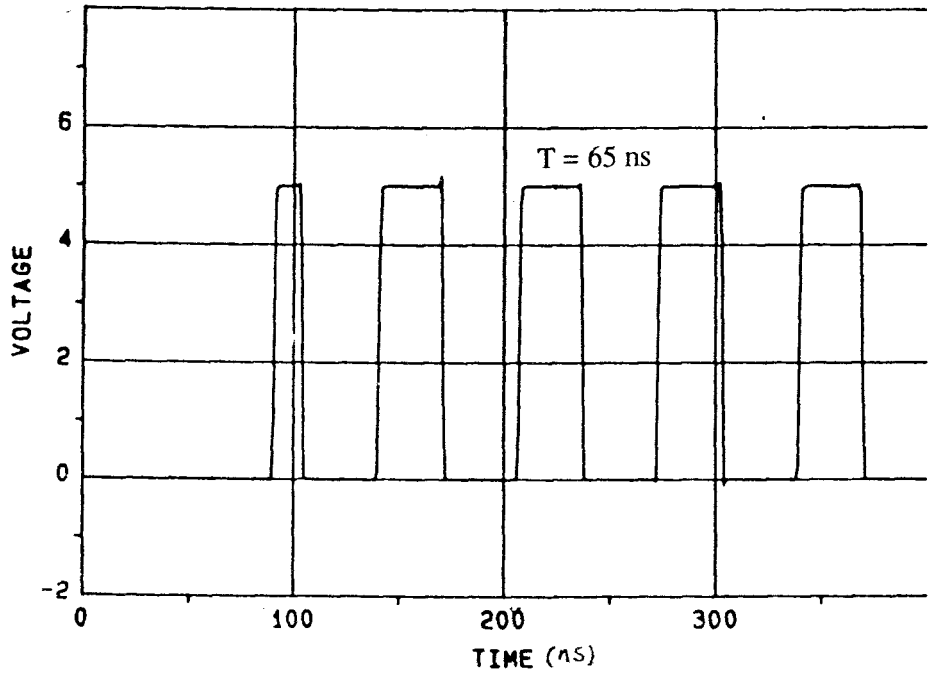


Figure 4.3 The simulated output waveforms of a 49-stage SI ring oscillator with fanout = 1 for I = 100 μA.

Figure 4.3 shows a simulated output waveform for the 49-stage ring oscillator with a bias current of 100 μA. The oscillation waveform is in terms of voltage as a output I-V buffer was used. The ring oscillator in Fig. 4.1 was simulated with different values of the bias current and the power supply voltages as shown in Table. 4.1; and the simulated results are plotted in Figs. 4.4 and 4.5.

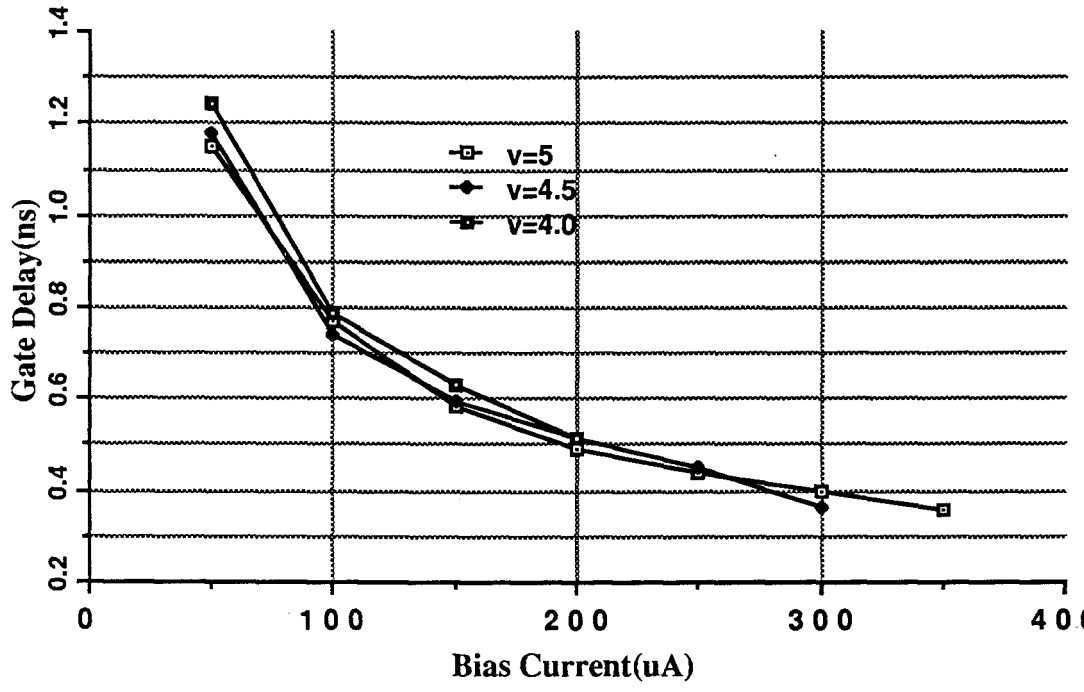


Figure 4.4 Simulated variations in gate delay with change in bias current and supply voltage with fanout = 1.

The graphs show that the delay of an SI inverter varies inversely to the bias current and is approximately constant with power supply voltage. A specific bias current is selected for a given speed requirement.

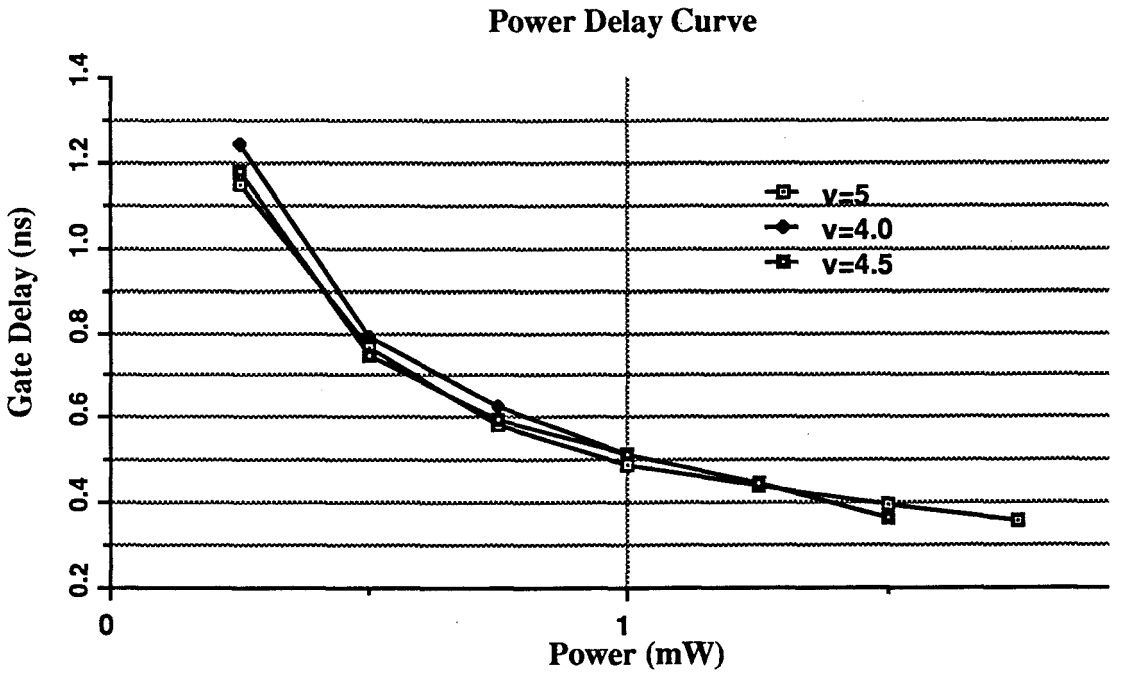
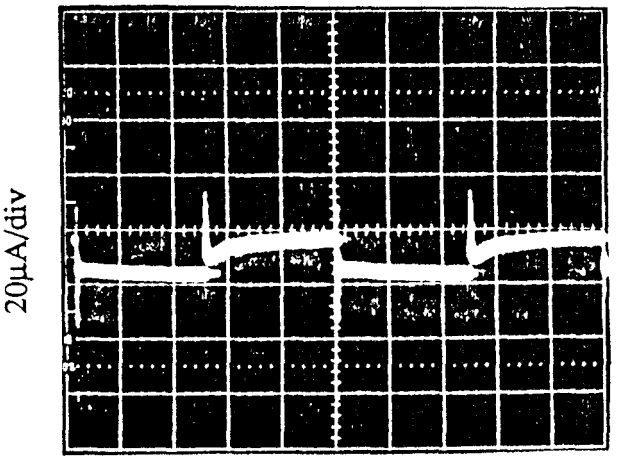
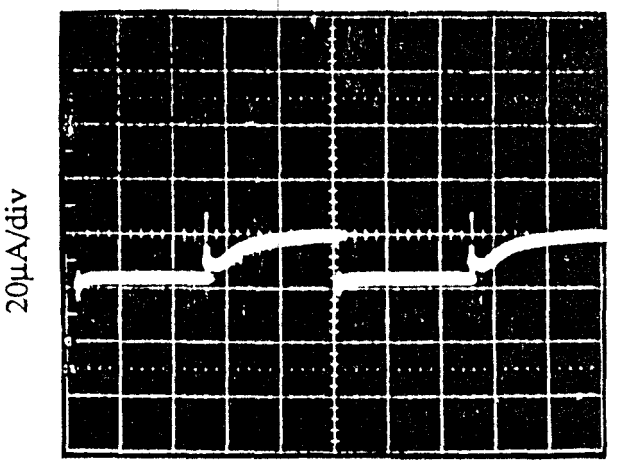


Figure 4.5 The power-delay curve of an SI inverter.

Figure 4.5 shows the simulated power-delay curves of an SI inverter; the delay of an inverter decreases as the power consumption increases. The graph also shows that the power-delay performance is insensitive to power supply variations. It is desired that the power-delay product be minimized and this aspect is taken up later. The measured power supply and ground spikes are shown in Fig. 4.6. The power supply noise spike is measured to be 18 μA, in good agreement with the simulation results.



Power supply current spikes



Ground current spikes

Figure 4.6 The measured power supply and ground noise spikes of an SI inverter (fanout = 1) for I = 100 μA and Vdd = 5 V.

4.2 A 4-Bit Carry Look-Ahead Adder

A carry look-ahead adder circuit has also been implemented to show that the logic works well at a system level. The speed of an adder is dependent on the time of carry propagation and on the speed of the gates. The block diagram of the adder is shown in Fig. 4.7.

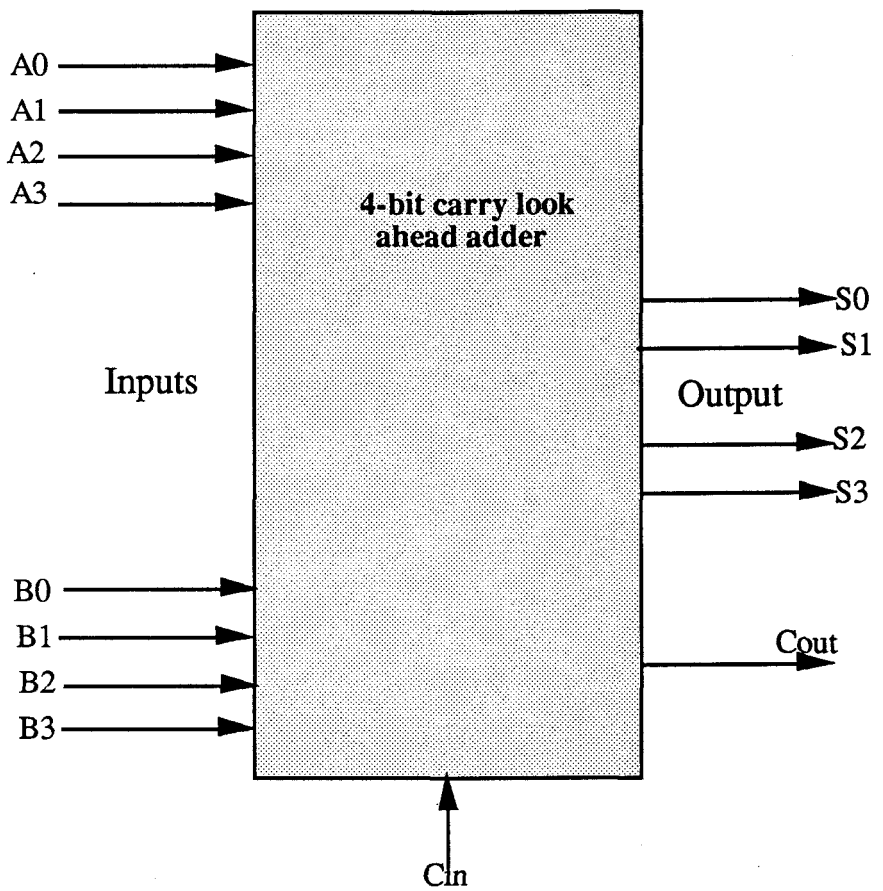


Figure 4.7 A block diagram of a 4-bit carry look-ahead adder.

In Fig. 4.7, the input 4-bit numbers are represented by A0-to-A3 and B0-to-B3, the output by S0-to-S3, the input carry by Cin and the output carry by Cout.

The logic equations of the adder [8] are given by the

$$SUM = A_I \Theta B_I \Theta C_I \qquad \text{where } \Theta \text{ is XOR} \tag{4.2}$$

$$CARRY = G_I + P_I G_{I-1} + P_I P_{I-1} G_{I-2} + \text{-----} + P_I P_{I-1} P_1 G_{I-0} + P_I P_{I-1} \text{-----} C_0 \tag{4.3}$$

where $P_I = A_I + B_I$ (Propagate signal) (4.4)

$G_I = A_I \times B_I$ (Generate signal) (4.5)

A carry is formed at the output of a given stage if one is generated in the given stage or in a previous stage and propagated to the given stage. Figure 4.8 shows the simulation results of the adder. The micro-chip photograph of the adder is shown in Fig. 4.9. The simulations predict a power dissipation of 320 mW.

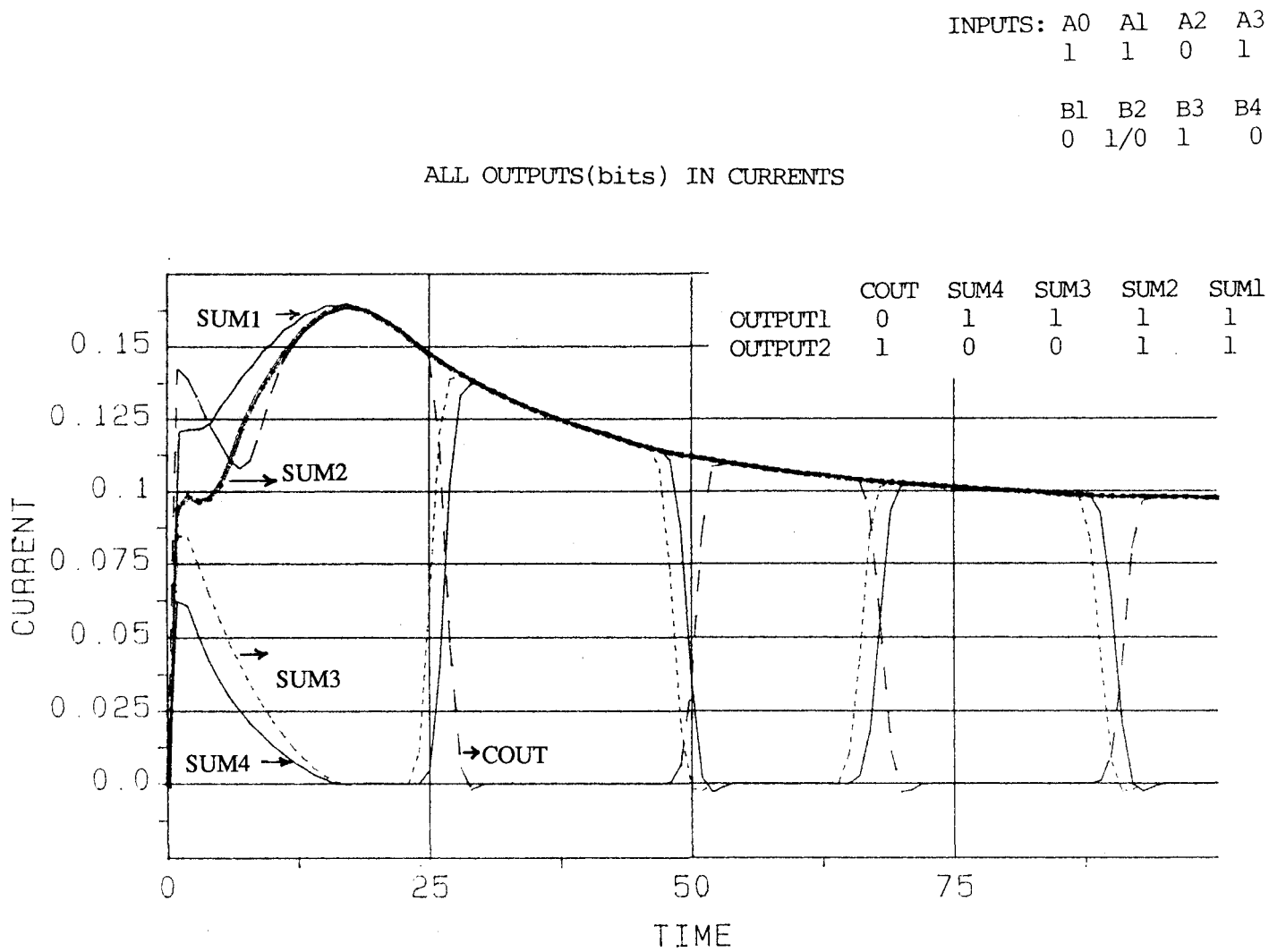


Figure 4.8 The output waveform of the 4-bit carry look-ahead adder.

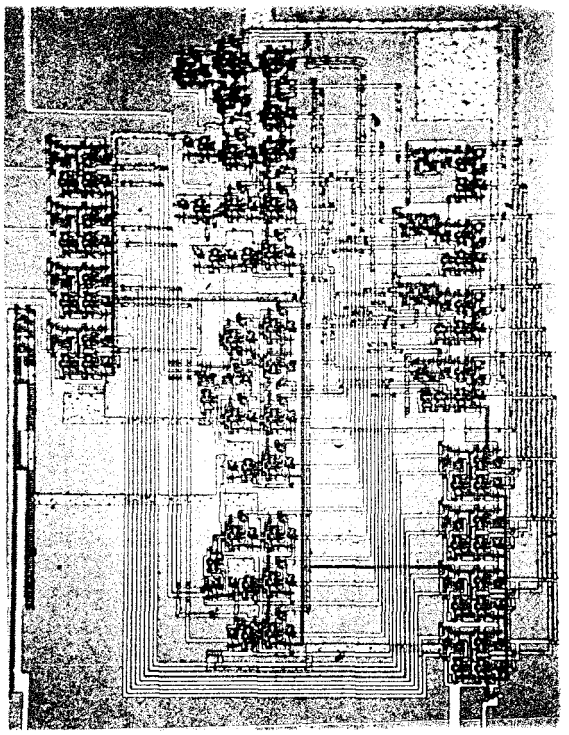


Figure 4.9 The micro-chip photograph of a 4-bit SI carry look-ahead adder.

4.3 Sequential Circuits

After looking at the functionality of combinational circuits, basic sequential circuits were designed and simulated [9]. A simple RS flip-flop is shown in Fig. 4.10. In a similar way, other sequential circuits are implemented. Because each fanout from a SI logic circuit requires a separate output branch, circuits that are optimum in terms of area/speed for conventional logic may not be optimum for SI implementations. This is a topic for future study.

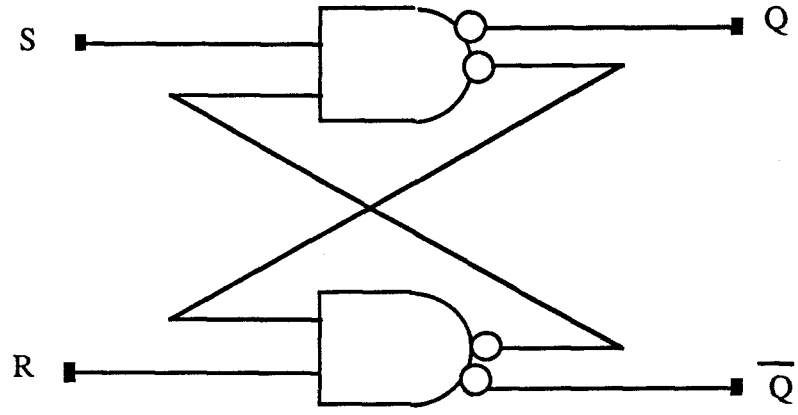


Figure 4.10 A schematic of a SI RS flip-flop.

5. SCALING OF TECHNOLOGIES

Continuing improvements in IC fabrication technology make it possible to reduce the internal dimensions of semiconductor devices. Early IC technologies had minimum dimensions of about 20 μm, while the present industry standard is sub-micron. The circuits described in this thesis are implemented in a 2 μm technology. The trend to reduce device dimensions will likely continue until the fundamental physical limitation of about 0.10 μm is reached [10]. Another limitation is due to a mechanism called subthreshold conduction [11]. It's effect is that the drain current does not go to zero at Vgs = Vt, but instead falls exponentially with decreasing Vgs. Thus this puts a limit on scaling the threshold voltages, especially in dynamic circuits in which the current in the off state must be very small. Scaling is a way to reduce the power-delay product of a device. The idea is to reduce the delay as well as the amount of power dissipated, subject to other design constraints.

5.1 The Scaling Laws

There are at least three scaling laws that are used to determine the performance of scaled circuits. They are the constant voltage (CV), the constant electric field (CE) and the quasi constant voltage (QCV). QCV is used with the reduction of power supply voltage from 5 V to 3.3 V. CV is the most widely scaling law used and will be used in our analysis along with the CE law. Table 5.1 shows the effects of scaling on various transistor parameters with respect to a scaling factor K, which is greater than 1.

TRANSISTOR PROPERTIES	CE	QCV	CV
Voltages (Vdd & Vt)	1/K	1/√K	1
Lateral Dimension (W & L)	1/K	1/K	1/K
Vertical Dimension (X & Tox)	1/K	1/K	1/√K
Doping Concentration (ND)	K	K	K

Table 5.1 The effect on transistor properties due to the basic scaling laws.

5.2 SI Logic under the CE and CV Scaling Laws

The SI logic circuits are analyzed using the relations in Table 5.1. The relations of the various parameters and characteristics are tabulated in Table 5.2. From the equations (3.10), (3.12), (3.14) (3.15) and (3.17), recall that the rise time $T_R = T_1 + T_2$, the fall time is T_F and that T_{delay} is the gate propagation delay.

TRANSISTOR PROPERTIES	CE	CV
Capacitance	1/K	$1/\sqrt{K}$
Transconductance	K	$\sqrt{K}$
Rise time [T_F]	$T_1/K^2 + T_2/K^{3/2}$	$T_1/K^{3/2} + T_2/K^{7/4}$
Fall time [T_F]	$1/K^{3/2}$	$1/K^{7/4}$
Bias Current [I]	1	1
Power consumption	1/K	1

Table 5.2 Scaling of SI under constant field and constant voltage scaling laws.

Thus the performance of the SI logic circuits will improve with scaling and hence can be used with future scaled industry standards.

6. CONCLUSIONS

A new logic family called switched-current logic (SI) was implemented. This logic works in the current domain unlike the existing conventional static CMOS logic families that work in the voltage domain. Using simple circuits, SI logic can be interfaced with the existing CMOS families. The delay of the SI logic inverter was simulated to be as low as 0.3 ns at I = 300 μA and Vdd = 5 volts; hence, the speed is comparable to that of a static CMOS gate. The speed of the gates can be increased by scaling the dimensions of the transistors. The propagation delay of the logic is found to independent of the power supply voltage and depends only on the constant bias current. The power supply noise spikes are measured to be 15 μA for an input current of 100 μA in comparison to the power supply noise spike generated from a static CMOS inverter of 1 mA. Thus, one the limitations in mixed-mode IC design is nearly eliminated. Several experimental SI logic IC's were fabricated in a 2 μm p-well CMOS technology available from the MOSIS service.

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