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Previous work at Stanford University has demonstrated that inductance in the substrate connection is the principal problem underlying the coupling of digital switching noise into analog circuits. The low impedance substrate can be treated as a single node over a local area. Switching in the digital circuits produces current transients in the substrate. These transients are subsequently amplified in the analog portions of the overall mixed-mode circuit. Various guard rings and other techniques, including the use of new logic circuit families, have been proposed to suppress this noise. This work demonstrates that by using the capacitance of a forward biased guard ring(s), the substrate noise at a specific frequency(ies) can be reduced by resonating the guard ring capacitance with the substrate lead inductance to provide a very low substrate-to-ground impedance.

In this manner, noise at particular frequencies, which are problematic to the analog circuit, can be suppressed. Tuning can be accomplished by varying the current in the forward-biased guard ring diodes.

# Resonant Forward-Biased Guard Rings <br> for <br> Suppression of Substrate Noise in <br> Mixed-Mode CMOS Circuits 

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Resonant Forward-Biased Guard Rings for<br>Suppression of Substrate Noise in Mixed-Mode CMOS Circuits

## CHAPTER 1: INTRODUCTION

Miniaturization and low power consumption are the major industry trends as low power and portable applications rapidly expand their presence in a variety of markets, including telecommunications and consumer electronics. These market requirements demand IC manufacturers to increase the level of circuit integration; indeed, these requirements are the driving force behind the explosion in mixedsignal application technology. Mixed-signal integrated circuits are applicationspecific products that combine analog building block functions, digital logic, and memory functions on the same silicon substrate. Using a single process technology, mixed-mode ICs offer the ideal solution to integrate analog, digital, and memory functions on a single chip in the effort to reduce power consumption and area requirements while simultaneously increasing reliability and performance.

## CHAPTER 2: BACKGROUND

Inductance in the substrate connection is the principal factor underlying the coupling of digital switching noise into analog circuits that are fabricated on the same die [1]. This noise is coupled into the common substrate of the digital and analog circuitry. As a result, switching in the digital circuits produces current transients in the underlying substrate. These transients are subsequently amplified in the analog portions of the overall mixed-mode circuit. This digital switching noise is transferred to the analog circuitry primarily through the substrate although capacitive coupling between the interconnect lines also contributes [1]. The introduction of significant noise into the analog portion of the mixed-mode circuit limits both the accuracy and precision of the analog functions, and therefore corrupts the analog signal.

Noise is the primary concern in integrating digital and analog functions onto the same silicon substrate. Smith et al. [2] report that substrate noise due to digital switching is typically several orders of magnitude greater than the flicker and thermal shot noise in silicon devices. Thus, substrate crosstalk between analog and digital circuits poses a potential problem in mixed-signal applications.

Various methodologies have been proposed to negate the influence of crosstalk in mixed-mode integrated circuits. Previous investigations of substrate crosstalk have focused primarily on the issue of capacitive coupling between logic lines and
the substrate. Typical solutions include minimizing the output resistance of analog circuits and increasing the physical separation between the analog and digital portions on the mixed signal integrated circuit. Smith et al. [2] suggest fabricating an $n$-well capacitor to suppress substrate noise and decouple the power supply noise.

Physical separation, implementing guard rings in both the near and far field, using a low-inductance substrate, and increasing the number of package pins were suggested by Su et al. [1] to reduce the effects of switching noise. Su et al. also proposed concentric n -well and $\mathrm{p}+$ guard rings to protect the analog portions of the chip.

Substrate pumping is another technique that has been proposed [3] [4] [5]. Substrate pumping develops a negative bias at the backgate terminal of the transistors. This lowers the diffusion-to-substrate capacitance and correspondingly decreases the noise coupled into the substrate. However, substrate pumping and the previously proposed techniques share the common drawback of providing only marginal reductions in noise; the noise level is typically reduced by a factor of two or three. Additionally, entirely new logic circuit families have been introduced in an effort to mitigate substrate noise generation. For example, Maskai et al. [6][7] introduced folded source-coupled logic in 1992.

The digital circuit investigated here consists of a 49-stage CMOS ring oscillator that shares a common substrate with a 2-stage CMOS analog amplifier. The ring oscillator is employed to generate substrate noise by virtue of the switching of its inverter stages. The noise associated with the switching of the inverters is coupled into the substrate. The switching noise is amplified by the amplifier and the result is observed at the amplifier's output node.

The proposed solution suggests fabricating a forward-biased guard ring at the common substrate node. This guard ring assumes the form of a narrow base width diode and acts as an on-chip capacitor. Theoretical analysis indicates that the resonant guard ring is capable of suppressing substrate noise by two orders of magnitude.

## CHAPTER 3: RESONANT FORWARD-BIASED GUARD RINGS

The amplifier shown in Figure 1 is a single-ended CMOS 2-stage differential amplifier that uses a single 5 V power supply. The transistors are simulated using $1 \mu m$ technology and modeled in HSPICE Level 3. Level 3 is based on the empirical SPICE 2G model and accounts for 2-dimensional effects depending upon junction depth and depletion depths. Level 3 also accounts for draininduced barrier lowering and offers greater probability of convergence. The area calculation parameter (ACM) allows HSPICE to model the bulk-to-source and the bulk-to-drain diodes. The ACM parameter controls the geometry of the source and drain diffusion and includes the diffusion resistance, capacitance, and DC currents to the substrate. The simulations utilize Level 2 of the area calculation method which calculates the parameters as functions of element area and width.

The amplifier consists of a differential input stage using n-channel transistors M3 and M4. M3 and M4 have $50 \mu \mathrm{~m}$ channel widths. Transistors M1 and M2 are pchannel active loads that drive the bias current through M5. Due to the symmetry of the differential input stage, M1 and M2 also have matched channel widths at $80 \mu \mathrm{~m}$. The ratio of the channel lengths between the NMOS and PMOS devices is determined by the ratio of the charge carrier mobilities of the NMOS and PMOS transistors. M5, with $100 \mu m$ channel width, simulates an ideal current source, and is connected to the gates of transistors M7 and M12 in the


Figure 1. $1 \mu m$ CMOS Single-Ended Differential Amplifier
other two branches. Both transistors M7 and M12 are NMOS devices with $50 \mu \mathrm{~m}$ channel length. This configuration attempts to force the same amount of current flowing through the output stage as flows through the bias transistor M5. Thus, transistors M6, M7, comprising the bias current branch where M6 is a PMOS device with $25 \mu m$ width, and M5 attempt to maintain constant current through M12. This improves the gain of the amplifier and increases its frequency range.

The parasitic capacitances of the amplifier are also shown in Figure 1. Stray capacitance $\mathrm{C}_{1}$ accounts for the wiring capacitance between the substrate, gates, and DC bias of the active loads. As determined from the layout in Appendix E, $C_{1}$ is 41.7 fF . $\mathrm{C}_{2}$ represents the 10.7 fF parasitic capacitance between substrate and the metal input line for M3. Similarly, $\mathrm{C}_{1}$ is 10.8 fF and accounts for the stray substrate-to-metal capacitance for M4.

The parasitic capacitance between the gate and substrate of transistor M11 is 27.6fF. The other significant stray capacitance, $C_{3}$, occurs at the output node. Again, the value of $C_{3}$ is determined from the layout in Appendix $E$ and is 11.9fF. C, simulates the metal-to-substrate capacitance.

Figure 2 illustrates the CMOS inverter with the associated parasitics. In contrast to the amplifier, the transistors in the ring oscillator each have $2 \mu \mathrm{~m}$ channel


Figure 2. CMOS Inverter Cell
lengths and both NMOS and PMOS devices have $4.8 \mu \mathrm{~m}$ channel widths. Note that this is a minimum-area design for the inverter stages. The inverter transistors are modeled using Level 3 in HSPICE. The capacitor $C_{w}$ represents the stray capacitance between the wiring and substrate. $C_{w}$ is 5.68 fF for the specific amplifier layout included in the Appendix E.

The parasitic capacitance $C_{o}$ accounts for the capacitance between the output node and the substrate. As determined from the layout, $C_{o}$ is 2.4 fF . The $10 \Omega$ resistor represents the resistance of the epitaxial layer. The parasitics were determined through automated parameter extraction using actual layouts of the amplifier and inverter stages of the ring oscillator.

Figure 3 shows the ring oscillator; the corresponding layout is shown in Appendix F. Forty-nine inverter stages are cascaded in a closed loop where the initial conditions are used to initiate oscillation [8]. Oscillation is achieved by grounding the input of the 49th inverter and simultaneously setting the output to 5 V . The noise associated with the switching of the inverters is coupled into the substrate. The switching noise is amplified by the amplifier and the result is observed at the amplifier's output node.

Figure 4 shows the AC small signal equivalent circuit for a PN junction diode under the condition of forward bias [9]. Whereas the depletion region capacitance $C_{j}$ is a direct result of the majority carrier response, the diffusion


Figure 3. 49-Stage Ring Oscillator

## COMMON SUBSTRATE NODE



NODE BETWEEN DIODE AND SUBSTRATE CONNECTION

Figure 4. AC Small-Signal Diode Model
capacitance $C_{d}$ derives from the minority carrier response. The series resistance $R_{p}$ represents the substrate bulk and parasitic contact resistance of the guard ring.

Diode structure is an important consideration in fabrication of the guard ring. Long base width diodes are characterized by

$$
\begin{equation*}
W \gg L_{p} \tag{1}
\end{equation*}
$$

where
$W=$ length of the region of the lightly doped material
$L_{p}=$ mean diffusion length of the minority carriers in the lightly doped material.
The minority carrier concentration reduces to the thermal equilibrium level in a distance $W$. Thus, the response time of long base width diodes is substantially shorter than diodes utilizing the full diffusion length of minority carriers.

Narrow base width diodes are characterised by
$W \ll L_{p}$
where
$W=$ length of the region of the more lightly doped material
$L_{P}=$ mean diffusion length of the minority carriers in the lightly doped material.
Since $W \ll L_{p}$, carrier recombination occurs at the epi-substrate interface and therefore the minority carrier lifetime may be replaced by the mean transit time $T T$. This results in much shorter response times compared to long base width diodes.

For narrow base width diodes, the mean transit time of the excess minority carriers, $T T$, replaces the minority carrier recombination lifetime, $\tau_{n}[7]$. The diffusion length is then replaced by the width $W$ of the lightly doped material.

As a result, the diffusion capacitance decreases significantly. This reduction in capacitance increases the resonant frequency of the RLC structure. For low bias, the narrow base width diode increases the resonant frequency into the gigahertz regime. This is precisely the type of frequency response/selectivity that is desired; the noise frequency was determined to be 0.875 GHz .

Since the guard ring is forward biased, the junction capacitance $C_{j}$ is insignificant and therefore the model reduces to the parallel combination of the diode conductance $G$ and diffusion capacitance $C_{d}$. The diode is modeled in Level 1 in HSPICE. In addition to specifying the transit time $T T$, the saturation current $I_{s}$ is also provided. The saturation current is determined to be $I_{s}=16.8 \mathrm{fA}$

However, to determine the optimal bias current through the diode, the frequency of the noise must be first determined. From Figure 6, which shows the noise waveform without any guard ring, it can be seen that the period of the fundamental is 4.0 ns over 3.5 complete periods. Thus,
$T=$ waveform period $=\frac{4.0 \mathrm{~ns}}{3.5 \text { cycles }}=1.14 \frac{\mathrm{~ns}}{\text { cycle }}$
$f=$ noise frequency $=\frac{1}{T}=\frac{1}{1.14 n s}=875 \mathrm{MHz}$
The radian frequency is given as
$2 \pi f=2 \pi(875 \mathrm{MHz})=5.5 \cdot 10^{9} \frac{\mathrm{rad}}{\mathrm{sec}}$
The saturation current of the diode is
$I_{o}=I_{s}=\frac{q A D_{n n p_{o}}}{w b}(A m p s)$
where representative values of standard CMOS technology have been chosen,
$D_{n}=25 \frac{\mathrm{~cm}^{2}}{\mathrm{sec}}$
$w_{b}=10 \mu m$
$n p_{0}=4.2 \cdot 10^{5} / \mathrm{cm}^{3}$
$A=10^{-5} \mathrm{~cm}^{2}=1000 \mu m^{2}$
$q=1.6 \cdot 10^{-19} \mathrm{C}$
and then
$I_{s}=16.8 f A$
Note that the relationship between the diode conductance and diffusion capacitance yields the transit time
where
$T T=$ transit time $=r \cdot C_{d}$
$C_{d}$ is the diffusion capacitance, and
$g=\frac{1}{r}=\frac{\operatorname{IDC}(m A)}{25 o h m s}$

Figure 5 illustrates the equivalent circuit of the guard ring diode, substrate inductance, and DC bias source in conjunction with the associated substrate connections for the digital and analog circuits.

The digital circuit consists of a 49-stage CMOS ring oscillator that shares a common substrate with a 2 -stage CMOS analog amplifier. The oscillator is employed to generate substrate noise by virtue of the switching of its inverter stages. This digital switching noise is coupled into the amplifier via the common substrate; the amplifier magnifies the noise and offers an output node for observation.

Thus, the ring oscillator and analog amplifier emulate the mechanism of substrate crosstalk that corrupts the analog signal in typical mixed-mode CMOS circuit applications. The substrate contact on the ring oscillator is connected to the common substrate through a $0.9 \Omega$ resistor; similarly, the amplifier substrate is connected to the common substrate through a $0.1 \Omega$ resistor. These resistances simulate the substrate contact resistance for their respective circuits. The local substrate node on the amplifier is also connected to a $1 \Omega$ resistor in series with a 10 nH inductor that leads to ground; the 10 nH inductor models the substrate inductance whereas the $1 \Omega$ resistor accounts for the series resistance in the substrate.


Figure 5. AC Equivalent Circuit of Guard Ring Structure

The AC equivalent circuit of the embedded guard ring structure reveals the RLC equivalent circuit configuration of the substrate inductance, parasitic contact resistances, forward-biased diode conductance, and forward-biased diffusion capacitance. The PN junction diode under conditions of forward bias can be modeled as shown in Figure 4. The depletion region capacitance $C_{j}$ is a direct result of the majority carrier response; the diffusion capacitance $C_{d}$ derives from the minority carrier response. Under forward bias, though, the depletion capacitance may be ignored. Figure 5 shows the small signal equivalent circuit where the series resistance $R_{p}$ represents the substrate and parasitic contact resistance.

As described above, the AC equivalent circuit of the guard ring structure forms an RLC circuit configuration. This circuit can be forced to resonate at a particular frequency by varying the current through the diode. The diffusion capacitance depends upon the diode current and, consequently, the capacitance can be varied by adjusting the DC bias across the guard ring diode. This allows tuning of the filter. The inductance of the wire bond and pin leads is modeled as a lumped parameter since the substrate is treated as a single node over a local area. Hence, adjusting the bias voltage will vary the resonant frequency of the equivalent RLC circuit.

Examination of the small signal AC equivalent circuit of the guard ring diode and substrate connection provides the insight for calculating the optimum DC bias such that the resonant guard ring will provide maximum suppression of the substrate noise.

From circuit theory [10], the driving point impedance at the common substrate contact is
$Z(s)=\frac{\left(s^{2}+\frac{1}{r C d} s+\frac{1}{L C d}\right) L}{s+\frac{1}{r C d}}$
where the resonant frequency $\omega_{0}$ is given as
$\omega_{o}=\sqrt{\frac{1}{L C d}}$
The resonant frequency can be expressed as a function of the diode parameters by substituting
$T T=r C_{d}$
into
$\omega_{0}=\sqrt{\frac{r}{L \cdot T T}}$
This shows the dependence of resonant frequency on the diode conductance.
Since the conductance is directly controlled by the bias current, the resonant frequency can be adjusted by varying $V_{\text {bias }}$.

At the resonant frequency $\omega_{s}$, the impedance looking down into the guard ring structure from the substate node is
$Z_{s}=\frac{1}{r} \frac{L}{C_{d}}=\frac{L}{T T}$

This impedance becomes very small for parameter values near the the resonant condition. Substituting the parameters

Substrate Inductance: $\quad L=10 \mathrm{nH}$
Diffusion Capacitance: $\omega_{o}=2 \pi(800 M H z)=\sqrt{\frac{1}{L C d}}$

$$
\begin{equation*}
C_{d}=3.3 \mathrm{pF} \tag{23}
\end{equation*}
$$

Diode Resistance: $\quad r=\frac{1}{g}=\frac{T T}{C d}=\frac{20 n s}{3.3 p F}=6.1 \mathrm{k} \Omega$
yields
$Z_{g}=0.5$.
Thus, a single guard ring theoretically provides two orders of magnitude of substrate noise reduction.

The quality factor $Q$ indicates the spectral width of the frequencies selected by the resonant guard ring structure. To maximize the noise reduction obtainable from a single guard ring diode, a low $Q$ and low magnitude impedance $\left|Z\left(\omega_{0}\right)\right|$ are desired.

The low $Q$ will alleviate the problem of precise determination of the frequency components in the substrate noise. Since mulitple frequency components exist in
the substrate noise spectrum, a low- $Q$ resonant structure offers the advantage of shunting several frequencies through the same guard ring. The quality factor $Q$, which is a measure of the selectivity of the RLC filter, is given as
$Q=\frac{r}{\omega_{0} L}=\frac{r C}{\omega_{0} L C}=T T \cdot \omega_{0}$
where
$T T=$ transit time $=20 \mathrm{~ns}$
$\omega_{b}=2 \pi f$
Several additional relationships are useful in the application of this technique. These relationships can be exploited to allow rapid and accurate determination of the proper parameters of the guard ring and DC bias source to achieve maximum suppression of the substrate noise.

The magnitude impedance of the RLC structure is

$$
\begin{equation*}
\left|Z\left(\omega_{0}\right)\right|=\frac{L}{r C_{d}}=\frac{L}{T T} . \tag{29}
\end{equation*}
$$

Another figure of merit is the product of the quality factor and impedance at resonance:

$$
\begin{equation*}
\left|Q \cdot Z\left(\omega_{0}\right)\right|=\frac{r}{\omega_{0} L} \cdot \frac{L}{r C_{d}}=\omega_{0} L \tag{30}
\end{equation*}
$$

Figure 6 illustrates the equivalent circuit configuration of the ring oscillator, amplifier, and substrate connections for a typical CMOS process that does not employ resonant forward-biased guard rings.


Figure 6. Typical CMOS Process With No Guard Ring

Figure 7 shows the response of the circuit in Figure 6 where no guard ring is utilized. Note that the noise magnitude in Figure 7 is about ten times greater than the noise magnitude from the circuit employing the resonant guard ring at optimum bias.

Figure 8 shows the result of a 1024-point Fast Fourier Transform (FFT) performed on the time-domain output signal for the circuit shown in Figure 6, where no guard ring is employed. The data indicates the largest frequency component occurs at 875 MHz . This agrees with the calculations performed on the results shown in the time domain response in Figure 7. To demonstrate the utility of the forward biased guard ring, the 875 MHz frequency was selected as the target frequency for suppression.

Figure 9 displays the output waveform from the amplifier for $V_{\text {bias }}=-0.40 \mathrm{~V}$. Note that this bias is 0.12 V positive with respect to the optimal bias point at 0.52 V . The steady state output noise voltage is 30 mV peak-to-peak.

Similarly, Figure 10 shows the response for $V_{b i a s}=-0.60 \mathrm{~V}$. Note that this bias is 0.08 V negative compared to the optimal bias point. The steady state output noise voltage is 10 mV peak-peak.

Figures 9 and Figure 10 demonstrate the sensitivity of the guard ring to variations in DC bias.
zhr tro<


Figure 7. Substrate Noise Magnitude w/o Guard Ring


Figure 8. FFT Components of Transient Response


Figure 9. Substrate Noise Magnitude at -0.40 V Bias


Figure 10. Substrate Noise Magnitude at -0.60 V Bias

Figure 11 illustrates the noise level at the optimal DC bias condition. The approximate magnitude of the noise voltage is 3 mV . Comparison of Figures 7 and Figure 11 reveal a significant decrease in the substrate noise. This comparison indicates that an order of magnitude reduction in noise level can be achieved by employing a single resonant forward-biased guard ring.

Figure 12 illustrates the result of a 1024-point Fast Fourier Transform perfomed on the output signal of the mixed-mode circuit. The FFT shows a 24 dB reduction in the substrate noise level at 875 MHz . This indicates that more than one order of magnitude reduction in the substrate noise level is obtainable. Note that this reduction is achieved through a single resonant forward-biased guard ring operating at the optimal DC bias condition.


Figure 11. Substrate Noise Magnitude at Optimal Bias


Figure 12. FFT Response of Guard Ring at Optimal Bias

## CHAPTER 4: CONCLUSION

This paper proposes the fabrication of a forward-biased guard ring to suppress substrate noise by reducing the substrate-to-ground impedance. The guard ring diode behaves as an on-chip capacitor. Adjusting the DC bias of the diode provides the proper diffusion capacitance to force the RLC circuit into resonance at the chosen frequency. Theoretical analysis indicates that the resonant guard ring is capable of suppressing substrate noise by two orders of magnitude. Simulation results illustrate that noise reduction of one order of magnitude through a single resonant guard ring is feasible. It is advantageous to obtain a low quality factor $Q$ and a low magnitude impedance $\left|Z\left(\omega_{0}\right)\right|$ since this allows the RLC circuit to attenuate a wider frequency range of switching transients. Multiple guard rings may be employed to suppress a variety of frequency components.

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## APPENDICES

## APPENDIX A: HSPICE CIRCUIT FILE

* Circuit File for 49-Stage Ring Oscillator and 2-Stage CMOS Amplifier
.MODEL DIODE D (LEVEL $=1 \mathrm{IS}=5.6 \mathrm{E}-15 \mathrm{TT}=20 \mathrm{E}-9$ )
.MODEL N_INVERTER NMOS(LEVEL $=3 \mathrm{LD}=0.15 \mathrm{U}$ WD $=0.3 \mathrm{U}$ VTO $=0.73$
$\mathrm{TOX}=200 \mathrm{E}-10 \mathrm{UO}=520 \mathrm{NSUB}=2.8 \mathrm{E} 16 \mathrm{VMAX}=1.35 \mathrm{E} 5 \mathrm{ETA}=0.02 \mathrm{THETA}=0.07$
$\mathrm{KAPPA}=0.1$ DELTA $=0.6 \mathrm{XJ}=0.1 \mathrm{U} \mathrm{NFS}=5 \mathrm{E} 11 \mathrm{RSH}=1000 \mathrm{RD}=0 \mathrm{RS}=0 \mathrm{CGDO}=1.85 \mathrm{E}-10$ $\mathrm{CGSO}=1.85 \mathrm{E}-10 \mathrm{CGBO}=2.5 \mathrm{E}-10 \mathrm{CJ}=3.2 \mathrm{E}-4 \mathrm{JSW}=2.8 \mathrm{E}-10 \mathrm{MJ}=0.95 \mathrm{MJSW}=0.12 \mathrm{JS}=1 \mathrm{E}-3$ $\mathrm{FC}=0 \mathrm{~PB}=0.8 \mathrm{ACM}=2$ )
.MODEL N_AMP_50 NMOS(LEVEL $=3 \mathrm{LD}=0.15 \mathrm{U} \mathrm{WD}=0.3 \mathrm{U}$ VTO $=0.73$ TOX $=200 \mathrm{E}-10$ $\mathrm{UO}=520 \mathrm{NSUB}=2.8 \mathrm{E} 16 \mathrm{VMAX}=1.35 \mathrm{E} 5 \mathrm{ETA}=0.02 \mathrm{THETA}=0.07 \mathrm{KAPPA}=0.1$ $\mathrm{DELTA}=0.6 \mathrm{XJ}=0.1 \mathrm{U} \mathrm{NFS}=5 \mathrm{E} 11 \mathrm{RSH}=1000 \mathrm{RD}=0 \mathrm{RS}=0 \mathrm{CGDO}=1.85 \mathrm{E}-10$ $\mathrm{CGSO}=1.85 \mathrm{E}-10 \mathrm{CGBO}=2.5 \mathrm{E}-10 \mathrm{CJ}=3.2 \mathrm{E}-4 \mathrm{CJSW}=2.8 \mathrm{E}-10 \mathrm{MJ}=0.95 \mathrm{MJSW}=0.12$ $\mathrm{JS}=1 \mathrm{E}-3 \mathrm{FC}=0 \mathrm{~PB}=0.8 \mathrm{ACM}=2$ )
.MODEL N_AMP_100 NMOS(LEVEL $=3 \mathrm{LD}=0.15 \mathrm{U} \mathrm{WD}=0.3 \mathrm{U}$ VTO $=0.73$ TOX $=200 \mathrm{E}-10$ $\mathrm{UO}=520 \mathrm{NS} \mathrm{UB}=\overline{2} .8 \mathrm{E} 16 \mathrm{VMAX}=1.35 \mathrm{E} 5 \mathrm{ETA}=0.02 \mathrm{THETA}=0.07 \mathrm{KAPPA}=0.1$ DELTA $=0.6 \mathrm{XJ}=0.1 \mathrm{U} \mathrm{NFS}=5 \mathrm{E} 11 \mathrm{RSH}=1000 \mathrm{RD}=0 \mathrm{RS}=0 \mathrm{CGDO}=1.85 \mathrm{E}-10$ $\mathrm{CGSO}=1.85 \mathrm{E}-10 \mathrm{CGBO}=2.5 \mathrm{E}-10 \mathrm{CJ}=3.2 \mathrm{E}-4 \mathrm{CJSW}=2.8 \mathrm{E}-10 \mathrm{MJ}=0.95 \mathrm{MJSW}=0.12$ $\mathrm{JS}=1 \mathrm{E}-3 \mathrm{FC}=0 \mathrm{~PB}=0.8 \mathrm{ACM}=2$ )
.MODEL P_INVERTER PMOS(LEVEL $=3 \mathrm{LD}=0.0 \mathrm{U} \mathrm{WD}=0.4 \mathrm{U}$ VTO $=-0.9$ TOX $=200 \mathrm{E}-10$ $\mathrm{UO}=180 \mathrm{NSUB}=2.8 \mathrm{E} 16 \mathrm{VMAX}=1.9 \mathrm{E} 5 \mathrm{ETA}=0.09 \mathrm{THETA}=0.13 \mathrm{KAPPA}=3 \mathrm{DELTA}=0.3$ $\mathrm{XJ}=0.0 \mathrm{U} \mathrm{NFS}=1 \mathrm{E} 12 \mathrm{RSH}=1400 \mathrm{RD}=0 \mathrm{RS}=0 \mathrm{CGDO}=1.85 \mathrm{E}-10 \mathrm{CGSO}=1.85 \mathrm{E}-10$
$\mathrm{CGBO}=2.5 \mathrm{E}-10 \mathrm{CJ}=5.2 \mathrm{E}-4 \mathrm{CJSW}=2.8 \mathrm{E}-10 \mathrm{MJ}=0.5 \mathrm{MJSW}=0.33 \mathrm{JS}=1 \mathrm{E}-3 \mathrm{FC}=0 \mathrm{~PB}=0.9$ $\mathrm{ACM}=2$ )
.MODEL P_AMP_80 PMOS(LEVEL $=3 \mathrm{LD}=0.0 \mathrm{U}$ WD $=0.4 \mathrm{U}$ VTO $=-0.9$ TOX $=200 \mathrm{E}-10$ $\mathrm{UO}=180 \mathrm{NSUB}=2.8 \mathrm{E} 16 \mathrm{VMAX}=1.9 \mathrm{E} 5 \mathrm{ETA}=0.09 \mathrm{THETA}=0.13 \mathrm{KAPPA}=3 \mathrm{DELTA}=0.3$ $\mathrm{XJ}=0.0 \mathrm{U} \mathrm{NFS}=1 \mathrm{E} 12 \mathrm{RSH}=1400 \mathrm{RD}=0 \mathrm{RS}=0 \mathrm{CGDO}=1.85 \mathrm{E}-10 \mathrm{CGSO}=1.85 \mathrm{E}-10$ $\mathrm{CGBO}=2.5 \mathrm{E}-10 \mathrm{CJ}=5.2 \mathrm{E}-4 \mathrm{CJSW}=2.8 \mathrm{E}-10 \mathrm{MJ}=0.5 \mathrm{MJSW}=0.33 \mathrm{JS}=1 \mathrm{E}-3 \mathrm{FC}=0 \mathrm{~PB}=0.9$ $\mathrm{ACM}=2$ )
.MODEL P_AMP_25 PMOS(LEVEL $=3 \mathrm{LD}=0.0 \mathrm{U} \mathrm{WD}=0.4 \mathrm{U}$ VTO $=-0.9$ TOX $=200 \mathrm{E}-10$ $\mathrm{UO}=180 \mathrm{NSUB}=\overline{2} .8 \mathrm{E} 16 \mathrm{VMAX}=1.9 \mathrm{E} 5 \mathrm{ETA}=0.09 \mathrm{THETA}=0.13 \mathrm{KAPPA}=3 \mathrm{DELTA}=0.3$ $\mathrm{XJ}=0.0 \mathrm{U}$ NFS $=1 \mathrm{E} 12 \mathrm{RSH}=1400 \mathrm{RD}=0 \mathrm{RS}=0 \mathrm{CGDO}=1.85 \mathrm{E}-10 \mathrm{CGSO}=1.85 \mathrm{E}-10$ $\mathrm{CGBO}=2.5 \mathrm{E}-10 \mathrm{CJ}=5.2 \mathrm{E}-4 \mathrm{CJSW}=2.8 \mathrm{E}-10 \mathrm{MJ}=0.5 \mathrm{MJSW}=0.33 \mathrm{JS}=1 \mathrm{E}-3 \mathrm{FC}=0 \mathrm{~PB}=0.9$ $\mathrm{ACM}=2$ )
* 49-STAGE RING OSCILLATOR and 2-STAGE AMPLIFIER
xinvl 0123 RO_sub inv
xinv2 01222 RO_sub inv xinv3 $013222 \mathrm{RO}_{-}$sub inv xinv4 014232 RO_sub inv xinv5 015242 RO_subinv xinv6 016252 RO_sub inv xinv7 017262RO_subinv xinv8 018272 RO_sub inv xinv9 019282 RO_sub inv xinv10 0110292 RO_sub inv xinvl1 01112102 RO_sub inv xinv12 01122112 RO_sub inv xinv13 01132122 RO_sub inv xinv14 01142132 RO_sub inv xinv15 01152142 RO_sub inv xinv16 01162152 RO_sub inv xinv17 01172162 RO_sub inv xinv18 01182172 RO_sub inv xinv19 01192182 RO_sub inv xinv20 01202192 RO_sub inv xinv21 01212202 RO_sub inv xinv22 01222212 RO_sub inv xinv23 01232222 RO_sub inv xinv24 01242232 RO_sub inv xinv25 01252242 RO_sub inv xinv26 01262252 RO_sub inv xinv27 01272262 RO_sub inv xinv28 01282272 RO_sub inv xinv29 01292282 RO_sub inv xinv30 01302292 RO_sub inv xinv31 0 1312302 RO_sub inv xinv32 0 I 322312 RO_subinv xinv33 01332322 RO_sub inv xinv34 01342332RO_sub inv xinv35 01352342 RO_sub inv xinv36 01362352 RO_sub inv xinv37 01372362 RO_sub inv xinv38 01382372 RO_sub inv xinv39 01392382 RO_sub inv xinv40 01402392 RO_sub inv xinv41 01412402 RO_sub inv xinv42 01422412 RO_sub inv xinv43 01432422 RO_sub inv xinv44 01442432 RO_sub inv xinv45 01452442 RO_sub inv xinv46 01462452 RO_sub inv xinv47 01472462 RO_sub inv xinv48 01482472 RO_sub inv xinv49 013482 RO_sub inv
xamp50 56 out 10 ampsub amp

```
* DC BIAS SOURCES
Vd 105
Vb1502.5
Vb2602.5
* INITIAL CONDITIONS FOR RING OSCILLATOR
.IC V(482)=0 V(3)=1
* SUBSTRATE CONTACT RESISTANCES
Rsub_osc RO_sub substrate 0.9
Rsub_amp ampsub substrate 0.1
R_contact ampsub wafer 1
* INDUCTANCE OF THE SUBSTRATE CONNECTION
L_substrate wafer 0 10n
*
* OMIT THIS SECTION FOR SIMULATIONS WITHOUT GUARD RING
* GUARD RING DIODE w/ CONTACT RESISTANCE and SUBSTRATE CONTACT
INDUCTANCE
R_L_C_contact substrate node_p 0.1
DDIODE node_p node_n+ DIODE
L_RLC node_n+ Pos_terminal 10n
*
* SUBSTRATE BIAS - CHOOSE ONE OF THE FOLLOWING:
a) V_bias Pos_terminal \(0-0.400\)
b) V_bias Pos_terminal \(0-0.600\)
c) V_bias Pos_terminal \(0-0.525\)
* INVERTER SUBCIRCUIT .subckt inv 10001100120013001400
* VSS VDD OUT IN SUB
m 01200130011001100 P_INVERTER \(\mathrm{L}=2 \mathrm{U} \mathrm{W}=4.8 \mathrm{U}\) AS \(=25.92 \mathrm{P}\) AD \(=25.92 \mathrm{P}\) PS \(=20.4 \mathrm{U}\) \(+\mathrm{PD}=20.4 \mathrm{U}\)
m 1120013001000 s N_INVERTER L=2U W \(=4.8 \mathrm{U}\) AS \(=25.92 \mathrm{P}\) AD \(=25.92 \mathrm{P}\) PS \(=20.4 \mathrm{U}\) \(+\mathrm{PD}=20.4 \mathrm{U}\)
cw 1300 s 5.68 f
co 1200 s \(2.40 f\)
rl 1400 s 10
.ends inv
```

```
* AMPLIFIER SUBCIRCUIT
.subckt amp 200 300700 100 0 ampsub
* +IN -IN OUT VDD GND SUB
* DIFFERENTIAL INPUT STAGE
M1 500 500 100 100 P_AMP_80 L=1U W=80U AS=432P AD=432P PS = 170.8U
+PD=170.8U
M2600500 100 100 P_AMP_80 L=1U W=80U AS=432P AD=432P PS=170.8U
+PD=170.8U
M3 500 200 400 s1 N_AMP_50 L=1U W=50U AS=270P AD=270P PS =110.8U
+PD=110.8U
M4600300400 s2 N_AMP_50 L=1U W=50U AS=270P AD=270P PS = 110.8U
+PD=110.8U
* OUTPUT STAGE
M11700600 100 100 P_AMP_80 L= 1U W = 80U AS=432P AD=432P PS=170.8U
+PD=170.8U
M127008000 s3 N_AMP_50 L=1U W=50U AS=270P AD=270P PS =110.8U PD=110.8U
*BIAS TRANSISTORS
M5 400 800 0 s4 N_AMP_100 L=1U W=100U AS=540P AD=540P PS=210.8U
+PD=210.8U
M6 800 800 100 100 P_AMP_25 L=1U W=25U AS=135P AD=135P PS =60.8U PD =60.8U
M7 800 800 0 s5 N_AMP_50-L}=1\textrm{U}W=50U AS=270P AD=270P PS =110.8U PD=110.8U
* SUBSTRATE CONNECTIONS
rl sl ampsub }1
r2 s2 ampsub 10
r3 s3 ampsub 10
r4 s4 ampsub }1
r5 s5 ampsub 10
* STRAY CAPACITANCES FROM LAYOUT OF AMPLIFIER
c1 500 ampsub 41.7f
c2 200 ampsub 10.7f
c3600 ampsub 27.6f
c4 300 ampsub 10.8f
c5 700 ampsub 11.9f
.ends amp
* OUTPUT ANALYSIS
.op
.tran 0.01n 10n
.fft V(out,10000) start =0 stop=10n np=1024
.meas tran Vout_rms rms V(out,10000) from=2ns to = 10ns
.end
```


## APPENDIX B: MODEL FILE FOR NARROW BASE DIODE

.MODEL DIODE D (LEVEL $=1 \mathrm{IS}=5.6 \mathrm{E}-15 \mathrm{TT}=20 \mathrm{E}-9$ )

APPENDIX C: MODEL FILE FOR N-CHANNEL DEVICES

```
.MODEL N_CHANNEL NMOS(LEVEL=3 LD=0.15U WD=0.3U VTO=0.73
TOX=200E-10 UO=520 NSUB=2.8E16 VMAX = 1.35E5 ETA =0.02 THETA =0.07
KAPPA=0.1 DELTA=0.6 XJ=0.1U NFS=5E11 RSH=1000 RD=0 RS=0 CGDO = 1.85E-10
CGSO=1.85E-10 CGBO=2.5E-10 CJ=3.2E-4 CJSW =2.8E-10 MJ=0.95 MJSW =0.12
JS=1E-3 FC=0 PB=0.8 ACM=2)
```

APPENDIX D: MODEL FILE FOR P-CHANNEL DEVICES

$$
\begin{aligned}
& \text { MODEL P_CHANNEL PMOS(LEVEL }=3 \mathrm{LD}=0.0 \mathrm{U} \mathrm{WD}=0.4 \mathrm{U} \text { VTO }=-0.9 \text { TOX }=200 \mathrm{E}-10 \\
& \text { UO }=180 \mathrm{NSUB}=2.8 \mathrm{E} 16 \mathrm{VMAX}=1.9 \mathrm{E} 5 \mathrm{ETA}=0.09 \mathrm{THETA}=0.13 \mathrm{KAPPA}=3 \mathrm{DELTA}=0.3 \\
& \mathrm{XJ}=0.0 \mathrm{U} \mathrm{NFS}=1 \mathrm{E} 12 \text { RSH }=1400 \mathrm{RD}=0 \mathrm{RS}=0 \mathrm{CGDO}=1.85 \mathrm{E}-10 \mathrm{CGSO}=1.85 \mathrm{E}-10 \\
& \mathrm{CGBO}=2.5 \mathrm{E}-10 \mathrm{CJ}=5.2 \mathrm{E}-4 \mathrm{CJSW}=2.8 \mathrm{E}-10 \mathrm{MJ}=0.5 \mathrm{MJSW}=0.33 \mathrm{JS}=1 \mathrm{E}-3 \mathrm{FC}=0 \mathrm{~PB}=0.9 \\
& \mathrm{ACM}=2)
\end{aligned}
$$

## APPENDIX E: LAYOUT OF CMOS AMPLIFIER



## APPENDIX F: LAYOUT OF RING OSCILLATOR



## APPENDIX G: LAYOUT OF CMOS INVERTER CELL



## APPENDIX H: FREQUENCY RESPONSE OF AMPLIFIER



## APPENDIX I: HSPICE CIRCUIT FILE FOR AMPLIFIER

```
*Circuit File for CMOS Differential Amplifier With Output Stage
.options post
* POWER and INPUT SIGNAL
VDD 1 0 DC 5V
VIN120 DC 2.5V
VIN2 30 DC 2.5V AC 0.001V
* AMPLIFIER CIRCUIT
M15511 P_AMP_80 L= 1U W = 80U
M2 6511 P_AMP_80 L=1U W=80U
M35240N_AMP_50 L=1U W=50U
M46340N_AMP_50 L= 1U W=50U
* OUTPUT STAGE
M117611P_AMP_80 L= 1U W = 80U
M127800 N_AMP_50 L=1UW W = 50U
*BIAS CIRCUIT
M54800N_AMP_100 L= 1U W=100U
M68811 P_AMP_25 L=1U W=25U
M78800N_AMP_50 L=1U W=50U
```

.$M O D E L$ N NMOS(LEVEL $=3 \mathrm{LD}=0.15 \mathrm{U}$ WD $=0.3 \mathrm{U}$ VTO $=0.73 \mathrm{TOX}=200 \mathrm{E}-10$
$+\mathrm{UO}=520 \mathrm{NSUB}=2.8 \mathrm{E} 16 \mathrm{VMAX}=1.35 \mathrm{E} 5 \mathrm{ETA}=0.02 \mathrm{THETA}=0.07 \mathrm{KAPPA}=0.1$

+ DELTA $=0.6 \mathrm{XJ}=0.1 \mathrm{U} \mathrm{NFS}=5 \mathrm{E} 11 \mathrm{RSH}=1000 \mathrm{RD}=0 \mathrm{RS}=0$
$+\mathrm{CGDO}=1.85 \mathrm{E}-10 \mathrm{CGSO}=1.85 \mathrm{E}-10 \mathrm{CGBO}=2.5 \mathrm{E}-10 \mathrm{CJ}=3.2 \mathrm{E}-4 \mathrm{CJSW}=2.8 \mathrm{E}-10$
$+\mathrm{MJ}=0.95 \mathrm{MJSW}=0.12 \mathrm{JS}=1 \mathrm{E}-3 \mathrm{FC}=0 \mathrm{~PB}=0.8 \mathrm{ACM}=2$ )
.MODEL N_AMP_50 NMOS(LEVEL $=3 \mathrm{LD}=0.15 \mathrm{U}$ WD $=0.3 \mathrm{U}$ VTO $=0.73$ TOX $=200 \mathrm{E}-10$
$+\mathrm{UO}=520 \mathrm{NSUB}=2.8 \mathrm{E} 16 \mathrm{VMAX}=1.35 \mathrm{E} 5 \mathrm{ETA}=0.02 \mathrm{THETA}=0.07 \mathrm{KAPPA}=0.1$
+ DELTA $=0.6 \mathrm{XJ}=0.1 \mathrm{U} \mathrm{NFS}=5 \mathrm{E} 11 \mathrm{RSH}=20 \mathrm{RD}=0 \mathrm{RS}=0$
$+\mathrm{CGDO}=1.85 \mathrm{E}-10 \mathrm{CGSO}=1.85 \mathrm{E}-10 \mathrm{CGBO}=2.5 \mathrm{E}-10 \mathrm{CJ}=3.2 \mathrm{E}-4 \mathrm{CJSW}=2.8 \mathrm{E}-10$
$+\mathrm{MJ}=0.95 \mathrm{MJSW}=0.12 \mathrm{JS}=1 \mathrm{E}-3 \mathrm{FC}=0 \mathrm{~PB}=0.8 \mathrm{ACM}=2$ )
* $\mathrm{RSH}=1000 / 50=20$
.MODEL N_AMP_100 NMOS(LEEVEL $=3 \mathrm{LD}=0.15 \mathrm{U} \mathrm{WD}=0.3 \mathrm{U}$ VTO $=0.73$ TOX $=200 \mathrm{E}-10$
$+\mathrm{UO}=520 \mathrm{NSUB}=2.8 \mathrm{E} 16 \mathrm{VMAX}=1.35 \mathrm{E} 5 \mathrm{ETA}=0.02 \mathrm{THETA}=0.07 \mathrm{KAPPA}=0.1$
+ DELTA $=0.6 \mathrm{XJ}=0.1 \mathrm{U} \mathrm{NFS}=5 \mathrm{E} 11 \mathrm{RSH}=10 \mathrm{RD}=0 \mathrm{RS}=0$
$+\mathrm{CGDO}=1.85 \mathrm{E}-10 \mathrm{CGSO}=1.85 \mathrm{E}-10 \mathrm{CGBO}=2.5 \mathrm{E}-10 \mathrm{CJ}=3.2 \mathrm{E}-4 \mathrm{CJSW}=2.8 \mathrm{E}-10$
$+\mathrm{MJ}=0.95 \mathrm{MJSW}=0.12 \mathrm{JS}=1 \mathrm{E}-3 \mathrm{FC}=0 \mathrm{~PB}=0.8 \mathrm{ACM}=2$ )
* $\mathrm{RS}=1000 / 100=10$
.MODEL P PMOS(LEVEL $=3 \mathrm{LD}=0.0 \mathrm{U} \mathrm{WD}=0.4 \mathrm{U}$ VTO $=-0.9$ TOX $=200 \mathrm{E}-10$
$+\mathrm{UO}=180 \mathrm{NSUB}=2.8 \mathrm{E} 16 \mathrm{VMAX}=1.9 \mathrm{E} 5 \mathrm{ETA}=0.09 \mathrm{THETA}=0.13 \mathrm{KAPPA}=3$
+ DELTA $=0.3 \mathrm{XJ}=0.0 \mathrm{U}$ NFS $=1 \mathrm{E} 12 \mathrm{RSH}=1400 \mathrm{RD}=0 \mathrm{RS}=0$
$+\mathrm{CGDO}=1.85 \mathrm{E}-10 \mathrm{CGSO}=1.85 \mathrm{E}-10 \mathrm{CGBO}=2.5 \mathrm{E}-10 \mathrm{CJ}=5.2 \mathrm{E}-4 \mathrm{CJSW}=2.8 \mathrm{E}-10$
$+\mathrm{MJ}=0.5 \mathrm{MJSW}=0.33 \mathrm{JS}=1 \mathrm{E}-3 \mathrm{FC}=0 \mathrm{~PB}=0.9 \mathrm{ACM}=2$ )
.MODEL P_AMP_80 PMOS(LEVEL $=3$ LD $=0.0 \mathrm{U} \mathrm{WD}=0.4 \mathrm{U}$ VTO $=-0.9 \mathrm{TOX}=200 \mathrm{E}-10$
$+\mathrm{UO}=180 \mathrm{NSUB}=2.8 \mathrm{E} 16 \mathrm{VMAX}=1.9 \mathrm{E} 5 \mathrm{ETA}=0.09 \mathrm{THETA}=0.13 \mathrm{KAPPA}=3$
+ DELTA $=0.3 \mathrm{XJ}=0.0 \mathrm{U} \mathrm{NFS}=1 \mathrm{E} 12 \mathrm{RSH}=17.5 \mathrm{RD}=0 \mathrm{RS}=0$
$+\mathrm{CGDO}=1.85 \mathrm{E}-10 \mathrm{CGSO}=1.85 \mathrm{E}-10 \mathrm{CGBO}=2.5 \mathrm{E}-10 \mathrm{CJ}=5.2 \mathrm{E}-4 \mathrm{CJSW}=2.8 \mathrm{E}-10$
$+\mathrm{MJ}=0.5 \mathrm{MJSW}=0.33 \mathrm{JS}=1 \mathrm{E}-3 \mathrm{FC}=0 \mathrm{~PB}=0.9 \mathrm{ACM}=2$ )
* $\mathrm{RSH}=1400 / 80=17.5$
.MODEL P_AMP_25 PMOS(LEVEL $=3 \mathrm{LD}=0.0 \mathrm{U} \mathrm{WD}=0.4 \mathrm{U}$ VTO $=-0.9 \mathrm{TOX}=200 \mathrm{E}-10$
$+\mathrm{UO}=180 \mathrm{NSUB}=2.8 \mathrm{E} 16 \mathrm{VMAX}=1.9 \mathrm{E} 5 \mathrm{ETA}=0.09 \mathrm{THETA}=0.13 \mathrm{KAPPA}=3$
+ DELTA $=0.3 \mathrm{XJ}=0.0 \mathrm{U}$ NFS $=1 \mathrm{E} 12 \mathrm{RSH}=56 \mathrm{RD}=0 \mathrm{RS}=0$
$+\mathrm{CGDO}=1.85 \mathrm{E}-10 \mathrm{CGSO}=1.85 \mathrm{E}-10 \mathrm{CGBO}=2.5 \mathrm{E}-10 \mathrm{CJ}=5.2 \mathrm{E}-4 \mathrm{CJSW}=2.8 \mathrm{E}-10$
$+\mathrm{MJ}=0.5 \mathrm{MJSW}=0.33 \mathrm{JS}=1 \mathrm{E}-3 \mathrm{FC}=0 \mathrm{~PB}=0.9 \mathrm{ACM}=2$ )
* $\mathrm{RSH}=1400 / 25=56$
*ANALYSIS
.OP
.AC DEC 10 kk 100E9
.END

