

AN ABSTRACT OF THE THESIS OF

Arathi Sundaresan for the degree of Master of Science in Electrical and Computer Engineering presented on May 30, 2006.

Title: Ground Tap Placement and Sizing to Minimize Substrate Noise Coupling in RF LNAs.

Abstract approved:

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The substrate noise injected by a stepped buffer circuit into two single-ended 1.5GHz low noise amplifiers is examined for a heavily doped 0.25 $\mu$ m CMOS process. The difference in the LNA noise rejection is characterized as a function of the size and placement of substrate contacts.

The use of a resistive model for the substrate, and SPICE models for the interconnect and passive device parasitics give good correlation between the measured and simulated results. A reduction of 2-12dB is achieved for the intermodulation products, with larger

substrate contacts. It is shown that large ground taps placed in close proximity to the input transistor are most effective in suppressing the IM levels

A detailed examination of the noise injection mechanisms in a stepped buffer shows that the injected noise is a strong function of the layout of the buffer interconnects.

Proposed methods to reduce the injected noise result in improvements of 9-11 dB.

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Ground Tap Placement and Sizing to Minimize Substrate Noise Coupling in RF LNAs

by

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Arathi Sundaresan, Author

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# GROUND TAP PLACEMENT AND SIZING TO MINIMIZE SUBSTRATE NOISE COUPLING IN RF LNAs

## 1. INTRODUCTION

Continued advances in semiconductor processing technologies have given way to unprecedented levels of integration. Systems on a chip, with their attractive form factor, reduced cost, and lower power consumption have become the preferred solution for today's high performance wireless communication and consumer electronics.

This integration of digital, analog, and RF circuitry on the same silicon chip comes at the expense of undesired noise coupling. Figure 1.1 depicts the mechanism of noise coupling in mixed-signal ICs. The switching activity of the digital logic

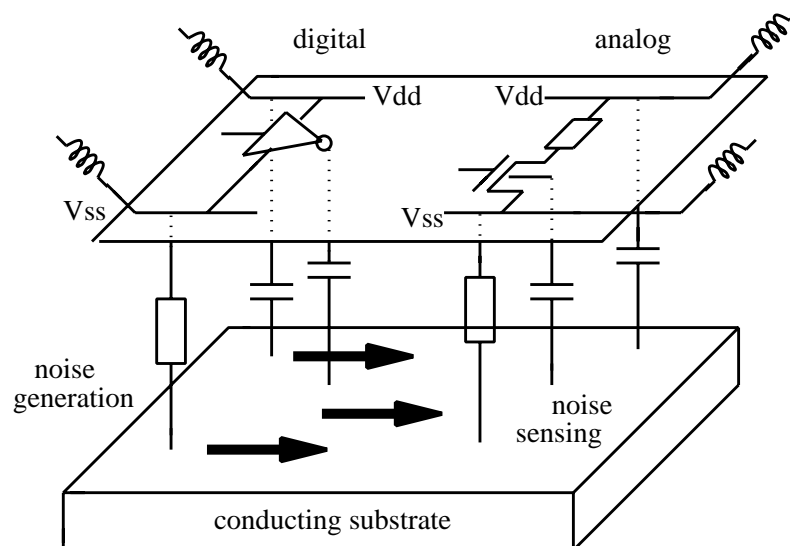


Figure 1.1. Mixed-signal substrate noise problem.

gates induces noise, which propagates through the supply lines and the non-insulating silicon substrate, adversely affecting the performance of sensitive analog and RF blocks placed on the same die [1-7]. With shrinking dimensions, this problem gets exacerbated, making research in the area of noise mitigation strategies a necessity [8].

Extensive research has been done previously on ways to tackle the issue of noise coupling in mixed-signal environments. Substrate noise reduction methods implemented to date, fall under the broad category of circuit level and physical level techniques. The former category includes design techniques that reduce the amount of injected noise [9-13], improve the substrate noise immunity of circuits [5] or cancel the generated substrate noise [7,14-16]. From a layout perspective, the orientation and placement of the noise sensitive blocks with respect to the noise source have been shown to be of significance [17]. The effect of power splitting and supply line routing has been considered in [18]. The use of guard rings for isolating sensitive circuitry has been extensively studied in [19-20]. Many of these techniques are being put to wide use today.

This thesis extends on previous research by examining another approach to circuit isolation. It focuses on employing substrate contacts, as a means to reduce noise. Although it is well known that an increase in the size of substrate contacts reduces the coupled noise, this effect has not been previously quantified. A systematic evaluation of the noise coupling and substrate tap sizing using measured and simulated data is provided for the first time in this work. Specifically, the influence of the sizing of ground taps on the noise performance of an RF LNA fabricated in a heavily doped



process is examined. The importance of low noise performance for an RF LNA makes it an ideal test vehicle for substrate noise evaluation. An insight into the actual improvement brought about by larger substrate contacts and the trade off in terms of the additional area occupied would help to evaluate the effectiveness of this technique. This evaluation is what is intended through this study.

Limitations of conventional noise reduction methods such as physical separation between analog and digital circuits and the use of guard rings for the heavily doped substrate makes this substrate type an ideal choice for this research. The reduced effectiveness of these methods arises due to the low resistive bulk of the heavily doped process. This makes any new method for substantial noise reduction in this substrate an attractive finding.

Two LNAs fabricated in a  $0.25\mu\text{m}$  CMOS process were examined in this work. The popular single-ended cascode architecture with inductive source degeneration was chosen. The two circuits differing in their substrate contact layouts were compared for their substrate noise coupling performance. Detailed simulations were performed for systematically scaled substrate tap areas, and the resulting improvements in the LNA noise performance were quantified. Additional simulations were carried out to identify substrate contact locations that would produce the largest noise reduction.

An analysis of substrate noise coupling in a mixed-signal system would be incomplete without addressing the issue of noise injection. Accordingly, this work also examines the noise generation in the stepped buffer circuit. Its various noise

injection mechanisms are identified and evaluated, and methods to reduce the noise are also proposed.

This thesis is organized as follows. The test circuits and the experimental setup are described in Section 2. The method for substrate noise modeling adopted in this work is detailed in Section 3. Section 4 presents the measured results. This is followed by analysis of the measured results and simulation of the effect of substrate contact sizing and location on the observed noise levels, in Section 5. Section 6 presents a detailed analysis of the noise injection mechanisms in the stepped buffer and finally, Section 7 provides concluding remarks.

## 2. TEST CIRCUITS

In this work, the effect of the noise generated by a stepped buffer circuit on a single-ended LNA is examined. This section provides a description of the test setup and details the design and layout of the buffer and amplifier circuits.

The test chip was fabricated in a 0.25 $\mu\text{m}$  heavily doped CMOS five metal, single poly process. A photograph of the packaged chip is provided in Figure 2.1. The LNA circuits occupy two corners as labeled in the figure. The stepped buffer circuits are placed adjacent to the amplifiers.

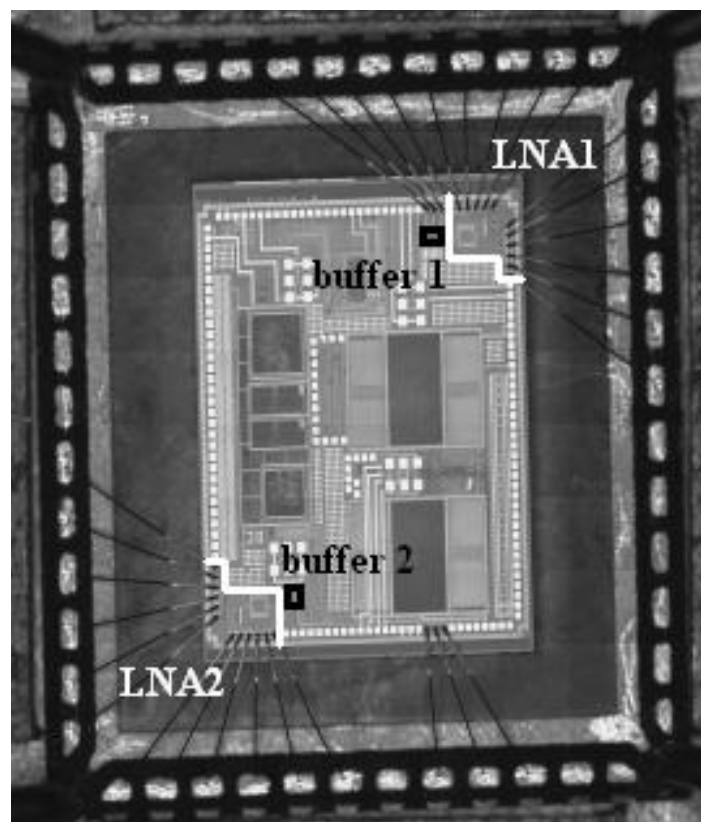


Figure 2.1. Photograph of packaged die.

## 2.1. Stepped Buffer

The stepped buffer is a digital circuit that finds use in many mixed-signal integrated circuits (ICs) as a driver for clock and output signals. The design of the buffer used to emulate the digital switching noise is described in [21]. The circuit comprises seven inverter stages, with each successive stage being a factor of  $e$  (2.718) larger than the preceding one as shown in Figure 2.2. Additionally, every stage except the last is loaded with another inverter to provide increased levels of noise injection.

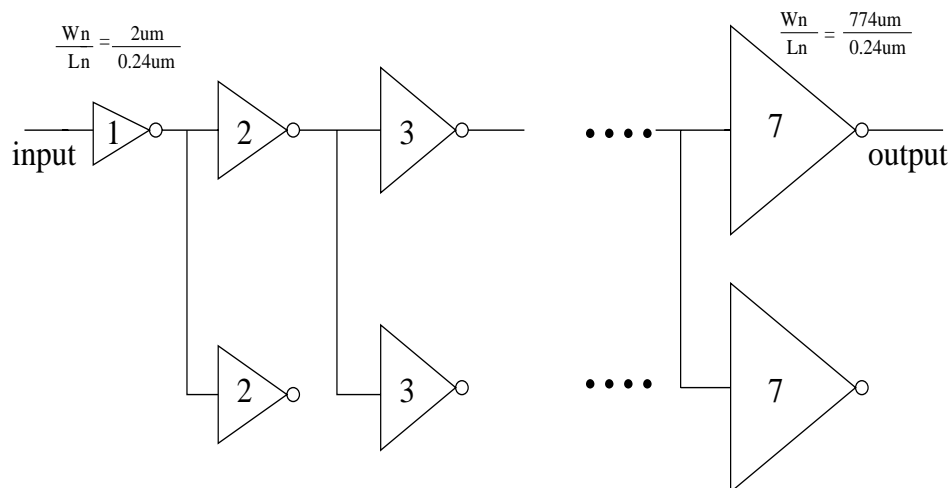


Figure 2.2. Stepped buffer circuit.

Two buffer circuits are laid out, one next to each of the LNAs under test. Each buffer is placed in close proximity to the LNA on which the effects of its noise injection are measured. The buffers each have an individual set of power, ground, and input pins.

## 2.2. Single-ended LNA

### 2.2.1. Circuit design

The design methodology for the amplifier is outlined in [22]. Figure 2.3 shows the single-ended amplifier topology with its inductively degenerated common source input transistor M0, biased by M2 and cascoded with the common gate output transistor M1. The circuit operates at 1.5GHz, with a power consumption of 8mW. This frequency range of operation makes the LNA suitable for global positioning system (GPS) applications. The input and output device dimensions that minimized

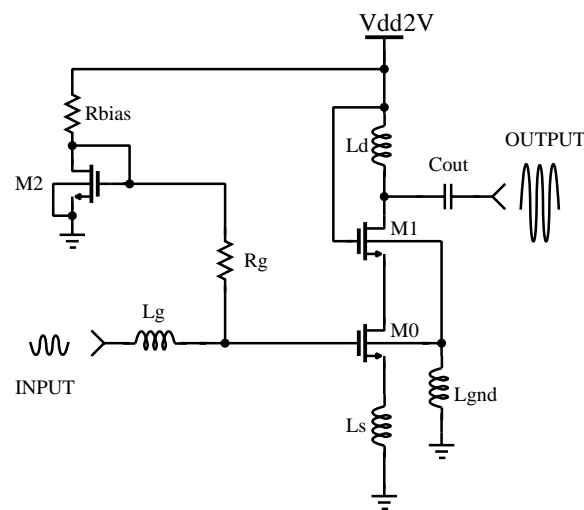


Figure 2.3. Circuit schematic of the single-ended LNA.

the overall noise figure were used. The source, gate and drain inductors, and the output capacitor were sized to match the input and output at the operating frequency.

### 2.2.2. Circuit Layout

The two LNAs are laid out on diagonally opposite corners of the die, to ensure similar package bond wire lengths for their corresponding pins. Both the layouts include a shielded input bond pad [23] to improve the circuit's noise performance. The source degeneration inductors are realized as bond wires, while the gate inductors are placed off-chip to enable post-fabrication input tuning to compensate for deviation from expected values of bond wire and board trace inductances. The drain inductor and output capacitor are implemented on-chip. An off-chip inductor  $L_{out}$  placed in series with  $C_{out}$  serves the same role at the output as that of the off-chip gate inductor at the input. The chip ground connects to the PCB ground through a low impedance path provided by four bond wires.

The two LNA layouts are identical in all respects except for the placement and sizing of their substrate contacts. The die photos of the two LNAs are provided in Figures 2.4 and 2.5. In subsequent sections, the layouts in Figure 2.4 and Figure 2.5 will be referred to as LNA1 and LNA2, respectively. LNA1 has fewer substrate taps, the exact number and sizing selected as prescribed by the design rules for the technology. They are realized as  $0.6\mu\text{m}$  wide sections with lengths ranging between  $10\mu\text{m}$  and  $20\mu\text{m}$ , placed alongside each of the three transistors. The combined area of these taps is  $60\mu\text{m}^2$ . LNA2 has its p+ contacts placed together to form a ground grid, which spans 400 times the area of the LNA1 taps, as highlighted and labeled in Figure 2.4.

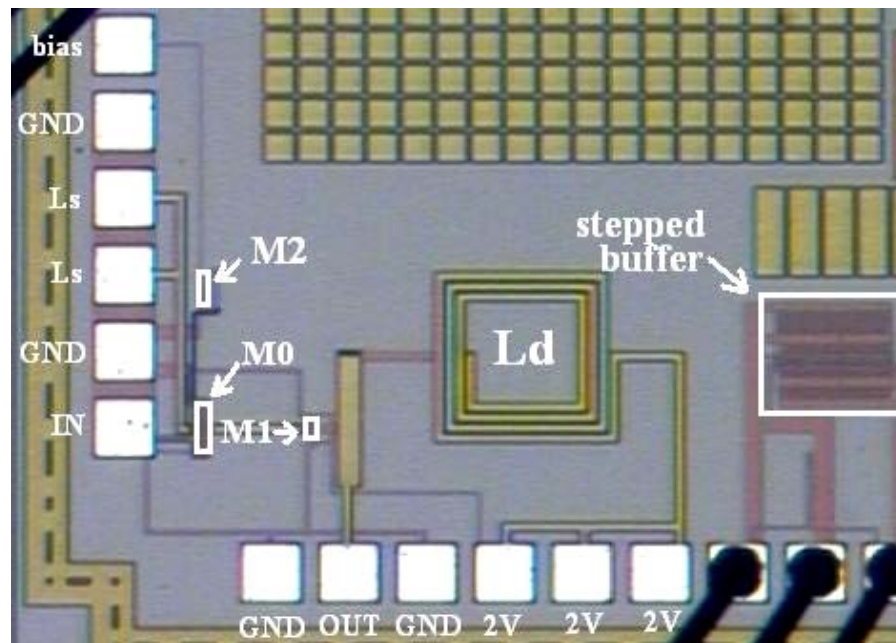


Figure 2.4. Die photograph of LNA1.

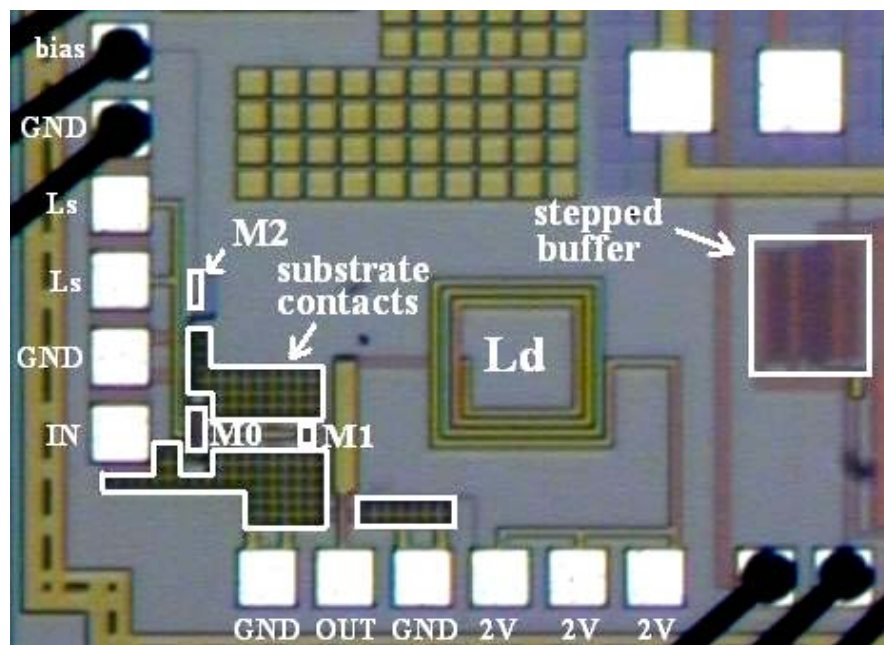


Figure 2.5. Die photograph of LNA2.

Additionally,  $0.6\mu\text{m}$  wide guard rings are placed around the input and cascode transistors M0 and M1, respectively. This was done to compare the reduction in noise levels brought about by the increased ground tap size with that resulting from a conventional guard ring structure.

### **2.3. Package and Printed Circuit Board**

The die was assembled in a 48-pin micro lead frame plastic package. The exposed bottom side of the die paddle enabled its direct soldering to the PCB ground plane. Non-conductive epoxy was used to attach the chip to the die paddle. The packaged die was mounted on a 2 layer, 31mil thick FR4 test board. The buffers operate with a 2.5V supply, while the LNAs use 2V supplies. The isolated on-chip digital and analog grounds were connected together on the test board. A detailed description of the PCB can be found in Appendix A.



### 3. MODELING

#### 3.1. Circuit Modeling

The switching activity of the buffer circuit causes current spikes in its power and ground lines. Owing to the parasitic inductors in these lines, the current spikes generate  $Ldi/dt$  noise, also known as ground bounce and supply droop, which gets coupled to the substrate via its substrate contacts. Another direct mode of coupling for the switching voltages is through the transistor junction capacitances and the input and output interconnect capacitances [24]. Thus, accurate interconnect modeling becomes mandatory for matching actual injected noise levels. Accurate models for the buffer power, ground, input and output lines on the die were obtained from TSMC 0.25 $\mu\text{m}$  process documentation and S-parameter simulation results from Momentum [25]. The PCB and package parasitics were also incorporated into the simulation. A detailed description of the models used is provided in Appendix B.

The LNA transistors sense fluctuations induced in the substrate by noisy blocks placed on the same die, through their pn junction and interconnect capacitances and by means of the “body effect” [26]. SPICE models for critical on-chip interconnects and bond pads were included. Three dimensional electromagnetic (EM) simulation results from the package manufacturer were used to create a package model. The bond wires self and mutual inductance values were obtained from FastHenry [27], and by using geometric approximations outlined by the EIA/JESD59 bond wire

modeling standard. Bond wire capacitances were modeled using FastCap [28]. A high frequency 3D EM simulation tool (HFSS) [29] was employed to provide S-parameter models for the controlled impedance input and output traces on the PCB.

### 3.2. Substrate Modeling

The silicon substrate, lacking purely isolative properties, acts as a noise propagation medium between circuit blocks placed on the same die. Substrates used in CMOS technologies are either heavily doped or lightly doped depending on their doping levels. The heavily doped substrate commonly used to combat latch up problems is used in this work. The doping profile can be represented by a three-layer approximation as shown in Figure 3.1. The thickness and resistivity of each layer is indicated.



Figure 3.1. Doping profile of the heavily doped substrate.

The substrate modeling approach considers every point in the circuit, which is relevant from the perspective of noise coupling as a contact. The substrate itself is treated as a resistive mesh [26] that connects each of these contacts to every other contact through a mutual resistance  $R_{ij}$ , and to the die backplane via a self-resistance  $R_{ji}$ . The NMOS transistor active areas, the interconnects, and the substrate taps are chosen as the contacts which represent the substrate coupling mechanisms, for this work. The contact layout data is an input to a Green's function based solver, EPIC [30], which generates the resistive network.

A simplified cross section of the heavily doped substrate, indicating the resistors taken into account for the noise simulations is provided in Figure 3.2. The presence

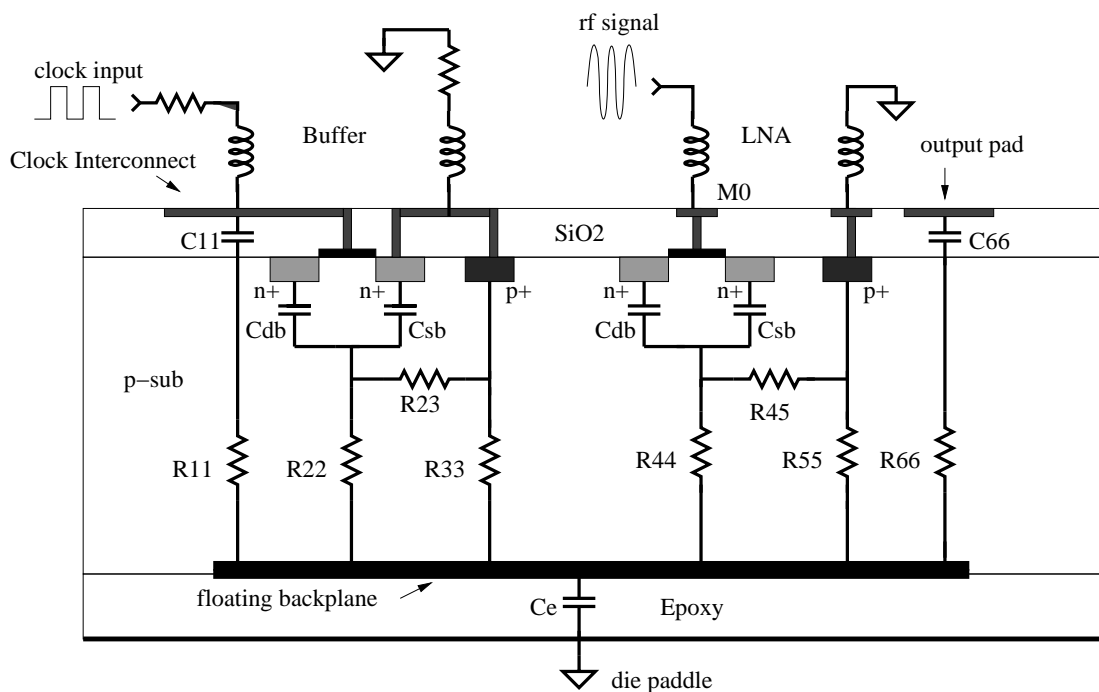


Figure 3.2. Cross-section of the heavily doped substrate showing the important coupling elements.

of the fairly ohmic epitaxial layer results in very large lateral resistances between contacts separated by distances larger than five times the epitaxial layer thickness [19]. This forces all the noise to flow directly into the substrate. The low resistance of this substrate makes the single node approximation for the backplane valid. All the self-resistances are connected to this common backplane. The large lateral resistances between widely spaced contacts are ignored. Of more significance are the mutual resistances between closely spaced contacts such as the MOSFETs and their bulk contacts, as depicted by  $R_{23}$  and  $R_{45}$ . The MOSFET junction capacitances that are part of the BSIM3V3 device model are labeled as  $C_{sb}$  and  $C_{db}$ .  $C_{11}$  and  $C_{66}$  represent the buffer input interconnect capacitance and the LNA output bond pad capacitance to the substrate, respectively. The non-conductive epoxy used to attach the die to the die paddle is modeled as a capacitance  $C_e$ .

## 4. MEASUREMENT RESULTS

### 4.1. Measurement Setup

S-parameter measurements were performed for LNA1 and LNA2 using an Agilent 8720 network analyzer. Substrate noise analysis was carried out by measuring the noise levels at the LNA outputs, resulting from the switching activity of the stepped buffers. Independent supplies for the four circuits made it possible to power off LNA2 and buffer 2 while monitoring the effect of buffer 1 on LNA1, and vice-versa, as illustrated by the top-level test layout shown in Figure 4.1. The buffers were clocked using a 2Vp-p, 50% duty cycle, 39MHz square wave generated by a Tektronix AWG520 waveform generator. A -18dBm sinusoidal signal from an Agilent 8665A signal generator was the input to the LNA under test. The LNA output spectrum was observed using an Agilent E4440A spectrum analyzer.

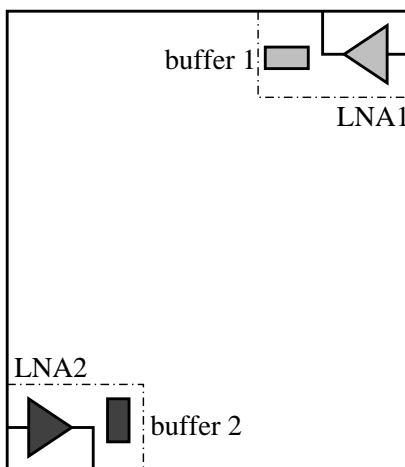


Figure 4.1. Test layout.

## 4.2. S-parameter Measurements

The measured S-parameters for LNA1 and LNA2 are shown in Figures 4.2 and 4.3, respectively. The losses arising from the test PCB account for the low forward gain of the LNA.

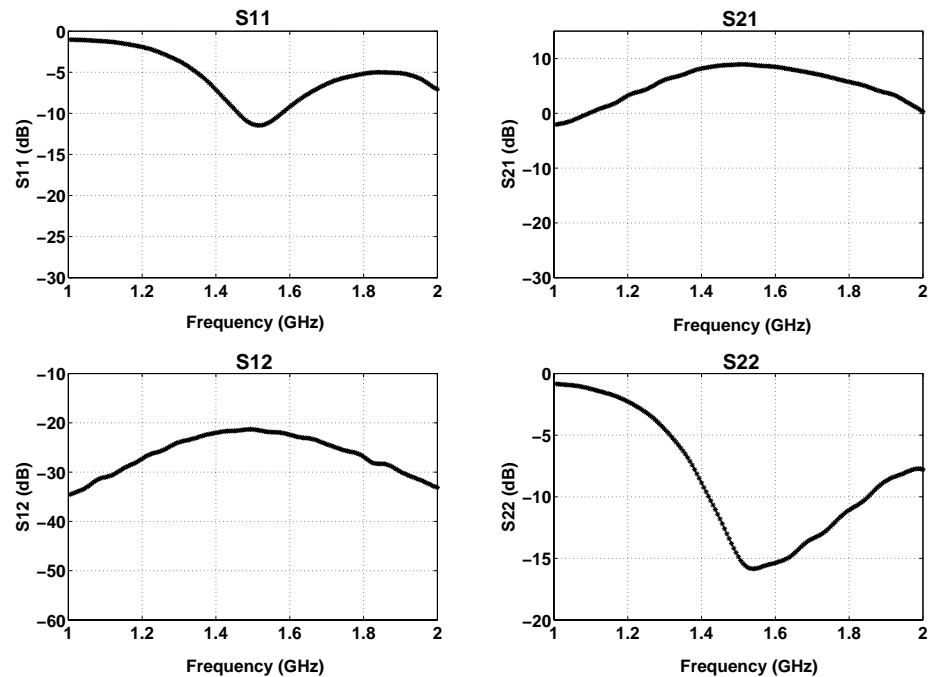


Figure 4.2. Measured S-parameters for LNA1.

To provide an effective comparison, and evaluate the influence of ground taps on the amplifier's noise rejection ability, the two LNAs are required to show conformity in their performance. The S-parameters, which effectively characterize the RF performance of the LNA, can be used as a standard for comparing the two circuits. It can be observed from Table 4.1 that the S-parameters are in reasonably good

agreement in a narrow band around 1.5GHz. It is deduced that the S-parameters do not completely match, due to asymmetries in the routing of the board traces.

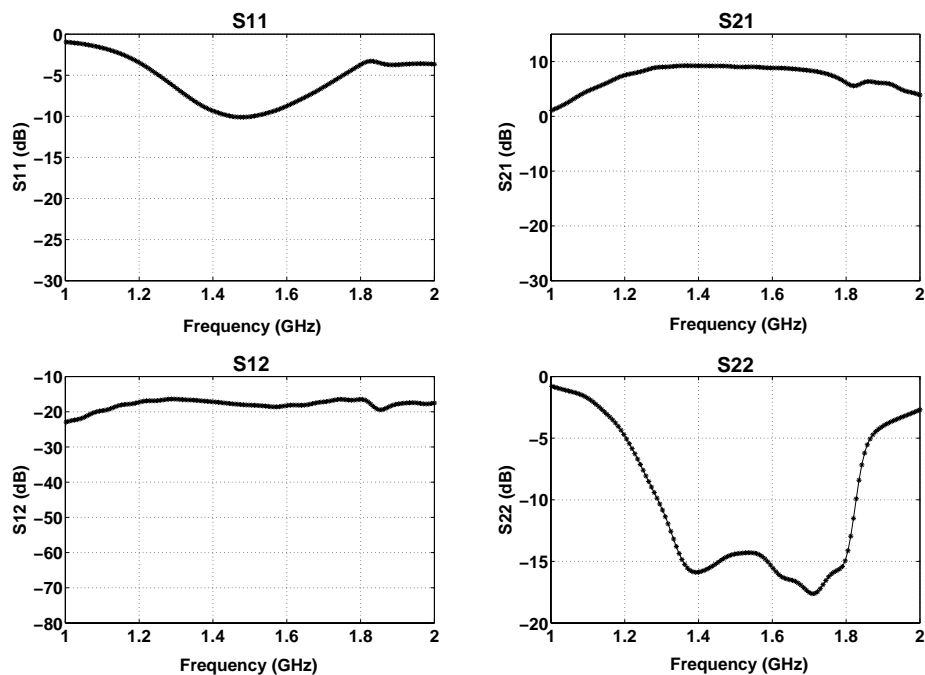


Figure 4.3. Measured S-parameters for LNA2.

Table 4.1. Measured performance of LNA1 and LNA2 at 1.5GHz.

	<b>LNA1</b>	<b>LNA2</b>
<b>S11 (dB)</b>	-11.3	-10.0
<b>S21 (dB)</b>	8.9	9.0
<b>S12 (dB)</b>	-21.3	-18.1
<b>S22 (dB)</b>	-14.9	-14.4

### 4.3. Substrate Noise Measurements

The noise injected by buffer 1 and buffer 2 appear at the output of the corresponding LNAs as shown in Figures 4.4 and 4.5, respectively. The spectrums clearly reveal the desired RF signal, and the unwanted noise levels resulting from the

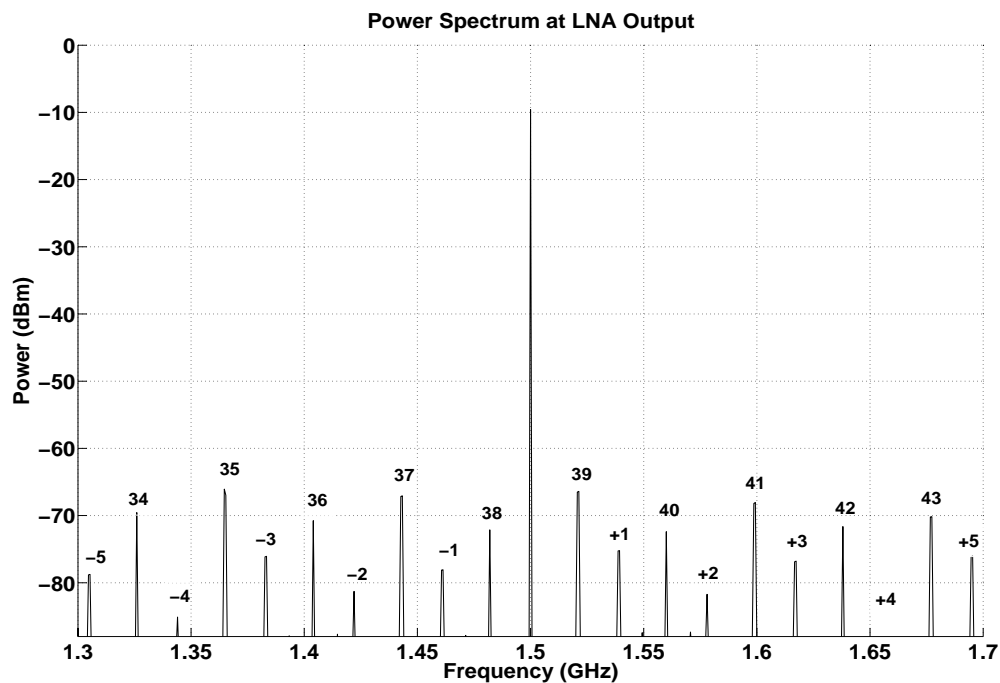


Figure 4.4. Noise injected by buffer 1 as seen at the output of LNA1.

buffer clock. An observation window spanning 400MHz around the signal was selected. The 1.5GHz RF signal is surrounded by the odd and even harmonics of the 39MHz clock. The harmonic tones that show up in the bandwidth of interest around the RF signal are the 34<sup>th</sup> - 43<sup>rd</sup> harmonics of the clock. Also seen, are the intermodulation (IM) tones, which are a result of the mixing of the low order clock



harmonics with the RF carrier. The IM terms arising from the 1<sup>st</sup> – 5<sup>th</sup> harmonics appear in the spectrum.

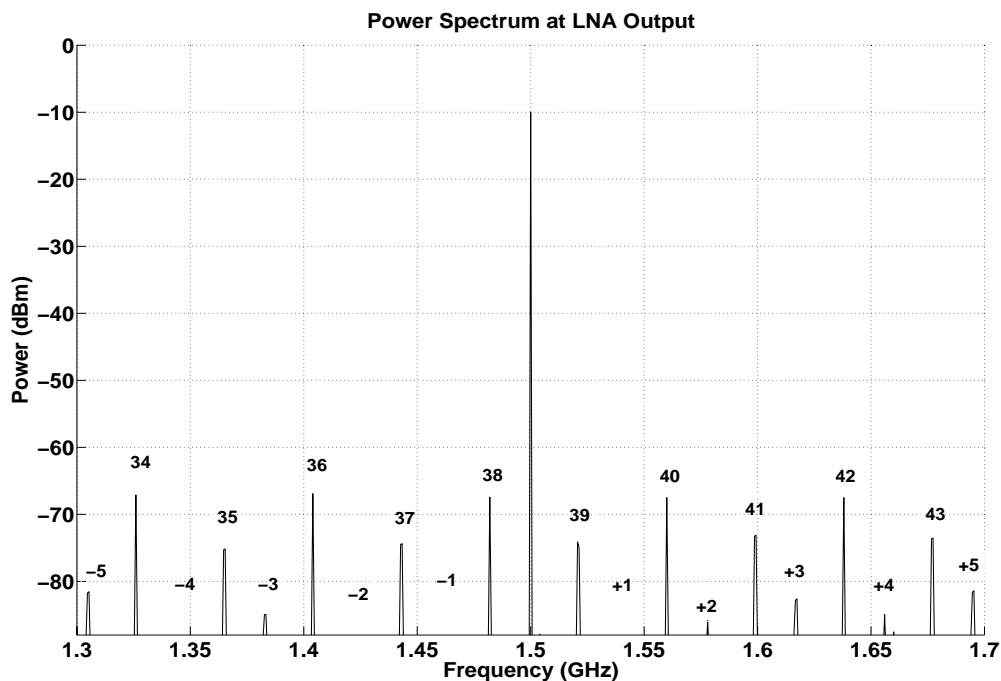


Figure 4.5. Noise injected by buffer 2 as seen at the output of LNA2.

It is evident from the measured spectrums that the increased substrate contacts lead to substantially lower IM noise levels in LNA2. The IM level decrease is in the range of 2-12dB, with the largest drop observed in the case of the 1<sup>st</sup> IM products labeled as +1 and -1 in Figures 4.4 and 4.5. A detailed interpretation of this result is provided in Section 5.

The harmonic noise coupling into the two LNAs exhibits dissimilarities, as seen from Figures 4.4 and 4.5. While LNA1 shows lower even harmonics, the opposite is

true for LNA2. This difference in behavior is unrelated to the sizing of the LNA substrate contacts. It is shown in Section 5 that this variation can be attributed to the noise injector, and is actually a product of the differences in the power and input routing of the two buffer circuits.

## 5. ANALYSIS OF NOISE COUPLING TO THE LNA

### 5.1. Interpretation of Measured Results

It can be seen from the measurements presented in Figures 4.4 and 4.5 that the harmonic noise levels are not matched for the two LNAs. While the odd harmonics are higher in LNA1, the opposite trend is observed for LNA2. The harmonics of the clock find a direct path to the amplifier output through its passive circuitry. It was shown in [22] that in a heavily doped substrate, almost 95% of the harmonic noise reaches the LNA output via the supply and output bond pads of the LNA, and the

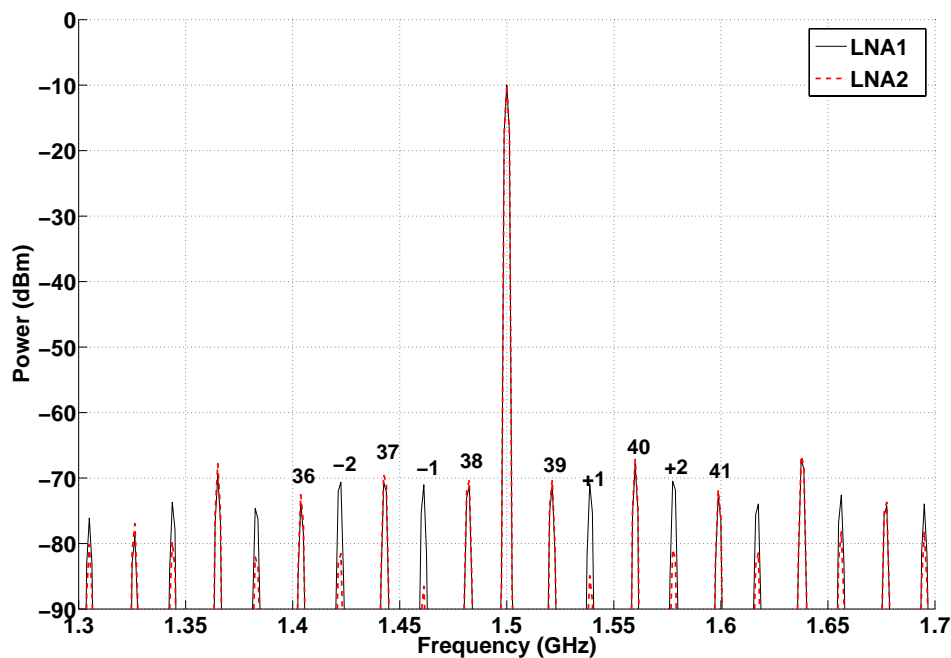


Figure 5.1. Simulated results showing the influence of ground tap sizing on the noise performance of LNA1 and LNA2 for identical buffer interconnect models.

drain inductor  $L_d$ . Since both the LNAs are identical in this respect, this variation is attributed to the noise injecting blocks. Figure 5.1 shows simulation results for the output spectrum of LNA1 and LNA2 with identical stepped buffer interconnect models. The model used is the one corresponding to buffer 2. It can be seen that the harmonic noise levels are similar in both cases. From this simulation, it is clear that the LNA substrate taps affect only the intermodulation noise coupling. Furthermore, the differences in the power, input, and output routing of the two buffer circuits are responsible for the unmatched harmonic levels at the LNA output. This is shown in the analysis presented in Section 6.

A comparison of the IM levels in Figures 4.4 and 4.5 shows the superior noise rejection of LNA2, owing to its larger substrate contacts. The reduction ranges between 2dB and 12dB, with the largest drop observed for the 1<sup>st</sup> IM products. Thus, while an increase in the ground tap area has a negligible effect on the coupled harmonic levels, it significantly reduces the IM levels. The salient coupling mechanisms for the IM noise were presented in [22]. It was shown that a predominant portion of the IM noise power is due to coupling into the bulk node of the input transistor M0, from the single substrate node, through the self-resistance  $R_{44}$ , as indicated in Figure 3.2. The varying effect of ground tap area on the harmonic and IM levels at the output is due to the different separations of the output pad and the input transistor bulk node from the ground tap. While the bulk node of the transistor, which is the dominant point of coupling for the clock harmonics that generate the IM products, lies in close proximity to the substrate tap, the output pad to which the

harmonics directly couple, is far removed from the taps. As a result of the large separation between the ground taps and the output pad, the self resistance of the pad to the backplane is relatively independent of contact scaling, which makes the noise coupling through the pad independent of contact area. On the other hand, due to its close proximity to the taps, the mutual resistance between the input transistor bulk node and the substrate taps, denoted by  $R_{45}$ , plays a significant role in reducing the coupled noise levels. The increased tap area reduces the value of  $R_{45}$ , which steers the noise away from the transistor bulk into the ground tap. With lesser noise coupling into the transistor, the IM products generated at the LNA output are reduced.

An effective quantification of the noise reduction brought about by increased substrate contacts requires scaling of the contact area in a systematic fashion. The associated trend in noise levels will bring to light the correlation between substrate contact area and the resulting improvements in the LNA noise performance. The two test cases with measured results correspond to the two extremes of the desired scaling spectrum. While LNA1 substrate contacts occupy the minimum area stated by the design rules for the technology, LNA2 contacts span 400 times this area. Thus, detailed simulations are required for gaining insight into the noise coupling behavior of all intermediate contact areas.

An ideal comparison would also require that the individual test setups be identical, except for the LNA substrate taps. From the discussion presented earlier in this section, it is clear that differences exist in the noise injection from the buffer circuits owing to their dissimilar interconnects. To offset these differences, two sets of

simulations are carried out. Set 1 characterizes the effect of substrate contact area on the LNA noise performance for noise injected by the parasitic models corresponding to the power and input/output traces of buffer 1, while set 2 does the same for the noise injected by the model for buffer 2.

## 5.2. Measured and Simulated LNA RF Performance

Simulation results need to closely predict the actual measured performance. Good matching between the two is an indication of accurate simulation models. This agreement becomes critical if valid conclusions are to be drawn entirely from subsequent simulation results. Figures 5.2 and 5.3 compare the measured and simulated S-parameters of LNA1 and LNA2, respectively. It can be observed that the measured and simulated values are in good agreement with each other, for both LNAs.

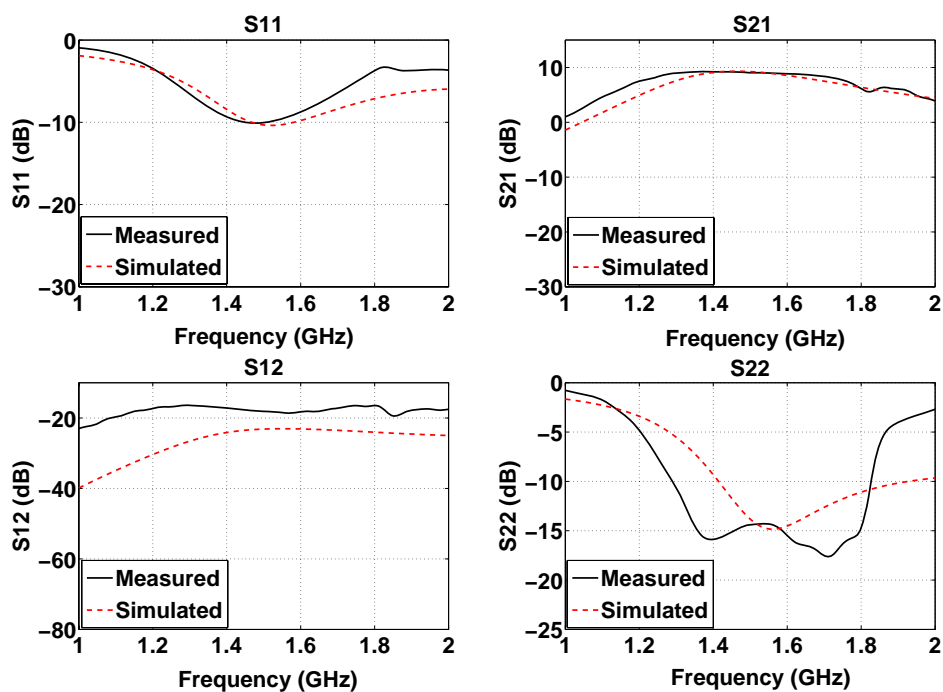


Figure 5.2. Simulated and measured S-parameters for LNA1.

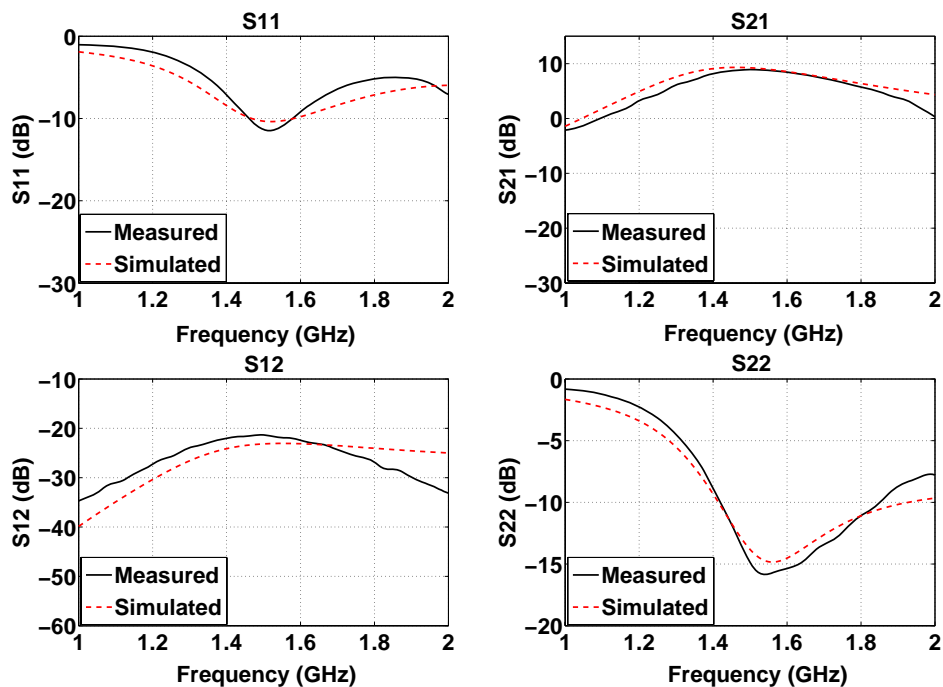


Figure 5.3. Simulated and measured S-parameters for LNA2.

### 5.3. Measured and Simulated Substrate Noise Coupling

The substrate noise simulations were done by performing a transient analysis on the buffer and LNA, with the common substrate modeled as described in Section 3. The resistive substrate network was included as part of the Spectre netlist. The MOSFET junction capacitances were accounted for as part of the BSIM3v3 device model description. A discrete Fourier transform computation on the transient output yielded the simulated LNA output spectrum. A comparison of the simulated and measured noise levels at the output of LNA1 and LNA2 is shown in Figures 5.4 and 5.5, respectively. Reasonably good agreement is demonstrated for both LNAs.



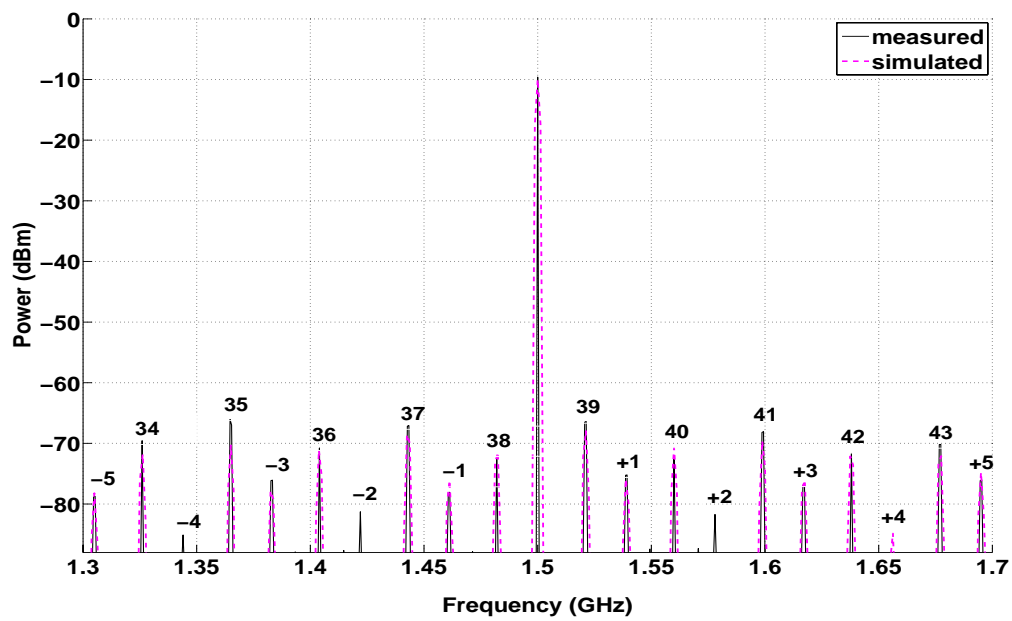


Figure 5.4. Simulated and measured noise levels at LNA1 output.

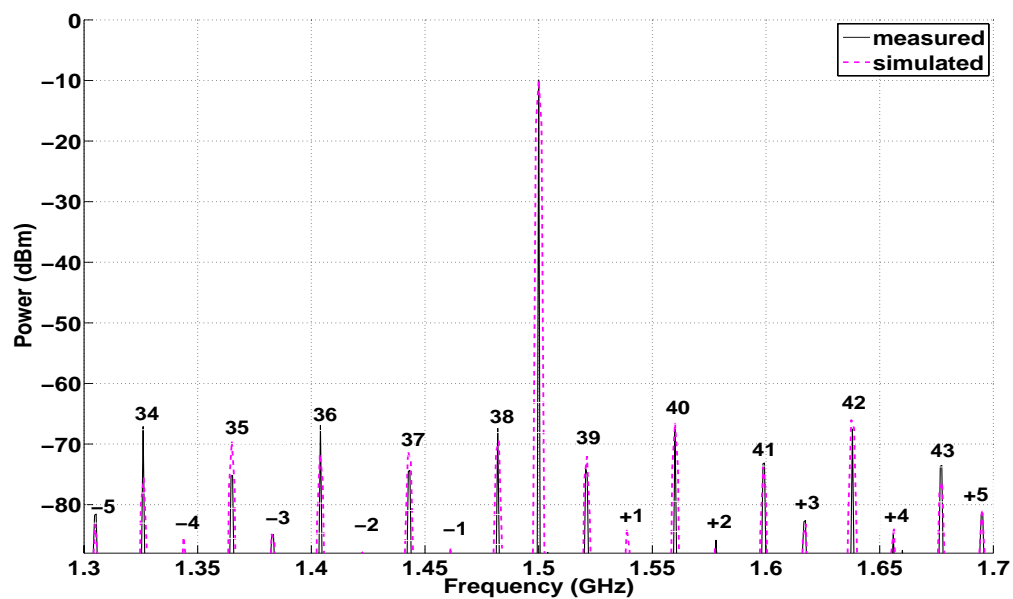


Figure 5.5. Simulated and measured noise levels at LNA2 output.

#### 5.4. Effect of Substrate Contact Sizing

The coupled noise levels at the output of the LNA were studied as a function of the substrate contact size. The layout of LNA1 contains 0.6 $\mu\text{m}$  wide sections of substrate contacts, with lengths ranging between 10 $\mu\text{m}$  and 20 $\mu\text{m}$ . These contacts, occupying a combined area of 60 $\mu\text{m}^2$ , were placed alongside each of the three transistors. The contacts were scaled in area using a scaling factor which was swept from 1 to 400. The contact area of 60 $\mu\text{m}^2$  in LNA1 was denoted by ‘X’, such that 400X corresponded to the contact area of 24,000 $\mu\text{m}^2$  for LNA2. Figures 5.6 and 5.7 highlight the differences in the substrate contact layout of the two LNAs. The solid lines represent the transistors, while the dashed lines outline the substrate taps. Seven intermediate cases were chosen, with substrate contact areas of 2X, 5X, 10X, 20X, 50X, 100X and 200X. The layouts for all test cases are provided in Appendix D.

As discussed earlier, the variation in ground tap area predominantly affects the IM noise levels. Therefore, the noise improvement is characterized entirely in terms of the IM levels in a 400MHz bandwidth. The noise is measured as an rms value, according to

$$IMnoise_{rms} = \sqrt{(IM_{-5})^2 + (IM_{-4})^2 + \dots + (IM_{+3})^2 + (IM_{+4})^2 + (IM_{+5})^2} \quad (1)$$

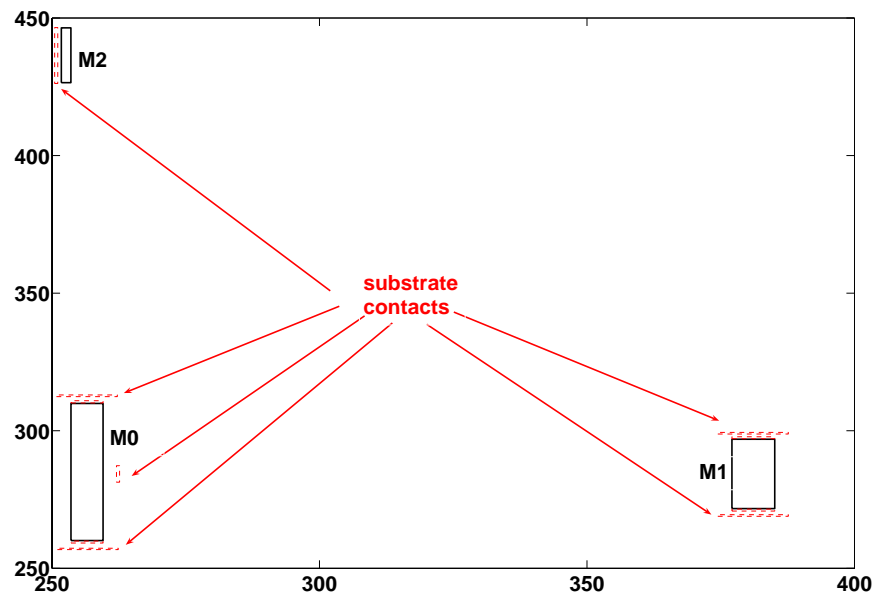


Figure 5.6. Layout of substrate contacts for LNA1.

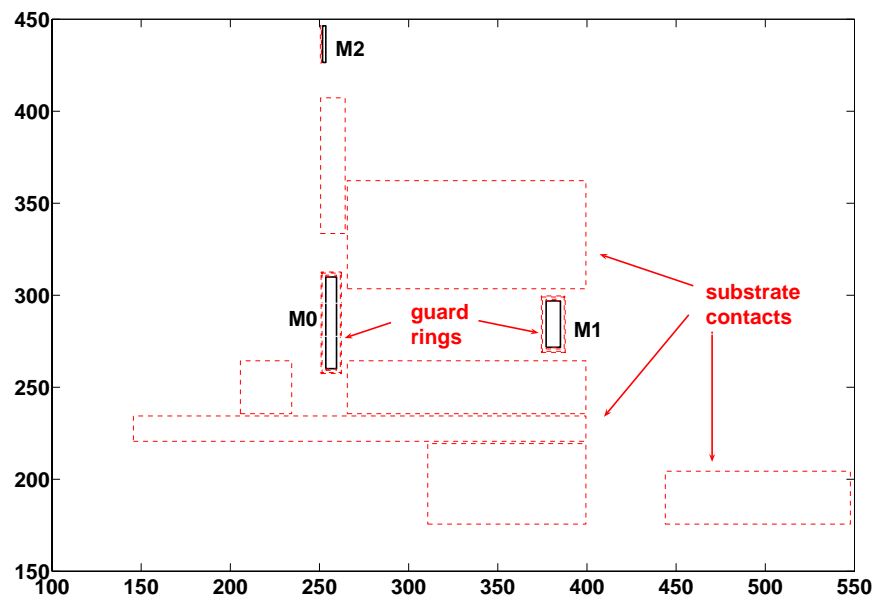


Figure 5.7. Layout of substrate contacts for LNA2.

A simulated plot of the rms IM noise levels as a function of the scaling factor is provided in Figures 5.8 and 5.9. The interconnect models corresponding to the layouts of buffer 1 and buffer 2 are used to inject noise for the cases represented by Figures 5.8 and 5.9, respectively. The additional noise reduction brought about by two 0.6 $\mu\text{m}$  wide guard rings laid out around the input and cascode transistors is also shown in the figures. Simulations are also performed for an increased guard ring width of 4 $\mu\text{m}$ . A comparison of the two plots indicates slightly lower levels of noise injection for the buffer 1 interconnect model. This is attributed to the shorter on-chip traces in buffer 1. Smaller interconnects have lower capacitive coupling to the substrate and hence inject less noise. Since the board level parasitics are comparable in both cases, the difference in noise levels is limited to the length variations of the on-chip interconnects.

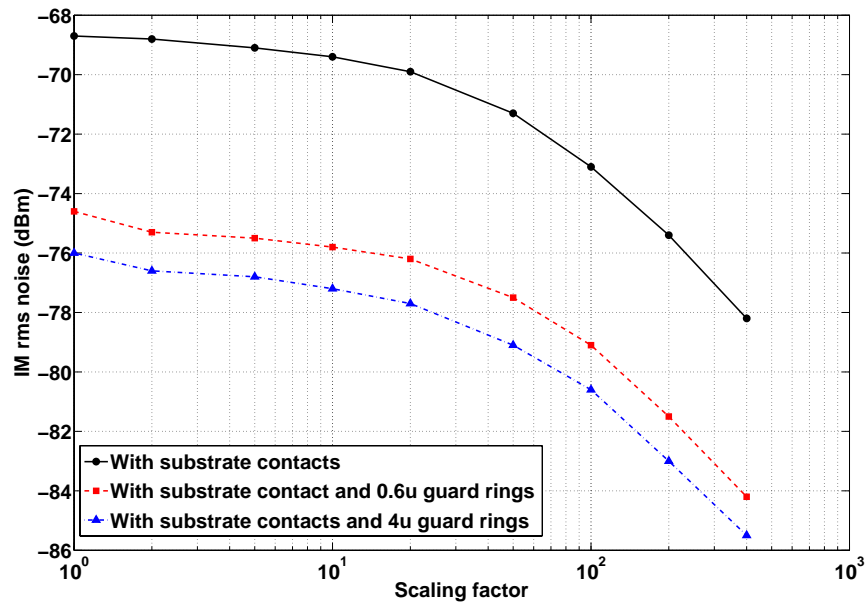


Figure 5.8. Variation of simulated noise levels with substrate contact area, for noise injected by buffer 1 interconnect models.

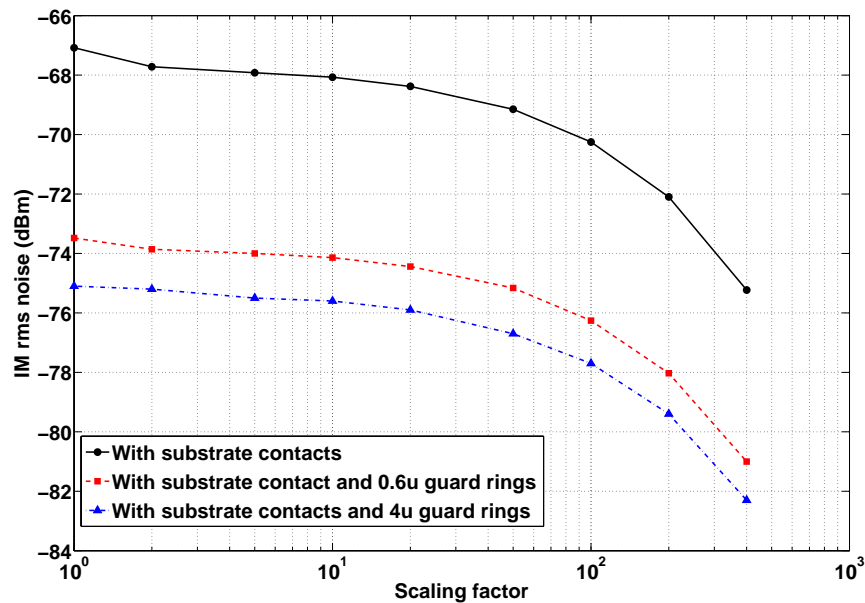


Figure 5.9. Variation of simulated noise levels with substrate contact area, for noise injected by buffer 2 interconnect models.

Both figures demonstrate that the noise reduction is insignificant for scaling factor values lower than 10. Increasing the area 100 times results in approximately a 3dB decrease in the noise levels. Every subsequent doubling of substrate contact area after this, yields substantial gain in isolation. At an area of 200X, the noise falls by 2dB further. The final size of 400X gives an improvement in isolation of 9dB from the first case.

Referring back to the measured results presented in Section 4, it can be noticed that the simulated results indicate a higher reduction in IM noise levels. While the reduction observed between the measured results shown in Figures 4.4 and 4.5 is about 6.5dB, the simulations predict 9dB. This inconsistency can be explained as follows. In the measurements, the on-chip grounds of both LNAs are tied together on the PCB, and connected to the external ground, as shown in Figure 5.10. Thus, when

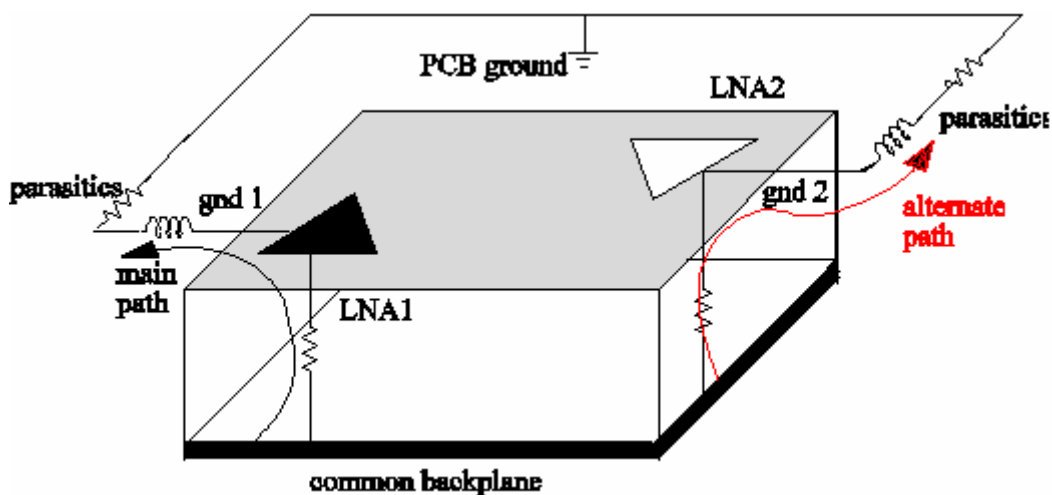


Figure 5.10. Multiple paths for noise to ground.

one LNA is powered on and being tested, the ground of the second LNA is active as well. The substrate, being heavily doped, has a backplane that can be modeled as a single node, owing to the low resistivity bulk. The noise path to ground, through the self-resistance of the substrate contact in the LNA of interest, is labeled as the main path. As indicated in the figure, there is an alternate path to ground, for the noise present on the backplane. Thus, the contribution of the main path to the noise reduction is underestimated. This can be supported with simulation results. When this additional path to ground is modeled, the noise reduction caused by the scaling of ground taps falls to 4.5dB, compared with the 9dB seen earlier. The measured noise levels for LNA1 and LNA2 should ideally match with the simulated values at the two extreme contact area cases. However, this is not observed because the noise measured at LNA1's output is injected by buffer 1 while that measured at LNA2 output is injected by buffer 2. In simulations the buffer model is kept constant for the entire scaling range. Therefore instead of the two measured values lying on the same noise level versus scaling factor curve, the noise measured at the LNA1 output matches with the simulated noise level corresponding to a contact area of 1X in Figure 5.8, while the noise measured at the LNA2 output matches with the simulated noise level corresponding to a contact sizing of 400X with 0.6 $\mu$ m wide guard rings in Figure 5.9.

The noise levels with the 0.6 $\mu$ m wide guard rings laid out around the input and the cascode transistors were simulated to examine the additional noise reduction brought about by those implemented in LNA2. It is observed that the increased

contact area and the guard rings achieve a combined increase in isolation of 14dB. The effect of increasing the guard ring width is also studied by simulating the case of  $4\mu\text{m}$  wide rings. The noise levels go down by another 1.5dB. Simulations for even wider guard rings were not possible, as the closely spaced ground taps start to overlap with the guard rings.

Additional simulations were performed to gain insight into the noise trends associated with further scaling. Substrate contact areas as large as 6,400X, corresponding to  $384,000\mu\text{m}^2$  were simulated. The plot with the entire range of dimensions considered is shown in Figure 5.11. It is clear that the noise levels continue to decrease sharply even beyond the contact dimensions of 400X. It is only after an area of approximately 2,000X that the curve begins to level off and the noise

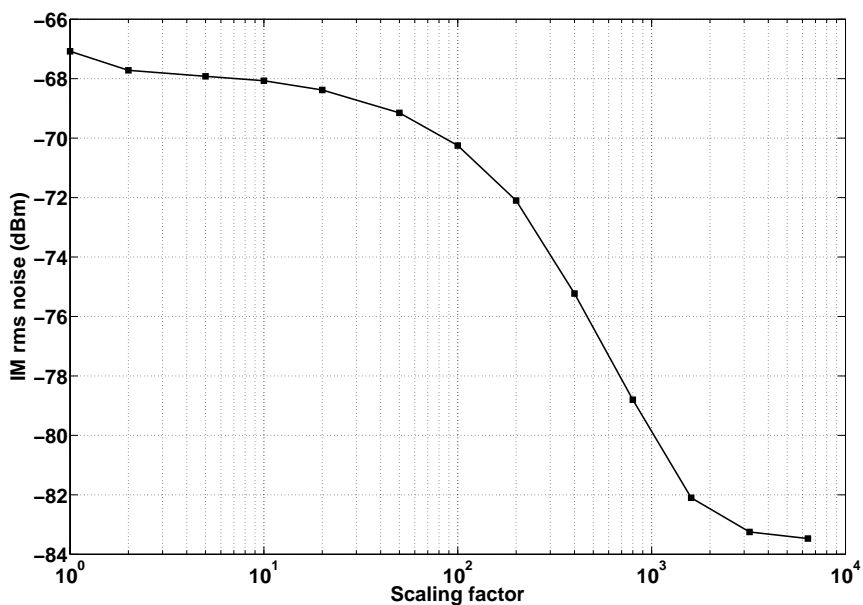


Figure 5.11. Simulated noise levels for substrate contact areas scaled from X to 6,400X.



levels remain fairly constant. The drop in the IM levels over the entire scaling range is approximately 16dB. At dimensions larger than 800X, however, the contacts are prohibitively large, and a trade-off between the chip area and the achieved noise levels has to be considered.

### 5.5. Importance of Substrate Contact Location

Having gained an understanding of the significance of substrate contact sizing for noise performance, we now focus on the importance of the location of substrate contacts. This analysis aims at identifying the best locations for the ground taps in terms of their noise reducing capabilities. Two experiments are considered. In

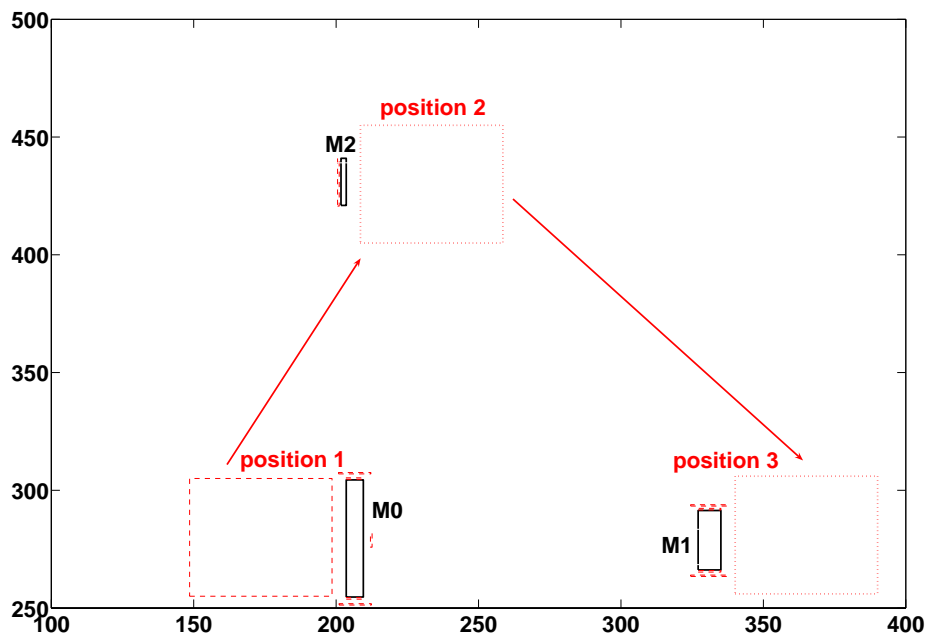


Figure 5.12. Substrate tap positions to identify the sensitive transistor.

Experiment 1, a  $50\mu\text{m} \times 50\mu\text{m}$  substrate contact is located as shown in Figure 5.12, to determine the best position. In position 1, the contact is located  $5\mu\text{m}$  from the input transistor. Positions 2 and 3 correspond to the contact placed at the same distance of  $5\mu\text{m}$  from the bias and cascode transistors, respectively. The associated IM noise levels are shown in Figure 5.13.

It is observed from Figure 5.13 that the contact placed close to M0 is capable of higher reduction in noise levels. As the input transistor is more susceptible to substrate noise, the path to ground provided by the substrate tap located next to it is more effective. There is no variation in the noise levels corresponding to positions 2 and 3. The reason for this will be explained along with the results of the second experiment in this analysis.

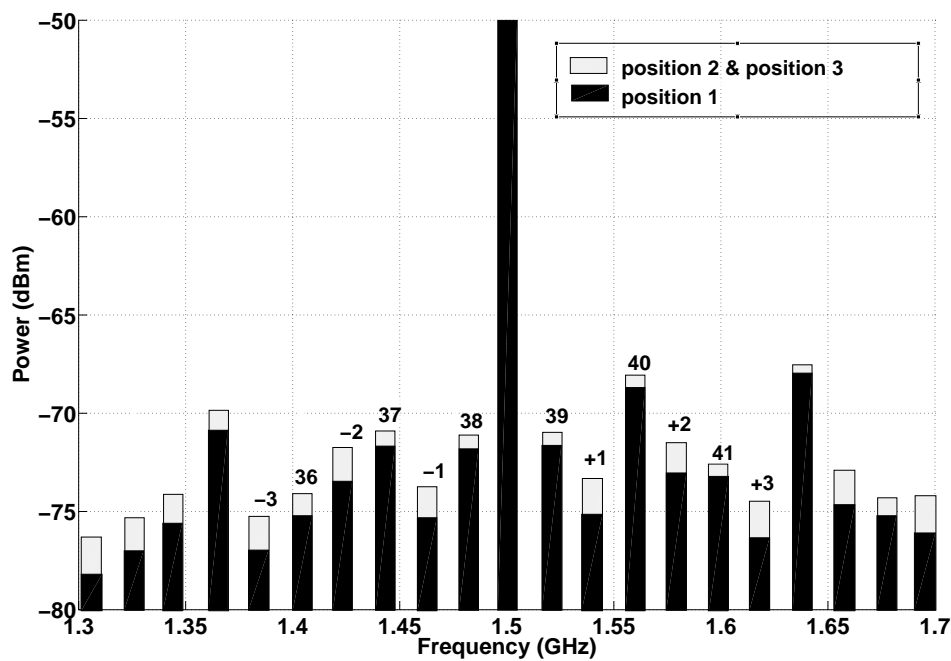


Figure 5.13. IM noise power for 3 different locations of a  $50\mu\text{m} \times 50\mu\text{m}$  contact.

As an extension, the additional case with the substrate contact placed between the input and cascode transistors as shown in Figure 5.14 was considered. It was found that the noise levels were comparable to that for position 1 of the previous case. This reiterates the finding that proximity to the input transistor is essential for substrate taps to be beneficial.

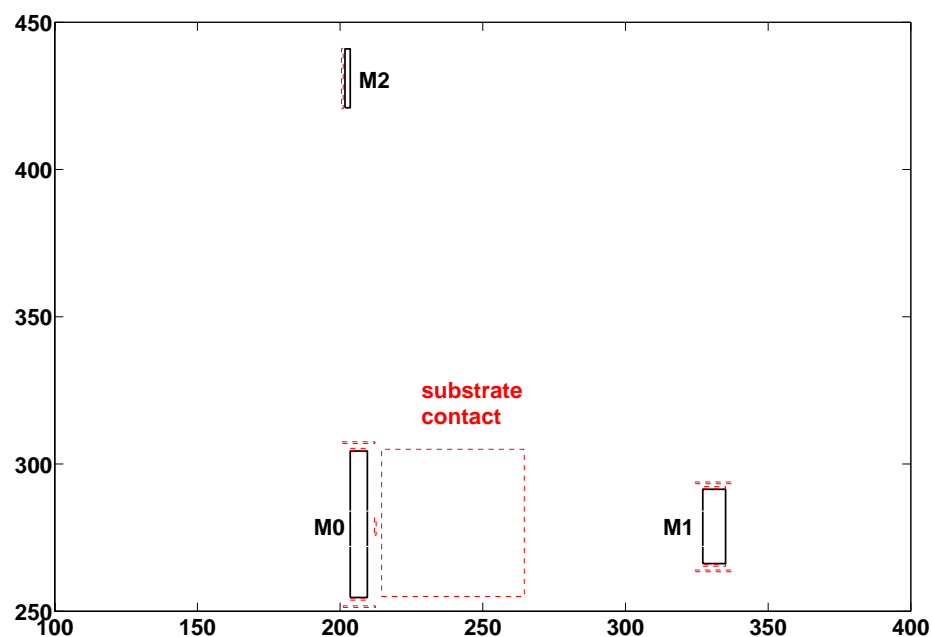


Figure 5.14. Substrate tap placed between the input and cascode transistors.

The finding that substrate taps placed close to the input transistor prove most effective is the basis for Experiment 2. The noise mitigation brought about by a substrate tap as a function of its separation from the sensitive input transistor is considered. Three contacts of dimensions  $5\mu\text{m} \times 5\mu\text{m}$ ,  $20\mu\text{m} \times 20\mu\text{m}$ , and  $50\mu\text{m} \times 50\mu\text{m}$  contact are studied. The effect of separation between the substrate contact and

the sensitive transistor is examined for each of the three contact dimensions. The separation is varied between  $2\mu\text{m}$  and  $40\mu\text{m}$  as shown in Figure 5.15.

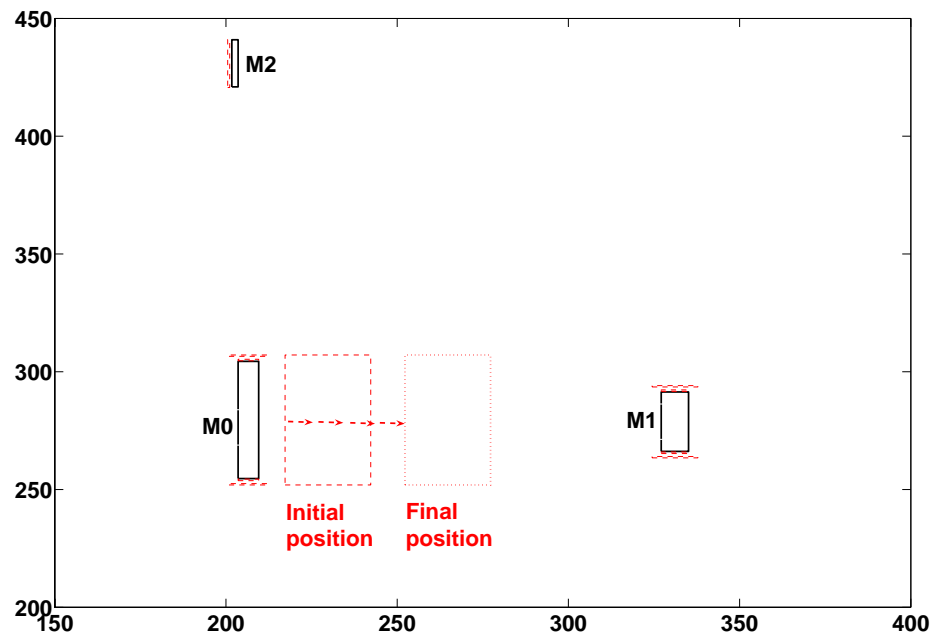


Figure 5.15. Separation between the substrate contact and the input transistor.

The simulated variation of the IM noise levels with separation between the substrate tap and the sensitive node is shown in Figure 5.16. The plot clearly emphasizes the need for taps in close proximity to the sensitive transistor. It can also be observed that the improvement in noise levels with smaller separations is more pronounced for larger substrate taps. While the tap dimension of  $5\mu\text{m} \times 5\mu\text{m}$  brings an improvement of only 0.6dB, the 10 times larger  $50\mu\text{m} \times 50\mu\text{m}$  contact causes an improvement of 3.5dB for the same variation in separation. It can also be observed that beyond a distance of  $20\mu\text{m}$  the noise levels do not vary. This reiterates the fact

that for heavily doped substrates, at separations larger than five times the epitaxial layer thickness, mutual resistances between contacts are not functions of the separation. For this reason, the noise levels resulting from substrate contacts placed in position 2 and position 3 in Experiment 1 are identical.

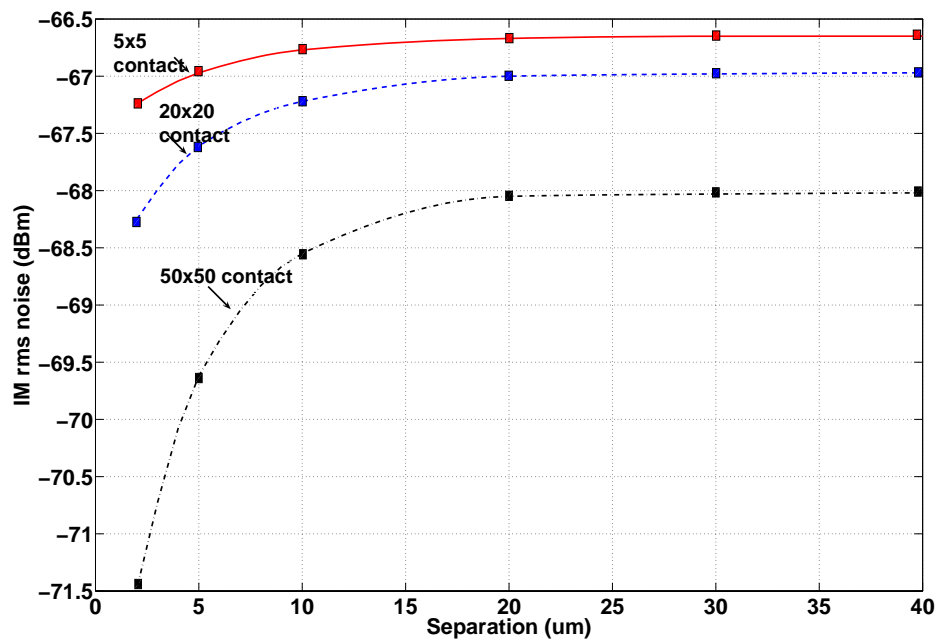


Figure 5.16. Variation of the simulated noise levels with separation between substrate taps and the sensitive node.

## 6. NOISE INJECTION MECHANISMS IN THE STEPPED BUFFER

The noise generated in the buffer circuit finds its way into the chip backplane through various paths. This noise on the backplane couples to the LNA output either directly or through the active circuit [22]. The previous section focused on reducing the noise levels at the amplifier output by implementing modifications to the LNA layout. In this section, we analyze the noise from the injector. It was seen from previous analysis that the injected noise levels are a strong function of the buffer's power, input, and output routing. This section provides an insight into the different noise generation and injection mechanisms in the stepped buffer. The odd and even harmonics of the coupling noise are independently studied.

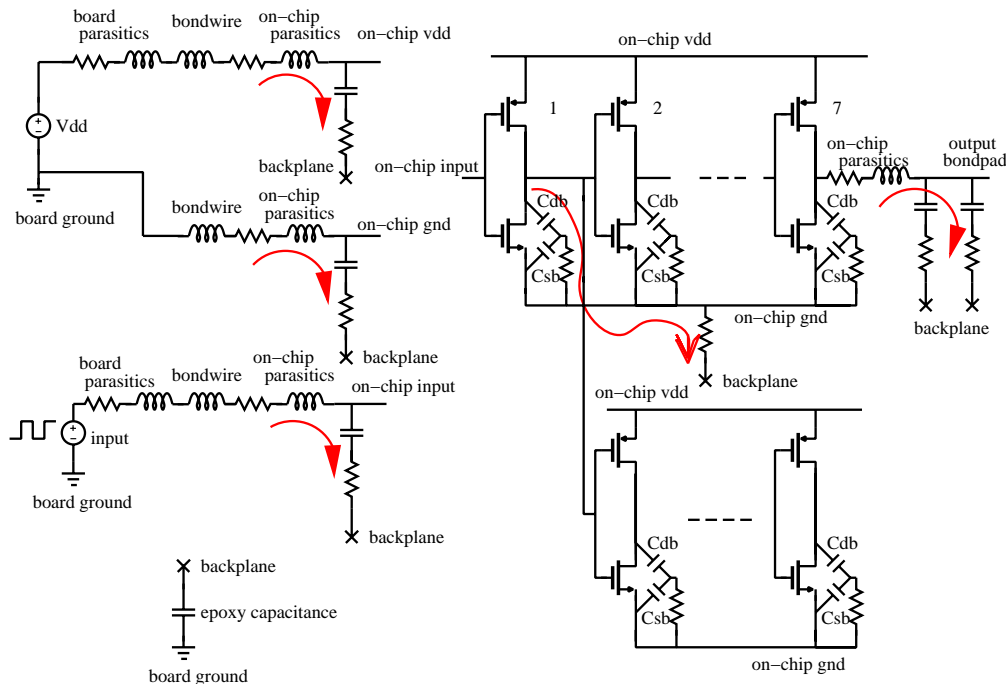


Figure 6.1. Noise injection paths in a stepped buffer.

The various sources of noise are examined for their harmonic content, and their individual contributions to both the harmonic as well as IM noise are quantified. Figure 6.1 highlights the major noise coupling paths in the stepped buffer circuit. The node labeled as back plane represents the single substrate node. It is seen that this connects to the board ground through the capacitance of the epoxy layer used to attach the die to the die paddle. The on-chip ground plane on the top metal layers is shown in the figure.

The dominant injection paths are enumerated below.

1. Input line capacitance to the substrate.
2. Output line and output bond pad capacitance to the substrate.
3. Power line capacitances to the substrate which inject  $Ldi/dt$  noise.
4. Transistor junction capacitances coupled with the bulk node and ground tap resistances to the back plane.

A discussion of each of these mechanisms, and methods to mitigate the generated noise are provided in the following sub sections.

### **6.1. Input Line**

The circuit setup used to simulate the noise generated by the input line is shown in Figure 6.2. A schematic of the buffer highlighting the path through which noise is injected into the back plane is shown. The effect of this noise is observed on the

output of the LNA. As earlier, this effect is analyzed by considering the clock harmonics and IM products appearing in the vicinity of the RF signal.

The parasitic model for the input line incorporates models for the board interconnect, package and on-chip interconnect. The board trace is modeled as a resistance in series with an inductance. The package parasitics include the package lead, bond wire and pin inductances. Among these, the bond wire inductance is found to be the most significant. The on-chip interconnect is represented as an RLGC model as explained in Appendix B. Ideal models for the remaining lines eliminate their noise contribution.

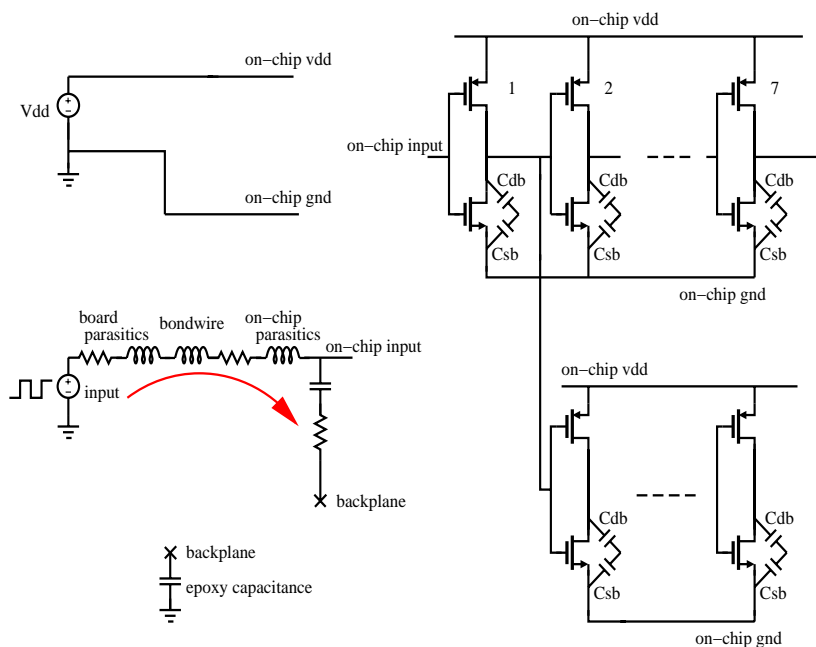


Figure 6.2. Noise injection from the input line.



The input line has a 50% duty cycle, 39 MHz square wave. Rapid voltage switching in the step input injects noise currents into the substrate given by  $i = C \frac{dv}{dt}$ . A rising edge induces a positive current spike, while a falling edge causes a negative one, as indicated in Figure 6.3. The parasitic inductor is responsible for the ringing observed during each transition. A consistent overall ringing behavior can also be observed during each transition. A consistent overall ringing behavior can also be observed in the waveforms. Since the LNA is on, the 1.5GHz signal couples to the common backplane via the amplifier's interconnect and bondpad capacitances to the substrate, and the spreading resistances. This gets capacitively coupled to the buffer

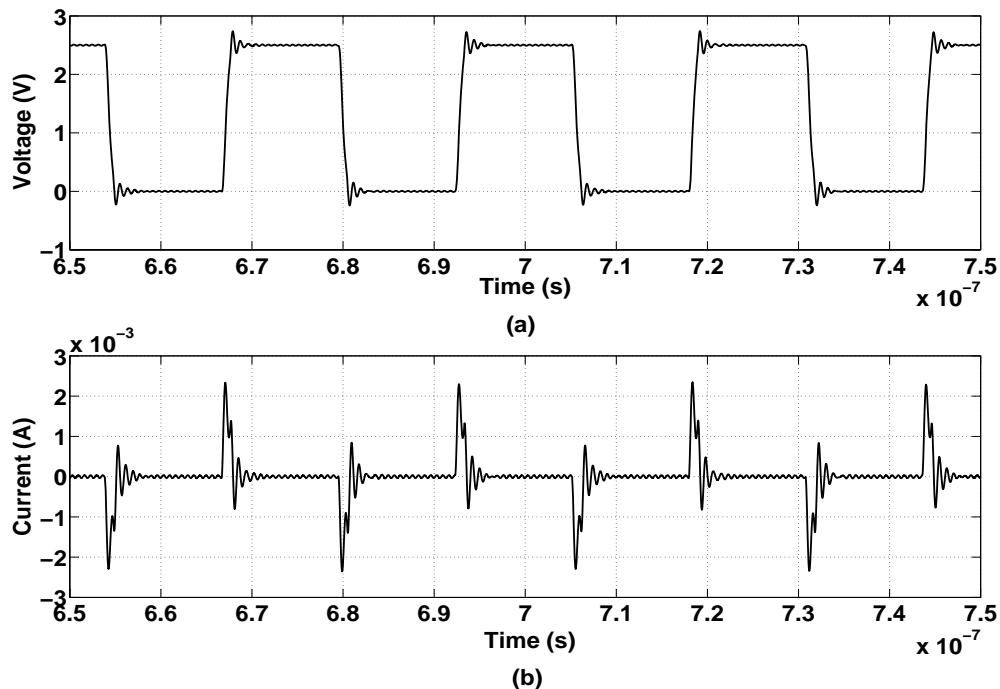


Figure 6.3. Transient input voltage and substrate current waveforms.

(a) Step input voltage. (b) Current injected into the input interconnect capacitance to substrate.

interconnects and appears as the observed ringing pattern. The model for LNA1 is used in this analysis.

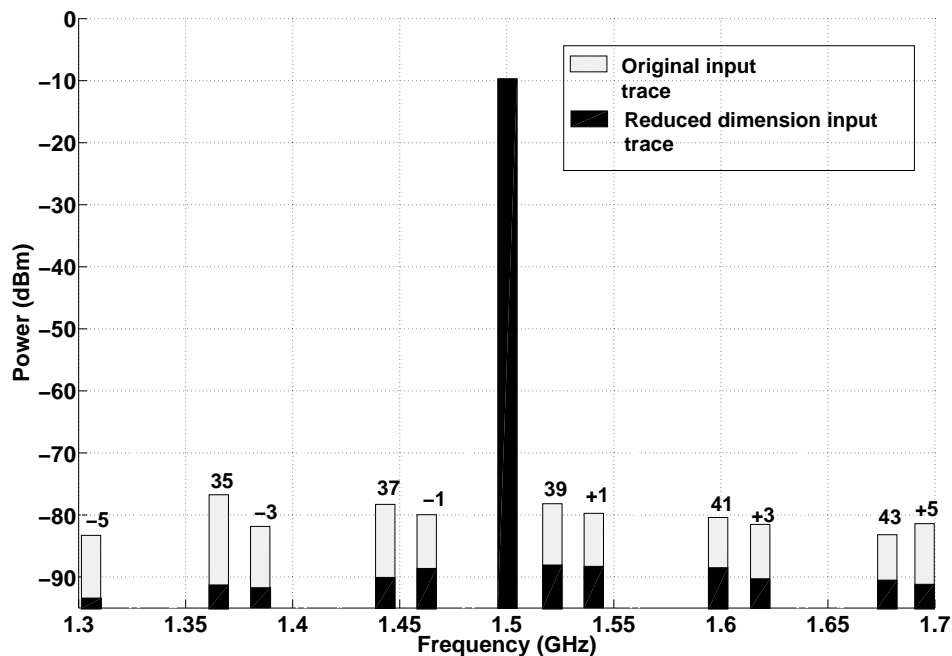


Figure 6.4. Noise levels at LNA output for noise injected by the buffer input line.

Owing to its symmetric nature, the step input generates only odd harmonics of the clock. Figure 6.4 provides a bar chart representation of the LNA output spectrum indicating the power levels of the harmonic and IM noise. It can be observed that the spectrum contains only odd-order harmonics and IM terms.

The on-chip interconnect capacitance to the substrate provides the primary coupling path for these clock harmonics. A lesser contribution comes from the large PCB trace inductance. Reducing the board trace length, and the on-chip interconnect

length and width can decrease the values of these critical parasitics. The output noise levels for a 50% reduction in the on-chip interconnect dimensions from  $1600\mu\text{m} \times 5\mu\text{m}$  to  $800\mu\text{m} \times 2.5\mu\text{m}$  are shown in Figure 6.4. It can be observed that the odd harmonic levels are significantly lower, the exact reduction being 11.5dB.

## 6.2. Output Interconnect and Bond Pad

The noise contribution of the output line is isolated as shown in the schematic of Figure 6.5. The output parasitics include an RLCG model for the  $1400\mu\text{m} \times 10\mu\text{m}$  on-chip trace, and an RC model for the bond pad. Appendix B provides a detailed explanation of the models used.

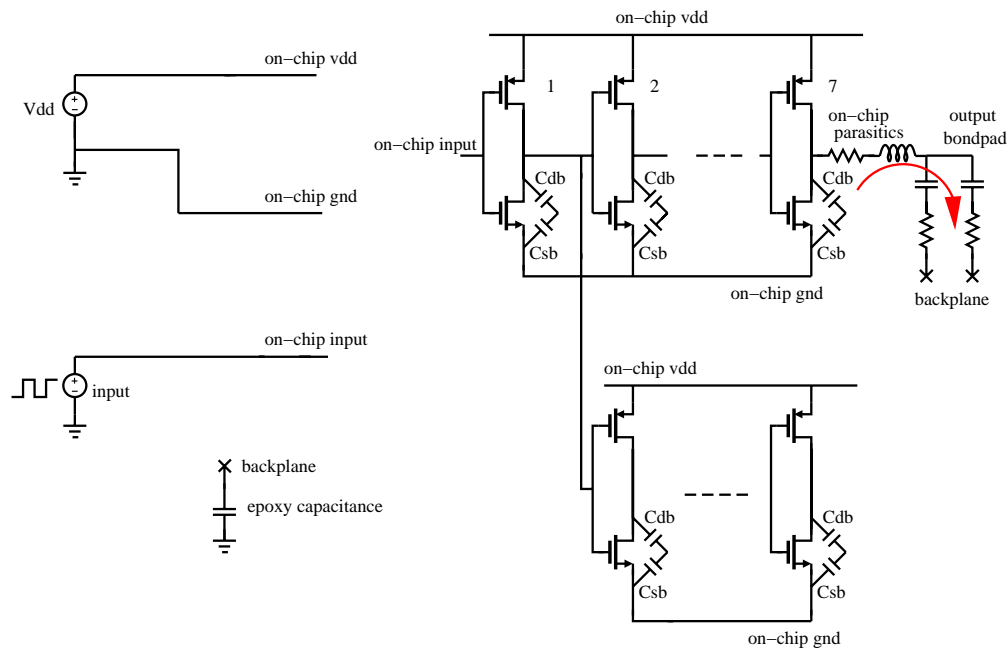


Figure 6.5. Noise injection from the output line.

The step waveform appearing at the output has a much faster  $t_{\text{rise}}$  and  $t_{\text{fall}}$  as compared to the input, owing to the high speed switching of CMOS devices. Faster switching brings with it the issue of strong higher order harmonics. This makes the output line a more dominant noise source, than the input line, particularly at gigahertz frequencies. This can be observed from the stronger odd harmonics around the RF signal in the LNA output spectrum shown by the bar chart in Figure 6.6.

The difference between the threshold voltages of the PMOS and NMOS devices causes skewing of the 50% duty cycle input, resulting in an asymmetric step waveform at the output. This deviation from an ideal square waveform gives rise to even harmonics as well, as seen in Figure 6.6. Thus, unlike the input, the output line injects both odd as well as even harmonic noise.

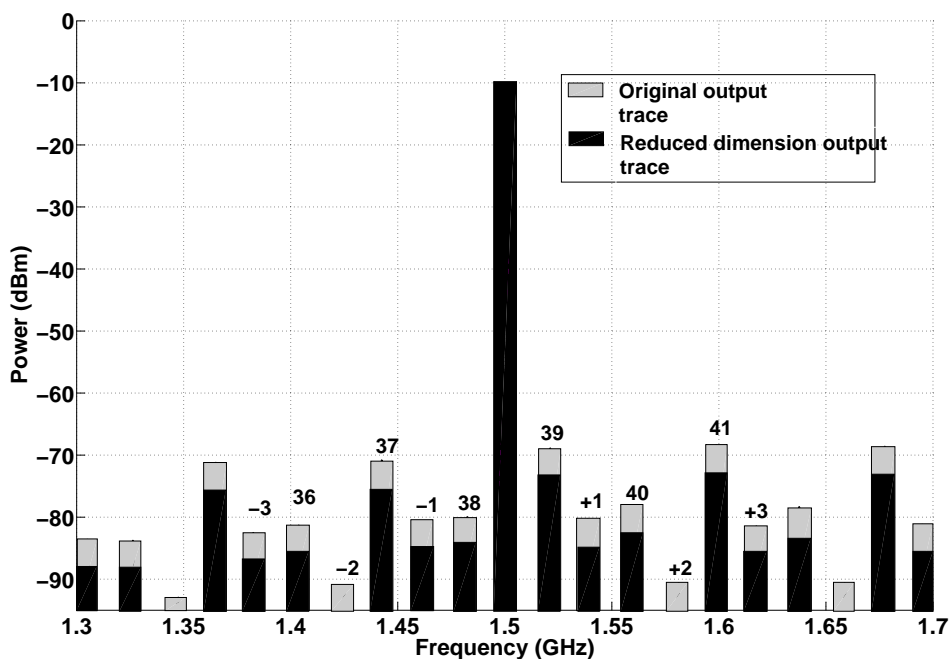


Figure 6.6. Noise levels at LNA output for noise injected by the buffer output line.

As in the case of the input line, the interconnect capacitance to the substrate plays the primary role in noise injection. Lowering its value by reducing the dimensions of the on-chip interconnect by half, results in reduced noise levels as shown in Figure 6.6. The harmonic levels are 4.5 dB lower.

### 6.3. Power and Ground Lines

The switching activity in the buffer creates current spikes in the power and ground lines. As a result of the parasitic inductances in these lines, voltage fluctuations proportional to the rate of change of current given by  $v = L \frac{di}{dt}$  are generated [31-33]. A better understanding of this phenomenon is possible with the help of the schematic of an inverter as provided in Figure 6.7. When a node makes a transition from a high state to a low state, a rush of current flows from the load capacitor into the chip ground. This sudden rush in combination with the pin, package and trace inductances causes a positive voltage spike on the ground line. This current initially builds up, and then recedes giving rise to what is known as ground bounce. Voltage spikes of much lower magnitude result from a low to high transition. The opposite phenomenon wherein a node switching from low to high causes a rush of current from the Vdd line into the load capacitor which generates a negative voltage spike on the power line, is called supply droop. The magnitude of these fluctuations increases with both the number of simultaneously switching

outputs, and the load capacitance. A larger capacitance stores more charge, hence sinking or sourcing more current and leading to larger voltage spikes.

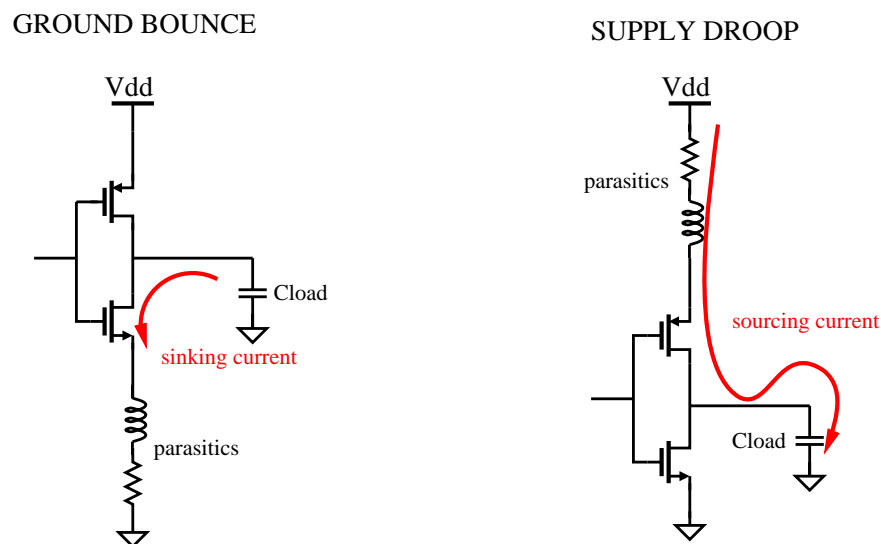


Figure 6.7. Ground bounce and supply droop mechanisms.

The transient voltage fluctuations generated by a single switching inverter, as observed on the power and ground lines are shown in Figure 6.8. Dimensions of  $30\mu\text{m}/0.25\mu\text{m}$  and  $15\mu\text{m}/0.25\mu\text{m}$  are chosen for the PMOS and NMOS devices, respectively. These values correspond to the sizes of the devices in one stage (3<sup>rd</sup>) of the stepped buffer. The load capacitance is 2pF, and the parasitic inductances on the power and ground lines are taken to be 5nH [21]. It can be observed that the falling edge of the output generates positive spikes on the ground voltage, while the rising edge gives rise to downward spikes on the power line.

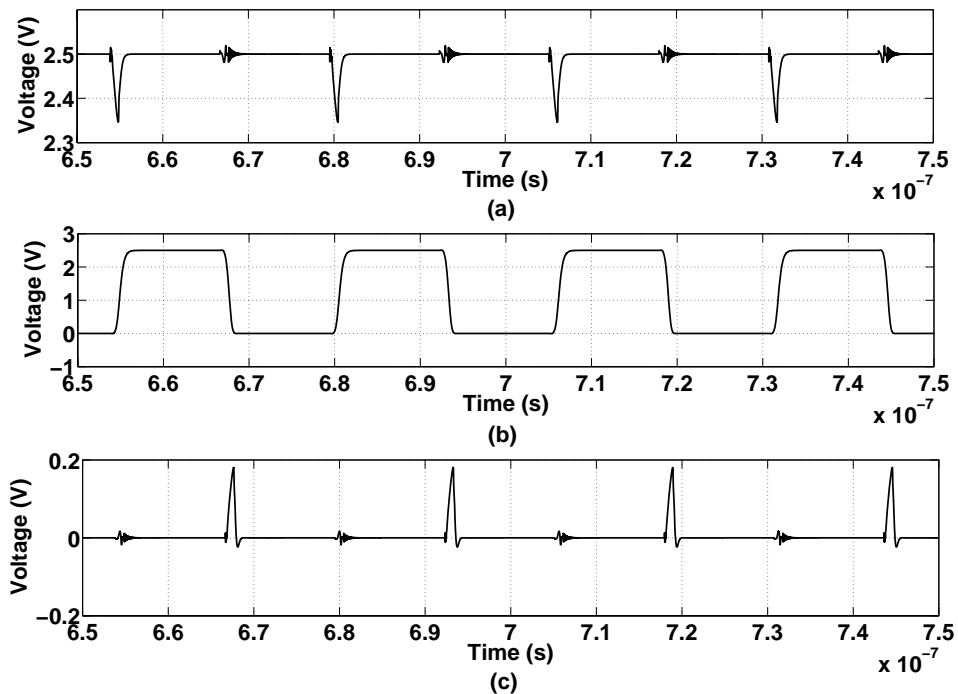


Figure 6.8. Voltage of the power, output, and ground lines in an inverter.

(a) Spikes on power line due to switching of the inverter. (b) Output voltage.

(c) Spikes on the ground line due to switching of the inverter.

### 6.3.1. Power Line

The schematic for simulating the noise contribution of the power line is shown in Figure 6.9. A single inverter was shown to cause power line voltage spiking only at the rising edges of its output. This is not true for the buffer circuit, as it comprises seven inverter stages, four of which switch simultaneously from low to high during the step input's falling edge while the remaining three make this transition for a rising step input edge. This would lead us to expect voltage fluctuations on the V<sub>dd</sub> line for both transitions. The magnitude of these spikes will be a function of the total loading

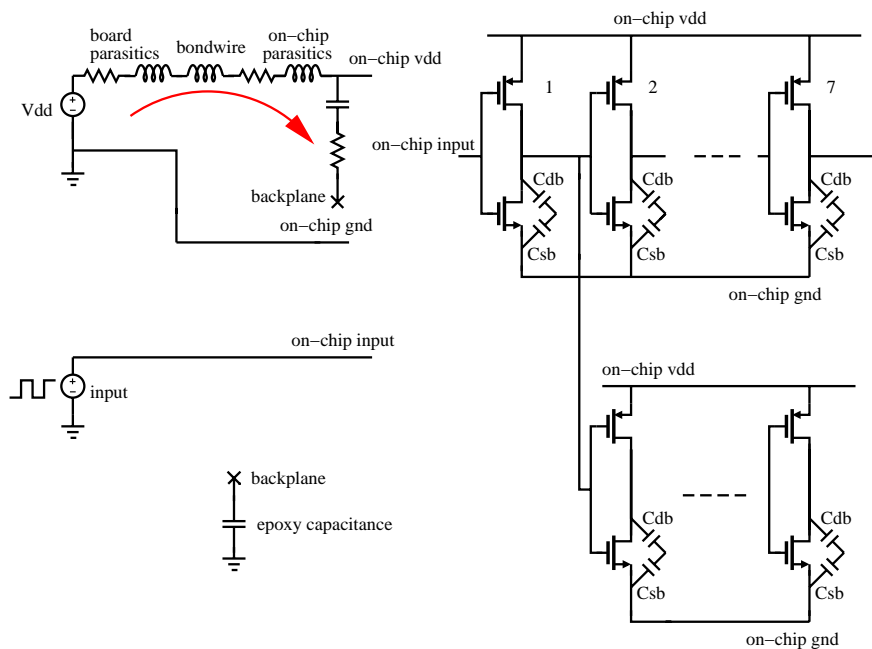


Figure 6.9. Noise injection from the power line.

of all the inverters making the transition of interest. Thus a substantial 78MHz ( $2f_{CLK}$ ) component is present in the power line voltage fluctuation. This would imply strong even harmonics in the noise injected by this line. The transient voltage waveform is shown in Figure 6.10.

A slightly higher magnitude for the spikes induced in the rising edge of the input step is evident. This is due to the larger loading of stages 2, 4 and 6, which make the low to high switch during this edge. As expected, the even harmonic power levels are higher at the LNA output as observed from Figure 6.11.



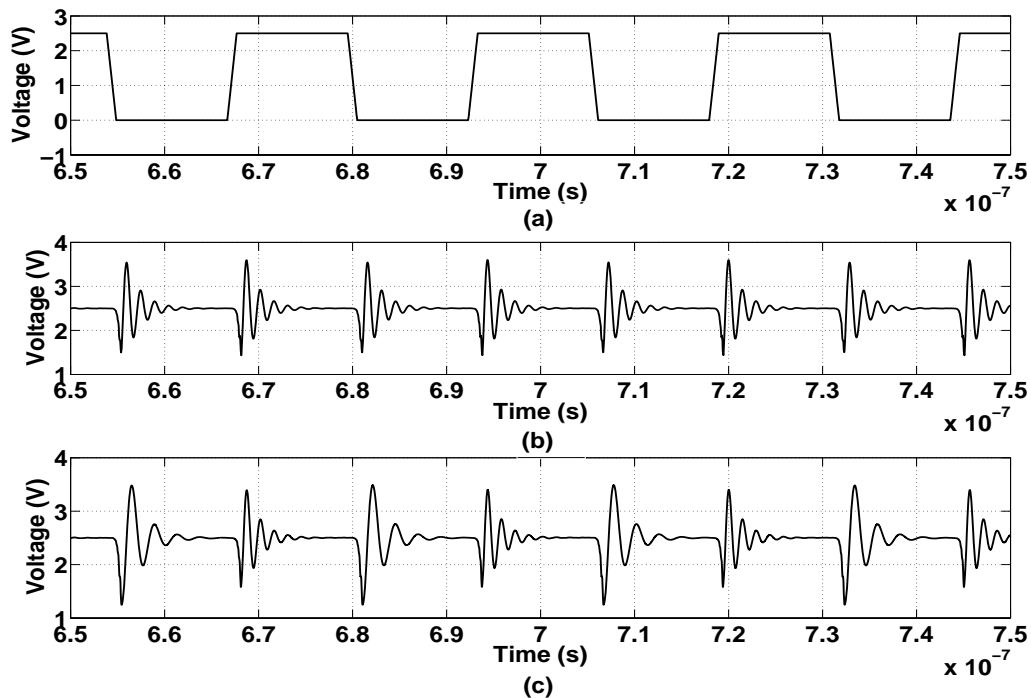


Figure 6.10. Voltage of the input and power lines in the stepped buffer.  
 (a) Step input. (b) Voltage on power line due to switching of the buffer.  
 (c) Voltage on power line due to switching of the buffer with additional output capacitance of 20pF.

To show the dependence on loading, a 20pF load capacitance is added to the final stage. This should result in increased voltage spikes during the falling edge of the input. The transient voltage waveform seen in Figure 6.10 (c) displays this expected behavior. The larger magnitude difference between the voltage spikes indicates a reduced 78MHz component and an increased 39MHz one. This effect manifests itself in the form of lowered even harmonics and boosted odd harmonics at the LNA

output, as seen from the bar graph for the case of an additional 20pF output capacitor in Figure 6.11.

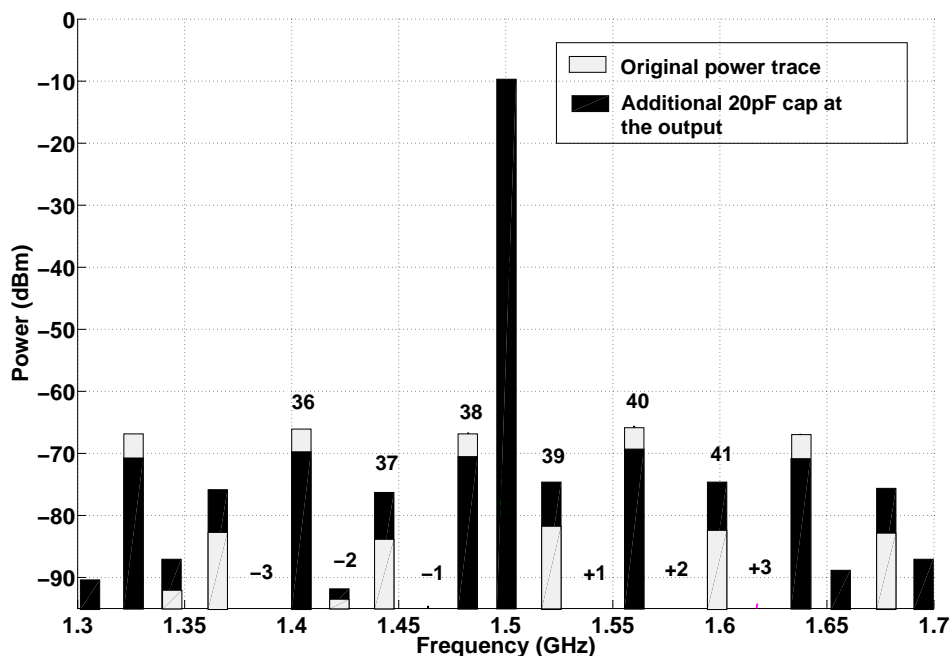


Figure 6.11. Noise levels at LNA output for noise injected by the buffer power line.

The generated noise levels are a strong function of the line inductance. Thus, a lower inductance would prove beneficial. Having identified a method to control the magnitudes of the harmonics, we proceed to make changes to the coupling path, to reduce the injected noise. As discussed previously, the primary coupling mechanism is through the interconnect capacitance. A 50% reduction in the on-chip interconnect dimensions of  $1700\mu\text{m} \times 35\mu\text{m}$  results in noise levels at the LNA output as shown in Figure 6.12. Thus an improvement of 7.3dB for the even harmonics and 6.3dB for the odd harmonics is achieved with the suggested method.

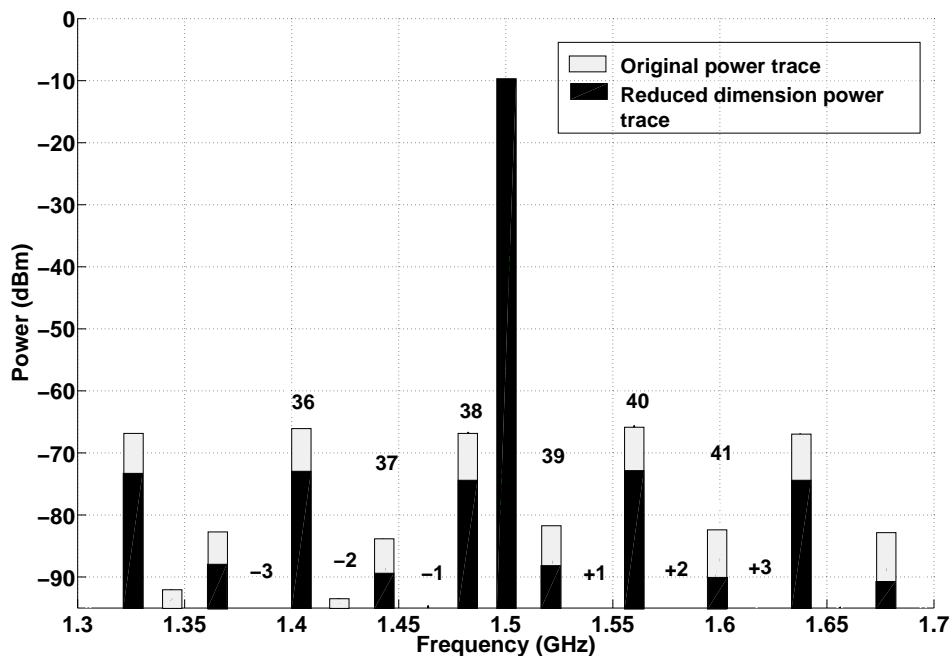


Figure 6.12. Noise levels at LNA output for noise injected by the reduced dimension power line.

### 6.3.2. Ground Line

The ground line is examined for its noise contribution in a similar fashion to the power line. Figure 6.13 provides the schematic used for this analysis. The noise generation mechanism is identical to the case of the power line. While the noise created is a function of the ground line parasitic inductance, the relative magnitude of the even and odd order harmonics is determined by the capacitive loading of the switching transistors. The difference lies in the components of the noise injection

path. While the noise generated by the power line finds a path to the backplane primarily through the interconnect capacitance, the ground line disturbances reach the back plane via two paths. Apart from the interconnect capacitance to the substrate, the ground taps which are biased by the ground line also inject noise into the substrate by way of their self-resistances to the back plane.

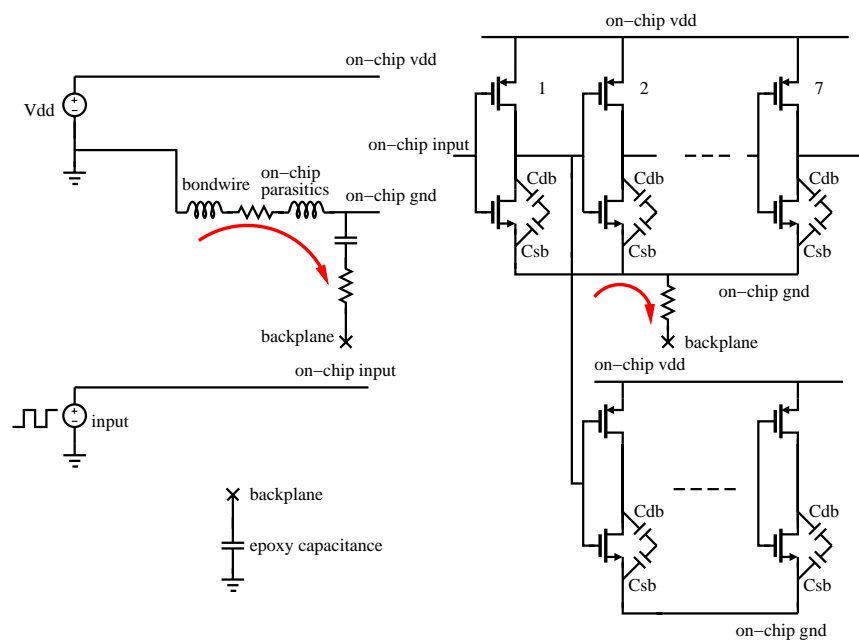


Figure 6.13. Noise injection from the ground line.

The noise levels at the LNA output arising from the buffer ground are indicated in Figure 6.14. The approach of reduced interconnect dimensions is employed once more to decrease the value of the coupling capacitance. As seen from the corresponding bar chart in Figure 6.14, this modification brings about approximately 3.8dB of noise reduction. The noise levels resulting from increasing the self-resistance of the substrate contact to a large value ( $1M\Omega$ ) are also shown in Figure

6.14. It is noticeable that this brings about additional reduction in noise levels. Increasing this resistance would however require minimizing the area of the buffer substrate contacts. As the sizes used are not very much higher than the required minimum, this approach to noise reduction is not possible. Thus, the former approach alone can be realized.

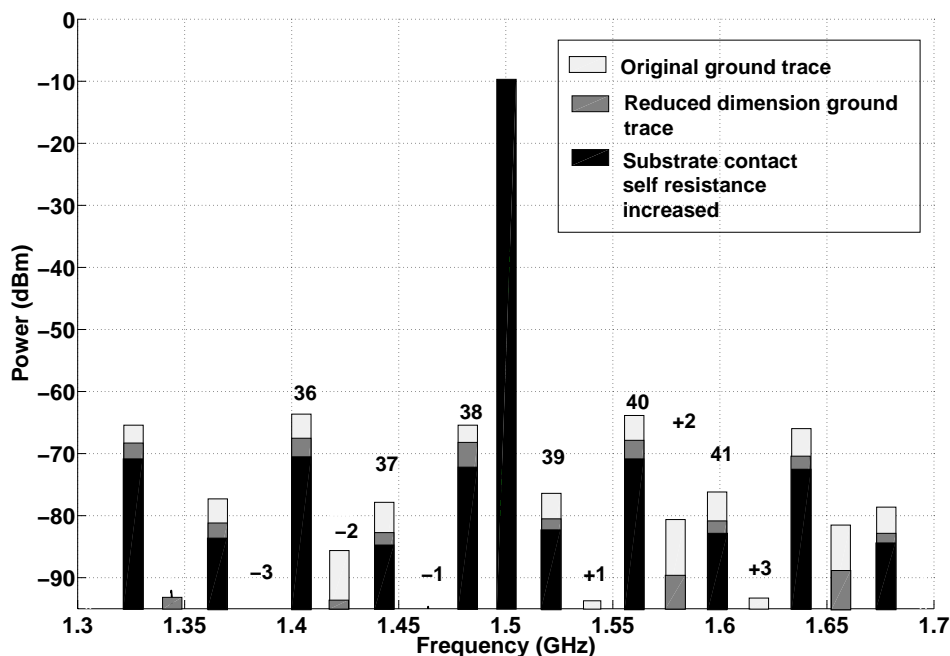


Figure 6.14. Noise levels at LNA output for noise injected by the buffer ground line.

#### 6.4. Transistor Junction Capacitances

This is the final noise coupling mechanism considered in this analysis. The coupling path is as highlighted in the schematic of Figure 6.15. The switching drain node of each of the NMOS transistors injects noise into the bulk by means of the

transistor drain-bulk junction capacitance. This bulk node connects to the back plane via its self resistance. The mutual resistance of the bulk node with the substrate contact forms another path to the back plane. However, relatively small values for the junction capacitance coupled with the large substrate resistances make the noise injection from the bulk nodes insignificant. Since the noise levels arising from this source are well below the contributions from the other sources discussed, this is omitted in subsequent analyses.

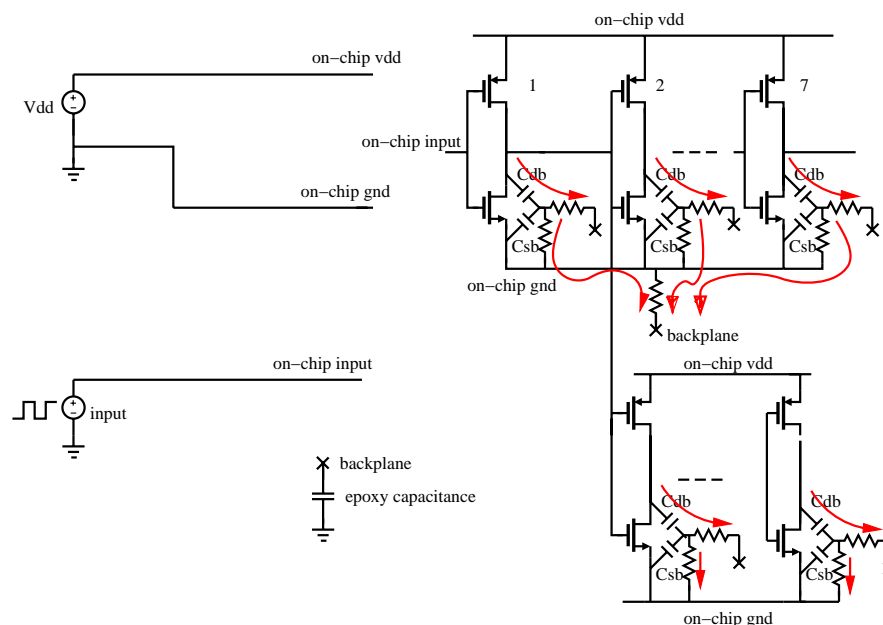


Figure 6.15. Noise injection from the transistor junction capacitors.

Following the individual assessment of each noise source, the previously suggested noise reduction methods are tested for their cumulative effect. It is observed that though each modification brought about a decrease in the order of 5-10dB, when implemented collectively, the decrease is not proportionately higher.

This is due to the interaction between the various mechanisms, which was ignored when evaluating their individual contributions. The levels of noise reduction brought about by halving the dimensions of each of the traces are shown in Figures 6.16 and 6.17. As seen in the pie chart provided in Figure 6.16, the maximum reduction of 3.73dB in the odd harmonic levels is achieved by decreasing the size of the output trace. Similarly, a 50% reduction in the ground trace dimensions brings about the maximum decrease in the even harmonic noise levels. The trace dimensions and the associated noise levels are summarized in Tables 6.1, 6.2 and 6.3. Tones below the noise floor are not listed.

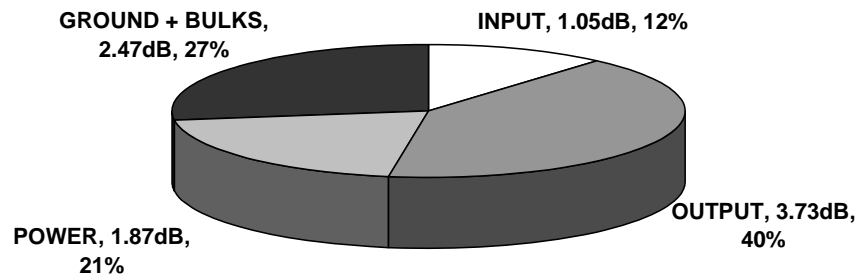


Figure 6.16. Decrease in odd harmonic noise levels caused by reducing interconnect dimensions.

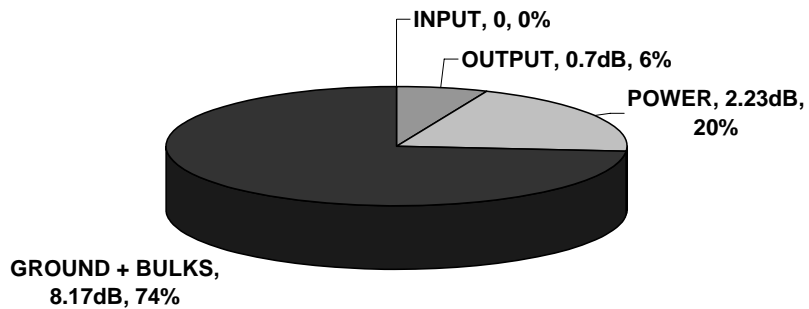


Figure 6.17. Decrease in even harmonic noise levels caused by reducing interconnect dimensions.

Table 6.1. On-chip interconnect dimensions.

Trace	Original Dimensions	Reduced Dimensions
Input	1600 $\mu\text{m}$ x 5 $\mu\text{m}$	800 $\mu\text{m}$ x 2.5 $\mu\text{m}$
Output	1400 $\mu\text{m}$ x 10 $\mu\text{m}$	700 $\mu\text{m}$ x 5 $\mu\text{m}$
Power	1700 $\mu\text{m}$ x 35 $\mu\text{m}$	850 $\mu\text{m}$ x 17 $\mu\text{m}$
Ground	1900 $\mu\text{m}$ x 35 $\mu\text{m}$	950 $\mu\text{m}$ x 17 $\mu\text{m}$



Table 6.2. Effect of on-chip interconnect dimensions on harmonic noise levels.

Trace	Odd Harmonics		Even Harmonics	
	Original Dimensions	Reduced Dimensions	Original Dimensions	Reduced Dimensions
Input	-74dBm	-85.5dBm	-	-
Output	-65dBm	-69.5dBm	-75dBm	-79.5dBm
Power	-80dBm	-86.3dBm	-62dBm	-69.3dBm
Ground	-74dBm	-77.8dBm	-61dBm	-64.8dBm

Table 6.3. Effect of on-chip interconnect dimensions on IM noise levels.

Trace	Odd IM		Even IM	
	Original Dimensions	Reduced Dimensions	Original Dimensions	Reduced Dimensions
Input	-78dBm	-87dBm	-	-
Output	-77dBm	-81.5dBm	-90dBm	-96dBm
Power	-	-	-92dBm	-
Ground	-94dBm	-	-80dBm	-87dBm

### 6.5. Individual Contributions to the Total Noise

Having identified the dominant frequency components of the noise injected by each of the four primary mechanisms, we proceed to quantify these individual contributions as a proportion of the total noise power seen at the output of the LNA.

The harmonic terms and the IM terms are analyzed separately. To demonstrate that the layout of the buffer strongly influences the noise levels, the noise contributions are quantified for both buffer 1 and buffer 2. It will be seen that the proportions vary widely between the two cases.

### 6.5.1. Harmonic Noise

The contributions of the higher order harmonic terms from the different sources are shown in Figures 6.18 and 6.19, respectively. It can be observed from the graph for the odd harmonic levels that the strongest contributors in buffer 1 and buffer 2 are

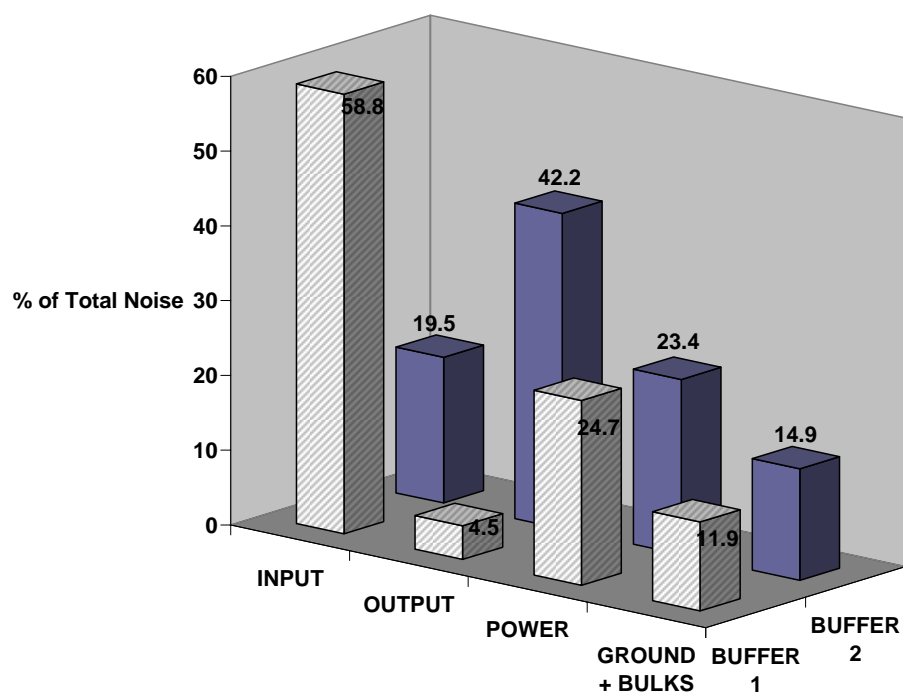


Figure 6.18. Individual contributions to the total odd harmonic noise levels for buffer 1 and buffer 2.

the input and output, respectively. Thus, differences in the layout not only bring variations in the absolute noise levels, but they can also significantly alter the noise trends. Figure 6.19 shows the even harmonic contributions. As expected, the input contribution is negligible. The even harmonics resulting from the output are entirely due to the output waveform's asymmetry. This asymmetry stems from the mismatch between the NMOS and PMOS threshold voltages due to which the devices turn on at different times after the input transition. This mismatch is off the order of a few hundred milivolts and not too large. Therefore, the output contribution is also small.

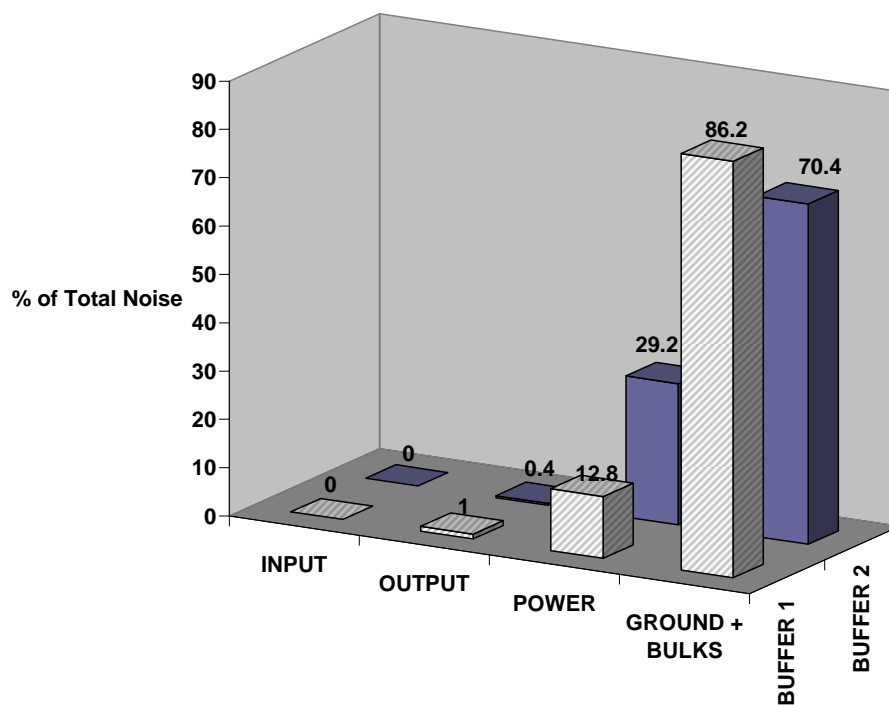


Figure 6.19. Individual contributions to the total even harmonic noise levels for buffer 1 and buffer 2

### 6.5.2. IM Noise

The contributions to the odd and even IM levels are summarized in Figures 6.20 and 6.21, respectively. One interesting observation is that the trends for the IM levels are not necessarily identical to those of the corresponding harmonic terms. While the even IM terms for both buffers show variations very similar to their respective even order harmonics, this is not true for the odd IM levels. The output in buffer 2 is the most dominant source for the odd harmonics, while its contribution to the odd IM levels is negligible. The IM products appear due to the mixing of the lower order clock harmonics with the RF signal. While the lower order harmonics arise predominantly due to the switching activity at the clock frequency, the higher order tones are the product of fast voltage transitions at the clock edges. The power spectrum plots for two voltage waveforms switching at identical clock frequencies, but with different rise and fall times are shown in Figure 6.22. The solid line corresponds to a transition time of 1ns, while the dashed line represents a rise and fall time of 0.2ns. It can be observed that the difference in transition speeds predominantly affects the higher order components. Thus, as the mechanisms generating the low frequency harmonics and high frequency harmonics are different, the trends for the IM levels and harmonics are expected to vary.

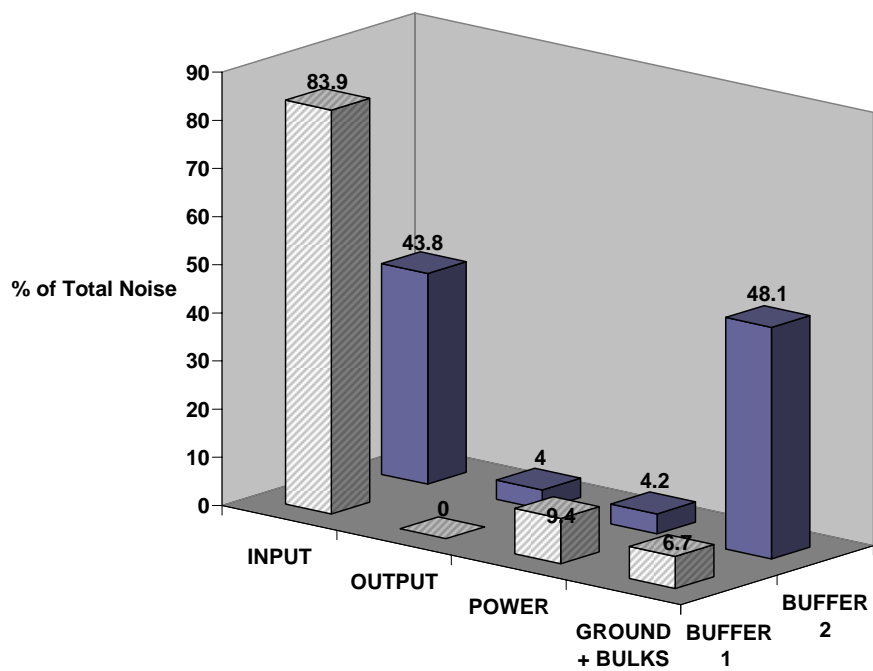


Figure 6.20. Individual contributions to the total odd IM noise levels for buffer 1 and buffer 2.

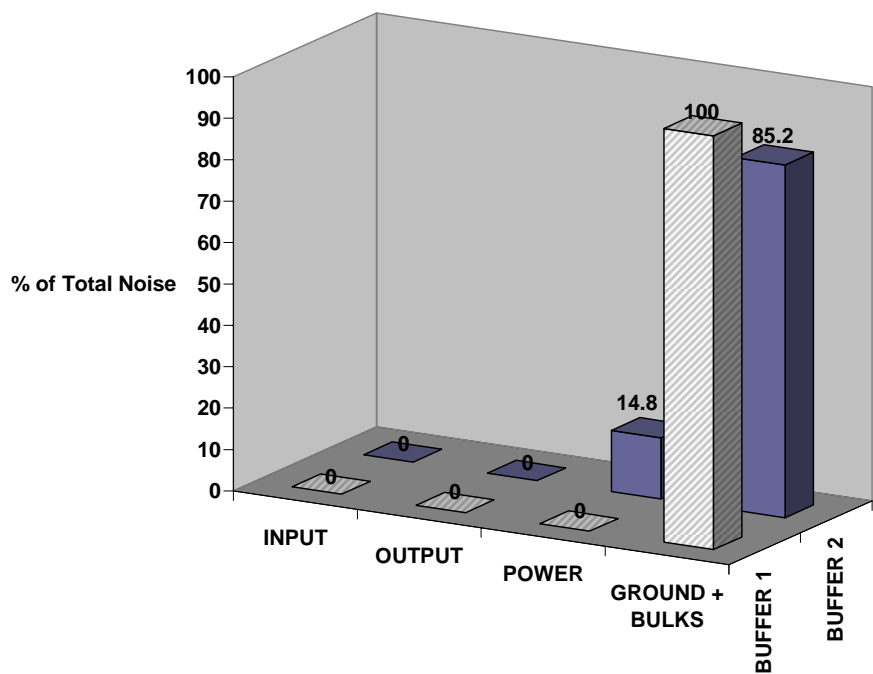


Figure 6.21. Individual contributions to the total even IM noise levels for buffer 1 and buffer 2.

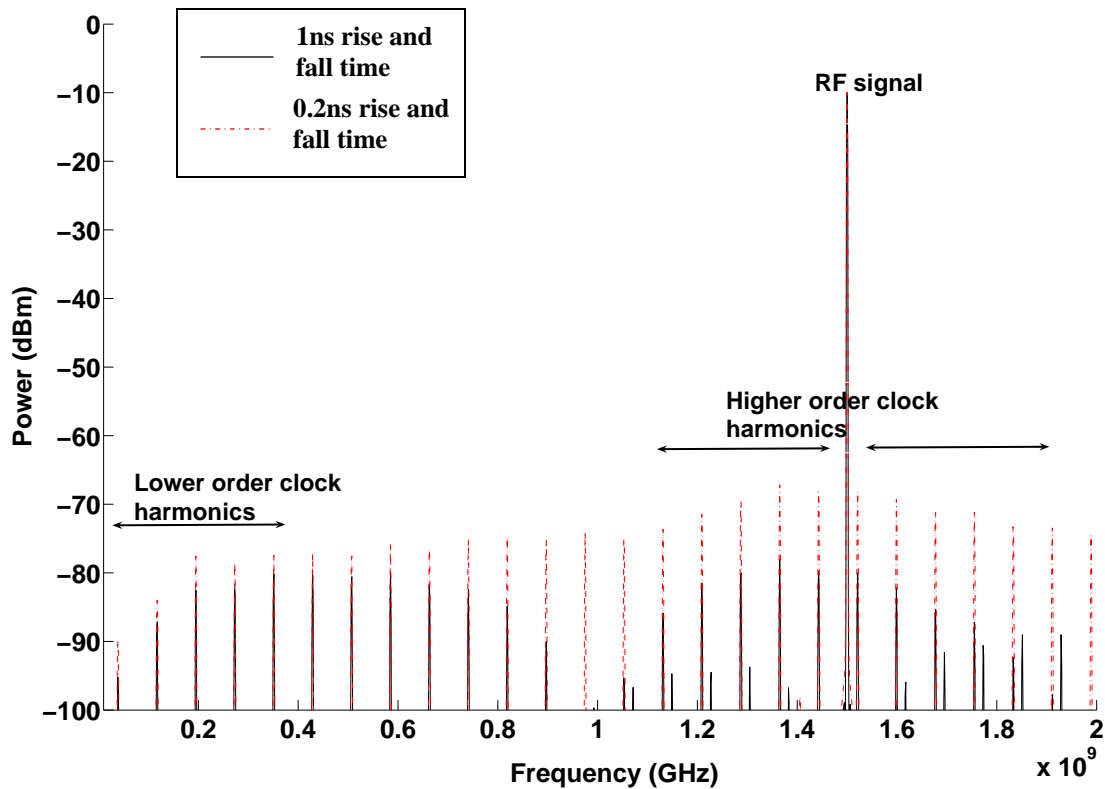


Figure 6.22. The effect of transition speeds on the frequency content of a switching voltage waveform.

The foregoing discussion shows that the stepped buffer interconnects are the primary sources for the noise injected into the substrate. Both, the absolute noise levels as well as the frequency content of the injected noise, are strongly dependent on the layout of the buffer's interconnects. Though these noise contributions cannot be completely eliminated, they can be minimized by proper layout techniques. It is

known that the noise generated in the power and ground lines is controlled by the parasitic inductance. Thus, reducing this inductance by minimizing the length of the board traces and the bond wires can help to lower the generated supply noise. It was seen that the dominant coupling path for noise from all the interconnects is the capacitance to the substrate. Minimizing this capacitance can significantly reduce the noise. This can be achieved by either reducing the dimensions of the on-chip interconnect or by using higher metal layers for routing as they have a weaker coupling to the substrate.

## 7. CONCLUSIONS

The noise injected into two single-ended 1.5GHz LNAs in a heavily doped process, with different substrate contact areas has been measured and simulated, with the substrate modeled as a resistive network. The measured and simulated results for the LNA S-parameters, as well as for the noise levels at the LNA output are in good agreement. The LNA with larger ground taps showed 2-12dB reduction in IM noise levels with the greatest reduction occurring in the 1<sup>st</sup> IM products. For clock frequencies much lower than the carrier frequency the 1<sup>st</sup> IM products are most detrimental as they lie closest to the signal frequency. Thus, a reduction in these tones is important. An increase in the substrate tap area by a factor of 400 improved the isolation by 9dB. Simulated results indicate that further scaling in the substrate tap area can bring even higher levels of isolation, at the expense of prohibitively large contacts. Guard rings of 0.6 $\mu$ m width placed around the input and cascode transistors added a further 6dB of isolation.

It was shown that the location of the substrate contacts also plays a significant role in the amount of noise reduction. Taps located close to sensitive nodes resulted in better noise performance. For the single-ended cascode topology considered, the input transistor was found to be most sensitive to substrate noise. A 50 $\mu$ m x 50 $\mu$ m substrate contact placed at a distance of 5 $\mu$ m from the input transistor reduced the noise levels by an additional 3dB as compared to contacts placed at the same distance from the bias or cascode transistors. It was also shown that substrate taps get more



effective as their proximity to the sensitive nodes is increased. Beyond a separation of approximately  $20\mu\text{m}$  the noise levels do not vary, reiterating the fact that at separations larger than five times the epi layer thickness, mutual resistances between contacts are not functions of the separation.

The analysis of the noise injection mechanisms in the stepped buffer demonstrated that the generated noise levels are a strong function of the buffer layout and routing. The dominant sources of noise were found to be the input and output interconnect capacitances to the substrate and the power and ground line inductances. The relative contributions of each of these sources also varied with the buffer layout. It was found that minimizing the length of the traces, on-chip and on the test board, reduced the amount of noise injection. A 50% reduction in all the interconnect lengths brought down the harmonic levels by 9-10dB.

The mismatch in the LNA S-parameters was attributed to the asymmetries in the board level routing. A ground plane discontinuity under the input and output trace of one of the LNAs could have contributed to this mismatch. This can be remedied by rotating the chip by  $180^\circ$ , since the pins of the two LNAs are perfectly symmetric. Due to a lack of time this measurement could not be incorporated in the thesis. Future work involving a similar analysis of ground taps for lightly doped substrates would prove useful owing to the growing popularity of these processes for RF applications. The impact of increased substrate taps on other analog and RF blocks like VCOs and PLLs needs to be examined. A method to automate the interconnect

and passive device modeling for performing substrate analysis would simplify the examination of more complicated circuits.

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**APPENDICES**

### Appendix A Printed Circuit Board (PCB)

This appendix provides a complete schematic of the PCB along with the component values. Also included, is a photograph of the board and general notes on the design of the PCB. Refer to figures A-1 and A-2.

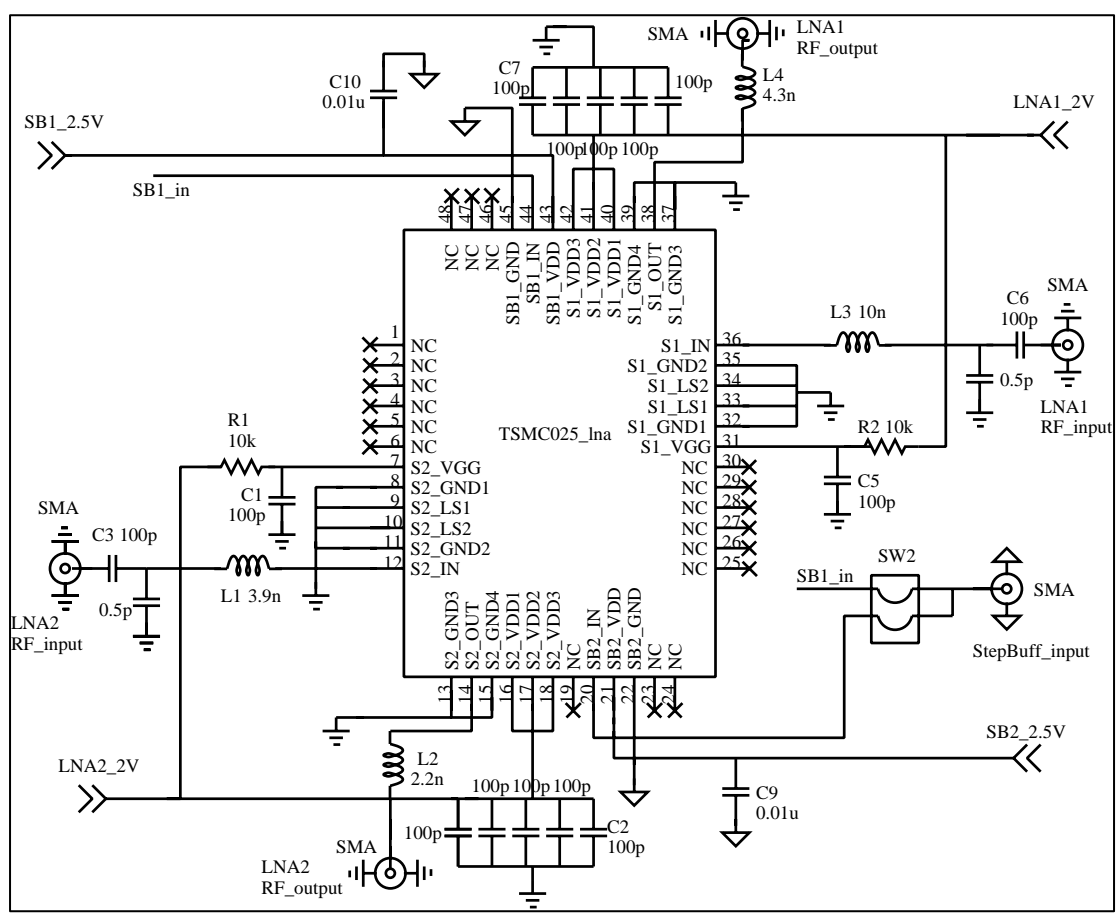


Figure A-1. Schematic of the printed circuit board.



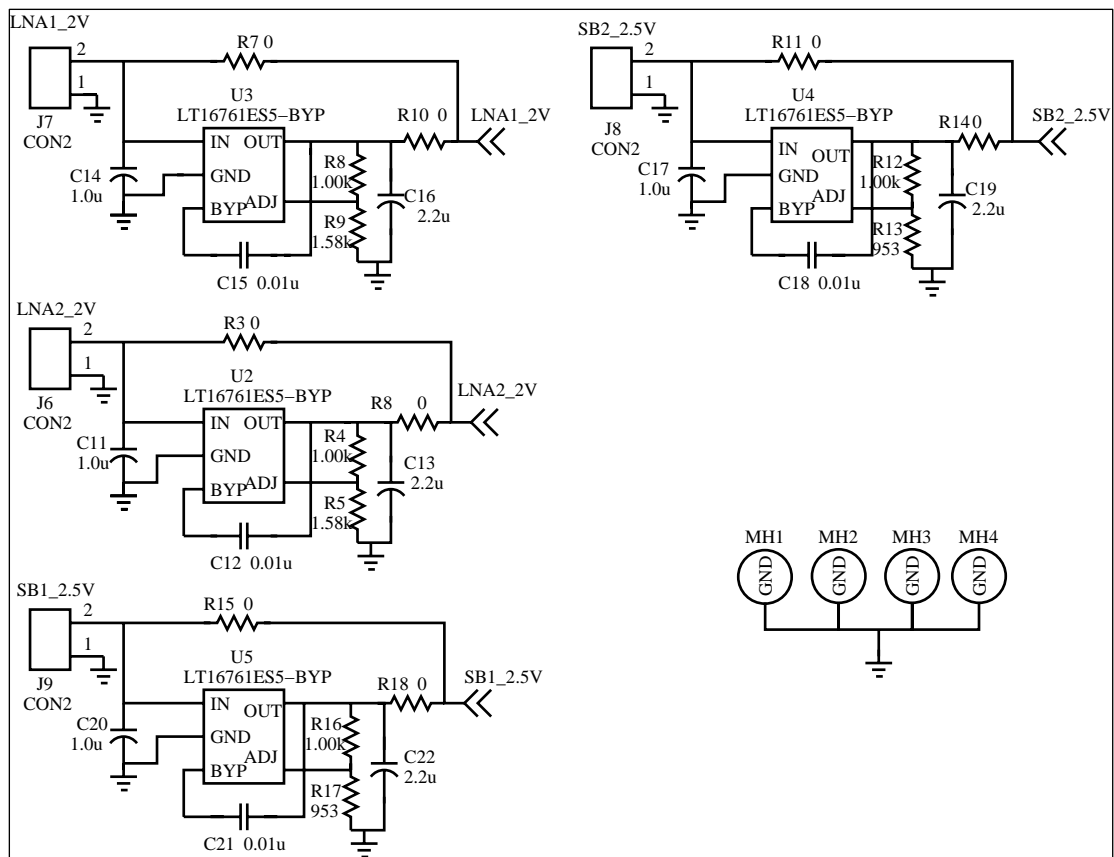


Figure A-2. Schematic of the printed circuit board.

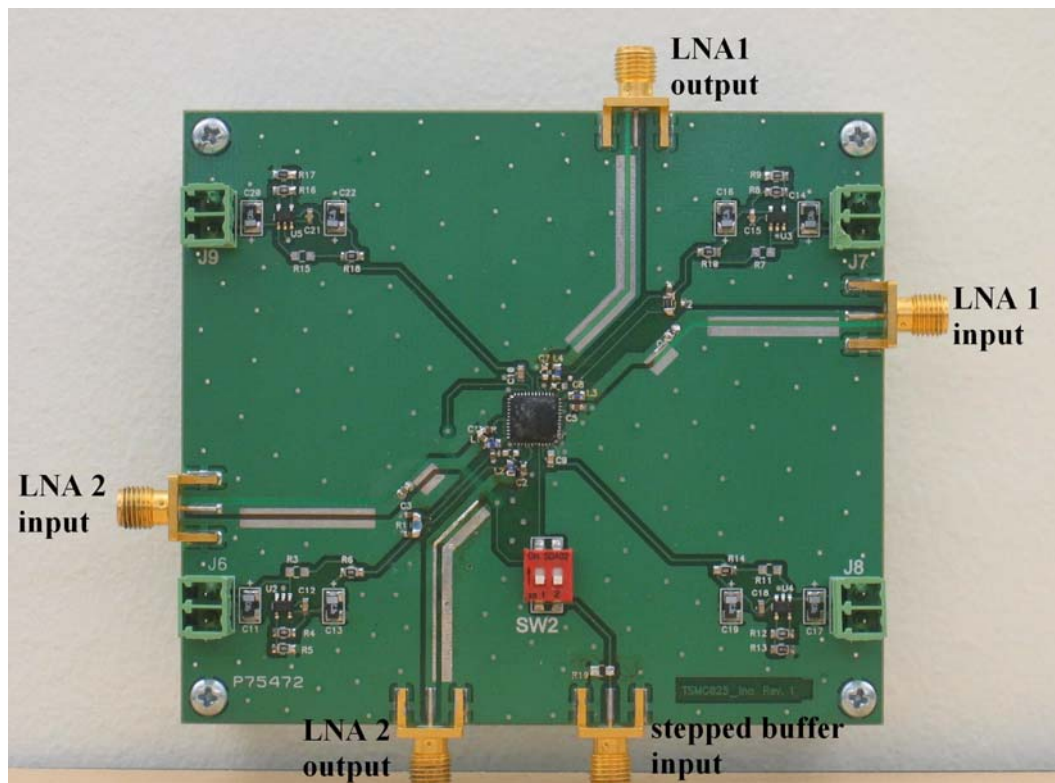


Figure A-3. Photograph of the test PCB.

### Design Notes

- 1) The board was laid out symmetrically to ensure similar PCB parasitics for both LNAs. It can be observed from the PCB photograph in Figure A-3 that the LNAs were placed and routed on diagonally opposite corners of the board. The two buffers and their supplies were routed in the remaining two corners.
- 2) All test circuits were provided with individual power supplies. The supply inputs were connected through low noise voltage regulators to provide isolation between the digital and analog circuits.

- 3) Power supply decoupling capacitors were placed very close to the IC pin to ensure maximum functionality. Several of them were placed in parallel for the 2V supplies of the LNAs to reduce the parasitic inductance of the supply path.
- 4) A single input was routed by means of a two-way switch to provide the clock input to the two buffers.
- 5) The bottom layer of the board was devoted to a continuous ground plane. The portions on the top layer devoid of signal traces, was also used as a ground plane. This was intended to reduce the unwanted coupling between signal traces. Several vias were added to stitch the bottom and top planes and to provide a true ground.
- 6) The RF transmission lines were all implemented as  $50\Omega$  controlled impedance traces. These traces were left exposed in places, to enable soldering of additional matching components if needed.
- 7) The LNAs have  $50\Omega$  input and output connections. SMA connectors were used to interface the board to the test equipment, as these have good performance at RF frequencies.
- 8) The off-chip matching components for the LNAs were placed as close to the IC as possible to reduce any unwanted PCB parasitics.

## **Appendix B Board, Package and On-chip Modeling**

### **PCB**

Models for the PCB traces were incorporated into the simulation setup. The 50 $\Omega$  input and output traces of the LNA were modeled as lossy transmission lines in Spectre. The presence of a ground plane discontinuity under two of these traces necessitated the use of more detailed models for them. A high frequency 3D EM simulation tool (HFSS) was employed to provide accurate S-parameter models, which were linked into Spectre as 2-port networks.

The surface mount R, L and C components on the board were included as either ideal components, or as SPICE models provided by the manufacturers.

### **Package**

Models were included for both the package leads and the bond wires. Capacitance and inductance data provided by the package manufacturer were used to generate the SPICE models for the leads. The bond wire models were calculated using geometric approximations outlined by the EIA/JESD59 bond wire modeling standard. This was used in conjunction with the 3D inductance and capacitance extraction tools, FastHenry and FastCap, respectively, to obtain the parasitics. An estimate of the bond wire lengths was obtained from a photograph of the packaged die before its encapsulation. This photo is shown in Figure 2.5 of Section 2

### On-chip Modeling

The on-chip interconnects for the LNA and stepped buffer were modeled as shown below in Figure B-1.  $L_s$  and  $R_s$  represent the series inductance and resistance of the line.  $C_{ox}$  depicts the oxide capacitance and  $R_{sub}$ , the spreading resistance of the substrate. The ground connection shown in this figure refers to the back plane or the single substrate node, which was connected to the PCB ground by the non-conductive epoxy used to attach the die to the die paddle. This epoxy layer was modeled as a capacitance. The values for these components were obtained from the TSMC 0.25 $\mu$ m process documentation and S-parameter simulation results from Momentum.

The models for the bond pads and the on-chip inductor and capacitor were taken from [18].

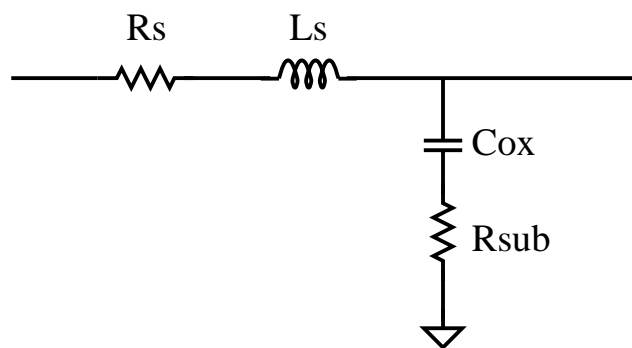


Figure B-1. SPICE model for on-chip interconnect.

### Appendix C LNA Center Frequency Shift

The  $S_{21}$  measurements of the LNA, designed for operation at 2.4GHz yielded a gain of 9dB centered around 1.5GHz. An explanation for this apparent shift in center frequency is presented in this section.

The output tuning of the LNA is typically controlled by the drain inductor and the output capacitor. However, the input and output impedance match can also have a significant effect on the gain response of the LNA. Since the on-chip magnitude response of the LNA achieved by tuning the drain inductor and capacitor gets shaped by the external input and output matching networks, a poor impedance match at the intended frequency of operation can reduce the  $S_{21}$  magnitude at that frequency. Large parasitic inductors at the LNA input and output result in lower frequency resonances for  $S_{11}$  and  $S_{22}$ , respectively. Due to larger reflection coefficients at the frequency of design the corresponding magnitude of the overall gain is lower. Better impedance match at lower frequencies results in higher gain at these frequencies. This results in a shifted appearance for the magnitude response. Two dominant factors were found to have contributed to the increased parasitics in the input and output lines.

- 1) Longer package bond wires owing to smaller die size, resulted in increased bond wire inductances.

2) The presence of a ground plane discontinuity on the test board, under the input and output traces resulted in longer current return paths, and hence larger loop inductances.

The latter factor was found to be more detrimental. The shift in  $S_{11}$  and  $S_{22}$ , and the resulting  $S_{21}$  after incorporating these additional parasitics is indicated in Figure C-1. It can be observed that the reduced resonant frequencies of  $S_{11}$  and  $S_{22}$  result in the magnitude response shifting to 1.5GHz.

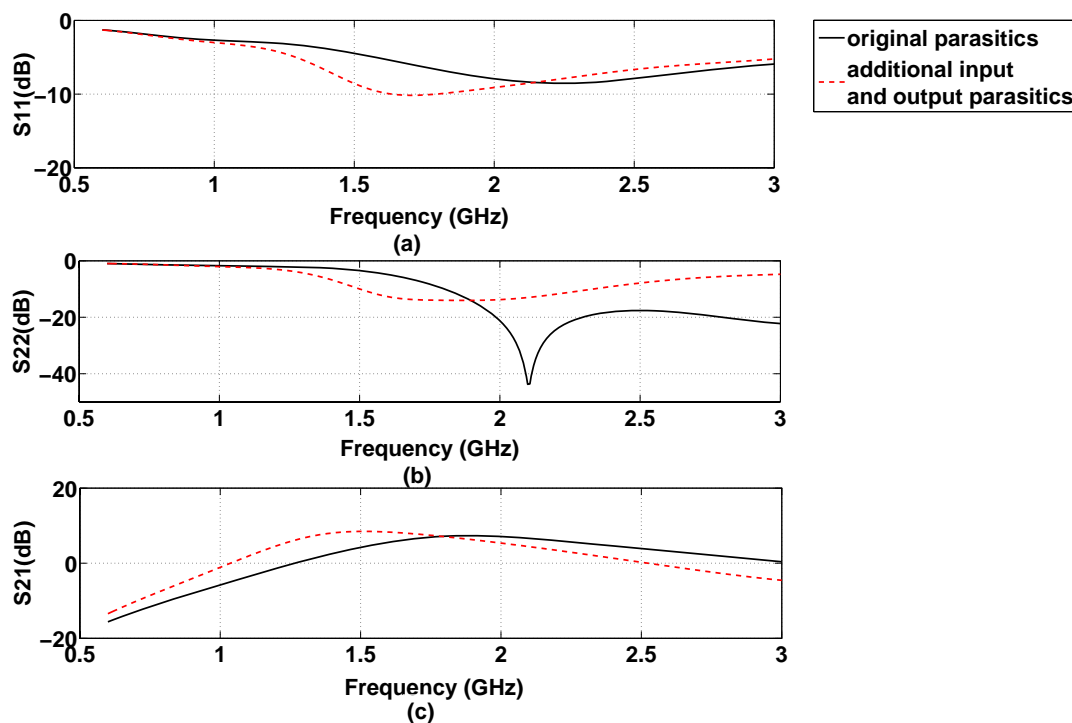


Figure C-1. The effect of additional input and output parasitics on the S-parameters of the LNA. (a)  $S_{11}$ . (b)  $S_{22}$ . (c)  $S_{21}$ .

## Appendix D Additional Test Cases for Analyzing the Influence of Substrate Contact Sizing

This section provides the substrate contact layouts for all intermediate test cases, simulated in order to quantify the influence of contact sizing on the noise performance of the LNA.

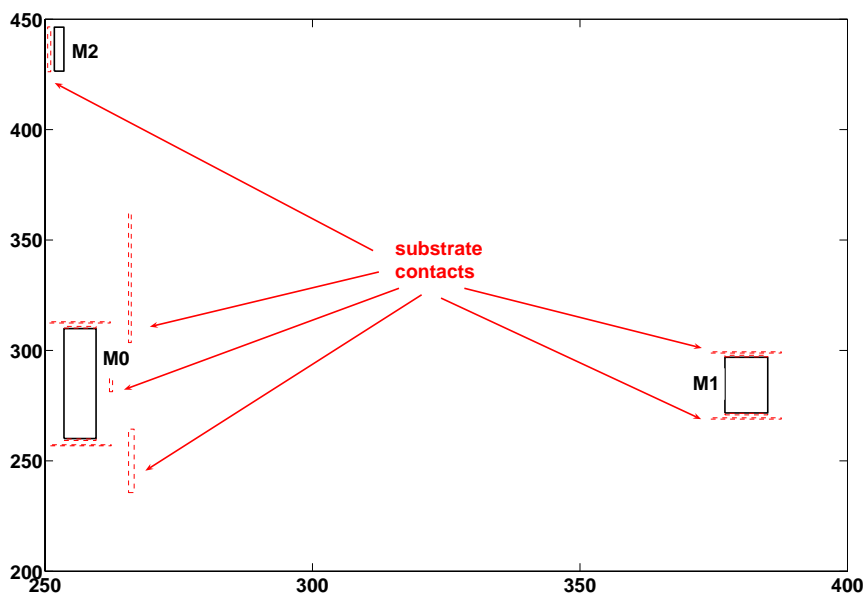


Figure D-1. Layout for substrate contact area of  $2X = 120\mu\text{m}^2$ .

$$IM_{\text{rms}} = -67.72\text{dBm.}$$

Figures D-1 – D-7 provide the layouts for the seven intermediate test cases. The last three figures in the section show the substrate contact positions for the additional cases simulated to analyze the noise trends for contact areas larger than  $400X$ .



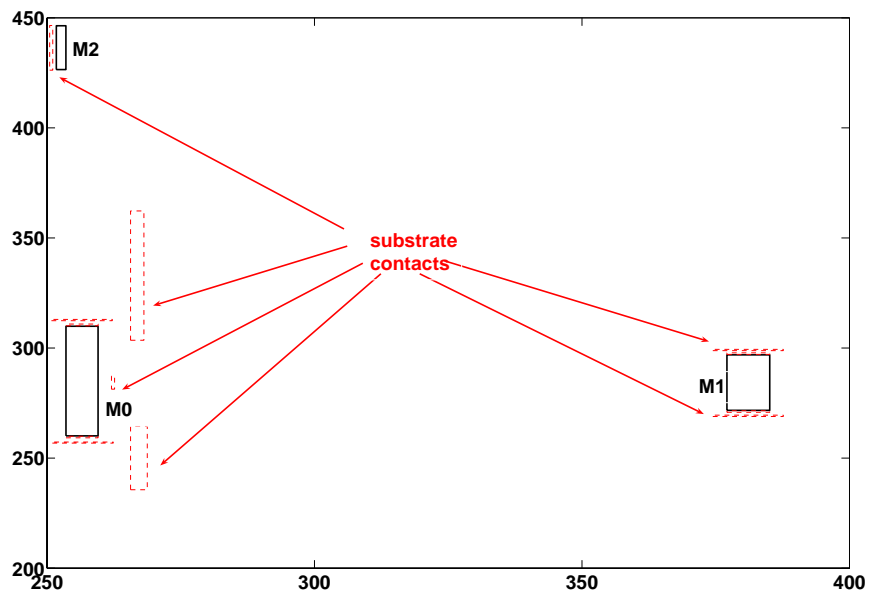


Figure D-2. Layout for substrate contact area of  $5X = 300\mu\text{m}^2$ .

$$\text{IM}_{\text{rms}} = -67.92\text{dBm}.$$

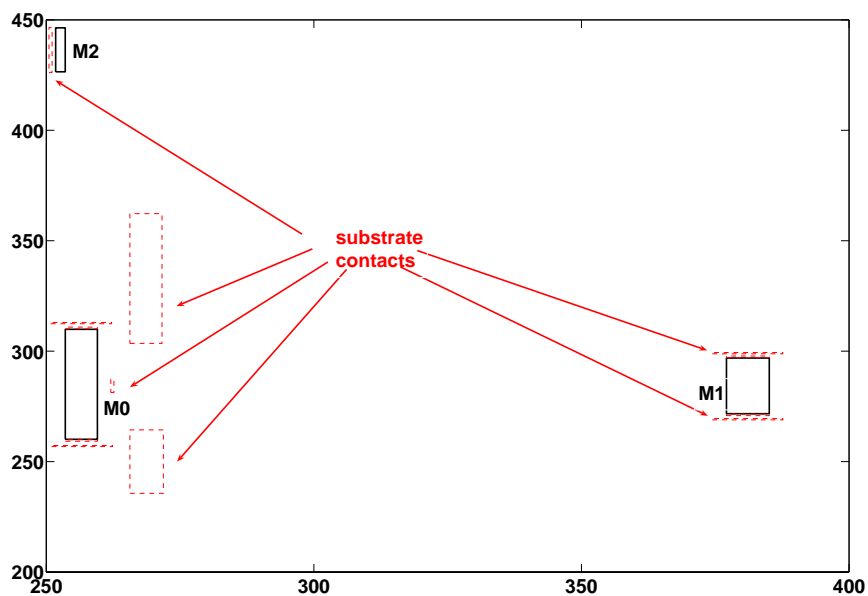


Figure D-3. Layout for substrate contact area of  $10X = 600\mu\text{m}^2$ .

$$\text{IM}_{\text{rms}} = -68.07\text{dBm}.$$

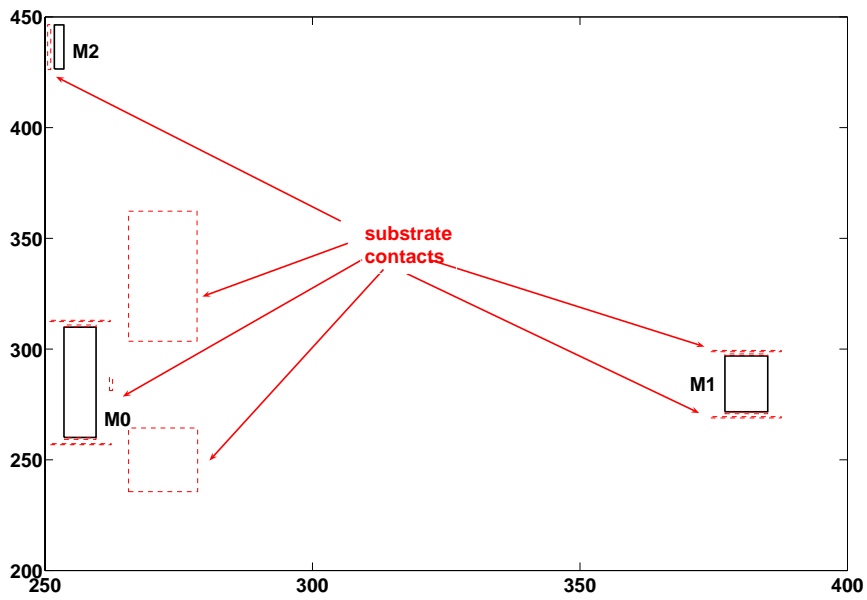


Figure D-4. Layout for substrate contact area of  $20X = 1,200\mu\text{m}^2$ .

$$IM_{\text{rms}} = -68.38\text{dBm}.$$

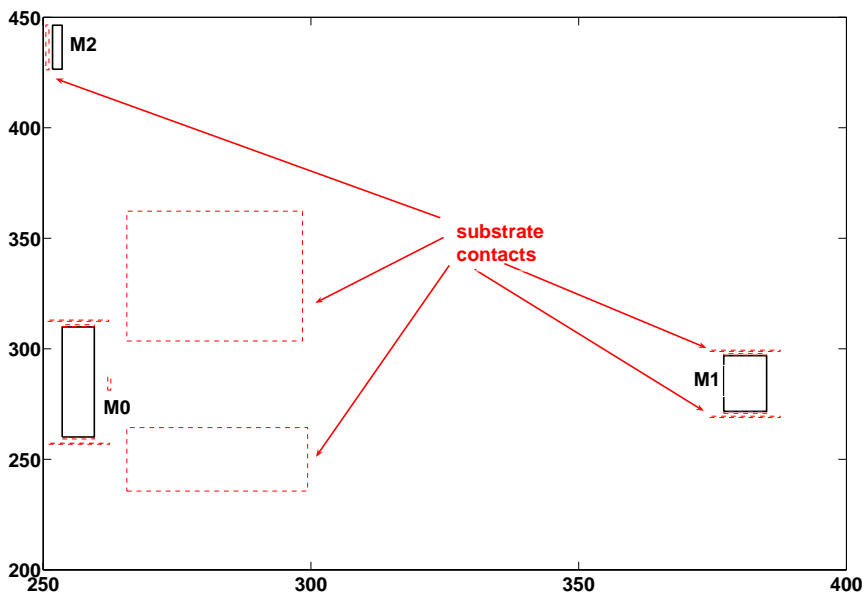


Figure D-5. Layout for substrate contact area of  $50X = 3,000\mu\text{m}^2$ .

$$IM_{\text{rms}} = -69.15\text{dBm}.$$

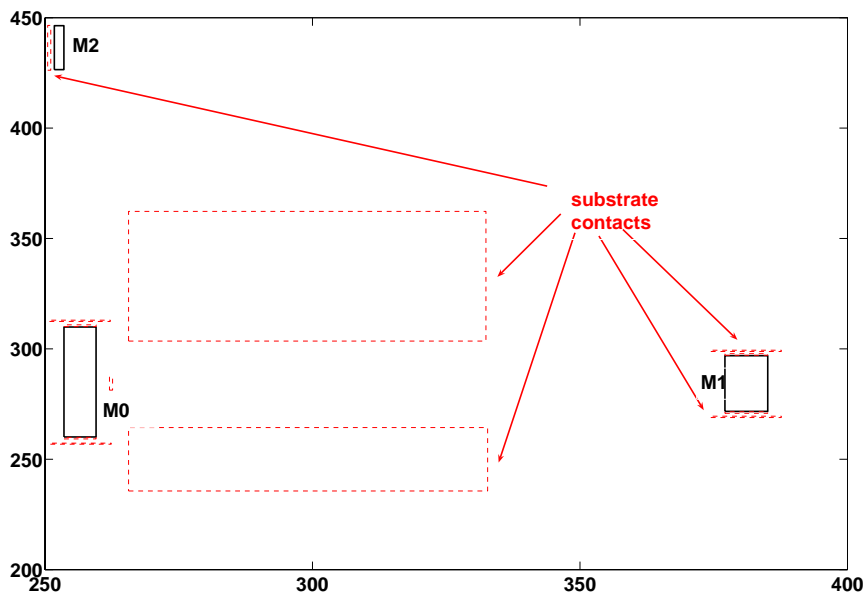


Figure D-6. Layout for substrate contact area of  $100X = 6,000\mu\text{m}^2$ .

$$IM_{\text{rms}} = -70.25\text{dBm.}$$

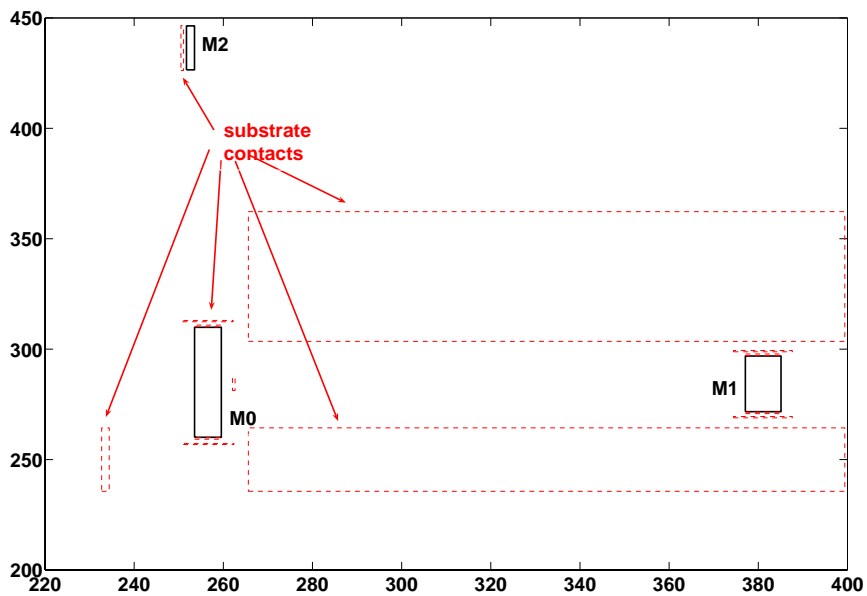


Figure D-7. Layout for substrate contact area of  $200X = 12,000\mu\text{m}^2$ .

$$IM_{\text{rms}} = -72.1\text{dBm.}$$

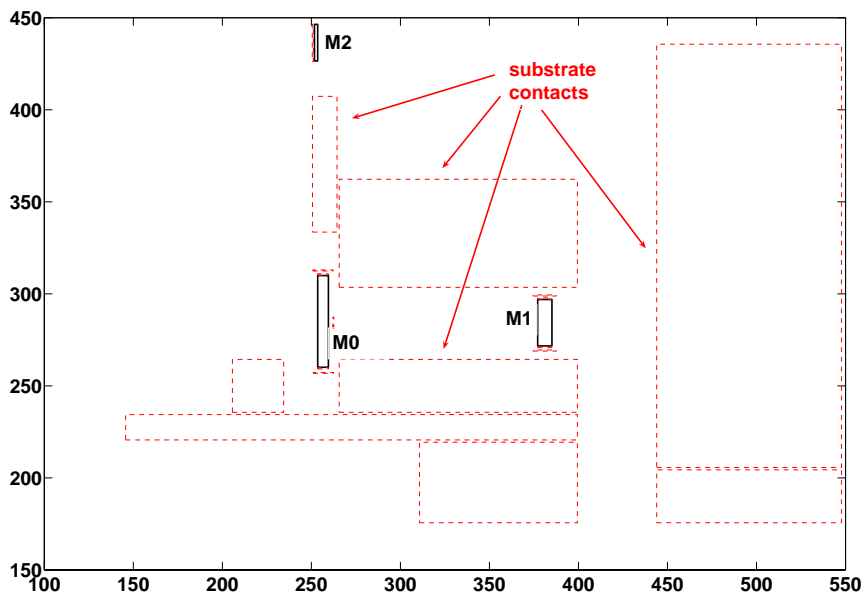


Figure D-8. Layout for substrate contact area of  $800X = 48,000\mu\text{m}^2$ .

$$IM_{\text{rms}} = -78.8\text{dBm.}$$

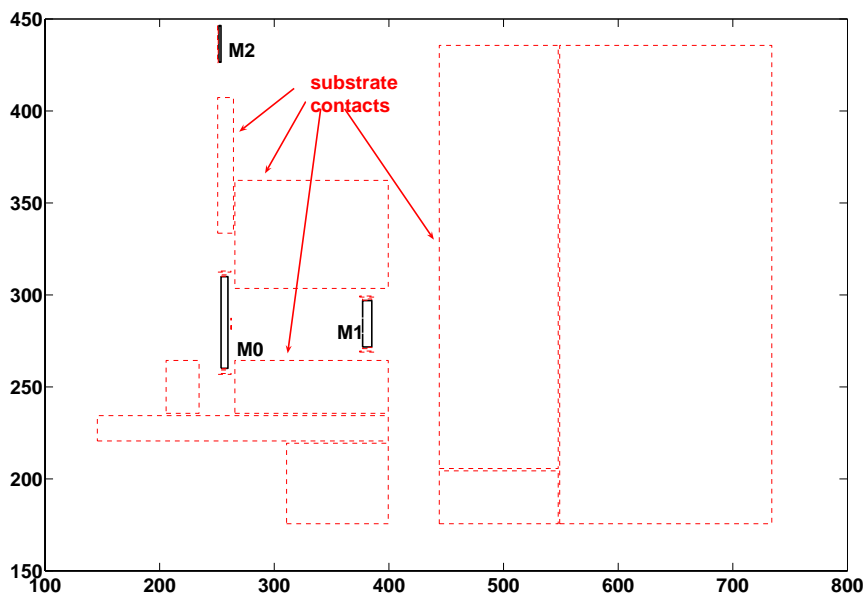


Figure D-9. Layout for substrate contact area of  $1,600X = 96,000\mu\text{m}^2$ .

$$IM_{\text{rms}} = -82.1\text{dBm.}$$

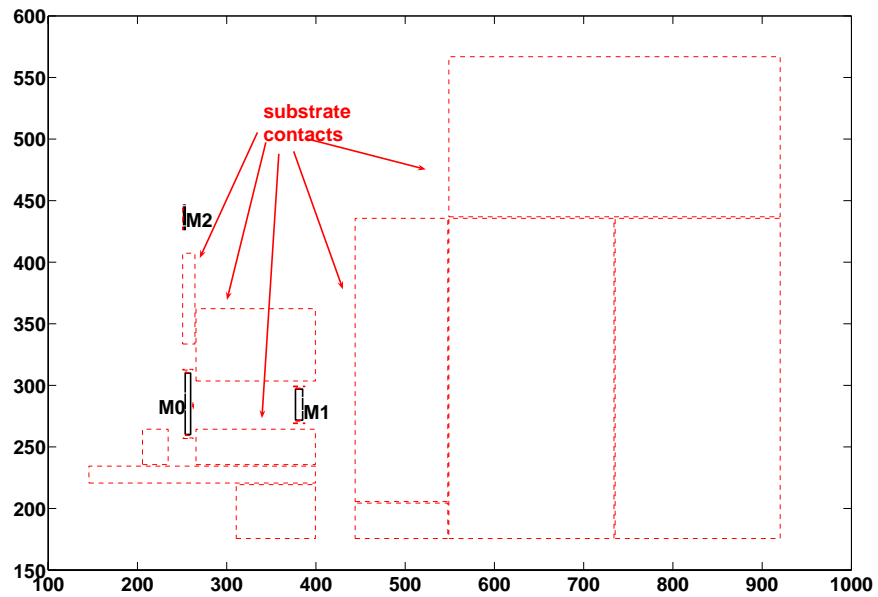


Figure D-10. Layout for substrate contact area of  $3,200X = 192,000\mu\text{m}^2$ .

$$\text{IM}_{\text{rms}} = -83.25\text{dBm}.$$