AN ABSTRACT OF THE DISSERTATION OF

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Evolution of the mobile communication standards and proliferation of hand-held devices mandate stringent Analog-to-Digital Converter (ADC) specifications. Among various ADCs, a $\Delta\Sigma$ ADC is best known as a power-efficient ADC when more than 12b is required. However, a conventional discrete-time (DT) $\Delta\Sigma$ Modulator ($\Delta\Sigma$M) is inadequate for low-power wideband applications due to the opamp settling requirement. Alternatively, a continuous-time (CT) $\Delta\Sigma$M can be used to decrease power consumption but has its own disadvantages such as clock jitter sensitivity, RC time constant variation, and excess loop delay.

The wideband modulators are often implemented as single-loop high-order modulators in a deep submicron process. The high-order modulator typically has a quantizer overloading problem as the input signal approaches to a full-scale range. A pole-optimization method can be used to extend the linear input range but it inevitably decreases signal to quantization noise ratio. This causes power penalty since it limits the maximum input power available.

Another challenge is linearizing a nonlinear multi-bit Digital-to-Analog Converter (DAC). On one hand, the DAC can be linearized by element sizing, sorting,

and calibration but these increase silicon area and power consumption. On the other hand, a Dynamic Element Matching algorithm (DEM) linearizes the DAC by averaging and shaping the mismatches with minimal design overhead. However, the DEM causes additional delay inside the feedback path. This can make the modulator unstable.

In this thesis, a multi-bit 3rd-order hybrid $\Delta\Sigma$M with over full-scale range and no DEM in the critical feedback path is presented. Removing the DEM in the critical path enables the modulator to minimize latency in the feedback path. A digital feedforward structure allows processing the input signal over the full-scale reference voltage. Combined benefits of the CT/DT implementation help to reduce power consumption and to mitigate the loop delay. Measurement results from a prototype demonstrate the effectiveness of the proposed ideas.

A Multi-Bit Hybrid DSM over Full-Scale Range without Feedback DEM

by

Sunwoo Kwon

A DISSERTATION

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APPROVED:

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Sunwoo Kwon, Author

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CHAPTER 1. INTRODUCTION

Evolution of the mobile communication standards and proliferation of hand-held devices mandate stringent Analog-to-Digital Converter (ADC) specifications: low power consumption for extended battery-operation time, wide bandwidth (BW) for fast data conversion, and high resolution/dynamic range for clear signal conversion without being corrupted by noise and interferers. As an example, one of the recent communication standards called Wireless Broadband requires signal BW larger than 9MHz and high data rate over 100Mbps [1] with minimum power consumption.

There are three candidates to meet the requirements: a pipeline ADC, a successive approximation ADC, and a $\Delta\Sigma$ Modulator ($\Delta\Sigma$M). The following section helps to select which type of ADC is best suited for the above demands.

1.1 ADC Literature Survey

Among various ADCs, the $\Delta\Sigma$M is best known as a power-efficient ADC when more than 12b is required. Fig. 1.1 shows comparison result between the Nyquist-rate ADCs and the $\Delta\Sigma$Ms, published from 2001 to 2009. Traditionally, the $\Delta\Sigma$Ms have been extensively utilized for low frequency applications whose signal BW is lower than several MHz ranges as demonstrated in Fig. 1.1. This is due

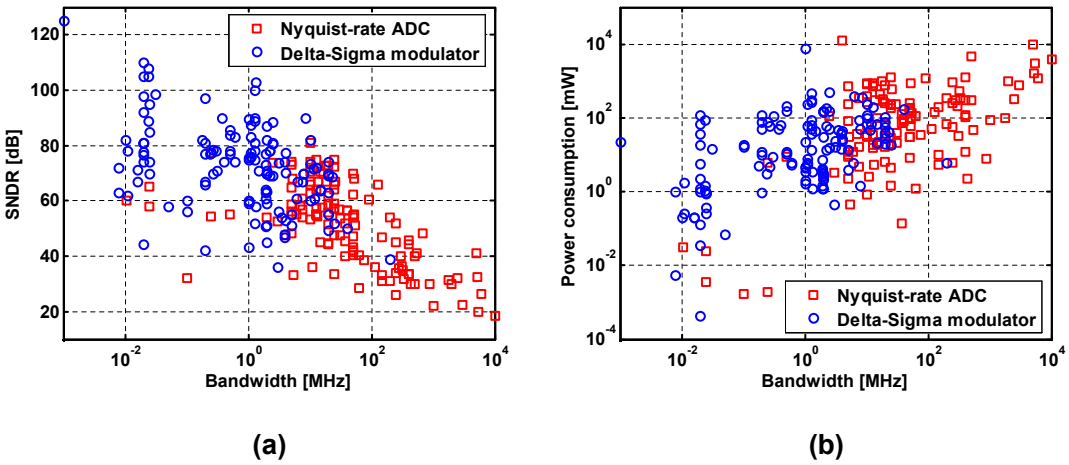

Figure 1.1: Performance comparison between Nyquist-rate ADCs and $\Delta\Sigma$ modulators: (a) SNDR versus bandwidth and (b) Power consumption versus bandwidth.

to the fact that, oversampling enables the modulator to reduce capacitor size and to tolerate circuit imperfections, e.g., finite opamp DC gain and Gain-BandWidth product (GBW) and noise shaping further suppresses in-band quantization noise and circuit imperfections. Consequently, the $\Delta\Sigma$M comprises simple analog circuitry in concert with less stringent circuit design requirements compared with the Nyquist-rate ADCs, which allows the $\Delta\Sigma$M to achieve more power-efficient signal conversion. At several MHz ranges, the $\Delta\Sigma$Ms has comparable performance to the Nyquist-rate ADCs. In the following section, it can be seen that the $\Delta\Sigma$M can extend signal BW over several tens MHz while maintaining its power-efficiency.

1.2 Delta-Sigma Modulator for Wideband Application

Recently, there are several efforts to increase $\Delta\Sigma$M's signal BW. Table 1.1 compares performance of the Nyquist-rate ADC and the $\Delta\Sigma$M whose BW is larger than 10 MHz and Signal-to-Noise-Distortion Ratio (SNDR) is higher than 70 dB.

Table 1.1: 20-40 MSPS 12-14b ADC performance comparison..

	ADC	BW [MHz]	SNDR [dB]	Power [mW]	FoM [pJ/Cn]	L_{MIN} [um]
□	Honda [2]	15	71	102	1.17	0.25
□	Siragusa [3]	20	72	394	3.03	0.18
□	Matsui [4]	10	70	34	0.66	0.18
□	Liu [5]	10	74	233	2.84	0.18
△	Hesner [6]	20	81	66	0.18	0.13
○	Moyal [7]	12	79	75	0.43	0.25
○	Bosi [8]	10	74	240	2.93	0.18
○	Mitteregger [9]	20	74	20	0.12	0.13
○	Malla [10]	20	70	28	0.27	0.09

$$\text{FoM} = \frac{\text{Power}}{2\text{BW} \cdot 2^{\left(\frac{\text{SNDR}-1.76}{6.02}\right)}}$$

□ Nyquist-rate ADC
△ Oversampled ADC
○ Delta-Sigma modulator

References [2], [3], [4], [5] are pipeline ADCs. Reference [6] is an oversampled successive-approximation ADC. References [7], [8], [9], [10] are ΔΣMs. As a metric of power efficiency, Figure of Merit (FoM) is used in the table. It is clear that the ΔΣMs can extend BW over 10 MHz more efficiently compared to the Nyquist-rate ADCs.

However, increasing signal BW of the ΔΣM is a difficult task. This is owing to the fact that the maximum sampling frequency is usually limited by technology and that the stability of ΔΣM degrades as the order of the ΔΣM increases [11]. Given that the sampling frequency and the order of the ΔΣM are fixed, the choice of implementation method heavily affects power efficiency. The next section provides a brief comparison between Discrete-Time (DT) and Continuous-Time (CT) implementation methods.

1.3 Discrete-Time and Continuous-Time Implementation

A DT ΔΣM requires higher GBW than a CT counterpart since the settling error of a CT integrator is less than that of a DT integrator, when GBW is relatively small [11]. References [8], [10] are implemented in DT domain, whereas [7], [9] are implemented in CT domain.

In spite of the power efficiency of the CT implementation, it has its own disadvantages, such as RC time constant variation, DAC clock jitter sensitivity, and excess loop delay. Hence, it is vital to understand the pros and cons of each implementation method. These are discussed in Chapter 2.

1.4 Linearizing Multi-Bit Digital-to-Analog Converter

A multi-bit quantizer/DAC is frequently utilized in the recent ΔΣMs since it provides numbers of benefits compared to a single-bit quantizer/DAC [11], [12]. Nonetheless, a physically built multi-bit DAC is inherently nonlinear, so a linearization technique should be applied so as not to degrade modulator performance. A calibration in analog domain can linearize the multi-bit DAC, but it usually increases silicon area and power consumption. On the other hand, a Dynamic Element Matching (DEM) technique [13] linearizes the DAC with minimal overhead. However, this introduces latency between the quantizer and the DAC. Consequently, at high clocking frequencies, it is difficult to perform the DEM algorithm.

The main focus of this thesis is linearizing the multi-bit DAC with minimal overhead and delay. By eliminating the DEM in the critical feedback path and by

putting the DEM in a forward path, a proposed modulator can have minimized feedback latency. More details can be found in Chapter 3.

1.5 Thesis Organization

Chapter 2 provides review of DT and CT implementation method, and DAC linearization techniques since appreciating the design challenges is a key for successful implementation. Chapter 3 presents a novel $\Delta\Sigma$ modulator which enables eliminating the DEM in the feedback path. Detailed system design method is provided. Circuit implementation is described in Chapter 4. Silicon measurement results are shown in Chapter 5. Conclusion for this thesis is drawn with a summary of the work.

CHAPTER 2. REVIEW OF PROPERTIES AND MULTIBIT DAC LINEARIZATION TECHNIQUES

Design challenges in wideband ΔΣMs and DAC linearization methods are reviewed. Several properties which impact modulator performance are discussed in this chapter.

2.1 Frequency Scalability and Pole/Zero Location

Integrators can be implemented in either DT or CT domain as shown in Fig. 2.1. The DT implementation, also known as Switched-Capacitor (SC) implementation, utilizes an equivalent resistor, a periodically charged/discharged capacitor. The equivalent resistance is given by (2.1). Note that the time constant of the DT implementation, τ_{DT}, is determined by clock period, $\mathrm{T_S}$, and relative ratio between $\mathrm{C_S}$ and $\mathrm{C_I}$.

$$\tau_{DT} \;=\; R_{EQ}C_I \;=\; T_S\frac{C_I}{C_S},\ where\ T_S = \frac{1}{F_S} \tag{2.1}$$

$$\tau_{CT} \;=\; R_{CT}C_{CT} \tag{2.2}$$

On the other hand, the time constant of the CT implementation, τ_{CT}, is determined by absolute value of capacitor and resistor as shown in (2.2). Process, voltage, and temperature variation cause the time constant to deviate from an ideal value, thus a time constant tuning scheme is required for the CT implementation. The tuning scheme helps the CT integrator to have frequency scalability, but the scalability is limited by the tuning range of the scheme. Tuning circuitry can be an

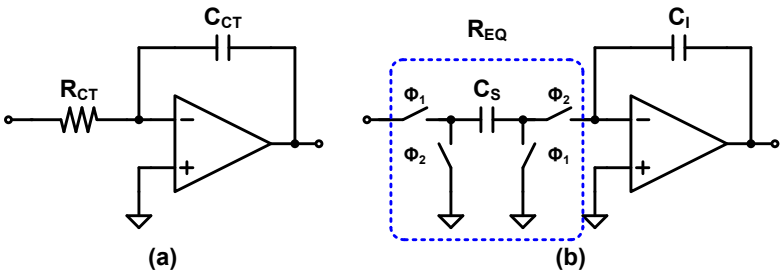

Figure 2.1: Integrator implementation: (a) Continuous-time integrator and (b) Discrete-time integrator.

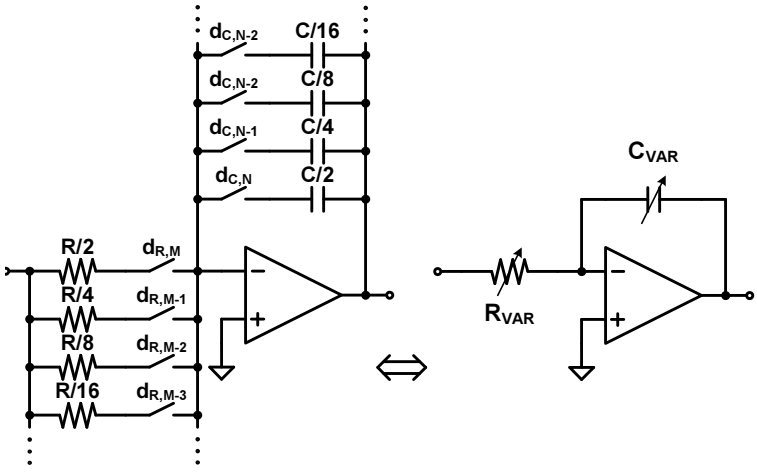

Figure 2.2: RC time constant tuning circuit for a continous-time integrator using a N-bit capacitive array and a M-bit resistive array.

array of resistors and/or capacitors as illustrated in Fig. 2.2, but increases silicon area due to routing and segmentation.

The discrete-time time constant, τ_{DT}, depends on the ratio between C_S and C_I, and sampling time which is precise. As a result, pole/zero location of the DT filter is accurately controlled to within $\pm$ 0.1 %. However, the continuous-time time constant, τ_{CT}, varies typically $\pm$ 20 % since two different materials cannot have the same variation. This variation can be controlled by the tuning circuit but the resolution of the tuning circuit still limits accurate pole/zero positioning. For

example, a time constant tuning circuit shown in Fig. 2.2 has a M+N-bit tuning accuracy. Time constant deviation from the ideal value will appear as integrator gain error and actual time constant, $\tau_{\mathrm{CT,a}}$, can be expressed by

$$\begin{aligned} \frac{1}{\tau_{CT,a}} &= \frac{1}{R_{CT,a}C_{CT,a}} = \frac{1}{R_{CT}C_{CT}(1+\Delta_R\Delta_C)} \\ &\approx \frac{1}{R_{CT}C_{CT}}(1-\Delta_R\Delta_C) \; when \; \Delta_R\Delta_C \ll 1 \end{aligned} \tag{2.3}$$

This gain variation changes the Noise Transfer Function (NTF) of a CT $\Delta\Sigma$M. As a result, integrator output swing increases (decreases) and the modulator performance improves (degrades) since a higher NTF pushes more noise to higher frequency and increases out of band gain. It is worth mentioning that the modulator becomes unstable when the time constant becomes relatively small, depending on the modulator topology and opamp swing range.

2.2 Clock Jitter Sensitivity

Apart from the input path of a modulator, in which the input frequency is always less than sampling frequency, a feedback DAC path processes all the frequency contents inside the modulator loop. As a result, any jitter induced on the DAC severely deteriorates modulator performance. Fig. 2.3 shows the effect of the DAC clock jitter for two implementation methods, especially when a single-bit DAC is used. Assuming that the opamp in the CT integrator is ideal, the waveform of $\mathrm{I_{DAC,CT}}$ is rectangular. When the jitter is induced on $\mathrm{V_{REF}}$ at the falling edge by σ_T, the jitter decides sampling instance of $\mathrm{I_{DAC,CT}}$. Consequently, the output of the CT integrator, $\mathrm{V_{O,CT}}$ has an error voltage, $\varepsilon_{\mathrm{O,CT}}$. This error is proportional to the amount of current and jitter.

On the other hand, the waveform of $\mathrm{I_{DAC,DT}}$ is exponentially decaying due

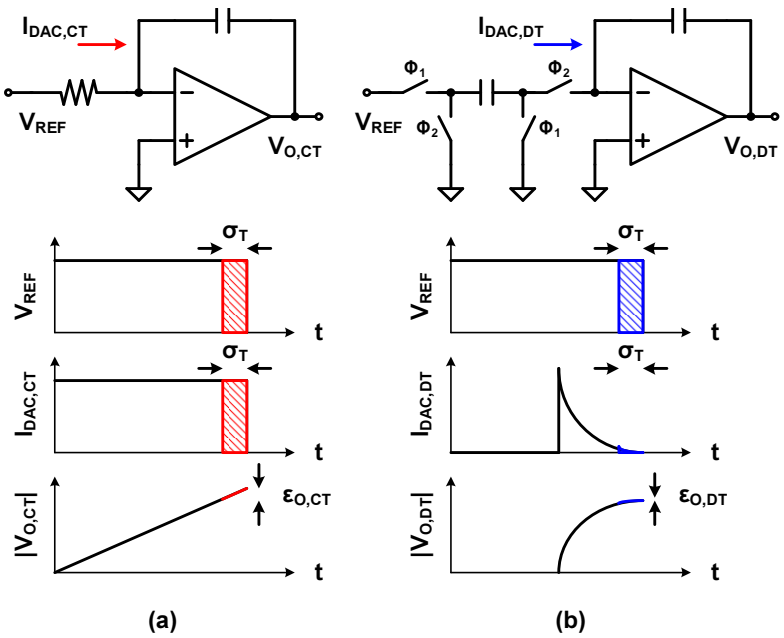

Figure 2.3: DAC clock jitter effect in: (a) Continuous-time integrator and (b) Discrete-time integrator.

to the nature of charge transfer with limited speed. The time constant of this exponential behavior depends on transconductance of opamp, equivalent resistance of switches, and capacitor values. The jitter forces charge integration to stop, but the output of the DT integrator, $V_{O,DT}$, has less deviation since major portion of charge is already transferred to the output. This is why the DT implementation has less jitter sensitivity compared to the CT implementation.

To mitigate the DAC clock jitter in the CT integrator, a Switched-Capacitor Resistor (SCR) technique [14], [15] can be used. The SCR is a variation of the DT implementation which has a large resistor to limit a peak current value. Increasing the number of levels of the DAC also helps to decrease the jitter-induced error since the multi-bit DAC has a smaller voltage step. For example, a N-bit DAC can have a minimum voltage step of $V_{REF}/2^{N-1}$ compared to the single-bit DAC

of which voltage step is V_{REF}.

2.3 Finite Opamp DC gain

Finite opamp DC gain, A_O, causes not only integrator gain error, λ_{dc}, but also phase erorr, γ. The transfer function of actual DT integrator can be modeled by (2.4) [16], [17]. The CT integrator also has modified transfer function which can be modeled by (2.5). Circuit implementation of each integrator can be referred to Fig. 2.1.

$$H_{DT,a}(z) \approx (1+\lambda_{DT,dc})\frac{C_S}{C_I}\frac{z^{-1}}{1-(1+\gamma_{DT})z^{-1}}, \tag{2.4}$$

$$where\ \lambda_{DT,dc} \approx -\frac{1}{\beta A_O}\ and\ \gamma_{DT} \approx -\frac{1}{\beta A_O}$$

$$H_{DT,a}(s) \approx (1+\lambda_{CT,dc})\frac{1}{R_{CT}C_{CT}}\frac{1}{s+\gamma_{CT}}, \tag{2.5}$$

$$where\ \lambda_{CT,dc} \approx -\frac{1}{A_O}\ and\ \gamma_{CT} \approx -\frac{1/R_{CT}C_{CT}}{A_O}$$

2.4 Finite Opamp GBW: Settling Error

The opamp is one of the most power-hungry building blocks in the ΔΣM. Hence, reducing power consumption of the opamp enables a desinger to improve power efficiency of the ΔΣM. However, decreasing GBW causes integrator gain error, λ_{GBW}.

First, consider an ideal DT integrator whose transfer function, $H_{DT,i}$, is given by (2.6). Assuming that GBW is finite and settling behavior is not limited by slew rate, the transfer function of the actual DT integrator, $H_{DT,a}$, is modified [16], [18]

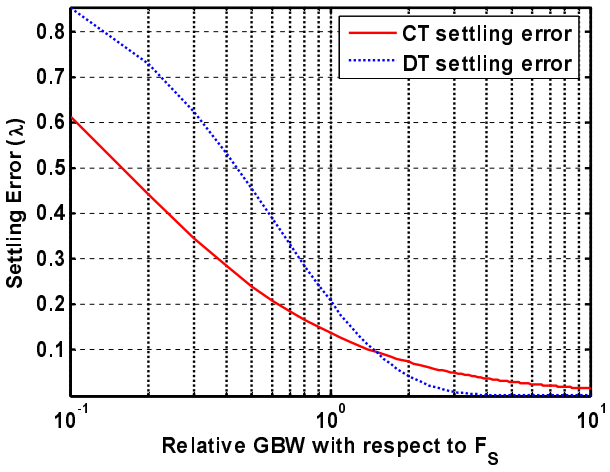

Figure 2.4: GBW-induced settling error in continuous-time integrator (red solid) and discrete-time integrator (blue dotted). Opamp GBW is normalized to sampling frequency, F_S

and given by (2.7). Note that $\frac{C_I}{C_S+C_I}$ is the feedback factor of the DT integrator.

$$H_{DT,i}(z) = \frac{C_S}{C_I}\frac{z^{-1}}{1-z^{-1}} \tag{2.6}$$

$$H_{DT,a}(z) \approx (1+\lambda_{DT})\frac{C_S}{C_I}\frac{z^{-1}}{1-z^{-1}}, \tag{2.7}$$

$$where\ \lambda_{DT,\ GBW} \approx -exp\Big(-\pi\frac{C_I}{C_S+C_I}\frac{GBW}{F_S}\Big)$$

Now, consider an ideal CT integrator whose transfer function, $H_{CT,i}$, is given by (2.8). Using the same assumption and ignoring the finite delay, the transfer function of the actual CT integrator, $H_{CT,a}$, is modified and given by (2.9).

$$H_{CT,i}(s) = \frac{1}{sR_{CT}C_{CT}} \tag{2.8}$$

$$H_{CT,a}(s) \approx (1+\lambda_{CT})\frac{1}{sR_{CT}C_{CT}}, \tag{2.9}$$

$$where\ \lambda_{CT,\ GBW} \approx -\frac{1/R_{CT}C_{CT}}{\omega_u} = -\frac{1/R_{CT}C_{CT}}{2\pi GBW}$$

Comparing (2.7) with (2.9) reveals that, as GBW decreases, $\lambda_{DT,\ GBW}$ grows exponentially and $\lambda_{CT,\ GBW}$ grows linearly. Fig. 2.4 shows the settling errors

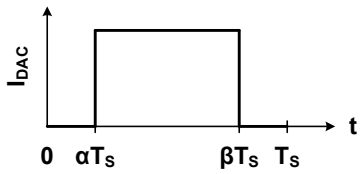

Figure 2.5: Definition of α and β in a current mode DAC.

depending on the finite GBW in both integrators. It is assumed that both integrators have the same gain of 1 and the same sampling frequency. When $\mathrm{GBW_{CT}} = \mathrm{GBW_{DT}} = \mathrm{F_S}$, $\lambda_{CT,\,GBW}$ is 0.137 and $\lambda_{DT,\,GBW}$ is 0.208. Although this comparison depends on a DT integrator feedback factor and a CT integrator coefficient, its tendency for the CT integrator to require less GBW remains unchanged.

2.5 Excess Loop Delay

The CT $\Delta\Sigma$M has a well known problem of excess loop delay [19]. This problem results from additional delay in the feedback paths around a quantizer. As a result, the transfer function of a CT loop filter is not equivalent to that of a DT loop filter. The speed of the feedback is limited by the regeneration time of a latch, DAC switching logic, and opamp delay. This is explained in Section 2.6. Depending on amount of the delay, the order of the $\Delta\Sigma$M may increase, thus causing the modulator to become unstable [19].

To mitigate the problem, the transfer functions of the CT and DT loop filter should match each other. This can be achieved by a impulse-invariant transformation method [19]. The transformation is shown in Table 2.1 and the definition of α and β is demonstrated in Fig. 2.5. When the same impulse is applied to each loop filter, the outputs of each filters should be identical as illustrated in Fig. 2.6.

Table 2.1: Impulse-invariant transformation: s-domain equivalency for z-domain pole. See Fig. 2.5 for α and β.

z-domain pole	s-domain	s-domain when $z_k = 1$
$\frac{1}{z-z_k}$	$\frac{r_o}{s-s_k} \times \frac{1}{z_k^{1-\alpha}-z_k^{1-\beta}}$ $r_0 = s_k$	$\frac{r_o}{s}$ $r_0 = \frac{1}{\beta-\alpha}$
$\frac{1}{(z-z_k)^2}$	$\frac{r_1 s+r_0}{(s-s_k)^2} \times \frac{1}{z_k(z_k^{1-\alpha}-z_k^{1-\beta})^2}$ $r_1 = q_1 s_k + q_0$ $r_0 = q_1 s_k^2$ $q_1 = z_k^{1-\beta}(1-\beta) - z_k^{1-\alpha}(1-\alpha)$ $q_0 = z_k^{1-\alpha} - z_k^{1-\beta}$	$\frac{r_1 s+r_0}{s^2}$ $r_1 = \frac{1}{2}\frac{\alpha+\beta-2}{\beta-\alpha}$ $r_0 = \frac{1}{\beta-\alpha}$

Previous efforts to alleviate the problem are summarized in [19]: Return-to-Zero DAC, coefficient tuning, and direct feedback path. Recent compensation methods are based on the direct feedback compensation technique [20]: analog compensation with dedicated adder [21], digital compensation [22], analog compensation merged in last integrator [9], [23]. Although these techniques effectively compensate the excess loop delay, loop filter synthesis becomes complicated [9]. On the other hand, the DT $\Delta\Sigma$M can easily alleviate the problem. More details are shown in Section 2.7.

2.6 Finite Opamp GBW: Additional Delay

As mentioned briefly in Section 2.4, the finite opamp GBW causes integrator gain error, as shown in Fig. 2.7 (a). Furthermore, the CT integrator has a different

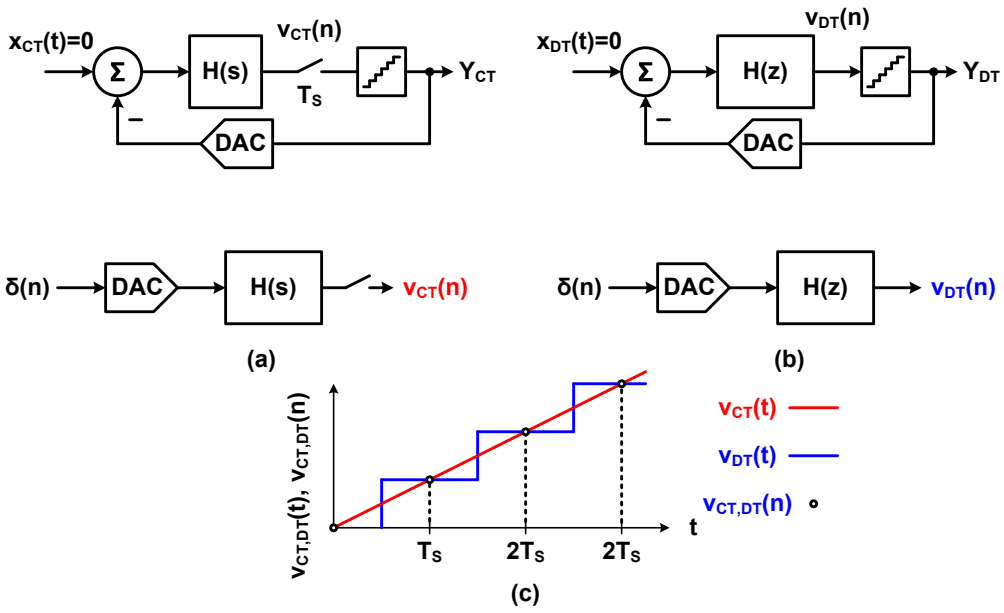

Figure 2.6: Impulse response of open-loop filters: (a) Continuous-time filter (b) Discrete-time filter, and (c) Output waveforms.

phase response as shown in Fig. 2.7 (b). The phase shift can be modeled by (2.10).

$$H_{CT,a}(s) \approx H_{CT,i}(s)\frac{1}{s+\tau_D},\ where\ \tau_D \approx \frac{1}{\omega_u + 1/R_{CT}C_{CT}} \tag{2.10}$$

The phase shift introduces additional delay in time domain, τ_{D}, which makes the loop filter slow. Consequently, it contributes to the excess loop delay. Fig. 2.8 demonstrates the influence of the additional delay in the CT integrator depending on unity-gain radian frequency, ω_{u}. Table 2.2 summarizes the effect of the finite ω_{u}. Notice that the lower ω_{u} is, the longer is the delay. This delay causes additional error at the output of the CT integrators. As an example, when $\omega_u = \frac{1}{\mathrm{T_s}}$, expected output voltage at 4 s (0.5×4) is equal to -2 V but the output actually becomes -2 V at 4.5 s.

Although the additional delay can be considered during the transformation phase, the delay can vary after fabrication. This uncertainty causes a peaking

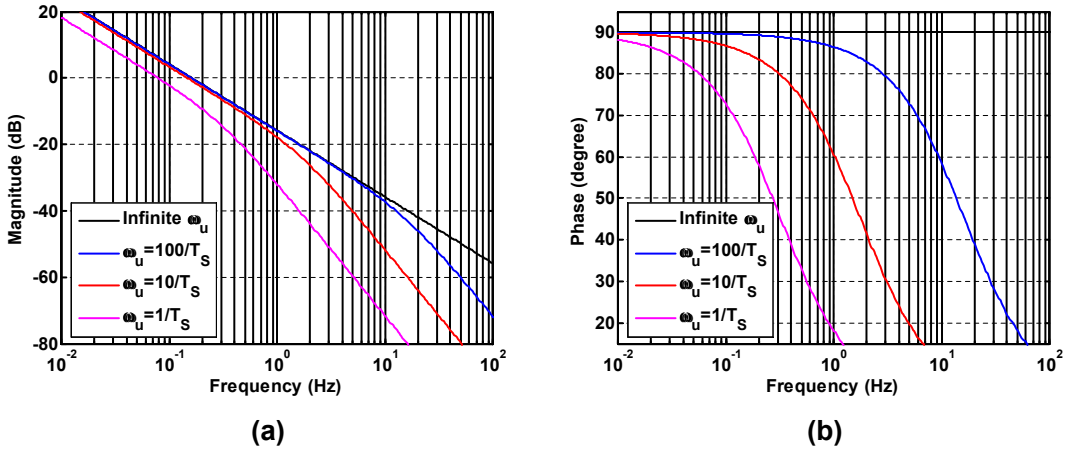

Figure 2.7: Frequency response of CT integrator when finite GBW is included: (a) Magnitude response and (b) Phase response.

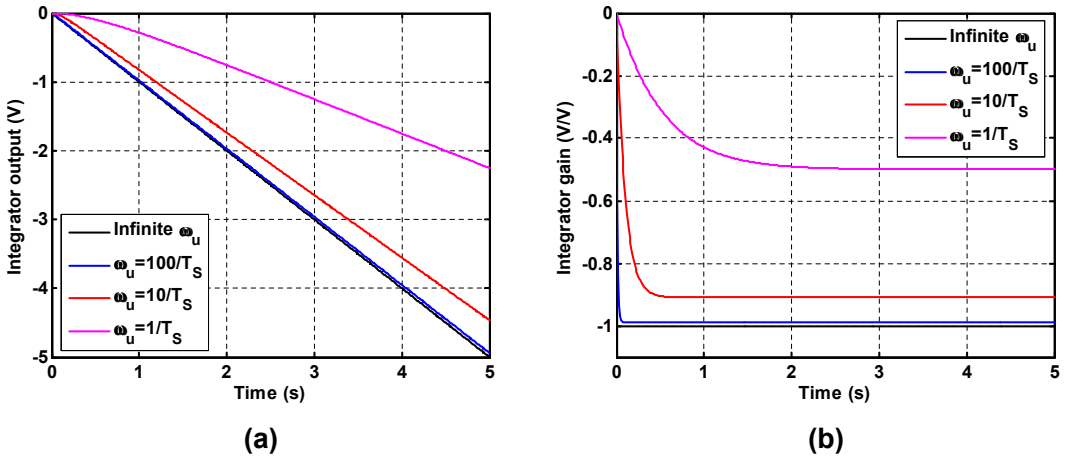

Figure 2.8: Additional delay of CT integrator due to finite opamp GBW: (a) Transient response when unit step applied and (b) Integrator gain variation.

around half the sampling frequency [9], [24], [25]. Depending on the location of the peaking, the out of band gain increases or decreases. As a result, the modulator has a different swing range.

Table 2.2: Influence of finite ω_u on CT integrator.

	Infinite ω_u	$\omega_u = \frac{100}{T_S}$	$\omega_u = \frac{10}{T_S}$	$\omega_u = \frac{1}{T_S}$
Ideal integrator gain(V/s)	1	1	1	1
Actual integrator gain(V/s)	1	0.990	0.909	0.500
Expected output voltage @ 5 s (actual gain (V/s) × 5 s)	5	4.95	4.54	2.50
Actual output voltage @ 5 s	5	4.95	4.46	2.25
Delay (ms)	0	9.9	90.9	500.0

2.7 Delay Allocation

Unlike the CT ΔΣMs, the DT ΔΣMs can easily overcome the excess loop delay problem. As an example, Fig. 2.9 (a) shows a first-order ΔΣM with a full-delay integrator. The full-delay can be split into two half-delays. One of them can be allocated to the integrator and the other to the quantizer as illustrated in Fig. 2.9 (b). Its circuit implementation is shown in Fig. 2.9 (c).

2.8 Anti-aliasing Filtering

Actual sampling of the CT ΔΣM occurs at the quantizer. The nature of the CT integrator offers an inherent low-pass filtering function, as illustrated in Fig. 2.10 (a). This filtering offers an *inherent* Anti-Aliasing Filtering (AAF). In case of the distributed feedback structure [12], the order of AAF is equal to the number of integrators.

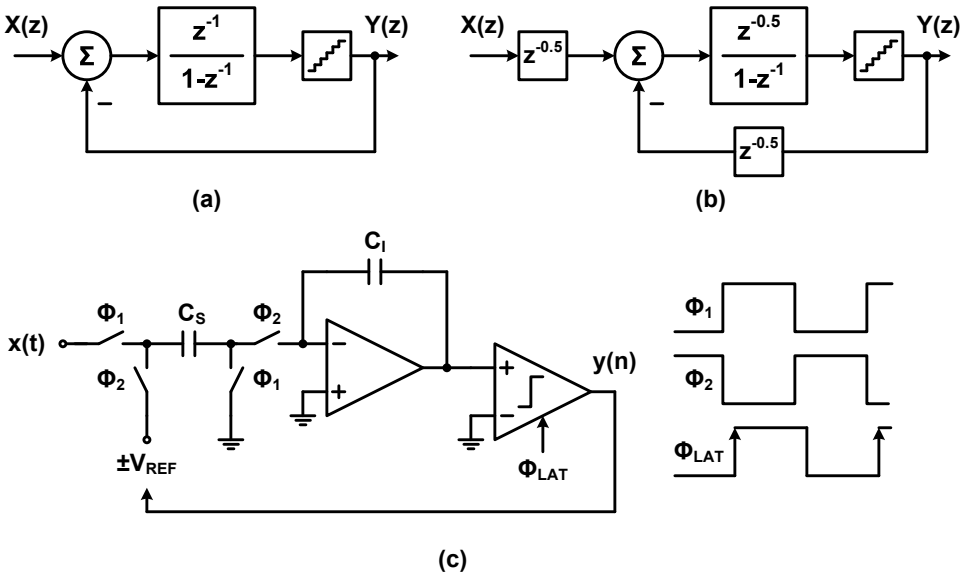

Figure 2.9: Allocation of half-delay in first-order ΔΣM: (a) Full-delay integrator (b) Half-delay integrator and half-delay quantizer, and (c) Circuit implementation of (b).

On the other hand, the DT ΔΣM samples the signal on sampling capacitor, C_S, as shown in 2.9 (c). Moreover, the signal transfer function (STF) of a DT ΔΣM is a form of all pass filter as shown in Fig. 2.10 (b). As a result, any blocker that goes into the modulator corrupts signal conversion, unless an explicit AAF exists in front of the DT ΔΣM.

Although the frequency of the blocker signal varies from system to system, it is worth noting that a feedforward path in the CT ΔΣM diminishes the inherent AAF function since the feedforward path creates a zero in STF. Furthermore, a direct feedforward from the DT modulator input to quantizer input tends to cause out-of-band signal peaking unless carefully designed [26]. The peaking increases the requirement of an AAF to achieve comparable amount of blocker suppression.

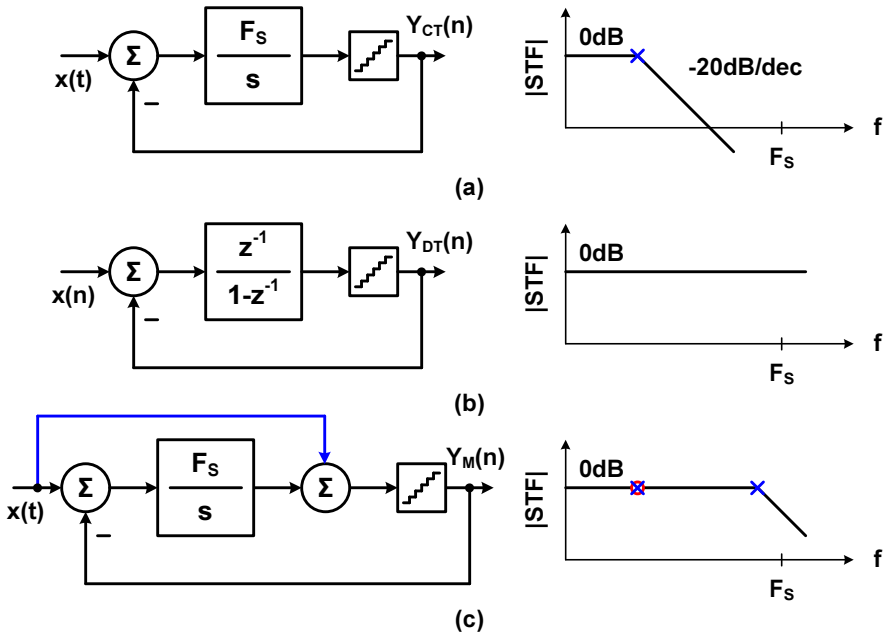

Figure 2.10: Block diagram and signal transfer function magnitude response of: (a) CT ΔΣM (b) DT ΔΣM, and (c) CT ΔΣM with feedforward path.

2.9 Thermal Noise

Practically, thermal noise from resistor/active element is a limiting factor which keeps a ΔΣM from achieving expected Signal to Quantization Noise Ratio (SQNR). This is due to the fact that thermal-noise-limited design helps to save power consumption. This section provides thermal noise limitation of each implementation. The following comparison assumes that resistors are the only noise sources and modulator are implemented in single-ended fashion.

A DT integrator processes thermal noise due to periodic sampling with switch that has a resistance, r_S, as shown in Fig. 2.11 (a). The noise directly appears at the output, Y_{DT}, since the gain of STF is equal to 1, shown in Fig. 2.11 (b). Noise power at Y_{DT} is given by (2.11). (This noise varies depending on opamp

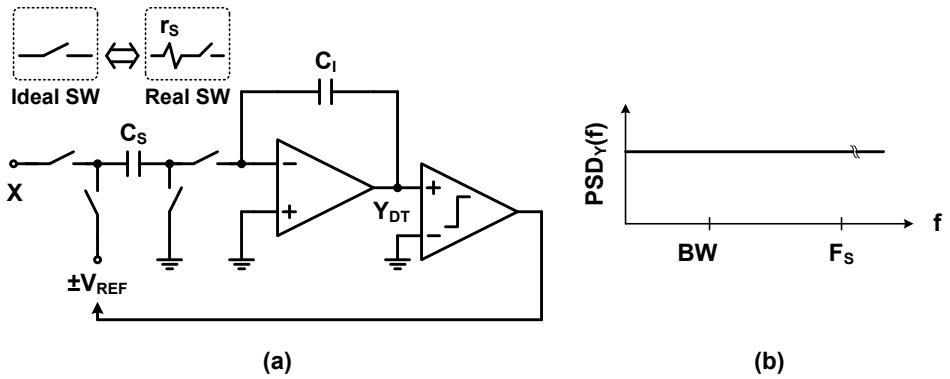

Figure 2.11: First-order DT ΔΣM: (a) Circuit implementation and and (b) Thermal noise power spectral density due to switch resistance, r_S.

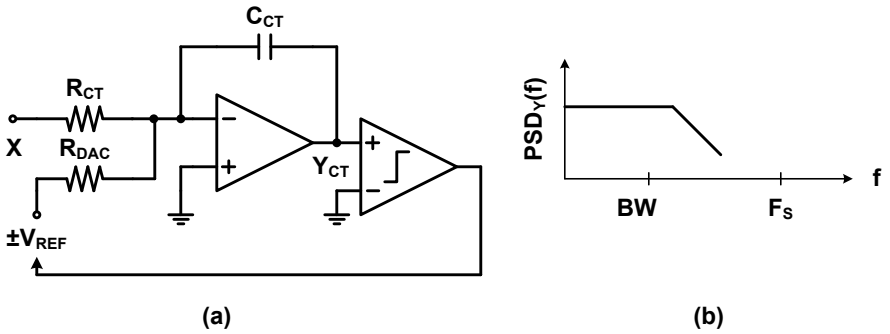

Figure 2.12: First-order CT ΔΣM: (a) Circuit implementation and (b) Thermal noise power spectral density due to resistor, R_{CT}.

transconductance and the resistance [11] but is assumed to be 2kT/C here.)

$$v_{n,DT}^2 \approx \frac{2kT}{C_S}\frac{1}{OSR} \tag{2.11}$$

A CT integrator also has thermal noise from input resistor, R_{CT}, as illustrated in Fig. 2.12 (a). The thermal noise from the resistor is low-pass filtered by the integrator unlike the DT ΔΣM. However, this shaped noise still can be considered as white noise since power spectral density is flat within the bandwidth of interest as shown in Fig. 2.12 (b). As a result, the noise power within the BW can be

described by

$$\begin{aligned} v_{n,CT}^2 &= 4kTR_{CT} \times BW = 4kTR_{CT} \times \frac{F_S}{2OSR} \\ &= 4kTR_{CT} \times \frac{1}{R_{CT}C_{CT}} \times \frac{1}{2OSR},\ if\ 1/R_{CT}C_{CT} = 1/F_S \\ &= \frac{2kT}{C_{CT}}\frac{1}{OSR} \end{aligned} \tag{2.12}$$

Eq. (2.11) and (2.12) can be generalized assuming that input path and feedback path have the same component values. Let $\alpha_{\mathrm{DT}} = \frac{\mathrm{C_S}}{\mathrm{C_I}}$ and $\alpha_{\mathrm{CT}} = \frac{1}{\mathrm{R_{CT}C_{CT}}}\frac{1}{\mathrm{F_S}}$, where α is the gain of each integrator.

$$\begin{aligned} v_{n,DT}^2 &\approx \frac{2kT}{\alpha_{DT}C_I}\frac{1}{OSR} \\ v_{n,CT}^2 &= \frac{2kT}{\alpha_{CT}C_{CT}}\frac{1}{OSR} \end{aligned} \tag{2.13}$$

Note that the CT $\Delta\Sigma$M does not sample any signal at $\mathrm{Y_{CT}}$ before the quantizer. Once sampled by the quantizer, the noise power due to $\mathrm{R_{CT}}$ will decrease depending on the ratio between noise cut-off frequency and sampling frequency [27].

It should be mentioned that the DT integrator shown in Fig. 2.11 can share $\mathrm{C_S}$ for input sampling and feedback DAC operation. On the other hand, the CT modulator cannot share $\mathrm{R_{CT}}$ and $\mathrm{R_{DAC}}$. Thus, the DT $\Delta\Sigma$M with the capacitor sharing scheme can have less noise assuming that the sharing does not introduce significant signal distortion. (Although the concept of distortion is different from that of noise, distortion can be an actual performance limiting factor.)

2.10 Comparison: CT versus DT Implementation

Various properties of the CT and DT $\Delta\Sigma$Ms are reviewed. Comparison results are summarized in Table 2.3, where β is the feedback factor of a DT integrator ($\frac{C_I}{C_S+C_I}$).

Table 2.3: Comparison between continuous-time and discrete-time ΔΣMs.

	CT ΔΣM	DT ΔΣM
Frequency scalability	No	Yes
Time constant variation	±20 %	$< \pm 0.1$ %
DAC clock jitter sensitivity	Poor	Fair
Integrator gain error (GBW)	$-\frac{1/R_{CT}C_{CT}}{2\pi GBW}$	$-\exp\{-\pi\frac{\beta GBW}{F_S}\}$
Integrator gain error (DC gain)	$-\frac{1/R_{CT}C_{CT}}{A_O}$	$-\frac{1}{\beta A_O}$
Integrator phase error	$-\frac{1/R_{CT}C_{CT}}{A_O}$	$-\frac{1}{\beta A_O}$
Integrator delay	$\frac{1}{\omega_u + 1/R_{CT}C_{CT}}$	$z^{-0.5}$ or z^{-1}
Quantizer delay compensation	Required	Not required
Delay allocation	Complicated	Easy
Inherent AAF effect	Yes	No
Thermal noise	$\frac{2kT}{OSR \cdot C_{CT}}$	$\frac{2kT}{OSR \cdot C_S}$

2.11 Multi-Bit DAC Linearization Techniques

In spite of several advantages of a multi-bit quantizer/DAC over a single-bit quantizer/DAC [12], the multi-bit DAC should be linearized to overcom process gradient. Otherwise, it directly degrades modulator performance since it is located at the front-end of the modulator. There are various DAC linearization techniques. This section reviews some of the techniques.

Element Sizing

The simplest linearization technique is increasing element size [28]. Increasing the size reduces random variation, thus improving linearity. Mismatch between DAC element can be calculated by (2.14),

$$\begin{aligned}\frac{\sigma(I_D)}{I_D}[\%] &= \Big[\frac{\sigma^2(\beta)}{\beta} + \frac{4\big\{100\sigma(V_{TH})\big\}^2}{(V_{GS}-V_{TH})^2}\Big]^{0.5} \\ &= \Big[\frac{A_\beta^2}{WL} + \frac{4A_{TH}^2}{WL(V_{GS}-V_{TH})^2}\Big]^{0.5}\end{aligned} \tag{2.14}$$

where β, $\mathrm{V_{TH}}$, $\mathrm{V_{GS}}$, A_β, and $\mathrm{A_{TH}}$ are current factor, transistor threshold voltage, gate-source voltage, current coefficient, and threshold voltage coefficient, respectively. The general rule is that every doubling device size improves linearity by 0.5b. However, matching property is highly sensitive to temperature, voltage and layout pattern. As a result, linearity is limited to around 13b or so [29], [30]. For the case of a current-steering DAC in a submicron process, the accuracy is further compromised by gate leakage current since the device size is so large [31].

Element calibration in analog domain

This method separately measures and tunes each element using analog circuitry [32]. Fig. 2.13 (a) demonstrates a basic principle: during calibration mode (Φ_C), the reference current, $\mathrm{I_{REF}}$ is converted into a voltage and then the voltage is stored on $\mathrm{C_{GS}}$. During normal operation mode ($\overline{\Phi_\mathrm{C}}$), the stored voltage acts as an bias voltage, thus, generating a matched current. However, this requires a frequent update since the gate voltage drops otherwise. Fig. 2.13 (b) shows a solution for the leaky gate voltage. With the help of a successive approximation register (SAR) logic, comparison results are stored in a static storage. In spite of

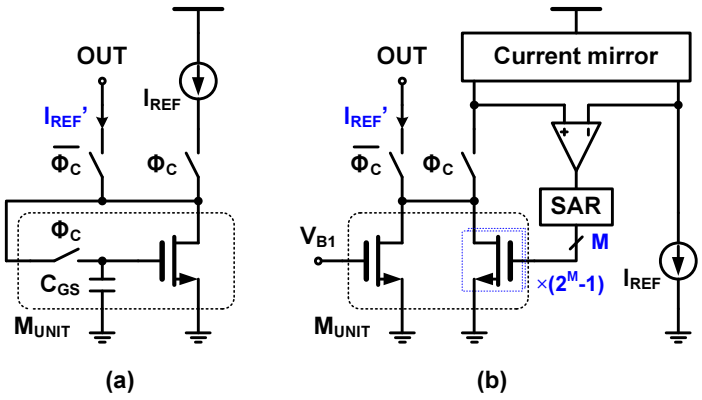

Figure 2.13: DAC calibration techniques in analog domain by using: (a) Transistor gate capacitance and (b) Auxiliary opamp and SAR.

high linearity more than 12b, the method increases power consumption and area due to additional transistor array (blue dotted box), opamp, and SAR logic.

Element Sorting

Sorting technique uses an algorithm: evaluate, sort, sum, re-sort, and arrange (or pick just matched element instead of sum, re-sort, and arrange) [33], [34], [35]. It also reduces random error since this dynamic sequencing is executed after chip fabrication. However, the technique utilizes complex biasing and routing schemes which increases parasitic capacitance. The large parasitic capacitance degrades settling behavior and introduces harmonics at high frequency. Furthermore, massive number of registers is necessary to store the evaluated result, especially when each DAC element is segmented to small size.

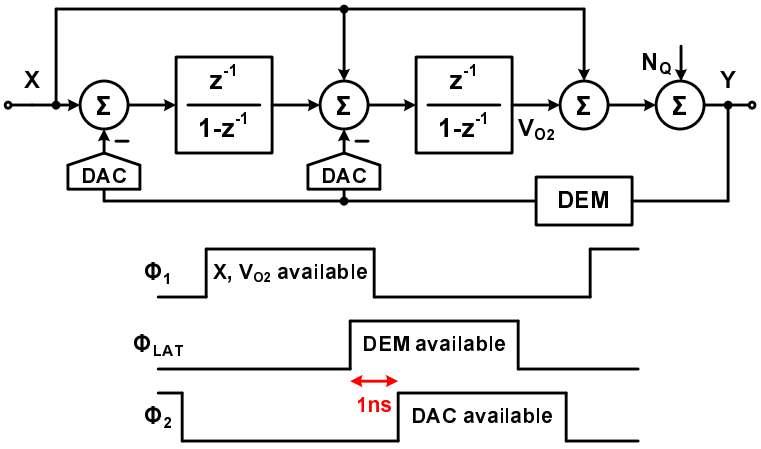

Figure 2.14: Second-order wideband ΔΣM with timing diagram.

Dynamic Element Matching

A Dynamic Element Matching (DEM) has been frequently utilized in ΔΣMs since the nonlinearity from the multi-bit DAC is high-pass filtered. Moreover, it can be easily implemented by using simple digital circuits, such as shifter and adder. As a result, the DEM consumes negligible amount of power while it helps to achieve excellent linearity [36].

However, the DEM increases latency in the DAC feedback path, which can cause instability of the modulator. This is due to the fact that the latency aggravates the excess loop delay as mentioned in Section 2.5. As an example, a data-weighted average technique for a 4b DAC implemented in 0.18 μm CMOS eats up approximately 1 ns [37] in the feedback path. Considering the finite regeneration time of latches and the setup/hold times of flip-flop, the feedback path delay tends to be significant in high-speed operation. This can be demonstrated with the help of Fig. 2.14. Ideally, the DEM should be executed before the DAC operation starts (or during the nonoverlapping phase between Φ_1 and Φ_2), but it

burdens the opamps when the execution takes more time. In other words, the opamps should be much faster to guarantee proper settling during the DAC operation. It should be noted that the CT $\Delta\Sigma$M has the same problem although the DT modulator is shown as an example. Practically, the latency in the CT $\Delta\Sigma$M is more detrimental since it usually operates at much higher sampling frequency.

The DEM latency has became one of the main bottlenecks on implementing $\Delta\Sigma$Ms [38], [39]. The main contribution of this thesis is proposing a novel $\Delta\Sigma$M without the DEM latency problem while the power consumption of the modulator is minimized.

CHAPTER 3. PROPOSED ΔΣ MODULATOR

Hybrid ΔΣ modulator system design is discussed in this chapter. Modulator requirements are specified and a suitable topology is selected to meet the design requirements. A novel Delta-Sigma modulator is proposed to have low latency in the feedback path. To solve the problems of a CT and a DT implementation, a hybrid implementation is presented with a RC time constant tuning scheme. Moreover, processing input signal over a full-scale range is described. MATLAB/Simulink modeling method is also discussed.

3.1 Modulator Specification

As a demonstration vehicle, Wireless Broadband is chosen. Although signal BW of 9 MHz and 12b resolution satisfies its ADC requirement [1], the design specification for this work is further extended to show fast clocking operation. Table 3.1 summarizes the new specifications. Power consumption includes the modulator, and a RC tuning circuit which facilitates operating frequency of CT integrators.

3.2 Modulator Topology

The most difficult task in this design is achieving 20 MHz BW. Table 3.2 shows possible candidates for the target specification by varying modulator order, OverSampling Ratio (OSR), and quantizer resolution. An 87 dB peak Signal-to-

Table 3.1: Modulator target specification.

Bandwidth	20 MHz
SNDR	$>$ 74 dB
Power supply	1.2 V
Design process	65 nm CMOS
Power consumption	$<$ 40 mW

Table 3.2: Possible modulator order, OSR, and quantizer resolution.

Order	2nd	2nd	3rd	3rd	4th	4th
Guaranteed Stability	Yes	Yes	No	No	No	No
Quantizer resolution (bit)	4	5	4	5	4	5
Oversampling ratio	33	25	16	13	11	9
SQNR (dB)	88.3	88.6	88.2	88.2	88.8	87.2
Sampling frequency (MHz)	1032	1000	640	520	440	360

Quantization-Noise Ratio (SQNR) is assumed to account for design margin. SQNR for each case is obtained based on (3.1) assuming a sinusoidal input signal applied

$$\begin{aligned} SQNR\ (dB) &= 10\ log\Big[\frac{0dBFS\ signal\ power}{Quantization\ noise\ power}\Big] \\ &= 10\ log\Big[\frac{3(2k+1)OSR^{2k+1}(2^N-1)^2}{2\pi^{2k}}\Big], \end{aligned} \tag{3.1}$$

where k and N are modulator order and quantizer resolution, respectively.

Remember that improving the resolution of quantizer increases quantizer/DAC design complexity, unless quantization noise truncation and cancellation/suppression are applied [40], [41]. A 4b quantizer is selected since it enhances SQNR with rea-

sonable design complexity.

The order of a modulator influences the stability of the modulator [12]. Pole optimization can be used to decrease the out-of-band gain, hence improving stability, but degrades SQNR. To counteract this degradation, zero optimization can be used [11]. However, this requires well matched passive components with relatively large ratio between a resonator path and integrator path. This is due to the fact that the location of the zero directly impacts SQNR. Moreover, the zero optimization increases in-band noise power due to additional component. Hence, no pole-zero optimization is used in this work.

Another factor that should be considered is clock frequency. Although the second order modulator guarantees stability, clock frequency of over 1GHz brings out another issue of inherent transistor switching speed. The switching speed is determined by the ratio of the transistor transconductance to its gate-source capacitance. The fourth-order modulators are clocked at lower frequency but they are more prone to a quantizer overload problem and may suffer from instability. Consequently, modulator design is based on third-order, 4b quantizer with 640 MHz clocking frequency and OSR of 16.

Once the order, quantizer, and OSR are fixed, a proper structure should be chosen. Among various structures published so far, a digital feedforward structure [42] is selected since this structure can achieve high power efficiency by decreasing the total number of comparators and by reducing internal signal swing at each integrator. Fig. 3.1 (a) shows a linearized block diagram of the chosen modulator topology. Although this modulator is able to reduce the total number of comparators, the output swing of second integrator is relatively large compared to a reference voltage. This is due to the fact that modulator has an STF equal to z^{-3}, instead of a high-pass filter form which introduces STF out-of-band peaking. The

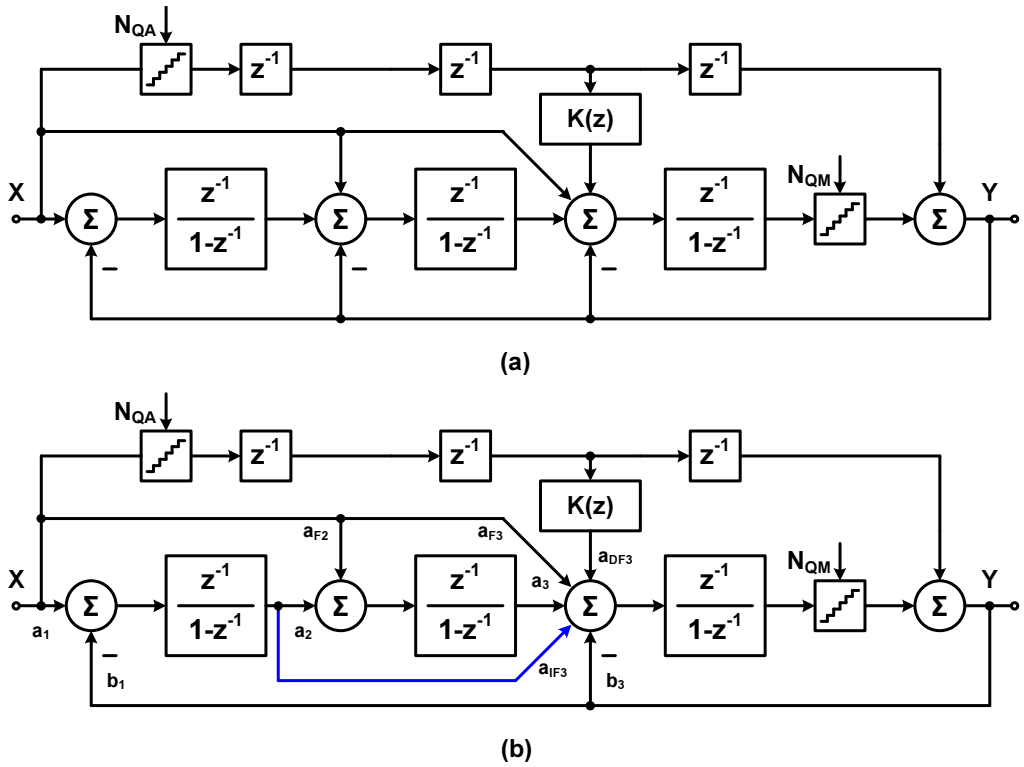

Figure 3.1: Third-order digital feedforward DT ΔΣM: (a) With distributed feedback paths and (b) With internal feedforward path.

wide swing range of the second integrator can be processed by using a two-stage opamp but this mandates more power consumption.

To mitigate the swing requirement, the internal feedforward path, a_{IF3}, is introduced while the second feedback path is removed as illustrated in Fig. 3.1 (b). This topology allows to use a single-stage opamp in the second integrator. Table 3.3 lists the coefficients for a DT prototype. Fig. 3.2 shows SQNR versus input amplitude and histogram of each integrator output when a -1 dBFS sinusoidal signal is applied. As demonstrated, the modulator can process a large signal up to 0 dBFS. This is due to the fact that the auxiliary quantizer, Q_A, quantizes the

Table 3.3: Modulator coefficient summary.

	a_i	b_i	a_{Fi}	a_{DFi}	a_{IFi}
First integrator	1/3	1/3	-	-	-
Second integrator	1	-	-1/3	-	-
Third integrator	3	3	1	-1	9

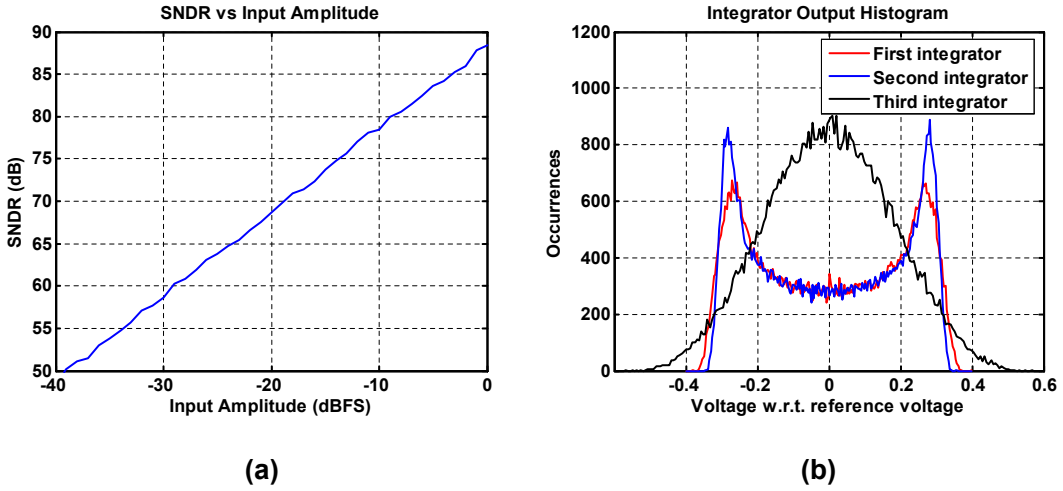

Figure 3.2: Third-order DT $\Delta\Sigma$ modulator: (a) SNDR versus input amplitude and (b) Integrator output histogram when a -1 dBFS sinusoidal signal is applied.

input signal, X, and only the residue of the quantizer is fed into the loop filter. In other words, the loop filter always processes a small signal compared to the reference. As a result, the main quantizer, Q_M, never becomes saturated. This is explained in more detail in Section 3.6.

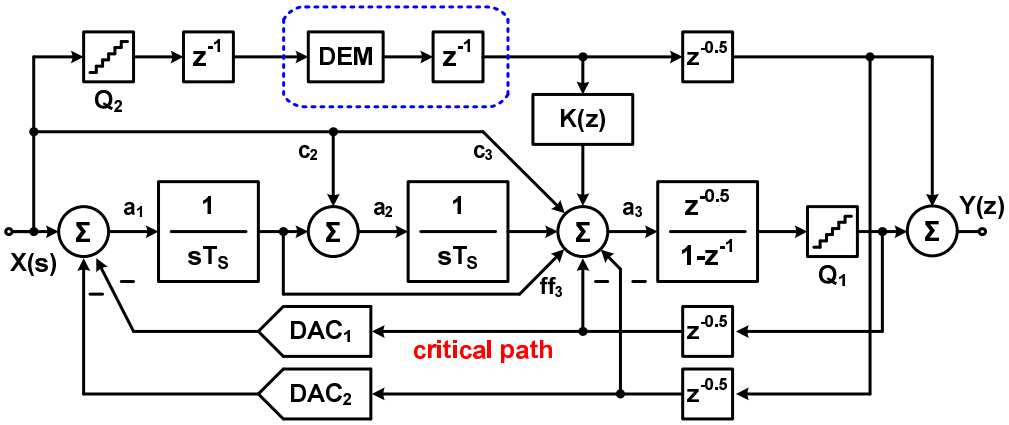

Figure 3.3: Proposed multi-bit 3rd-order hybrid ΔΣ modulator. The dotted line represents the DEM logic including finite gate delay.

3.3 Proposed Modulator

The proposed multi-bit 3rd-order hybrid ΔΣM is illustrated in Fig. 3.3. The proposed modulator is based on [42]. In conventional ΔΣMs, the DEM is inside the feedback path, denoted as *critical path* in Fig. 3.3, which causes extra delay. Instead, the proposed ΔΣM has the DEM in the forward path since the delays in the forward path can be utilized for executing the DEM. The first two integrators are continuous-time (CT) integrators to reduce power consumption and the last integrator is a discrete-time (DT) integrator to alleviate the loop delay and the quantizer timing problem [9], [24]. The main quantizer, Q_1, is effectively a 4b quantizer which uses a 9-level quantizer (+2 dBFS) instead of a 7-level quantizer (0 dBFS). Adding two more comparators enables the proposed modulator to process over full scale signal. Detailed descriptions on each method are explained in the following Sections.

K(z) is a noise cancellation filter [42] and merged with the last DT integrator

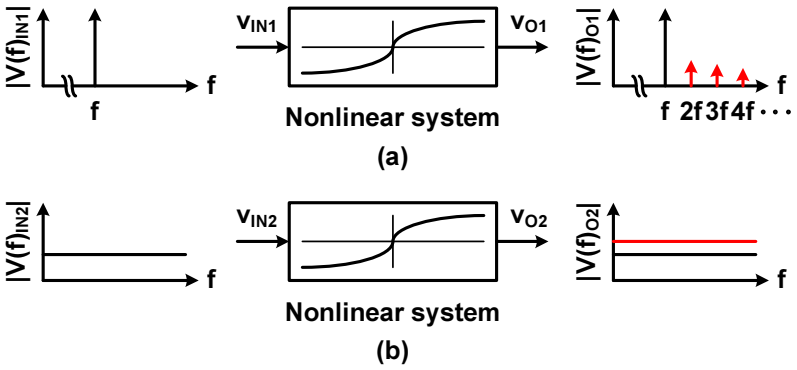

Figure 3.4: Nonlinear system output frequency spectra when (a) single-tone and and (b) random noise is injected.

to relieve digital hardware complexity. The auxiliary quantizer, Q_2, is a 3b, 7-level quantizer. The front-end DACs are switched-mode current-steering DACs. The internal feedforward path, ff_3, is used to reduce the swing of the second integrator and to remove second feedback DACs. Third DACs are implemented by a switched-capacitor DAC.

3.4 Elimination of DEM in Feedback Path

The output of a $\Delta\Sigma$M always contains an input signal plus shaped quantization (random) noise. Fig. 3.4 shows output frequency spectra of a nonlinear block (here, nonlinear DAC) when a single-tone and random noise are applied to the block. Fig. 3.4 (a) can be explained by a simple mathematical equation [43]. Fig. 3.4 (b) can be understood intuitively. Each frequency content introduces its own harmonics as in the single-tone case. However, the harmonics from each content will be spread over the entire BW, since random noise has an almost equal amount of frequency content over a given BW. As a result, random noise just increases the

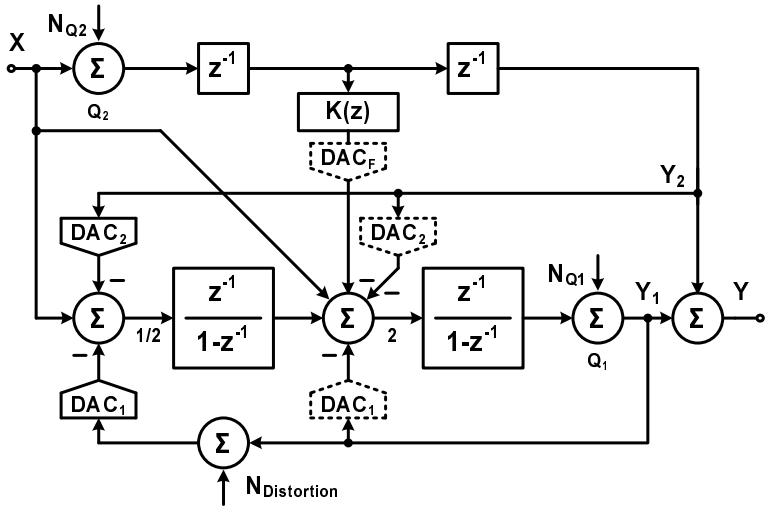

Figure 3.5: Linearized model of a 2nd-order digital feedforward structure with separate DACs.

noise floor when it passes through the nonlinear block instead of creating tones.

For the sake of simplicity, a linearized model of a 2nd-order digital feedforward structure is shown in Fig. 3.5 to demonstrate how the DEM can be eliminated in the critical path. Assume, for now, that Q_2 and DAC_2 are ideal. Each integrator only processes random noise since the input signal, X, and the output of DAC_2, Y_2, cancel each other. Consequently, Y_1 only contains the *random quantization error*. DAC_1 raises noise floor instead of creating harmonics as a low-distortion structure is less susceptible to nonlinear opamp gain [44]. However, the limited resolution of Q_2 and DAC_2 prevents the input signal from being canceled. As a result, Y_1 contains the input signal but the signal power is attenuated as shown in (3.2).

$$Y_1 = (1 - z^{-2})X + z^{-2}N_{Q2} + (1 - z^{-1})^2 N_{Q1} \tag{3.2}$$

Although a 3rd-order modulator is utilized for the actual implementation, the prop-

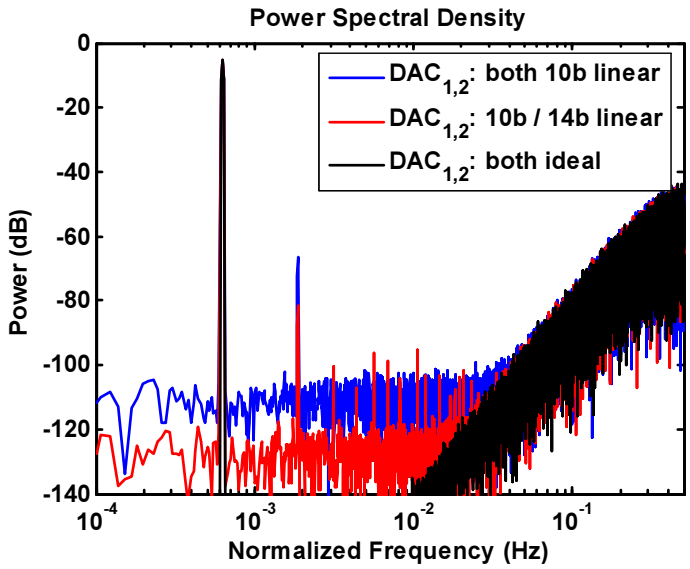

Figure 3.6: Frequency spectra from 3 different types of DACs combinations: (a) $DAC_{1,2}$ are 10b linear (blue dotted), (b) DAC_1 is 10b linear and DAC_2 is 14b linear (red solid), and (c) $DAC_{1,2}$ are ideal (black dashed).

erty shown in (3.2) remains unchanged. System-level simulations are performed and Fig. 3.6 shows frequency spectra with different DAC linearity. A 10b linear DAC is typical and can be achieved without much effort. A 14b DAC can be easily obtained from the 10b DAC by applying the DEM. Case (a) shows a high third harmonic due to 10b linearity from DAC_2. Case (b) has a smaller third harmonic but has multiple high-order harmonics. These high-order harmonics come from the Q_2 since the quantization noise from this quantizer, N_{Q2}, is not fully randomized.

The fact that random noise only raises the noise floor implies that the nonlinear effect due to random noise can be tolerable, since performance of a $\Delta\Sigma$M is often limited by thermal noise and/or DAC clock jitter. Usually SQNR is higher than SNR. The error generated by the nonlinear DAC which processes only quantization noise, affects SNR marginally as long as the increased noise floor is not comparable to thermal noise and/or DAC clock jitter.

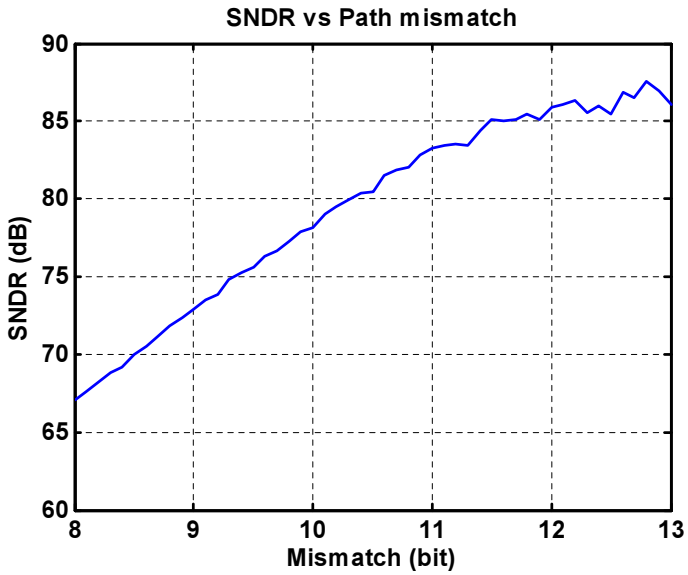

Figure 3.7: SNDR variation due to path mismatch between $DAC_{1,2}$.

Path mismatch between $DAC_{1,2}$ degrades modulator performance owing to the leakage from N_{Q2}. However, a 9-10b path mismatch is sufficient enough to obtain a 12b ENOB as demonstrated in Fig. 3.7. In this simulation, a -2 dBFS input sinusoidal signal is applied, thus maximum SQNR achievable is 87 dB.

3.5 Hybrid Loop Filter Implementation

The DT integrator employs a half-delay for the main quantizer, Q_1, as shown in Fig. 3.8. As a result, the quantizer in the critical path can have relaxed timing (a dedicated half-delay), hence mitigating the excess loop delay problem. The bias current requirement of the integrator is relaxed due to capacitor scaling and linear settling. Furthermore, it eliminates a possible timing problem from the quantizer [24] since the DT integrator output remains constant during latching phase.

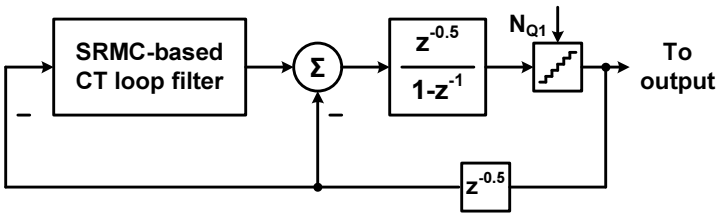

Figure 3.8: Hybrid CT/DT loop filter implementation with a dedicated half-delay for the quantizer.

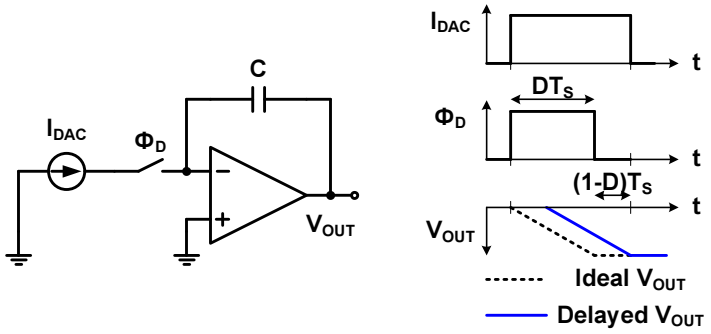

Figure 3.9: SRMC-based CT integrator additional delay absorption.

The first two CT integrators are incorporated with the Switched-R-MOSFET-C scheme (SRMC) to tune the RC time constant [45] and to desensitize them from DAC clock jitter [36], since it is the pulse width variation of the tuning clock that alters the output of the integrators. Furthermore, it enables the integrator to absorb the finite opamp delay as illustrated in Fig. 3.9. Note that the delay results from the finite opamp GBW. Although the finite GBW decreases integrator gain, it is not illustrated in the figure. Assume that a clock duty ratio is D, where D<0.9. The rest of clock period, $(1 - D)T_S$, can be used to buffer the delay.

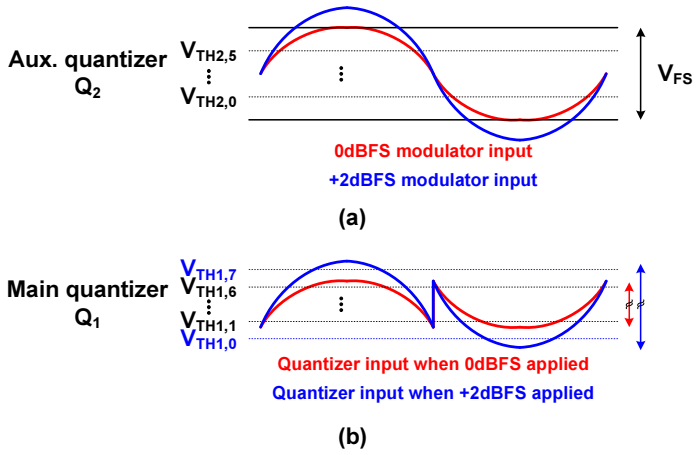

Figure 3.10: Quantizer input waveforms when 0 dBFS and +2 dBFS signals are applied to the proposed modulator: (a) Auxiliary quantizer, Q_2, and (b) Main quantizer, Q_1.

3.6 Over-Full-Scale Input Signal Process

As shown in (3.2), the last integrator mainly processes the quantization errors. This means that the main quantizer, Q_1, is relatively free from the modulator input amplitude. When the modulator input is equal to or less than V_{REF}, shown in Fig. 3.10 (a), the outputs of each integrator are well bounded. This is due to the fact that the auxiliary quantizer, Q_2, chops off the modulator input signal and the loop filter always sees a smaller signal, red solid line, as illustrated in Fig. 3.10 (b). Now, assume a large signal over the full-scale is applied to the modulator. In Fig. 3.10 (a), a +2 dBFS is applied, blue solid line. As long as each integrator and the main quantizer, Q_1, can handle increased swing ranges, the modulator is not overloaded [46], [47].

Various system-level simulations show that, *without* noise transfer function pole optimization, the last integrator swings $\pm 0.5\ V_{REF}$ when a 0 dBFS input signal applied and that the modulator does not show any overload, which would lead to

selecting the 7-level quantizer, corresponding threshold levels from $V_{TH1,1}$ to $V_{TH1,6}$ in Fig. 3.10 (b). Noticing that the first two integrators have smaller swing ranges ($\pm 0.3/0.4$ V_{REF}) than the last one, this margin can be utilized to maximize the modulator power efficiency. Two additional comparators can be used to accommodate an increased swing range for Q_1, thus the 4b-equivalent 9-level quantizer, corresponding threshold levels from $V_{TH1,0}$ to $V_{TH1,7}$, is selected to convert a +2 dBFS input signal. However, further input amplitude increase may cause a reverse diode turn-on when the input amplitude is larger than power supply rails. In this design, the nominal power supply and reference voltages are 1.2 V and 2 V_{PP}, respectively.

3.7 RC Time Constant Tuning Circuit

The time-constant tuning circuitry is an important building block since a CT filter can have a different filter response depending on the time constant. In this design, the SRMC technique is used to tune the time constant [45]. Fig. 3.11 shows a simplified circuit diagram of the tuning circuit. It comprises a master tuning circuit which has a CT/DT integrator, a RC low-pass filter, a voltage-controlled current source (VCCS), and a duty-ratio-controlled pulse generator. The final output, ϕ_{Duty}, is fed to the master circuit as well as a slave circuit, the SRMC-based CT integrators in the loop filter. Detailed operational principle can be found in [45].

Furthermore, the tuning circuitry desensitizes the modulator from the clock jitter coming from an external clock source [36]. The external clock jitter only shifts the starting instance of ϕ_{Duty}. The actual pulse width jitter of ϕ_{Duty} is purely decided by thermal noise and switching noise of the tuning circuitry itself. This can be understood with the help of Fig. 3.12. A solid line represents the

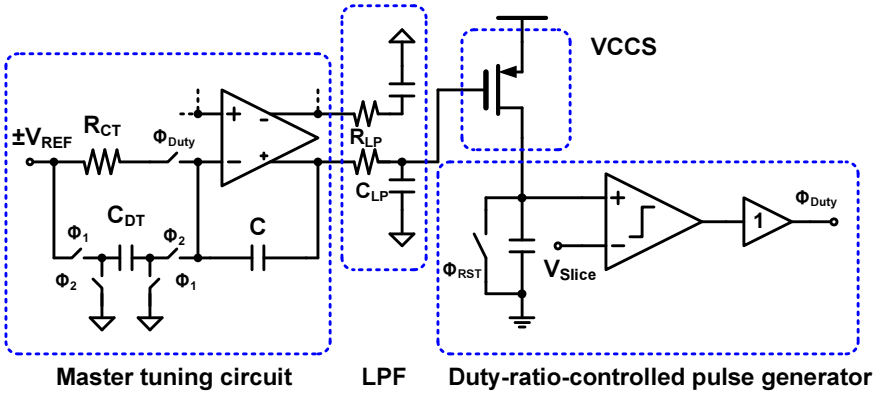

Figure 3.11: RC time constant tuning circuitry.

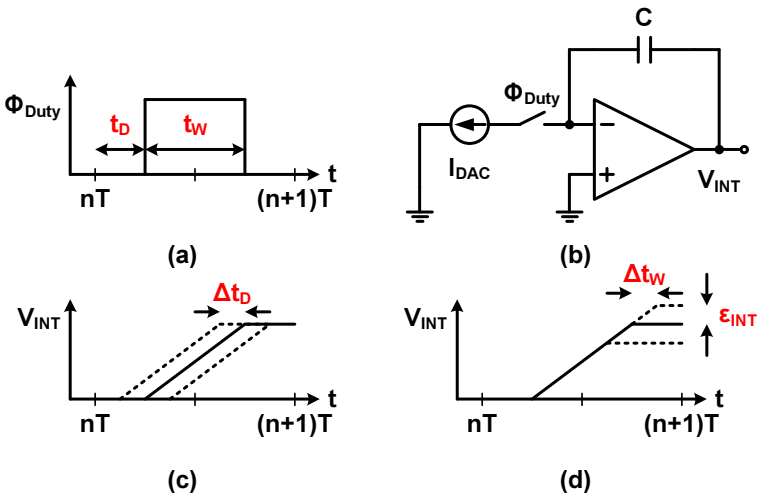

Figure 3.12: Effect of clock jitter on a SRMC-based integrator: (a) Definition of pulse width and delay, (b) SRMC-based integrator diagram, (c) Integrator output depending on pulse delay jitter, and (d) Integrator output depending on pulse width jitter.

integrator output under ideal case (no jitter) and a dotted line for the jitter-influenced output. As shown in Fig. 3.12 (c), the pulse delay jitter only changes the starting instance. As a result, the output value remains the same. However, the pulse width jitter affects the output as shown in Fig. 3.12 (d). The pulse width jitter changes the actual integration time, thus preventing the integrator

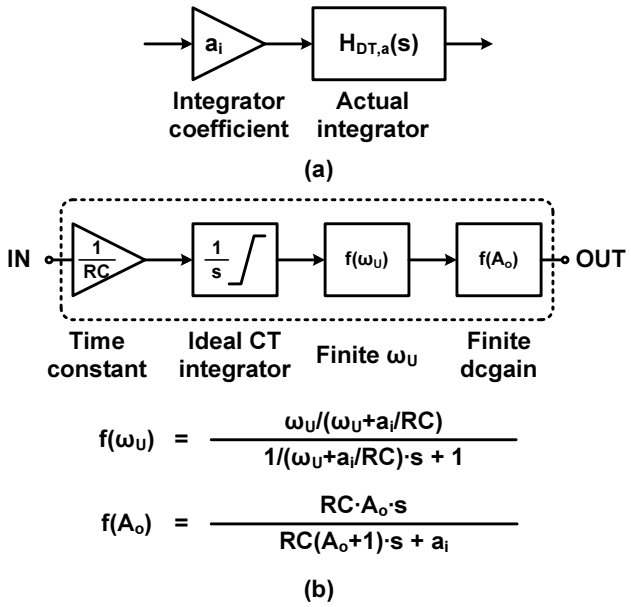

Figure 3.13: CT integrator modeling: (a) Simulink modeling block and (b) Actual CT integrator modeling block.

from having a correct output.

3.8 MATLAB/Simulink Modeling

The properties of the CT and DT integrator have been reviewed in the previous chapter. This section describes how the effects prevalent in the CT integrators can be modeled in MATLAB/Simulink. Modeling method for the DT integrators can be referred to [48]. DAC clock jitter effect is also modeled in this section.

CT Integrator

Fig. 3.13 (a) shows a Simulink block diagram which includes the finite GBW and DC gain effects in actual CT integrators. Fig. 3.13 (b) further illustrates how the actual integrator can be modeled. The gain block is for a given sampling frequency (or time constant). The ideal CT integrator block has a clipping ability to mimic an opamp output swing range available. Following mathematic blocks generate the output value depending on the finite GBW and DC gain.

Note that this modeling has limitations since it is based on linear analysis and assumptions. Especially, opamp nonlinearity modeling needs more attention. Although the opamp nonlinearity can be modeled by using either an arctangent function or a high-order polynomial expansion, such as $x+a_3x^3+a_5x^5\cdots$ assuming that x is the opamp output value, the nonlinearity of a transistor-level opamp may be quite different from the modeled nonlinearity.

DAC Clock Jitter

Fig. 3.14 (a) shows the actual effect caused by jitter and modeled jitter effect. It is difficult add jitter to the Simuilnk pulse generator block since the pulse width cannot be controlled in random manner. Instead, DAC current has a random variation. As long as $\frac{\sigma_{Jitter}}{t_W} = \frac{\Delta I_{DAC}}{I_{DAC}}$, the error charges for both cases equal to each other. Fig. 3.14 (b) demonstrates how the jitter effect is modeled in the block. It receives an ideal DAC value at each sample and the pulse generator creates a fixed pulse width, t_W, with an amplitude of 1. The DAC value is also multiplied by a random number for each sampling period which is produced by

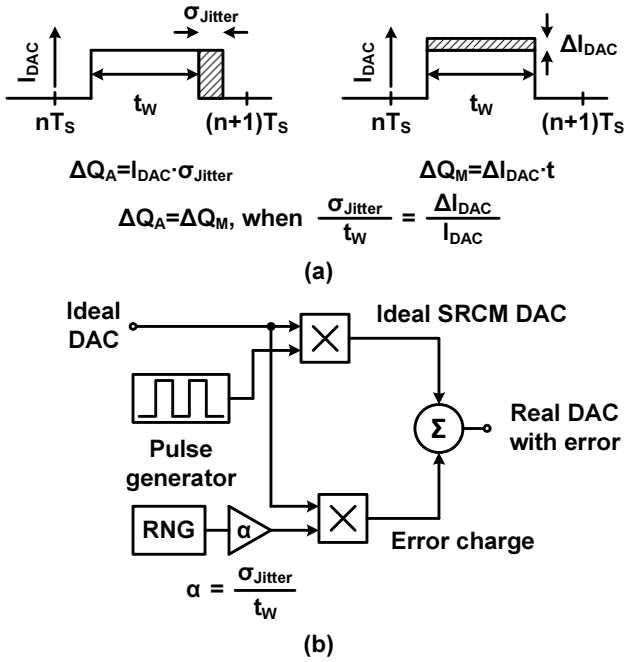

Figure 3.14: DAC clock jitter modeling: (a) Actual jitter effect (left) and modeled jitter effect (right) and (b) Real DAC modeling block.

the random number generator (RNG) followed by a weight, $\frac{\sigma_{\text{Jitter}}}{t_W}$. Two multiplied values are summed together to create a jitter-induced error charge plus the ideal DAC value.

A possible error is integration slope variation. However, this is not problematic since the output of the SRMC-based integrator remains constant once ϕ_{Duty} is off. In other words, this error is negligible since the output is sampled by the following DT integrator where only the final output affects the loop filter response.

CHAPTER 4. CIRCUIT IMPLEMENTATION

Circuit implementation is discussed in this chapter. Simulation results for the building blocks and for the modulator are shown.

4.1 Loop Filter Implementation

Fig. 4.1 shows loop filter implementation. The two CT integrators are active RC integrators to ease the design. The DT integrator shares the input sampling capacitor with the DAC capacitor to save power consumption. The noise cancelation filter, K(z), is merged into the DT integrator. The pulse width of Φ_{CT} can be arbitrary, but the rising edge of the clock must be synchronized with the rising edge of Φ_1. Note that the DEM in the forward path and integrator input common-mode feedback circuits [36] are not shown for simplicity.

To verify the functionality of the proposed modulator, ideal circuit components are used to implement the modulator. Fig. 4.2 shows power spectral density from the *ideal* modulator. SNDR is 86dB when a -3 dBFS sinusoidal signal is applied. Input frequency is 3.125 MHz.

4.2 Opamps

The first opamp requires 30 dB DC gain and 1000 MHz GBW. A single-stage telescopic opamp can be a possible candidate for this purpose since the opamp requires a small signal swing range, moderate DC gain, and large GBW. However,

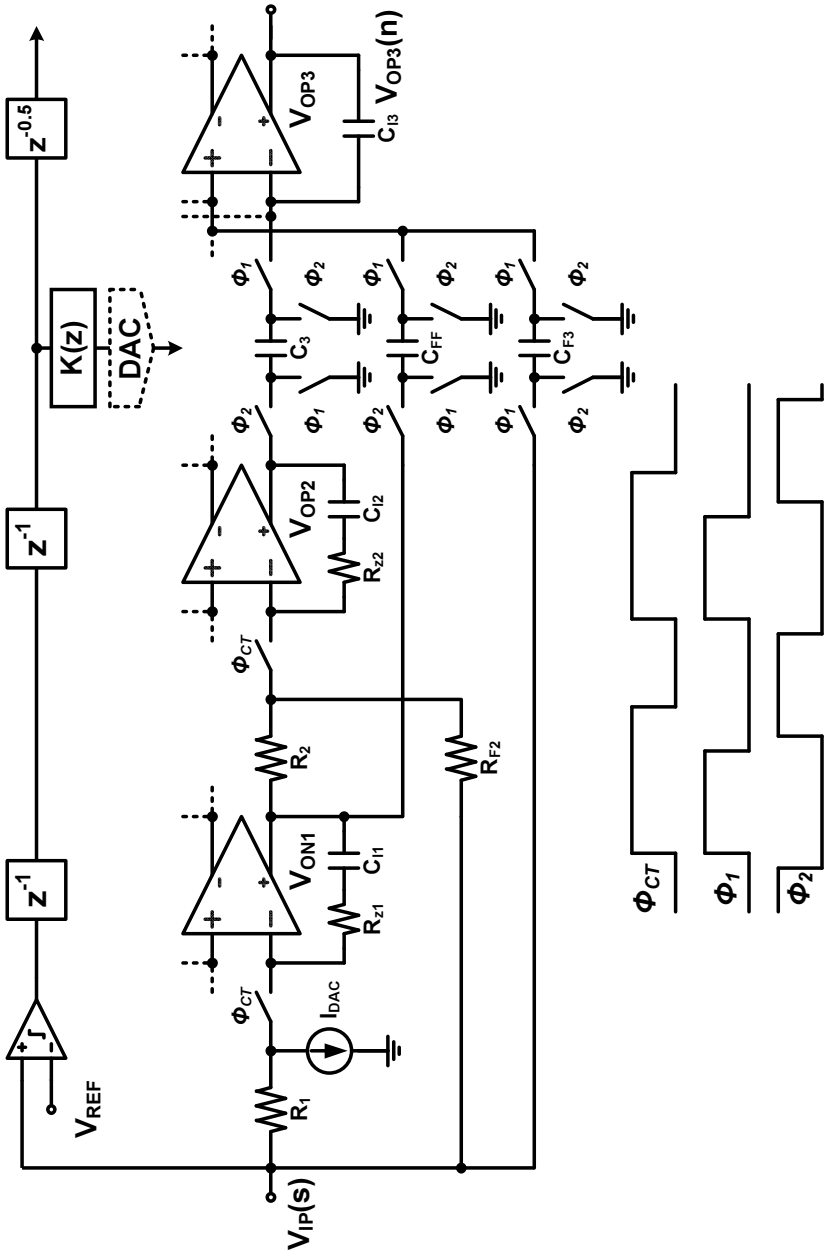

Figure 4.1: Proposed ΔΣM loop filter implementation.

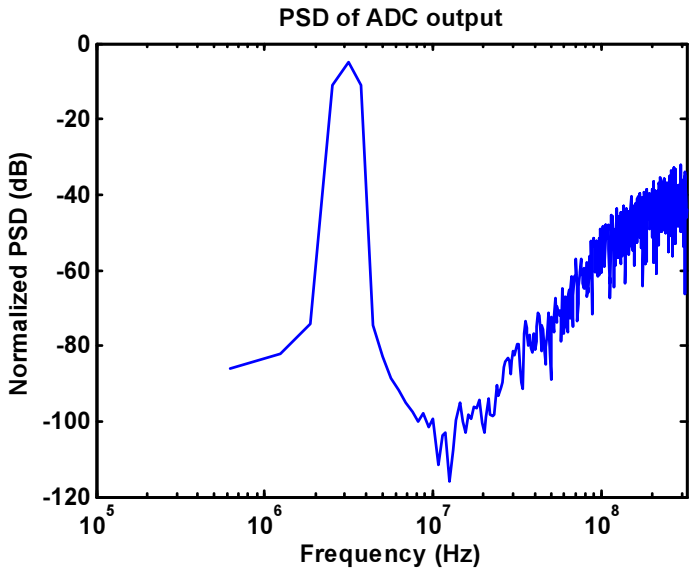

Figure 4.2: Power spectral density using ideal components.

the single-stage opamp may not be able to directly drive the resistor of the second integrator since the resistor may degrade DC gain. When the load resistor is small, the DC gain drops since $A_O = g_m(r_O//R_{2nd})$, where A_O, g_m, r_O, and R_{2nd} are opamp DC gain, transconductance, equivalent output impedance, and the 2nd integrator input resistor, respectively. A two-stage opamp can be utilized to improve DC gain with the resistive loading but this increases power consumption. Fortunately, for a small integrating capacitor, the loading resistor value could be high enough to allow the use of the single-stage opamp. Noise analysis indicates that thermal noise from the second integrator is not a dominant noise source. Thus, the second integrating capacitor is scaled down and the loading resistor value can be increased.

Fig. 4.3 shows the single-stage telescopic opamp with the loading resistor for the first opamp. Note that bias circuitry is not shown for simplicity. To minimize power consumption and thermal noise, a NMOS-input differential pair is used.

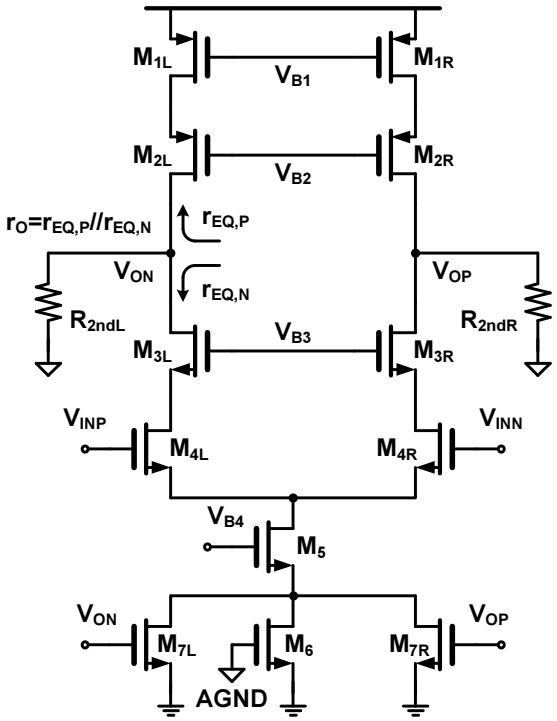

Figure 4.3: Single-stage telescopic opamp for first integrator.

Transistors M_4′s use 5× the minimum channel length to suppress flicker noise and to lower threshold voltage. Transistor pair, M_7′s, is a CT common-mode feedback (CMFB) circuit working in the linear mode. To have a relatively wide linear swing range for the opamp, the output impedance, r_O, is larger than the loading resistor.

The second opamp requires 30 dB DC gain and 700 MHz GBW. The same opamp is used for the second integrator except that the bias current is scaled down. This opamp only drives a capacitive load. As a result, the actual DC gain remains unchanged.

The third opamp requires 40 dB loop gain and 480 MHz loop gain bandwidth. To achieve a relatively high DC gain in a submicron process and a wide swing range, a two-stage gain-boosted telescopic opamp is used, as shown in Fig. 4.4. Note that

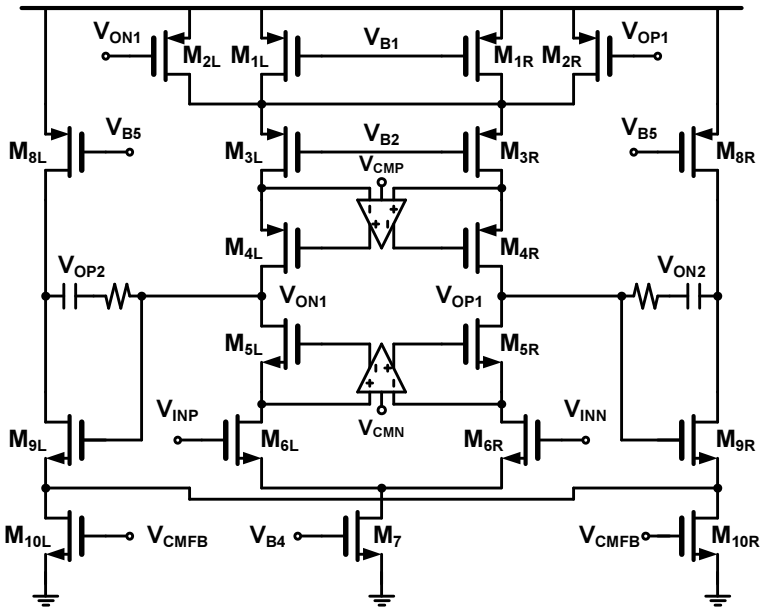

Figure 4.4: Two-stage gain-boosted opamp for third integrator.

the 2nd-stage CMFB opamp and bias circuitry are not shown for simplicity. M_2 pair is a CT CMFB for the first stage. Bias voltages, V_{CMP} and V_{CMN}, control the common-mode input of the gain-boosting opamp, thus the output common-mode voltages are fixed. To save power consumption of the second stage, a NMOS input pair, M_9's, is used with the help of a current source working in the saturation mode, M_{10}'s. This reduces the swing range but system-level simulation confirms that the swing range is wide enough. Although the two-stage opamp is utilized, power consumption is moderate since a low feedback factor (0.1) reduces the effective load capacitance at the output of the second stage, thus helping minimize the bias current in the second stage.

Table 4.1 summarizes opamp performances. The nominal power supply for the process is 1.2 V. For testability purpose, ± 20 % bias current, supply, temperature, and process variation are covered.

Table 4.1: Opamp performance summary.

	DC gain (dB)	BW (MHz)	Input-referred noise (V^2)
First opamp	34	1100	5.85×10^{-11}
Second opamp	39	830	4.76×10^{-10}
Third opamp	83	640	2.01×10^{-7}

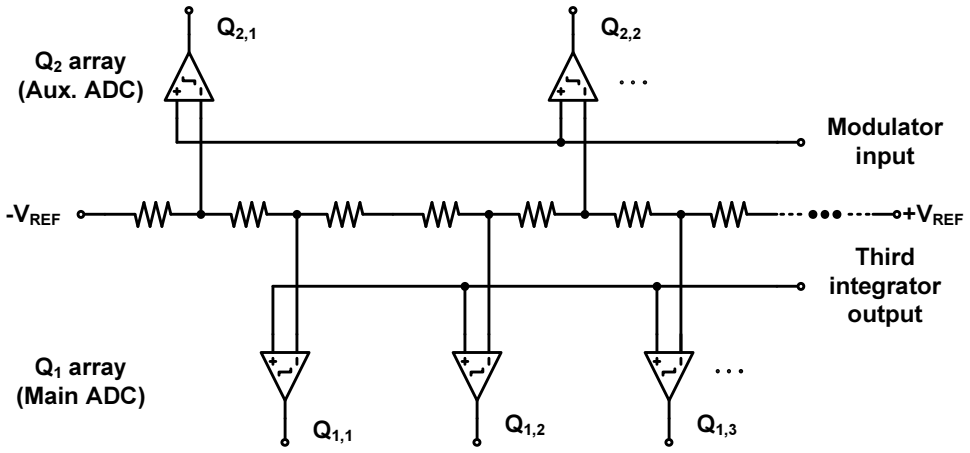

Figure 4.5: Quantizer and resistive ladder configuration.

4.3 Quantizers

Two quantizers (7-level for Q_1 and 9-level for Q_2) share the same resistive ladder to save power and use the same comparator topology as illustrated in Fig. 4.5. Q_1 is repeated by every four resistors and Q_2 by every two resistors. Note that actual implementation is fully-differential. The comparator comprises a static preamplifier and a dynamic latch followed by an SR flip-flop. The SR flip-flop hold the output data for one period, thus eliminating a D-type flip-flop. When a 8 mV_{PP}($\sim$ 0.1 V_{LSB}) step pulse is applied to the comparator, it has a conversion

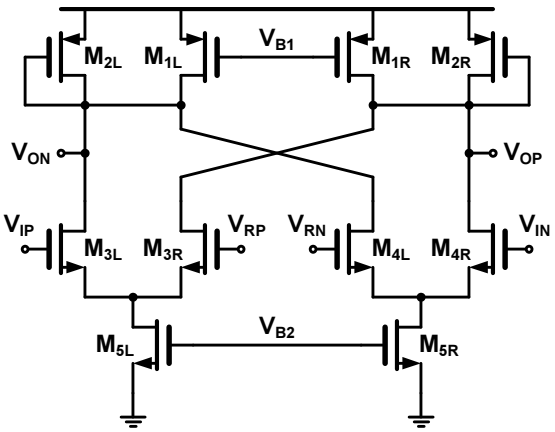

Figure 4.6: Four-input preamplifier.

time of 160 ps in a nominal condition. The worst case conversion time is 500 ps when 1 V, slow-slow, and 125 °C condition is assumed.

The preamplifier is a four-input static low-gain opamp, without an input offset cancelation technique, to minimize the loading of the last integrator. Transistors M_1′s are inserted to improve DC gain ($\sim$ 10 dB) of the preamplifier. This is owing to the fact that $r_O = (r_{O1}//\frac{1}{g_{m2}})$ and that more current flows through M_1. The main purpose of this preamplifier is to minimize a digital kick-back noise coming from the regenerative latch. The input transistors are properly sized to have a 5b matching accuracy and a 5b equivalent input offset voltage to avoid clipping. This is especially important to process over the full-scale range.

4.4 Digital-to-Analog Converters

The cascode current-steering DACs are used for the multi-bit DACs due to their high output impedance. A unit DAC cell is shown in Fig. 4.7 (a). M_1 has a large area (5×15 μm^2) to have more than 10b matching. Monte-Carlo simulations

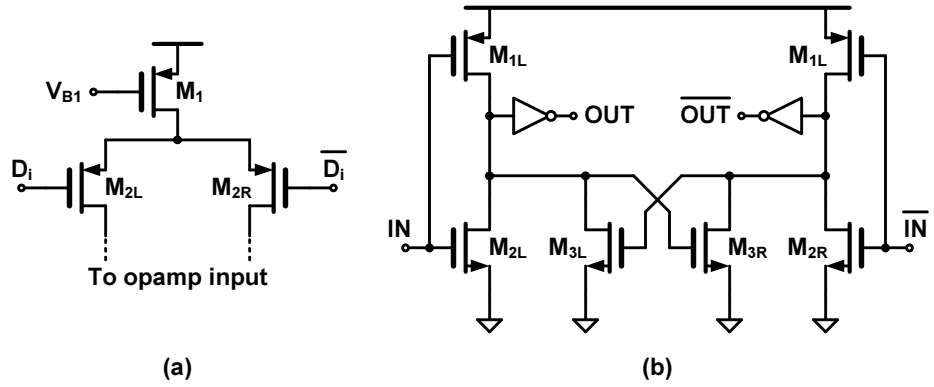

Figure 4.7: Current-steering DAC: (a) DAC Unit cell and (b) DAC driver.

confirm that the DAC has a 10.5b matching accuracy. M_2 pairs also operates in the saturation mode, so that the output impedance of each cell is large enough to reduce DAC nonlinearity. Fig. 4.7 (b) illustrates a DAC driver. This DAC driver outputs, OUT and $\overline{\text{OUT}}$, directly drive the gate of M_2's of the DAC. Different cross-over points of OUT and $\overline{\text{OUT}}$ may introduce nonlinearity [32]. To make the cross-over point tunable, the power supplies of the DAC driver are made tunable externally. Minimizing parasitic capacitance at the source of M_2 pair helps improve linearity. Improvement can be achieved by stacking additional transistor between M_1 and M_2 but this reduces $V_{DS,sat}$ of each transistor. Especially, the reduced voltage headroom forces to increase M_1 area since matching is also related to the headroom.

The DAC_2 unit cell consists of two DAC_1 unit cells since the quantization step of DAC_2 is two times that of DAC_1. Likewise, the width of each DAC_2 driver is two times that of DAC_1 driver.

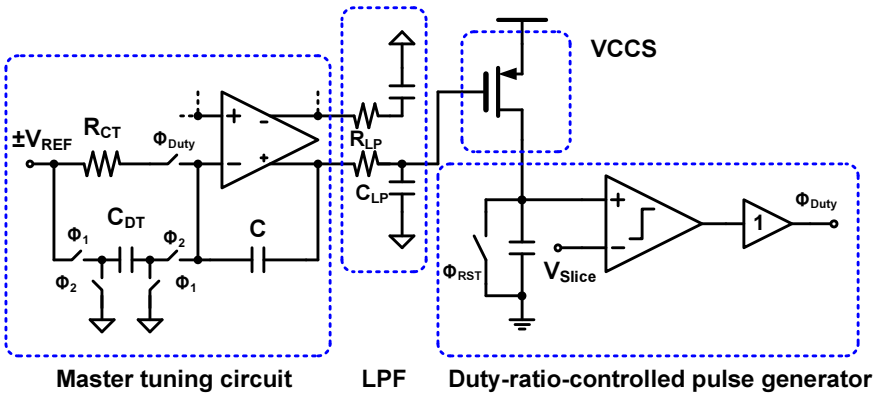

Figure 4.8: RC time constant tuning circuitry.

4.5 RC Time Constant Tuning Circuit

The master tuning circuit, shown in Fig. 4.8 once again for convenience, requires a good opamp since any nonideality in the opamp directly shows up in the duty-controlled clock. A two-stage telescopic opamp is used for this opamp. The CT path is identical to the first integrator and the DT path is designed to operate at half the modulator clocking frequency. The RC low-pass filter has a corner frequency at 12.6 kHz to filter out high frequency contents. A single PMOS transistor is used to implement the voltage-controlled current source. Note that only one of the low-pass filter outputs is fed to the transistor. This is due to the fact that the slicer is already implemented in a single-ended configuration. The slicer is a 5-transistor opamp as shown in Fig. 4.9.

Unlike typical opamp noise analysis where noise from a bias current source is ignored, noise contribution from M_3 should be considered since the gate voltages of M_2's can be different. This is most likely true after fabrication since capacitor and resistor values drift away from their nominal values. To minimize thermal and flicker noise, a large area with a small W/L ratio is selected for M_3. Furthermore,

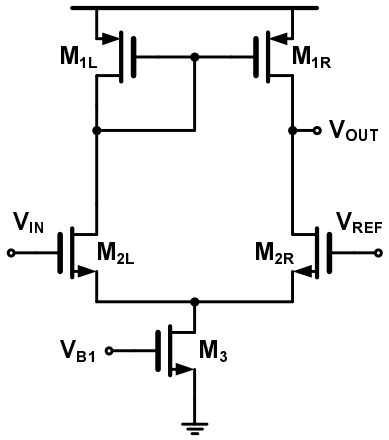

Figure 4.9: Single-ended opamp for slicer.

to reduce noise from a bias circuit, a mirroring ratio between M_3 and a diode-connected transistor (not shown in the figure) is 1:1 and a large MOSCAP is placed between the gate and the source of M_3.

4.6 Digital Blocks

Dynamic Element Matching

The DEM circuit is used for DAC_2, and block diagram for the DEM is shown in Fig. 4.10. The output of the auxiliary quantizer, Q_2, is converted to a binary code to expedite a 3b addition which implements a digital integrator with the help of the feedback. The D-type flip-flop synchronizes the 3b adder outputs and a DEM pointer (ptr) decides where to start [11].

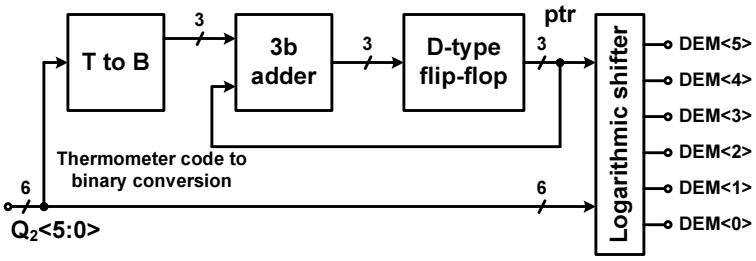

Figure 4.10: Block diagram of dynamic element matching (DEM) circuit.

Interface Circuitry between Modulator and Decimation Filter

A fast clocking frequency mandates a minimum delay between the modulator and a decimation filter. Otherwise, modulator output will be skewed and the final output grabbed by a logic analyzer may end up with missing codes, which raises noise floor. To deal with the fast clocking frequency, an interface circuit uses a quarter clock cycle ($F_S/4$). The quarter clocks (denoted CLK160, CLK160B, CLK160Q, and CLK160QB) can be obtained by using D-type filp-flops as shown in Fig. 4.11. With the help of CLK320 and CLK160, 640 MSPS data are demuxed by four and then each demuxed data are held by the quadrature clock for 1/160 μs. Finally, the 160 MSPS data are synchronized with one of the 160 MHz clock signals. Timing diagram of these process is demonstrated in Fig. 4.12.

Fig. 4.13 illustrates block diagram of the interface circuitry. The 5b adder is implemented in a binary format to save hardware, thereby necessitating a thermometer to binary converter. A 5b adder sums two quantizer outputs. CLK320M and CLK160M creates combinations of 11, 10, 01 and 00, so that 5b 640 MHz data can be demuxed. The final outputs, for example $D_4, P<4:1>$, are synchronized once again (not shown in the figure) and go to I/O drivers. This relaxes logic analyzer timing problem and minimizes substrate coupling generated from the I/O

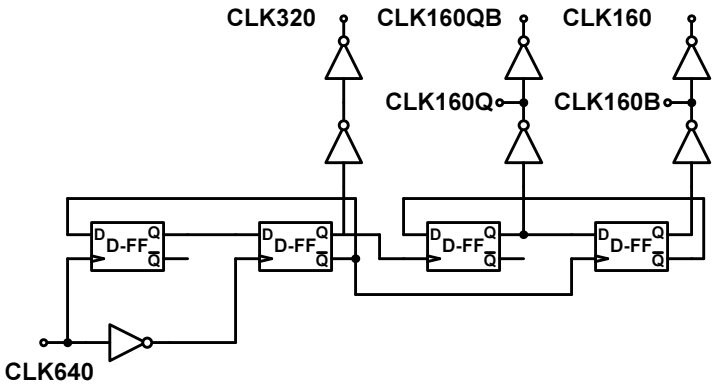

Figure 4.11: Frequency divider and quadrature clock generation circuit.

drivers.

4.7 Modulator Simulation Result

A full circuit-level modulator has been simulated by using the building blocks mentioned before. Fig. 4.14 shows a power spectral density of the modulator. Simulated SQNR, SQNDR, and SFDR is 76 dB, 70 dB, and 77 dB, respectively, when a -4 dBFS sinusoidal input signal at 3.125 MHz is applied. It is strongly believed that harmonics are generated by simulation time-step. Due to a long simulation period, the modulator and the tuning circuitry are run separately. A duty ratio assumed in this simulation is 80 % of T_S, where $T_S = \frac{1}{640\ \mathrm{MHz}}$.

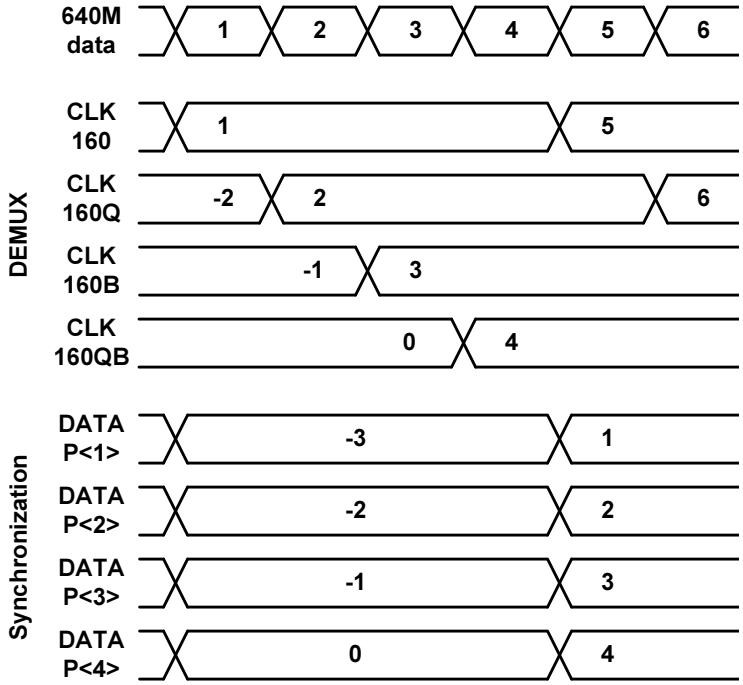

Figure 4.12: Modulator output and demuxed output timing diagram.

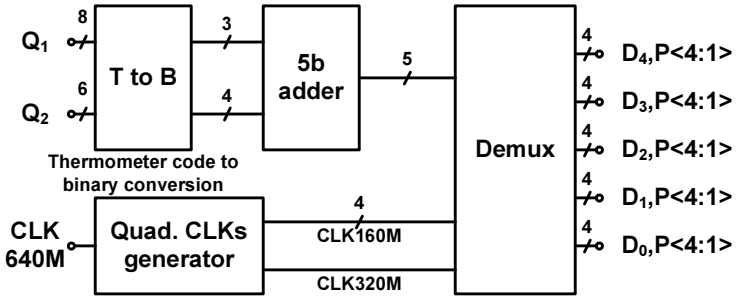

Figure 4.13: Block diagram of interface circuit.

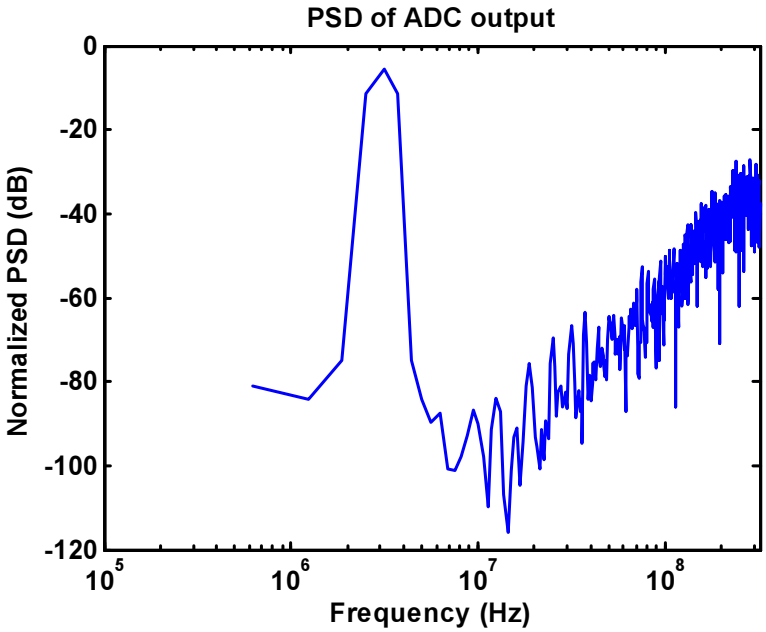

Figure 4.14: Power spectral density using real components.

CHAPTER 5. MEASUREMENT RESULTS

The prototype ADC was fabricated in a 1P6M 65 nm CMOS process. Fig. 5.1 shows the die photo of the prototype IC. The core area excluding I/O drivers and output buffers (i.e., the modulator with the decimation filter) is 0.6 mm^2 (0.97 $\times$ 0.62 mm).

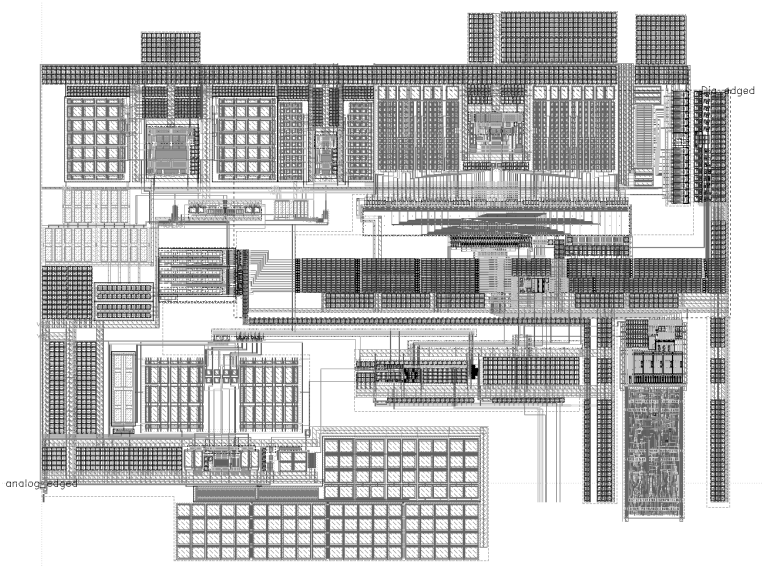

Figure 5.1: Die photo (temporarily replaced with layout).

Sampling Frequency of 100 MHz

First measurement is done at 100 MHz clocking frequency. Fig. 5.2 shows the measured power spectral density of the modulator when a -3 dBFS sinusoidal signal at 29 kHz is applied. A 65536-point FFT is used. Measured SNR, SNDR, and SFDR are 62.7, 63.0, and 82.5 dB, respectively. Fig. 5.3 demonstrated the

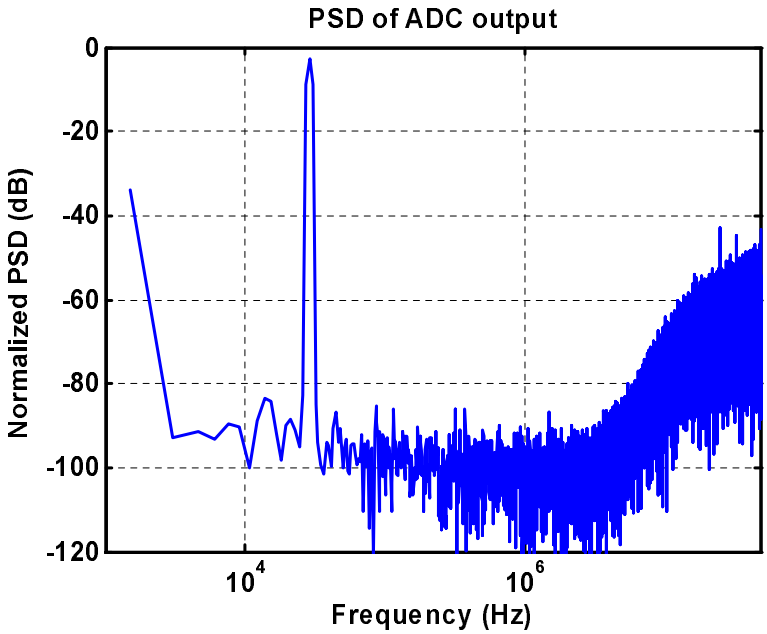

Figure 5.2: Measured output spectrum when F_S at 100 MHz.

measured SNR and SNDR versus input amplitude. The measured peak SNR, SNDR, and SFDR are 64.5 dB, 63.6 dB, and 82.5 dB, respectively. DR is 68 dB. Around -5 dBFS, the SNR starts not to increase linearly with respect to the input amplitude. This is because jitter performance is worse than expected. In fact, it was confirmed that capacitor values reduced by 40 % compared to their nominal values, thus worsening the jitter from the tuning circuit.

The measured performance is summarized in Table. 5.1. BW is 3.125 MHz and OSR is 16. Although analog power supply can be lowered to 1.1 V, digital supply is fixed at 1.2 V. This is due to the sensitivity of the clock receiver circuit to supply voltage variation. Note that digital power consumption includes I/O drivers and the digital portion of the time constant tuning circuit. Analog power consumption also includes the analog portion of the tuning circuit. Based on circuit-level simulation results, the modulator consumes 60 % of the total power.

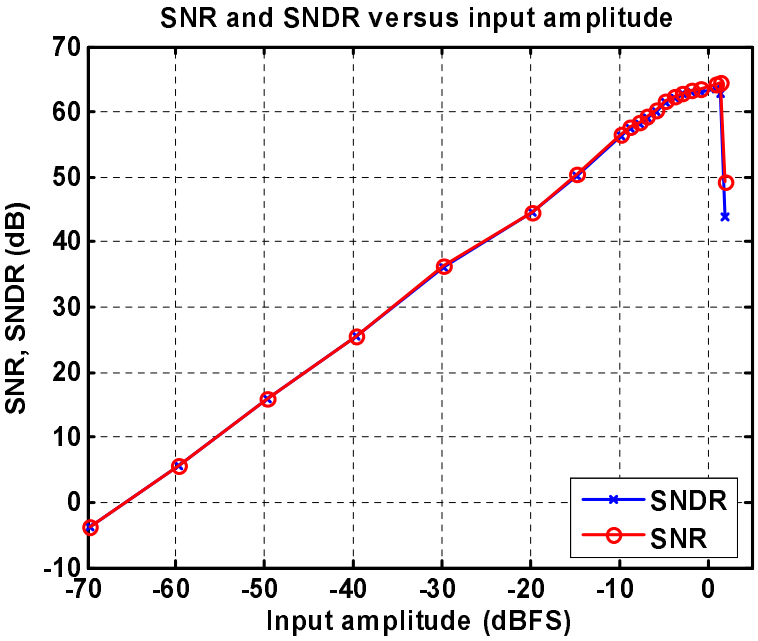

Figure 5.3: Measured SNR and SNDR versus input amplitude when F_S at 100 MHz.

Sampling Frequency of 160 MHz

Second measurement is performed when F_S is at 160 MHz. Fig. 5.4 shows the measured SNR and SNDR versus input amplitude. Peak SNR, SNDR, and SFDR are 63.0 dB, 60.9 dB, 76.0 dB, respectively. DR is 67 dB. Compared to the F_S of 100 MHz, both SNR and SNDR drop by 2-3 dB. This is mainly due to harmonics as shown in Fig. 5.5. A -3 dBFS sinusoidal input signal at 31.8 kHz is applied. The measured SNR, SNDR, and SFDR for the -3 dBFS input are 60.6 dB, 60.3 dB, and 76.0 dB, respectively. Table 5.2 summarizes the measured performance.

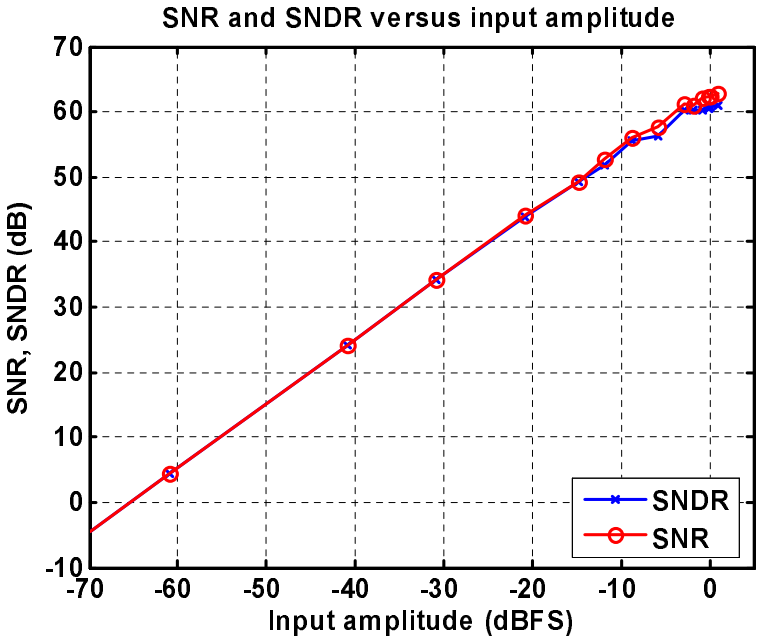

Figure 5.4: Measured SNR and SNDR versus input amplitude when F_S at 160 MHz.

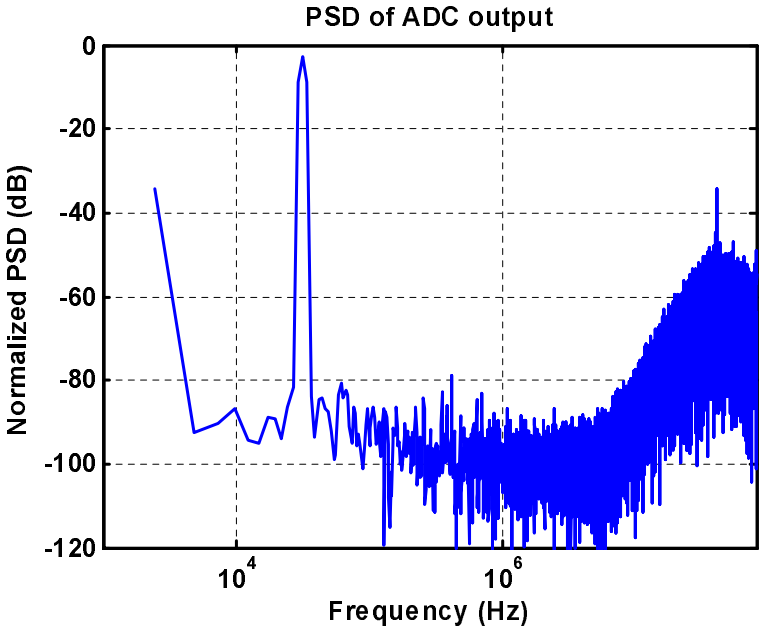

Figure 5.5: Measured output spectrum when F_S at 160 MHz.

Table 5.1: Performance summary of $\Delta\Sigma$ ADC, F_S at 100 MHz.

Sampling frequency	100 MHz
Bandwidth	3.125 MHz
Peak SNR/SNDR/SFDR F_{IN} @ 29 kHz	65 dB/64 dB/83 dB
DR	68 dB
Process	1P6M 65 nm CMOS
Power supply	1.1 V(A), 1.2 V(D)
Power consumption	8.1 mW(A), 2.9 mW(D)
Area	0.6 mm^2 (0.97×0.62 mm)

Sampling frequency of 640 MHz and 800 MHz

Further measurements have been taken at higher sampling frequencies. Fig. 5.6 show the measured spectral densities for the decimation filter outputs. Fig. 5.6 (a) and (b) are measured when F_S are 640 MHz and 800 MHz, (20 MHz and 25 MHz BW) respectively. When a -3 dBFS sinusoidal signal is applied, 49 dB SNDR and 55 dB SNR are measured at 640 MHz sampling frequency. The frequency of the input signal is 107.4 kHz. For 800 MHz sampling frequency, the measured SNDR and SNR are 45 dB and 50 dB, respectively. The frequency of the input signal is 134.3 kHz.

Compared to the previous two cases, higher noise floor and higher harmonics can be observed. It seems that the higher noise floor is due to supply noise and the higher harmonics are due to the DAC switching.

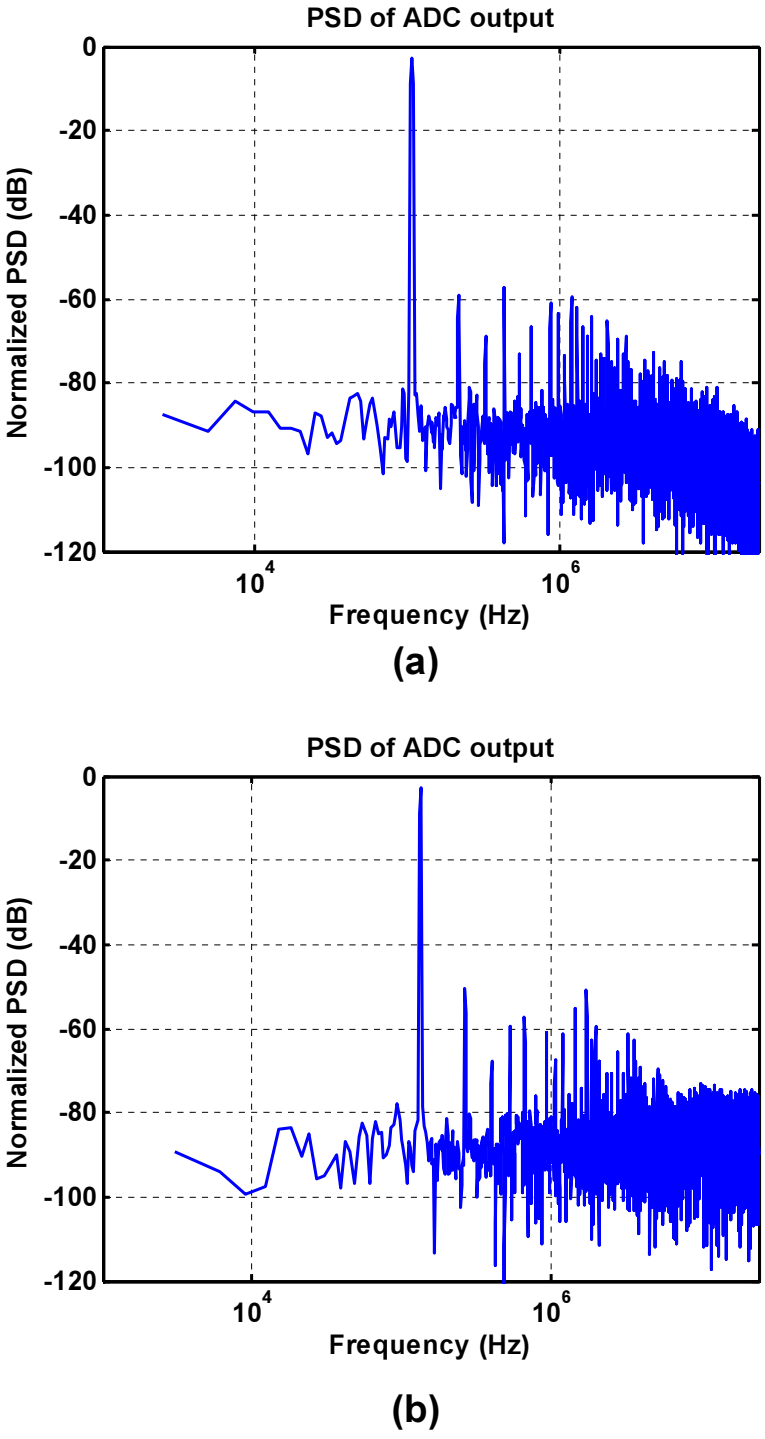

Figure 5.6: Measured decimated output spectrum when F_S is at: (a) 640 MHz and (b) 800 MHz.

Table 5.2: Performance summary of $\Delta\Sigma$ ADC, F_S at 160 MHz.

Sampling frequency	160 MHz
Bandwidth	5 MHz
Peak SNR/SNDR/SFDR F_{IN} @ 31.7 kHz	63 dB/61 dB/76 dB
DR	67 dB
Power supply	1.1 V(A), 1.2 V(D)
Power consumption	8.1 mW(A), 2.9 mW(D)

CHAPTER 6. CONCLUSION

A new multi-bit hybrid $\Delta\Sigma$ modulator is presented. Eliminating the feedback DEM allows minimizing the excess loop delay which corrupts loop filter response. This makes the modulator well suited for high-speed operation since the feedback path has less latency. The combined benefits of continuous/discrete time implementation with the switched-R-MOSFET-C technique help to reduce power consumption and to further mitigate the excess loop delay problem. The digital feedforward structure enables the modulator to process input signals over the full-scale range without any quantizer overload. This makes the modulator power-efficient.

A prototype modulator is implemented in a 1P6M 65 nm CMOS process. When BW is 3.125 MHz and F_S is 100 MHz, the modulator achieves a peak SNR, SNDR, SFDR, and DR of 65 dB, 64 dB, 82 dB, and 68 dB, respectively. When BW is 5 MHz, measured peak SNR/SNDR/SFDR are 63 dB/61 dB/72 dB with a DR of 67 dB at 160 MHz sampling frequency. The prototype IC implementation demonstrates a 11 mW 11b ENOB 14b linear 3.125 MHz BW $\Delta\Sigma$ ADC and the efficacy of the proposed ideas.

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