



## AN ABSTRACT OF THE DISSERTATION OF

Vikas S. Shilimkar for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on January 3, 2014.

Title: Enabling Metal-Fill-Aware Design of Integrated Circuits

Abstract approved: \_\_\_\_\_

Andreas Weisshaar

In advanced integrated circuit (IC) processes, the metal fill inserted to meet foundry imposed density requirements degrades the performance of interconnects and passive components which ultimately affects the overall circuit performance. Accounting for this degradation through electromagnetic and equivalent circuit modeling is becoming a critical aspect of IC design. However, electromagnetic simulation of interconnects and passive components including metal fill quickly becomes prohibitive due to the large problem complexity while the modeling methods in the literature are limited in accuracy and ignore important effects.

This thesis investigates fast and scalable modeling methods for interconnects and spiral inductors in the presence of metal fill. We demonstrate a novel three dimensional problem reduction approach to model the parasitic capacitance due to metal fill in multi-conductor interconnects. Further, we demonstrate a unique technique for modeling metal fill in spiral inductors. We present a systematic on-wafer measurement characterization approach for model verification.

Ultimately, the research presented in this thesis will enable efficient metal-fill-aware design of integrated circuits through fast and accurate models for interconnects and passive components in the presence of metal fill.

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# Enabling Metal-Fill-Aware Design of Integrated Circuits

by

Vikas S. Shilimkar

A DISSERTATION

submitted to

Oregon State University

in partial fulfillment of  
the requirements for the  
degree of

Doctor of Philosophy

Presented January 3, 2014  
Commencement June 2014

Doctor of Philosophy dissertation of Vikas S. Shilimkar presented on January 3, 2014.

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I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

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Vikas S. Shilimkar, Author

## ACKNOWLEDGEMENTS

The completion of this thesis was a team effort at school and at home. I would like to take this opportunity to acknowledge the support from many people and organizations.

The largest contribution to the success of this work goes to my advisor, Dr. Andreas Weisshaar. He provided the freedom to pursue my ideas and own the research project. This was a great training to become an independent researcher. He provided the much needed encouragement during the tough times. I thank him for teaching me the quality, discipline, and rigor required in research. I enjoyed several classes he taught which formed a strong base for my graduate research as well as future industry career. I thank him for being patient. I greatly appreciate the continuous financial support during my graduate life. Even during his absence while serving at the National Science Foundation, he was very diligent in being available for research discussions, thus teaching me commitment to research work by example.

I want to thank Profs. Karti Mayaram, Patrick Chiang, Albercht Jander, and Alan Wang for being on my program committee. They always provided a constructive criticism which helped me improve some aspects of the thesis. I thank Prof. Wade Marcum for serving as graduate committee representative for my preliminary and final examinations. I also thank Prof. Mayaram for teaching interesting circuits classes. The work done during the final project of his RFIC class became part of this thesis. Prof. Albercht Jander provided access to Applied Magnetics Lab, which was a great help during the measurement phase of this work.

I want to thank financial support from center for design of analog-digital integrated circuits (CDADIC) for this research project. CDADIC member companies provided a very valuable feedback on the research direction and the relevance of this work. The engineers and scientists from the member companies contributed through technical discussions. This includes Daryl Carbonari, Richard Soenneker, and Dr. Rodrigo Carrillo-Ramirez from Analog Devices Inc., Dr. Arjun Karroy from TowerJazz Semiconductors (formerly Jazz Semiconductors). I want to thank Dr. Karroy for his timely help during my chip tapeouts and discussions on the technical relevance of this work. Dr. David Yeh from the Semiconductor Research Corporation (SRC) always encouraged this research and encouraged for papers in SRC Techcon conference. Special thanks to scientists

and engineers from Intel who contributed to my understanding of the problem at deep sub-micron process nodes, this includes Dr. Telesphor Kamgaing, Dr. Jad Rizk, Dr. Jonathan Jensen, and Dr. Ritochit Chakraborty.

The measurement characterization part of this thesis received a partial support from IEEE MTT-ARFTG society in the form of a student fellowship. I thank Dr. Leonard Hayden from Teldyne LeCroy (formerly with Cascade Microtech) for his help with measurements, for teaching me the principles of on-chip measurements, and his mentorship throughout my graduate school. I would like to thank Dr. Dylan Williams from the National Institute of Standards and Technology for his guidance on the on-chip calibration standard design for VNA calibration. He pointed out the importance of metal fill consideration for on-chip calibration structures, this topic became a part of this thesis.

Next I want to thank Steven Gaskill for his friendship over the years. Thanks for listening to my ideas and providing critical feedback on my work. I also thank him for providing the eddy-current loss calculations code. I want to thank lab mates Lei Zheng and Dyuti Sengupta, and classmates Ram Ravichandran, Hariprasath Venkatram, Ankur Guharoy, and Amr Elshazly for their friendship. Also thanks to Jayesh Iyer for his guidance over the years.

A large portion of credits also go to my family for their unconditional love and support throughout the graduate school. I want to thank my mother for teaching me the importance of hard work and people skills, and my father for discipline and persuasiveness. Without their encouragement to higher education, I would not be here. Next I want to thank my brother and sister for their love and support. I also thank my extended family for their patience during the time of PhD education.

Finally, special thanks go to my wife and daughter for their incredible support and unconditional love, especially during the toughest times in the graduate school. Thanks to my daughter for being a stress reliever machine and for being a source of inspiration. Thanks to my lovely wife for a great support during this graduate school journey. Thank god for blessings.

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*To my family*

## Chapter 1: Introduction to Metal Fill in Integrated Circuits

Wireless connectivity, power efficiency, and cost are important aspects of electronic system design. Wireless (data and power) connectivity is becoming a crucial part of many consumer and medical electronic systems. At the same time, power efficient electronics play a key role from the environmental standpoint. The predominantly cost driven semiconductor manufacturing industry is consistently pursuing cost-effective small form factor integrated circuit (IC) designs. This effort leads to three-dimensional (3D) integration of circuits and components. This integration is achieved through multi-domain circuit blocks on the same chip as well as through vertical stacking. This integration brings many system level trade-offs. One of the major trade-offs during this compact design is the choice between on-chip vs. off-chip high quality passive components. The integration of passive components on an IC faces the following challenges:

- Typical digital circuits require a highly doped semi-conducting substrate to reduce the potential drop across the chip. On the other hand, for RF/mixed-signal circuit applications, noise coupling through the substrate is a major concern, and therefore, a lightly doped substrate is preferred. For a mixed-signal IC, this leads to a trade-off in the doping concentration of the substrate. Therefore RF circuits need to be designed on a process that has higher doping than a typical dedicated RF semiconductor manufacturing process. The higher conductivity of the semi-conducting substrate leads to challenges in passive component integration as the quality of passive components is degraded due to the power dissipated in the substrate. Therefore to achieve a better performance, design modifications such as a patterned ground shield [1] are desired.
- The size of passive components is a major concern in the integration. Typically the size of such components is wavelength dependent, and therefore, a larger size is required for circuits operating at the lower spectrum of radio frequencies. This leads to an increase in the chip size and consequently the cost per wafer. To address this challenge, slow-wave structures [2] are realized with a compromise on

the quality factor of the components.

- The time required for the design phase of ICs is one of the factors that determine the time-to-market for a product. This time is determined by the availability of computationally efficient models for component design. As the accurate estimation of passive component performance requires computationally expensive electromagnetic simulations, the design and optimization of such components is limited. This leads to design spins as the performance can only be evaluated through a measurement based characterization ultimately affecting the time-to-market.
- Semiconductor manufacturing process variations at lower process nodes become an additional challenge as the variations in the process dimensions and material properties require a statistical model for circuit simulations. This statistical analysis relies on good estimations of variations and time-consuming simulations. This increases the IC design and model development cost.
- Advanced IC manufacturing processes require metal, polysilicon, and active layers to meet layout density rules. Therefore dummy metal features are added as a part of the design rules. These metal fills need to be considered during model creation as they negatively impact the performance of the components.

This thesis addresses the last bullet item in the passive components integration challenges. This first chapter introduces readers to metal fills in integrated circuits. Several aspects of metal fill are reviewed as follows. Section 1.1 describes the need for metal fill and typical filling algorithms. This is followed by Section 1.2 which describes the fundamental electromagnetic effects when a floating conductor is brought into time-varying electromagnetic fields. Section 1.3 continues the discussion on the effects of metal fill more at the circuit element level and demonstrates the impact on the performance of representative interconnects and spiral inductors. Section 1.4 demonstrates the impact of metal fill on circuit performance. Here the performance degradation of an LC oscillator is shown through circuit simulations. Section 1.5 discusses the possibility of increase in chip area if metal fill is blocked in large passive components. This is followed by a statement of the overall research objectives and contributions of this thesis in Sections 1.6 and 1.7, respectively. Finally Section 1.8 provides the organization of this thesis.

## 1.1 Metal Density Requirements

In this section we discuss the need for metal fill and methods to insert metal fill during the IC manufacturing process.

### 1.1.1 Advanced IC Manufacturing Process

Advanced IC manufacturing processes employ Chemical Mechanical Polishing (CMP) to planarize metal and dielectric layers [3]. Although CMP is a widely used planarization process, there are still challenges due to variations in significant surface topography caused by non-uniform IC layouts. Metal dishing and oxide erosion [4] are two major defects caused during the CMP process. Metal dishing is mainly observed in high metal density areas and results in variations in the inter-layer-dielectric (ILD) heights. Oxide erosion is a localized thinning of the dielectric and occurs during polishing. It results in an excessive oxide removal during the CMP. These defects depend on layout patterns, the polishing process settings, the over-polish time, and the incoming electroplated topography [5]. The CMP defects described in this section affect the physical dimensions of the metal layers and ILD. This impacts the electrical performance of the circuits, interconnects, and passive components. Apart from the electrical effects, there are yield related issues due to these CMP defects. Thus it is important to reduce these defects caused by layout pattern density variations.

To reduce the post-CMP defects, the layout needs to meet certain requirements. Requirements are imposed on the uniformity of metal, polysilicon, and active layers to meet certain local and global density criteria. The issues with pattern density variation could be resolved by inserting dummy features in the lower density regions and slotting of layout features in the higher density regions. These dummy features are electrically non-functional. Figure 1.1 shows an illustration of how dummy metal fills improve the post-CMP profiles [6]. These dummy features are also called tiles and, therefore, the layout step is called *tiling*. Metal fills reduce dishing and erosion in metal and ILD by increasing the pattern density uniformity.

### 1.1.2 Metal Filling: Requirements and Algorithms

The process of metal filling in any metal layer has the following objectives:

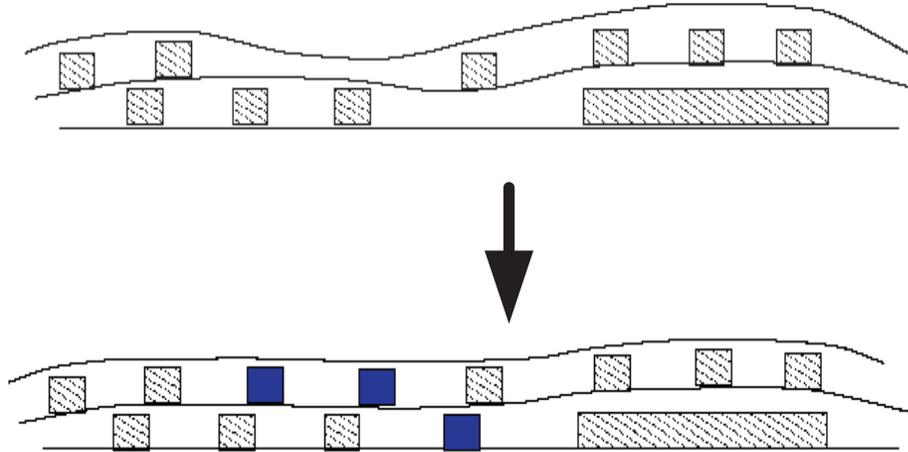


Figure 1.1: Cross section of a wafer showing two metal layers. ILD planarization problem without metal fill (top drawing). Metal fills (dark) inserted (bottom drawing) improve planarization (taken from [6]).

- Meet the metal density requirements outlined by the foundry.
- Reduce the variations in metal density within the metal layers.
- Reduce the number of metal fill that is added to reduce the mask size.
- Mitigate the impact on electrical performance through parasitic aware filling.

There are several algorithms that meet the above mentioned requirements. Here we review a representative algorithm presented in [7].

The filling algorithm processes the layout database generated by the IC designer and imposes the constraints provided by the foundry. Consider the scenario in Fig. 1.2. Here  $n$  is the layout region to be analyzed,  $w$  is the moving window size over which metal density needs to be checked,  $B$  is the buffer distance within which metal fill needs to be blocked,  $U$  is the upper bound and  $L$  is the lower bound on the density for each layer.

The first step in the algorithm is to find out the extremal density windows. The extremal density windows are the windows with minimum and maximum metal density calculated for a given window size of  $w \times w$  and  $k$  disjoint rectangles in  $n \times n$  layout region.

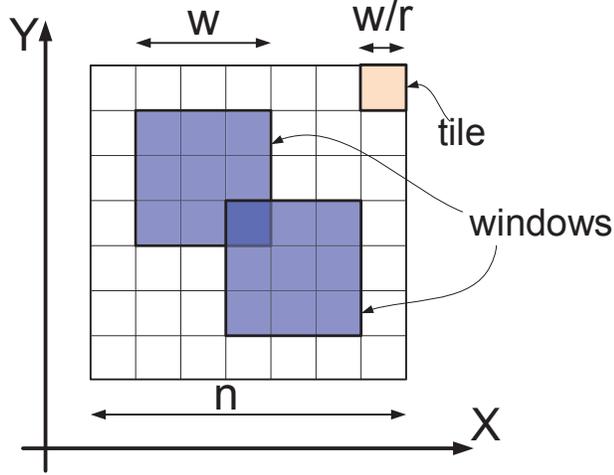


Figure 1.2: Moving window algorithm (reproduced from [7]).

For this operation, the density is calculated by moving the window with an increment of  $w/r$ , also referred to as *r-dissection*. For each of the dissections, the density is calculated as a Boolean operation of presence or absence of rectangles in a much smaller grid  $c$ , where  $c$  is equal to the minimum width or spacing for a given layer. Thus the area density is calculated for each tile,  $T_{ij}, i, j = 1, 2, \dots, \frac{n}{w/r}$ . After the density analysis, the next step is filling. In this step, the first part is the determination of optimal amount of fill that needs to be added to meet all the criteria described before. If the area density in each of the tiles is known, then slack in each tile ( $slack(T) = U - density(T)$ ) is calculated as the maximum fill amount that can be added without violating the upper bound  $U$ . The slack of a window  $W$ ,  $slack(W)$ , is calculated as the sum of all the tiles slack as  $\sum_{i,j} slack(T_{ij})$  within the window. The fill area within each tile,  $p_{ij} = p(T_{ij})$  is determined such that

$$0 \leq p_{ij} \leq slack(T_{ij}) \quad (1.1)$$

and

$$\sum_{T_{ij} \in W} p_{ij} \leq \max\{U \cdot w^2 - area(W), 0\} \quad (1.2)$$

where  $area(W)$  is the area of the layout rectangles in the window  $W$ . The next step is to actually synthesize the metal fill geometry. Here several parasitic aware criteria are introduced to mitigate the impact of metal fill and the filling is performed accordingly.

## 1.2 Electromagnetic Effect of Metal Fill

When a floating metal fill is inserted in a time-varying electromagnetic field, it alters both the electric as well as the magnetic fields. In this section, we discuss both effects in more details.

### 1.2.1 Electrostatic Formulation

In this subsection, we will review the effects of a floating metal object in an applied electric field. We consider the electrostatic case and ignore the time-harmonic electric field as the relaxation frequency of the metal conductors is much larger than the maximum frequency under consideration.

Figure 1.3 shows a floating metal object with a surface ( $S$ ). For a floating metal object in the absence of any external electric field, the free electrons in the conduction band are orientated so that the energy at the equilibrium is minimized<sup>1</sup>. When an external electric field,  $\vec{E}_e(\vec{r})$  (produced by sources not shown), is applied, the charges on the surface of the conductor are aligned to minimize the total energy [8]. Charges are induced on the surface with surface charge density  $\rho_s$  in such a way to produce an equal and opposite internal electric field  $-\vec{E}_e(\vec{r})$ . This leads to the total field inside the metal object to be zero. Since the fields inside the conductor are zero, the tangential component,  $E_t$ , of the electric field at the surface of the conductor is zero (tangential electric field is continuous at the boundary). On the other hand, the normal component of the electric field density,  $D_n$ , is equal to the surface charge density (normal electric field density is discontinuous with the discontinuity being equal to the surface charge density, and the electric field density inside the conductor is zero). This develops a normal electric field at the surface of the metal object. The total electric field outside the metal object is the sum of the applied electric field,  $\vec{E}_e(\vec{r})$  and the induced electric

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<sup>1</sup>Sir William Thomson's theorem (1848)

field,  $\bar{E}_i(\bar{r})$ ,

$$\bar{E}(\bar{r}) = \bar{E}_e(\bar{r}) + \bar{E}_i(\bar{r}). \quad (1.3)$$

The electric potential on the metal object is related to the electric field by the gradient,  $\bar{E}(\bar{r}) = -\nabla\Phi$  (since  $\nabla \times \bar{E}(\bar{r}) = 0$ ). Therefore, the surface of the conductor is an equipotential surface.

The non-zero normal component ( $E_n$ ), is related to the induced surface charge density,  $\rho_s$ , as

$$\bar{E}(\bar{r}) \cdot \hat{n} = \rho_s/\epsilon \quad (1.4)$$

where  $\epsilon$  is the permittivity of the medium surrounding the conductor. For this initially uncharged floating conductor, the total charge is equal to zero, i.e.

$$\oint_S \nabla \cdot \bar{D}(\bar{r}) d\bar{S} = Q_{tot} = 0. \quad (1.5)$$

The insertion of this floating conductor changes the electric fields and therefore the stored electric energy. The energy without the floating conductor is

$$W_e = \frac{1}{2} \int_v \epsilon |\bar{E}_e(\bar{r})|^2 dV \quad (1.6)$$

and with the floating conductor is

$$W_{e,f} = \frac{1}{2} \int_v \epsilon |(\bar{E}_e(\bar{r}) + \bar{E}_i(\bar{r}))|^2 dV. \quad (1.7)$$

From a circuit point of view, this increase in stored energy is interpreted as the increase in the capacitance of the structure producing the applied electric field.

The former discussion helps in the understanding of the relationship between the applied electric field and the induced charge density. Also, it gives an appreciation of the electromagnetic formulation of the problem.

## 1.2.2 Eddy-current Loss

In this subsection, we review the effect when metal fill is introduced into a time-harmonic magnetic field. According to Ampere's law, the impressed time-harmonics current generated by a spiral inductor causes a time-harmonic applied magnetic field,  $\bar{H}_a(\bar{r})$  inside

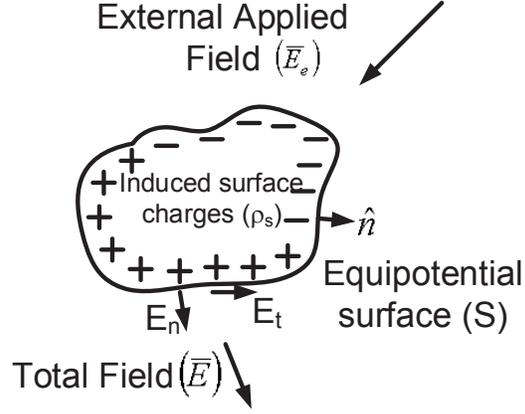


Figure 1.3: Floating conductor in electric field.

the metal fill volume as

$$\bar{H}_a(\bar{r}) = \int \frac{I'(\bar{r}') d\bar{l}' \times \bar{R}}{4\pi R^3} \quad (1.8)$$

where the current element is  $I'd\bar{l}'$  and the vector  $\bar{R}$  points from a source to an observation point. This time-harmonic magnetic field creates an electromotive force (emf),  $v_e$ , according to Faraday's law as

$$v_e = \oint \bar{E}(\bar{r}) \cdot d\bar{l} = -j\omega\mu \int_S \bar{H}_a(\bar{r}) \cdot d\bar{S} \quad (1.9)$$

where  $\mu$  is the permeability of the surrounding medium (here assumed to be homogeneous). Due to the finite conductivity of the metal fill, emf  $v_e$  produces a current density inside the metal fill,  $\bar{J}_e(\bar{r})$ . According to Lenz's law, this eddy-current  $\bar{J}_e(\bar{r})$ , produces a magnetic field,  $\bar{H}_r(\bar{r})$  as

$$\nabla \times \bar{H}_r(\bar{r}) = \bar{J}_e(\bar{r}) \quad (1.10)$$

that opposes the time-harmonic magnetic field  $\bar{H}_a(\bar{r})$ . Substituting  $\bar{J}_e(\bar{r})$  into the time-harmonic Faraday-Maxwell's equation gives a relationship between the applied field and response field as

$$\nabla \times \bar{E}(\bar{r}) = \nabla \times \frac{\bar{J}_e(\bar{r})}{\sigma} = \nabla \times \nabla \times \frac{\bar{H}_r(\bar{r})}{\sigma} = -j\omega\mu (\bar{H}_a(\bar{r}) + \bar{H}_r(\bar{r})). \quad (1.11)$$

The response field,  $\bar{H}_r(\bar{r})$  opposes  $\bar{H}_a(\bar{r})$  and reduces the total magnetic energy

$$j\omega\mu \int \frac{1}{2} |\bar{H}_a(\bar{r}) + \bar{H}_r(\bar{r})|^2 dV \quad (1.12)$$

stored in the interconnect or spiral inductor structure, thus reducing the effective inductance in addition to increasing its resistance.

The average total power loss due to the eddy-currents in metal fill volume ( $v_{\text{fill}}$ ) can be given by the Poynting's theorem as

$$P_L = \frac{1}{2} \oint (\bar{E}(\bar{r}) \times \bar{H}^*(\bar{r})) \cdot d\bar{S} = \frac{1}{2} \int_{v_{\text{fill}}} \bar{E}(\bar{r}) \cdot \bar{J}_e^*(\bar{r}) dv = \frac{1}{2} \int_{v_{\text{fill}}} \frac{|\bar{J}_e(\bar{r})|^2}{\sigma} dv \quad (1.13)$$

### 1.3 Metal Fill Impact on Interconnects and Passive Components

In this section we discuss the impact of metal fill on representative components in terms of their electrical parameters. The results for a single interconnect and a spiral inductor are repeated from [9] and [10], respectively.

#### 1.3.1 Interconnects

The insertion of metal fill in an on-chip interconnect increases its capacitance and resistance, and decreases its inductance. We illustrate these parasitic effects on a single interconnect embedded microstrip performance for different metal fill designs. The test structures under consideration are analyzed using a full-wave simulator [11]. The embedded microstrip is placed on the top-most metal layer (M6) and the ground plane is in the bottom-most metal layer (M1), as shown in Fig. 1.4. Three different microstrip designs with metal fill are considered for this analysis, each with  $5 \mu\text{m}$ ,  $10 \mu\text{m}$ , and  $15 \mu\text{m}$  wide lines and corresponding characteristic impedances of  $68 \Omega$ ,  $50 \Omega$ , and  $40 \Omega$ , respectively. The impact of metal fill size on the transmission line characteristics is studied with  $10 \times 10 \mu\text{m}^2$ ,  $5 \times 5 \mu\text{m}^2$ , and  $2.5 \times 2.5 \mu\text{m}^2$  metal fills placed on the top two layers (M6 and M5). For each design, the metal density is kept constant at 50%. The per-unit-length (p.u.l.) parameters are calculated from the transmission-line characteristic impedance ( $Z_o$ ) and propagation constant ( $\gamma$ ). These parameters are obtained from the simulated S-parameters as

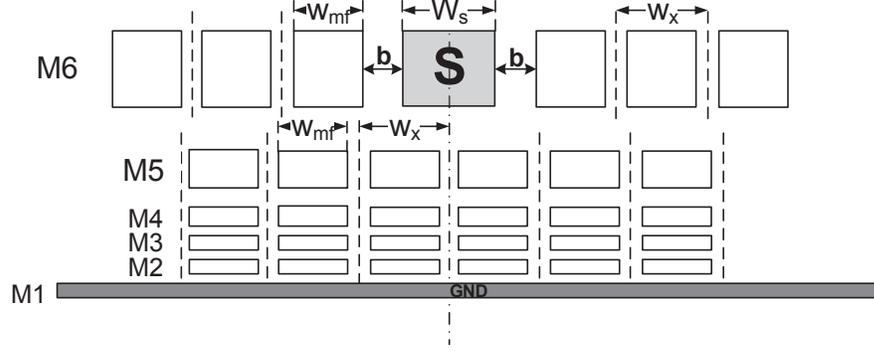


Figure 1.4: Simulation setup for single interconnect.

$$Z_o = Z_p \sqrt{\frac{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}}} \quad (1.14)$$

$$\gamma = \alpha + j\beta = \frac{1}{l} \cosh^{-1} \left( \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{2S_{21}} \right). \quad (1.15)$$

Here  $Z_p$  is the port impedance and  $l$  is the length of the interconnect. It is straightforward to calculate the p.u.l. parameters as

$$R = \text{Re}(Z_o \gamma) \quad (1.16a)$$

$$C = \frac{\text{Im}\left(\frac{Z_o}{\gamma}\right)}{\omega} \quad (1.16b)$$

We study the p.u.l. capacitance and resistance parameters to compare the electric and magnetic parasitic effects for different metal fill sizes,  $W_{mf}$ . Figure 1.5 shows the impact of metal fill size increase on parasitic capacitance and resistance at 10 GHz. The capacitance increases as the size of metal fill is increased. This is observed for all the microstrip designs. For example, for a  $5 \mu\text{m}$  wide line, default  $10 \times 10 \mu\text{m}^2$  fills resulted in a 75.7% increase in capacitance. On the other hand,  $2.5 \times 2.5 \mu\text{m}^2$  fills resulted in a 47.5% capacitance increase. The resistance also increased as the size of metal fill is increased for all the microstrip designs. For example, for a  $5 \mu\text{m}$  wide line, default  $10 \times 10 \mu\text{m}^2$  fills

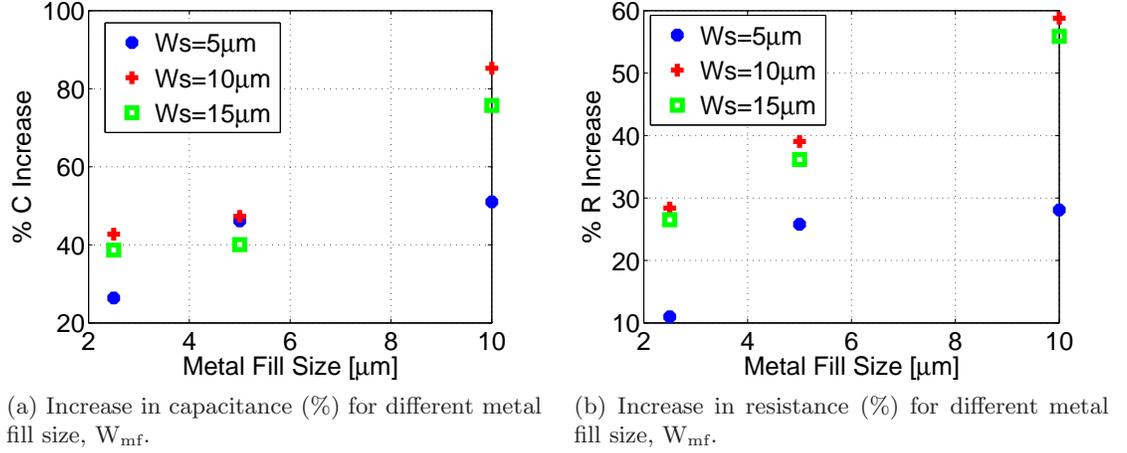


Figure 1.5: Simulation results for single interconnect.

resulted in a 50.0% increase in resistance while  $2.5 \times 2.5 \mu\text{m}^2$  fills gave a 30.0% increase. Thus, in the case of smaller fills, both eddy-current loss and parasitic capacitance are reduced. On the other hand, from the post-processing and layout perspective, the smaller metal fills cause difficulty in the following aspects of the overall design flow: 1) increase in the number of added metal fill features, which increases the database size (as well as extraction netlist); 2) increase in the number of features to scan for mask/reticle defectivity during manufacturing; and 3) increase in the cost of masks/reticles, which is dependent on the database size and the amount of defect scanning required.

### 1.3.2 Coupled Interconnects

A coupled-line structure with a ground plane is considered for analysis using a full-wave simulator [11]. The coupled lines are on the top-most metal layer (M6) and the ground plane is on the bottom-most metal layer (M1), as shown in Fig. 1.6a. Three different coupled lines are considered for this analysis with  $3 \mu\text{m}$ ,  $5 \mu\text{m}$ , and  $10 \mu\text{m}$  width and with  $2.8 \mu\text{m}$  spacing. The impact of metal fill size on the transmission line characteristics are studied. Metal fills are on the two layers M6 and M5. For each design, the metal density is kept constant at 50%. For calculating the p.u.l. parameters for the even and odd mode, the four-port S-parameters are first converted to two-port even- and

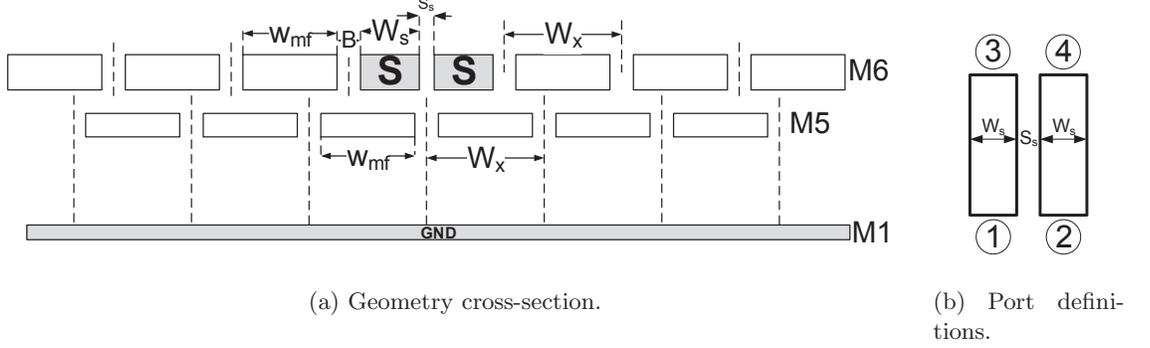


Figure 1.6: Coupled interconnect simulation setup.

odd-mode S-parameters by

$$S_e = \frac{1}{2} \begin{bmatrix} S_{11} + S_{12} + S_{21} + S_{22} & S_{13} + S_{14} + S_{23} + S_{24} \\ S_{31} + S_{23} + S_{41} + S_{42} & S_{33} + S_{34} + S_{43} + S_{44} \end{bmatrix} \quad (1.17)$$

and

$$S_o = \frac{1}{2} \begin{bmatrix} S_{11} - S_{12} - S_{21} + S_{22} & S_{13} - S_{14} - S_{23} + S_{24} \\ S_{31} - S_{32} - S_{41} + S_{42} & S_{33} - S_{34} - S_{43} + S_{44} \end{bmatrix} \quad (1.18)$$

assuming a symmetric network and ignoring mode mixing. Here ports 1 and 3 are at the each ends of line-1, and ports 2 and 4 are at the each ends of line-2 as shown in Fig. 1.6b. Ports 1 and 2, and ports 3 and 4 are on the same side of the structure, respectively. Further, the p.u.l. parameters for each mode are calculated similar to the single line study.

We compare the p.u.l. capacitance and resistance for the even and odd mode to demonstrate the impact of different metal fill designs. Fig. 1.7 shows the impact of metal fill size on even mode and odd mode p.u.l. capacitance and resistance. The p.u.l. capacitance increases as the size of metal fill is increased. This behavior is observed for all the line widths. For example, for 3  $\mu\text{m}$  wide lines, the default  $10 \times 10 \mu\text{m}^2$  fills resulted in an 84.2% increase in even mode capacitance. On the other hand,  $2.5 \times 2.5 \mu\text{m}^2$  fill provided only a 45.3% increase. The even mode resistance increased with the size of metal fill for all the line widths. For example, for a 3  $\mu\text{m}$  wide line, default  $10 \times 10 \mu\text{m}^2$  fill provided a 53.9% increase in resistance, while  $2.5 \times 2.5 \mu\text{m}^2$  fills lead to a

28.2% increase. The odd mode characteristics show insignificant effect of metal fill size variations.

### 1.3.3 Spiral Inductors

In this subsection, we will demonstrate the impact of metal fill on a spiral inductor in terms of its inductance and quality factor. Figure 1.8 illustrates the changes in an equivalent circuit model (ECM) due to metal fill. As shown in the figure, the metal fill parasitics increase the shunt capacitance in the ECM. This additional capacitance,  $\Delta C$ , degrades the quality factor of the spiral inductor. When metal fill is placed into a time-varying magnetic field, eddy currents are induced in the metal fill as explained in the previous section. These eddy currents reduce the inductance, and increase the series resistance as shown in the figure. These effects increase the losses and further degrade the quality factor of the spiral inductor.

The parameters that we will study are extracted from the 2-port network parameters. The inductance  $L_s$  is obtained from  $-1/Y_{12}$  as

$$L_s = \frac{Im(-1/Y_{12})}{\omega} \quad (1.19)$$

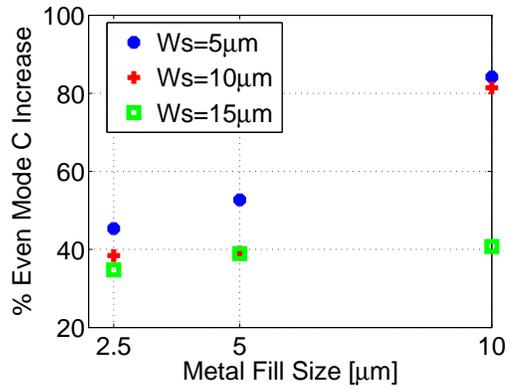
The quality factor,  $Q$ , can be defined as the ratio of energy stored to the energy dissipated and is given as

$$Q = 2\pi \cdot \frac{W_m - W_e}{W_{\text{loss}}} = -\frac{Im(Y_{11})}{Re(Y_{11})} \quad (1.20)$$

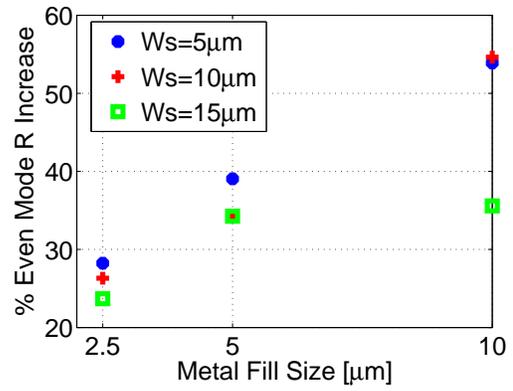
where  $W_m$  is the peak magnetic energy stored,  $W_e$  is the peak electric energy stored, and  $W_{\text{loss}}$  is the energy loss in one oscillation cycle [1].

To understand the impact of metal fill, full wave simulations are performed in a commercial simulator [11]. A simple square spiral inductor geometry is considered to demonstrate the impact on spiral inductor performance.

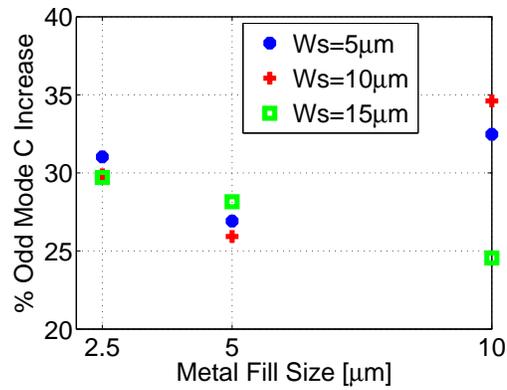
Figure 1.9 shows the simulation setup for the square inductor without metal fill. Figure 1.9a shows the top view of the inductor. A four-turn inductor with 6  $\mu\text{m}$  width, 2  $\mu\text{m}$  inter-winding spacing, 70  $\mu\text{m}$  inner diameter, and 130  $\mu\text{m}$  outer size, as shown in the figure, is considered. Figure 1.9b shows the side view of the structure. A ground



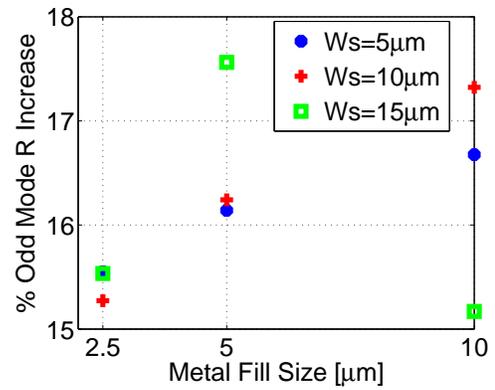
(a) Increase in pul even mode capacitance for different metal fill size,  $W_{mf}$ .



(b) Increase in pul even mode resistance for different metal fill size,  $W_{mf}$ .



(c) Increase in pul odd mode capacitance for different metal fill size,  $W_{mf}$ .



(d) Increase in pul odd mode resistance for different metal fill size,  $W_{mf}$ .

Figure 1.7: Coupled interconnect simulation results.

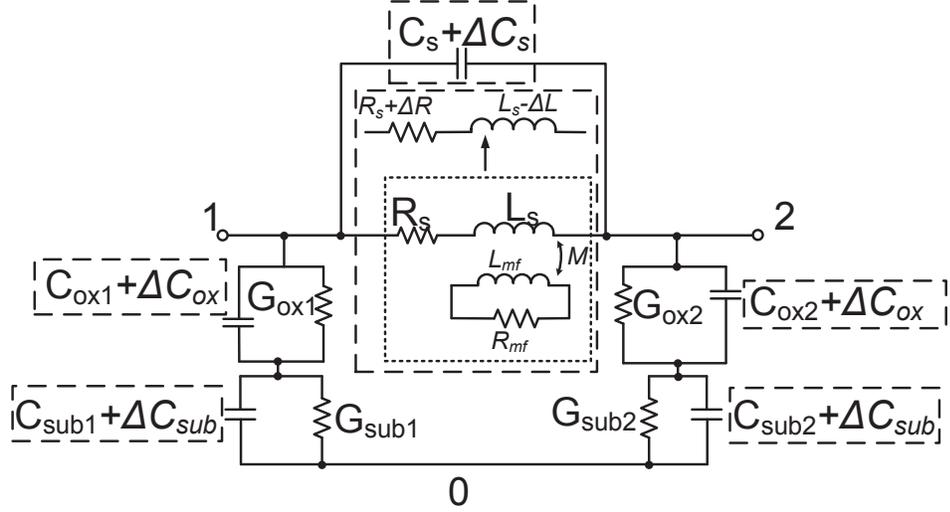


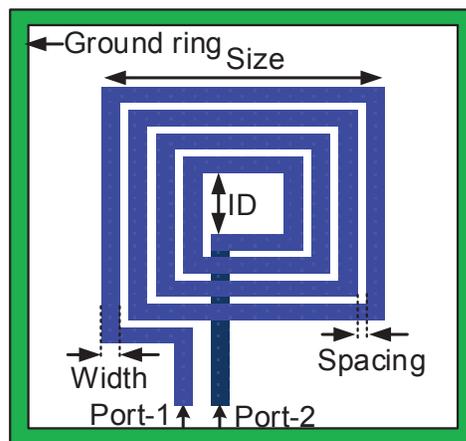
Figure 1.8: Simple  $\pi$  model of a spiral inductor with metal fill parasitics.

ring is placed around the coil to mimic the ground used for measurement purposes and it is assumed to be a perfect conductor. A lossy substrate with 10 S/m conductivity is considered. Figure 1.10 shows the setup for the simulations with M6 metal fills and M5 metal fills. The metal fill density and number of fills are equal in both setups. A  $9 \times 9 \mu\text{m}^2$  metal fill is placed with a density of about 30%. In the case of M6 metal fills, the fills are placed at 10  $\mu\text{m}$  buffer distance away from the spiral inductor.

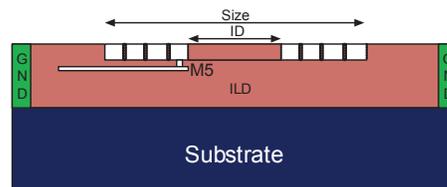
Figure 1.11b shows the simulation results for Q degradation due to metal fill. The M6 metal fill shows a 9% degradation in Q and the M5 metal fill shows 14% degradation in Q as shown in the figure.

## 1.4 Metal Fill Impact on Circuit Performance

In this section, we further discuss the impact of metal fill on the performance of an active circuit. For this study, we designed an LC oscillator in a 0.18  $\mu\text{m}$  BiCMOS process. We designed a spiral inductor which is a part of the LC tank in the oscillator. This inductor is used without and with metal fill to study the impact of metal fill on the oscillator circuit performance. The effect of metal fill considered in this work is mainly through

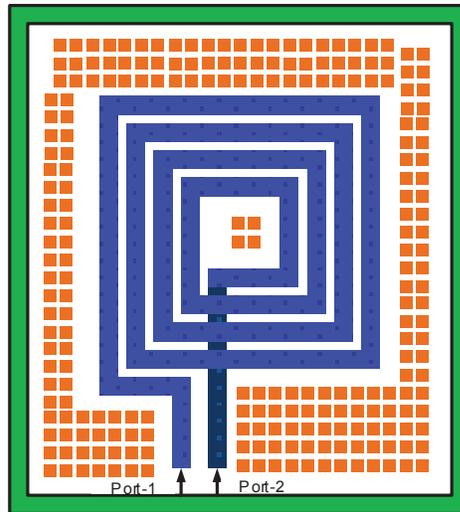


(a) Top view

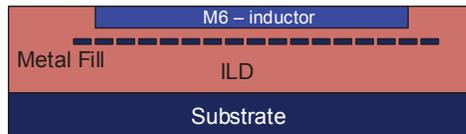


(b) Side view

Figure 1.9: Full-wave simulation setup for a square spiral inductor: without fills



(a) M6 metal fill top view



(b) M5 metal fill side view

Figure 1.10: Full-wave simulation setup for a square spiral inductor: with fills

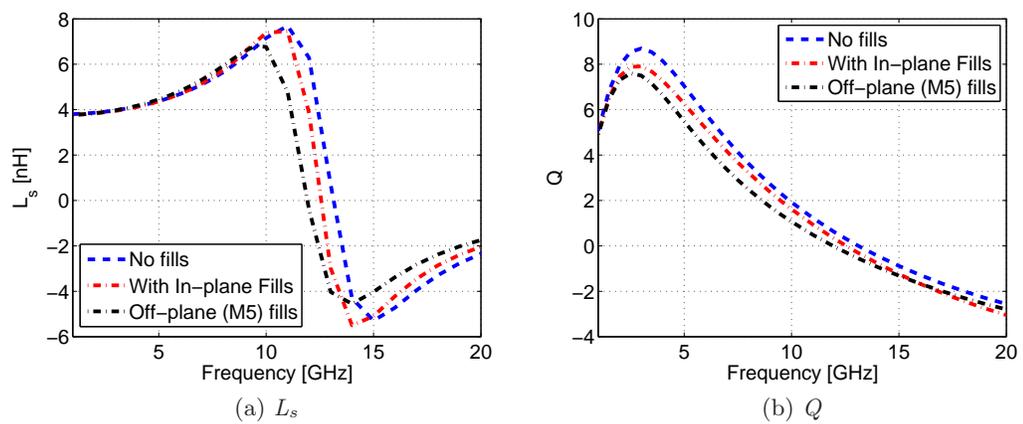


Figure 1.11: Full-wave simulation results for square inductor.

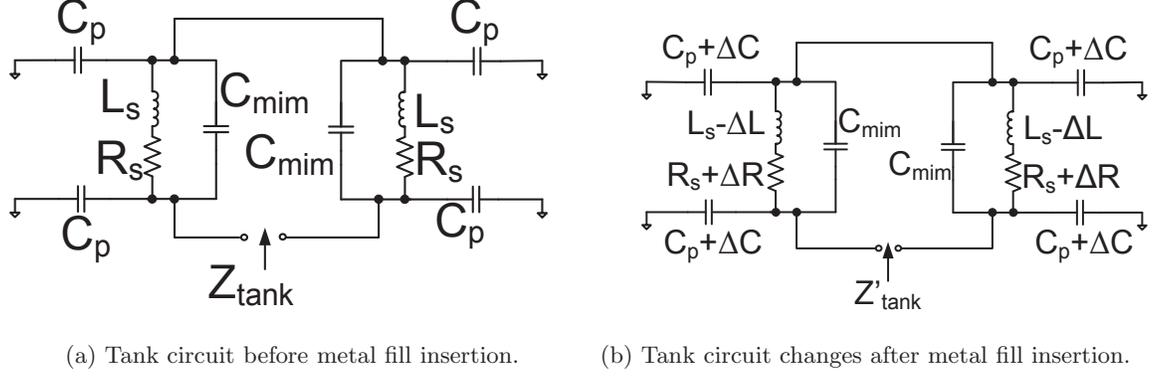


Figure 1.12: LC Oscillator tank.

the spiral inductor component, and we will discuss the impact of metal fill on the LC tank circuit used in the oscillator design.

To demonstrate the impact of metal fill on the tank circuit, consider the tank circuit in Figure 1.12a. It shows a  $C_{mim}$  in parallel with a simple equivalent circuit of the spiral inductor.  $R_s$  is the resistance due to DC and AC losses in the inductor,  $C_p$  is the shunt capacitance. As metal fill is inserted around and underneath the spiral inductor, the parasitic shunt capacitance increases by an amount  $\Delta C$  and the series resistance increases by an amount  $\Delta R_s$ , as discussed in the previous section. This is illustrated in Figure 1.12b. Since the oscillator under consideration shown in Fig. 1.15 is a differential circuit, two tanks are needed. The impedance across the two tanks is an important parameter for the oscillator operation. Figure 1.13 shows the impedance across the two nodes and the changes in the impedance as the series resistance and shunt capacitance is increased. As can be seen from the figure, the increase in series resistance reduces the peak amplitude and the capacitance increase changes the resonance frequency.

In general for the oscillator topology, the phase noise of the circuit relative to the carrier signal can be calculated as [12]

$$L(\Delta\omega) = 10 \log \left( \frac{2kT}{P_{sig}} \left( \frac{\omega}{2Q\Delta\omega} \right)^2 \right). \quad (1.21)$$

Here  $K$  is Boltzman's constant,  $T$  is the absolute temperature in Kelvins,  $P_{sig}$  is the carrier signal power,  $Q$  is the quality factor of the spiral inductor, and  $\omega$  and  $\Delta\omega$  are the

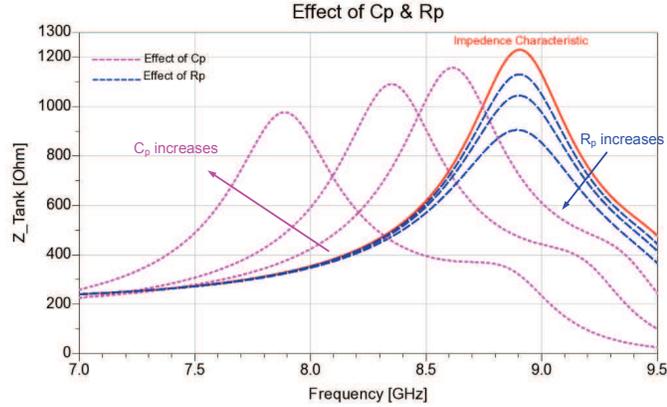


Figure 1.13:  $Z_{tank}$  change due to increase in series resistance  $R_s$  and shunt capacitance  $C_p$ .

frequency of operation and offset frequency, respectively. As can be seen in this equation, the phase noise is inversely proportional to  $Q$  and therefore, as metal fill is inserted, the phase noise increases.

Now we consider the design of the oscillator circuit. First the source coupled pair with tank circuit is designed to achieve a desired number of oscillations and a reasonable noise performance. This is followed by the design of the current source circuit. Figure 1.15 shows the topology selected for the oscillator design. Here, an ideal current source biases the pair. First, the oscillation frequency of this stage is given by [13]

$$f_{osc} = \frac{1}{2\pi\sqrt{2LC}} \quad (1.22)$$

The frequency of oscillation is selected as 8.9 GHz which is equal to the peak  $Q$  frequency of the spiral inductor. For all the metal fill designs, the DC inductance value is kept as 2.2 nH. Figure 1.14 shows an ECM extracted from spiral inductor simulated S-parameters. This model is used in all circuit simulations. With the inductor value known, the capacitor value is computed as 73 fF to achieve 8.9 GHz oscillation frequency. A  $5 \times 5 \mu\text{m}^2$  Metal-Insulator-Metal (MIM) capacitor is used to implement this value. The impact of metal fill on MIM capacitor parasitics is ignored. The transistor sizes are selected in such a way that the oscillation criterion as well as the low noise performance are achieved.

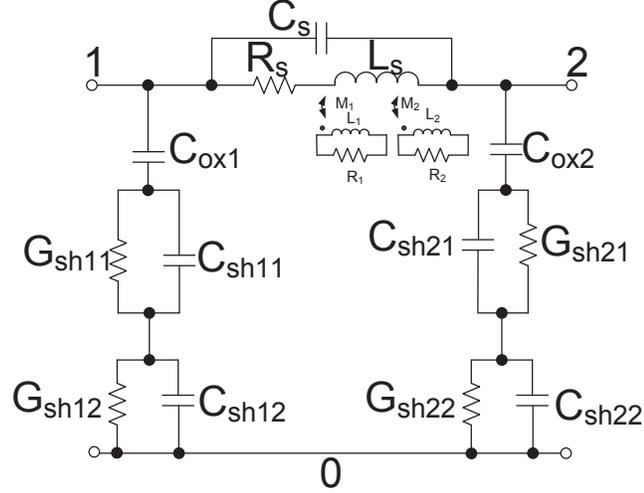


Figure 1.14: Spiral inductor higher order model extracted from EM simulation results.

The oscillation criterion for this circuit is given as

$$Re(Z_{tank}) > \frac{2}{g_m} \quad (1.23)$$

where  $g_m$  is the transconductance of the transistor. Through iterations, the transistor size is selected as  $W/L = 6 \mu\text{m}/0.5 \mu\text{m}$ . The  $I_{bias}$  current value is chosen as 0.5 mA so that the oscillation criterion is met. To evaluate the oscillator performance degradation due to metal fill, we use the extracted circuit models in the design and perform the analysis. Two test cases are considered for this analysis: without and with M5 metal fill.

Figure 1.16 shows the transient and noise analysis results. As can be seen from the transient analysis, as metal fill is inserted, the oscillation swing reduces from 1.21 V to 0.95 V. The settling time has also increased from 6.4 nS to 8 nS due to the additional capacitive loading as a result of metal fill insertion. The oscillation frequency reduces from 8.99 GHz to 8.66 GHz. The overall effect of the additional parasitics can be seen in the phase noise. Reduced Q results in degraded phase noise as well. In the phase noise analysis, the noise is degraded from -100.9 dBc/Hz to -95.45 dBc/Hz.

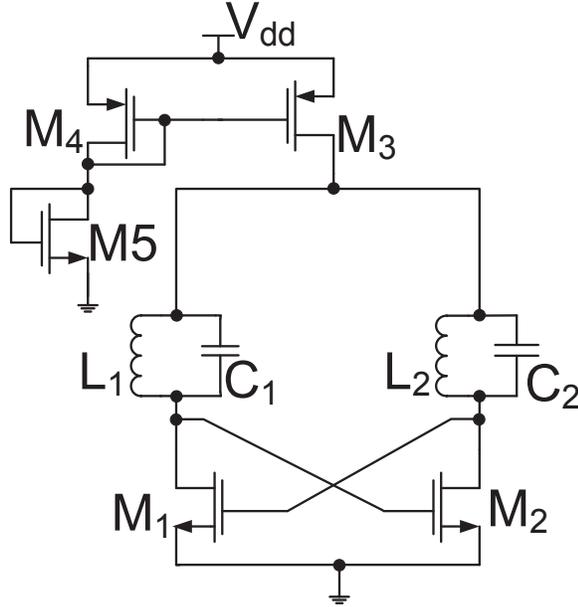
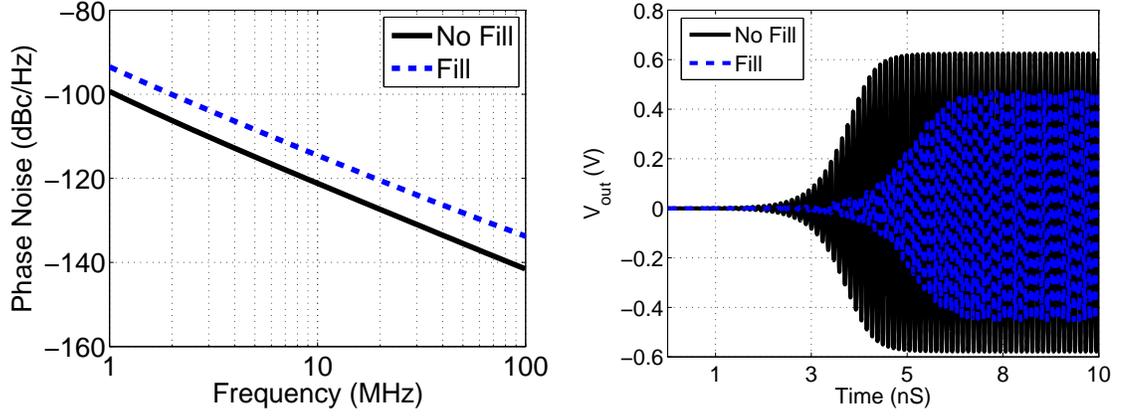


Figure 1.15: Oscillator schematics.

## 1.5 Impact on Chip Size due to Blocking of Metal Fill

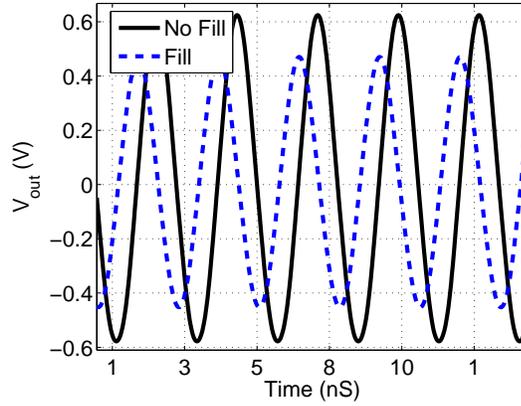
In this section, we discuss the impact on IC size if metal fill is blocked in certain regions, especially underneath large passive components. A few low end BiCMOS processes ( $0.18\mu\text{m}$  and higher) typically have less constrained design rules. In these processes, metal fill insertion underneath the large components such as spiral inductors and baluns can be blocked. Typically, in RF layouts, one of the trade-offs is between the noise coupling and the chip area. For cost reasons, the chip is typically densely laid out. At the same time, in a typical RF chip, most of the area is consumed by passive components. Figure 1.17 shows a die photo of such a chip used in a satellite transceiver application [14].

For this analysis, we assume the following notation:  $A_o$  is the original chip area without metal fill added,  $c : 0 \rightarrow 1$  is a coverage factor for passive components calculated as the ratio of the total area occupied by the passive components and  $A_o$ ,  $D_{np}$  is the density of chip area other than passive components ( $(1 - c)A_o$ ),  $D_{max}$  is the maximum



(a) Phase noise.

(b) Transient response.

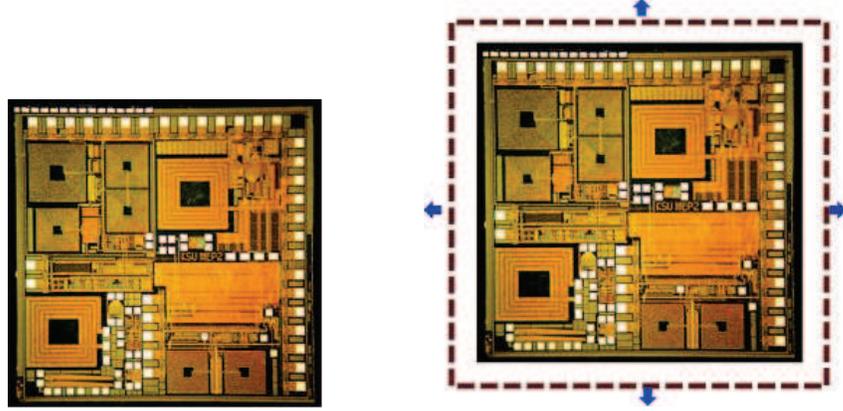


(c) Details of Fig. 1.16b.

Figure 1.16: Performance degradation due to metal fill.

possible metal density for the metal layer,  $D_{req}$  is the global density target for the entire chip. If the density of the chip area  $(1 - c)A_o$  is less than  $D_{req}$  and metal fill insetion in the area occupied by passive components  $(c \cdot A_o)$  is blocked, the area of the chip needs to be increased to  $A_n$ . Thus for this new area, the required density can be calculated as

$$D_{req} = \frac{D_{np} \cdot (1 - c)A_o + (A_n - A_o) \cdot D_{max}}{A_n} \quad (1.24)$$



(a) An example RFIC with large number of passive components. (b) Chip size increase if metal fill blocked in proximity to passive components.

Figure 1.17: Impact of metal fill keep out zones for RF application IC.

Rearranging for the ratio  $\frac{A_n}{A_o}$ ,

$$\frac{A_n}{A_o} = \frac{D_{np} \cdot (1 - c) - D_{max}}{D_{req} - D_{max}}. \quad (1.25)$$

Figure 1.18 shows the trend in increase in chip size as the desired density is increased for various passive component coverage factors. When the area ratio is larger than 1, the chip size needs to be increased to meet the density requirements. For example, if passive components coverage is 50% ( $c = 0.5$ ) and the rest of the chip excluding passive components has a metal density of 50% and the maximum possible density is 60%, the increase in chip area is 1.167X.

## 1.6 Research Objectives

The research work in this thesis addresses challenges in enabling metal-fill-aware design of integrated circuits. The main objective of this research is to demonstrate a profound change in the existing computer-aided-design (CAD) flow of passive components in the presence of metal fill. The existing CAD flow treats metal filling as a post processing

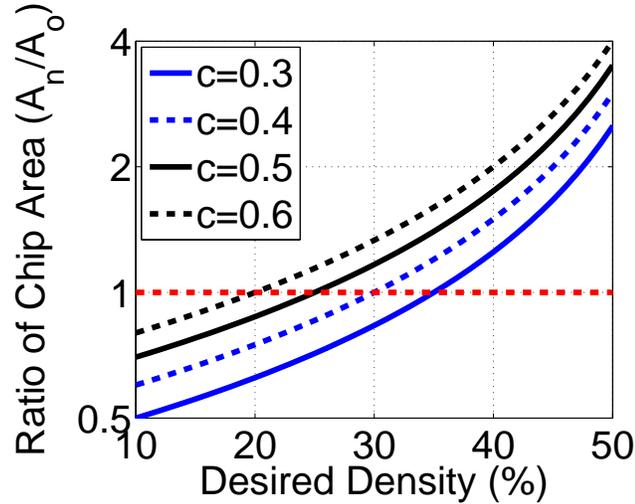


Figure 1.18: Increase in chip size as a function of desired density requirements.

step. This is mainly due to the lack of fast and scalable methods to include the effect of metal fill in passive components. The change demonstrated in the IC CAD flow makes metal fill an inherent part of the IC design process. To achieve this, the designers need models that accurately and efficiently include the effects of metal fill in the passive components. Furthermore, design guidelines to optimize the performance of these components are key applications of the models. Therefore, an objective of this research is to demonstrate modeling methods that are fast and accurate over broad ranges of physical dimensions, process parameters, and frequencies. Due to the complexity of the on-chip passive components, we rely on accurate measurement characterization for the performance evaluation of the components. Therefore, another objective of this thesis is to demonstrate accurate characterization approaches for on-wafer measurement of passive components.

## 1.7 Research Contributions

Although the theory and techniques demonstrated in this thesis are demonstrated for representative transmission line and spiral inductor structures, they are applicable to a class of problems. To achieve the objectives described in the previous section, this thesis

makes the following contributions:

1. A problem reduction approach is demonstrated for including floating conductors in the modeling of uniform transmission lines. The novelty of this approach is in the techniques demonstrated for the reduction of a complex problem in all the three dimensions. With our approach, the required computational complexity is significantly reduced and therefore this technique is very attractive for uniform on-chip transmission line problems. The impact of the technique is demonstrated by its application to multi-conductor embedded microstrips and coplanar waveguides. These structures are very relevant for microwave/millimeter-wave IC design. The theoretical contribution of this approach includes a formulation for an effective linear density that transforms a complex 3D problem into simpler 2D problems.
2. A modeling method for rectangular spiral inductors in the presence of metal fill is demonstrated. The uniqueness of this method lies in the computations of the partial element equivalent circuits representation of metal fill parasitic effects and their incorporation in the partial element equivalent circuit of spiral inductors. Techniques are demonstrated to calculate the partial resistance, inductance, conductance, and capacitance elements of metal fill in the spiral inductor. With this work, we are now able to estimate the performance of spiral inductors in the presence of metal fill, which enables the design and optimization of these components. Similar techniques are not available in the literature that can capture parasitic effects of metal fill in spiral inductors. The theoretical contribution of this work includes the analytical estimation of spiral inductor electric and magnetic fields and computation of individual partial elements to capture metal fill effects.
3. Finally we demonstrate an accurate characterization of on-chip passive components using an on-wafer VNA calibration technique. The uniqueness of this work is in the implementation of on-chip calibration standards. Further, the statistical analysis of the measurement results provides a better confidence in the results. This work is the first time demonstration of on-chip multi-line through-reflect-line (MTRL) calibration standards design for spiral inductor measurements and application of statistical error analysis methods.

## 1.8 Organization of the Thesis

This thesis is organized as follows. We discuss the capacitance modeling aspects of metal fill for transmission lines in Chapter 2. This is followed by a full-wave electromagnetic distributed modeling method for spiral inductors in the presence of metal fill in Chapter 3. Chapter 4 provides the details of the on-chip calibration structures and statistical error analysis. Chapter 5 presents the comparison of the measurement results with the models for the fabricated transmission line and spiral inductor. Finally, Chapter 6 provides conclusions and directions for future work.

## Chapter 2: Modeling Technique for Metal Fill Parasitic Capacitance

### 2.1 Introduction

In the previous chapter, we discussed the metal filling requirements and the impact of metal fill on active and passive circuits. Up to this point, hopefully readers have a good appreciation for the severity of the metal fill problem in integrated circuits. With this background, now we focus our discussion to the modeling methods we proposed to estimate the parasitic effects of metal fill. This knowledge of metal fill parasitic effects during the design phase enables metal-fill-aware design of integrated circuits. In this and the next chapters, we provide details of the capacitance modeling of multi-conductor interconnects and passive components in the presence of metal fill.

In this chapter, we present a general modeling technique for the capacitance of on-chip interconnects in the presence of metal fill. We verify the performance of the technique in terms of accuracy and computational efficiency by comparison with electromagnetic simulations. We demonstrate the applicability of our modeling method for on-chip embedded microstrip and coplanar waveguide (CPW) transmission lines in the presence of both, metal fill and floating metal strips used to realize slow-wave structures. In Section 2.2, we first discuss the major challenges in modeling interconnects capacitance in the presence of metal fill. In Section 2.3, we provide a focused review of prior research work on this problem and show the limitations of two representative methods in terms of accuracy. Next, in Section 2.4, we give details of the physical problem and its corresponding electrostatic problem formulation. In Sections 2.5 and 2.6, we give an overview and provide detailed steps of our solution approach, respectively. Following the details of the solution approach, we demonstrate its performance through a rigorous verification and its computational efficiency in Section 2.7. We show versatility of the approach in Section 2.8 with four representative applications: 1) embedded microstrip with metal fill, 2) embedded microstrip with floating metal strips orthogonal to the transmission line, 3) CPW with metal fill, and 4) CPW with floating metal strips orthogonal to the waveguide.

## 2.2 Challenges in Capacitance Modeling

In this section, we provide details of the major challenges in analyzing the problem of multi-conductor interconnects in the presence of metal fill using traditional methods. The traditional approaches of solving a capacitance of the metal fill problem include: i) solution of Poisson's equation through numerical methods; ii) closed-form expressions for the capacitance using analytical or empirical formulations. First, we discuss challenges associated with a fully numerical approach.

The primary challenge in solving this problem is the large number of metal fills added during the post-processing of the IC layout. Typically, in noise sensitive regions, IC designers carefully lay out interconnects with very few other interconnects close-by; this results in a lower metal density near critical signal lines. Consequently, the post-processing (metal density design rule check) of this layout arrangement requires metal filling in all metal layers surrounding the critical interconnects. To mitigate the parasitic effects, the size of the metal fill is kept small [10], further increasing the number of fills in a given layout region. Therefore, depending on the number of metal layers in a process technology, the total number of metal fills can be very large. This poses a limitation to the numerical methods.

The numerical solution of electrostatic problems requires solution to Poisson's partial differential equation,

$$\nabla^2 \Phi(\bar{r}) = -\rho(\bar{r}') / \epsilon \quad (2.1)$$

for the unknown volume charge distribution,  $\rho$  [15]. Here  $\Phi$  is the potential everywhere in the homogeneous space and  $\epsilon$  is the dielectric material permittivity. For conductor problems, one solution approach to solve for the unknown surface charge density is through an integral formulation as

$$\Phi(\bar{r}) = \iint_S G(\bar{r}, \bar{r}') \rho_S(\bar{r}') dS' \quad (2.2)$$

where  $S$  is the conductor surface under consideration, and  $G(\cdot)$  is the Green's function (potential at  $\bar{r}$  due to a point charge at  $\bar{r}'$ , where  $\bar{r}, \bar{r}' \in \mathbb{R}^3$ ) appropriate for the problem. The problem can be solved using appropriate basis functions to approximate the unknown charge density and testing functions to force the known potentials on the conductors.

The total charge on a conductor and the known potential are used to solve for the capacitance matrix. Extension of this approach for the metal fill problem is illustrated in [16]. Another approach is to directly discretize Poisson's equation using the Finite Difference or Finite Element method to solve for the unknown potential or field and calculate the total charge on each conductor as

$$Q = -\epsilon \oint \frac{\partial \Phi}{\partial n} dl \quad (2.3)$$

and further calculate the capacitance as  $C = Q/V$  for a known potential on the conductor. Research in [17] shows an implementation of a floating condition in the Finite Element Method that is appropriate for the metal fill problem.

The potential on floating metal fills is unknown because the metal fill structures are not treated as a part of the signal conductors. Hence many commercial legacy parasitic extraction tools may be limited in solving this problem. One way to solve this problem is to treat metal fill as a part of the signal interconnects. This leads to many additional entries in the capacitance matrix corresponding to the large number of metal fills. To minimize the burden on the circuit simulator, this circuit network needs to be reduced by using the floating condition for metal fill (total charge on floating conductor equals 0). This reduction can be computationally expensive as the number of metal fills is typically large. Since metal fill is treated as a signal conductor, it is required to discretize the metal fill geometry sufficiently dense to accurately capture the unknown charge density or fields. This increases the number of solution unknowns and makes the problem computationally expensive.

The second approach to solve for capacitance of a metal fill problem is to develop closed-form-expressions for the capacitance or an equivalent parameter (such as effective dielectric material property or a physical dimension) that aids in the solution. For this approach, scalability of the solution with respect to the physical dimensions (such as interconnect and metal fill size, separation, thickness, etc.) and material parameters (such as permittivity of each inter-layer-dielectric layer, etc.) is an issue. To achieve scalability in this approach, a large number of physical dimensions and process parameters need to be considered. The multi-conductor interconnect capacitance calculation without metal fill itself is a complex problem and the insertion of metal fill further increases this complexity by significantly increasing the number of physical dimensions (such as metal fill

size, density, thickness, location, etc.). This poses challenges in solving the problem in analytical or semi-analytical/empirical form.

## 2.3 Literature Review

In this section, we provide a focused review of capacitance modeling methods proposed in the literature for interconnects in the presence of metal fill. Next, we evaluate the performance of two representative methods in terms of their accuracy.

### 2.3.1 Summary of Previous Methods

Researchers have treated the problem of metal fill parasitic capacitance using both, numerical and empirical approaches. The approaches using numerical methods such as the Boundary Element Method (BEM) [16] and Markov chain based hierarchical approaches [18],[19] are computationally expensive. The second approach is to develop closed-form-expressions based on analytical or semi-analytical/empirical formulations. For example, simple formulas presented in [20], [21] enable fast parasitic capacitance modeling; however, they have limited accuracy over a wide range of physical parameters. Research published in [22] is limited to capacitance formulas that deal with coupling capacitance between interconnects, and ignore the capacitance to ground or to the reference conductor. Another approach is to capture the effect of metal fill through parametric approximation. For example, a study presented in [23] is based on replacing each metal layer with an effective dielectric constant; however, this paper excludes the details of this effective dielectric constant calculations. Further, Gaskill et al. have developed wide-range closed-form expressions for an effective dielectric constant, which aid in the calculation of parasitic capacitance of metal fill between parallel plates [24]. Another approach is to store the capacitance values in a form of look-up-tables, as demonstrated in a design of experiment (DOE) based approach [25]. It relies on the look-up-table formed with precomputed electromagnetic simulation results over a range of physical geometry parameters.

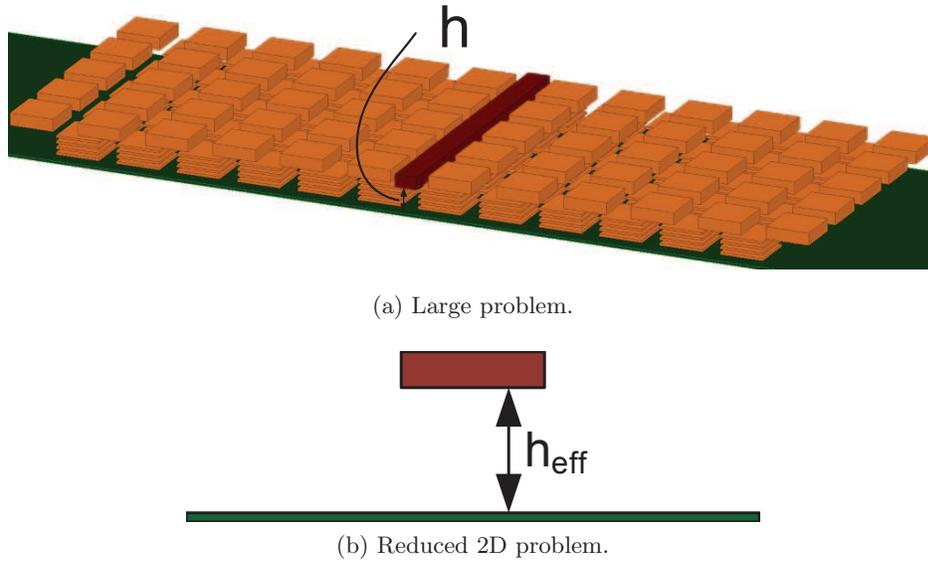


Figure 2.1: Approximation of metal fill effects using effective height,  $h_{\text{eff}}$  in [20].

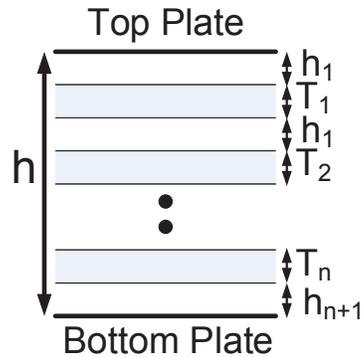


Figure 2.2: Approximation of metal fill effects using effective height: derivation of  $h_{\text{eff}}$  using parallel plate scenario.

### 2.3.2 Implementation of Representative Methods

To assess the accuracy of previously published methods, we verified the performance of two fast and scalable methods for metal fill capacitance in interconnect. These methods are based on adjusting the height of the interconnect over the ground plane. Figure 2.1

shows the setup used to evaluate the methods. The adjusted height is calculated by subtracting the metal fill layer thicknesses as

$$h_{\text{eff}} = h - \sum_i T_i \quad (2.4)$$

where  $h$  is the height of the interconnect over the ground plane, and  $T_i$  is the thickness of the  $i^{\text{th}}$  metal fill layer. This approach assumes a fundamental parallel plate formulation shown in Fig. 2.2. Consider a scenario where  $n$  floating metal layers are added into the parallel plate configuration. The total parallel plate capacitance is a series combination of individual per unit length parallel plate capacitances as

$$C_t = \frac{1}{\frac{h_1}{\epsilon W} + \frac{h_2}{\epsilon W} + \dots + \frac{h_{n+1}}{\epsilon W}} = \frac{1}{\frac{1}{\epsilon W} (h_1 + h_2 + \dots + h_{n+1})} = \frac{\epsilon W}{h - \sum_i T_i}. \quad (2.5)$$

Here  $h_i$  is the height of the  $i^{\text{th}}$  metal layer over ground plane,  $W$  is the width of the parallel plate, and  $\epsilon$  is the material permittivity. In the above equation, the term in the denominator of the right hand side is  $h_{\text{eff}}$ .

To verify this assumption, we inserted metal fill between a single interconnect and a ground plane in a 0.18  $\mu\text{m}$  Bi-CMOS process as shown in Fig. 2.1a. The methods in [26] and [20] were implemented to calculate the capacitance with metal fill. Both the methods rely on the approximation of metal fill using an  $h_{\text{eff}}$  parameter previously discussed. The method proposed in [20] relies on a 2D electrostatic simulator for the calculations for the geometry shown in Fig. 2.1b. On the other hand, the method proposed in [26] relies on the capacitance calculation of the reduced problem using closed-form-expressions. Figures 2.3a and 2.3b show the histogram of error between the total capacitance computed with the closed-form-expression and simulated using an electrostatic simulator [27]. We varied the dimensions of the metal fill as well as the interconnect over a wide-range of physical parameters. Since the effective height is not a function of interconnect and metal fill dimensions, these approaches result in inaccurate results.

The  $h_{\text{eff}}$  approach overestimates the capacitance for low metal fill density as the sparsely distributed metal fill is approximated by a continuous metal layer. This explains the negative errors in the histogram. However, it is non-trivial to see the positive errors in Fig. 2.3a. The explanation for this effect is as follows. Asymptotically, as the density approaches 100 % (metal fill planes), the total capacitance is a series combination of

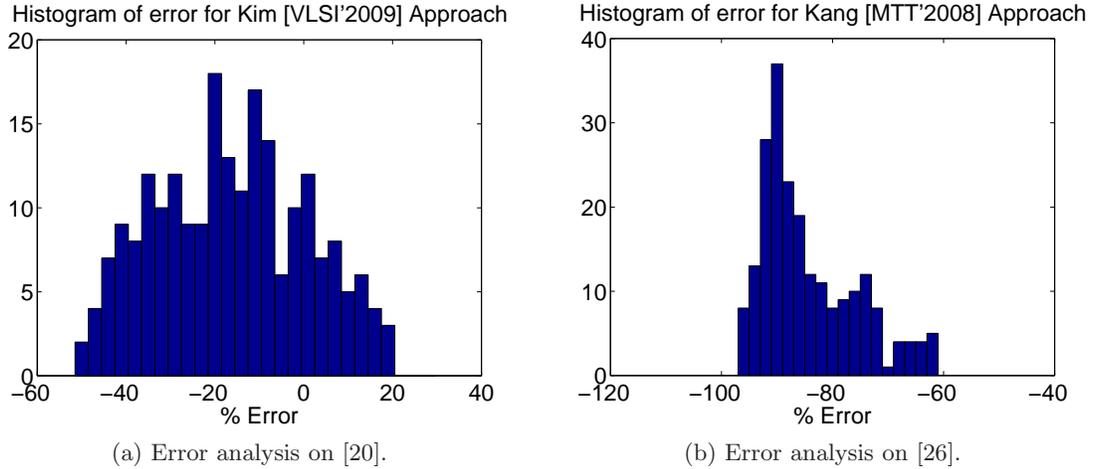


Figure 2.3: Performance of previous methods for 0.18  $\mu\text{m}$  process stack-up.

two capacitances. The first is the parallel plate capacitance between the metal fill layer and the ground plane. The second is the capacitance between the interconnect and the metal fill layer separated by  $h_1$ . This second capacitance is much smaller than the parallel plate capacitance. Therefore the overall capacitance in simulations is that of the second capacitance. However, for the  $h_{\text{eff}}$  based approach, the capacitance is that of the interconnect over a ground plane at height of  $h_{\text{eff}}$  since  $h_{\text{eff}} > h_1$ . Therefore the parallel plate based  $h_{\text{eff}}$  assumption underestimates the capacitance. This results in a positive error in the histogram.

## 2.4 Problem Formulation

This section provides the details of the physical problem under consideration in terms of physical and material properties.

Figure 2.4 shows the problem under consideration. The metal fills are laid on all metal layers including the metal layer of the interconnect. The filling is uniform in both the x- and z-direction. The size and density of metal fill is assumed to be the same on all the layers. The aspect ratio of metal fill is assumed to be one (square metal fill). All metal fill are assumed to be floating. The objective is to solve the problem with scalability in the physical dimensions as well as the material parameters. Figure 2.5

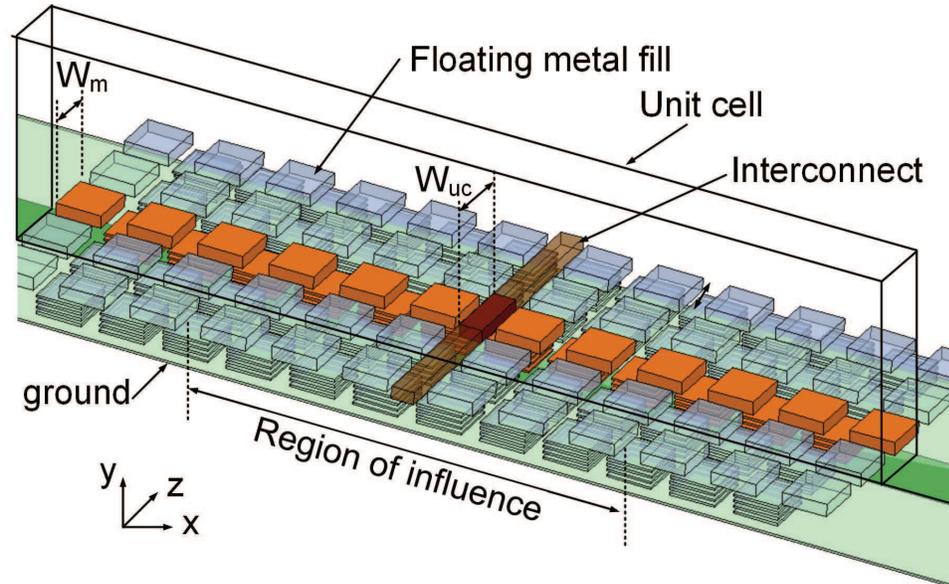


Figure 2.4: 3D problem with unit cell (highlighted) and indicated region of influence.

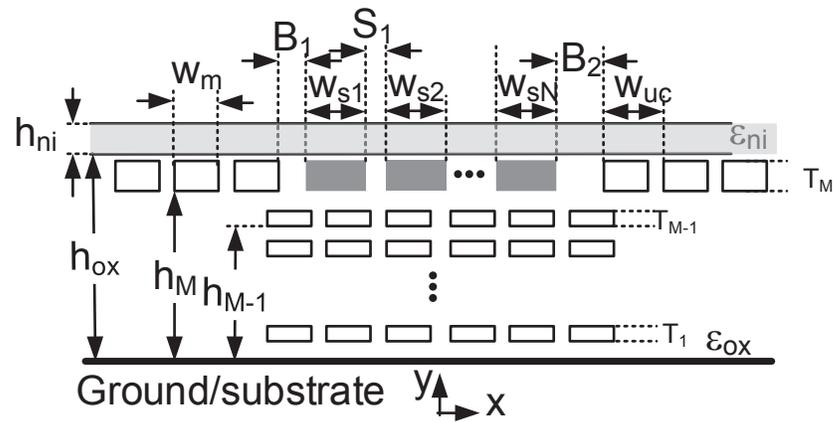


Figure 2.5: Cross-sectional view of problem setup.

shows the cross-section of the problem setup. The scalable physical parameters include: widths ( $W_{s1}, W_{s2}, \dots, W_{sN}$ ) of  $N$  interconnects and spacings ( $S_1, S_2, \dots, S_{N-1}$ ) between

the interconnects, buffer distances ( $B_1$  and  $B_2$ ) between interconnects and the nearest metal fill in the same metal layer, metal fill size ( $W_m$ ) and density ( $D$ ), the location of each metal fill ( $x_i, y_i, z_i \ i : 1 \rightarrow P$ ) where  $P$  is the number of metal fills. The vertical technology stack includes: height of oxide ( $h_{ox}$ ) and nitride layers ( $h_{ni}$ ), height of  $M$  metal layers over the substrate ( $h_i \ i : 1 \rightarrow M$ ), and thickness ( $T_i \ i : 1 \rightarrow M$ ) of each metal layer. The material parameters include the dielectric constants of each dielectric and substrate layers.

Refer to 1.2.1 for the electromagnetic formulation in terms of the boundary conditions, potential, and charge assumptions.

## 2.5 Overview of Solution Approach

Our solution approach is a combination of empirical and numerical techniques. It leverages the simplicity and speed-up due to the empirical part and the accuracy due to the numerical part. In the proposed approach, we utilize the periodicity of the metal fill layout and reduce the electrostatic problem to a unit cell. This unit cell consists of a vertical stack of metal fill in the longitudinal direction ( $z$ ) as highlighted in Fig. 2.4. We estimate the electric field for a given interconnect structure and determine the region of influence (ROI) for metal fills to be considered. This reduces the number of metal fills in the lateral direction ( $x$ ). We have developed an effective linear density parameter to transform the complex 3D problem into simpler 2D problems which reduces the complexity of numerical computations ( $O(n^3) \rightarrow O(n^2)$ ). We further replace the metal fills in the lower metal layers with an effective dielectric constant reducing the problem in the vertical ( $y$ ) direction. Thus, at the end of the problem reduction, the remaining fewer metal fills can be solved efficiently using a 2D electrostatic simulator or appropriate closed-form-expressions for multi-conductor interconnects with multiple dielectric layers.

## 2.6 Details of Solution Approach

This section provides the details of the three major steps in our problem reduction approach, each corresponding to a problem reduction in one dimension. We will also provide details of the approach, its physical motivation, and justification using experimental evidence.

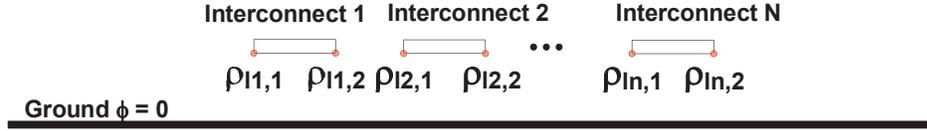


Figure 2.6: Interconnect lines on ground plane approximated as two line charges at the lower corners to estimate the electric fields.

### 2.6.1 Number of Metal Fills to Consider

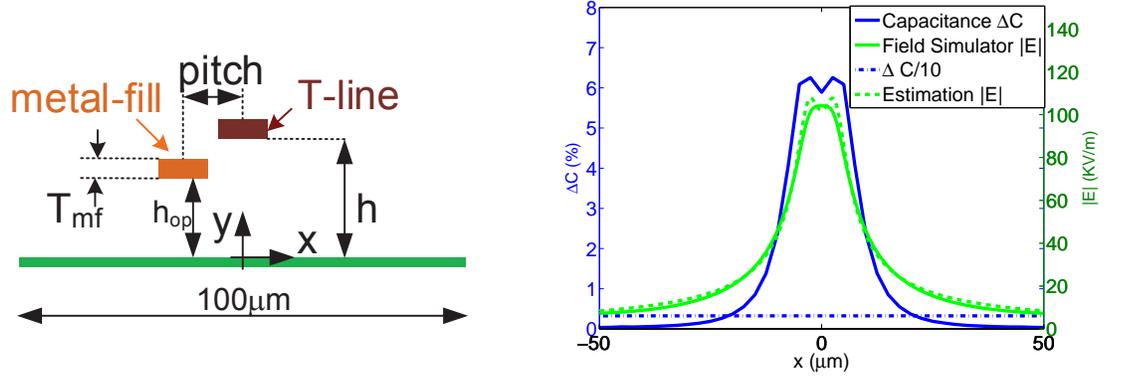
One of the important challenges in solving this problem is the number of metal fills which makes the size of the problem very large. Therefore a key step is to identify the number of critical metal fills that need to be considered for the modeling process. We define a region of influence (ROI), as the distance over which the magnitude of the applied electric field generated by the interconnects is within a certain percentage of the maximum electric field. The motivation behind using the electric field as a criterion to determine ROI is as follows. The induced surface charge density,  $\rho_s$ , on the floating metal fill is proportional to the applied electric field, and the induced electric field is proportional to the induced charge density. The increase in capacitance due to insertion of a metal fill is proportional to the energy stored in the electric fields of the interconnect structure, and therefore, is proportional to the magnitude square of the applied electric field.

To determine ROI, we estimated the electric field in the lateral dimension ( $x$ ) assuming a 2D problem without metal fill. We approximate the interconnects on a ground plane as a pair of line charges located at the lower corners of the interconnect as shown in Fig. 2.6.

The total electric field due to  $N$  interconnects each represented by two line charges at  $\vec{r}'_{m,1}$  and  $\vec{r}'_{m,2}$  is

$$\vec{E}(\vec{r}, \vec{r}') = \sum_{m=1}^N \frac{\rho_{l(m,1)}}{2\pi\epsilon|\vec{r} - \vec{r}'_{m,1}|} \hat{a}_{r_1} + \frac{\rho_{l(m,2)}}{2\pi\epsilon|\vec{r} - \vec{r}'_{m,2}|} \hat{a}_{r_2} \quad (2.6)$$

where  $\vec{r}$  is a vector pointing to the observation point,  $\rho_{l(m,1)}$  and  $\rho_{l(m,2)}$  are the line charge densities associated with the  $m^{\text{th}}$  interconnect.  $\rho_{l(m,1)}$  and  $\rho_{l(m,2)}$  are calculated from the 2D per unit length (p.u.l.) capacitance of the  $m^{\text{th}}$  interconnect to ground,  $C_{m0}$ . To



(a) Problem setup.

(b) Performance of the approximation through a comparison with an electrostatic field simulator: electrical field as a function of lateral dimension at  $h = h_{op}$  (height of the metal layer underneath interconnect line) and increase in capacitance as a function of metal fill lateral ( $x$ ) location.

Figure 2.7: Verification of electric field estimation.

verify the accuracy of this approximation, we calculated the electric field due to a single interconnect on a ground plane using a 2D electrostatic simulator [27] and compared the results with our approximation. Figure 2.7a shows a setup for the verification. The interconnect line is at a height of  $h$  from the ground and the metal fill is at a height of  $h_{op}$  from the ground plane. The metal fill thickness is  $T_{mf}$ . Figure 2.7b shows the electric field magnitude (right  $y$ -axis) as a function of the lateral position ( $x$ ) at  $y = h_{op} + T_{mf}/2$ , where  $h_{op}$  is the height of the metal layer containing metal fill over the ground plane. As the figure shows, our simple line charge approximation is able to provide a sufficiently accurate estimation of the electric field. To validate our hypothesis of increase in metal fill capacitance as a function of the applied electric field, we performed a simple test. We plotted the increase in capacitance due to a single metal fill placed at height  $h_{op}$  as a function of the lateral distance ( $x$ ) from the center of the line at  $x = 0$  to  $x = 50 \mu\text{m}$ . The interconnect width is  $10 \mu\text{m}$  and has a thickness of  $2 \mu\text{m}$ . Metal fill size is  $10 \mu\text{m}$  and thickness is  $1 \mu\text{m}$ . Figure 2.7b shows an increase in capacitance (left  $y$ -axis) as a function of the pitch ( $x$ -distance between the center of interconnect line to the center of metal fill) calculated from a 2D electrostatic simulator [27]. As can be seen

from the figure, the slope of capacitance reduction is higher than the slope of electric field reduction. This result shows the validity of our approach to identify the number of significant metal fills. Next, the task is to determine an appropriate cut-off limit for the normalized electric field. From the experimental evidence, we assume approximately 5% as the cut-off distance to define the ROI. Then, all the metal fills present within the ROI in the lateral direction ( $x$ ) are considered and all the other metal fills are ignored.

### 2.6.2 Problem Reduction using Periodicity

In this subsection, we will discuss our approach for the longitudinal problem reduction considering the periodic arrangement of metal fills. The metal filling algorithms described in Chapter 1 typically fill uniformly in the area of lower metal density. Figure 2.4 shows the 3D problem under consideration. For uniform filling, the metal density and size are constant in a particular region of layout. Therefore in the ROI, we assumed that these structures are periodic along the longitudinal direction ( $z$ ). The spatial interval of this periodic structure (referred to as unit cell size,  $W_{uc}$ ) is determined by metal fill size and density as

$$W_{uc} = \frac{W_m}{\sqrt{D}} \quad (2.7)$$

where  $W_m$  is the metal fill size and  $D$  is the metal fill area density. Figure 2.9 shows a periodic structure with even boundary conditions ( $E_x$  and  $E_y$  exist,  $E_z = 0$ ) at the unit cell walls, at  $z = \pm W_{uc}/2$ . Figure 2.8 shows the interconnect treated as a transmission line with characteristic impedance  $Z_0$ . The additional capacitance due to metal fill is shown as a periodically loaded capacitance,  $C_{mf}$ . We verified that this additional capacitance can be treated as a lumped capacitance as opposed to a cascade of two transmission lines of length  $W_{uc}/2$ , and an admittance of  $j\omega C_{mf}$ . See Appendix A for more details of the periodic structure considerations to the problem. Thus, in this step we reduce the longitudinal number of metal fill to a unit cell consisting of one vertical stack of metal fill, as shown in Fig. 2.9. Note that only the metal fill inside ROI are shown.

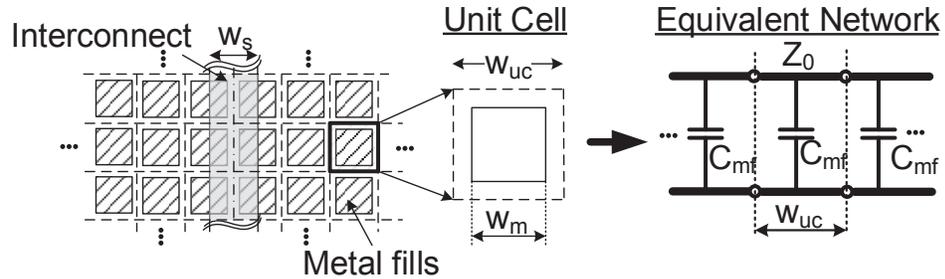


Figure 2.8: Demonstration of periodicity property of metal fill structure.

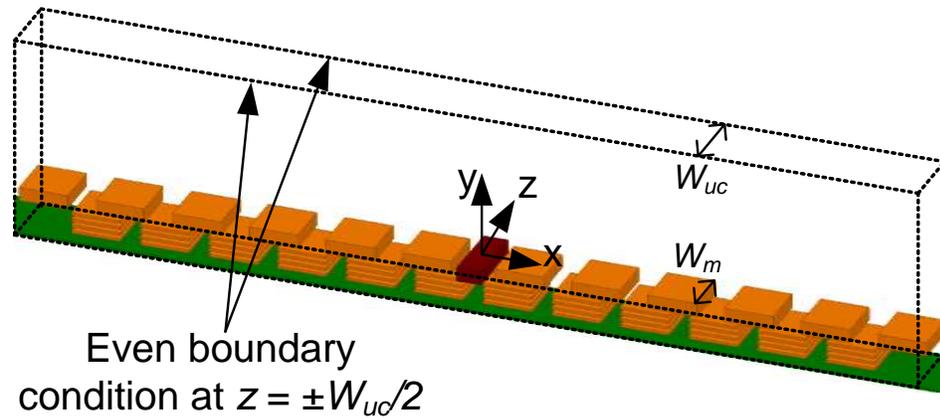


Figure 2.9: Unit cell showing the reduced 3D problem.

### 2.6.3 3D to 2D Problem Reduction

In this subsection, we discuss our approach for transforming the 3D unit cell problem of Fig. 2.9 to two simpler 2D problems. This step further reduces the computational (speed and memory) complexity in solving the problem.

#### Approach

To demonstrate our approach, we provide an example of one metal fill in the unit cell, as shown in Fig. 2.10a. The figure shows an interconnect (node 1) of physical length  $L_p$  and a metal fill (node 2) in the same metal layer. The total increased capacitance

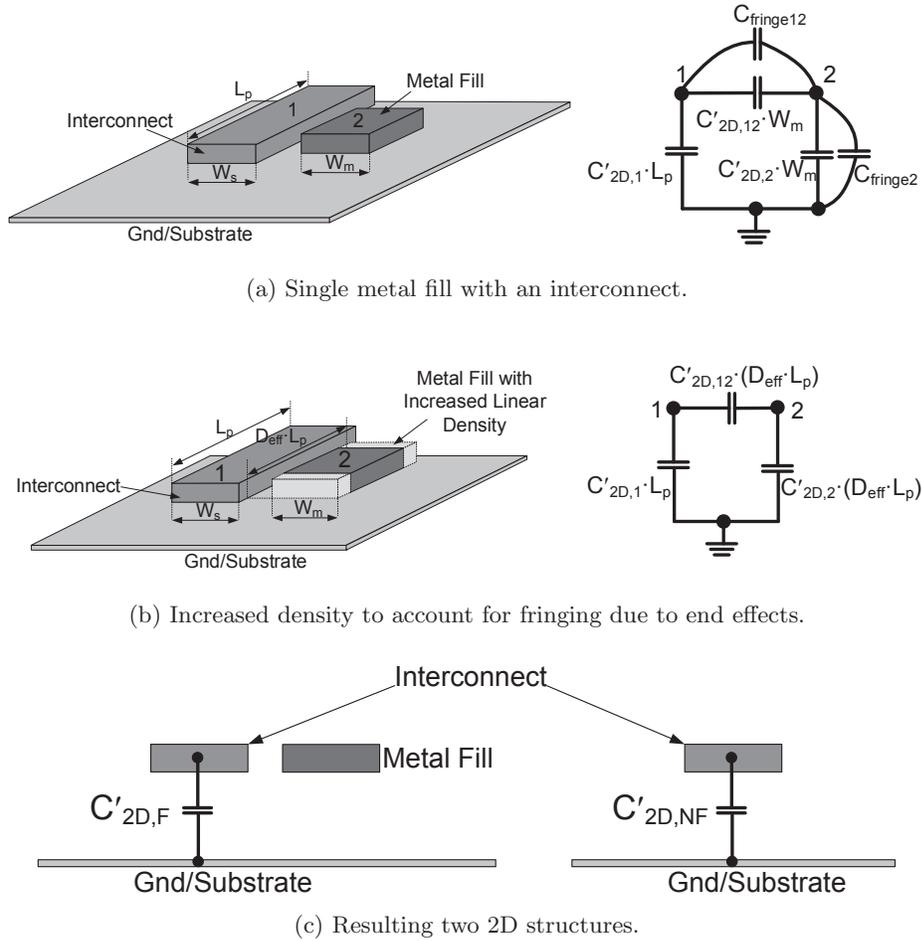


Figure 2.10: Demonstration of problem solution approach.

due to the metal fill has two components: line to metal fill capacitance for length  $L_m$ ,  $C'_{2D,12} \cdot W_m$  (since  $W_m = L_m$ ), and fringing capacitance due to the end effects of the metal fill front and back faces in the  $xy$  plane,  $C_{fringe12}$  and  $C_{fringe2}$ . This structure can be equivalently treated as a line-to-line 2D capacitance with an extended length ( $\Delta L$ ) in the  $z$ -direction that accounts for the fringing. Fig. 2.10b shows the metal fill length extended to  $L_p$  that accounts for this fringing capacitance between the metal fill and the interconnect. After this extension by  $\Delta L$ , the new metal fill length is less than  $L_p$ , i.e.  $L_m + \Delta L < L_p$ . This section of interconnect of length  $L_p - (L_m + \Delta L)$  without metal

fill needs to be accounted by including the capacitance without metal fill.

We define an effective linear density,  $D_{\text{eff}}$ , as the ratio of the extended metal fill length,  $L_m + \Delta L$ , and the physical length,  $L_p$ . As shown in the equivalent circuit in Fig. 2.10b, the capacitance between nodes 1 and 2 is replaced by an equivalent capacitance equal to  $C'_{2\text{D},12}(D_{\text{eff}}L_p)$ . Since the end effects are accounted for, the interconnect line and metal fill can be treated as two 2D problems illustrated in Fig. 2.10c. The per-unit-length capacitance of the equivalent 2D structures are  $C'_{2\text{D},\text{F}}$  (with fill) and  $C'_{2\text{D},\text{NF}}$  (no fill). Finally, the effective total per-unit-length line capacitance of the original 3D structure is approximated as

$$C'_{3\text{D},\text{F}} = D_{\text{eff}}C'_{2\text{D},\text{F}} + (1 - D_{\text{eff}})C'_{2\text{D},\text{NF}}. \quad (2.8)$$

The first term in the equation represents the capacitance due to the extended metal fill and the second term represents the capacitance due to the  $L_p - (L_m + \Delta L)$  section without metal fill. The 2D capacitances  $C'_{2\text{D},\text{F}}$  and  $C'_{2\text{D},\text{NF}}$  of these structures can be efficiently calculated with 2D electrostatic methods or suitable closed-form expressions. The formulation for  $D_{\text{eff}}$  is proposed in the next subsection. This approach using two 2D capacitance calculations and the predetermined formula for  $D_{\text{eff}}$  results in a much faster 3D capacitance calculation compared to the 3D electrostatic simulation.

## Formula Development

In this sub-section, we illustrate the closed-form-expression development for the previously defined effective linear density,  $D_{\text{eff}}$ .  $D_{\text{eff}}$  enables the calculation of the total capacitance of a 3D structure from two 2D per-unit-length capacitance calculations. To develop a general closed-form-expression for  $D_{\text{eff}}$ , we used the setup with a cross-sectional view shown in Fig. 2.5 and described in Section 2.4. The 2D and 3D electrostatic simulations are performed in Ansoft Maxwell [27].

As discussed previously,  $D_{\text{eff}}$  is defined as the ratio of metal fill extended length and physical length of the unit cell,

$$D_{\text{eff}} = \frac{L_m + \Delta L}{L_p}. \quad (2.9)$$

This physical length,  $L_p$ , is equal to the unit cell size due to the periodicity assumption, i.e.  $L_p = W_{uc}$ . Therefore, we rewrite  $D_{\text{eff}}$  as a function of metal fill area density ( $D$ ), and metal fill length ( $L_m$ ) as

$$D_{\text{eff}} = \frac{L_m + \Delta L}{W_{uc}} = \sqrt{D} \left( \frac{L_m + \Delta L}{W_m} \right) = \sqrt{D} \left( 1 + \frac{\Delta L}{W_m} \right) = \sqrt{D} \left( 1 + \frac{\Delta L}{L_m} \right) \quad (2.10)$$

Since we assume the aspect ratio to be 1,  $W_m = L_m$ .

The next step is the determination of  $\Delta L/L_m$ . For this formula development, we systematically vary the interconnect, metal fill, and technology stackup related parameters and compute the  $\Delta L/L_m$  using electrostatic simulations of the 3D unit cell and the 2D reduced problem. Rearranging (2.8),  $D_{\text{eff}}$  can be written as

$$D_{\text{eff}} = \frac{C'_{3\text{D},\text{F}} - C'_{2\text{D},\text{NF}}}{C'_{2\text{D},\text{F}} - C'_{2\text{D},\text{NF}}}. \quad (2.11)$$

Further,  $\Delta L/L_m$  is rewritten as

$$\frac{\Delta L}{L_m} = \frac{D_{\text{eff}}}{D} - 1 = \frac{C'_{3\text{D},\text{F}} - C'_{2\text{D},\text{NF}}}{D (C'_{2\text{D},\text{F}} - C'_{2\text{D},\text{NF}})} - 1. \quad (2.12)$$

$C'_{3\text{D},\text{F}}$  is determined using setup shown in Fig. 2.9,  $C'_{2\text{D},\text{F}}$  is determined using its 2D cross-section at the center of the unit cell, and  $C'_{2\text{D},\text{NF}}$  is calculated using the same 2D cross-section without metal fill. We verified the sensitivity of  $\Delta L/L_m$  as a function of  $D$ ,  $W_m$ ,  $B$ , and  $W_s$  for a single interconnect. From this sensitivity analysis, we formulate  $\Delta L/L_m$  as a function of  $D$  and  $L_m$ .

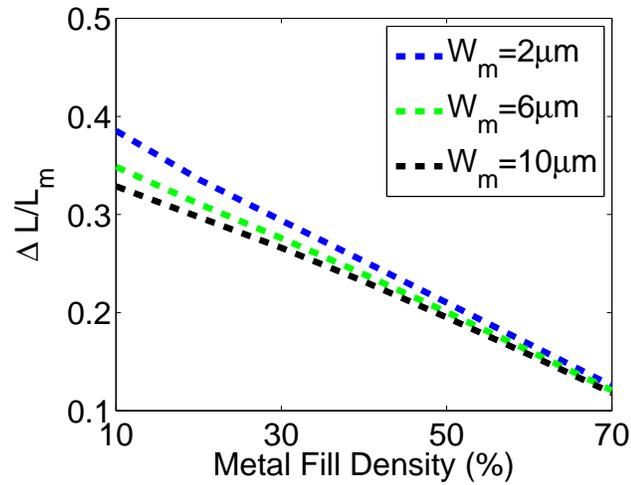
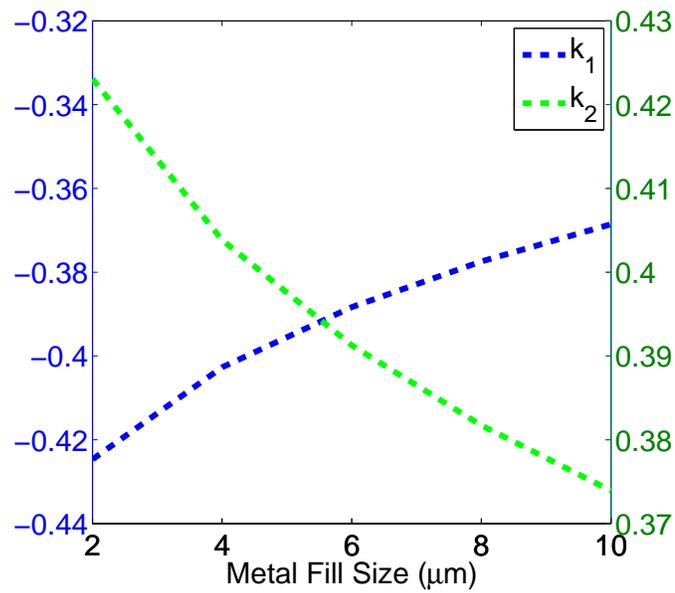
Figure 2.11a shows  $\Delta L/L_m$  as a function of metal fill density. This extended length is approximated as a linear function of metal fill density with empirical coefficients  $k_1$  and  $k_2$  as

$$\frac{\Delta L}{L_m} = k_1 D + k_2. \quad (2.13)$$

The empirical coefficients  $k_1$  and  $k_2$  are plotted in Fig. 2.11b. These coefficients are formulated as a linear function of metal fill size as

$$k_1 = k_3 W_m + k_4 \quad (2.14)$$

$$k_2 = k_5 W_m + k_6. \quad (2.15)$$

(a)  $\Delta L/L_m$  as a function of metal fill density.(b) Coefficients  $k_1$  and  $k_2$  as a function of metal fill size.Figure 2.11: Formulation of  $\Delta L/L_m$  function.

The coefficients  $k_i$  ( $i = 3, 4, 5, 6$ ) are determined using the DIRECT global optimization

algorithm over a range of physical parameters [28].

$$k_3 = 6874.67 \quad (2.16)$$

$$k_4 = -0.4336 \quad (2.17)$$

$$k_5 = -6022.06 \quad (2.18)$$

$$k_6 = 0.4309 \quad (2.19)$$

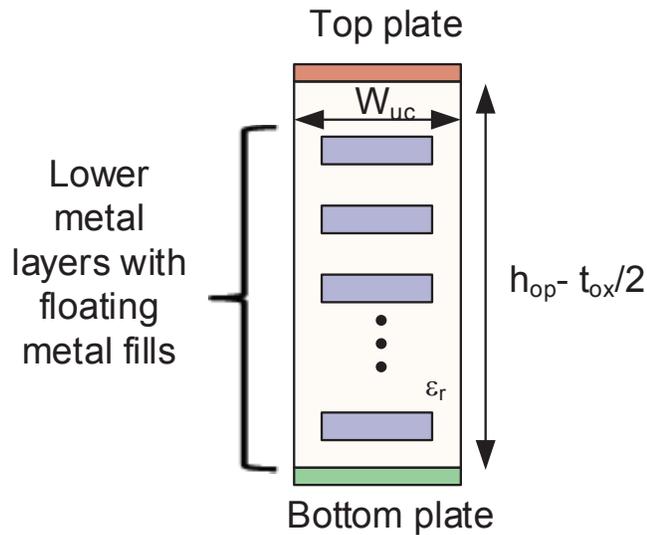
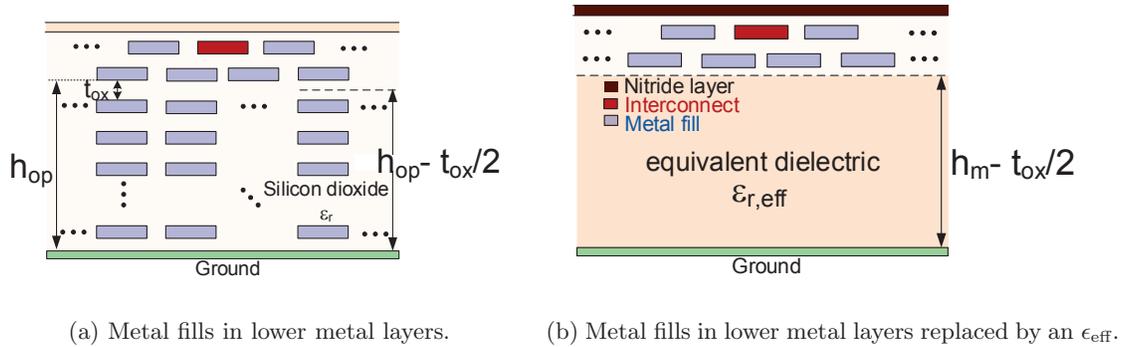
It should be noted that the total interconnect capacitance is a function of the technology stack-up parameters, such as the thicknesses of metal and oxide layers. However, our 2D calculations account for the vertical stack-up related parameters as well as  $W_s$ ,  $W_m$ ,  $D$ , and  $B$ .

#### 2.6.4 Effective Dielectric Constant for Lower Metal Layers

So far in our problem reduction approach, we have transformed the complex 3D problem into two simpler 2D problems. We further reduce the 2D problem with metal fills by approximating the lower layers of metal fill as an effective dielectric medium. The effective material permittivity approach is commonly used in a homogeneous mixture of dielectric and metal particles. Here, the assumption is that the localized electric dipole moment due to the floating metal particles is equivalently replaced by an effective dielectric constant that produces the same polarization.

#### Approach

This method was first applied to the metal fill problem in [23]. In [29], metal fill is replaced by an empirically calculated permittivity by fitting to 3D simulations. In this work, we determine the effective permittivity from a 2D simulation of the equivalent parallel plate configuration shown in Fig. 2.12c. We replace the lower layers of metal fill with an effective dielectric medium of height  $h_m - t_{ox}/2$ , where  $h_m$  and  $t_{ox}$  are height of metal layer below the interconnect and thickness of oxide, respectively, as shown in Fig. 2.12a.



(c) Unit cell of the parallel plate configuration for  $\epsilon_{eff}$  estimation.

Figure 2.12: Metal fill parasitic modeling in lower layers.

## Effective Dielectric Constant Estimation

We use our 2D problem to calculate the effective dielectric constant ( $\epsilon_{eff}$ ) as a function of the dimensions of metal fill. Figure 2.12b shows the lower dielectric medium after replacing it with an effective dielectric constant ( $\epsilon_{eff}$ ). The setup for this calculation is shown in Fig. 2.12b. This calculation for a given process technology is performed using

a 2D electrostatic simulator with a stack of metal fills as

$$\epsilon_{\text{eff}} = \frac{C_{\text{pp}} \cdot (h_{\text{ox}} - t_{\text{ox}}/2)}{\epsilon_0 \cdot W_{\text{uc}}}. \quad (2.20)$$

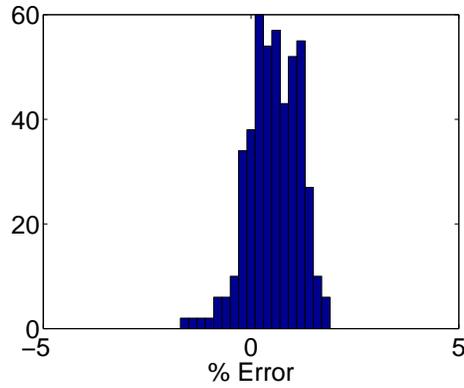
Here  $C_{\text{pp}}$  is the parallel plate capacitance including metal fill obtained using a 2D electrostatic simulator.

## 2.7 Performance

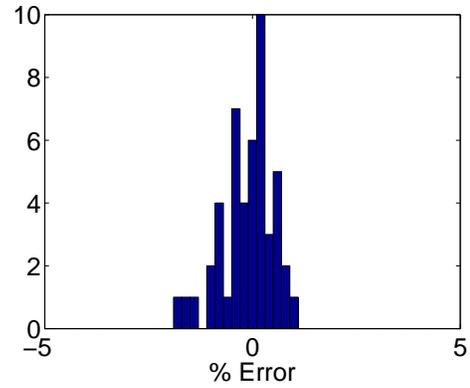
We evaluate the performance of the proposed approach for coplanar multi-conductor transmission lines with metal fill on all the layers. We verified the accuracy of our model by varying the width of the line from 2  $\mu\text{m}$  to 10  $\mu\text{m}$ , the size of metal fill from 2.5  $\mu\text{m}$  to 10  $\mu\text{m}$ , the density from 10 % to 60 %, all in three representative process technologies; 250 nm, 180 nm, and 90 nm. The results are compared with a 3D electrostatic simulator [27] to calculate the error. To achieve confidence in the commercial simulator results, we performed the convergence analysis and compared the results of the simulator with analytical solutions available for canonical geometries. Furthermore, the simulator results are compared with a different simulator appropriate for the problem.

Due to the large variations in the dimensions, we have about 648 error data points. To meaningfully present the error, we show a histogram of the error, where the  $x$ -axis represents the % error, and the  $y$ -axis represents the population of a particular error bin. Ideally, this histogram should be one bar at 0%. Figure 2.13 summarizes the maximum error histogram in capacitance calculations. The 3D to 2D reduction approach is found to be accurate to within 6 % as seen from Fig. 2.13a for a single interconnect and 2.13c for multi-conductor interconnects. Further approximation using  $\epsilon_{r,\text{eff}}$  is accurate to within 9.5 % as seen from Figs. 2.13d and 2.13d. Note for all the charts, the error is centered and highly populated around 0%, and 90% of the error points are within  $\pm 3\%$ .

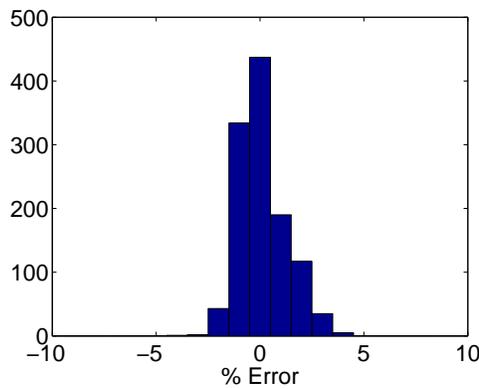
The speed-up in the calculations is determined by comparing the convergence of 3D simulations for a unit cell with our method. Figure 2.14 illustrates the speed-up in the convergence behavior of the method compared with a unit cell 3D electrostatic simulation for four conductors. It can be noted that the 2D simulations converge much faster than the 3D simulations. If 1% of the converged value is considered as a criterion, the speed-up for the first two problem reduction steps (lateral and longitudinal reduction) is 10X



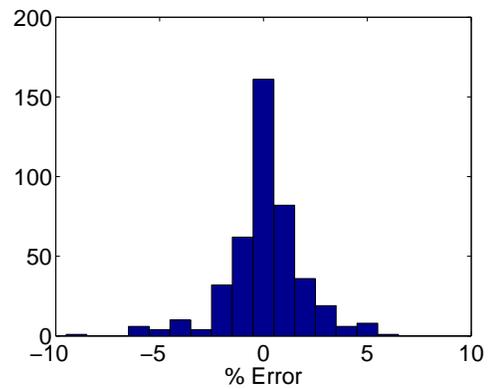
(a) Max. error with lateral and longitudinal problem reduction for single interconnect.



(b) Max. error with lateral, longitudinal, and vertical problem reduction for single interconnect.



(c) Max. error with lateral and longitudinal problem reduction for multi-conductor interconnects.



(d) Max. error with lateral, longitudinal, and vertical problem reduction for multi-conductor interconnects.

Figure 2.13: Summary of capacitance modeling approach: histogram of maximum error.

and further with vertical problem reduction using  $\epsilon_{\text{eff}}$ , the speed-up is 12X. Note that the speed-up numbers are from a commercial simulator. If closed-form expression or an efficient custom simulator are developed, the speed-up numbers can be improved further.

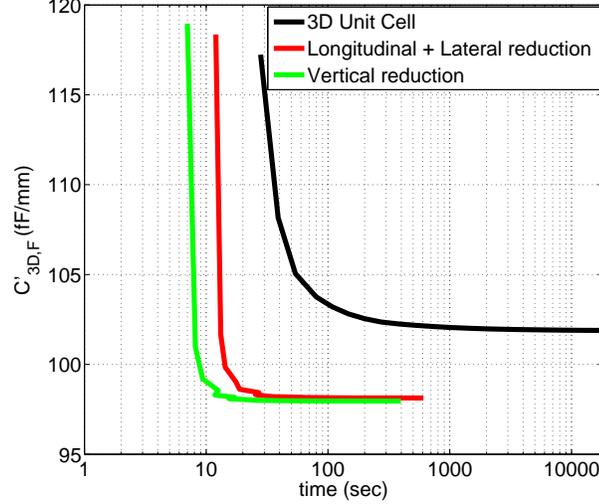


Figure 2.14: Convergence behavior of 3D simulation results as compared to the 2D simplified problem: comparison for four conductor interconnect with  $W_s = 10 \mu\text{m}$ ,  $W_m = 2.5 \mu\text{m}$ ,  $S = 2 \mu\text{m}$ , and  $D = 10 \%$ .

## 2.8 Applications

In this section we demonstrate the versatility of the proposed approach for four important applications. We apply it to calculate the total capacitance in embedded microstrip and coplanar waveguide transmission lines in the presence of square metal fill. Further, we demonstrate the applicability of our approach to slow-wave structures based on embedded microstrip and coplanar waveguide. Historically, slow-wave structures are used to reduce the propagation velocity of travelling waves, e.g., in travelling wave tube (TWT) [30] to match electron beam velocity. Recently, such structures have been utilized for miniaturization of on-chip passive components, commonly referred to as artificial dielectric, for example in [31] for a voltage controlled oscillator and in [32] for on-chip antenna. The basic idea here is to reduce the travelling wave propagation velocity through periodic discontinuities.

### 2.8.1 Embedded Microstrip with Metal Fill

In this subsection, we demonstrate the application of our modeling technique to a set of on-chip transmission line designs with metal fill. We study the trade-off between the slow-wave factor and the reduction in the quality factor of the transmission lines.

To study this trade-off and evaluate the performance of our model, we have considered the designs shown in Table 2.1. The 3D quasi-static simulations are performed in Ansys Maxwell 3D simulator [27]. To determine the distributed resistance and inductance of the transmission lines with metal fill, we first compute these parameters for the case without metal fill [33] and then, determine the increase in resistance and reduction in inductance due to eddy-current loss in metal fill [34]. The p.u.l. capacitance without metal fill is calculated using a 2D simulator and the capacitance with metal fill is calculated using the approach presented in this chapter. For the designs under consideration, we define the slow-wave factor ( $k$ ) and the reduction in quality factor ( $q$ ), as

$$k = \frac{\lambda_f}{\lambda_{nf}} = \frac{\beta_{nf}}{\beta_f} \qquad q = \frac{Q_f}{Q_{nf}} = \frac{\beta_f \alpha_{nf}}{\alpha_f \beta_{nf}}. \quad (2.21)$$

Here,  $\lambda$ ,  $\alpha$ , and  $\beta$  are wavelength, attenuation constant, and phase constant, respectively. The subscripts  $nf$  and  $f$  represent the structures without and with metal fill, respectively. The  $\alpha$  and  $\beta$  parameters are evaluated from the per unit length *RLGC* parameters as

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \quad (2.22)$$

Table 2.1 shows a comparison between model and 3D simulation. The subscripts *sim* and *mod* refer to the parameter calculation using 3D simulations and our models, respectively. As can be seen from the table, our modeling approach is able to estimate  $k$  to within 1.2 % error and  $q$  to within 4 % error for most of the cases and 9.2 % error for one case. The error in the eddy-current loss calculations may be due to the inaccuracy in the loss calculations for metal fill close to the transmission line. This is due to the assumption of uniform magnetic field in [34]. It can be noted that the eddy-current loss in metal fill is non-negligible. For example, for the 50  $\Omega$  design with 2.5  $\mu\text{m}$  and 30 % density, 10 % reduction in the wavelength results in 27 % degradation in the quality factor. Thus, applying our method to on-chip transmission line designs such as [35] and [36], the designs can be optimized, saving fabrication cost and computationally expensive

Table 2.1: Summary of the trade-off between slow-wave factor and quality factor, and model accuracy at 10 GHz.

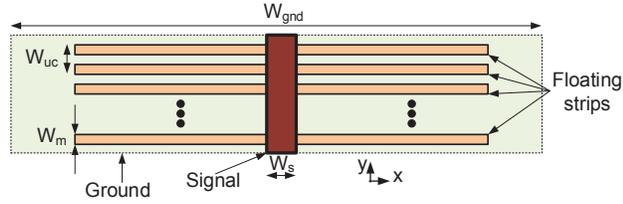
Design ( $Z_0$ - $W_m$ -D)	$\mathbf{k}_{sim}$	$\mathbf{k}_{mod}$	$\mathbf{k}_{err}$ (%)	$\mathbf{q}_{sim}$	$\mathbf{q}_{mod}$	$\mathbf{q}_{err}$ (%)
98 $\Omega$ -10 $\mu\text{m}$ -30 %	0.92	0.92	0.6	0.75	0.75	1.0
98 $\Omega$ -10 $\mu\text{m}$ -60 %	0.87	0.88	0.8	0.61	0.60	0.4
98 $\Omega$ -2.5 $\mu\text{m}$ -30 %	0.91	0.92	1.0	0.78	0.77	0.7
98 $\Omega$ -2.5 $\mu\text{m}$ -60 %	0.88	0.88	0.7	0.67	0.64	3.2
50 $\Omega$ -10 $\mu\text{m}$ -30 %	0.92	0.92	0.4	0.63	0.62	1.0
50 $\Omega$ -10 $\mu\text{m}$ -60 %	0.88	0.88	0.5	0.47	0.47	1.3
50 $\Omega$ -2.5 $\mu\text{m}$ -30 %	0.91	0.92	1.2	0.63	0.61	3.7
50 $\Omega$ -2.5 $\mu\text{m}$ -60 %	0.87	0.88	0.8	0.49	0.45	9.2

full-wave electromagnetic simulations without compromising the accuracy of the results.

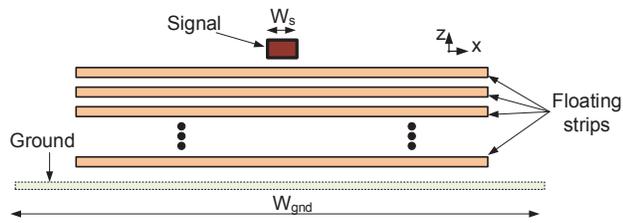
## 2.8.2 Embedded Microstrip Slow-wave Structures

We further applied our modeling approach to floating metal strips used to realize on-chip slow-wave structures in embedded microstrip. These types of structures, if connected to ground or power through transistors, are also referred to as **Digitally Controlled Artificial Dielectric (DiCAD)** [31]. Here, we consider only the artificial dielectric part without the controlling transistors. Figure 2.15 shows the top view of the problem under consideration. As can be seen, the floating strips of metal are orthogonal to the transmission line. This arrangement enhances dipole moment, while, at the same time, it mitigates eddy-current loss. Since the lateral dimension of the strip is large, the fringing electric fields are increased. This increases the electrostatic energy stored in the fields, and therefore increases the dielectric constant. Since the longitudinal dimension of the strip is kept minimal, the surface area that is exposed to the time-varying magnetic fields, is minimal. Therefore, the power loss due to the eddy-currents is minimized.

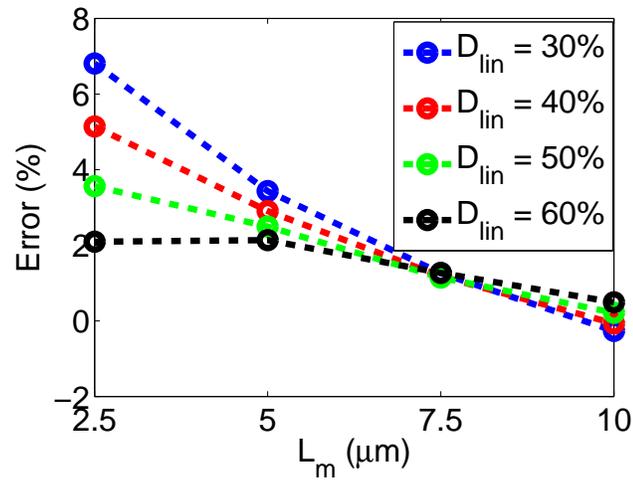
We approach this problem of solving for the capacitance of the DiCAD structure using the method described in this chapter. This 3D problem can be reduced to a simpler 2D problem shown in Fig. 2.15b. Here the metal strip width in the longitudinal



(a) Top view of slow-wave structure.



(b) 2D structure after 3D to 2D transformation.

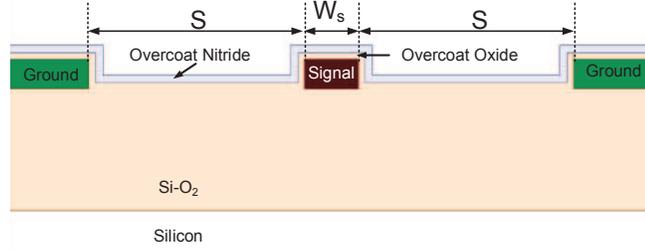


(c) Accuracy performance of our approach.

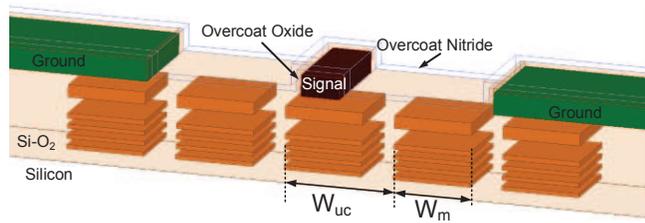
Figure 2.15: Embedded microstrip slow-wave structure.

direction is  $W_m$  and the spacing between the strip is given by a linear density defined as

$$D_{lin} = \frac{W_m}{W_{uc}} \quad (2.23)$$



(a) Cross-sectional view of CPW without metal fill.



(b) 3D view with metal fill.

Figure 2.16: Simulation setup for CPW with  $W_s = 5 \mu\text{m}$ ,  $S = 20 \mu\text{m}$ ,  $W_m = 10 \mu\text{m}$ , and  $D = 50 \%$  in HFSS

where  $W_{uc}$  is the unit cell size as shown in Fig. 2.15a. We use the  $D_{\text{eff}}$  formulation with the same empirical coefficients to calculate the total 3D capacitance. The area density ( $D$ ) in the expression is replaced by a product of the linear densities in the  $x$  and  $y$  directions, respectively. The linear density in the  $x$  direction is assumed to be 1 as the metal strips are much wider than the signal conductor width. The linear density in the  $y$  direction is equal to density  $D_{\text{lin}}$ . The length of metal fill is replaced by  $W_m$ . Figure 2.15c shows the accuracy of this method as a function of floating conductor length ( $W_m$ ) in the longitudinal direction for various densities ( $D_{\text{lin}}$ ). As can be seen from the figure, for this limited set of variations in the physical parameters in a  $0.18 \mu\text{m}$  BiCMOS [37] process technology, the maximum error is within 7 %.

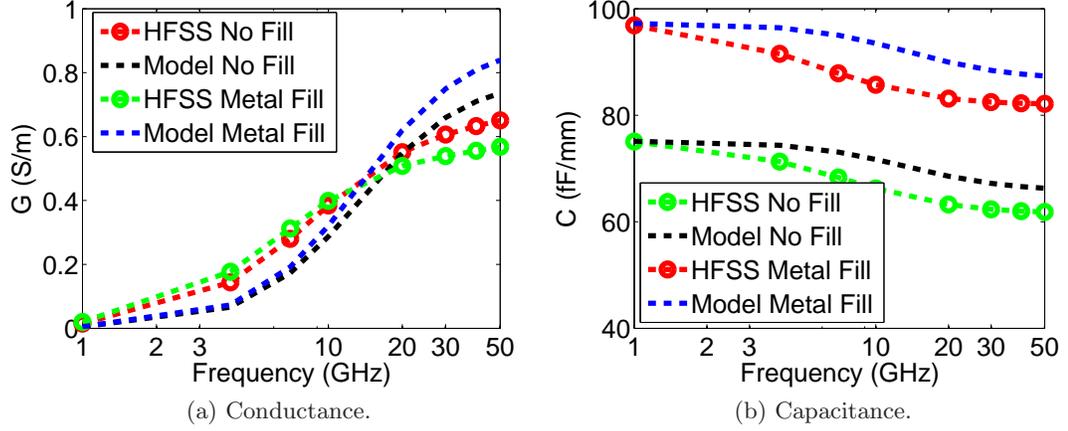


Figure 2.17: Comparison for CPW with  $W_s = 5 \mu\text{m}$ ,  $W_m = 10 \mu\text{m}$ , and  $D = 50\%$

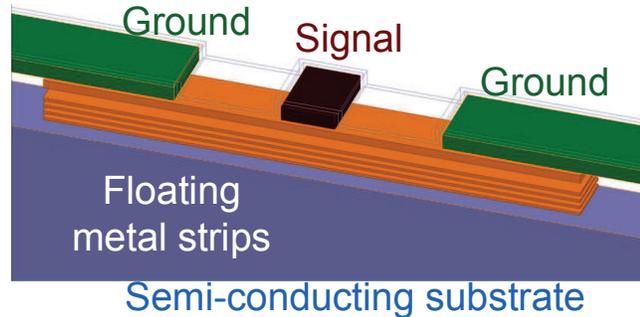
### 2.8.3 Coplanar Waveguide with Metal Fill

At millimeter wave frequencies, the coplanar waveguide (CPW) is a commonly used transmission line structure due to the high quality transmission line elements that can be realized at these high frequencies [38]. The ground on the same layer has the advantage of shielding the signal lines from circuits in close proximity. On the down side, the chip size cost increases rapidly due to the ground signals. This leads to a compromise for shielding vs. the chip size for this type of structures.

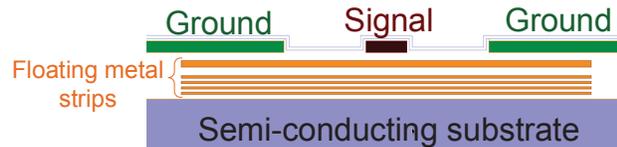
We designed a CPW with signal width of  $5 \mu\text{m}$  and signal to ground spacing of  $20 \mu\text{m}$  in a  $0.18 \mu\text{m}$  technology stackup. The (real part of) characteristic impedance of  $97.2 \Omega$ , attenuation constant of  $0.11 \text{ dB/mm}$ , and phase constant of  $45.5 \text{ rad/m}$  are achieved at  $1 \text{ GHz}$ . The goal of this study is to verify our capacitance modeling technique for a structure for different metal fill fringing field patterns. The metal fills are inserted in the metal layers lower than the layer of the signal and ground conductors<sup>1</sup>. The structure with metal fill incorporates  $10 \mu\text{m} \times 10 \mu\text{m}$  metal fills with  $50\%$  density on all the layers. The metal fills are assumed to be periodic in the lateral and the longitudinal direction.

Figure 2.16 shows the analysis setup for the case without and with metal fill. The signal and ground conductors are laid on the top metal layer to reduce eddy-current

<sup>1</sup>Spacing between the signal and ground is small enough that there will not be any filling for most of the practical cases as long as the filling window size is larger than the spacing.



(a) 3D view of slow-wave structure.



(b) 2D view of slow-wave structure after 3D to 2D transformation.

Figure 2.18: CPW slow-wave structure.

losses. As a part of the fabrication process, the top metal layer is coated with a silicon dioxide layer, silicon nitride, and a passivation layer (not shown). The displacement current in the semi-conducting substrate is non-negligible. We use a C-GC [39] modeling approach to capture this substrate effect. Figure 2.17 shows the results for the per unit length shunt conductance (2.17a) and capacitance (2.17b) comparison between the full-wave simulation [11] and our model. It can be seen from the figure that the change (increase) in *equivalent*  $G(\omega)$  due to metal fill is not significant. Hence the model inaccuracy can be ignored. For the shunt *equivalent*  $C(\omega)$ , the model is able to capture the metal fill effects over a broad range of frequencies. The low frequency capacitance is captured very accurately. Also note that the added 50% density metal fill increases the total capacitance by almost 30% at 1 GHz and by almost 33% at 50 GHz. The error in capturing CPW capacitance without and with metal fill is approximately 7% and 1.2% (root mean square error) and a maximum of 8.2% and 9%, respectively, over the entire band of frequencies.

### 2.8.4 Coplanar Waveguide with Slow-wave Structures

We further applied our technique to on-chip CPW based slow-wave structures, similar to the embedded microstrip based slow-wave structure. Figure 2.18a shows the 3D problem under consideration. In these types of structures, the floating strips are used as a slow-wave structure. Similar to the embedded microstrip problem, we transform this problem into two 2D problems, as shown in Fig. 2.18b. We calculate the total p.u.l. 3D capacitance from the two 2D capacitances using the same  $D_{\text{eff}}$  formulation. We verified the accuracy performance of our approach over a range of physical parameters:  $W_s = (2, 6, 10) \mu\text{m}$ ,  $L_m = (2.5, 5.0, 7.5, 10.0) \mu\text{m}$ ,  $D_{\text{lin}} = (30, 40, 50, 60)\%$  for a  $0.18 \mu\text{m}$  process technology. As shown from the results, the method is accurate to within 8.9%.

## 2.9 Conclusion

In this chapter we presented an efficient approach to account for parasitic capacitance of multi-conductor interconnects in the presence of metal fills. Our capacitance modeling approach is based on reducing the problem complexity in all three physical dimensions. Typical speed-up obtained is 12 fold compared to a 3D electrostatic capacitance simulator. The maximum error in self and mutual capacitance is  $< 6\%$  and  $< 10\%$ , respectively over a wide range of physical parameters. We predict the slow-wave factor of transmission line designs with  $< 1.2\%$  error and Q degradation with  $< 4\%$  error. For an embedded microstrip with floating metal strip formed as a slow-wave structure, the capacitance is predicted to within 7% error. The CPW parasitic capacitance in the presence of metal fill is predicted to within 1% and 9% error at 1 GHz and 50 GHz, respectively. For a CPW with floating metal strip formed as a slow-wave structure, the capacitance is predicted to within 9% error.

## Chapter 3: Metal-Fill-Aware Spiral Inductor Analysis

### 3.1 Introduction

In the previous chapter, we described our approach to model capacitance of multi-conductor interconnects in the presence of metal fill. In this chapter, we present a new approach to model spiral inductors in the presence of metal fill [40]. In the previous chapter we outlined the challenges in modeling the capacitance of interconnects in the presence of metal fill. In this chapter, we extend this discussion to the modeling of metal fill effects in the time-varying electromagnetic fields in Section 3.2. Section 3.3 provides details of the prior research to address some of the challenges. In Section 3.4 we first provide the details of our modeling approach by stating the problem under consideration in terms of the physical parameters and then in terms of the electromagnetic effects to be modeled. This section is followed by a brief overview of our solution approach in Section 3.5. In Section 3.6 we present an overview of the partial-element-equivalent-circuit (PEEC) formulation. In Section 3.7 we provide the details of the partial elements computations without metal fill, and in Section 3.8 we extend this formulation to include metal fill. Finally we state the modified nodal analysis (MNA) formulation for our problem in Section 3.9 and demonstrate the accuracy and computational efficiency of our method in Section 3.10.

### 3.2 Modeling Challenges in Presence of Metal Fill

The passive components designed in radio frequency integrated circuits typically consume a considerable amount of chip area due to their large size. Apart from the size of these components, fabrication on the semi-conducting substrate poses challenges in terms of their efficient numerical analysis. Especially at high frequencies, the skin and proximity effects with metal conductors become significant. Furthermore, the displacement currents and eddy-currents in the semi-conducting substrate are non-negligible at high frequencies. Therefore modeling of such passive components is a challenging task.

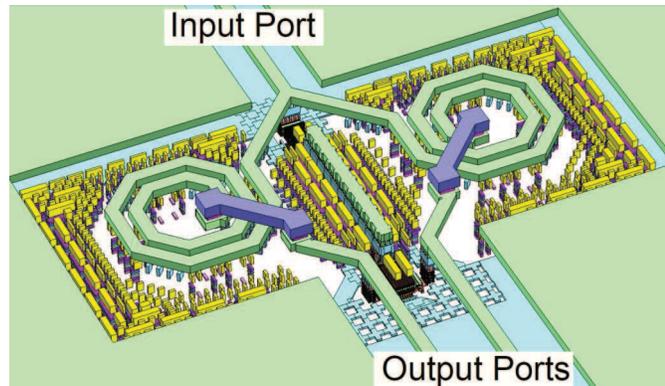


Figure 3.1: 60 GHz Wilkinson power divider in 65 nm CMOS process (taken from [41])

In addition to these modeling challenges, the addition of metal fill underneath these large passive components increases the parasitic capacitance and losses due to the eddy-currents in metal fill. These effects degrade the performance of the components and the circuits using them. Therefore it is important to accurately and efficiently model these effects.

Typically the metal fill size is much smaller than the passive components such as spiral inductors or transformers. Therefore, to meet the metal density requirements, a large number of metal fills are added. For example, for a  $200 \mu\text{m} \times 200 \mu\text{m}$  spiral inductor, approximately 178 metal fills of  $10 \mu\text{m} \times 10 \mu\text{m}$  need to be added in each layer to achieve 50% metal density. If there are 5 metal layers underneath the passive component, about 890 metal fills in total need to be added. Figure 3.1 illustrates the complexity of a typical metal fill problem. It shows a Wilkinson power divider operating at 60 GHz in a 65 nm process with foundry enforced dummy metal structures [41]. To capture the electromagnetic effects at these high frequencies, fine meshing of the geometry is required. Achieving this in a commercial full-wave simulator is a prohibitive task. Therefore, a method to generate fast and accurate circuit models that include the impact of metal fill is needed for a reliable design and optimization of on-chip spiral inductors.

### 3.3 Literature Review

To address some of the challenges, recent research has considered high frequency eddy-current losses in metal fills and their impact on the characteristics of transmission lines [42] and spiral inductors [43]. The model in [43] ignores the skin effect inside the metal fill and, therefore, has limited accuracy over a broad range of frequency. Also, this method ignores the parasitic capacitance effect and, therefore, is further limited in accuracy. Research in [42] approximates the skin effect; however, it is shown to be accurate over only a narrow band of frequency in [34].

### 3.4 Problem Formulation

In this section we discuss the problem formulation first in terms of the physical layout related parameters and technology specific material properties. This is followed by a discussion on the electromagnetic effects that need to be captured for the described problem.

#### 3.4.1 Problem Setup

Figure 3.2 shows the setup of a typical problem to be solved. In this work, we consider a rectangular spiral inductor with metal fill on all layers. The spiral inductor and metal fill geometry can be imported from a graphic database system II (GDSII) file [44]. Alternatively, it can be specified by the dimensions shown in the figure. Here  $D_{ox}$  and  $D_{oy}$  are component dimensions in the x- and y- directions, respectively. The  $D_{ix}$  and  $D_{iy}$  are the x- and y- dimensions, respectively of the inner opening. The spiral inductor turns can be specified in lieu of either the inner or outer dimensions.  $W_s$  and  $S$  are the width of the spiral inductor segment and the spacing between the turns, respectively.  $W_u$  is the width of the underpass. The metal fills are specified by their size,  $W_m$  and the density,  $D$ . Further, the location of each metal fill  $(x, y)$  needs to be specified for capturing the parasitic effects of metal fill.

Figure 3.3 shows a technology cross-section view of the problem under consideration. The passive components are typically placed on the thickest (top layer) layer which is coated with an oxide layer (relative permittivity  $\epsilon_{ox}$ , thickness  $T_{ox}$ ) and nitride layer (relative permittivity  $\epsilon_{ni}$ , thickness  $T_{ni}$ ). Each metal layer has associated conductiv-

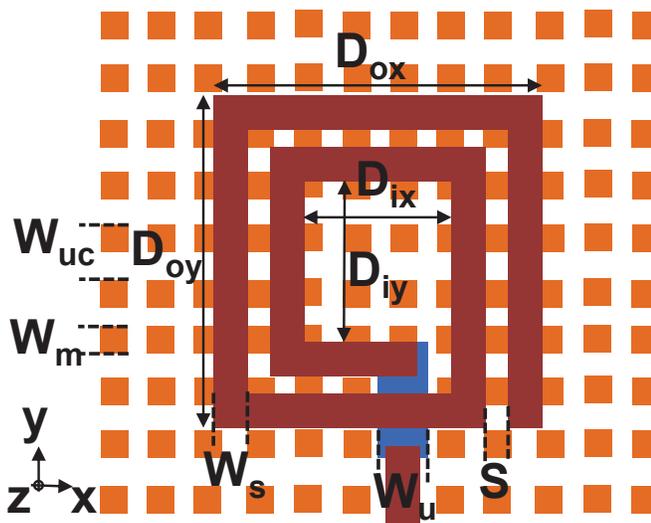


Figure 3.2: Problem setup with dimensions of spiral inductor and metal fills under consideration.

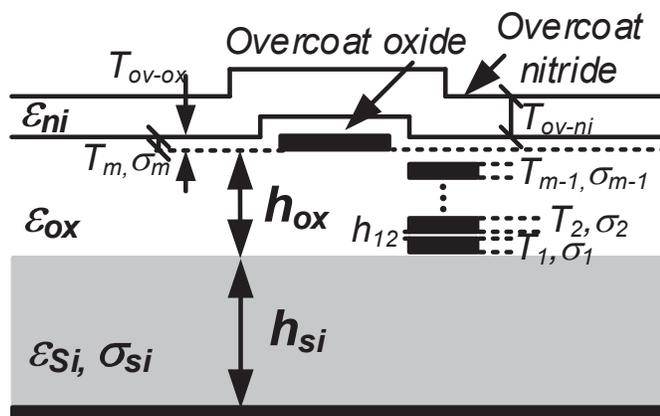


Figure 3.3: Typical process technology related parameters.

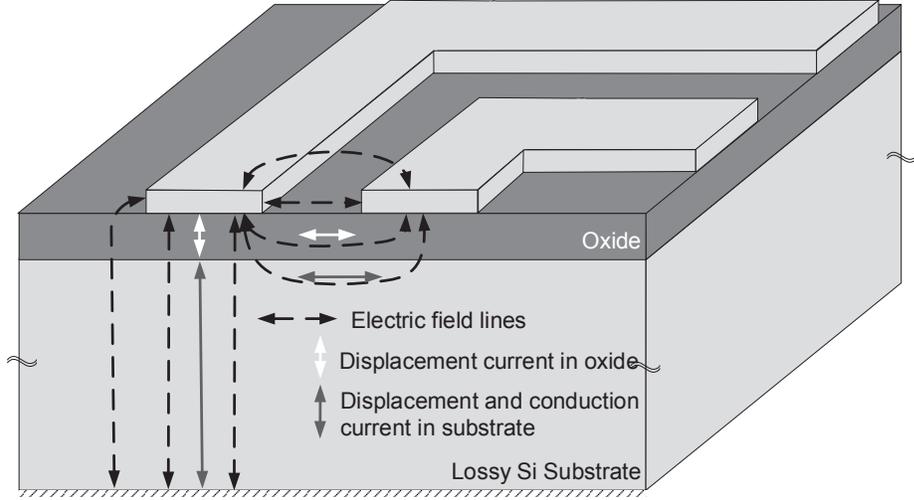


Figure 3.4: Cross-sectional view of a spiral inductor corner and qualitative demonstration of the electric fields. (Reproduced from [45])

ity  $(\sigma_1, \sigma_2, \dots, \sigma_m)$  and thickness  $(T_1, T_2, \dots, T_m)$ . The inter-layer dielectric (ILD) has associated conductivity  $(\epsilon_1, \epsilon_2, \dots, \epsilon_m)$  and thickness  $(h_{12}, h_{23}, \dots, h_{m-1,m})$ . The semi-conducting substrate has a thickness of  $h_{\text{si}}$ , conductivity of  $\sigma_{\text{si}}$ , and permittivity  $\epsilon_{\text{si}}$ .

### 3.4.2 Electromagnetic Effects to be Captured

The time-varying charges and currents in the inductor give rise to time-varying electric and magnetic fields. Figure 3.4 illustrates the electric fields in a cross-sectional view of a rectangular spiral inductor. The time-varying electric fields cause displacement currents in the substrate  $(\partial \bar{D} / \partial t)$ . Due to the inhomogeneity of the problem, there are surface charges at the boundary of the oxide and the lossy substrate. Figure 3.4 shows the presence of electric fields between the inductor and substrate, and also the presence of electric fields between windings as the electric potential varies along the spiral inductor turns.

The impressed time-varying current in the structure produces a time-varying magnetic field in each turn. The magnetic fields in each turn interact with each other as

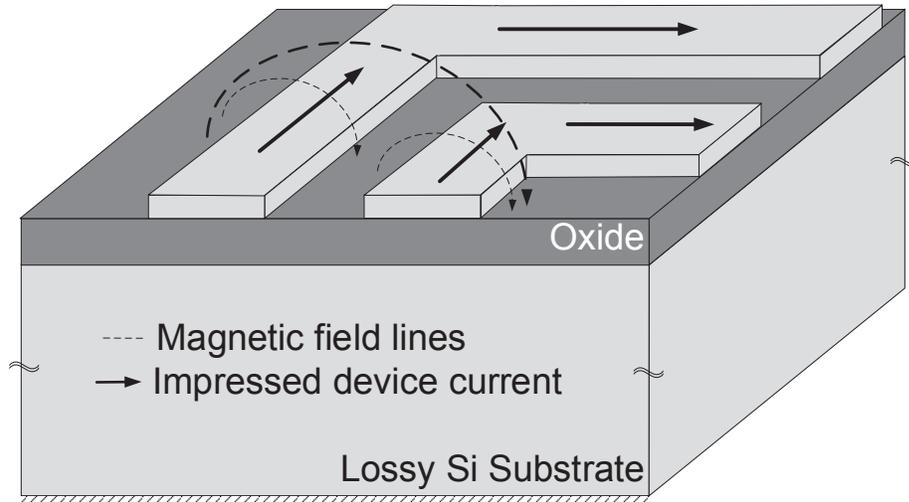


Figure 3.5: Cross-sectional view of a spiral inductor corner and qualitative demonstration of the magnetic fields. (Reproduced from [45])

illustrated in Figure 3.5. Due to the time-varying magnetic fields inside the conductor, an electromotive force (emf) is induced that opposes the magnetic field, and hence the current producing it. This causes the currents to flow more towards the edge (or skin) of the conductor. This is referred to as the skin-effect. For a neighboring conductors, the coupled magnetic field due to current in the neighboring conductor creates an emf. This emf produces eddy-currents opposing the magnetic fields due to the current in the neighboring conductor. This leads to current crowding toward the outer edges of the coupled conductors and is referred to as the proximity effect. Both of these frequency dependent effects change the current density in the spiral inductor and need to be captured by the models.

Now, we briefly discuss the impact of metal fill that needs to be accounted for in the model. As metal fill is inserted into the spiral inductor's electromagnetic fields, it alters the fields. Figure 3.6 illustrates the changes in the electric fields due to metal fill. These floating structures in the fringing fields or the fields underneath the spiral inductor, cause additional capacitive coupling as described in the previous chapter. There is also a change in the fields between the windings. Both of these effects need to be considered.

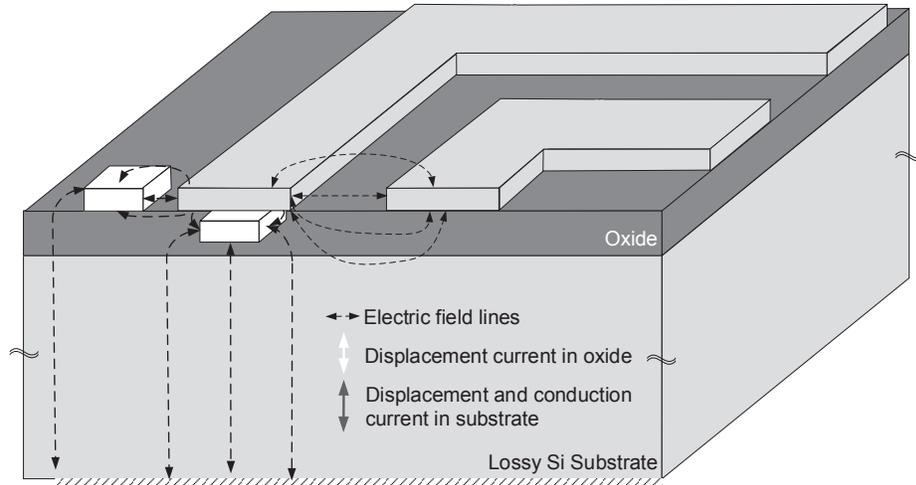


Figure 3.6: Cross-sectional view of a spiral inductor corner and qualitative demonstration of the electric fields in the presence of metal fill. (Reproduced from [45])

When metal fills are placed in the time-varying magnetic field of a component such as a spiral inductor, eddy currents are induced in the metal fill. Figure 3.7 illustrates the eddy current loops in the metal fill. These eddy currents reduce the inductance and increase the series resistance. These effects are frequency dependent, increasing the losses and degrading the quality factor of the spiral inductor.

### 3.5 Overview of Solution Approach

Figure 3.8 shows an overview of the solution approach presented here. There are three representative parts in the approach: segmentation and meshing of the physical structure, calculation of the partial elements, and the modified nodal analysis. To address the challenges of capturing the metal fill parasitic effects in large passive components such as spiral inductors, we have developed a solution approach that incorporates empirical methods for capturing the capacitive [46] and inductive parasitic effects [34]. The simulator is based on the partial element equivalent circuit (PEEC) modeling technique [47] in which the electromagnetic problem is represented by partial circuit elements. The modified nodal analysis (MNA) [48] is then used to solve the circuit problem. Here,

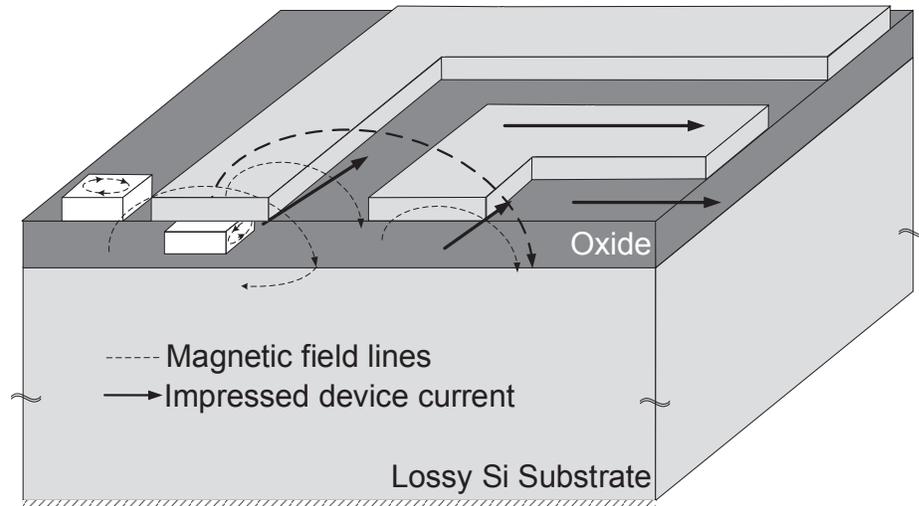


Figure 3.7: Cross-sectional view of a spiral inductor corner and qualitative demonstration of the magnetic fields in the presence of metal fill. (Reproduced from [45])

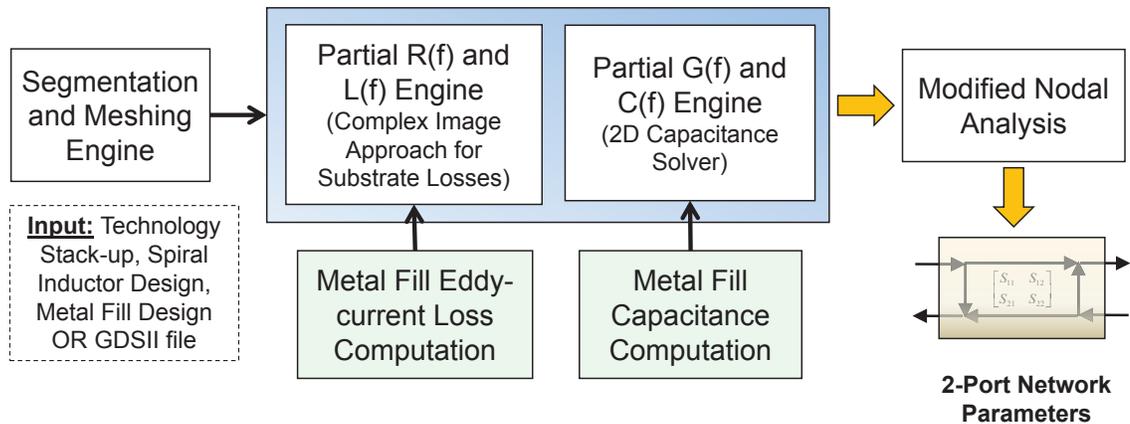


Figure 3.8: Overview of the solution approach.

we generate network parameters over the frequency range of interest. In the spirit of equivalent circuit representation, we also model the metal fill parasitic effects in terms of their equivalent resistance, inductance, conductance and capacitance. The segmented and meshed geometry equivalent partial resistance and inductance circuit elements are

calculated using closed-form expressions [49]. The semi-conducting substrate effects are efficiently captured using the complex image approach [50]. The partial capacitance and conductance is calculated from corresponding 2D capacitances.

## 3.6 Partial Element Equivalent Circuits Technique

In this section we provide a detailed formulation of the PEEC method. First we describe the electric field integral equation (EFIE) formulation of PEEC followed by the partial circuit element formulation through discretization of the EFIE.

### 3.6.1 Partial Element Equivalent Circuits Method

The methods for solving a full-wave problem can be broadly classified into the differential equation (DE) based and the integral equation (IE) based methods. For DE methods, the finite-difference-time-domain (FDTD) and the finite element method (FEM) are commonly used for time domain and frequency domain analyses, respectively [51]. FDTD method spatially discretizes the physical problem and Maxwell's equations are solved for electric and magnetic fields in the time domain. The matrix representing a set of equations to be solved in this method is very sparse resulting in efficient solution of the problem. The advantage of these methods is efficiency with which complex problems with spatially varying properties are modeled accurately. The disadvantage of such methods is the non-triviality or the difficulty in frequency domain analysis of the circuits. For the FEM a complex problem can be efficiently solved, however, the large number of unknowns in FEM is a limitation.

Traditional integral equation (IE) based solutions such as the method of moments (MoM<sup>1</sup> [52])<sup>2</sup> discretize the problem of volumes and surfaces into canonical elements to represent the unknown charge or current densities using a set of known basis functions. These methods are limited due to the denser matrices that need to be inverted, which requires larger computational resources in MoM [51].

In contrast to the traditional IE methods, the PEEC method represents the integral

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<sup>1</sup>Also referred as the boundary element method (BEM) in applied mathematics [15]

<sup>2</sup>In applied mathematics, the MoM is used for discretizing both the DE and IE types of boundary value problems. However, here we refer to IE type of problem, especially concerning the electric field IE (EFIE).

equations corresponding to each discretized cell as equivalent circuit elements, including partial resistance, partial inductance, coefficient of potential, and controlled voltage and current sources. Thus the problem is converted from the physical representation to a circuit representation. Further, this large circuit problem with passive elements and controlled sources are solved using circuit analysis technique such as the modified nodal analysis (MNA) or general tableau formation.

In this work, we adopt the PEEC formulation for its formulation of converting a complex physical problem into an equivalent circuit that can be efficiently solved with circuit analysis techniques. Methods such as MoM and FEM require spatial discretization of the entire problem, which results in a large number of unknowns. As discussed in Section 3.2, the discretization of metal fill leads to a prohibitive problem complexity. In contrast, PEEC can be used to represent the metal fill caused additional resistance, capacitance, and inductance in a circuit element form. This leads to an efficient solution of the problem.

### 3.6.1.1 PEEC Formulation

The PEEC formulation is based on the EFIE formulation of the Maxwell's equations. In PEEC-EFIE, the total electric field at a point is expressed as a superposition of the fields due to source charge and current densities [47]. The electric field at any point in a conductor is given as the superposition of the incident field and the fields due to the currents in the conductor (current density  $\bar{J}^C(\bar{r}, t)$ ) and charge on the conductor as

$$\bar{E}_0(\bar{r}, t) = \frac{\bar{J}^C(\bar{r}, t)}{\sigma} + \frac{\partial \bar{A}(\bar{r}, t)}{\partial t} + \nabla \Phi(\bar{r}, t) \quad (3.1)$$

where  $\bar{J}^C(\bar{r}, t)$  is the conduction current through the conductor. Using Ampere's law, the total current in the problem can be written as

$$\nabla \times \bar{H}(\bar{r}, t) = \bar{J}^C(\bar{r}, t) + \epsilon_0(\epsilon_r - 1) \frac{\partial \bar{E}(\bar{r}, t)}{\partial t} + \epsilon_0 \frac{\partial \bar{E}(\bar{r}, t)}{\partial t} = \bar{J}(\bar{r}, t) + \epsilon_0 \frac{\partial \bar{E}(\bar{r}, t)}{\partial t}, \quad (3.2)$$

where the second term includes the polarization current and the third term is the current due to free space charges. The second term in 3.1 represents the electric fields due to the time-varying external magnetic field outside the conductor. The vector magnetic

potential can be written as [53]

$$\bar{A}(\bar{r}, t) = \mu \int_{v'} G^A(\bar{r}, \bar{r}') \bar{J}(\bar{r}', t_d) dv' \quad (3.3)$$

where  $G^A(\bar{r}, \bar{r}')$  is an appropriate Green's function and  $J(\bar{r}', t_d)$  is the total current, and  $t_d = t - R/v_p$ . Here  $t_d$  is referred to as retarded time (and the potential as retarded potential),  $R$  is the distance between the source point  $(x', y', z')$  and observation point  $(x, y, z)$ , and  $v$  is the velocity of the propagating signal equal to  $1/\sqrt{\mu\epsilon}$  in a homogeneous medium.

The third term in (3.1) is the gradient of the scalar electric potential. This scalar electric potential can be given as

$$\Phi(\bar{r}, t) = \frac{1}{\epsilon} \int_{v'} G^\Phi(\bar{r}, \bar{r}') \rho(\bar{r}', t_d) dv'. \quad (3.4)$$

Thus the total electric field can be rewritten as a summation of the integrals forming the EFIE as

$$\begin{aligned} \bar{E}_0(\bar{r}, t) = & \frac{\bar{J}^C(\bar{r}, t)}{\sigma} + \mu \int_{v'} G^A(\bar{r}, \bar{r}') \frac{\partial \bar{J}(\bar{r}', t_d)}{\partial t} dv' \\ & + \mu \epsilon_0 (\epsilon_r - 1) \int_{v'} G^A(\bar{r}, \bar{r}') \frac{\partial^2 \bar{E}(\bar{r}', t_d)}{\partial t^2} dv' + \nabla \left[ \frac{1}{\epsilon} \int_{v'} G^\Phi(\bar{r}, \bar{r}') \rho(\bar{r}', t_d) dv' \right]. \end{aligned} \quad (3.5)$$

This EFIE, along with the continuity equation,

$$\nabla \cdot \bar{J}(\bar{r}', t_d) = -\frac{\partial \rho(\bar{r}', t_d)}{\partial t} \quad (3.6)$$

complete the necessary equations for the solution of charge ( $\rho(\bar{r}', t_d)$ ) and current ( $\bar{J}(\bar{r}', t_d)$ ) densities.

### 3.6.2 Discretization and Partial Elements

Similar to the MoM approach, the discretization of the EFIE is done through approximation of the unknowns in terms of a combination of local basis functions. Specifically for PEEC, a pulse basis is utilized, assuming the charge density and current density to

be constant over a discretized surface and volume, respectively.

For the  $k^{th}$  conductor with  $N_{\gamma k}$  discretizations in the cross-sectional dimension, the  $\gamma$  component of the current density is expressed as

$$J_{\gamma k}(t') = \sum_{n=1}^{N_{\gamma k}} \Psi_{\gamma nk}(\bar{r}) J_{\gamma nk}(t_n) \quad (3.7)$$

where  $\gamma \in (x, y, z)$ , and  $nk$  represents  $n^{th}$  element in  $k^{th}$  conductor.  $t_n = t - |\bar{r} - \bar{r}_n|/v$  is an approximation of  $t'$  and

$$\Psi_n(\bar{r}) = \begin{cases} 1 & \gamma nk^{th} \text{ cell} \\ 0 & \text{otherwise,} \end{cases}$$

Similarly, the charge density on the surface of the  $k^{th}$  conductor with  $M$  discretizations is expressed as

$$\rho_k(t_m) = \sum_{m=1}^{M_k} \psi_{mk}(\bar{r}) \rho_{mk}(t_m), \quad (3.8)$$

where  $t_m = t - |\bar{r} - \bar{r}_m|/v$  is an approximation of  $t'$  and

$$\psi_n(\bar{r}) = \begin{cases} 1 & \gamma nk^{th} \text{ cell} \\ 0 & \text{otherwise,} \end{cases}$$

Substituting these expansions in the EFIE for  $K$  spiral inductor segments,

$$\begin{aligned} \bar{E}_0(\bar{r}, t) = & \frac{\bar{J}^C(\bar{r}, t)}{\sigma} + \sum_{k=1}^K \sum_{n=1}^{N_{\gamma k}} \mu \int_{v_k} G^A(\bar{r}, \bar{r}') \frac{\partial \Psi_{\gamma nk}(\bar{r}) J_{\gamma nk}(t_n)}{\partial t} dv' \\ & + \sum_{k=1}^K \mu \epsilon_0 (\epsilon_r - 1) \int_{v_k} G^A(\bar{r}, \bar{r}') \frac{\partial^2 \bar{E}(\bar{r}', t_d)}{\partial t^2} dv' \\ & + \sum_{k=1}^K \sum_{m=1}^{M_k} \nabla \left[ \frac{1}{\epsilon} \int_{s_k} G^\Phi(\bar{r}, \bar{r}') \psi_{mk}(\bar{r}) \rho_{mk}(t_m) ds' \right]. \end{aligned} \quad (3.9)$$

Next, Galerkin's method [54] is used to enforce the EFIE at each cell. In this particular method, the testing functions are the same as the basis functions. Therefore, applying

the procedure at one cell on a conductor means the following operation

$$\frac{1}{a_\gamma} \int_{v_\gamma} f(\bar{r}) dv = \frac{1}{a_\gamma} \int_{a_\gamma} \int_{l_\gamma} f(\bar{r}) dl da, \quad (3.10)$$

where  $v_\gamma$ ,  $a_\gamma$ , and  $l_\gamma$  are the volume, area, and length of the cell, respectively. It is the point in the formulation, where we assume no external incident field, making the left hand side of the EFIE equal to zero. Enforcing the EFIE on the  $l^{th}$  cell,

$$\begin{aligned} 0 = & \int_{v_l} \frac{\bar{J}^C(\bar{r}, t)}{\sigma} dv_l + \sum_{k=1}^K \sum_{n=1}^{N_{\gamma k}} \mu \int_{v_l} \int_{v_k} G^A(\bar{r}, \bar{r}') \frac{\partial J_{\gamma nk}(t_n)}{\partial t} dv' dv_l \\ & + \sum_{k=1}^K \mu \epsilon_0 (\epsilon_r - 1) \int_{v_l} \int_{v_k} G^A(\bar{r}, \bar{r}') \frac{\partial^2 \bar{E}(\bar{r}', t_d)}{\partial t^2} dv' dv_l \\ & + \sum_{k=1}^K \sum_{m=1}^{M_k} \int_{v_l} \nabla \left[ \frac{1}{\epsilon} \int_{s_k} G^\Phi(\bar{r}, \bar{r}') \rho_{mk}(t_m) ds' dv_l \right]. \end{aligned} \quad (3.11)$$

Now we interpret each of the terms in the above IE as circuit elements. In the first term, on the  $l^{th}$  cell, the resistance of the cell can be written as

$$R_l = \frac{l_l}{\sigma a_l} \quad (3.12)$$

and the current through the cross-sectional area  $a_l$  as  $J^C = I_l/a_l$ . Therefore the first term on the right hand side of the equation is interpreted as a voltage drop of  $v_r = R_{\gamma l} I_{\gamma l}$ . The second term can be rewritten as

$$v_l = \left[ \sum_{k=1}^K \sum_{n=1}^{N_{\gamma k}} \frac{\mu}{a_l a_{\gamma nk}} \int_{v_l} \int_{v_k} G(\bar{r}, \bar{r}') dv' dv_l \right] \frac{\partial I_{\gamma nk}(t_n)}{\partial t} \quad (3.13)$$

where the term in the square bracket is recognized as a partial inductance [55]. Unlike the inductance which is always defined for a closed loop of wires, the partial inductance is defined for incomplete (open) loop of wires or a finite length segment of wires. The partial inductance between two segments with cross-sectional areas  $a_k$  and  $a_m$  perpendicular to the current flow going from  $b_k$  to  $c_k$  and  $b_m$  to  $c_m$ , respectively,  $(b_{k,m}, c_{k,m}) \in (x, y, z)$  is

$$L_{p_{km}} = \frac{\mu}{4\pi a_k a_m} \int_{a_k} \int_{a_m} \int_{b_k}^{c_k} \int_{b_m}^{c_m} \frac{|\bar{d}\bar{l}_k \cdot \bar{d}\bar{l}_m|}{r_{km}} da_k da_m \quad (3.14)$$

where  $r_{km}$  is the euclidean distance between the two segments. Thus  $v_l = L_{p_{km}} \partial I / \partial t$  forms a voltage across a partial inductance  $L_{p_{km}}$ .

The third term in the IE is the electric field inside a dielectric region with relative permittivity  $\epsilon_r$ . This term, after integration, can be referred to as a partial capacitance in series with a partial inductance to capture coupling between other cells [55].

The last term of the IE is identified as a capacitive coupling. Rewriting the gradient operator as a partial derivative, the last term becomes

$$\frac{1}{\epsilon} \sum_{k=1}^K \sum_{m=1}^{M_k} \int_{v_l} \left[ \frac{1}{\partial \gamma} \int_{s_k} G^\Phi(\bar{r}, \bar{r}') \rho_{mk}(t_m) ds' \right] dv_l. \quad (3.15)$$

The term in the square brackets can be approximated as

$$\int_{v_l} \frac{\partial}{\partial \gamma} F(\gamma) dv_l \approx a_l \left( F\left(\gamma + \frac{\gamma}{2}\right) - F\left(\gamma - \frac{\gamma}{2}\right) \right). \quad (3.16)$$

using a finite difference approximation. It indicates the shift in the half cell size between inductive cells and capacitive cells. When this result is applied to the IE with  $Q_{mk} = \rho_{mk} a_{mk}$ , the Green's functions associated with the positive and negative end of the  $l^{th}$  cell are abbreviated as  $G^\Phi(\bar{r}^+, \bar{r}')$  and  $G^\Phi(\bar{r}^-, \bar{r}')$ , respectively. Therefore the last term can be rewritten as

$$v_c = \frac{1}{\epsilon} \sum_{k=1}^K \sum_{m=1}^{M_k} Q_{mk}(t_m) \left[ \int_{s_k} G^\Phi(\bar{r}_l^+, \bar{r}') ds' - \int_{s_k} G^\Phi(\bar{r}_l^-, \bar{r}') ds' \right] dv_l. \quad (3.17)$$

The partial coefficients of potential can be represented as

$$pp_{ij} = \frac{1}{a_j} \int_{s_j} G^\Phi(\bar{r}, \bar{r}') ds'. \quad (3.18)$$

In general, a potential  $\Phi_i$  on a conductor with charge  $Q_i$  can be represented by using

the coefficient of potentials as

$$\Phi_i(t) = \sum_{j=1}^n pp_{ij} Q_j(t - t_d). \quad (3.19)$$

If the retardation effect is ignored, this formulation can be represented in its conventional capacitance equivalent circuit. However, for the retarded potentials, it is represented in terms of the partial coefficients of potentials and voltage source [56] as

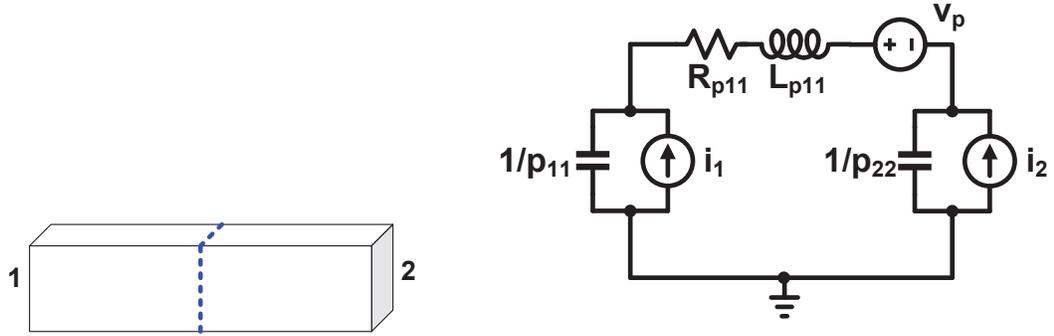
$$v_i^C(t) = \sum_{j \neq i} \frac{p_{ij}}{p_{jj}} \Phi'_j(t_d). \quad (3.20)$$

Similarly, for the inductive coupling, a voltage source in series with the partial self inductance can capture the coupling between two conductors as

$$v_i^L(t) = \sum_{j \neq i} \frac{L_{p_{ij}}}{L_{p_{jj}}} \Phi'_{ij}(t_d) \quad (3.21)$$

Fig. 3.9a shows a rectangular conductor under consideration for the purpose of exemplifying the terms in the IE. This conductor has two nodes at the ends of the conductor. The partitioning for the coefficient of potential is shown by the dotted line. The partition reflects the shift by  $\gamma/2$  identified in the previous equations. Figure 3.9b shows the equivalent circuit for the scenario of a single conductor. Referring back to (3.11), the first term on the right hand side is represented by  $R_{p11}$ , the second term is represented by  $L_{p11}$ . For a multi-conductor scenario, a voltage source in series is more appropriate to account for magnetic coupling between the  $k^{th}$  and  $m^{th}$  cell. The third term does not exist since no dielectric is present; however, in the case of a dielectric block, a series combination of partial capacitance and partial inductance realize the equivalent circuit as discussed before. The last term is represented by  $p_{11}$  and  $p_{22}$  in shunt with a current source. The coefficient of potential represents the capacitance for partition 1 and 2, and the current sources  $i_1$  and  $i_2$  represent the capacitive coupling.

Thus, the EFIE is interpreted in terms of the partial resistance, inductance, conductance, and capacitance. Next we discuss our specific implementation of the method.



(a) Single conductor under consideration (b) Partial elements corresponding to the integral equation

Figure 3.9: Equivalent circuit model for a conductor with two nodes.

### 3.7 Partial Element Computations without Metal Fill

We will discuss the computations of partial elements in this section. In this work, we will not consider the retarded time (assuming  $R \ll v_p \rightarrow t_d \approx t$ ). Also, we will assume the segmentation in such a way that the current and charge densities vary only in the lateral and vertical dimensions and ignore the variations in the longitudinal dimension for each cell. Also, we represent the magnetic coupling between the mesh elements in terms of partial mutual inductance and the electric coupling in terms of the partial capacitances.

#### 3.7.1 Partial Resistance and Inductance

We partition the spiral inductor geometry into segments as shown in Fig. 3.10 and each segment into rectangular conductors. The amount of discretization is a trade-off between the computational resources vs. the accuracy achieved. The segmentation for the equivalent circuit calculation is performed based on the corner discontinuities observed for the spiral inductor components. The corners create discontinuities in the current direction and therefore the magnetic field produced by it. This changes the flux linkages with other segments and therefore partial mutual inductances. The maximum length of a segment or whether the segment is to be sub-divided into two segments is determined from the minimum wavelength as  $(\sqrt{\mu\epsilon}f_{max})^{-1}/10$ . For example, for a

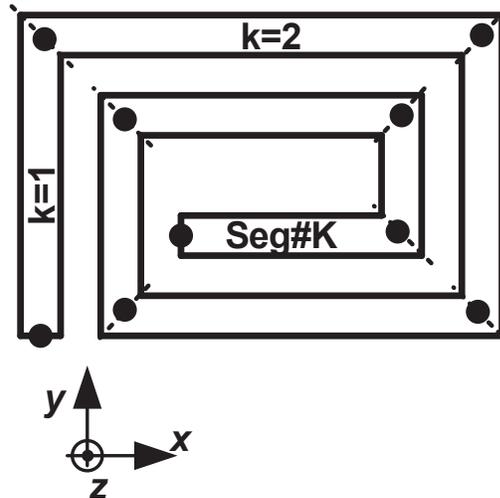


Figure 3.10: Segmentation for the spiral inductor for partial resistance and inductance computation.

spiral inductor outer dimension of  $200 \mu\text{m}$ , if a typical on-chip dielectric material ( $\text{SiO}_2$ ) is considered with a dielectric constant of  $\approx 4$ , the maximum frequency at which the largest segment can be considered without splitting is  $\approx 75 \text{ GHz}$ .

We also mesh the cross-section of each segment to capture the skin effect in the conductors and the proximity effect due to nearby segments. Each mesh element assumes a uniform current density in the cross-section. This is a rectangular pulse function approximation for each of the conductors. The uniform meshing yields optimization in terms of the partial element computations. Since the width and thickness of each rectangular conductor are the same, the self partial inductance values can be reused throughout the segments. This reduces the computing resources required for the partial self term calculations. However, the amount of computing resources required for the partial mutual inductance terms is large. Each partial mutual inductance calculation is a summation of 64 self partial inductance calculations as shown in [49]. The meshing can

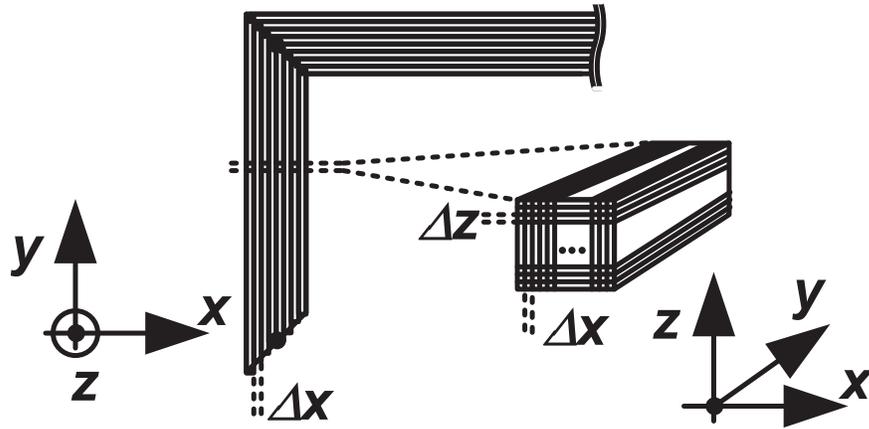


Figure 3.11: Meshing for partial resistance and inductance elements computation of the spiral inductor.

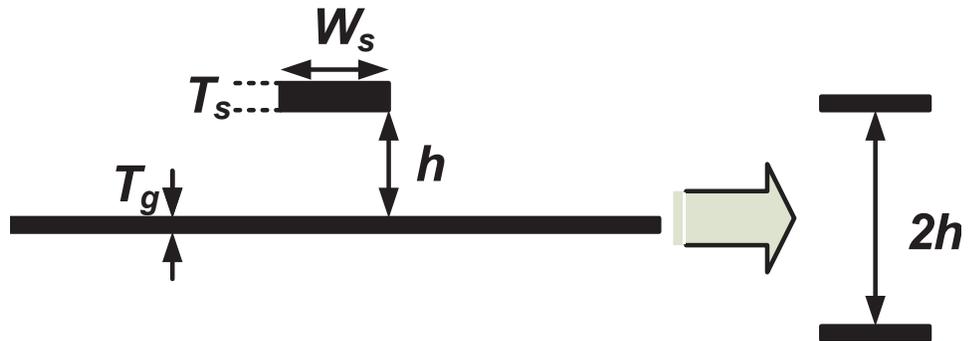


Figure 3.12: Setup for a conductor over a ground plane and its equivalent using a real image conductor.

be optimized by employing non-uniform discretization of the cross-section to efficiently capture the non-uniform cross-sectional current density. The function

$$\sum_{k=1}^K \sum_{n=1}^{N_{\gamma k}} \frac{\mu}{a_l a_{\gamma nk}} \int_{v_l} \int_{v_k} G^A(\bar{r}, \bar{r}') dv' dv_l \quad (3.22)$$

is evaluated for each  $k^{th}$  segment and each  $n^{th}$  cell within the  $k^{th}$  segment according to

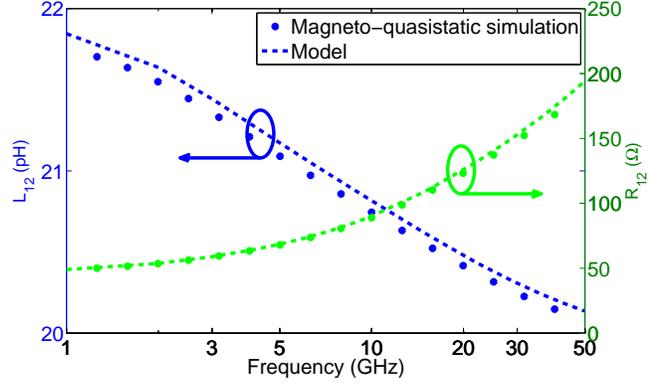


Figure 3.13: Performance of real image approach to model conductor over a ground plane through comparison with a full-wave simulator results.

the meshing as shown in Fig. 3.11. Here  $x : 1 \rightarrow W_k/\Delta x; z : 1 \rightarrow T_k/\Delta z$ , where  $W_k$  is the width of  $k^{th}$  segment and  $T_k$  is the thickness of  $k^{th}$  segment,  $\Delta x$  and  $\Delta z$  are the size of the discretization in the  $x$  and  $z$  direction, respectively. The Green's function  $G(\vec{r}, \vec{r}')$  is available in closed-form for rectangular conductors, such as in [57], and with a better numerical stability in [49]. This process yields a partial resistance matrix with elements

$$R_{kn} = \frac{1}{\sigma_k} \frac{l_n}{a_{\gamma nk}} \quad (3.23)$$

where  $\sigma_k$  is the conductivity of the metal layer in which the  $k^{th}$  segment is placed. The partial resistances  $R_{kn}$  are combined into partial resistance matrix  $[R_{DC}]$ . The partial inductance matrix is calculated as shown in (3.14) and referred to as  $[L_{air}]$ . We exemplify the accuracy of our approach for a simplified case of a conductor over a ground conductor. Figure 3.12 shows a  $50 \mu\text{m}$  long and  $10 \mu\text{m}$  wide conductor over a ground plane. The effect of the ground plane can be accounted for by replacing the ground plane by an image conductor at twice the height from the ground plane, as shown in the figure. The conductor conductivity is  $3.8 \times 10^7 \text{ S/m}$ . Figure 3.13 shows the comparison of resistance and inductance calculated from a magnetoquasi-static simulator [27]. The results shown in Fig. 3.13 demonstrate the accuracy of the discretized partial element calculations.

So far the partial inductance formulation captures the skin and proximity effects within the spiral inductors. The eddy-current loss in the semi-conducting substrate is a

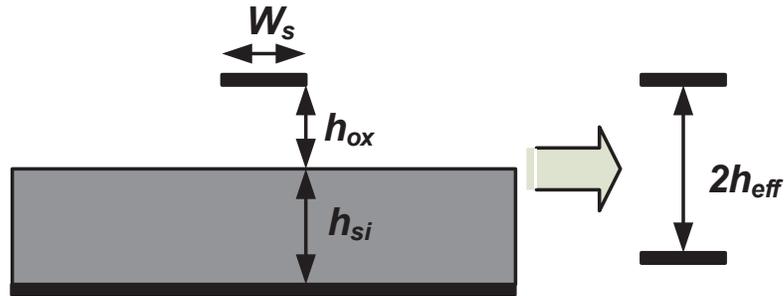


Figure 3.14: Setup for a conductor over a semiconductor substrate and a ground plane and its equivalent using a complex image.

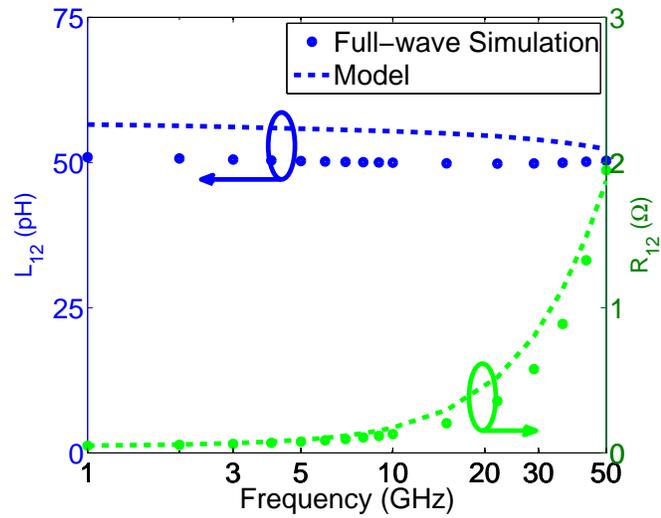


Figure 3.15: Performance of complex image approach to model conductor over a semiconductor substrate and a ground plane through comparison with a full-wave simulator results.

significant loss mechanism in on-chip interconnects and spiral inductors. This loss results in a reduction in inductance of the spiral inductor and an increase in the series resistance, which ultimately degrades the quality factor of the component. This loss can be captured using a multi-layered Green's function [58],[59], which is computationally expensive. We adopt a fast method to capture the losses using the complex image approach for single layer semi-conducting substrate [50] and implemented for spiral inductors in [60]. Consider a conductor on a layer of semi-conducting silicon substrate and inter-layer-dielectric as shown in Fig. 3.14. In this approach, the image conductor is located at twice the complex effective height  $h_{\text{eff}}$  given by

$$h_{\text{eff}} = h_{\text{ox}} + (1 - j) \frac{\delta}{2} \tanh \left( \frac{(1 + j) h_{\text{si}}}{\delta} \right) \quad (3.24)$$

where  $h_{\text{ox}}$  and  $h_{\text{si}}$  are the conductor height over the silicon-oxide interface and the height of silicon substrate, respectively.  $\delta$  is the skin depth defined as  $1/\sqrt{\pi\mu\sigma_{\text{si}}f}$ . Intuitively, at very low frequencies, the substrate eddy-current loss can be approximated to be negligible and therefore  $h_{\text{eff}}$  should approach  $h_{\text{ox}} + h_{\text{si}}$ . In this scenario, if the  $\delta$  is assumed to be very large, the argument of the  $\tanh$  function is very small, which leads to the approximation of the function as the argument itself, resulting in the second term of the  $h_{\text{eff}}$  equation equal to  $h_{\text{si}}$ . At very high frequencies, as  $\delta$  approaches zero, this second term can be ignored, resulting in  $h_{\text{eff}} \rightarrow h_{\text{ox}}$ . This can be intuitively understood by exchanging frequency with conductivity, leading to a highly conductive substrate, mimicking our previous scenario of solid conducting ground plane and making the image distance real and equal to twice height over the ground plane.

Figure 3.15 shows an example result for this method for a 10  $\mu\text{m}$  wide conductor, 11  $\mu\text{m}$  above the silicon-oxide interface, with 400  $\mu\text{m}$  thick substrate, and 10 S/m substrate conductivity.

Figure 3.16 shows the resulting partial elements equivalent circuit for two adjacent spiral segments. The partial resistances and inductances are frequency dependent due to the semi-conducting substrate. There are also mutual partial inductances (not shown) between each branch within segments and between segments.

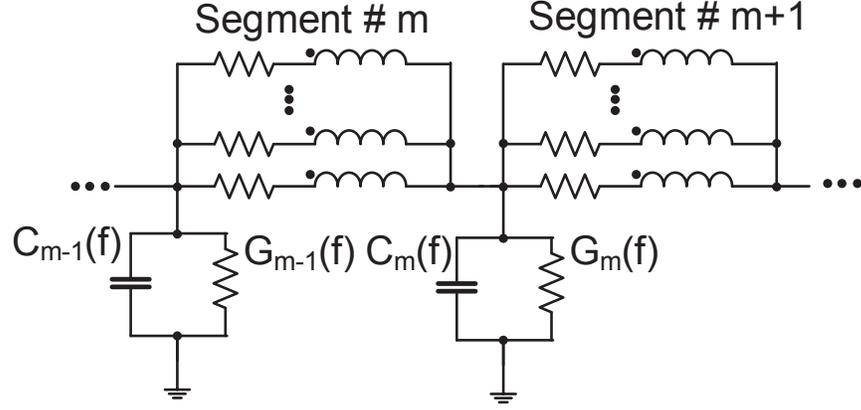


Figure 3.16: Partial elements representation of two adjacent spiral inductor segments.

### 3.7.2 Partial Conductance and Capacitance

In this subsection we discuss the partial capacitance and conductance calculations without metal fill. We partition the spiral inductor structure into segments with an offset of half the cell length as demonstrated by (3.16). The problem is partitioned by dividing a segment into two subsegments as shown in Fig. 3.17. At each node  $k_i$ , the partial capacitance to ground is the partial capacitance of a  $90^\circ$  bend if  $k_{i+1}$  exists or of a  $l_{i-1}/2$  subsegment otherwise. The partial mutual capacitance between node  $k_i$  and  $k_j$  is the partial mutual capacitance between the bends or segments associated with the respective nodes.

For the calculation of bend partial capacitance to ground, we split the bend into two segments of length  $(l_i - W_s)/2$  and  $(l_{i+1} - W_s)/2$ , and calculate the total capacitance using

$$C_{ii} = C'_i \left( \frac{l_i - W_s}{2} \right) + C'_{i+1} \left( \frac{l_{i+1} - W_s}{2} \right) \quad (3.25)$$

where  $C'_i$  is the unit length (p.u.l.) capacitance determined from the cross-section of the multi-conductor arrangement. The partial mutual capacitance is calculated as

$$C_{ij} = C'_{i,j} \left( \frac{\frac{l_i - W_s}{2} + \frac{l_j - W_s}{2}}{2} \right) + C'_{i+1,j+1} \left( \frac{\frac{l_{i+1} - W_s}{2} + \frac{l_{j+1} - W_s}{2}}{2} \right). \quad (3.26)$$

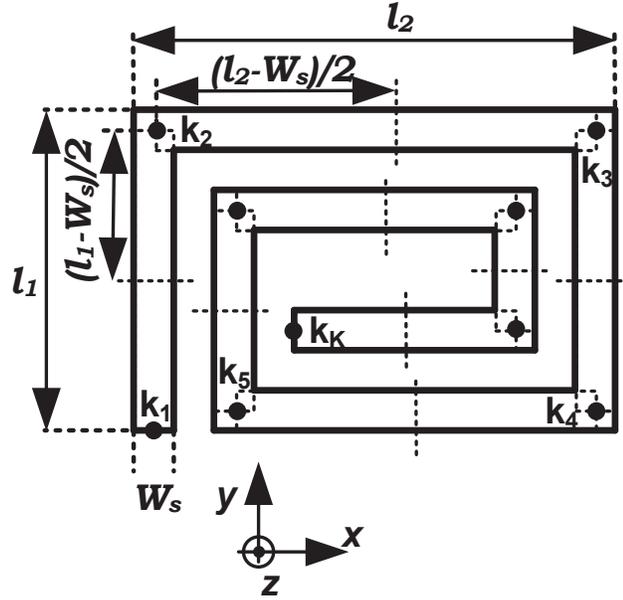


Figure 3.17: Segmentation for partial conductance and capacitance computations of the spiral inductor.

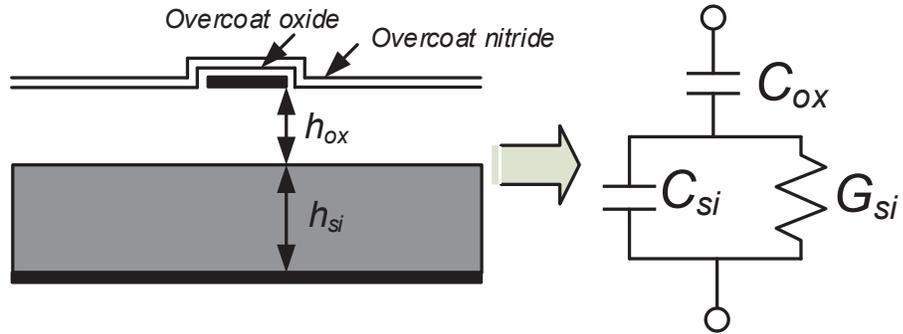


Figure 3.18: On-chip embedded interconnect and its equivalent quasi-TEM C-GC model.

In the following we discuss the equivalent circuit for representing the

$$\sum_{k=1}^K \sum_{m=1}^{M_k} \int_{v_l} \nabla \left[ \frac{1}{\epsilon} \int_{s_k} G(\bar{r}, \bar{r}') \rho_{mk}(t_m) ds' dv_l \right] \quad (3.27)$$

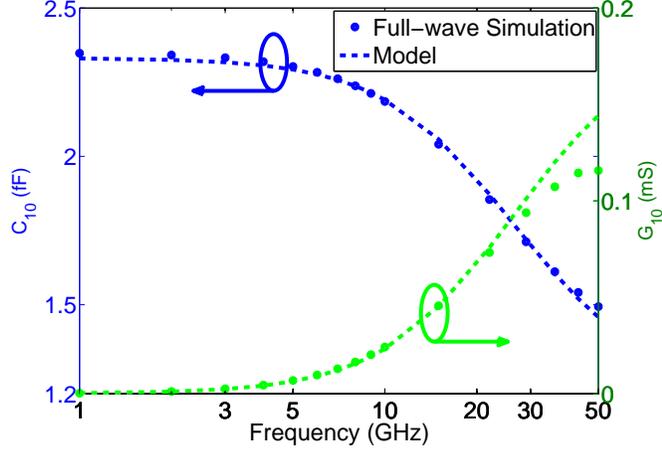


Figure 3.19: Performance of the C-GC model compared with a full-wave simulator results for the interconnect structure shown in Fig. 3.18.

term in integral equation (3.11). Since we are ignoring retardation effects between the cells, we can treat the half size offset cell as a partial self capacitance [56]. Therefore the potential at the  $i^{th}$  node is directly represented by a capacitance at the node as

$$\Phi_i(t) = \sum_{j=1}^n \frac{1}{C_{ij}} Q_j(0) \quad (3.28)$$

and the coupling to this node is represented by a partial mutual capacitance as

$$v_i^C(t) = \sum_{j \neq i} \frac{C_{jj}}{C_{ij}} \Phi_j(t). \quad (3.29)$$

Therefore we can determine the values of these partial capacitances using an electrostatic approximation, which reduces the complexity for the spiral inductor segment (or cell) capacitance and mutual capacitances. However, for on-chip spiral inductors, the effects of substrate displacement current need to be taken into account as frequency increases. Similar to the substrate eddy-current loss calculations, Green's functions have been developed for accounting for such effects (see, for example, [61]). These Green's functions rely on the discretization of the entire spiral inductor geometry and may also incur numerical instabilities [62]. Therefore, we utilize a quasi-electrostatic approximation [63]

for solving this problem. The effects of the substrate can be incorporated by using a C-GC representation [64] of this conductor-oxide-silicon structure shown in Fig. 3.18. We calculate the capacitances of the problem shown in the figure using a 2D electrostatic simulator. We utilize the low frequency and high frequency asymptotic electrostatic values of the shunt capacitance to calculate the values of  $C_{\text{ox}}$  and  $C_{\text{si}}$ . At the low frequency limit, the displacement current in the substrate is negligible and therefore the frequency dependent shunt conductance (equivalent conductance of C-GC shown in Fig. 3.18) is also negligible (since oxide is assumed to be lossless) and the capacitance is equal to  $C_{\text{ox}}$ . At the very high frequency asymptotic value, the displacement current in the substrate dominates, and therefore, the equivalent capacitance  $C_{\text{HF}}$  is a series combination of  $C_{\text{ox}}$  and  $C_{\text{si}}$ . Thus, the value of  $C_{\text{si}}$  can be calculated from the asymptotic values as

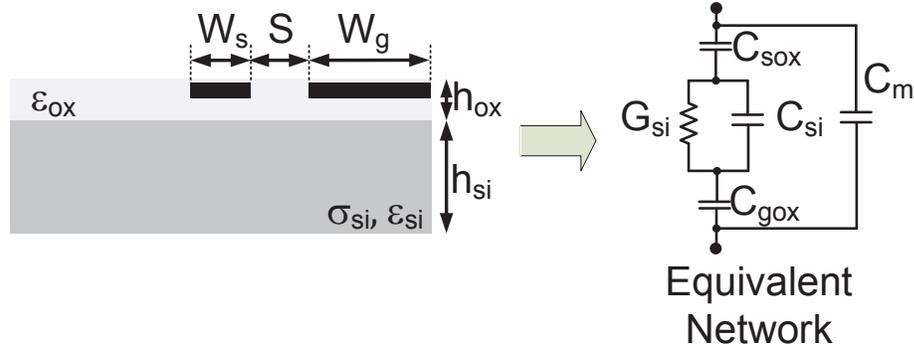
$$C_{\text{si}} = \frac{C_{\text{ox}}C_{\text{HF}}}{C_{\text{ox}} - C_{\text{HF}}}. \quad (3.30)$$

Further, the value of  $G_{\text{si}}$  is calculated from the relaxation time constant of the substrate as

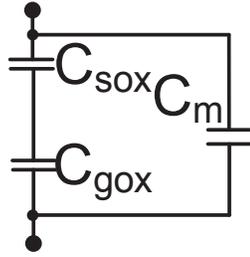
$$\frac{G_{\text{si}}}{C_{\text{si}}} = \frac{\sigma_{\text{si}}}{\epsilon_{\text{si}}}. \quad (3.31)$$

Figure 3.19 shows the performance of this approximation for the structure shown in Fig. 3.18 with a signal conductor width of 10  $\mu\text{m}$ . As can be seen from the figure, the C(f) model results agree well with the full-wave simulation results. We observe deviations in the G(f) result comparison beyond 30 GHz and see the limitations of the C-GC approximation.

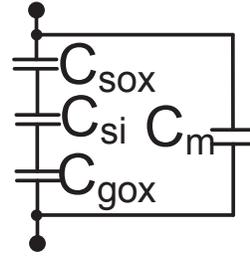
For measurement purposes, spiral inductors are typically surrounded by a ring of ground conductor; therefore, the zero potential is not always at the back of the substrate. For this reason, we verify our C-GC model for both coplanar Ground-Signal-Ground (GSG) and Signal-Ground (SG) test scenarios. Figures 3.20 and 3.21 show the geometry and the model performance, respectively. Similar to the cond-ox-ground scenario described before, the LF calculation is performed for a geometry in which the substrate is replaced with a conductor. This calculation provides the values of  $C_{\text{sox}}$ ,  $C_{\text{gox}}$ , and  $C_m$ . At the high frequency, the substrate is replaced with a dielectric with permittivity equal to  $\epsilon_{\text{si}}$ . This approximation provides the value of  $C_{\text{si}}$  since the values of  $C_{\text{sox}}$ ,  $C_{\text{gox}}$ , and  $C_m$  are known from the LF approximation. Further, the  $G_{\text{si}}$  and  $C_{\text{si}}$  are related by the



(a) Geometry and its equivalent circuit for all frequencies



(b) Equivalent circuit for low frequencies (LF)



(c) Equivalent circuit for high frequencies (HF)

Figure 3.20: Floating coplanar ground conductor in the same layer of signal conductor.

relaxation time constant of the substrate, similar to the signal-oxide-substrate-ground structure shown before.

In some test measurement setups, this ground conductor ring is shorted to the substrate creating a local substrate ground as shown in Fig. 3.22. Utilizing a similar approach as for the signal-ox-substrate-ground structure shown before, we achieve good performance for our  $C(\omega)$  model up to 50 GHz, as shown in Fig. 3.23. The  $G(\omega)$  results show deviations beyond 30 GHz, as noticed before.

### 3.8 Partial Element Computations with Metal Fill

In this section we discuss the partial element computations in the presence of metal fill.

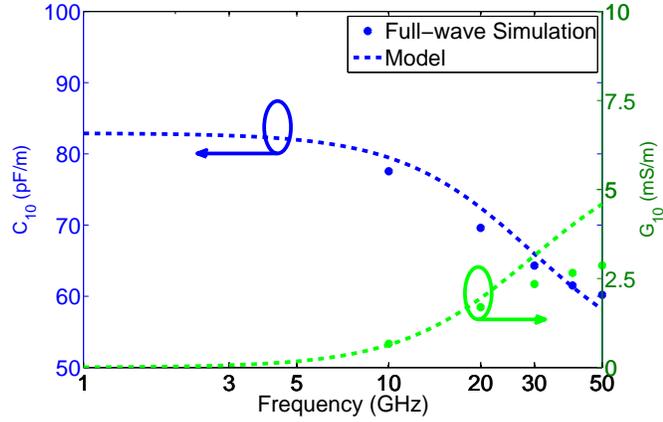


Figure 3.21: Comparison of the C-GC model with full-wave simulator results for the coplanar interconnect structure shown in Fig. 3.20a.

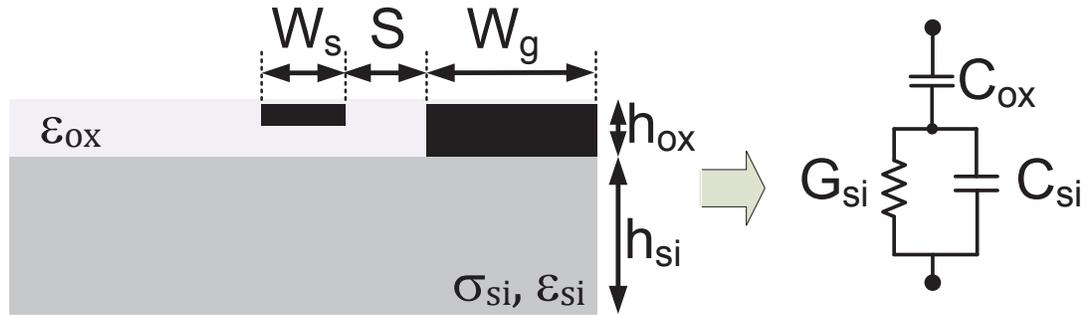


Figure 3.22: Coplanar ground conductor tapped to silicon substrate in the same layer of signal conductor and its equivalent circuit.

### 3.8.1 Partial Resistance and Inductance

The eddy-current loss calculations in one metal fill is based on the approach presented in [34] and [65]. The effect of introducing metal fill into a time-varying magnetic field is discussed in Chapter 1. We repeat the information here for the reader's convenience. According to Ampere's law, the impressed time-harmonics current generated by a spiral inductor causes a time-harmonic applied magnetic field,  $\vec{H}_a(\vec{r})$  inside the metal fill

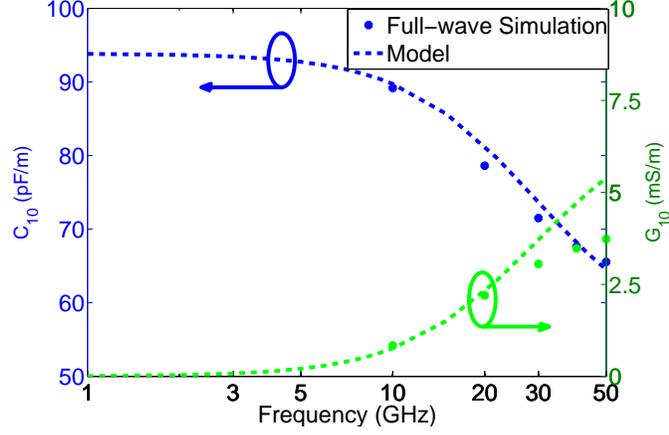


Figure 3.23: Comparison of C-GC model with full-wave simulator results for the coplanar interconnect structure with substrate tap shown in Fig. 3.22.

volume as

$$\vec{H}_a(\vec{r}) = \int \frac{I'(\vec{r}') d\vec{l}' \times \vec{R}}{4\pi R^3} \quad (3.32)$$

where the current element is  $I d\vec{l}'$  and the vector  $\vec{R}$  points from a source to an observation point. This time-harmonic magnetic field creates an electromotive force (emf),  $v_e$ , according to Faraday's law as

$$v_e = \oint \vec{E}(\vec{r}) \cdot d\vec{l} = -j\omega\mu \int_S \vec{H}_a(\vec{r}) \cdot d\vec{S} \quad (3.33)$$

where  $\mu$  is the permeability of the surrounding medium (here assumed to be homogeneous). Due to the finite conductivity of the metal fill, emf  $v_e$  produces a current density inside the metal fill,  $\vec{J}_e(\vec{r})$ . According to Lenz's law, this eddy-current  $\vec{J}_e(\vec{r})$ , produces a magnetic field,  $\vec{H}_r(\vec{r})$  as

$$\nabla \times \vec{H}_r(\vec{r}) = \vec{J}_e(\vec{r}) \quad (3.34)$$

that opposes the time-harmonic magnetic field  $\vec{H}_a(\vec{r})$ . Substituting  $\vec{J}_e(\vec{r})$  into the time-harmonic Faraday-Maxwell's equation gives a relationship between the applied field and response field as

$$\nabla \times \vec{E}(\vec{r}) = \nabla \times \frac{\vec{J}_e(\vec{r})}{\sigma} = \nabla \times \nabla \times \frac{\vec{H}_r(\vec{r})}{\sigma} = -j\omega\mu (\vec{H}_a(\vec{r}) + \vec{H}_r(\vec{r})). \quad (3.35)$$

The response field,  $\bar{H}_r(\bar{r})$  opposes  $\bar{H}_a(\bar{r})$  and reduces the total magnetic energy

$$j\omega\mu \int \frac{1}{2} |\bar{H}_a(\bar{r}) + \bar{H}_r(\bar{r})|^2 dV \quad (3.36)$$

stored in the interconnect or spiral inductor structure, thus reducing the effective inductance in addition to increasing its resistance.

The average total power loss due to the eddy-currents in metal fill volume ( $v_{\text{fill}}$ ) can be given by the Poynting's theorem as

$$P_L = \frac{1}{2} \oint (\bar{E}(\bar{r}) \times \bar{H}^*(\bar{r})) \cdot d\bar{S} = \frac{1}{2} \int_{v_{\text{fill}}} \bar{E}(\bar{r}) \cdot \bar{J}_e^*(\bar{r}) dv = \frac{1}{2} \int_{v_{\text{fill}}} \frac{|\bar{J}_e(\bar{r})|^2}{\sigma} dv \quad (3.37)$$

We are interested in this power loss since the increase in effective resistance,  $R_{\text{mf}}(\omega)$ , can be directly calculated from the known impressed current ( $I$ ) that generates the applied magnetic field ( $\bar{H}_a(\bar{r})$ ) as

$$R_{\text{mf}} = 2 \frac{P_L}{|I|^2}. \quad (3.38)$$

Gaskill et al. [34] have approached this problem by approximating the power loss due to a uniform applied field in terms of a normalized power loss function. This technique is further extended in [65] by representing the loss in each metal fill due to a spatially arbitrarily oriented applied field for each field direction as

$$P_{\text{fill},i} = \frac{W_m}{\sigma} \{ |H_{ax}|^2 G_{xy} + |H_{ay}|^2 G_{xy} + |H_{az}|^2 G_z \} \quad (3.39)$$

Here  $H_{ax}$ ,  $H_{ay}$ , and  $H_{az}$  are the x-, y-, z-direction components of the applied field at the center of the metal fill volume,  $\sigma$  is the conductivity of the metal layer,  $W_m$  is the metal fill size (assuming an aspect ratio of 1), and  $G$  is an empirical function. The  $G_{xy}$  and  $G_z$  functions are given as

$$G\left(\frac{w_m t}{\delta^2}, \frac{W_m}{t}\right) \approx \frac{k_1 \left(\frac{w_m t}{\delta^2}\right)^{k_2}}{\left(k_3 \left(\frac{w_m t}{\delta^2}\right)^{k_4} + 1\right)^{k_5}}. \quad (3.40)$$

The  $k_i$ 's ( $i = 1, \dots, 5$ ) are functions of  $W_m/T_m$  which are similarly expressed by empirical

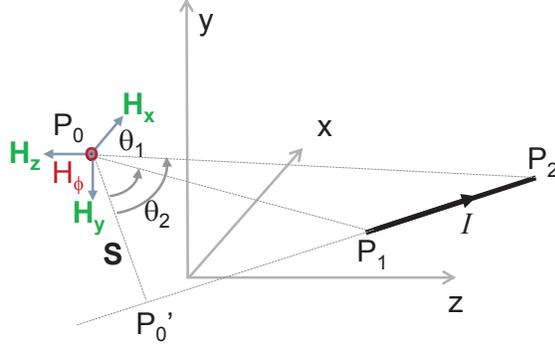


Figure 3.24: Problem setup for  $\bar{H}(\bar{r})$  field calculations for a finite current filament.

functions as

$$k_1 = 0.0692, \quad (3.41a)$$

$$k_2 = 214 \left( \frac{W_m}{T_m} \right)^{-1.57} + 29.6, \quad (3.41b)$$

$$k_3 = 2.23, \quad (3.41c)$$

$$k_4 = 0.617 \left( \frac{W_m}{T_m} \right)^{0.0281}. \quad (3.41d)$$

Here  $T_m$  is the metal fill thickness.

For a spiral inductor, the total applied field at the center of the metal fill is calculated by superposition of the fields due to each segment. To calculate the magnetic field, we discretize the spiral inductor geometry into segments, as shown in Fig. 3.10. The magnetic field due to each finite length segment is approximated by a set of finite length filaments. See Appendix B for the derivation of the magnetic field due to the finite length line current. This magnetic field is analytically calculated as follows.

The magnetic field at the center of metal fill,  $P_0(x, y, z)$ , due to a finite filament between  $P_1(x'_1, y'_1, z'_1)$  to  $P_2(x'_2, y'_2, z'_2)$ , as shown in Fig. B.1, is given by

$$\bar{H}(\bar{r}) = \frac{I (\sin(\theta_2) - \sin(\theta_1)) \bar{V}_{21} \times \bar{V}_{0'0}}{4\pi S \|\bar{V}_{0'0}\|} \quad (3.42)$$

where

$$\theta_2 = \frac{\pi}{2} - \cos^{-1} \left( \frac{\|\bar{V}_{21}\|^2 + \|\bar{V}_{20}\|^2 - \|\bar{V}_{10}\|^2}{2\|\bar{V}_{21}\| \cdot \|\bar{V}_{20}\|} \right) \quad (3.43a)$$

$$\theta_1 = \theta_2 - \cos^{-1} \left( \frac{\|\bar{V}_{20}\|^2 + \|\bar{V}_{10}\|^2 - \|\bar{V}_{21}\|^2}{2\|\bar{V}_{20}\| \cdot \|\bar{V}_{10}\|} \right) \quad (3.43b)$$

$$S = \frac{\|\bar{V}_{01} \times \bar{V}_{02}\|}{\|\bar{V}_{21}\|}. \quad (3.43c)$$

Here  $\bar{V}_{mn}$  is a vector going from  $P_n$  to  $P_m$ . The quantity  $S$  is the Euclidean distance between  $P_0$  and the line formed by  $\bar{V}_{21}$ . The individual components in Cartesian coordinates can be calculated as

$$H_x = \bar{H}(\bar{r}) \cdot \hat{a}_x, \quad (3.44a)$$

$$H_y = \bar{H}(\bar{r}) \cdot \hat{a}_y, \quad (3.44b)$$

$$H_z = \bar{H}(\bar{r}) \cdot \hat{a}_z. \quad (3.44c)$$

To verify the accuracy of our approximation for a spiral inductor geometry, we extracted the magnetic field for 1 A current source from a Finite Element Method (FEM) magnetostatic simulator [27]. Figure 3.25 shows the spiral inductor under consideration with 1.5 turns and  $50 \mu\text{m} \times 50 \mu\text{m}$  inner dimension. The segments are  $10 \mu\text{m}$  wide and  $2 \mu\text{m}$  spaced apart. Figure 3.26 shows the results of the  $\bar{H}_a(\bar{r})$  computations for 1 A current source compared with the field simulator results along the  $y$ -axis at  $x = 0$  and at a vertical separation of  $2.79 \mu\text{m}$  from the segments. The 10 segments are approximated by one and three filaments to evaluate the accuracy of this simplified approach. As expected, the approximation with three filaments gives better accuracy as compared to the single filament case and is sufficiently accurate to use for the loss calculations.

After the estimation of the fields, (3.39) is used to calculate the total power loss in the  $i^{\text{th}}$  metal fill. The total power loss due to all metal fills shown in Fig. 3.28 is calculated as the superposition of loss in each metal fill ignoring coupling between them. This provides the total increase in resistance  $R_{\text{mf}}(\omega)$  from (3.38). The decrease in inductance is calculated by fitting  $R_{\text{mf}}(\omega)$  to a Foster network shown in Fig. 3.27. The real part of the series impedance of the Foster network is equated to  $R_{\text{mf}}(\omega)$  and the imaginary

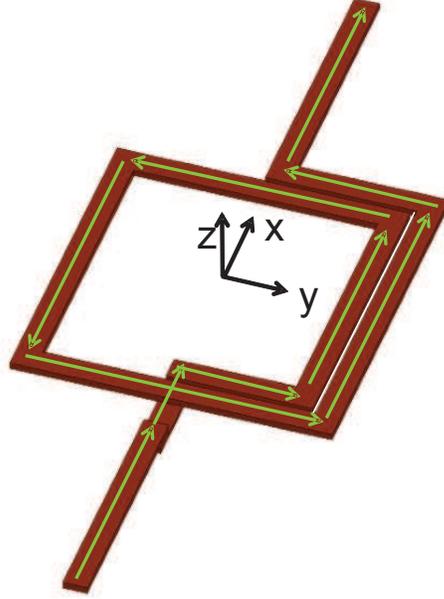


Figure 3.25: Spiral inductor structure used for the verification of magnetic field estimation.

part provides  $L_{\text{mf}}(\omega)$  as

$$R_{\text{mf}}(\omega) = \sum_{i=1}^3 \frac{\omega^2 R_i L_i^2}{R_i^2 + \omega^2 L_i^2}, \quad (3.45a)$$

$$L_{\text{mf}}(\omega) = \sum_{i=1}^3 \left( \frac{R_i^2 L_i}{R_i^2 + \omega^2 L_i^2} - L_i \right). \quad (3.45b)$$

Note  $L_{\text{mf}}$  is zero at DC and negative at frequencies . This series impedance,  $Z_{\text{mf}}(\omega) = R_{\text{mf}}(\omega) + j\omega L_{\text{mf}}(\omega)$ , due to metal fill is incorporated in the spiral inductor partial elements formulations by distributing the impedance in each of the discretized segment. The contribution of the applied fields due to the  $i^{\text{th}}$  segment to the total power loss is determined by first calculating the p.u.l. metal fill series impedance,  $Z'_{\text{mf}}(\omega)$ , for the entire spiral inductor. The contribution due to the  $i^{\text{th}}$  segment is calculated by multiplying

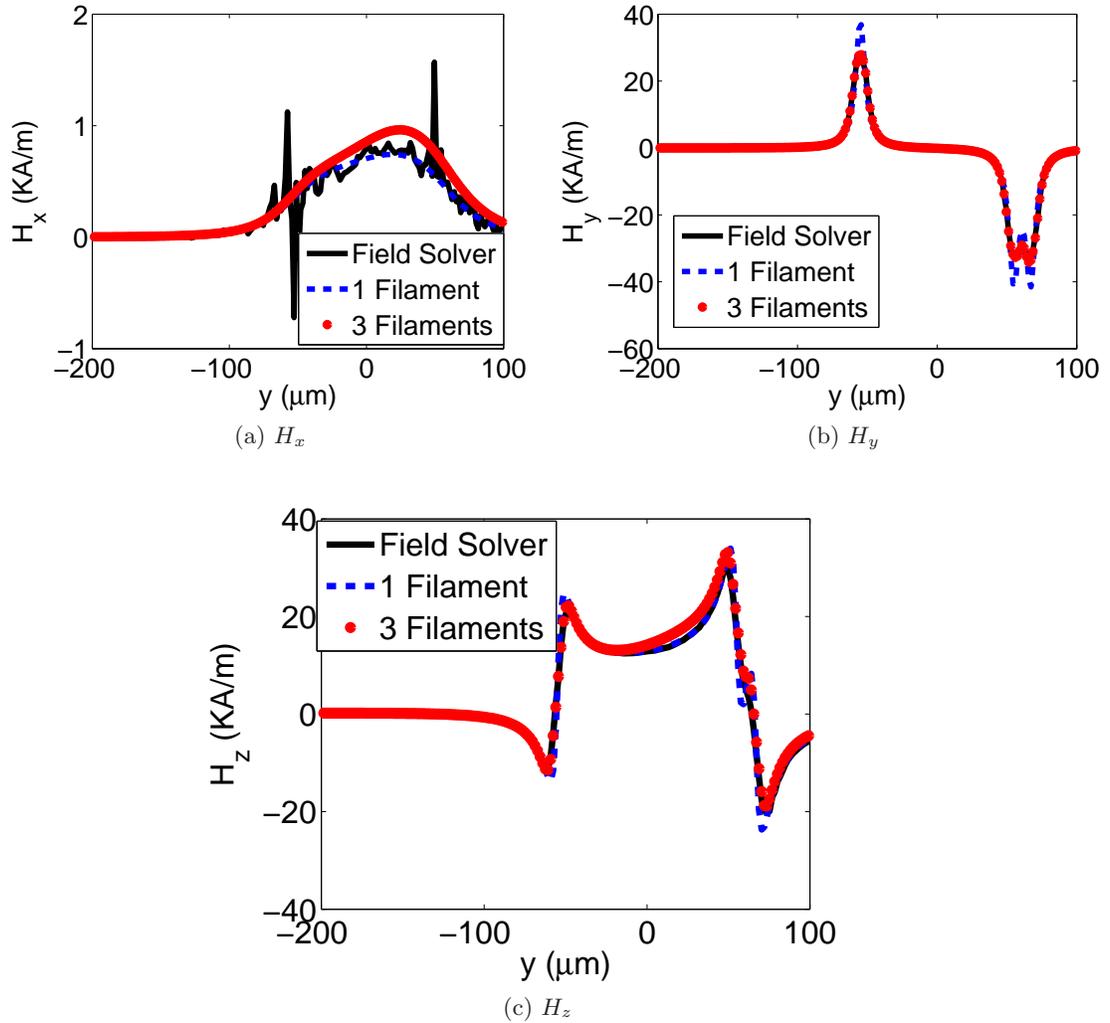


Figure 3.26: Comparison of analytic model with FEM simulator results for magnetic field estimation for 1 A current source.

the p.u.l. impedance by the length of the segment as

$$Z'_{\text{mf},i}(\omega) = l_i \frac{Z_{\text{mf}}(\omega)}{\sum_{i=1}^K l_i} \quad (3.46)$$

where  $l_i$  is the length of the  $i^{\text{th}}$  segment. These partial elements  $Z_{\text{mf},i}(\omega)$  are inserted in

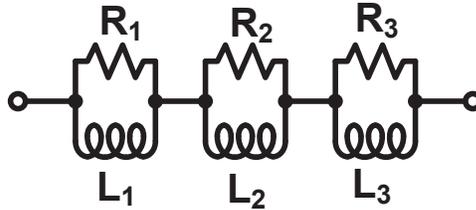


Figure 3.27: Foster network used to fit  $R_{mf}(\omega)$ .

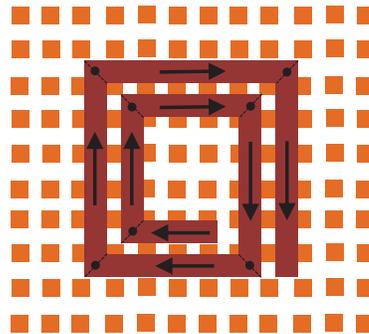


Figure 3.28: Partition used for metal fill eddy-current loss calculations.

the spiral inductor by splitting the  $i^{th}$  node as shown in Fig. 3.29.

### 3.8.2 Partial Conductance and Capacitance

The inclusion of metal fill parasitic capacitance effects is based on further partitioning of the segment (dashed lines shown in Fig. 3.30) into unit cells and using the problem reduction approach [46] discussed in Chapter 2. For each of the single or coupled segments with metal fill, the complex 3D problem is reduced to two 2D problems.

First the unit cells are identified for the spiral inductor layout with metal fill as shown in Fig. 3.31. Here, the number of metal fills to consider is determined by estimating the electric fields due to a set of finite length line charges. See Appendix C for the derivation of the electric field due to the finite length line charge. This electric field is used to

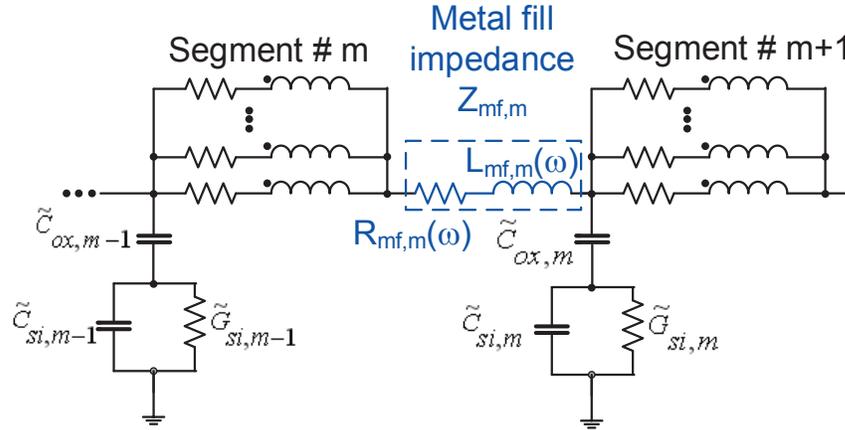


Figure 3.29: Inclusion of metal fill capacitance and eddy-current loss effects in the partial equivalent circuit of two adjacent segments.

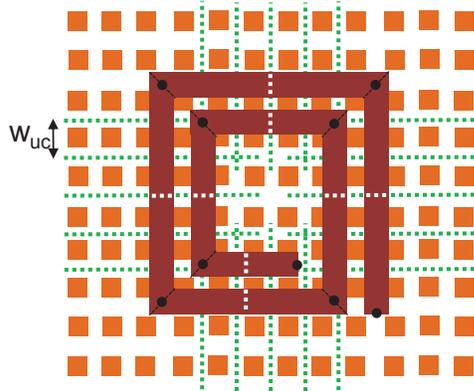


Figure 3.30: Partition for partial conductance and capacitance computation in the presence of metal fill.

determine the *region of influence* and therefore the critical metal fills to consider for the next step in the problem reduction. This completes the first step of the lateral problem reduction. Next, we identify the unit cells that are critical for the partial capacitance calculations. Referring to Fig. 3.31, unit cell UC-1 is identified for the partial capacitance calculations of a coupled conductor,  $k_{i,2}$  and  $k_{j,2}$ . Unit cell UC-7 is used to calculate the

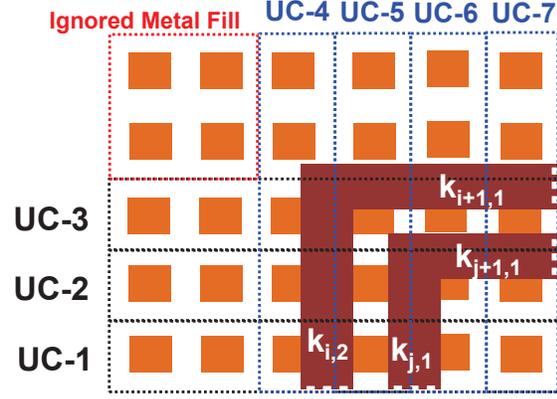


Figure 3.31: Details of the metal fill unit cell approximations used for partial conductance and capacitance computation.

partial capacitance between coupled conductors  $k_{i+1,1}$  and  $k_{j+1,1}$ . The metal fills in the left top dashed box are ignored for the calculations assuming the fringing fields due to the corner of the bend in the presence of metal fill to be negligible.

The p.u.l. low frequency (LF) asymptotic self and mutual capacitances of the multi-conductor structure are calculated using the effective linear density as

$$C'_{\text{LF}} = C'_{\text{mf,LF}} D_{\text{eff}} + C'_{\text{nf,LF}} (1 - D_{\text{eff}}). \quad (3.47)$$

The p.u.l. high-frequency (HF) asymptotic self and mutual capacitances are calculated as

$$C'_{\text{HF}} = C'_{\text{mf,HF}} D_{\text{eff}} + C'_{\text{nf,HF}} (1 - D_{\text{eff}}) \quad (3.48)$$

where  $C'_{\text{nf,LF}}$ ,  $C'_{\text{nf,HF}}$ ,  $C'_{\text{mf,LF}}$ , and  $C'_{\text{mf,HF}}$  are the no fill low frequency, no fill high frequency, fill low frequency, and fill high frequency 2D capacitances, respectively.  $D_{\text{eff}}$  is an effective linear density described in Chapter 2. The partial C-GC elements are calculated using these capacitances and the relaxation time constant of the substrate as discussed in the previous section. Figure 3.29 shows the corresponding equivalent circuit elements including metal fill with modified element values,  $\tilde{C}_{ox,m-1}$ ,  $\tilde{C}_{si,m-1}$ ,  $\tilde{G}_{si,m-1}$ ,

$\tilde{C}_{ox,m}$ ,  $\tilde{C}_{si,m}$ , and  $\tilde{G}_{si,m}$ . The entries in the partial capacitance matrix are calculated by multiplying the p.u.l. capacitance by appropriate segment lengths as shown for the case without metal fill.

### 3.9 Modified Nodal Analysis

The PEEC method relies on the circuit simulation techniques for either the time-domain or the frequency-domain analysis. In this work, we focus on the frequency-domain analysis of the problem at hand.

The partial resistance and inductance matrices form the impedance matrix in the MNA formulation [48]. Partial conductances and capacitances form the admittance matrix in the MNA formulation. The DC resistance of each cell and the partial self and mutual inductances of all the cells yield a free space impedance matrix as

$$Z_{\text{free}} \begin{bmatrix} [Z_{11}] & 0 & [Z_{12}] & 0 & [Z_{13}] & 0 & \cdots & [Z_{1K}] & 0 \\ [Z_{21}] & 0 & [Z_{22}] & 0 & [Z_{23}] & 0 & \cdots & [Z_{2K}] & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ [Z_{K1}] & 0 & [Z_{K2}] & 0 & [Z_{K3}] & 0 & \cdots & [Z_{KK}] & 0 \end{bmatrix}, \quad (3.49)$$

where

$$Z_{ii} = \begin{bmatrix} R_{ii,11} + j\omega L_{ii,11} & j\omega L_{ii,12} & j\omega L_{ii,13} & \cdots & j\omega L_{ii,1M} \\ j\omega L_{ii,21} & R_{ii,22} + j\omega L_{ii,22} & j\omega L_{ii,23} & \cdots & j\omega L_{ii,2M} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ j\omega L_{ii,M1} & j\omega L_{ii,M2} & j\omega L_{ii,M3} & \cdots & R_{ii,MM} + j\omega L_{ii,MM} \end{bmatrix} \quad (3.50)$$

and

$$Z_{ij|_{i \neq j}} = \begin{bmatrix} j\omega L_{ij,11} & j\omega L_{ij,12} & j\omega L_{ij,13} & \cdots & j\omega L_{ij,1M} \\ j\omega L_{ij,21} & j\omega L_{ij,22} & j\omega L_{ij,23} & \cdots & j\omega L_{ij,2M} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ j\omega L_{ij,M1} & j\omega L_{ij,M2} & j\omega L_{ij,M3} & \cdots & j\omega L_{ij,MM} \end{bmatrix}. \quad (3.51)$$

Here K is the total number of segments and M is the total number of mesh elements in each segment.

After using the approach in [66], we calculate the complex inductance matrix  $[L_{si}]$  for all the cells. After accounting for the substrate effects, the free space impedance matrix is modified as

$$[Z_{ij}^*] = [Z_{ij}] - \omega \text{Im}([L_{si}]) - j \text{Re}([L_{si}]). \quad (3.52)$$

The augmentation of the original  $[Z]$  matrix with metal fill impedance  $Z_s(f)$  is given as

$$\begin{bmatrix} [Z_{11}] & 0 & [Z_{12}] & 0 & [Z_{13}] & 0 & \cdots & [Z_{1K}] & 0 \\ 0 & Z_{\text{mf},1} & 0 & 0 & 0 & 0 & \cdots & 0 & 0 \\ [Z_{21}] & 0 & [Z_{22}] & 0 & [Z_{23}] & 0 & \cdots & [Z_{2K}] & 0 \\ 0 & 0 & Z_{\text{mf},2} & 0 & 0 & 0 & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ [Z_{K1}] & 0 & [Z_{K2}] & 0 & [Z_{K3}] & 0 & \cdots & [Z_{KK}] & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \cdots & 0 & Z_{\text{mf},K} \end{bmatrix} \quad (3.53)$$

Here,  $[Z_{ij}]$  is the impedance matrix between the  $i^{\text{th}}$  and  $j^{\text{th}}$  segment.  $Z_{\text{mf},m}$  is the metal fill impedance added between the  $m^{\text{th}}$  and the  $(m+1)^{\text{th}}$  segment as shown in Fig. 3.29.

The admittance matrix  $[Y_{b1}]$  comprising the partial capacitance ( $C_{ii}(\omega)$ ) and conductance ( $G_{ii}(\omega)$ ) elements for  $N_n$  nodes and  $P$  mutual capacitances ( $C_m$ 's) is formulated as

$$\left[ \begin{array}{cccccc|cccc} Y_{11} & 0 & 0 & \cdots & 0 & 0 & j\omega C_{m1} & 0 & 0 & 0 \\ 0 & Y_{22} & 0 & \cdots & 0 & 0 & 0 & j\omega C_{m2} & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & 0 & 0 & \ddots & \vdots \\ 0 & 0 & 0 & Y_{PP} & \cdots & 0 & 0 & 0 & \cdots & j\omega C_{mP} \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & 0 & Y_{N_n N_n} & 0 & 0 & 0 & 0 \end{array} \right] \quad (3.54)$$

where

$$Y_{ii} = G_{ii}(\omega) + j\omega C_{ii}(\omega). \quad (3.55)$$

The right hand side partition of the  $[Y_{b1}]$  matrix along with the incident matrix for MNA [67] give the mutual admittance between the corresponding nodes. The  $G(\omega)$  and  $C(\omega)$  partial elements above include the effect of metal fill, therefore further modification to

the matrix formulation is not required.

The short-circuit Y parameters of the spiral inductor are calculated by solving the modified nodal analysis formulation as

$$[U] = \begin{bmatrix} A_1 Y_{b1} A_1^T & A_2 \\ Y_{b2} A_2^T & Z_b \end{bmatrix}^{-1} [S] \quad (3.56)$$

where  $Y_{b2}$  is an identity matrix  $[I]_{(N_b+2) \times (N_b+2)}$ ,  $N_b = M \times K + K$  is total number of branches,  $A_1$  is an incident matrix corresponding to the shunt branches, and  $A_2$  is an incident matrix corresponding to the series branches shown in Fig. 3.29. Finally, the Y-parameters of the spiral inductor can be calculated as

$$\left. \begin{array}{l} Y(1,1) = -U(N_n + 1, 1) \\ Y(2,1) = -U(N_n + 2, 1) \end{array} \right\} \quad \text{for } S = \begin{bmatrix} [0]_{N_n \times 1} \\ 1 \\ 0 \\ [0]_{N_b \times 1} \end{bmatrix} \quad (3.57)$$

and

$$\left. \begin{array}{l} Y(1,2) = -U(N_n + 1, 2) \\ Y(2,2) = -U(N_n + 2, 2) \end{array} \right\} \quad \text{for } S = \begin{bmatrix} [0]_{N_n \times 1} \\ 0 \\ 1 \\ [0]_{N_b \times 1} \end{bmatrix}. \quad (3.58)$$

$N_n$  is the total number of nodes  $2K+1$  for the spiral inductor in the presence of metal fill due to node splitting as discussed in the previous section.

### 3.10 Comparison with Full-wave Simulation

We verified the accuracy of our method by comparison with a commercial full-wave simulator, HFSS [11]. To achieve confidence in the commercial simulator results, we performed the convergence analysis and compared the results of the simulator with analytical solutions available for canonical geometries. Furthermore, the simulator results are compared with a different simulator appropriate for the problem.

We simulated a spiral inductor with 1.5 turns,  $10 \mu\text{m}$  width and  $2 \mu\text{m}$  spacing designed in a  $0.18 \mu\text{m}$  BiCMOS process. Figure 3.32 shows the problem setup. The metal

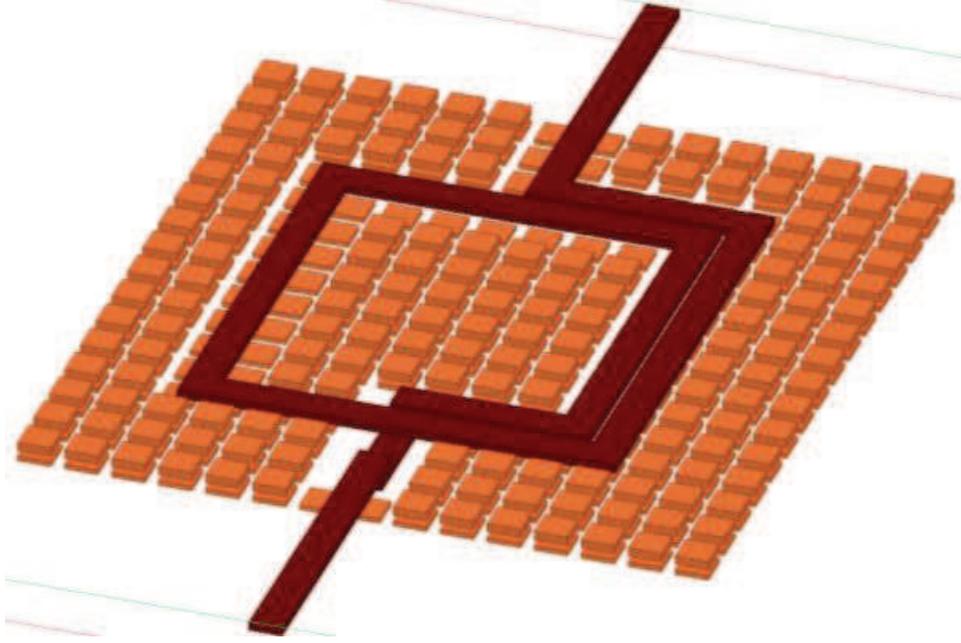


Figure 3.32: Problem setup for results in Fig. 3.33.

fills are  $10 \mu\text{m} \times 10 \mu\text{m}$  with 50% density. The HFSS simulation took  $\sim 56.4$  hours and 39.7GB of memory for 15 frequency points on an Intel<sup>®</sup> Xeon<sup>®</sup> server. On the other hand, our method took  $\sim 25$  mins. and 177 MB of memory for the same problem on the same computer. We compared the equivalent series inductance,  $L_{12} = \text{Im}(-1/Y_{12})/\omega$ , resistance,  $R_{12} = \text{Re}(-1/Y_{12})$ , and quality factor  $Q_{11} = -\text{Im}(Y_{11})/\text{Re}(Y_{11})$  of the spiral inductor. Figure 3.33 shows this comparison. We achieve RMS errors<sup>3</sup> of 2.5% without metal fill and 4.7% with metal fill in the estimation of inductance; rms error of 5.9% without metal fill and 4.6% with metal fill in the estimation of the quality factor. Also note that the degradation of the quality factor due to metal fill is accurately estimated at about 31% at peak Q frequency.

<sup>3</sup>error between vectors  $\hat{x}$  (estimated) and  $x$  (true) =  $100 \times \frac{\|x - \hat{x}\|_2}{\sqrt{N}\|x\|_\infty}$

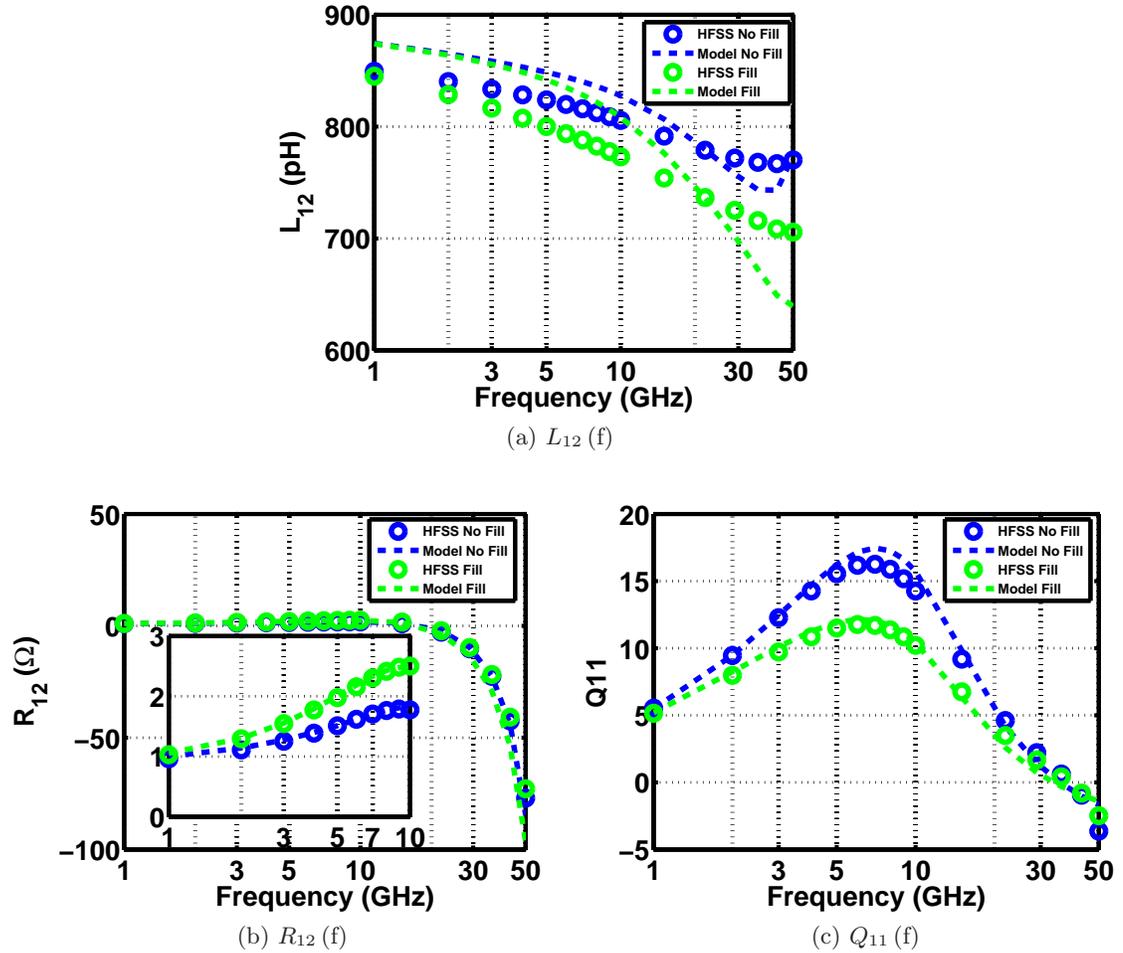


Figure 3.33: Comparison of model with full-wave simulation results for setup shown in Fig. 3.32.

### 3.11 Conclusion

In this chapter, we have presented a new method to capture the impact of additional parasitics due to metal fill inserted in spiral inductors. The results obtained with our method agree within 6% with commercial simulator results. We have also illustrated the computational challenges in terms of time and memory required to solve a subset of this problem. This demonstrates the computational efficiency of our method in terms of the

memory and time.

## Chapter 4: Broadband Characterization of On-chip Passive Components

### 4.1 Introduction

In the previous two chapters we presented modeling methods for on-chip interconnects and passive components in the presence of metal fill. In Chapter 2, we discussed a scalable modeling approach for the capacitance of multi-conductor interconnects and in Chapter 3, we discussed the spiral inductor scalable models in the presence of metal fill. There are two ways to verify the accuracy of our models: a rigorous set of electromagnetic simulations and a measurement based characterization of fabricated test structures. As we pointed out in Chapter 3, the computational resources (time and memory) required to solve a relatively small problem in a commercial full-wave electromagnetic (EM) solver become exorbitant. In fact, EM simulations for a large spiral inductor with metal fill in all metal layers may be prohibitive in commercial solvers. Therefore, we employed measurement based characterization to verify the accuracy of our models for large problem sizes. We investigated approaches for on-chip measurement based characterization and we discuss representative methods in this chapter. In the next chapter, we provide a comparison between our models and measurement results.

This chapter is organized as follows. In Section 4.2, we provide an overview of a typical on-chip measurement characterization setup and define metrics used to quantify the confidence in measurement results. In Section 4.3, we discuss challenges associated with on-chip component characterization and practical considerations for non-idealities in the measurement setup. Section 4.4 describes two error models for VNAs. In Section 4.5 we introduce two approaches for on-chip measurements. Section 4.6 provides VNA calibration methods used for on-chip component characterization followed by Section 4.7, which describes two widely used de-embedding techniques for removing test fixture non-idealities. Section 4.8 describes methods to capture the uncertainties associated with the measurement process. Finally, in Section 4.9 we demonstrate a comparison between full-wave electromagnetic simulations and measurement results for a spiral inductor.

## 4.2 Overview of On-chip Passive Component Characterization

This section provides an overview of a typical on-chip passive component characterization process. First, we provide details of a typical measurement interconnection waveguides starting from a measurement equipment to a device under test (DUT). Second, we will define quantities that are commonly used for evaluating the performance of measurement results.

### 4.2.1 Typical On-chip Measurement Setup

We start our discussion of on-chip passive component characterization with a typical set of instruments and connections used in the DUT measurements. This work is limited to the scattering (**S**) parameter measurements; therefore, we consider a typical setup shown in Fig. 4.1. The setup shows important aspects of a typical on-chip measurement based characterization, including a vector network analyzer (VNA), wafer probes, and mounting and connection accessories. The VNA is connected to the probes using coaxial cables. These cables are very low loss, low dispersion, flexible and very well shielded. The diameter of the connectors used for connecting the VNA to these cables and cables to the probes are typically 3.5 mm, 2.92 mm, 2.4 mm, 1.82 mm, and 1 mm for single mode operation up to 32 GHz, 46 GHz, 50 GHz, 65 GHz, and 110 GHz, respectively. The wafer probes are mounted on a movable chuck for their placement and landing on the IC metal pads. For each port, the wafer probe is typically arranged as a Ground-Signal (GS) or Ground-Signal-Ground (GSG) tip. For a two-port measurement using a single probe fixture (with two-ports), the wafer probe tips are arranged as Ground-Signal-Ground-Signal-Ground (GSGSG) or Ground-Signal-Signal-Ground (GSSG). The test chip to be characterized is placed on a chuck with vacuum suction.

Along the signal propagation path from the connector of the VNA to the DUT reference plane, the traveling waves incur several discontinuities. Figure 4.2 shows an equivalent cascaded transmission line network of this path in terms of the wave guiding structures. The first discontinuity (outside VNA) comprises the VNA connectors. Although by construction connectors are designed to maintain a transverse electromagnetic (TEM) mode of the propagating waves, discontinuities occur at the connections. This mode is continued in the coaxial cable used to connect wafer probe to the VNA connec-

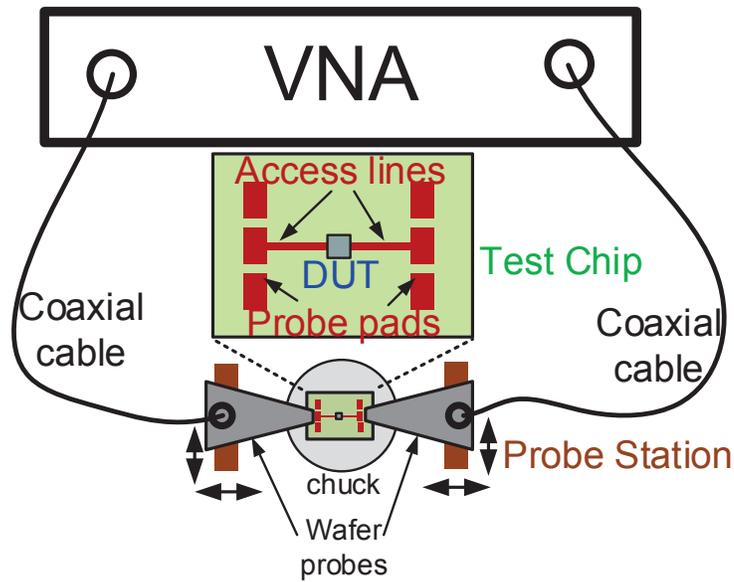


Figure 4.1: Typical device under test (DUT) measurement setup for on-wafer characterization using a vector network analyzer (VNA).

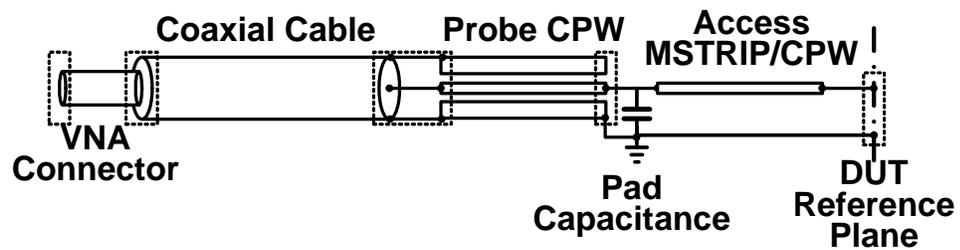


Figure 4.2: Wave guiding structures from VNA connector to DUT reference plane. Discontinuities are indicated by dotted lines and DUT reference plane is indicated by a dash-dot line.

tor. At the wafer probe interface, the guiding structure changes from coaxial to an air coplanar waveguide (CPW). With the discontinuity due to a change in reference plane, this connection attempts to convert the coaxial TEM mode to an air CPW TEM mode.

During the measurements, the probe lands on contact metal pads on the chip. At this connection, the waves incur a discontinuity in form of the probe tip to metal pad contact resistance and metal signal pad to ground capacitance. Further, the probe pads are connected to the DUT terminals using a set of access transmission lines. These transmission lines are typically realized as an embedded CPW or microstrip structures. Depending on the manufacturing process technology used, these transmission lines are usually embedded in overcoat nitrides and/or oxides, and planarized on inter-layer-dielectric (ILD) layers. Thus the air CPW TEM mode on wafer probes converts to a quasi-TEM mode in the access transmission lines. From the DUT point of view, the end of this access transmission line forms the reference plane for the measurements. The calibration and de-embedding techniques are classified based on how to account for the systematic non-idealities in this network.

#### 4.2.2 Definitions of Metrics

Before we define the metrics used in evaluating the confidence in a measurement result, we discuss goals of a measurement based characterization. The main goal of this process is to achieve accuracy and certainty in results, which leads to a confidence in the measurement results.

The **accuracy** is defined as *the agreement between the result of a measurement and a true value of the measurand* [68]<sup>1</sup>. The knowledge of the true value is very difficult in the scenarios of the DUT considered in this work. Therefore we will focus more on the certainty part of the metric. Next we consider repeatability and reproducibility of the measurements. The **repeatability** of the measurements is the *closeness of the agreement between the results of successive measurements of the same measurand carried out in the same conditions of measurements*. For our test scenarios, we calculate it by repeating the measurements at different times. The **reproducibility** of the measurements is *closeness of the agreement between the results of measurements of the same measurand carried out under changed conditions of measurements*. For our test scenarios, it can be calculated by change in calibration, repeated probing of devices, change in operator, or performing the measurements in a different laboratory location. Further, the **uncertainty** is defined as

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<sup>1</sup>Since these quantities are defined in the reference, we reproduce the definitions *as is* from the reference. We do not intend to distort the wordings from the definitions.

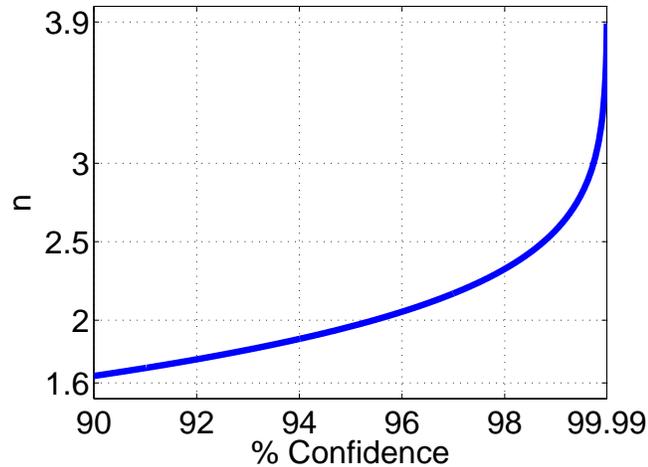


Figure 4.3: Factor  $n$  in  $\mu \pm n\sigma$  as a function of percentage of confidence.

a parameter associated with the result of a measurement, that characterizes the dispersion of the values that could be reasonably attributed to the measurand. This uncertainty is measured in terms of statistical quantities such a standard deviation ( $\sigma$ ) or a multiple of a standard deviation ( $n\sigma$ ).

Before we discuss the details of uncertainty related quantities, we define the two main causes of these uncertainties, the random and systematic errors. According to [68], the **random error** is a result of a measurement minus the mean that would result from an infinite number of measurements of the same measurand carried out under repeatability conditions. The causes of such errors include instrument drifts, random noise sources, and deterioration of the connections. The **systematic error** is defined as a mean that would result from an infinite number of measurements of the same measurand carried out under repeatability conditions minus a true value of the measurand. The causes of systematic error include non-ideal calibration standards, numeric instability of calibration algorithm.

To calculate the uncertainty in the measurement, if a certain probability distribution function (pdf) of measurand is known or assumed, a confidence interval (CI) is defined to quantify the errors. The estimated sample mean and variance value from  $N$  repeated

measurements  $(X_1, X_2, \dots, X_N)$  treated as a discrete random variables are given by

$$\bar{X} = \frac{1}{N} \sum_{i=1}^N X_i \quad (4.1)$$

$$\sigma^2 = \frac{1}{N} \sum_{i=1}^N (X_i - \bar{X})^2. \quad (4.2)$$

The confidence interval gives an estimated value of the parameter with a certain confidence, e.g., often 95 % or 99 %. For a normal probability distribution function (pdf) with an estimated mean,  $\bar{X}$ , and standard deviation,  $\sigma$ , the CI is equal to  $100(1-\alpha)$  % of the estimated mean value, where  $\alpha$  is a small number ( $0 < \alpha < 1$ ) [69]. This CI is calculated from the condition that

$$P(g_1(\mu) < \bar{X} < g_2(\mu)) = 1 - \alpha \quad (4.3)$$

so that

$$\int_{-\infty}^{g_1(\mu)} f(x; \mu) d\bar{x} = \alpha/2 \quad (4.4)$$

$$\int_{g_2(\mu)}^{\infty} f(x; \mu) d\bar{x} = \alpha/2. \quad (4.5)$$

Here  $f(x; \mu)$  is the pdf of the sampling distribution of  $\bar{X}$  and  $g_1$  and  $g_2$  are functions of  $\mu$ . If the random variable is assumed to have a normal pdf, that is,  $\bar{X} \sim N(\mu, \sigma)$ , then the pdf of  $x$  is given as,

$$f(x; \mu, \sigma) = \frac{1}{\sigma\sqrt{2\pi}} \exp \left[ -\frac{1}{2} \left( \frac{x - \mu}{\sigma} \right)^2 \right]. \quad (4.6)$$

The probability that the random variable lies between  $g_1(\mu)$  and  $g_2(\mu)$  can be calculated as

$$P(g_1(\mu) < \bar{X} < g_2(\mu)) = \frac{1}{\sigma\sqrt{2\pi}} \int_{g_1(\mu)}^{g_2(\mu)} \exp \left[ -\frac{1}{2} \left( \frac{x - \mu}{\sigma} \right)^2 \right] dx. \quad (4.7)$$

If the two bounds are written in the form of  $\sigma$  so that

$$g_1(\mu) = \mu - n\sigma \quad (4.8)$$

$$g_1(\mu) = \mu + n\sigma \quad (4.9)$$

then the value of  $n$  can be evaluated using a complementary error function as

$$n = \sqrt{2} \operatorname{erf}^{-1}(1 - \alpha). \quad (4.10)$$

See Appendix D for details of the derivation. For example, for a 95% CI, the value of  $n$  is 1.9599, the range is  $\mu \pm 1.9599\sigma$ . For a 99.99 % CI, the value of  $n$  increases to 3.891. Figure 4.3 shows this trend for CI between 90% to 99.99%.

### 4.3 Challenges in On-chip Measurement Characterization

In this section, we will discuss practical challenges associated with achieving the goals of the measurement process in a practical setting [70].

- **Changes in Instrument State: Drifts**

The temporal change in the characteristics of the instruments used causes drifts in the VNA, coaxial cables, probes, and connectors. The main cause of drift in the VNA and other measurement accessories is the changes in the local temperature within the internal units. Depending upon the state of the equipment (ON and OFF switching of units which depends on the operations), some local hot spots are created irrespective of the room temperature control. For cables, flexing of cables results in short term drifts. Therefore calibration and de-embedding need to be repeated after a few hours.

- **Cable Stability** The stability (electrical as well as mechanical) of coaxial cables inside and outside the VNA is an important factor that impacts the uncertainty and even causes serious issues, including incorrect measurement results. It can also lead to a significant source of random error. These types of errors can not be calibrated or de-embedded out. The only way to account for these errors is to include them in the error analysis and making them part of the error bounds [71]. The instability in the cable characteristics are caused by moving or flexing of the cables. The severity of the impact depends on the material used and the design of the cables. These types of errors can be minimized by reducing the flexing or

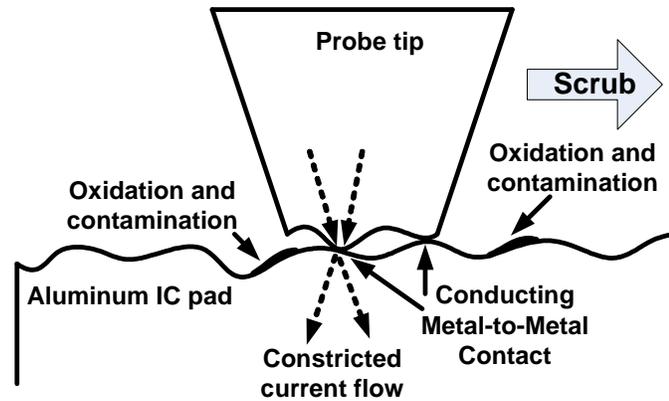


Figure 4.4: Probe landing on an aluminum IC pad (reproduced from [72]).

movement of the cable by keeping the calibration and de-embedding test structures close to the DUT structures.

- **Probe Contact Resistance and its Repeatability**

The on-chip measurements rely on making a reliable contact to the IC metal pads. The wafer probes landed on these pads result in a resistance between the probe tip and the contact pad. This resistance is referred to as contact or constriction resistance. This contact resistance is caused by several factors that are related to the fundamental physics of the two materials in contact as well as practical fabrication related issues [73]. During on-chip probing, the current through the probes is crowded in an effective contact area, and this results in localized heating raising the temperature and oxidation growth. Figure 4.4 illustrates the effects of landing a wafer probe tip on an aluminum metal pad. The practical issues that increase the contact resistance and the variability associated with it are the following:

1. In practical manufacturing of the probe tips and the IC metal pads, a surface roughness exists due the polishing tools used in the fabrication process. Also depending upon the properties of metal being polished, some metals can provide better polishing or smoother surfaces than others.
2. Even if a substantial tip area is designed to land on the IC metal pad, in reality, only a portion of the tip surface area is in contact. This is mainly due

to bends or damages in the probe tip and deformation of the soft IC contact pad material caused by multiple probe landings. This leads to a rough surface reducing the effective contact area.

3. Typically contact pads are fabricated so that the overcoat oxide is removed for ease of probing. This results in exposure of the contact metal to air leading to oxidation. The rate of oxidation formation depends on the type of metal and room conditions. For example, the rate of oxidation in aluminum is much higher than that of copper.
4. Dust or debris either on the surface of the probe tip or IC contact pad results in a reduced effective contact area ultimately increasing contact resistance.

Repeatability in the contact resistance between the probe tip and the IC pad is a serious issue in accurate on-chip DUT measurements. Depending on the type of probe (GS or GSG or GSGSG or GSSG), the planarity mismatch between each probe tip also affects the contact resistance. Typically, before probing, this planarity can be verified by probing a softer material followed by a visual inspection of the depth and width of the marks made by the probe tip. This non-planarity between probe tips can be adjusted by a mechanical alignment of the probe using the probe station.

- **Noise**

The noise in the VNA equipment predominantly affects the performance of low power level measurements. The noise floor of VNAs is determined by the intermediate frequency (IF) bandwidth of the VNA. Lower IF bandwidth results in larger measurement acquisition time, therefore noise and acquisition time form a trade-off in the measurements [70].

High performance equipment, calibration algorithms, de-embedding techniques, and error analysis techniques have been developed to address some of these challenges.

## 4.4 VNA and Error Models

In this section, we discuss a typical two-port VNA architecture and the error terms that model the non-idealities. This is followed by details of VNA calibration algorithms in

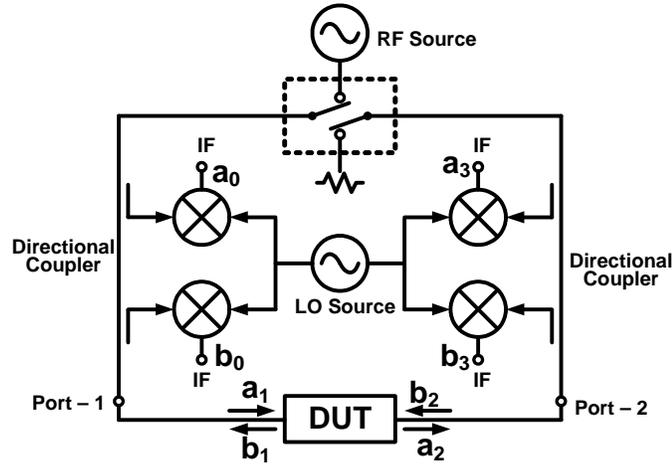


Figure 4.5: Simplified block diagram of a two-port VNA.

the next section.

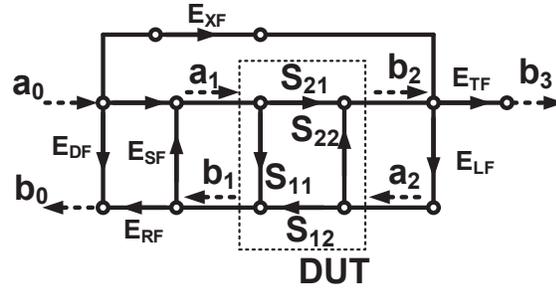
Figure 4.5 shows a generic block diagram representation of a fairly complex two-port VNA with a DUT connected. A shared tunable RF source is used to generate the incident waves at both the ports. Depending upon forward or reverse stimulations, the port is either connected to this RF source or terminated in a port impedance. Directional couplers are used to couple the incident and reflected waves at each port. The output of the directional couplers are fed to a mixer which down converts the RF signal to an intermediate frequency (IF). The second input of the mixer is fed with a local oscillator tuned to  $RF + IF$  frequency. The scattering parameters of the DUT are defined using the incident and reflected waves at the DUT reference plane as

$$S_{11} = \left. \frac{b_1}{a_1} \right|_{a_2=0} \quad (4.11)$$

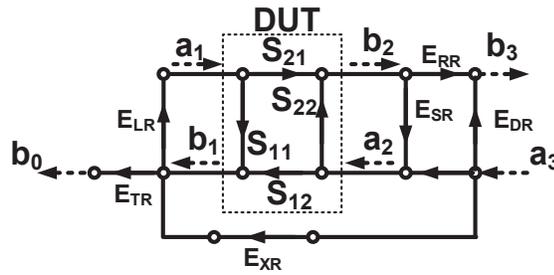
$$S_{12} = \left. \frac{b_1}{a_2} \right|_{a_1=0} \quad (4.12)$$

$$S_{21} = \left. \frac{b_2}{a_1} \right|_{a_2=0} \quad (4.13)$$

$$S_{22} = \left. \frac{b_2}{a_2} \right|_{a_1=0} \quad (4.14)$$



(a) Forward stimulation



(b) Reverse stimulation

Figure 4.6: Raw measured scattering parameters in the presence error mechanisms for forward and reverse stimulation.

and the raw scattering parameters are defined as

$$S_{11}^m = \frac{b_0}{a_0} \Big|_{a_3=0} \quad (4.15)$$

$$S_{12}^m = \frac{b_0}{a_3} \Big|_{a_0=0} \quad (4.16)$$

$$S_{21}^m = \frac{b_3}{a_0} \Big|_{a_3=0} \quad (4.17)$$

$$S_{22}^m = \frac{b_3}{a_3} \Big|_{a_0=0} \quad (4.18)$$

Here  $a_i$  and  $b_i$  are the incident and reflected waves at port  $i$ , respectively. The VNA *raw* S-parameters are calculated from  $a_0$ ,  $b_0$ ,  $a_3$ , and  $b_3$ , as indicated in the figure. To

calculate the DUT S-parameters from these *raw* S-parameters, the VNA needs to be corrected for the systematic errors introduced by the circuits and components used for the measurements. This task is performed through the process of calibration.

Calibration is a process of correcting for the non-idealities in the VNA. To represent these non-idealities, several error models are developed. Figure 4.6 shows a *twelve-term* error model for an equivalent representation of the DUT in the presence of error sources for a two-port VNA. Figure 4.6a shows the signal flow graph (see Appendix E for a review on signal flow graph) when a wave  $a_0$  at port 1 is incident and the reflected waves at both the port receivers are measured ( $b_0$  at port 1 and  $b_3$  at port 2). Figure 4.6b shows the signal flow graph when a wave  $a_3$  at port 2 is incident and the reflected waves at both the port receivers are measured. The error terms are represented with a two letter subscript, the first letter referring to the error mechanism, and the second letter referring to forward (**F**) or reverse (**R**) stimulation scenario.

Letter **D** refers to the directivity of the coupler (shown in Fig. 4.5) that is used for coupling incident and reflected waves into the mixers. Unlike conventional definition of directivity of a directional coupler, here the directivity error refers to leakage of the coupler. This error is the ratio between the power leakage from the RF source to  $b_0$  and loss from the RF source to  $a_0$ .

Letters **R** and **T** refer to the errors associated with reflection tracking and transmission tracking, respectively. These errors account for the loss of signal from the RF source to either of ports, and from the ports to  $b_0$  and  $b_3$ . Letter **S** and **L** refer to the errors associated with source and load match, respectively. These errors account for the mismatches at the RF source termination at the ports depending up on the forward or reverse stimulation. Letter **X** refers to the errors associated with the leakage or crosstalk from  $a_0$  to  $b_3$  in the forward stimulation mode and from  $a_3$  to  $b_0$  in the reverse stimulation mode.

As a summary, the error terms  $E_{RF}$ ,  $E_{TF}$ ,  $E_{TR}$ , and  $E_{RR}$  can be categorized as related to the tracking response;  $E_{SF}$ ,  $E_{LF}$ ,  $E_{LR}$ , and  $E_{SR}$  can be categorized as related to the mismatch;  $E_{DF}$ ,  $E_{XF}$ ,  $E_{XR}$ , and  $E_{DR}$  can be categorized as related to the leakage. These *twelve-term* error formulations are implemented in a typical VNA, therefore, a calibration algorithm needs to convert the calculated error quantities into these error terms.

For the forward stimulation shown in Fig. 4.6a, the measured S-parameters can be

written in terms of the the DUT S-parameters and the error terms as

$$S_{11}^m \equiv \frac{b_0}{a_0} = E_{DF} + \frac{E_{RF}(S_{11} - S_{11}S_{22}E_{LF} + S_{12}S_{21}E_{LF})}{1 - S_{22}E_{LF} - E_{SF}(S_{11} - S_{11}S_{22}E_{LF} + S_{12}S_{21}E_{LF})} \quad (4.19)$$

$$S_{21}^m \equiv \frac{b_3}{a_0} = E_{XF} + E_{TF} \frac{S_{21}}{1 - S_{11}E_{SF} - E_{LF}S_{22} + E_{SF}E_{LF}(S_{11}S_{22} - S_{12}S_{21})}. \quad (4.20)$$

Similarly, for the reverse stimulation shown Fig. 4.6b, the S-parameters can be derived from the flow-graph as

$$S_{22}^m \equiv \frac{b_3}{a_3} = E_{DR} + \frac{E_{RR}(S_{22} - S_{11}S_{22}E_{LR} + S_{12}S_{21}E_{LR})}{1 - S_{11}E_{LR} - E_{SR}(S_{22} - S_{11}S_{22}E_{LR} + S_{12}S_{21}E_{LR})} \quad (4.21)$$

$$S_{12}^m \equiv \frac{b_0}{a_3} = E_{XR} + E_{TR} \frac{S_{12}}{1 - S_{22}E_{SR} - E_{LR}S_{11} + E_{SR}E_{LR}(S_{11}S_{22} - S_{12}S_{21})}. \quad (4.22)$$

See Appendix E for the details of the derivation. After the VNA calibration, the DUT S-parameters are calculated from [74]

$$S_{11} = \frac{S_{11}^m - E_{DF}}{DE_{RF}} \left[ 1 + (S_{22}^m - E_{DR}) \frac{E_{SR}}{E_{RR}} \right] - \frac{S_{12}^m S_{21}^m E_{LF}}{DE_{TF} E_{TR}}, \quad (4.23)$$

$$S_{12} = \frac{S_{21}^m}{DE_{TF}} \left[ 1 + (S_{22}^m - E_{DR}) \frac{E_{SR} - E_{LF}}{E_{RR}} \right], \quad (4.24)$$

$$S_{21} = \frac{S_{12}^m}{DE_{TR}} \left[ 1 + (S_{11}^m - E_{DF}) \frac{E_{SF} - E_{LR}}{E_{RF}} \right], \quad (4.25)$$

$$S_{22} = \frac{S_{22}^m - E_{DR}}{DE_{RR}} \left[ 1 + (S_{11}^m - E_{DF}) \frac{E_{SF}}{E_{RF}} \right] - \frac{S_{12}^m S_{21}^m E_{LR}}{DE_{TF} E_{TR}}, \quad (4.26)$$

where

$$D = \left[ 1 + (S_{11}^m - E_{DF}) \frac{E_{SF}}{E_{RF}} \right] \left[ 1 + (S_{22}^m - E_{DR}) \frac{E_{SR}}{E_{RR}} \right] - \frac{S_{12}^m S_{21}^m E_{LF} E_{LR}}{E_{TF} E_{TR}}. \quad (4.27)$$

Now that we have discussed the error models and methods to calculate DUT S-parameters from the raw measurements, we will discuss commonly used approaches used for determining the error terms.

## 4.5 Approaches for On-chip Measurements

There are two approaches for capturing the systematic errors due to the VNA and the test fixtures used for embedding the DUT. First is the conventional two-step approach, also called *two-tier* approach and second is a one-step approach, also called *one-tier* approach. The two approaches differ in their definition of the *DUT*. In the two-tier approach, the DUT is defined as the structure that is being probed, while in the one-tier approach [75], the DUT is defined as the structure that is embedded in the test fixture, as shown in Fig. 4.2.

### 4.5.1 Conventional Two-tier Approach

The conventional approach for characterization of on-chip components, such as a spiral inductor, includes two steps, or tiers. First, the calibration algorithms, such as *short-open-load-through* (SOLT), *through-reflect-line* (TRL) [76], or *line-reflect-reflect-match* (LRRM) [77], accomplish the calibration of the vector network analyzers (VNA) up to the probe tip. This step shifts the reference plane of the measurement system to the tip of the probe [78]. Second, a de-embedding technique such as *open-through* [79], or *line-line*, or *open-short-through* [80] follows the calibration to extract the parasitics due to the probe pad and the access transmission lines from the probe pad to the DUT terminal.

### 4.5.2 One-tier Approach

In the one-tier approach [75], we perform the characterization of the device under test (DUT) in a single step. The approach uses on-chip calibration standards to perform the calibration of VNA error terms, which include cables, probes, probe pads, and interconnect parasitics. The DUT is embedded in the calibration *through* structure. This process shifts the reference plane of the measurement system to the terminals of the DUT.

The common part in both of these approaches is the calibration algorithm, and we will discuss commonly used algorithms in the next section.

## 4.6 Calibration Algorithms

The goal of VNA calibration is to move the reference plane to the end of the probe tip or to the reference plane of the DUT. An important requirement of a good calibration algorithm is accuracy over a broad bandwidth. It should rely on as few known calibration standards as possible because of the non-idealities associated with the fabrication of these calibration standards. In light of these requirements, we will review two such algorithms, viz. SOLT and TRL.

### 4.6.1 *Short-Open-Load-Through*

SOLT is one of the most commonly used calibration algorithm. After this calibration, the DUT reference plane is defined at the tip of the wafer probe. The calibration standards are probed on the impedance standard substrate (ISS). These standards are typically fabricated on a low loss materials. The contact resistance between the ISS material and the probe tip is designed to be very low.

#### 4.6.1.1 *Short Standard*

A *short* standard is realized by a conductor pad shorting the signal and ground probe tips. Ideally, this leads to a reflection coefficient of -1. Substituting  $S_{11} = S_{22} = -1$  in equations 4.19 and 4.21, the measured raw S-parameters can be directly written in terms of the error terms as

$$S_{11}^m = E_{DF} + \frac{-E_{RF}}{1 + E_{SF}} \quad (4.28)$$

$$S_{22}^m = E_{DR} + \frac{-E_{RR}}{1 + E_{SR}}. \quad (4.29)$$

#### 4.6.1.2 *Load Standard*

A broadband load impedance is placed at the reference plane between the signal and ground terminals. The value of the load is selected to be equal to the port impedance (typically 50  $\Omega$ ). A challenge here is to realize a very accurate load over a broad range of frequencies. The parasitic effects of the resistive material and the terminals lead

to a significant deviation from the ideal behavior of a real impedance. This is a major limitation in achieving broad bandwidth in this calibration algorithm, or other algorithms such as *LRRM*, which rely on a broadband load/match. Ideally, the match condition leads to a reflection coefficient of 0. Substituting  $S_{11} = S_{22} = 0$ , and  $S_{12} = S_{21} = 0$  in the raw measurement equations 4.19 and 4.21, it can be seen that, the  $E_{XF}$  and  $E_{XR}$  can be directly calculated from the  $S_{12}^m$  and  $S_{21}^m$  parameters. These values can be determined from one of the *open*, *through*, or *load* standards; however, it is typically determined from the *load* standard.

#### 4.6.1.3 *Open* Standard

The tip of the wafer probe is kept open which isolates the signal and ground terminals. Ideally, this leads to a reflection coefficient of 1. Substituting  $S_{11} = S_{22} = 1$  in the raw measurement equations, the measured S-parameters can be directly written in terms of the error terms as

$$S_{11}^m = E_{DF} + \frac{E_{RF}}{1 - E_{SF}} \quad (4.30)$$

$$S_{22}^m = E_{DR} + \frac{E_{RR}}{1 - E_{SR}}. \quad (4.31)$$

With the information from the *open* and *short* standards, the error terms  $E_{RF}$  and  $E_{RR}$  can be calculated by the two equations above.

#### 4.6.1.4 *Thru* Standard

Typically a known transmission line is implemented on the ISS to realize a *through* standard. This transmission line is assumed to be a lossless (or very low known loss) transmission line ( $S_{12} = S_{21} = 1$ ) and perfectly matched ( $S_{11} = S_{22} = 0$ ). This yields the measured S-parameters in terms of the error terms as

$$S_{11}^m = E_{DF} + \frac{E_{RF}E_{LF}}{1 - E_{SF}E_{LF}} \quad (4.32)$$

$$S_{21}^m = E_{XF} + \frac{E_{TF}}{1 - E_{SF}E_{LF}} \quad (4.33)$$

$$S_{12}^m = E_{XR} + \frac{E_{TR}}{1 - E_{SR}E_{LR}} \quad (4.34)$$

$$S_{22}^m = E_{XR} + \frac{E_{TR}}{1 - E_{SR}E_{LR}}. \quad (4.35)$$

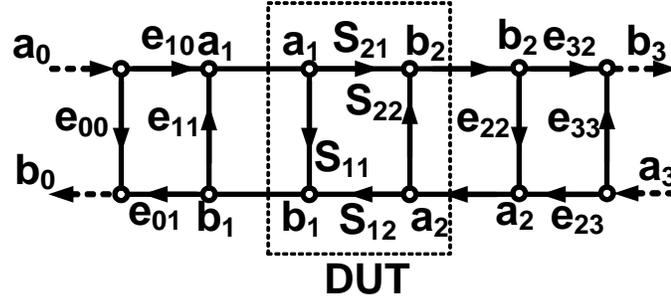
This set of four equations provide  $E_{TF}$ ,  $E_{LF}$ ,  $E_{TR}$ , and  $E_{LR}$  error terms. A known delay and loss for a *through* standard can be easily captured in the above formulation by setting  $S_{12} = S_{21} = e^{-\gamma l}$ , where  $\gamma$  is the known propagation constant and  $l$  is known length of the transmission line.

The basic SOLT algorithm formulation assumes ideal standards, and in practical situations, it is difficult to realize ideal standards. The *short* standard is limited by the parasitic resistance and inductance due to the realized short on the ISS. For the open standard, the fringing capacitance at the probe poses a limitation. To overcome such difficulty, wafer probe manufacturers often provide the short inductance and the open capacitance of the probe. With the load standard, it is very difficult to achieve a very accurate impedance over a broad range of frequency. The through structure lacks in accurate loss values over a broad range of frequencies. Studies such as [81] attempt to quantify the errors due to the non-idealities of the calibration standards used in *SOLT* algorithm.

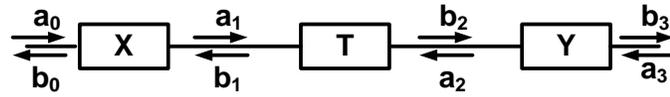
#### 4.6.2 Through-Reflect-Line

TRL is a widely used calibration method proposed by Engen and Hoer [76]. Unlike SOLT, this method is based on the *eight-term* error model shown in Fig. 4.7a. To discuss the algorithm, consider Fig. 4.7b which represents the signal flow graph of Fig. 4.7a in an equivalent network formulation. The DUT is represented by  $\mathbf{T}$  and is embedded in the two error boxes  $\mathbf{X}$  and  $\mathbf{Y}$ . Note that these matrices are the transfer scattering parameters [82]. These error boxes include the effects of cables, connectors, transformation of reference impedances, and VNA imperfections as explained in Section 4.4. The *raw* VNA measurements include the measurement of the ratios of  $b_i$  and  $a_j$ ,  $i, j \in [0, 3]$  referred to as  $S_{ij}^m$ . The DUT scattering parameters are denoted by  $S_{ij}$ , as before. Once the error terms are determined, the DUT scattering parameters are calculated as

$$T = X^{-1}T_m Y^{-1} \quad (4.36)$$



(a) Error model



(b) Equivalent representation in terms of T-parameters.

Figure 4.7: *Eight-term* error model and equivalent network representation.

where

$$X = \frac{1}{e_{10}} \begin{bmatrix} -e_{00}e_{11} + e_{10}e_{01} & e_{00} \\ -e_{11} & 1 \end{bmatrix} \quad (4.37)$$

$$Y = \frac{1}{e_{32}} \begin{bmatrix} -e_{22}e_{33} + e_{23}e_{32} & e_{22} \\ -e_{33} & 1 \end{bmatrix} \quad (4.38)$$

$$T_m = \frac{1}{S_{21}^m} \begin{bmatrix} -S_{11}^m S_{22}^m + S_{12}^m S_{21}^m & S_{11}^m \\ -S_{22}^m & 1 \end{bmatrix}. \quad (4.39)$$

It can be noted that, to solve for the error terms, the number of unknowns are seven and not eight because only the product terms  $e_{10}e_{01}$ ,  $e_{23}e_{32}$ , and  $e_{10}e_{32}$  are required, and not the individual error terms. Ultimately, this *eight-term* error model needs to be translated into the *twelve-term* error model for implementation in conventional VNAs. To do this, two additional terms are defined called the *switch-terms*. These switch terms are defined as

$$\Gamma_F \equiv \left. \frac{a_3}{b_3} \right|_{\text{Source at Port 1}} \quad (4.40)$$

$$\Gamma_R \equiv \left. \frac{a_0}{b_0} \right|_{\text{Source at Port 2}} . \quad (4.41)$$

Therefore the TRL calibration algorithm solves for a total of nine error terms, and these error terms are used to calculate the *twelve-term* error model.

#### 4.6.2.1 *Through* Standard

The through calibration standard is similar to the SOLT method. For on-chip calibrations, the through standard is a finite length ( $L_{\text{through}}$ ) transmission line. Due to this finite length, TRL is also referred to as the *Line-Reflect-Line* (LRL) algorithm. The reference plane can be shifted along this *through* transmission line for the DUT measurements. However, typically the DUT reference plane is defined as the center of the *through* transmission line. Along with measuring the raw scattering parameters of the *through* standard, the *switch-terms* are also directly measured by the VNA. By setting  $S_{12} = S_{21} = 1$  and  $S_{11} = S_{22} = 0$ , the error terms can be directly written in terms of the raw measurements. With this condition, the measurement reference plane is moved to the center of the *through* standard. The raw measurements along with *switch-terms* measurements give six equations.

#### 4.6.2.2 *Line* Standard

The *line* calibration standard(s) forms a key structure in determining the accuracy of the results. The electrical length of this *line* standard is at least  $20^\circ$  to  $160^\circ$  different than the *through* standard. At  $180^\circ$  (or half wavelength), the *through* standard will be the same as the *line* standard resulting in redundancy. Assuming this line impedance is the same as the reference impedance, the raw measurements yield another four equations to solve the problem. However, two more unknowns, the complex propagation constant, is added, thus making the total number of unknowns to be 11.

#### 4.6.2.3 *Reflect* Standard

The *reflect* standard, similar to the SOLT algorithm, is basically an open or a short at the DUT reference plane. These standards can be realized with a via short (via

impedance non-idealities) or an open line (open line fringe capacitance and radiation). This adds two more equations and one unknown as the reflection coefficient of the reflect standard, thus making the total number of equations to be equal to twelve for the same number of unknowns.

### 4.6.3 Characteristic Impedance Calculations in TRL

So far in the discussion, we have assumed that the calibration standards have the same characteristic impedance as that of the port or reference impedance of the VNA over the frequency of interest. The main reason for the calibration standards to deviate from the port impedance is the presence of losses in the conductors and the dielectric material between the signal and ground. The condition of constant characteristic impedance is easier to meet for off-chip calibration standards where a very high conductivity conductor material such as gold can be used. Achieving low conductor loss is difficult for on-chip calibration standards; however, it is possible to coat the probing pads with gold. Typically for advanced IC manufacturing process metals, such as copper and aluminum, alloys are used. Therefore, the transmission lines realized in these materials are lossy and the characteristic impedance of the line changes as a function of frequency. This leads to difficulties in the definition of the standards. Williams et al. [83] proposed a method to estimate the characteristic impedance of the line from the propagation constant. The propagation constant of a transmission line can be calculated using raw data of two lines [84]. The method relies on the assumption of a low or no loss inter-layer-dielectric (ILD) material used between signal and ground. With this assumption, the per unit length (p.u.l.) conductance (G) can be ignored and the p.u.l. capacitance (C) can be assumed to be constant over a band of frequencies of interest. Thus the characteristic impedance can be determined as

$$Z_0 = \frac{\gamma}{j\omega C}. \quad (4.42)$$

Propagation constant  $\gamma$  can be calculated from the raw measurements directly using *through* and *line* measurements. The capacitance of the lines can also be measured using DC measurements [85] or obtained by electromagnetic simulations [86]. Once the characteristic impedance is determined, a conventional renormalization technique is used to set the reference impedance equal to the constant port impedance [82].

#### 4.6.4 Multi-line TRL

The conventional TRL calibration technique is inherently narrow band as it has a limitation in frequencies over which the *line* standard can be used. This band is limited to the frequencies corresponding to  $20^\circ$  to  $160^\circ$  phase of the transmission line. To overcome this limitation, multiple transmission line standards are used; however, discontinuities between the line standards is an issue. To overcome this limitation, Marks proposed a *Multi-line through reflect line* (MTRL) [87] algorithm. In this work, we adopt this calibration technique implemented in MultiCal [88]. The MTRL calibration algorithm relies on *multiple lines* of known capacitance p.u.l., which are used to determine the characteristic impedance of the *line* standard [83], as discussed before. In addition, a *through* and a *reflect* complete the calibration standards. In contrast, the calibration algorithms employed in the two-tier methods, such as SOLT, rely on a known broadband *load* (typically  $50\ \Omega$ ) and a known *through* delay (phase shift). The less constrained MTRL calibration standards make it an attractive method for on-chip characterization. However, this method has the drawback of requiring large chip real estate to implement the multiple line standards, especially to achieve accuracy at lower frequencies.

##### **Design of On-chip Calibration Standards**

We designed the MTRL calibration standards in a  $0.18\ \mu\text{m}$  Bi-CMOS process [37]. This process has six metal layers. Figure 4.8 shows a die photo of a *line* standard ( $L_i$ ) embedded in the *through* standard ( $L_{\text{through}}$ ). Figure 4.9 shows the cross-sectional view at the MTRL reference plane (center of the *through* standard). We see from the figure that the transmission line signal conductor is laid out on the top metal layer (M6) with ground on M3 through M1. The ground planes are connected to each other through inter-metal-layer vias and to the silicon substrate through a p-tap. In addition, the ground planes are periodically slotted to meet the foundry imposed stress requirements, except for a width of  $80\ \mu\text{m}$  in the cross-section centered underneath the signal conductor. This assures that the transmission line characteristics are unaltered.

To design the transmission lines, we simulated various transmission line structures (cross-section shown in Fig. 4.9) in a full-wave electromagnetic solver (HFSS) [11]. The full-wave electromagnetic solver is used to calculate the transmission line  $Z_o$  and  $\gamma$  from

the S-parameters.  $Z_o$  is obtained as

$$Z_o = Z_p \sqrt{\frac{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}}} \quad (4.43)$$

where  $Z_p$  is the port impedance ( $50\Omega$ ). The propagation constant  $\gamma$  is obtained as

$$\gamma = \alpha + j\beta = \frac{1}{L} \cosh^{-1} \left( \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{2S_{21}} \right) \quad (4.44)$$

where  $L$  is the length of the transmission line.

The selection of transmission line lengths is a crucial part in the design of MTRL standards. Based on full-wave electromagnetic simulations, we designed the transmission line structure using the technology process parameters (typical values of metal thicknesses, inter-layer dielectric thicknesses, material properties, etc.). A line width of  $12 \mu m$  for the cross-section shown in Fig. 4.9 provides a characteristic impedance of approximately  $50 \Omega$  at 10 GHz and varies from  $54 \Omega$  to  $48.5 \Omega$  within the desired range of 1 GHz to 40 GHz, mainly due to the eddy-current losses in the metal (inter-layer dielectric loss tangent is assumed to be negligible). We gave special consideration to the selection of the *multiple-line* lengths to cover the desired frequency range. Figure 4.10 shows the phase of the designed transmission lines. We selected appropriate upper and lower bounds for the phase as  $45^\circ$  and  $135^\circ$ , respectively (a conservative range). The maximum length possible on the chip determines the lower bound on the frequency range. For this test chip, the die size is  $5 \text{ mm} \times 5 \text{ mm}$ . Excluding the launching probe pads, the *through* line ( $200\mu m$ ), and the foundry imposed edge to metalization rules, the maximum length of the line is 4.3 mm. Table 4.1 shows the frequency bands for the three different transmission line lengths. The frequencies corresponding to  $135^\circ$  and  $45^\circ$  in phase gives the upper and lower frequency bounds, respectively. We select the line lengths starting from the longest line possible for a given test chip. The frequency at which this line ( $L_i$ ) exhibits  $135^\circ$ ,  $f_{i+1}$ , gives the next line length as

$$L_{i+1} = \frac{45}{\beta_i}, \quad (4.45)$$

where  $\beta_i$  is the phase constant (in  $^\circ/\text{m}$ ) at frequency  $f_{i+1}$ . The length of the *through* standard is sufficiently long ( $100 \mu m$ ) on each side of the DUT to make sure only the

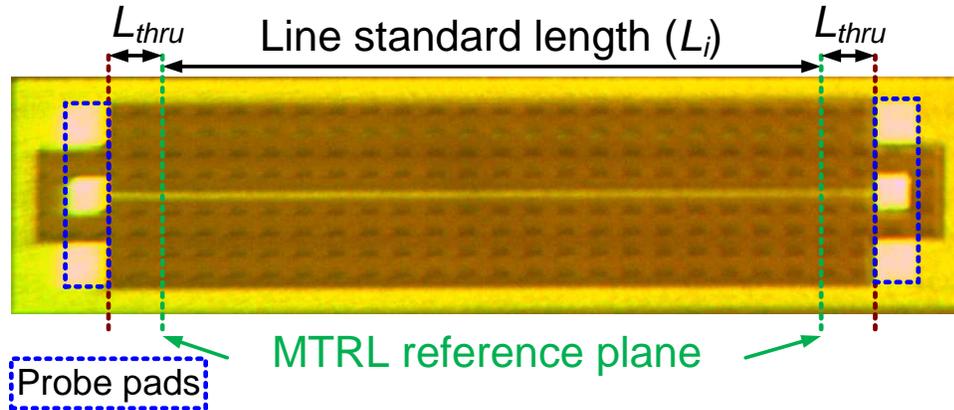


Figure 4.8: The fabricated *Line* calibration standard. Vertical dashed lines indicate reference planes.

Table 4.1: MTRL Line Standard Design

	Length	Freq. lower bound	Freq. upper bound
Line1	4.300 mm	4.28 GHz	13.77 GHz
Line2	1.433 mm	13.77 GHz	42.23 GHz
Line3	0.477 mm	42.23 GHz	127.61 GHz

dominant mode propagates (quasi-TEM) and higher order modes die out leading up to the DUT. This also makes sure the DUT terminal is far away from the discontinuity due to probe pads. The *reflect* standard is an open transmission line of length  $100 \mu\text{m}$ . The *through* de-embedding structure designed for the two-tier method acts as a *through* MTRL standard and the *open* de-embedding structure as a *reflect* MTRL standard.

Recently, statistical calibration methods such as [89] have been developed for calibration as well as uncertainty analysis. Further, there are methods such as *line-reflect-match* (LRM) and *line-reflect-reflect-match* (LRRM) [77] which attempt to overcome the limitations of the SOLT algorithm.

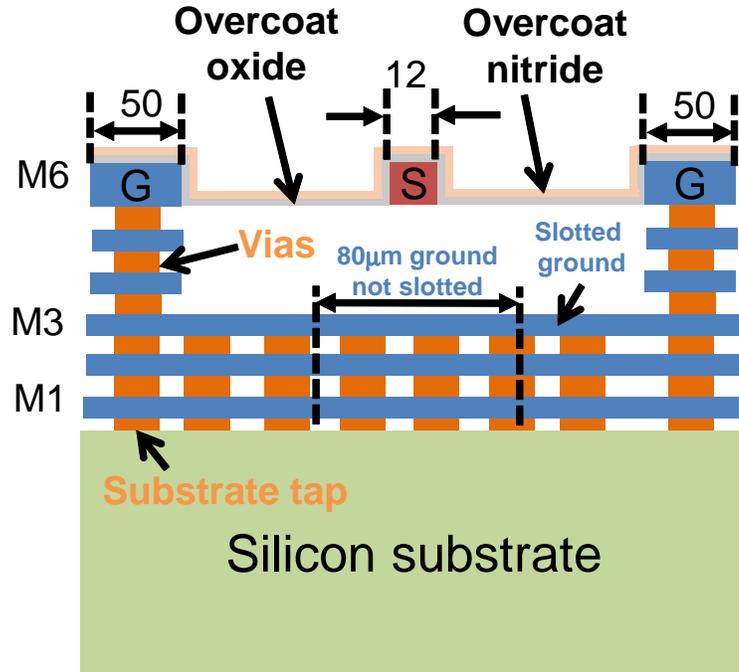


Figure 4.9: Cross-sectional view of line/through standard at the reference plane for one-tier calibration (dimensions in  $\mu m$ ).

## 4.7 De-embedding Techniques

The next step in a conventional two-tier method is de-embedding of the probe pad and access line interconnect parasitic effects after calibration. Figure 4.11 shows an equivalent representation of the the parasitic effects. Here,  $Y_1(\omega)$  and  $Y_2(\omega)$  represent the probe pad shunt admittance at port 1 and 2, respectively. Further, the series impedance  $Z_{1r}(\omega)$  and  $Z_{2r}(\omega)$  represent the parasitic effect of the access lines used for interconnection between probe pad and DUT terminal at port 1 and 2, respectively.

To de-embed the DUT, researchers have investigated several methods. Here we will review two representative methods.

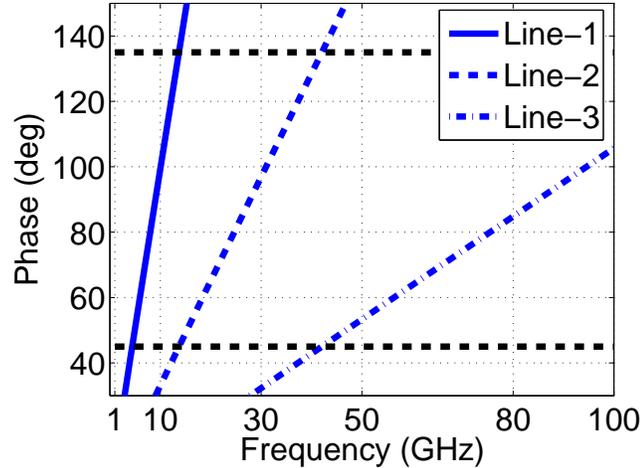


Figure 4.10: The simulated phase constant of the *Line* calibration standard. Horizontal dashed lines indicate a phase of  $45^\circ$  and  $135^\circ$ , respectively.

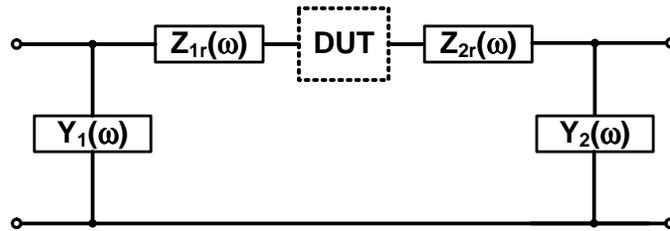


Figure 4.11: Equivalent circuit model for the DUT embedded in the test fixture.

#### 4.7.1 *Open-through* De-embedding Technique

This technique relies on the assumption that the interconnect access lines are shorter than a fraction of the minimum wavelength and, therefore, can be represented as a lumped elements. Figure 4.12 shows the DUT embedded in the *through* and *open* de-embedding structures for a two-port scenario.

The DUT Y-parameters are calculated as

$$Y_{DUT} = \left[ (Y_{meas} - Y_{open})^{-1} - (Y_{through} - Y_{open})^{-1} \right]^{-1}, \quad (4.46)$$

where  $Y_{meas}$  is the Y-parameter of the DUT embedded in the test fixture,  $Y_{open}$  is the

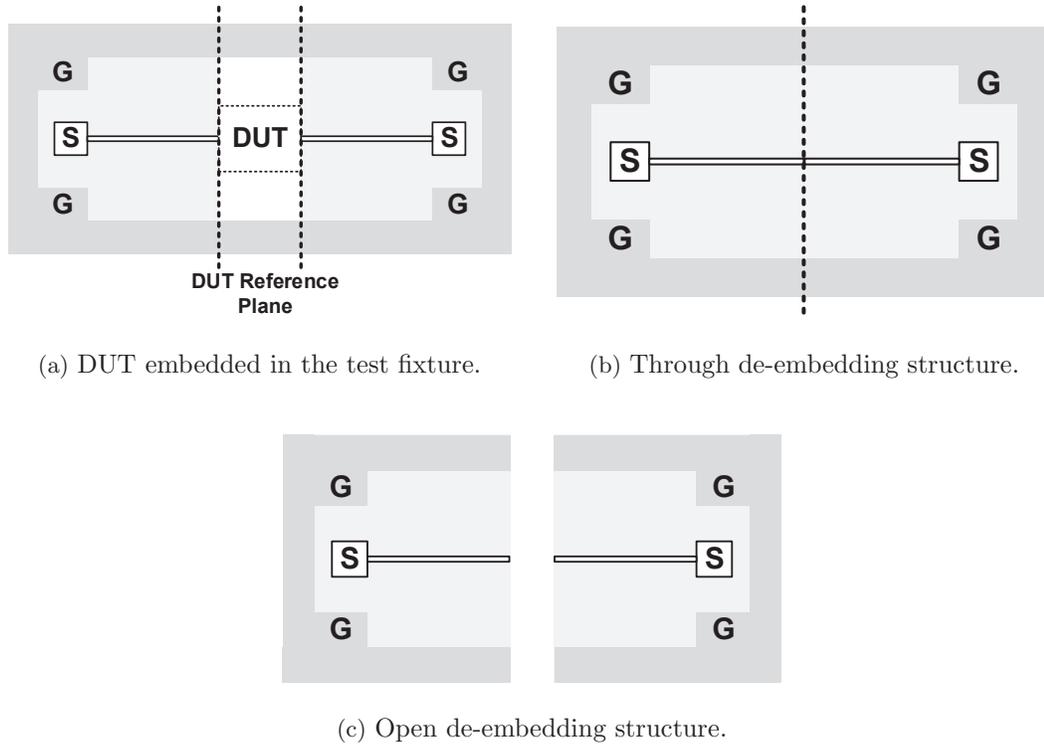


Figure 4.12: Open-through de-embedding method structures.

Y-parameter of the *open* de-embedding test fixture, and  $Y_{through}$  is the Y-parameter of the *through* de-embedding test fixture.

#### 4.7.2 Line-line

The *line-line* de-embedding technique [90] is based on the calculation of the DUT ABCD parameters by cascading the access transmission line parameters. It utilizes two transmission lines to determine the ABCD parameters of the access transmission lines. This technique is based on similar studies published in [91].

## 4.8 Uncertainty Error Analysis

Up to this point in this chapter, we have assumed the steps in measurement procedure such as acquiring data for calibration algorithms and de-embedding techniques to be error free. There are several sources of systematic and random errors in typical on-chip measurements. The systematic error, as defined in Section 4.2, are systematic variations that are caused by sources such as variations in the calibration kit standards used. The random errors include sources such as instrument drift, cable instability, wafer probe contact resistance, noise, etc. To confirm the repeatability and reproducibility of the measurement results, we performed multiple measurements at different times and for multiple probings. These errors result in uncertainties in the scattering parameter measurement results, which are further propagated to the derived parameters such as the Y-parameters and DUT electrical parameters such as one-port inductance ( $L_{11}$ ), quality factor ( $Q_{11}$ ), and resistance ( $R_{11}$ ).

To propagate the uncertainties, there are several methods such as a linearization of the transformation function around the mean value, non-linear transformation [92], Monte-Carlo simulations, polynomial chaos [93], etc. In this thesis, we will use the linearization based approach and compare it to Monte-Carlo simulations.

### 4.8.1 Linearity Based Error Analysis

The measurement results can be analyzed for repeatability and reproducibility related errors using the laws of propagation of uncertainty [68]. This statistical error analysis is performed for multi-line TRL measurements. The analysis is performed by repeating the probing of devices for a given calibration coefficients. The repeated measurements generate a set of S-parameters over the desired frequency range. We first calculate the covariance matrix of the measured S-parameters at each frequency as [94]

$$\Sigma_S = \begin{bmatrix} \sigma(S_{11}^r, S_{11}^r) & \sigma(S_{11}^r, S_{11}^i) & \sigma(S_{11}^r, S_{12}^r) & \cdots & \sigma(S_{11}^r, S_{22}^i) \\ \sigma(S_{11}^i, S_{11}^r) & \sigma(S_{11}^i, S_{11}^i) & \sigma(S_{11}^i, S_{12}^r) & \cdots & \sigma(S_{11}^i, S_{22}^i) \\ \sigma(S_{12}^r, S_{11}^r) & \sigma(S_{12}^r, S_{11}^i) & \sigma(S_{12}^r, S_{12}^r) & \cdots & \sigma(S_{12}^r, S_{22}^i) \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ \sigma(S_{22}^i, S_{11}^r) & \sigma(S_{22}^i, S_{11}^i) & \sigma(S_{22}^i, S_{12}^r) & \cdots & \sigma(S_{22}^i, S_{22}^i) \end{bmatrix} \quad (4.47)$$

Here, superscript  $r$  and  $i$  refer to the real and imaginary part of the corresponding S-parameter, respectively.  $\sigma(S_{ij}^{r,i}, S_{mn}^{r,i})$  is the covariance between  $S_{ij}^{r,i}$  and  $S_{mn}^{r,i}$  and is defined as  $E(S_{ij}^{r,i})E(S_{mn}^{r,i}) - E(S_{ij}^{r,i} \cdot S_{mn}^{r,i})$ , where  $E(\cdot)$  is the expected value of the argument. Next the uncertainties in the S-parameters can be propagated to the Y-parameters by a linearized transformation leading to

$$\Sigma_Y = J\Sigma_S J^T. \quad (4.48)$$

Here,  $J$  is the Jacobian matrix. For  $S$ - to  $Y_{11}$ - parameter conversion, the  $J$  matrix is given as

$$J = \begin{bmatrix} \frac{\partial Y_{11}^r}{\partial S_{11}^r} & \frac{\partial Y_{11}^r}{\partial S_{11}^i} & \frac{\partial Y_{11}^r}{\partial S_{12}^r} & \frac{\partial Y_{11}^r}{\partial S_{12}^i} & \frac{\partial Y_{11}^r}{\partial S_{21}^r} & \frac{\partial Y_{11}^r}{\partial S_{21}^i} & \frac{\partial Y_{11}^r}{\partial S_{22}^r} & \frac{\partial Y_{11}^r}{\partial S_{22}^i} \\ \frac{\partial Y_{11}^i}{\partial S_{11}^r} & \frac{\partial Y_{11}^i}{\partial S_{11}^i} & \frac{\partial Y_{11}^i}{\partial S_{12}^r} & \frac{\partial Y_{11}^i}{\partial S_{12}^i} & \frac{\partial Y_{11}^i}{\partial S_{21}^r} & \frac{\partial Y_{11}^i}{\partial S_{21}^i} & \frac{\partial Y_{11}^i}{\partial S_{22}^r} & \frac{\partial Y_{11}^i}{\partial S_{22}^i} \end{bmatrix} \quad (4.49)$$

To calculate the Jacobian matrix for this conversion, we represent the Y-parameters in terms of their real and imaginary parts as  $Y_{11}^{r,i}$ .

#### 4.8.2 Monte-Carlo Based Error Analysis

The uncertainty analysis can be performed using the linearization of the transformation function around the mean ( $\mu$ ) value, as shown in the previous subsection. However, as the transformation functions contain significant non-linear operations, this assumption may become inappropriate. Therefore, we employ a Monte Carlo simulations (MCS) based approach [95] to capture the impact of the non-linearities in the transformation. We treat the real and imaginary parts of the S parameters as correlated random variables ( $X_1, X_2, \dots, X_M$ ). Thus we have eight random variables ( $M = 8$ ) for a two-port S-matrix. From the  $N$  repeated measurement, we obtain an  $N \times M$  matrix of data where each column represents a random variable and each row indicates an observation. This matrix is used to calculate the covariance matrix ( $\Sigma_S \in \mathbb{C}^{M \times M}$ ) and mean vector ( $\mu_S \in \mathbb{C}^{1 \times M}$ ). From the measured mean and standard deviation, we generate 1000 samples using a multi-variate Gaussian probability distribution function formulated as [96]

$$f(x, \mu_S, \Sigma_S) = \frac{1}{\sqrt{|\Sigma_S|} (2\pi)^M} e^{-\frac{1}{2}(x-\mu_S)\Sigma_S^{-1}(x-\mu_S)^T}. \quad (4.50)$$

We performed a non-linear transformation on this random sample space from S to Y using a Monte-Carlo simulation (MCS). In the case of spiral inductors, we are interested in  $\text{Re}(Y_{11})$  and  $\text{Im}(Y_{11})$ . The MCS produces 1000 samples of these two random variables, which are used to calculate the  $2 \times 2$   $\Sigma_Y$  matrix and  $1 \times 2$   $\mu_Y$  matrix at each frequency point. In the case of the one-tier MTRL approach, we propagate uncertainties from S-parameters to Y-parameters and further to DUT electrical parameters. In the case of two-tier SOLT approach, we propagate uncertainties from S-parameters of each embedded DUT, open, and through de-embedding structures to the Y-parameters, further propagated through the de-embedding procedure to the Y-parameters of the DUT and finally to the DUT electrical parameters.

## 4.9 Results

In this work, we employ the *short-open-load-through* (SOLT) calibration algorithm implemented in WinCal [97] followed by an *open-through* de-embedding technique as discussed before. For calibration, we use an off-chip commercial impedance substrate standard (ISS) [97]. We fabricated a *through* de-embedding structure of  $200 \mu\text{m}$  ( $100 \mu\text{m}$  interconnect on each side) and an *open* de-embedding structure. Figure 4.13 shows the DUT with  $100 \mu\text{m}$  lead in lines. Figure 4.14 shows the cross-sectional view at the probing pads. The width of the signal probe pad (G-S-G  $150 \mu\text{m}$ ) is  $80 \mu\text{m}$  to minimize the pad capacitance, while at the same time it is sufficiently large to provide a reliable probe landing [98].

### 4.9.1 Device Under Test

The DUT for this study is a spiral inductor designed for 2.4 GHz RF circuits. We designed a 3.5 nH rectangular spiral inductor with a peak quality factor of 10 at 2.4 GHz. The spiral inductor has 4.5 turns with outer dimensions of  $200 \mu\text{m} \times 200 \mu\text{m}$ , width of  $12 \mu\text{m}$ , and inter-winding spacing of  $2.5 \mu\text{m}$ . Figure 4.13 shows the DUT embedded in the calibration structure. We extract the DUT parameters from the Y-parameters converted from the measured two-port S-parameters. The quantities of interest are one-port inductance ( $L_{11}$ ), resistance ( $R_{11}$ ), and quality factor ( $Q_{11}$ ) calculated as:

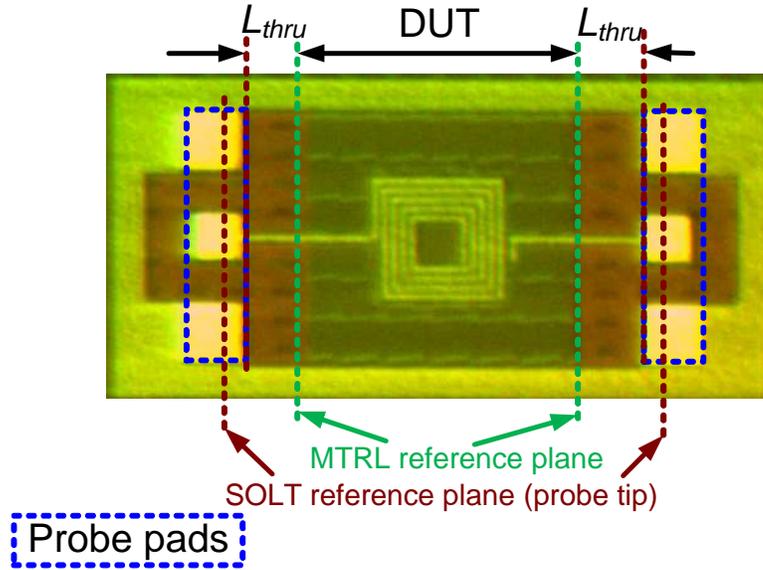


Figure 4.13: The DUT (4.5 turn rectangular spiral inductor) embedded in MTRL through calibration standard.

$$L_{11} = \text{Im} \left( \frac{1/Y_{11}}{\omega} \right) \quad (4.51)$$

$$R_{11} = \text{Re} (1/Y_{11}) \quad (4.52)$$

$$Q_{11} = -\frac{\text{Im}(Y_{11})}{\text{Re}(Y_{11})}. \quad (4.53)$$

#### 4.9.2 Full-wave Electromagnetic Simulations

The measurement results are compared with full-wave em simulation results. The electromagnetic simulations are setup to imitate the DUT as closely as possible to the fabricated test structure. Figure 4.15 shows the spiral inductor fabricated with two lumped ports at the terminals, which mimic the wave launch from the probe pad. The ground reference for both ports is connected together replicating the fabricated DUT. The ground is connected to the silicon substrate using a tap. A long simulation time and fine mesh compared to the skin depth was setup and convergence of the results was

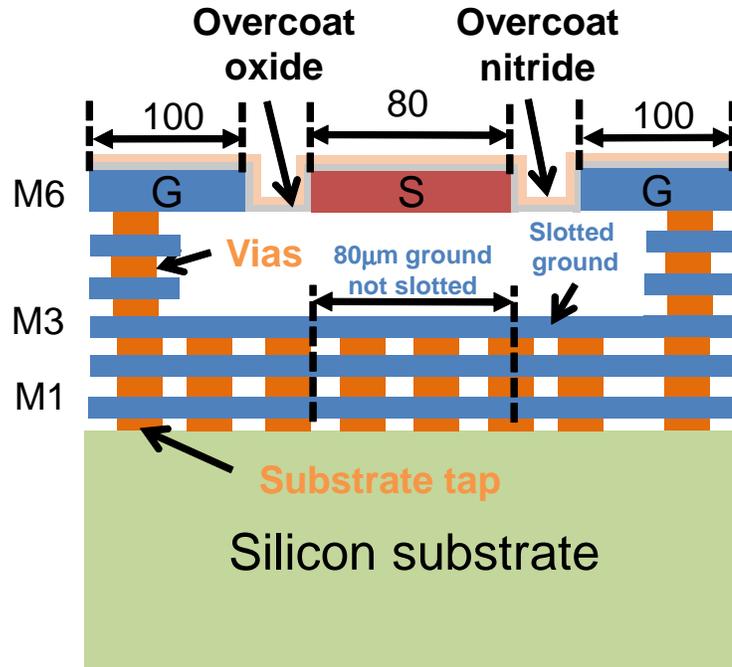


Figure 4.14: Cross-sectional view of GSG probe pads (dimensions in  $\mu m$ ).

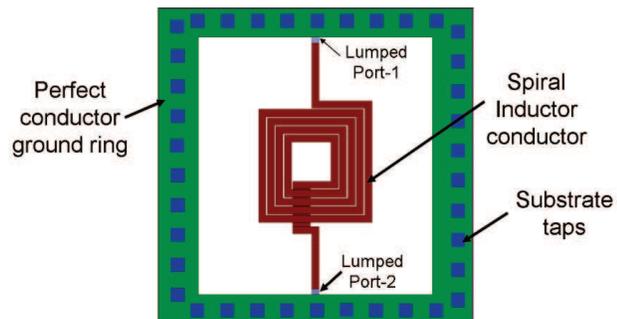


Figure 4.15: Spiral inductor full-wave simulation setup.

confirmed. For the simulations, we ignored the uncertainties in material properties and process dimensions.

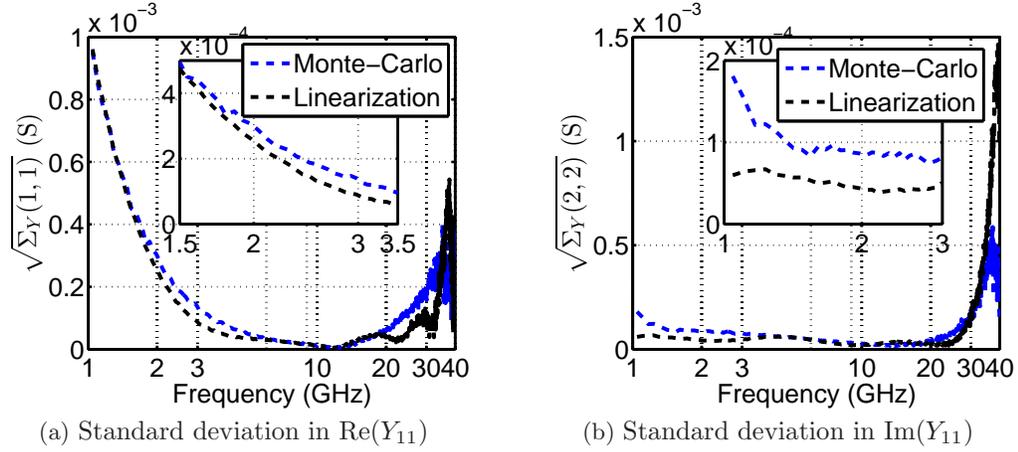


Figure 4.16: Comparison of standard deviation in  $Y_{11}$  parameters calculated using linearization approach and Monte-Carlo simulations.

### 4.9.3 Comparison of Linearization and MCS Approach

In this subsection we compare the results of the uncertainties calculated using linearization based approach and the Monte-Carlo simulations (MCS). We calculated the Jacobian matrix elements using Matlab symbolic toolbox [99]. Figure 4.16 shows the comparison between the two methods. As can be seen from the figure, the linearization based approach is limited in accurately determining the uncertainties. Therefore in this work we use the MCS approach.

### 4.9.4 Measurement Results

We performed the measurements using an HP 8510C VNA and Cascade Microtech GSG Infinity probes [97] with the aforementioned two methods. We compare the measurement results with the full-wave electromagnetic simulation results of the DUT. Figure 4.17 shows the  $\mu \pm 2\sigma$  of the  $\text{Re}(S_{11})$  from the five repeated measurements. We assume a normal distribution of the S-parameters to calculate the uncertainties in Y-parameters. Figure 4.18 shows the  $\mu \pm 2\sigma$  of the  $\text{Re}(Y_{11})$  propagated from  $[\mathbf{S}]$ . Further, Figs. 4.19b, 4.19a, and 4.19c show the uncertainties in the derived circuit parameters. The measurement results agree well with the simulation results, giving good confidence in

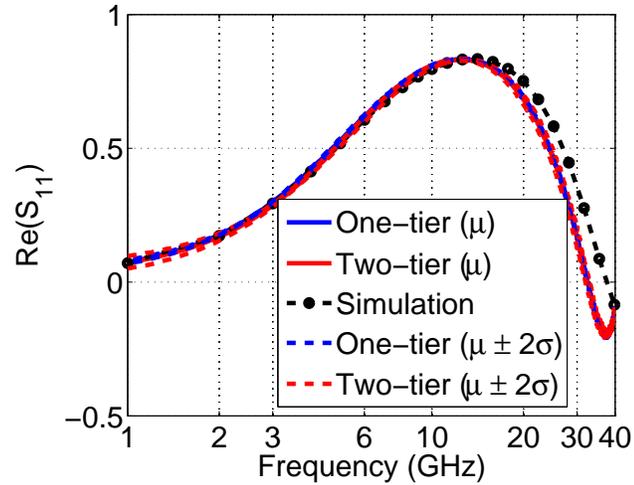


Figure 4.17:  $\text{Re}(S_{11})$  ( $\mu \pm 2\sigma$ ) of measured spiral inductor and comparison with full-wave solver.

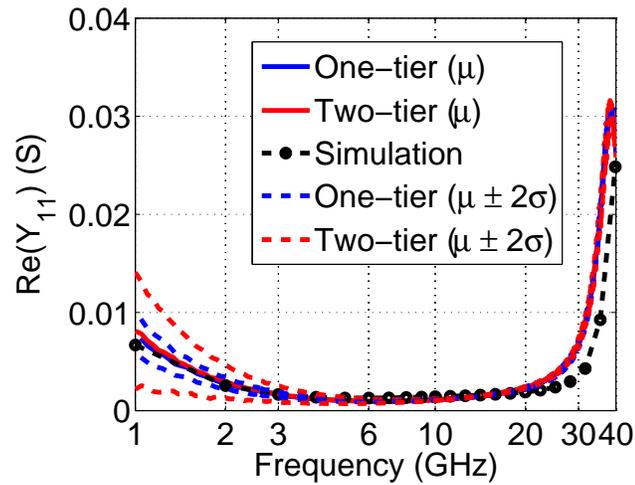


Figure 4.18:  $\text{Re}(Y_{11})$  ( $\mu \pm 2\sigma$ ) of measured spiral inductor and comparison with full-wave solver.

the measurement procedure. The figures also show large variations in  $Y_{11}$  and  $Q_{11}$  for the two-tier method. Also, we see some unexpected noise in  $R_{11}$  and  $Q_{11}$  of the one-tier results beyond 30 GHz.

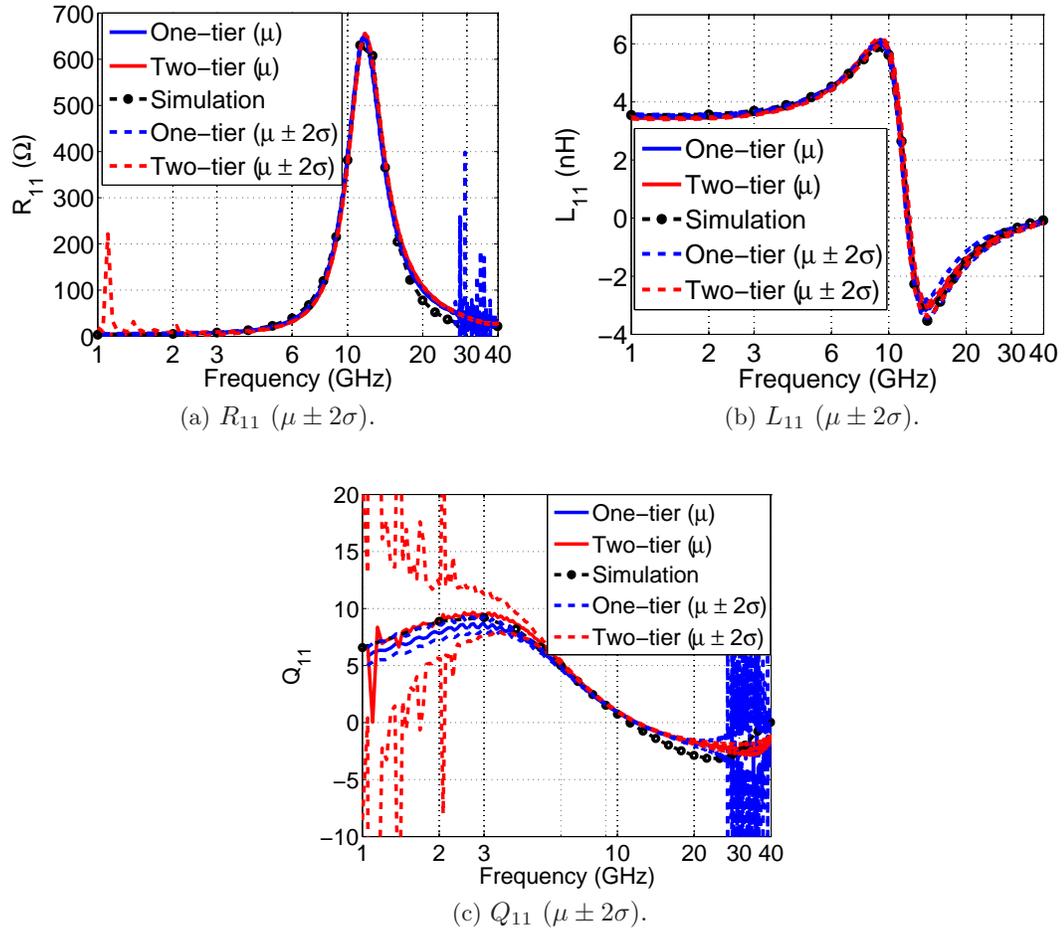


Figure 4.19: The uncertainty analysis and comparison with full-wave solver.

## 4.10 Conclusion

In this chapter, we provided a review of VNA error models and algorithm to capture the terms in the model. We discussed the statistical error analysis and found the linearization based approach limited in determining the uncertainties, and therefore we rely on MCS for the uncertainty calculations. We discussed the design of MTRL on-chip calibration standards for a one-tier method of characterization proposed by Williams et al. [100]. To capture the random errors in the measurement setup, we performed a basic Monte

Carlo based statistical error analysis. Also, we compared the results with a full-wave electromagnetic solver. The results for the measured DUT spiral inductor agree well with the simulation results. This demonstrates an accurate characterization approach for on-chip spiral inductors with the multi-line TRL method.

## Chapter 5: Model Validation using On-chip Passive Component Characterization

### 5.1 Introduction

In this thesis, so far we have discussed the modeling and characterization methods for on-chip passive components. In this chapter we demonstrate the accuracy verification of our proposed modeling techniques. This verification is achieved through the fabrication of the representative test structures in 0.18  $\mu\text{m}$  BiCMOS process. This chapter is organized as follows. Section 5.2 shows the design and fabrication of transmission line structures without and with metal fill followed by a comparison between full-wave simulation, measurement, and model results for the fabricated test structures. Section 5.3 shows the design and fabrication of spiral inductor structures without and with metal fill followed by a comparison between measurement and model results for the fabricated test structures. Finally, Section 5.4 concludes the chapter.

### 5.2 Transmission Lines

In this section, we verify the accuracy of the capacitance modeling method proposed in Chapter 2 and eddy-current modeling method presented in Chapter 3. For this verification, we discuss the design and fabrication of the test structures, outline the parameters of interest, and show the comparison of model results with full-wave simulation and measurement results up to 40 GHz.

#### 5.2.1 Design and Fabrication of Test Structures

We designed the embedded microstrip transmission line test structures in a 0.18  $\mu\text{m}$  Bi-CMOS process [37]. This process has six metal layers. Figure 5.1 shows a die photo of this line embedded in the *through* MTRL calibration standard. Figure 5.2 shows the cross-sectional view of the transmission line without metal fill at the calibration reference

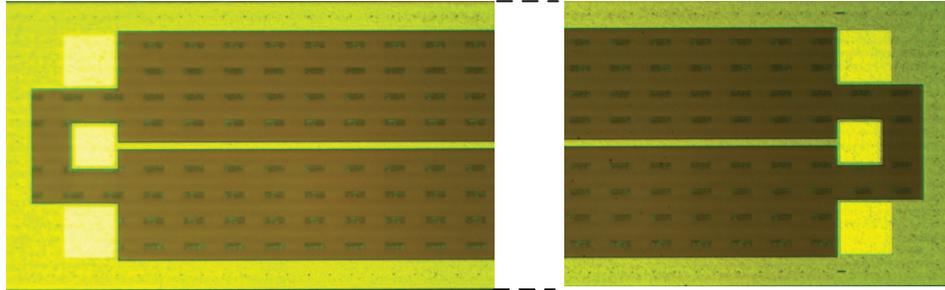


Figure 5.1: Die photo of transmission line without metal fill

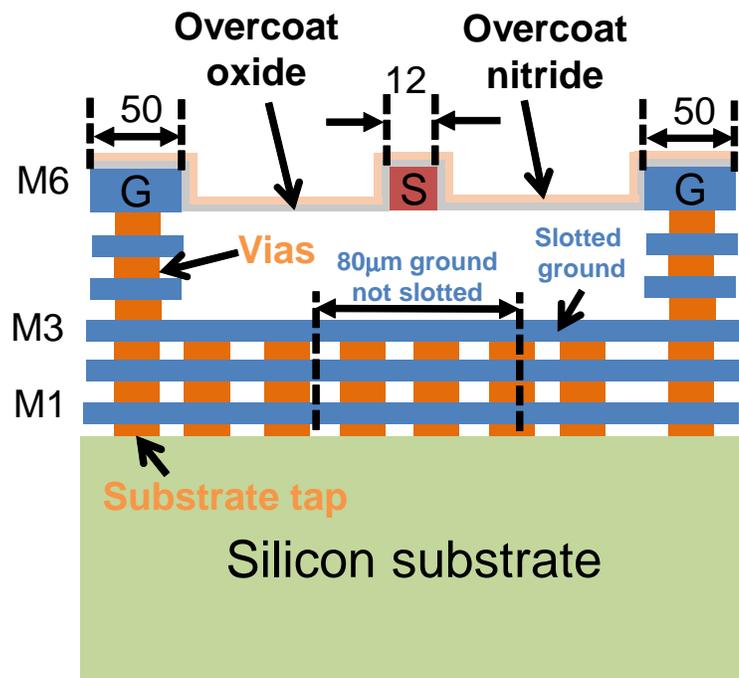


Figure 5.2: Cross-sectional view of transmission line without metal fill (dimensions in  $\mu m$ ).

plane. The transmission line signal conductor is laid out on the top metal layer (M6) with ground on M3 through M1. The ground planes are connected to each other through inter-metal-layer vias and to the silicon substrate through p-taps. In addition, the ground planes are periodically slotted to meet the foundry imposed stress requirements, except for a width of  $80 \mu m$  centered underneath the signal conductor. This assures that the

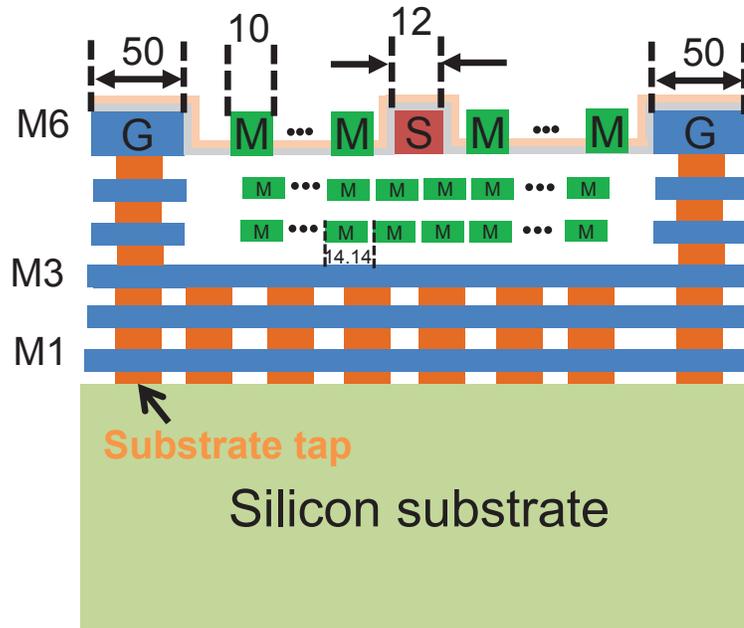


Figure 5.3: Cross-sectional view of transmission line with metal fill (dimensions in  $\mu m$ ).

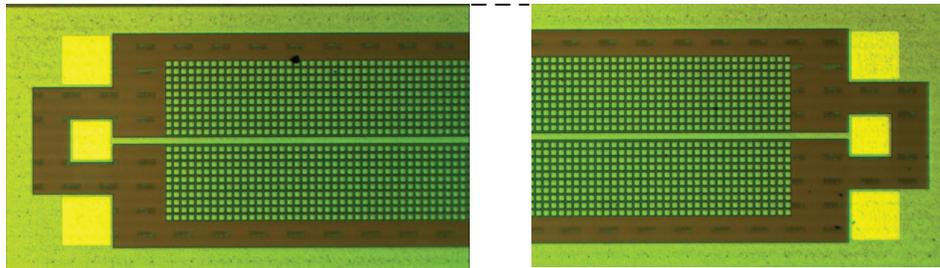


Figure 5.4: Die photo of transmission lines with metal fill of size  $10 \mu m \times 10 \mu m$  and 50 % metal density.

transmission line characteristics are unaltered.

To design the transmission lines, we simulated various transmission line structures (cross-section shown in Fig. 5.2) in a full-wave electromagnetic simulator [11]. The S-parameters obtained from the full-wave electromagnetic simulator are used to calculate

the transmission line  $Z_o$  and  $\gamma$ .  $Z_o$  is obtained as

$$Z_o = Z_p \sqrt{\frac{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}}} \quad (5.1)$$

where  $Z_p$  is the port impedance. The propagation constant  $\gamma$  is obtained as

$$\gamma = \alpha + j\beta = \frac{1}{L} \cosh^{-1} \left( \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{2S_{21}} \right) \quad (5.2)$$

where  $L$  is the length of the transmission line. Here the length of the transmission line is 1.433 mm. The designed characteristic impedance is about 50  $\Omega$  at 10 GHz.

To verify the accuracy of our metal fill modeling methods, we fabricated the exact same line with metal fill. Figure 5.4 shows the transmission line die photo with metal fill and Fig. 5.4 shows the cross-sectional view of the structure at the center of a unit cell. In a unit cell 20 metal fills of size 10  $\mu\text{m} \times 10 \mu\text{m}$  and 50 % metal density are added on each layers (M6 through M4). The buffer distance (edge to edge distance) between signal line (S) and metal fill (M) on M6 is 5  $\mu\text{m}$ .

## 5.2.2 One-tier Measurements

We performed the measurements on the test structures using MTRL on-chip calibration method described in Chapter 4. We compare the measurement results with full-wave simulation results as well. Figures 5.5a and 5.5b show the per unit length (p.u.l.) resistance and inductance, respectively, of the transmission lines without and with metal fill. After the insertion of metal fill, the resistance is increased by 39% and the inductance is reduced by 5.7% at 10 GHz. The results show good agreement between the model, full-wave simulations, and measurement data. The measurements are taken using a 40 GHz coaxial cables. The deviation and noise in the measurements at frequencies  $> 20$  GHz may be attributed to the cables. Figures 5.6a and 5.6b show the per unit length (p.u.l.) conductance and capacitance, respectively, of the transmission lines without and with metal fill. The metal fill increases the p.u.l. capacitance by 44%. The results show good agreement between the model, full-wave simulation, and measurement data. We expected the p.u.l. conductance to be negligible due to the low ( $\ll 0.01$ ) dielectric loss in the ILD. The p.u.l. conductance measurement results show negligible values up to

20 GHz and are noisy beyond 20 GHz. Figures 5.7a and 5.7b show the real and imaginary part of the characteristic impedance, respectively. These results also show a good agreement in results obtained with all the three methods. The real part of characteristic impedance is reduced due to metal fill by 19% at 10 GHz. The imaginary part of the impedance is negative as expected. The results show a significant deviations, however, the real part of characteristic impedance is critical for the design process.

### 5.3 Spiral Inductors

In this section, we verify the accuracy of our spiral inductor modeling method presented in Chapter 3. For this verification, we discuss the design and fabrication of the test structures, outline the parameters of interest, and show the comparison of model results with the measurement results up to 40 GHz.

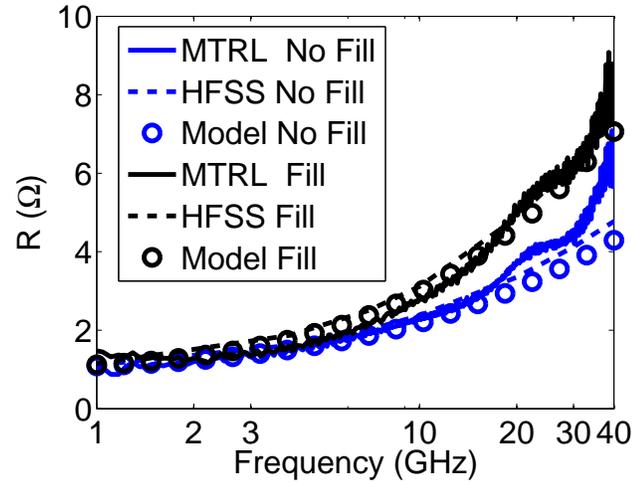
#### 5.3.1 Design and Fabrication of Test Structures

The test structure for the verification of our models is a rectangular spiral inductor used in 2.4 GHz RF circuits. We designed a 3.5 nH rectangular spiral inductor with a peak quality factor of 10 at 2.4 GHz. The spiral inductor has 4.5 turns with outer dimensions of  $200 \mu\text{m} \times 200 \mu\text{m}$ , width of  $12 \mu\text{m}$ , and inter-winding spacing of  $2.5 \mu\text{m}$ . Figure 5.8 shows the die photo of the test spiral inductor embedded in MTRL *through* calibration structure. The figure also shows the details of the lateral dimensions. To validate the proposed modeling method, we fabricated the same inductor in the presence of metal fill. Metal fills of size  $10 \mu\text{m} \times 10 \mu\text{m}$  and 60 % metal density are inserted on layers (M6 through M1) as shown in the die photo of Fig. 5.9. The buffer distance (edge to edge distance) between the inductor and the metal fill on M6 is  $> 20 \mu\text{m}$ .

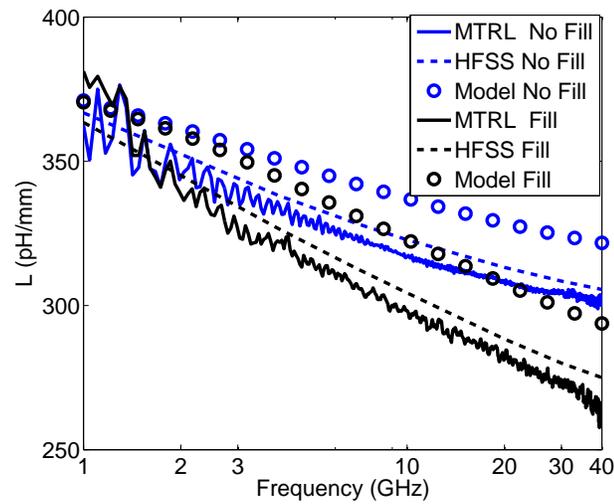
We extract the spiral inductor parameters from the Y-parameters which are converted from the measured two-port S-parameters. The quantities of interest are one-port inductance ( $L_{11}$ ), resistance ( $R_{11}$ ), and quality factor ( $Q_{11}$ ) calculated as:

$$L_{11} = \text{Im} \left( \frac{1/Y_{11}}{\omega} \right) \quad (5.3)$$

$$R_{11} = \text{Re} (1/Y_{11}) \quad (5.4)$$



(a) Resistance p.u.l.

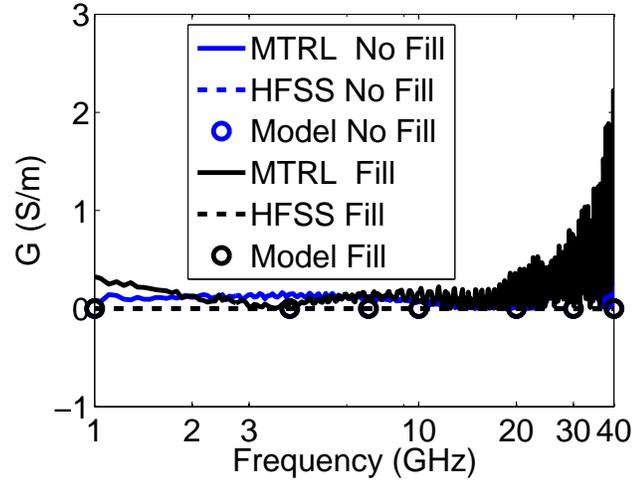


(b) Inductance p.u.l.

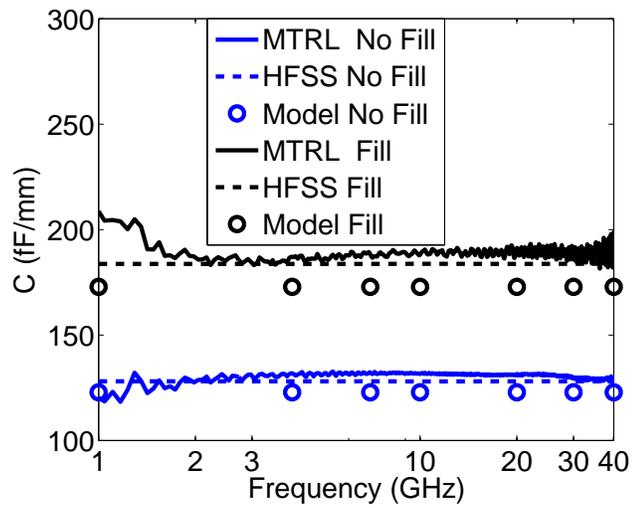
Figure 5.5: Transmission line p.u.l. parameters with and without metal fill

$$Q_{11} = -\frac{\text{Im}(Y_{11})}{\text{Re}(Y_{11})}. \quad (5.5)$$

Further, the port-1 shunt equivalent capacitance ( $C_{10}$ ) and conductance ( $G_{10}$ ) are cal-



(a) Conductance p.u.l.



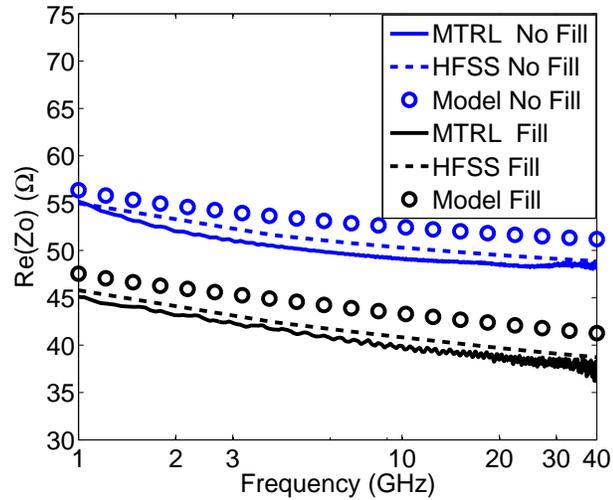
(b) Capacitance p.u.l.

Figure 5.6: Transmission line p.u.l. parameters with and without metal fill

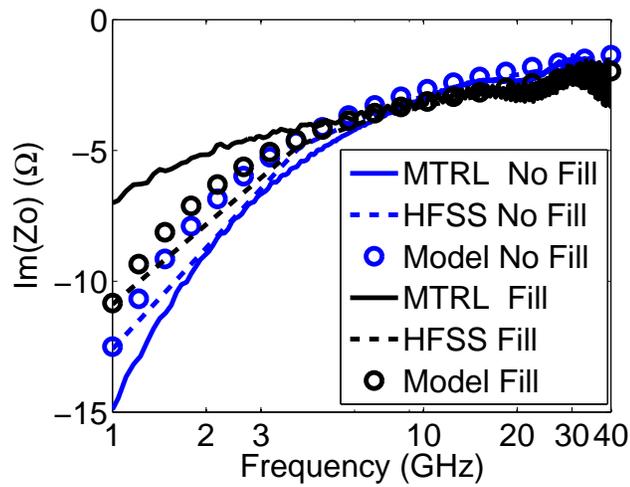
culated as

$$C_{10} = \text{Im} \left( \frac{Y_{11} + Y_{12}}{\omega} \right) \quad (5.6)$$

$$G_{10} = \text{Re} (Y_{11} + Y_{12}) . \quad (5.7)$$



(a) Real characteristic impedance



(b) Imaginary characteristic impedance

Figure 5.7: Transmission line characteristic impedance with and without metal fill.

### 5.3.2 One-tier Measurements

Figures 5.10a and 5.10b show a comparison between the measurement and model results for  $R_{11}$  and  $L_{11}$ . The model results agree with the measurement results up to 10 GHz and

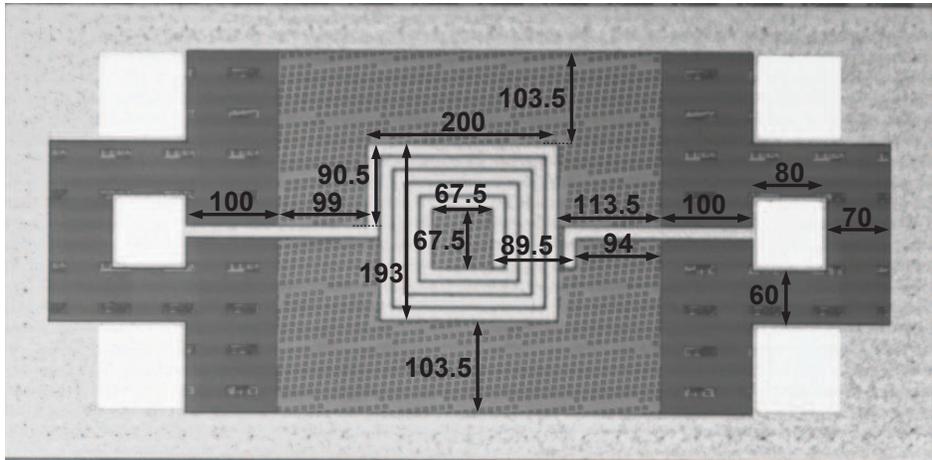


Figure 5.8: Die photo of spiral inductor without metal fill

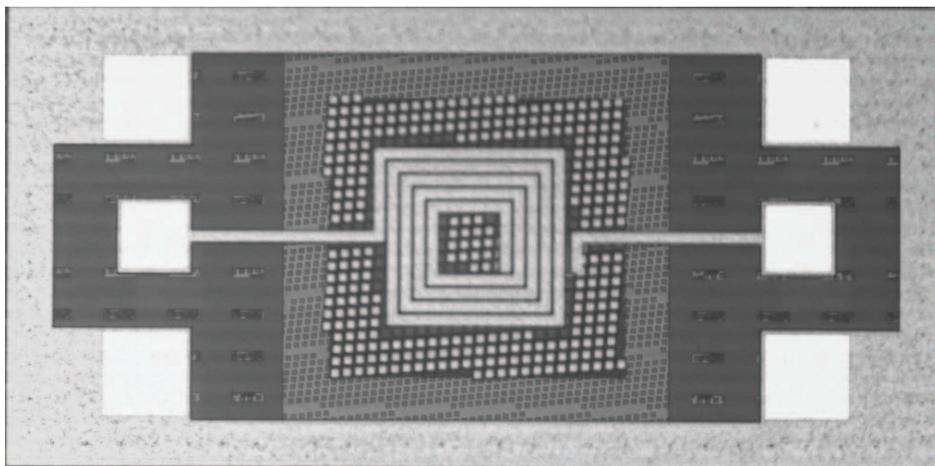
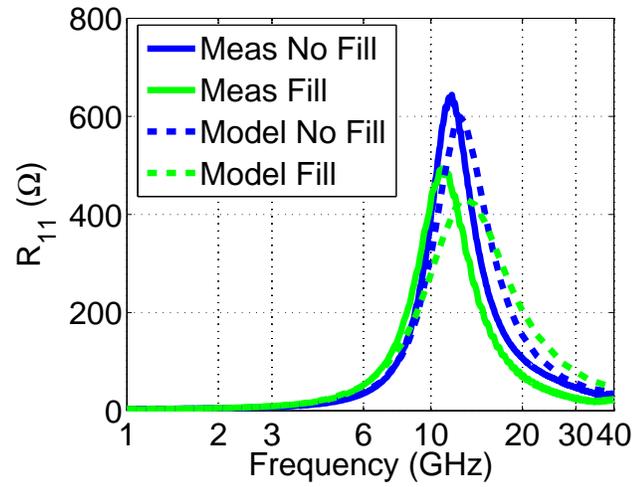
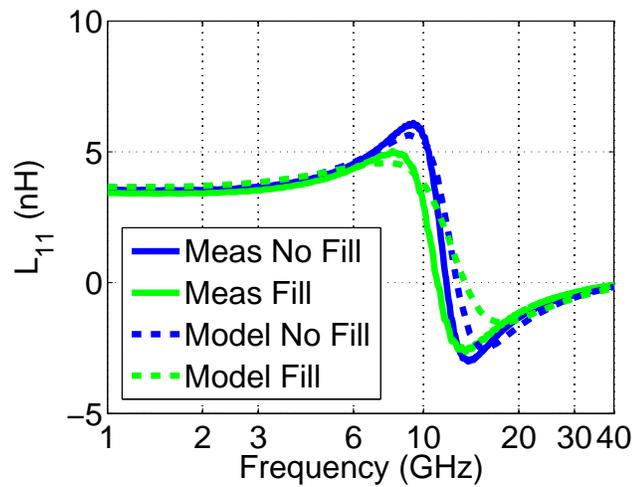


Figure 5.9: Die photo of spiral inductor with metal fill of size  $10 \mu\text{m} \times 10 \mu\text{m}$  and 50 % metal density.

show deviations beyond 10 GHz. These deviations can be attributed to the inaccuracies in the process material properties and variations in the technology dimensions. Similarly the port 1 shunt capacitance and conductance results shown in Figs. 5.11b and 5.11a are accurate up to 20 GHz and show deviations at frequencies larger than 20 GHz. Figure 5.12 shows a comparison of the port-1 quality factor model and measurement results.



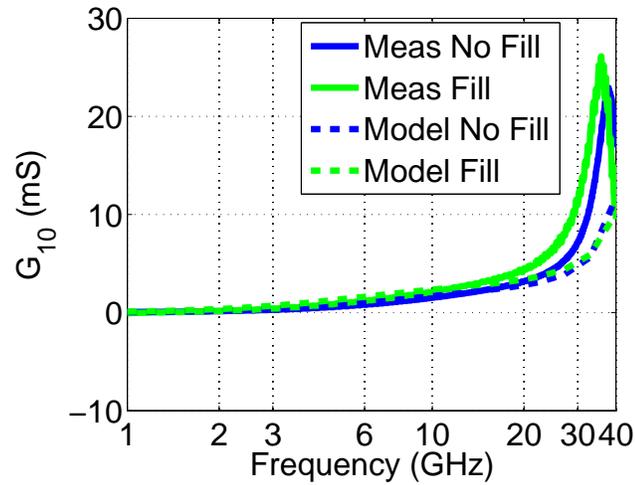
(a) Port 1 resistance



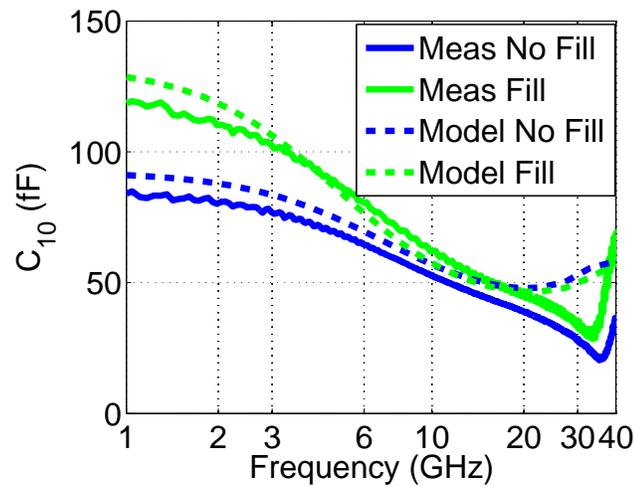
(b) Port 1 inductance

Figure 5.10: Spiral inductor one port equivalent parameters with and without metal fill; comparison with models

As can be seen from the figure, the results agree well up to 20 GHz and start to deviate above 20 GHz.



(a) Port 1 conductance



(b) Port 1 capacitance

Figure 5.11: Spiral inductor one port equivalent parameters with and without metal fill; comparison with models

## 5.4 Conclusion

In this chapter, we verified the performance of our modeling methods for the transmission line and rectangular spiral inductor. The models for transmission lines matched with

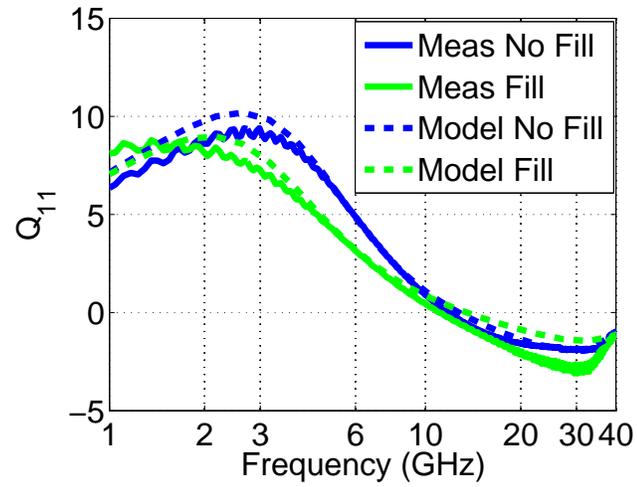


Figure 5.12: Spiral inductor quality factor with and without metal fill; comparison with models

the measurement results up to 40 GHz. The models for spiral inductors matched up to 10 GHz for port inductance and resistance, up to 20 GHz for port 1 capacitance, conductance, and the quality factor.

## Chapter 6: Summary and Future Work

### 6.1 Summary

In this thesis, we have presented fast and scalable modeling approaches for capturing parasitic effects of metal fill in on-chip interconnects and passive components. Further, we have demonstrated an accurate on-wafer measurement characterization approach along with statistical analysis for on-chip passive components.

We have demonstrated the degradation in the performance of interconnects and spiral inductors due to the insertion of metal fill through full-wave electromagnetic simulation results. Further we have shown the effect of such degradation on circuit performance, demonstrating the severity of the metal fill impact. We have given a quantitative treatment to an assumption that metal fill can be blocked in some regions of an IC and have shown that, in some scenarios, blocking metal fill can in fact lead to an increase in chip size.

With this motivation, we have presented a novel method for addressing the complex problem of parasitic capacitance of multi-conductor interconnects in the presence of metal fill. This proposed method significantly reduces the computational complexity through a set of dimensional reductions using analytical and empirical approximations. The verification of the hypotheses presented is achieved through comparison of capacitance calculated using our method and a commercial electromagnetic simulator. The results agree within 10% for all the verification over a wide range of physical and technology parameters. We have demonstrated the versatility of the approach through applications to floating metal fill in different interconnect structures such as an embedded microstrip and a coplanar waveguide, and different types of metal fill, such as a rectangular metal fill.

Further we have presented models for the capacitance of and eddy-current loss in spiral inductors in the presence of metal fill. We have demonstrated methods to calculate the partial circuit elements that represent metal fill parasitic effects. Using a commercial full-wave electromagnetic simulator, we have validated the presented methods. The

results agreed to within 6% up to 50 GHz for a rectangular spiral inductor.

We have designed multi-line TRL calibration standards for accurate characterization of on-chip passive components. In addition, we have utilized covariance-matrix-based methods for statistical treatment of the uncertainty in the measurement results. We have demonstrated the accuracy of the systematic measurement based characterization approach through comparison with full-wave simulation results.

We have utilized the measurement based characterization approach to verify the presented modeling methods. We have presented measurement results for a representative transmission line and spiral inductor in the presence of metal fill and demonstrated good agreement between the model results and the measurement results.

## 6.2 Future Work

This thesis has addressed the large problem of modeling of metal fill parasitics in complex structures. The future direction of this research topic includes the extension of the presented techniques to other passive components such as transformers, coupler, and filters. The techniques for spiral inductors may scale directly to these types of geometries. With the availability of fast and scalable models to capture metal fill parasitics, traditional optimization algorithms can be utilized for design optimization of circuit blocks in the presence of metal fill.

Apart from these broad future research topics, a few specific improvements can also be achieved. The capacitance modeling method presented in this thesis could be extended to a more general metal fill layout. The computational efficiency of the problem could be further enhanced through the development of a set of closed-form expressions for the reduced problem or by developing a fast custom 2D capacitance simulator with an efficient implementation of the floating condition for metal fill.

The calculation of the shunt admittance of spiral inductor coupled segments is based on a simple C-GC model. The accuracy of these approximations, especially at millimeter-wave and higher frequencies, is questionable. Future research may focus on the development of a set of closed-form expressions through a rigorous analysis of propagating modes in the metal-insulator-substrate (MIS) structure. Also, the accuracy of this model could be further enhanced by considering the inductance in the shunt branch.

The computational burden of the proposed method for spiral inductors still lies with

the partial inductance matrix computations without metal fill. With metal fill, only a non-significant amount of time and memory requirements are added. The problem of passive components without metal fill could be efficiently solved using an intelligent non-uniform meshing and approximate estimation of partial inductance calculations.

For the measurement characterization using on-chip calibration standards in the presence of metal fill, the effect of metal fill needs to be evaluated at millimeter frequencies and beyond. The periodic structure formed by metal fill may exhibit significant attenuation and excite a number of non-evanescent higher order modes affecting the accuracy of the on-chip calibrations. This phenomenon due to the periodic metal fill may violate the assumptions of single dominant mode propagation used in the calibration algorithms and in the procedure for determination of the characterization impedances from the propagation constant. These effects will have significant ramifications on the way we perform VNA measurements.

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## APPENDICES

## Appendix A: Bloch Wave Considerations for Floating Metal Filled TRL Calibration Standards

In this appendix, we give a Bloch wave considerations to the metal fill periodic structure problem as suggested by Williams [101].

### A.1 Background

TRL (through-reflect-line) is a widely used VNA calibration algorithm. It relies on an accurate measurement of propagation constant ( $\gamma$ ) of calibration transmission line structures using an uncalibrated VNA measurements [84]. This accurate measurement of the propagation constant is used to calculate the characteristics impedance ( $Z_0$ ) [83] of the calibration standards. This frequency dependent characteristics impedance is used for the renormalization of the corrected VNA measurements to the port reference impedance.

In the case of on-chip measurements using TRL algorithm, the calibration standards need to be realized on the same chip as that of the device under test (DUT). Realization of on-chip transmission line standards poses several challenges including:

- The longest length achievable on-chip is limited by the size of the chip and the DFM (design for manufacturability) rules. This sets the low frequency bound on the TRL calibration accuracy.
- On-chip transmission lines are fairly lossy due to the alloys used in the fabrication. Therefore, the electrical properties, such as the characteristics impedance and propagation constant are highly frequency dependent. This stresses the capability of calibration algorithm to accurately capture these frequency dependent behaviors.
- The losses in these transmission lines further increase due to frequency dependent eddy-currents and displacement currents when fabricated on the semi-conducting

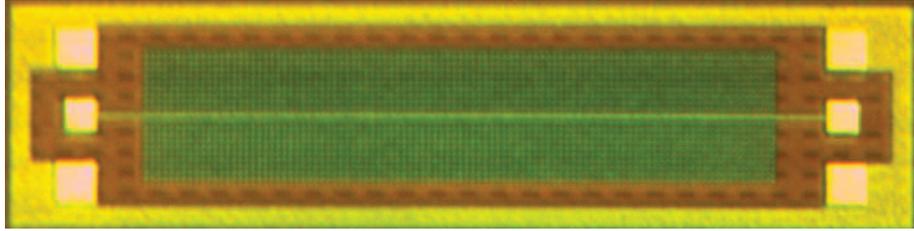


Figure A.1: A die photo of transmission lines on a  $0.18 \mu\text{m}$  BiCMOS test chip.

substrate. Therefore the signal conductor are typically shielded from the semi-conducting substrate by laying a solid ground plane underneath it.

- Laying out a solid ground plane in advanced integrated circuit (IC) manufacturing processes poses challenges in terms of stress and metal density requirements. Therefore often the ground planes need to be periodically slotted to release the stress and reduce the metal density. This invalidates the single propagating mode assumption of the transmission line structure.
- Every metal layer on the IC needs to meet a certain minimum metal density to reduce planarization and polishing related defects. This leads to the addition of floating non-functional metal fill structures on metal layers. Typically layout routing underneath the signal conductors of the calibration structures is avoided to realize a uniform single mode transmission line. However, with the addition of metal fill, the transmission line structures are no longer physically uniform.

In this Appendix, we attempt to address the last bullet point in the aforementioned list of challenges.

## A.2 Problem Statement

Figure A.1 shows a typical on-chip transmission line with metal fill added. This transmission line is designed in a  $0.18 \mu\text{m}$  BiCMOS process. The designed characteristics impedance is  $50 \Omega$  at about 10 GHz and the length is  $1.433 \mu\text{m}$ . In this particular case,  $10 \mu\text{m} \times 10 \mu\text{m}$  size metal fill with 50% density is added on all the layers. These metal fills are periodically added to meet the metal density requirements. When such floating

structures are added in the calibration standards, the physical uniformity is disturbed and therefore the assumptions in the TRL calibration algorithm need to be carefully re-evaluated. At some point in frequency, these structures may need to be treated as a periodic structures.

Therefore we wish to address the following questions:

1. Do we need to consider periodicity condition? Why can't we just lump additional capacitance and resistance/inductance due to metal fill into p.u.l. line parameters?
2. In the presence of metal fill, is the assumption of constant capacitance and negligible  $G/\omega C$  still valid?
3. Can we represent the energy stored in the higher order modes as reactive circuit elements?
4. Are there higher order mode interactions between unit cells of the periodic structure?

### A.3 Periodic vs. Uniform Assumption

In this section we address the first question. For this discussion, consider a unit cell of lossless transmission line. Figure A.2 shows a section called as a unit cell (of length  $W_{uc}$ ) of non-uniform transmission line as a cascade of: a uniform transmission line section of length  $W_{uc}/2$ , a capacitance  $C_{mf}$  to represent energy stored in the higher order modes excited due to metal fill discontinuity, and a uniform transmission line section of length  $W_{uc}/2$ .  $V_n$  and  $I_n$  represent the total<sup>1</sup> voltage and current amplitudes at the input of this  $n^{th}$  unit cell, respectively.  $V_{n+1}$  and  $I_{n+1}$  represent the total voltage and current amplitudes at the input of next  $(n+1)^{st}$  unit cell, respectively. These two voltage and currents are related as [82]

$$\begin{aligned} \begin{bmatrix} V_n \\ I_n \end{bmatrix} &= \begin{bmatrix} \cos\left(\frac{\theta}{2}\right) & jZ_0 \sin\left(\frac{\theta}{2}\right) \\ jY_0 \sin\left(\frac{\theta}{2}\right) & \cos\left(\frac{\theta}{2}\right) \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C_{mf} & 1 \end{bmatrix} \\ &\times \begin{bmatrix} \cos\left(\frac{\theta}{2}\right) & jZ_0 \sin\left(\frac{\theta}{2}\right) \\ jY_0 \sin\left(\frac{\theta}{2}\right) & \cos\left(\frac{\theta}{2}\right) \end{bmatrix} \begin{bmatrix} V_{n+1} \\ I_{n+1} \end{bmatrix} \end{aligned} \quad (\text{A.1})$$

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<sup>1</sup>sum of contributions from the TEM incident and reflected components

where  $\theta = \beta W_{uc}/2$ . The input/output total voltage/currents can be related through the ABCD parameters and the propagation constant as

$$\begin{bmatrix} V_n \\ I_n \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_{n+1} \\ I_{n+1} \end{bmatrix} = e^{\gamma_p W_{uc}} \begin{bmatrix} V_{n+1} \\ I_{n+1} \end{bmatrix} \quad (\text{A.2})$$

and it can be rearranged so that

$$\begin{bmatrix} A - e^{\gamma_p W_{uc}} & B \\ C & D - e^{\gamma_p W_{uc}} \end{bmatrix} \begin{bmatrix} V_{n+1} \\ I_{n+1} \end{bmatrix} = [0 \quad 0]^T. \quad (\text{A.3})$$

For this eigenvalue problem, non-trivial solution exists only if the determinant is zero. Therefore,

$$\begin{vmatrix} A - e^{\gamma_p W_{uc}} & B \\ C & D - e^{\gamma_p W_{uc}} \end{vmatrix} = AD - BC - e^{\gamma_p W_{uc}} (A + D) + e^{2\gamma_p W_{uc}} = 0 \quad (\text{A.4})$$

If the unit cell is assumed to be symmetric, i.e. all the metal fills aligned with same size and density on all the metal layers,  $A = D$ . From the reciprocity of the network, we have  $AD - BC = 1$ , therefore

$$1 - e^{\gamma_p W_{uc}} (2A) + e^{2\gamma_p W_{uc}} = e^{\gamma_p W_{uc}} (e^{-\gamma_p W_{uc}} + 2A + e^{\gamma_p W_{uc}}) = 0. \quad (\text{A.5})$$

For the term  $e^{\gamma_p W_{uc}}$  to be zero, either  $\gamma_p$  or  $W_{uc}$  should be  $-\infty$ , and therefore,

$$e^{-\gamma_p W_{uc}} + e^{\gamma_p W_{uc}} = 2 \cosh(\gamma_p W_{uc}) = -2A \quad (\text{A.6})$$

$$\gamma_p = \frac{\cosh^{-1}(A)}{W_{uc}} \quad (\text{A.7})$$

Next, to solve for the characteristics impedance, we use the eigenvalue equation as

$$(A - e^{\gamma_p W_{uc}}) V_{n+1} = -B I_{n+1} \quad (\text{A.8})$$

$$Z_{0,p} = \frac{V_{n+1}}{I_{n+1}} = \frac{-B}{A - e^{\gamma_p W_{uc}}} \quad (\text{A.9})$$

From the eigenvalue equation, the value of  $e^{\gamma_p W_{uc}}$  can also be written as

$$e^{\gamma_p W_{uc}} = \frac{(A + D) \pm \sqrt{(A + D)^2 - 4}}{2} \quad (\text{A.10})$$

which can be substituted in the equation for  $Z_{0,p}$  as

$$Z_{0,p} = \frac{-2B}{2A - (A + D) \pm \sqrt{(A + D)^2 - 4}} \quad (\text{A.11})$$

$$= \frac{-2B}{\pm \sqrt{A^2 - 1}} \quad \text{since } A = D \quad (\text{A.12})$$

$$= \pm \sqrt{\frac{B}{C}} \quad \text{since } AD - BC = 1 \rightarrow A^2 - 1 = BC \quad (\text{A.13})$$

Finally, the ABCD parameters from (A.1) can be used to calculate  $Z_{0,p}$  and  $\gamma_p$ .

Now, we need to evaluate if the periodic structure consideration can be ignored and up to what frequency the assumption of lumped metal fill capacitance is valid. We calculate the characteristics impedance and propagation constant for the lumped scenario as

$$Z_{0,L} = \sqrt{\frac{L'}{C' + C'_{mf}}} \quad (\text{A.14})$$

$$\beta_L = \sqrt{L' (C' + C'_{mf})} \quad (\text{A.15})$$

where  $L'$  and  $C'$  are per unit length (p.u.l.) inductance and capacitance of uniform transmission lines without metal fill, respectively.  $C'_{mf}$  is the additional pul capacitance which represents higher order modes ( $C'_{mf} = C_{mf}/W_{uc}$ ) due to metal fill.

Figure A.3 and A.4 show the comparison between the two approaches for  $L' = 250 \text{ nH/m}$  and  $C' = 100 \text{ pF/m}$  resulting in  $50 \Omega$  and  $2 \times 10^8 \text{ m/s}$  line and  $C'_{mf} = 20 \text{ pF/m}$ . It can be seen that the characteristics impedance and phase constant can be determined from the lumped assumption and the line is electrically smooth up to a certain frequency. The values start to deviate beyond that frequency, however, the deviation is insignificant for the case shown. The main reason for this is the unit cell size is considerably smaller compared to the wavelength.

To study this effect further, we plot the error in  $Z_0$  (defined as  $\frac{Z_{0,p} - Z_{0,L}}{Z_{0,p}} \times 100$ ) as a function of frequency in Fig. A.5. In the same plot we show unit cell normalized

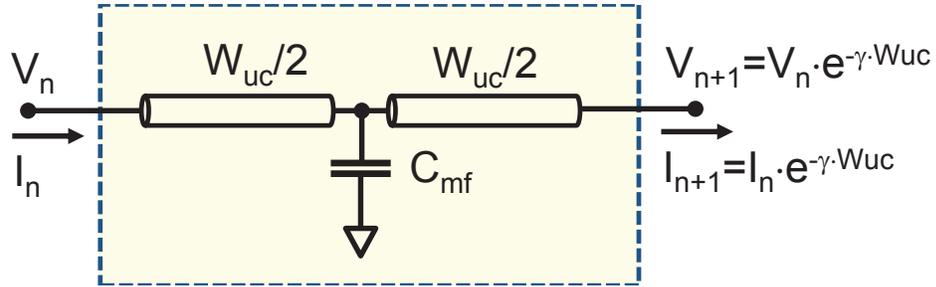


Figure A.2: A uniform transmission line periodically loaded with a capacitance  $C_{mf}$ .

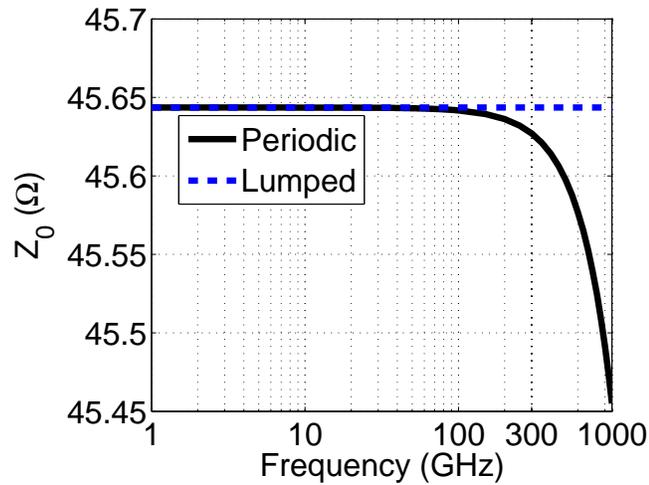


Figure A.3: Comparison between periodic and lumped assumption: characteristic impedance

to the wavelength as  $W_{uc}/\lambda$  ( $\lambda = 2\pi/\beta$ ). As can be seen from the figure, for the case of  $0.66 \times 10^8$  m/s line, the 1% error is at about 500 GHz and  $W_{uc}/\lambda$  is 0.1233. At 500 GHz, the faster line ( $2 \times 10^8$  m/s)  $Z_0$  error is 0.1% and the corresponding  $W_{uc}/\lambda$  is 0.0418. Thus the error is wavelength dependent and periodicity considerations are required beyond the frequency corresponding to about 0.1233 normalized unit cell.

#### A.4 Assumptions on $G'$ and $C'$

In this section we will address the second question mentioned in the problem statement. The method for determination of characteristics impedance relies on accurate measure-

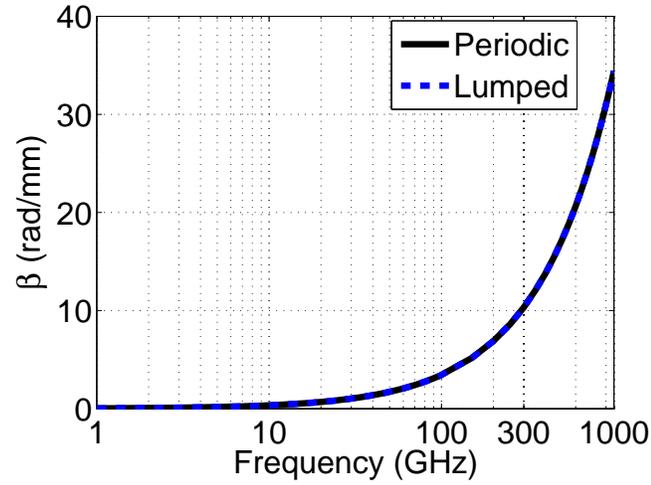


Figure A.4: Comparison between periodic and lumped assumption: phase constant

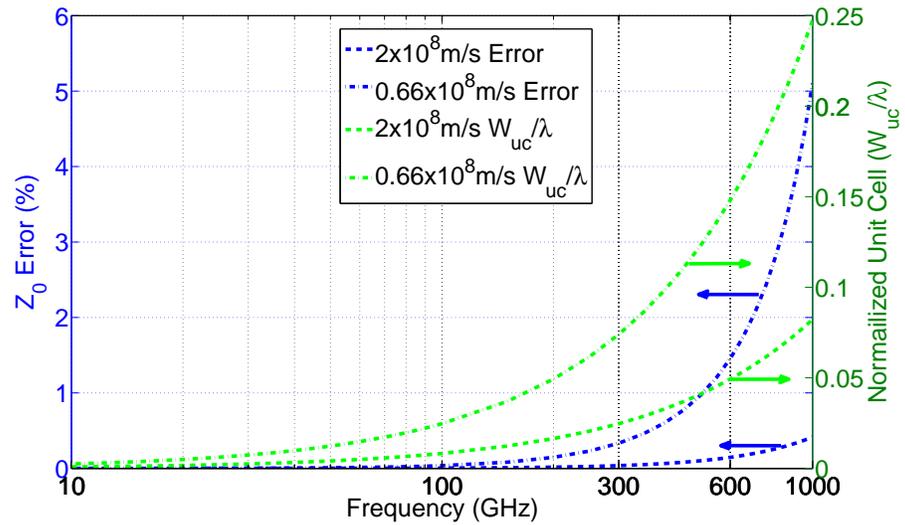


Figure A.5: Error in characteristics impedance and unit cell normalized to wavelength.

ment of the propagation constant without VNA calibration [87]. Further, to calculate

the characteristics impedance, following is used [83]

$$\frac{\gamma}{Z_0} = G' + j\omega C'. \quad (\text{A.16})$$

Assuming a low dielectric loss ( $G' \ll \omega C'$ ) and if the capacitance of transmission line can be measured [85] or simulated,  $Z_0$  can be determined. Here we evaluate the assumption of capacitance calculations and negligible  $G'$  through measurements using multi-line TRL calibration.

A test chip with transmission lines including metal fill was fabricated in a 0.18  $\mu\text{m}$  process. The two-port scattering ( $S$ ) parameters are obtained after the calibration and converted to transmission line parameters assuming an electrically uniform line, i.e. the ABCD parameters of this line given by

$$\begin{bmatrix} \cosh(\gamma L) & Z_0 \sinh(\gamma L) \\ Y_0 \sinh(\gamma L) & \cosh(\gamma L) \end{bmatrix} \quad (\text{A.17})$$

and therefore  $Z_0$  and  $\gamma$  calculated as

$$Z_0 = \sqrt{\frac{B}{C}} = Z_p \sqrt{\frac{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}}} \quad (\text{A.18})$$

$$\gamma = \frac{\cosh^{-1}(A)}{L} = \frac{1}{L} \cosh^{-1} \left( \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{2S_{21}} \right). \quad (\text{A.19})$$

Further, the p.u.l. parameters are calculated as

$$R' = \text{Re}(Z_0\gamma) \quad (\text{A.20})$$

$$L' = \text{Im} \left( \frac{Z_0\gamma}{\omega} \right) \quad (\text{A.21})$$

$$G' = \text{Re} \left( \frac{\gamma}{Z_0} \right) \quad (\text{A.22})$$

$$C' = \text{Im} \left( \frac{\gamma}{\omega Z_0} \right) \quad (\text{A.23})$$

The same transmission line structure was simulated in a full-wave electromagnetic simulator [11] and the p.u.l. parameters were obtained.

Figure A.6 shows the p.u.l. capacitance as a function of frequency for both, the

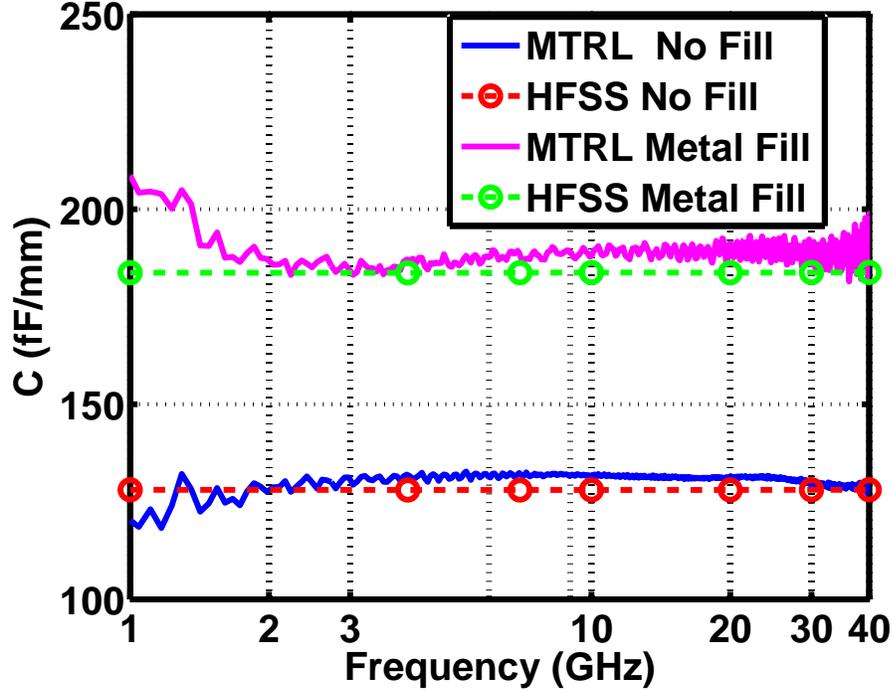


Figure A.6: Capacitance as a function of frequency for lines without and with metal fill.

line without metal fill and with metal fill. It can be seen from the figure that the capacitance is fairly constant from the simulation results as well as measurement results. The low frequency deviations may be attributed to the bandwidth limitation of the TRL algorithm. Figure A.7 shows the validation of the assumption that  $G'/\omega C'$  can be ignored. For the frequency range of 3-40 GHz,  $G'/\omega C' < 0.06$  which is  $\ll 1$  up to 40 GHz. Further, high frequency characterization is needed to validate this assumption above 40 GHz.

## A.5 Higher Order Mode Circuit Element Approximation

In the previous section, the energy stored in the fringing electric field due to metal fill discontinuity was represented by a shunt capacitance,  $C_{mf}$ . To accurately represent the discontinuity, the local field needs to be described in terms of the superposition of the

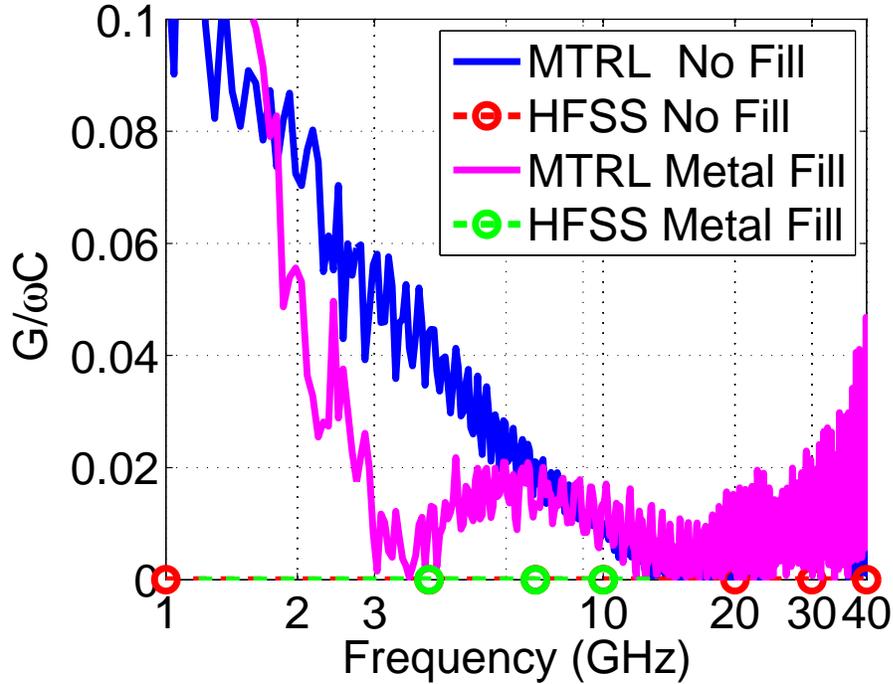


Figure A.7:  $G'/\omega C'$  as a function of frequency for lines without and with metal fill.

dominant propagating mode and an infinite number of higher order modes.

This assumption can be evaluated through a commercial full-wave solver [11] using the periodic boundary condition.

## A.6 Higher Order Mode Interactions

In the previous sections, the interactions of the higher order modes between adjacent unit cell are ignored. This approximation is based on the assumptions that only the dominant mode propagates, all the higher order modes decay before reaching the unit cell boundary and have insignificant energy. However, for high metal fill density, the separation between metal fills is reduced, and the higher order modes may not have a negligible value at the boundary between the unit cell. This modifies the propagation constant of the periodic structure. Figure A.8 shows the top view of the unit cell structure with these interactions

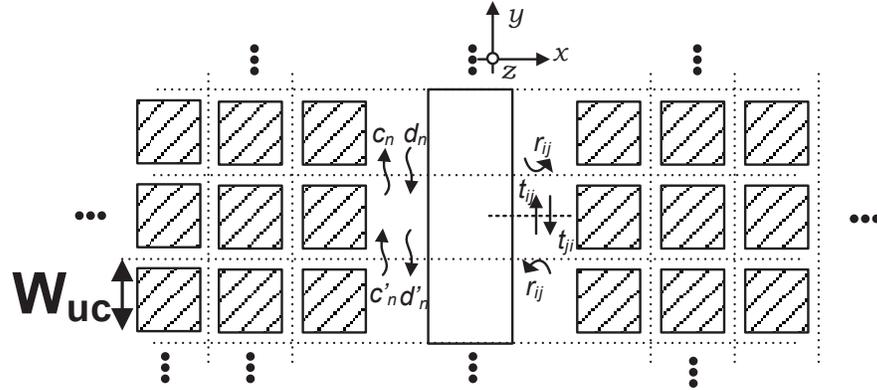


Figure A.8: All modes consideration for the periodic structure (based on [102]).

[102]. Here mode amplitudes  $c_n, c'_n$  represent forward-propagating  $n^{\text{th}}$  mode and  $d_n, d'_n$  represent backward-propagating  $n^{\text{th}}$  mode.  $r_{ij}$  and  $t_{ij}$  are the reflection and transmission coefficients for the  $i^{\text{th}}$  mode with  $j^{\text{th}}$  mode incident, respectively. To represent the problem in an equivalent circuit form, we need to utilize a multi-mode equivalent circuit that represents each of the mode as discussed in [103].

## Appendix B: Magnetic Field due to Finite Length Filament

In this appendix we derive an expression for a magnetic field due to a finite length current carrying filament. We consider a two-dimensional problem due to rotational symmetry of the fields. Consider a scenario in Fig. B.1 for this derivation. Let us consider a differential current segment of  $dx'$  given by  $\vec{r}' = x'\hat{x}$  as shown in the figure. This current source vector is given by  $I d\vec{r}' = (Idx')\hat{x}$ . The observation point  $P$  is given by  $\vec{r}_p = x\hat{x} + y\hat{y}$  and the vector from the source to the observation point is given as  $\vec{r} = \vec{r}_p - \vec{r}' = (x - x')\hat{x} + y\hat{y}$ . Using Biot-Savart law, the field due to this infinitesimal current source  $(Idx')\hat{x}$  is

$$d\vec{H}(\vec{r}) = \frac{I d\vec{r}' \times \hat{r}}{4\pi r^2} = \frac{(Idx')\hat{x} \times \vec{r}}{4\pi r^3} = \frac{I d\vec{r}' \times \hat{r}}{4\pi r^2} = \frac{I y dx' \hat{z}}{4\pi ((x - x')^2 + y^2)^{3/2}} \quad (\text{B.1})$$

as the unit vector  $\hat{r}$  is given as

$$\hat{r} = \frac{\vec{r}}{r} = \frac{(x - x')\hat{x} + y\hat{y}}{\sqrt{(x - x')^2 + y^2}} \quad (\text{B.2})$$

and the cross product is

$$d\vec{r}' \times \vec{r} = (dx')\hat{x} \times ((x - x')\hat{x} + y\hat{y}) = y dx' \hat{z}. \quad (\text{B.3})$$

The magnetic field due to the finite length segment from  $P_1$  to  $P_2$  is given as the contributions of each of the infinitesimal current segments as

$$\vec{H}(\vec{r}) = \int_{-L/2}^{L/2} \frac{I y dx' \hat{z}}{4\pi ((x - x')^2 + y^2)^{3/2}} = - \frac{I(x - x')\hat{z}}{4\pi y ((x - x')^2 + y^2)^{1/2}} \Big|_{-L/2}^{L/2} \quad (\text{B.4})$$

$$= \frac{I}{4\pi y} \left( \frac{(x + L/2)}{((x + L/2)^2 + y^2)^{1/2}} - \frac{(x - L/2)}{((x - L/2)^2 + y^2)^{1/2}} \right) \hat{z} \quad (\text{B.5})$$

$$= \frac{I}{4\pi y} (\sin(\theta_2) - \sin(\theta_1)) \hat{z} \quad (\text{B.6})$$

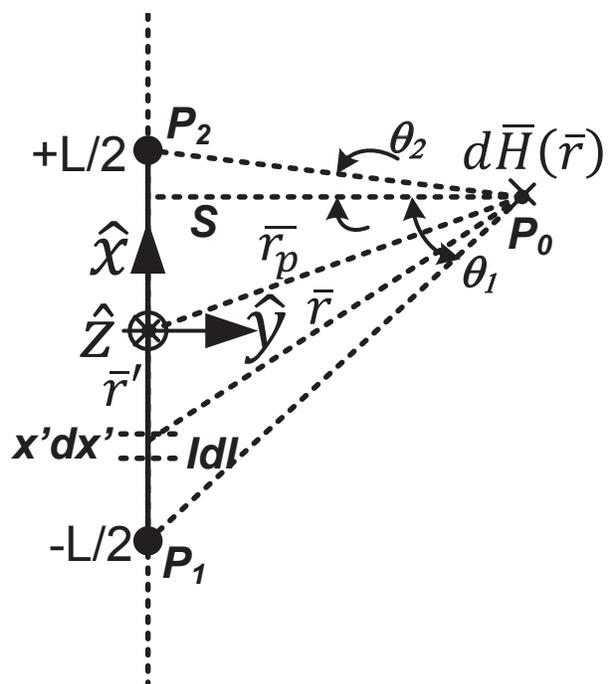


Figure B.1: Formulation for  $\bar{H}(\bar{r})$  field calculations for a finite current filament.

## Appendix C: Electric Field due to Finite Length Charge

In this appendix we derive an expression for a electric field due to a finite length charge carrying filament. We consider a two-dimensional problem due to rotational symmetry of the fields. Consider a scenario in Fig. C.1 for this derivation. Let us consider a differential charge segment of  $dx'$  given by  $\vec{r}' = x'\hat{x}$  as shown in the figure. This current source vector is given by  $\rho_l d\vec{r}' = (\rho_l dx')\hat{x}$ . The observation point  $P$  is given by  $\vec{r}_p = x\hat{x} + y\hat{y}$  and the vector from the source to the observation point is given as  $\vec{r} = \vec{r}_p - \vec{r}' = (x - x')\hat{x} + y\hat{y}$ . Using Coulomb's law, the field due to this infinitesimal charge source  $(I dx')\hat{x}$  is

$$d\vec{E}(\vec{r}) = \frac{dq\hat{r}}{4\pi\epsilon_0 r'^2} = \frac{\rho_l dx'\vec{r}}{4\pi\epsilon_0 r'^3} = \frac{\rho_l dx'[(x - x')\hat{x} + y\hat{y}]}{4\pi\epsilon_0 ((x - x')^2 + y^2)^{3/2}} \quad (\text{C.1})$$

as the unit vector  $\hat{r}$  is given as

$$\hat{r} = \frac{\vec{r}}{r} = \frac{(x - x')\hat{x} + y\hat{y}}{\sqrt{(x - x')^2 + y^2}}. \quad (\text{C.2})$$

The electric field due to the finite length segment from  $P_1$  to  $P_2$  is given as the contributions of each of the infinitesimal charge segments as

$$\vec{E}(\vec{r}) = \int_{-L/2}^{L/2} \frac{\rho_l dx' [(x - x')\hat{x} + y\hat{y}]}{4\pi\epsilon_0 ((x - x')^2 + y^2)^{3/2}} \quad (\text{C.3})$$

$$= \frac{\rho_l}{4\pi\epsilon_0} \left[ \frac{1}{((x - x')^2 + y^2)^{1/2}} \hat{x} + \frac{x' - x}{y ((x - x')^2 + y^2)^{1/2}} \hat{y} \right]_{-L/2}^{L/2} \quad (\text{C.4})$$

$$= \frac{\rho_l}{4\pi\epsilon_0} \left( \frac{y}{((x - L/2)^2 + y^2)^{1/2}} - \frac{y}{((x + L/2)^2 + y^2)^{1/2}} \right) \hat{x} + \quad (\text{C.5})$$

$$\frac{\rho_l}{4\pi\epsilon_0} \left( -\frac{x - L/2}{((x - L/2)^2 + y^2)^{1/2}} + \frac{x + L/2}{((x + L/2)^2 + y^2)^{1/2}} \right) \hat{y} \quad (\text{C.6})$$

$$= \frac{\rho_l}{4\pi\epsilon_0} (\cos(\theta_1) - \cos(\theta_2)) \hat{x} + \frac{\rho_l}{4\pi\epsilon_0} (\sin(\theta_2) - \sin(\theta_1)) \hat{y} \quad (\text{C.7})$$

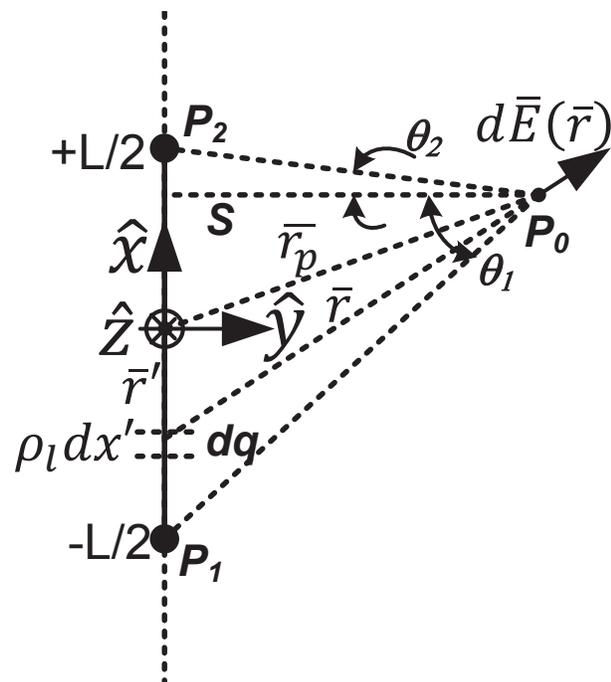


Figure C.1: Formulation for  $\vec{E}(\vec{r})$  field calculations for a finite line charge filament.

## Appendix D: Confidence Interval Derivation

To calculate the uncertainty in the measurement, if a certain probability distribution function (pdf) of measurand is known or assumed, a confidence interval (CI) is defined to quantify the errors. The estimated sample mean and variance value from  $N$  repeated measurements ( $X_1, X_2, \dots, X_N$ ) treated as a discrete random variables are given by

$$\bar{X} = \frac{1}{N} \sum_{i=1}^N X_i \quad (\text{D.1})$$

$$\sigma^2 = \frac{1}{N} \sum_{i=1}^N (X_i - \bar{X})^2. \quad (\text{D.2})$$

The confidence interval gives an estimated value of the parameter with a certain confidence, e.g. often 95 % or 99 %. For a normal probability distribution function (pdf) with an estimated mean,  $\bar{X}$ , and standard deviation,  $\sigma$ , the CI is equal to  $100(1-\alpha)$  % of the estimated mean value, where  $\alpha$  is a small number ( $0 < \alpha < 1$ ) [69]. This CI is calculated from the condition that

$$P(g_1(\mu) < \bar{X} < g_2(\mu)) = 1 - \alpha \quad (\text{D.3})$$

so that

$$\int_{-\infty}^{g_1(\mu)} f(x; \mu) d\bar{x} = \alpha/2 \quad (\text{D.4})$$

$$\int_{g_2(\mu)}^{\infty} f(x; \mu) d\bar{x} = \alpha/2. \quad (\text{D.5})$$

Here  $f(x; \mu)$  is the pdf of the sampling distribution of  $\bar{X}$  and  $g_1$  and  $g_2$  are functions of  $\mu$ . If the random variable is assumed to have a normal pdf, that is,  $\bar{X} \sim N(\mu, \sigma)$ , then the pdf of  $x$  is given as,

$$f(x; \mu, \sigma) = \frac{1}{\sigma\sqrt{2\pi}} \exp \left[ -\frac{1}{2} \left( \frac{x - \mu}{\sigma} \right)^2 \right]. \quad (\text{D.6})$$

The probability that the random variable lies between  $g_1(\mu)$  and  $g_2(\mu)$  can be calculated as

$$P(g_1(\mu) < \bar{X} < g_2(\mu)) = \frac{1}{\sigma\sqrt{2\pi}} \int_{g_1(\mu)}^{g_2(\mu)} \exp\left[-\frac{1}{2}\left(\frac{x-\mu}{\sigma}\right)^2\right] dx. \quad (\text{D.7})$$

If the two bounds are written in the form of  $\sigma$  so that

$$g_1(\mu) = \mu - n\sigma \quad (\text{D.8})$$

$$g_2(\mu) = \mu + n\sigma \quad (\text{D.9})$$

then the probability can be rewritten as

$$P(\mu - n\sigma < \bar{X} < \mu + n\sigma) = \frac{1}{\sigma\sqrt{2\pi}} \int_{\mu-n\sigma}^{\mu+n\sigma} \exp\left[-\frac{1}{2}\left(\frac{x-\mu}{\sigma}\right)^2\right] dx \quad (\text{D.10})$$

$$= \frac{2}{\sigma\sqrt{2\pi}} \int_{\mu}^{\mu+n\sigma} \exp\left[-\frac{1}{2}\left(\frac{x-\mu}{\sigma}\right)^2\right] dx. \quad (\text{D.11})$$

Using change of variables,  $u = \frac{x-\mu}{\sqrt{2}\sigma}$ ,  $du = dx/\sqrt{2}\sigma$ ,

$$P(\mu - n\sigma < \bar{X} < \mu + n\sigma) = \frac{2}{\sigma\sqrt{2\pi}} \sqrt{2}\sigma \int_0^{n/\sqrt{2}} \exp(-u^2) du \quad (\text{D.12})$$

$$= \frac{2}{\sqrt{\pi}} \frac{1}{2} \sqrt{\pi} [\text{erf}(u)]_0^{n/\sqrt{2}} \quad (\text{D.13})$$

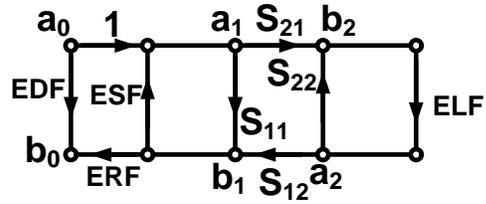
$$= \text{erf}\left(n/\sqrt{2}\right). \quad (\text{D.14})$$

The value of  $n$  can be evaluated using the complementary error function as

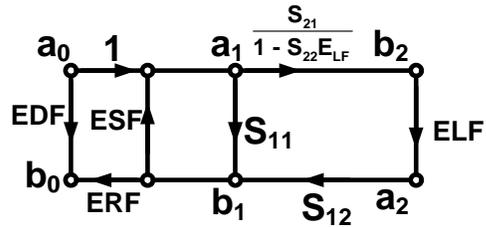
$$n = \sqrt{2} \text{erf}^{-1}(1 - \alpha). \quad (\text{D.15})$$

## Appendix E: Signal Flow Graph

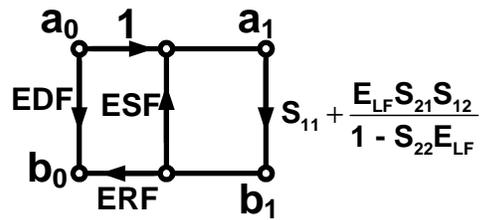
This appendix provides a derivation for  $S_{11m}$  and  $S_{21m}$  used for the error term derivation of a *twelve-term* error model. We use the signal flow graph decomposition principles [102] for deriving the expressions. Figure E.1 shows the step-by-step derivation of the  $S_{11m}$  and Fig. E.2 shows the step-by-step derivation of the  $S_{21m}$ .



(a) Step 1



(b) Step 2



(c) Step 3

$$\frac{1}{1 - E_{SF} \left( S_{11} + \frac{E_{LF} S_{21} S_{12}}{1 - S_{22} E_{LF}} \right)}$$

$$= \frac{1}{1 - S_{22} E_{LF} - E_{SF} (S_{11} (1 - S_{22} E_{LF}) + E_{LF} S_{21} S_{12})}$$

$$= \frac{S_{11} (1 - S_{22} E_{LF}) + E_{LF} S_{21} S_{12}}{1 - S_{22} E_{LF}}$$

(d) Step 4

$$E_{DF} \frac{S_{11} (1 - S_{22} E_{LF}) + E_{LF} S_{21} S_{12}}{1 - S_{22} E_{LF} - E_{SF} (S_{11} (1 - S_{22} E_{LF}) + E_{LF} S_{21} S_{12})}$$

(e) Step 5

Figure E.1: Step by step signal flow graph reduction for  $S_{11m}$  derivation.

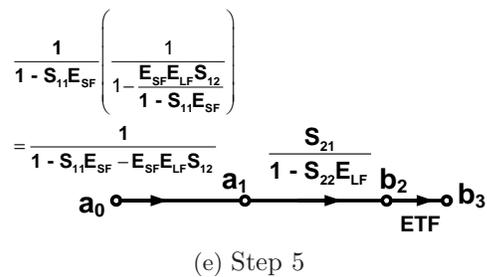
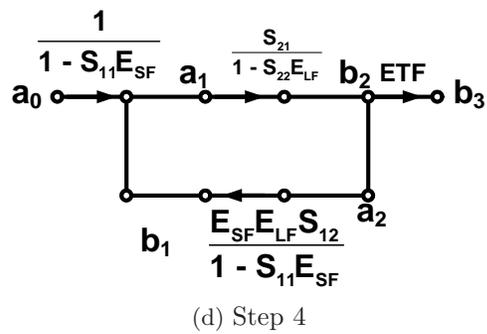
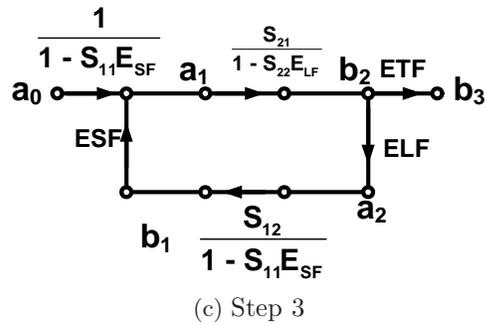
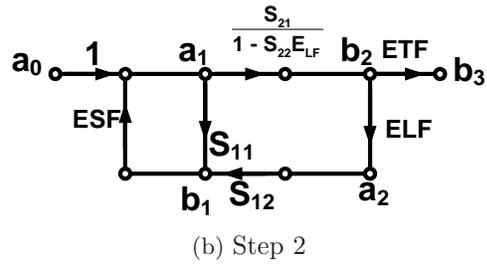
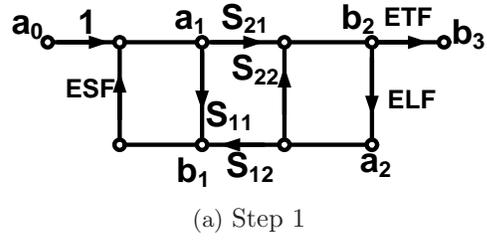


Figure E.2: Step by step signal flow graph reduction for  $S_{21m}$  derivation.

