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Un-Ku Moon

With the ever-increasing demand for portable devices used in applications such as wireless communication, mobile computing, consumer electronics, etc., the scaling of the CMOS process to deep submicron dimensions becomes more important to achieve low-cost, low-power and high-performance digital systems. However, this downscaling also requires similar shrinking of the supply voltage to insure device reliability. Even though the largest amount of signal processing is done in the digital domain, the on-chip analog-to-digital interface circuitry (analog-to-digital and digital-to-analog converters) is an important functional block in the system. These converters are also required to operate with low-voltage supply.

In this thesis, design techniques for low-voltage and low-power analog-to-digital converters are proposed. The specific research contributions of this work include (1) introduction of a new low-voltage switching technique for switched-capacitor circuit design, (2) development of low-voltage and low-distortion delta-sigma modulator, (3) development of low-voltage switched-capacitor multiplying digital-to-analog converter (MDAC), (4) a new architecture for the low-power

Nyquist rate pipelined ADC design. These design techniques enable the implementation of low-voltage and low-power CMOS analog-to-digital converters. To demonstrate the proposed design techniques, a 0.6 V, 82 dB, 2-2 cascaded audio delta-sigma ADC, a 0.9 V, 10-bit, 20MS/s CMOS pipelined ADC and a 2.4 V, 12-bit, 10MS/s CMOS pipelined ADC were implemented in standard CMOS processes.

Design Techniques for Low-Voltage and Low-Power Analog-to-Digital Converters

by

Gil Cho Ahn

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APPROVED:

Major Professor, representing Electrical and Computer Engineering

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Director of the School of Electrical Engineering and Computer Science

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Dean of the Graduate School

I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Gil Cho Ahn, Author

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To my parents Haesook Park and Ikhee Ahn

DESIGN TECHNIQUES FOR LOW-VOLTAGE AND LOW-POWER ANALOG-TO-DIGITAL CONVERTERS

CHAPTER 1. INTRODUCTION

1.1. Motivation

The emerging market for portable devices used in applications such as wireless communication, mobile computing, consumer electronics, etc. requires integration of many functional blocks on a single chip to achieve low-cost, low-power and high-performance. The continued downscaling of the CMOS process to deep submicron dimensions has enabled the building of a system on a chip. However, this downscaling also requires similar shrinking of the supply voltage to insure device reliability [1]. The International Technology Roadmap for Semiconductors [2] shown in Fig. 1.1 predicts a maximum supply voltage equal to 0.8 V in 2007, and only 0.7 V in 2010 for state-of-the-art CMOS digital technology. This aggressive supply scaling requires low-voltage operation for the on-chip interface circuitry (analog-to-digital and digital-to-analog data converters) as well. Even though an increasing amount of signal processing is performed in the digital domain, analog-to-digital converters (ADCs) are still important building blocks to interface real world (analog signal) and digital system on a chip.

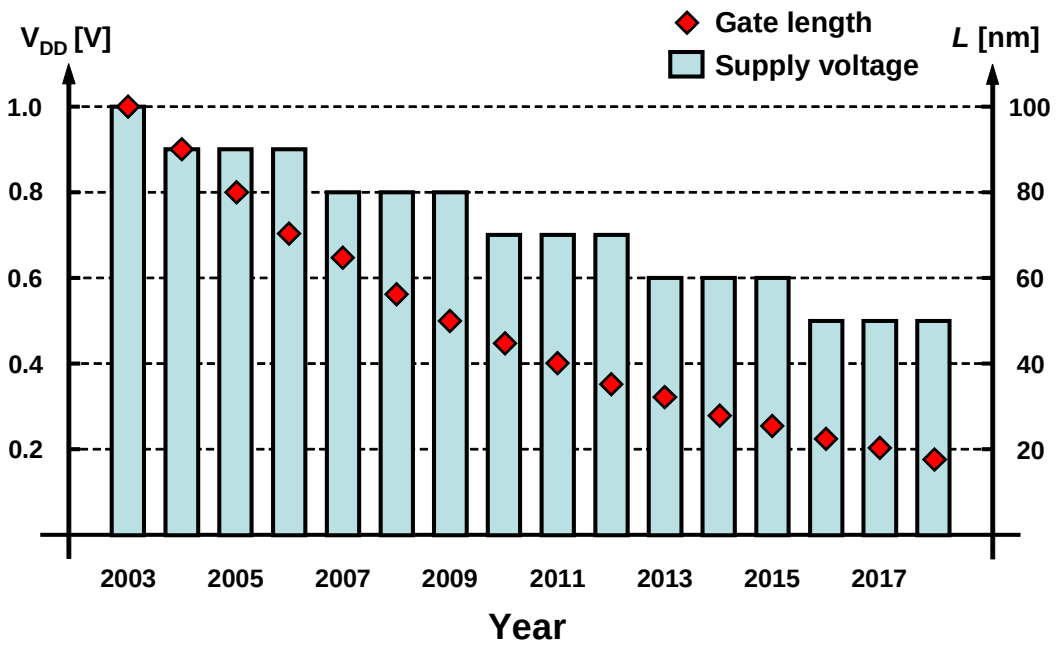


Figure 1.1: Semiconductor Industry Association 2004 forecast of CMOS voltage supply.

Switched-capacitor circuits provide a robust technique for building analog signal processing blocks in CMOS process. The inherent charge storing ability of CMOS technology enables accurate signal processing in mixed-signal applications such as filters and data converters using switched-capacitor circuits. However, supply voltage scaling with miniaturization of CMOS devices resulted in restricted operating conditions for switched-capacitor circuits. New and sometimes complicated design techniques are needed to overcome these issues.

1.2. Contributions

This research is focused on the development of design techniques for low-voltage and low-power analog-to-digital converters. The specific research contri-

butions of this work include:

- Introduction of a new low-voltage switching technique for switched-capacitor circuit design [3].
- Delta-sigma modulator architecture suitable for low-voltage operation [3].

These proposed design techniques enable the implementation of low-voltage and low-power CMOS analog-to-digital converters. To demonstrate the validity of the proposed techniques, an audio delta-sigma ADC design example is presented.

1.3. Organization

Chapter 2 describes the problems associated with low-voltage circuit design. Low-voltage design issues related with floating switch, noise and distortion will be explained.

Chapter 3 introduces design techniques of low-voltage switched-capacitor circuit. Previous design techniques and proposed switched-RC technique will be described.

Chapter 4 presents a design example of low-voltage audio delta-sigma ADC. Fundamentals of delta-sigma ADC and proposed modulator architecture for low-voltage and high-performance operation will be discussed. Circuit implementation of all the building blocks will be described in detail.

Chapter 5 presents a design example of pipelined ADC targeting low-voltage operation. Fundamentals of pipelined ADC and the employed architecture will be described. Circuit implementation of all the building blocks will be explained in detail.

Chapter 6 presents design example of a pipelined ADC targeting low-power and high-resolution. Pipelined architecture and circuit implementation for low-power and high-resolution will be presented.

Finally, the summary of this work, conclusions and future work are described in Chapter 7.

CHAPTER 2. LOW-VOLTAGE CIRCUIT DESIGN ISSUES

This Chapter provides the necessary background to understand why low-voltage circuit operation is required for state-of-the-art deep submicron CMOS technology and describes the three main issues with low-voltage analog circuit design.

2.1. Supply voltage scaling

The goal of CMOS scaling is to achieve high-speed and high-density transistors. It allows faster circuit operation by increasing the cutoff frequency (f_t) and the transconductance (g_m). Fig. 2.1 shows the cross-sectional view of an NMOS transistor. The expressions for its f_t and g_m are given below:

$$f_t = \frac{\mu_n \upsilon_d}{2\pi L^2}\,, \tag{2.1}$$

$$g_m = \mu_n \frac{\varepsilon_{ox}}{t_{ox}} \frac{W}{L} (V_{GS} - V_{TH})\,, \tag{2.2}$$

where μ_n is the mobility of electrons, ε_{ox} is the permittivity of the oxide, t_{ox} is the oxide thickness, W is the channel width, L is the channel length, V_{TH} is the threshold voltage and V_{GS} is the voltage between gate and source nodes. As shown in eq. 2.1 and eq. 2.2, both g_m and f_t are functions of channel length L. Clearly, both transconductance and cutoff frequency increase with decreasing channel length. Furthermore, the transconductance is also improved by the reduction in the oxide thickness (t_{ox}) in scaled devices.

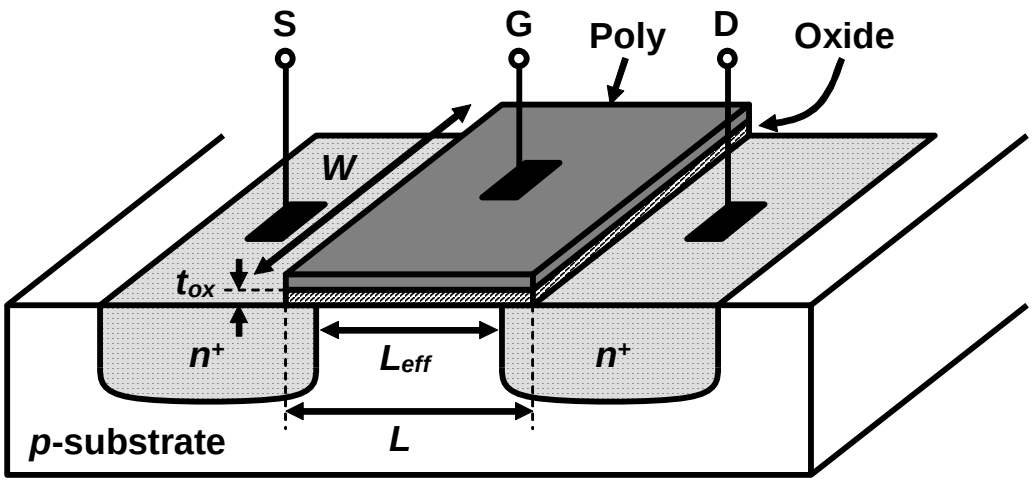


Figure 2.1: Structure of a NMOS device.

However, scaling of supply voltage is also required along with device scaling for two main reasons. First, low-power operation (especially for the digital circuits) creates strong demand for low supply voltage. The power in digital circuits is a function of supply voltage (V_{DD}) as shown in eq. 2.3:

$$P_{DIGITAL} = C{V_{DD}}^2 f + I_{leak} V_{DD}\,, \tag{2.3}$$

where I_{leak} is the leakage current of the transistors and C is the capacitance switched at frequency f. Second, the reliability issues associated with advanced submicron technology, such as gate oxide breakdown and drain-induced barrier lowering (DIBL) effects, limit the maximum allowable supply voltage. Drain-induced barrier lowering is a phenomenon in which the increased electric field due to shorter channel lengths results in accelerated electrons often referred to as "hot electrons". These *hot electrons* can cause lower saturation current, threshold voltage drift and even latch-up with large drain-source voltage [4]. In order to suppress these effects, the gate-oxide thickness is reduced to increase the vertical electric field and thus enabling stronger control of the channel by the gate terminal. At the same time,

the drain-to-source voltage needs to be scaled to reduce the lateral electric field to circumvent DIBL. Furthermore, if the applied supply voltage over the gate is not scaled proportionately, then the gate oxide will experience large electric field, which can cause oxide breakdown. These voltage limitations of the technology mandate low-voltage operation of the on-chip mixed-signal interface circuitry to avoid violating the reliability constraints of the technology.

2.2. Floating switch problem

The switched-capacitor (SC) technique is the most commonly used method for building analog blocks in CMOS technology. Fig. 2.2 shows a typical SC integrator. One of the key components of this SC circuit is the floating switch shown in the dotted circle. The operation of the SC integrator is as follows. During the $\phi 1$ phase, the input signal V_{IN} is sampled into the capacitor C_S through the CMOS switch. Ideally, the CMOS switch in this on-state should act as a constant linear conductor. However, in practice, the conductance of the switch varies with the input signal level as shown in Fig. 2.3. For example, the NMOS switches are "on" when the input signal is lower than $V_{DD} - V_{TN}$. As input signal V_{IN} is lowered, the conductance of the NMOS switch increases. Similarly, the PMOS switches are "on" when the input signal is higher than $|V_{TP}|$. The conductance of the PMOS switch increases as V_{IN} goes high. If the supply voltage is large enough compared to the sum of the threshold voltages of NMOS and PMOS transistors, the conductance of the CMOS switch is constant over the whole input signal range as shown in Fig. 2.3(a). On the other hand, if the reduced supply voltage is comparable to the sum of the threshold voltages as shown in Fig. 2.3(b) then the input signal range for the constant conductance will be reduced . However, if the supply

voltage is less than the sum of threshold voltages, then both transistors turn off in the mid-input signal range. For proper operation, the gate overdrive voltage must be much larger than the sum of the CMOS switch threshold voltages and the input signal amplitude. Thus, higher gate overdrive voltage has been used in previous low-voltage SC circuits, using global clock boosting or bootstrapping by voltage multiplication for the clock signals [1][5][6]. The next chapter describes these existing low-voltage SC circuits in detail.

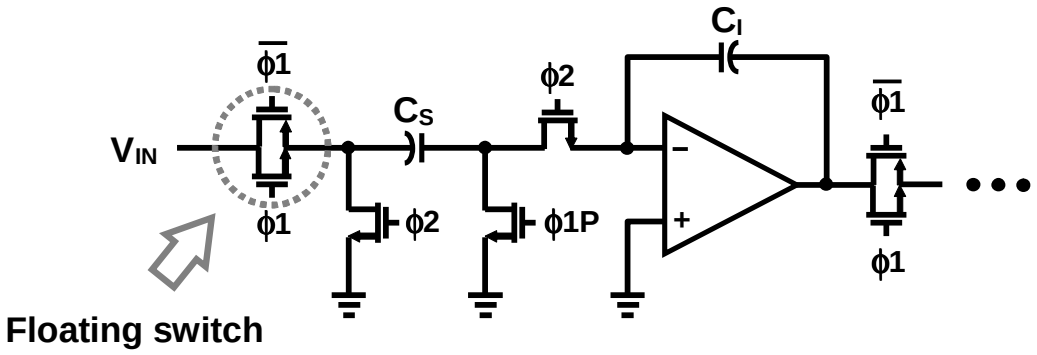


Figure 2.2: Conventional SC integrator with the floating switches.

2.3. Noise

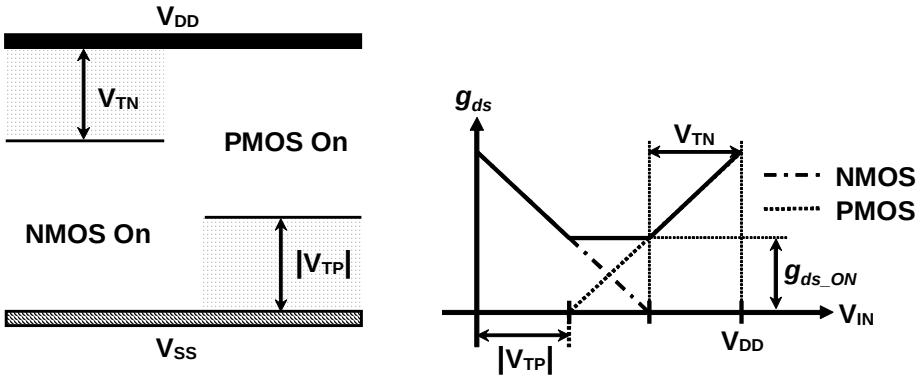
Electronic noise due to both sampling switches and the amplifier poses considerable design challenges at low supply voltage. Scaling down of the supply voltage dictates reduction of the available input and output signal swing range. Therefore the thermal noise in the circuit must be scaled proportionally to maintain the same dynamic range. However, there exists a trade-off between noise and power consumption. For example, in the SC circuit, the kT/C noise power

is inversely proportional to capacitor value C. Traditional low-noise SC circuit design techniques involve choosing larger capacitors in order to achieve high SNR. However, this increased capacitive load results in excess power consumption.

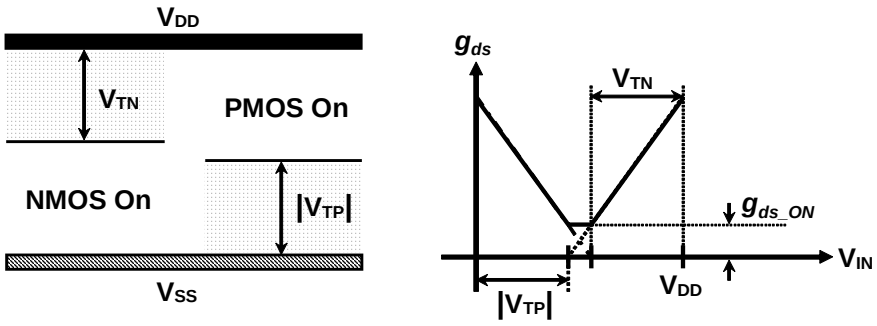
2.4. Distortion

Distortion also limits the overall performance of the system. Large signals permitted with high supply voltages typically result in wide dynamic range. In applications requiring low distortion, all signals can be scaled down at the expense of lower signal power. However, with sub-1 V supply, the conflicting requirements of large signal swing and low distortion make a challenging design task. Typically, the dominant sources of distortion in low-voltage SC circuit are floating switch and the amplifier. As shown in Fig. 2.3(b), the input signal range for the constant conductance of CMOS switch decreases with supply voltage scaling. This results in more nonlinearity because of the signal dependent on-resistance of the switch. The RC time constant variation with different signal level causes different settling time and creates harmonic tones. Rail-to-rail output stage is preferred in low-voltage amplifier design to maximize the dynamic range. However, such an amplifier usually provides relatively modest linearity under very low supply voltage conditions.

In the following chapters, both architectural and circuit-level techniques are proposed to overcome the floating switch, noise and distortion issues mentioned in this chapter.



(a)



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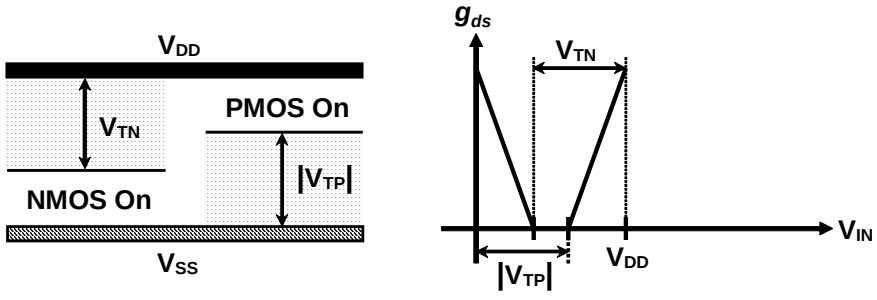


(c)

Figure 2.3: Conductance of MOS switches.

CHAPTER 3. LOW-VOLTAGE SWITCHED-CAPACITOR CIRCUITS

Switched-capacitor (SC) technique provides an accurate and robust way of designing CMOS analog circuits. However, the realization of a low-voltage SC circuit becomes difficult, since the floating switches required in conventional switched-capacitor circuits are not operational for very low supply voltages. Existing low-voltage techniques for switched-capacitor circuit implementation are first described, and new techniques shown to further improve the performance of these circuits are described.

3.1. Multi-Threshold MOSFET

Lower threshold NMOS and PMOS transistors can be used at the expense of an extra mask layer for the CMOS process. It gives a simple and straightforward solution for the low-voltage SC circuit implementation, except for the extra cost of additional processing. However, the leakage current of MOS transistor with low threshold voltage limits the accuracy of charge transfer, and hence the effectiveness of this approach.

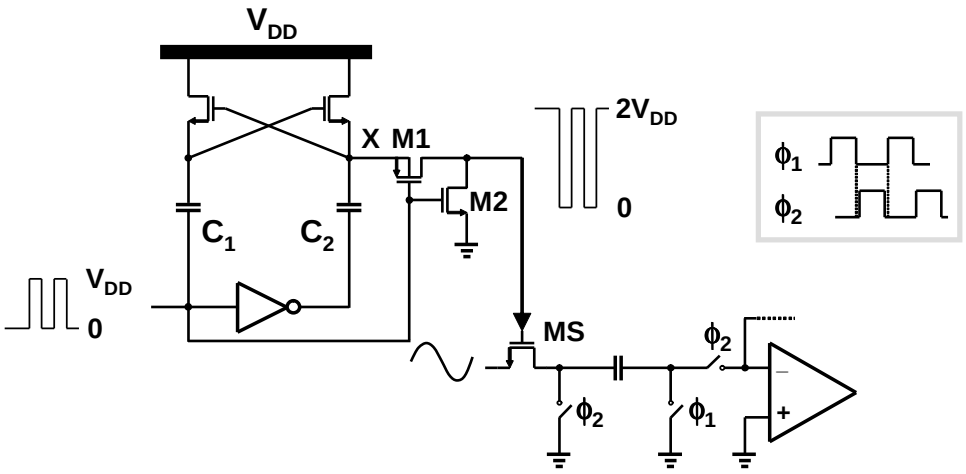


Figure 3.1: Schematic of clock boosting circuit.

3.2. Clock Voltage Boosting

Higher gate overdrive voltage can be used instead of using lower threshold voltage MOS transistors for the low-voltage SC implementation. Fig. 3.1 shows a clock boosting circuit proposed by Nakagome *et al* [5]. It provides approximately $2V_{DD}$ output swing with V_{DD} input clock swing as indicated by eq. 3.1:

$$V_{HI} = 2V_{DD}\frac{C_2}{C_2 + C_p + C_{gate,MS}}\,, \tag{3.1}$$

where C_p is the parasitic capacitance at node X and $C_{gate,MS}$ is the gate capacitance of the floating switch MS. When the input signal is at V_{DD}, capacitor C_2 is charged to V_{DD} by connecting the inverted output level V_{SS} to the bottom plate and V_{DD} to the top plate. During this phase, the output level of the boosted clock is lowered by turning off PMOS transistor M1 and turning on NMOS transistor M2. When the input signal is V_{SS}, bottom plate of C_2 goes up to V_{DD} and the M1 transistor is *on* resulting in boosted output voltage at the gate of MS. During this phase,

M4 is *off* and C_1 is charged to V_{DD}. A pipelined ADC design using boosted clock was reported in [6]. However, scaled fine-line width CMOS process cannot sustain the high voltage ($2V_{DD}$) stress because of reliability issues, such as oxide breakdown explained in Chapter 2. This technique is effective for a high-voltage CMOS process.

3.3. Clock Bootstrapping

Clock bootstrapping technique [1] [7] [8] also enables a low-voltage switching operation using higher gate overdrive voltage. Fig. 3.2 shows the basic concept of bootstrapped circuits. During $\phi 2$ phase, capacitor C_{BAT} is precharged to V_{DD} and switch MS is turned off by connecting its gate to ground. During the following $\phi 1$ phase, capacitor C_{BAT} is connected between the gate and source of the switch MS. It provides a constant V_{GS} equal to V_{DD} independent of input signal level. Fig. 3.3 shows a real implementation of bootstrapping circuit reported in [1]. It improves circuit reliability compared to the clock voltage boosting scheme by limiting the terminal voltage between any two nodes to less than the supply voltage. Linearity of the switch is also improved due to constant on-resistance resulting from constant V_{GS}. However, it requires separate bootstrapping circuits for each switch, resulting in more die area and power consumption.

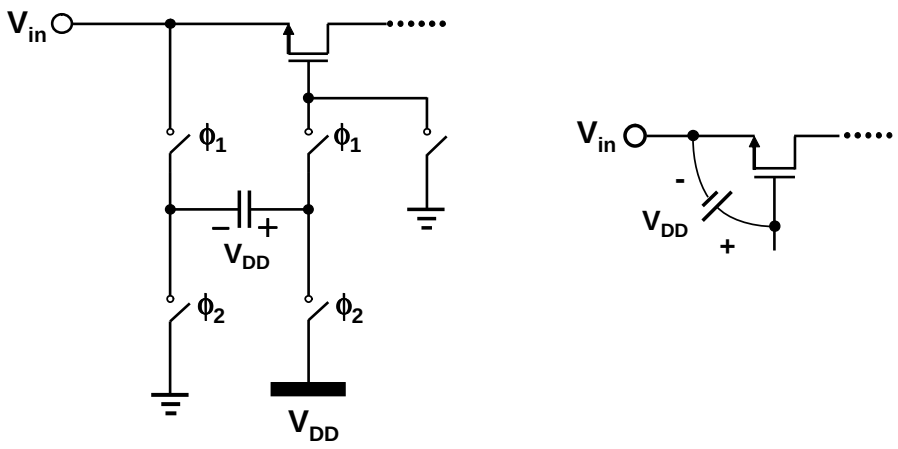


Figure 3.2: Conceptual diagram of bootstrapping circuit.

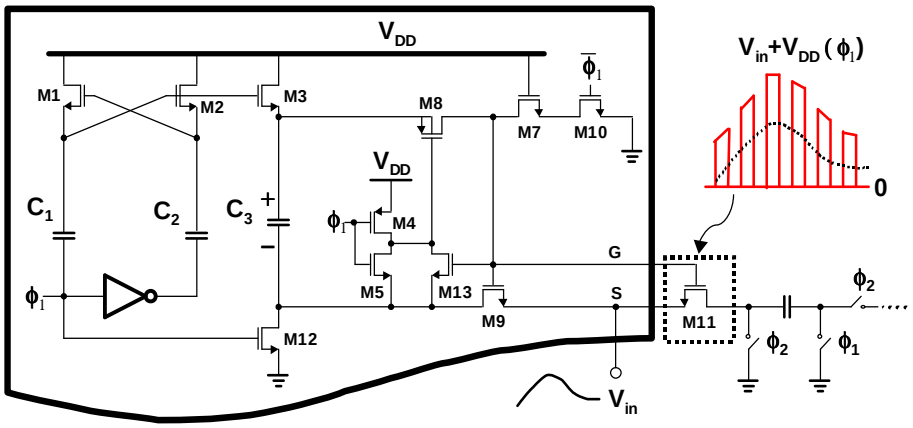


Figure 3.3: Full schematic of bootstrapping circuit.

3.4. Switched-Opamp Technique

The switched-opamp (SO) technique [9][10][11] [12][13] enables the low-voltage switched-capacitor operation by eliminating the floating switch. Instead of using the floating switch with higher gate overdrive voltage, the amplifier itself is used as a switch combined with additional reference switch. Fig. 3.4 shows a switched

opamp followed by the integrator. The switched opamp is simply a two-stage Miller-compensated amplifier with two extra switches. The output impedance of this amplifier is controlled by turning on and off these switches. During $\phi 1$ phase, the amplifier is *on* and the output signal is sampled on the capacitor C_S. During $\phi 2$ phase, the high output impedance of the amplifier allows the integrating operation of the following stage by connecting the bottom plate of the sampling capacitor C_S to the ground. It provides reliable low-voltage switching operation by avoiding any high terminal voltage between any two nodes. However, this technique faces a trade-off between speed and accuracy due to the slow start-up transients of the opamp.

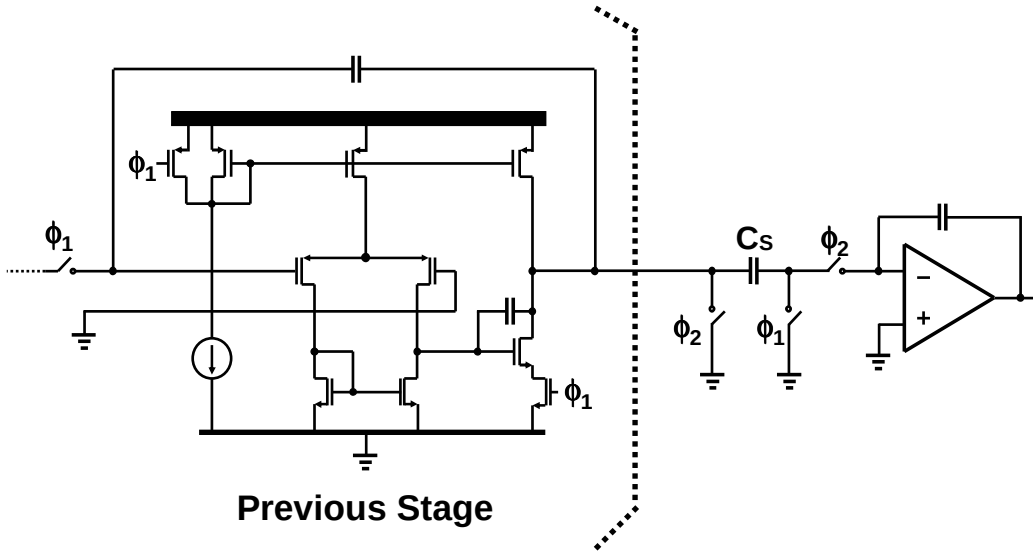


Figure 3.4: Schematic of switched-opamp implementation.

3.5. Opamp-Reset Switching Technique

The opamp-reset switching technique (ORST) [14][15][16] enables true low-voltage operation by eliminating the floating switch, just as the switched opamp (SO) technique. The ORST also improves operating speed by allowing the opamp to remain in the active state. Fig. 3.5 shows the schematic of an integrator driven by an ORST. It uses unity-gain feedback configuration to provide the fixed reset level for the following stage. During $\phi 1$ phase, the amplified output signal of previous stage is sampled into the sampling capacitor C_S. During the following $\phi 2$ phase, sampled charge in the C_S is transferred into the integrating capacitor C_I by connecting the bottom plate of the C_S to the reset level provided by the unity-gain configuration of previous stage. Though this technique enables faster operation, it has higher power consumption and settling issues due to unity gain feedback during the reset phase. Moreover, different output common-mode levels between two phases makes it harder to implement it using a fully differential circuit.

3.6. Switched-RC Technique

In this work, a different solution based on switched-RC technique is proposed. The basic concept is illustrated in Fig. 3.6. As shown, the input SC branch of the conventional structure is replaced by a switched-RC branch, in which the floating switch of the conventional integrator is replaced by a resistor R_1. This modification results in two advantages. First, it obviates the need for the floating switch, and second, the linearity of the input sampling is improved. The operation of this

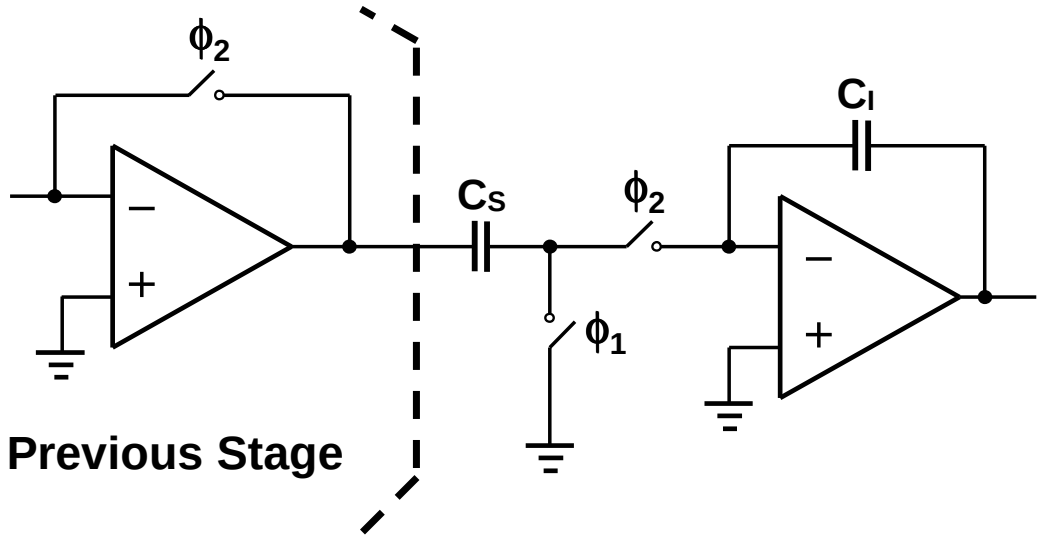


Figure 3.5: Opamp-reset switching technique (ORST).

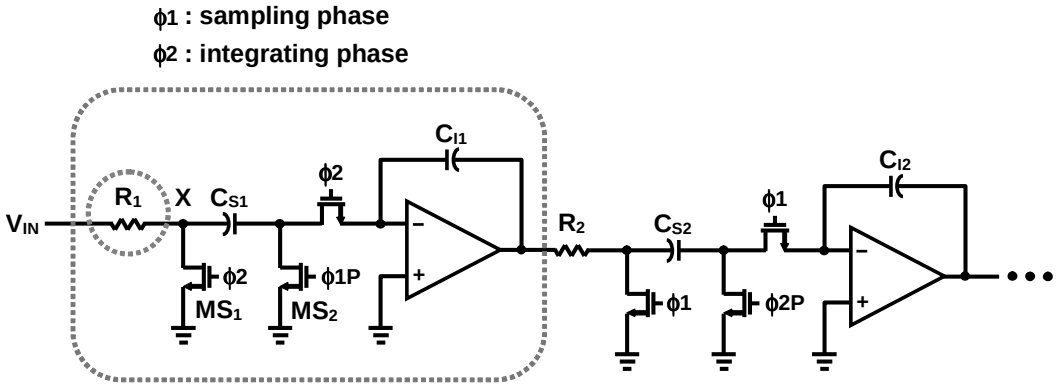


Figure 3.6: Low-voltage integrator with switched-RC input branch.

circuit is as follows. During the $\phi 1$ phase, the signal is sampled into the capacitor C_{S1} through resistor R_1 and the MS_2 switch. During the following $\phi 2$ phase, the signal charge is transferred to the integrating capacitor C_{I1} by connecting the bottom plate of C_{S1} to ground through switch MS_1. During this phase, the voltage V_X at node X is determined by the ratio of the ON resistance R_{ON1} of the MS_1

switch and the resistor R_1:

$$V_X(n+\frac{1}{2}) = \frac{R_{ON1}}{R_1 + R_{ON1}} V_{IN}(n+\frac{1}{2})\,. \tag{3.2}$$

The output voltage of the integrator can be found from charge conservation as:

$$V_{OUT}(n+\frac{1}{2}) = V_{OUT}(n) + \frac{C_{S1}}{C_{I1}} V_{IN}(n) - \frac{C_{S1}}{C_{I1}} \frac{R_{ON1}}{R_1 + R_{ON1}} V_{IN}(n+\frac{1}{2})\,. \tag{3.3}$$

The gain error due to the ON resistance of switch MS is the last term in eq. 3.3. For sufficiently high oversampling ratio (OSR), $V_{IN}(n+\frac{1}{2})$ will be very close to $V_{IN}(n)$, and the error can then be approximated by eq. 3.4:

$$\text{Gain Error} = \frac{C_S}{C_I} \frac{R_{ON}}{R_1 + R_{ON}}\,. \tag{3.4}$$

Note, that the gain error introduced by the non-ideal ground at node X does not necessarily result in large distortion, as shown next. In equation 3.4, R_{ON} is the only nonlinear term, and hence the sole source of nonlinearity. Its value is given in eq. 3.5, which shows that R_{ON} is a function of $V_{DS} = V_X$:

$$R_{ON} = \frac{1}{\mu_n C_{OX}(W/L)[(V_{GS} - |V_{TH}|) - V_{DS}]}\,. \tag{3.5}$$

Even though V_X changes with the input signal, the signal variation at node X is attenuated by the ratio of R_1 and R_{ON} (see eq. 3.2), and hence the change in R_{ON} is small compared to that of a floating switch. Both the nonlinearity of the input sampling and the gain error can be reduced by making the linear resistor R_1 much larger than the variable ON resistance of the reset switch MS. However, there is a trade-off. Larger R_1 results in improved gain accuracy and lower distortion during the $\phi 2$ phase, but during the $\phi 1$ phase, a large $R_1 C_S$ time constant degrades the sampling accuracy. Thus R_1 should be small enough to satisfy the settling requirement during the sampling phase.

The gain of the opamp in a switched-RC (SRC) integrator changes significantly between the phases. During the $\phi 1$ phase, the amplifier drives the resistive load R_2, which results in a low DC gain due to the low load impedance. However, during this reset phase, the charge stored in C_I will be preserved, and the output voltage of the integrator will be recovered in the following $\phi 2$ phase, when the gain of amplifier returns to its high value as its resistive load is removed. The virtual ground voltage therefore also returns to its low value needed for the charge transfer. Hence, the effective DC gain of the amplifier in a SRC integrator can be the same as in a conventional SC one. Note also that the voltage between any two nodes is always less than the supply voltage, and therefore this technique is free from device reliability problems.

As illustrated in Fig. 3.6, the phasing of the clock signals in adjacent SRC integrators must be shifted. Thus, there is a $T/2$ delay between the input and the output of the integrator, where $T = 1/f_{clk}$ is the clock period.

CHAPTER 4. 0.6 V 82 dB 2-2 CASCADED AUDIO DELTA-SIGMA ADC

This chapter presents the design of low-voltage audio delta-sigma ADC. The main purpose of this work is to introduce low-voltage design techniques that enable high performance analog circuit operation in deep submicron processes. Architectural and circuit design techniques are presented for switched-RC circuits operating under very low supply voltage conditions. To demonstrate the proposed techniques, a wide-dynamic-range audio delta-sigma ADC with sub-1 V supply and low (1 mW) power consumption was designed. While the realization was demonstrated in a 0.35 μm CMOS technology, the key principles of the proposed techniques, which depend on the relative voltages of transistor threshold and supply, are directly applicable in finer linewidth submicron CMOS processes.

4.1. Delta-Sigma ADC Basics

4.1.1. Fundamentals of ADC

An analog-to-digital converter is a system that converts analog input signal such as voltage and current into digital output. It samples signal with discrete time step and quantizes with discrete decision levels. Fig. 4.1 shows the basic concept of an ADC.

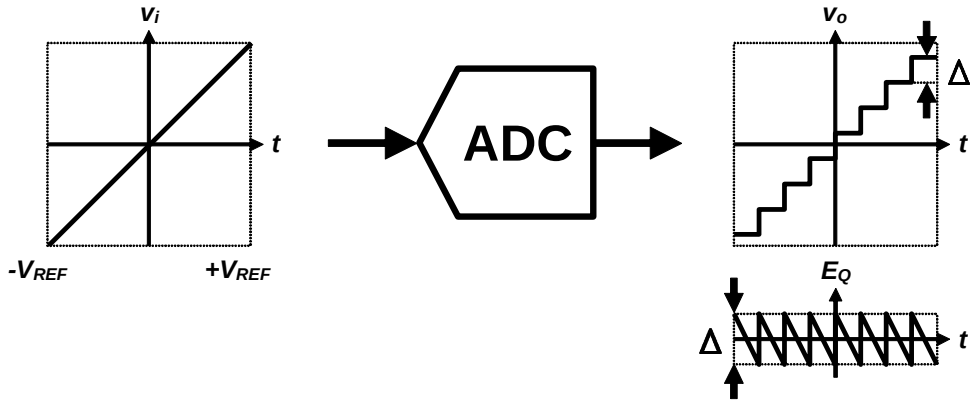


Figure 4.1: Concept diagram of an analog-to-digital converter.

In the Fig. 4.1,

$$\Delta = \frac{2V_{REF}}{2^N - 1}\,. \tag{4.1}$$

where N is the output bit resolution of the ADC, and Δ is the quantizer step size. Under the assumption of uniformly distributed quantization error, the power of the quantization error can be given by

$${\sigma_E}^2 = \frac{\Delta^2}{12}\,, \tag{4.2}$$

and the maximum SNR of N-bit ideal ADC can be approximated by eq. 4.3

$$\text{SNR} = 6N + 2\text{dB}\,. \tag{4.3}$$

Fig. 4.2 shows the spectrum of a Nyquist-rate ADC output. If the input signal frequency (f_{in}) is less than half of the sampling frequency (f_S) the input signal can be restored according to the Nyquist sampling theorem.

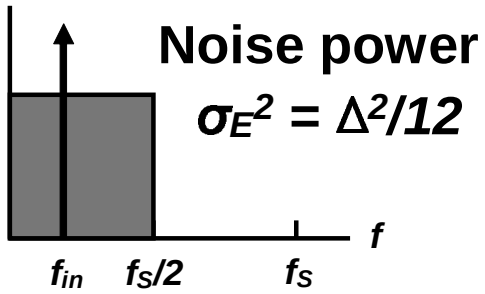


Figure 4.2: Spectrum of Nyquist rate ADC.

4.1.2. Fundamentals of a delta-sigma ADC

The two main features of a delta-sigma ADC are oversampling and noise shaping. As described in the previous section, the quantization noise power is assumed to be uniformly distributed over the pass band, from DC to $f_S/2$. If we increase the sampling rate, then this noise power will be spread out over increased frequency range as shown in Fig. 4.3. And if the out-of-band noise is filtered out in the digital domain, then the SNR can be improved by the ratio $\frac{f_s}{2f_B}$. However, increasing SNR just by the oversampling ratio (OSR) is impractical. For example, to get a 14-bit SNR with 1-bit quantizer, OSR of 2^{28} is required. To relax the requirement of OSR, noise shaping is applied. With the noise shaping, higher SNR can be achieved with reasonable OSR. Fig. 4.4 shows the block diagram of the 1st-order 1-bit delta-sigma modulator. The transfer functions for the signal and quantization noise are given in eq. 4.5 and eq. 4.6

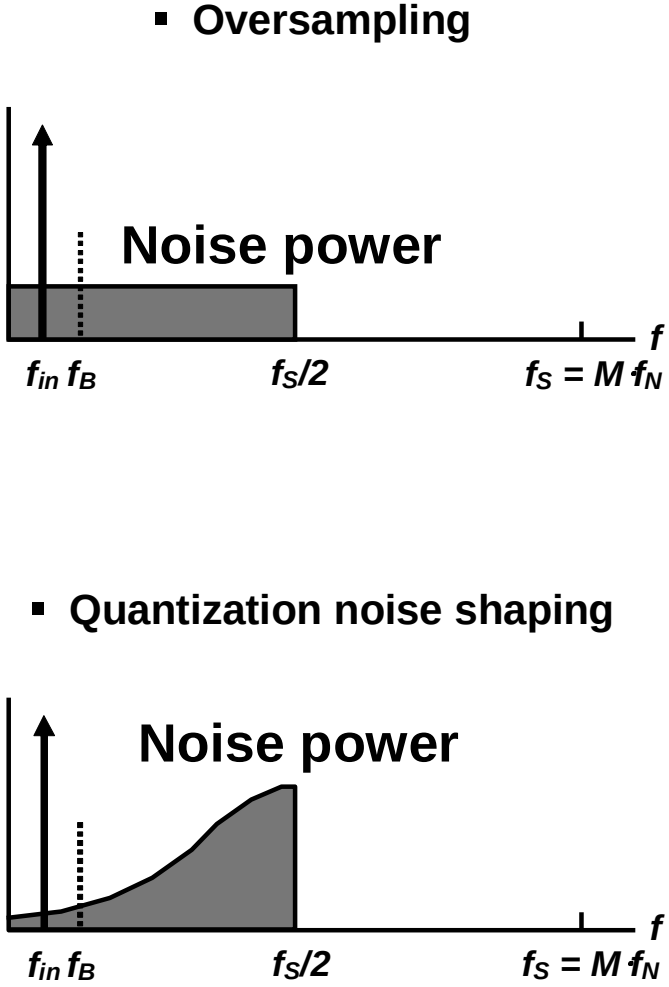


Figure 4.3: Spectrum of oversampling ADC.

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})Q(z) \tag{4.4}$$

$$STF = z^{-1} \tag{4.5}$$

$$NTF = 1 - z^{-1}\,, \tag{4.6}$$

where $Q(z)$ is a quantization error. Here, the quantization noise $Q(z)$ is shaped by the first order differentiator. It results in lower noise level within the pass band

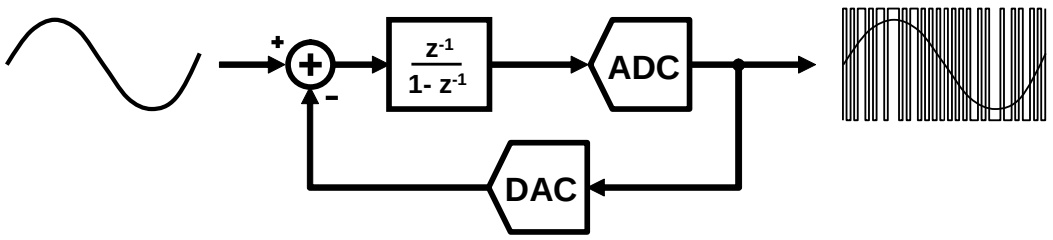


Figure 4.4: Block diagram of the 1st order delta-sigma modulator.

and higher noise level outside of the signal band. Thus, with noise shaping, higher SNR can be achieved with reasonable OSR.

4.2. Modulator Architecture

As discussed in the Chapter 2, there are three main problems in low-voltage analog IC design. A circuit solution is proposed in Chapter 3 for the problem associated with floating switches. For the other two problems (distortion and noise), architectural solutions can be found. These are discussed in this Chapter, in the context of an audio ADC.

For the targeted performance (13∼14 ENOBs) and relatively narrow bandwidth, delta-sigma ADC converters seems to be optimal. The achievable SNR with such converters improves with increased order, higher resolution internal quantizer, and higher oversampling ratio (OSR). Internal resolution higher than 1 bit requires digital correction or filtering of the nonlinearity of the internal DAC, which increases the complexity and power dissipation. Choosing a single-bit internal quantization, and using the Schreier Toolbox in MATLAB [17], it was found that a fourth-order modulator combined with a relatively low oversampling ratio (OSR

= 64) is adequate to meet the required performance.

A 2-2 MASH architecture was selected, as it allows a larger input signal for stable operation than a single fourth-order loop. This structure consists of two stages, each containing a second-order delta-sigma modulator. The first stage converts the input signal into one bit stream with filtered quantization noise Q1, while the second stage converts only Q1, and adds its own filtered quantization noise Q2.

The configuration chosen for both stages of the MASH is the low-distortion feed-forward topology proposed in [18]. In this architecture, under ideal conditions, the loop filter processes only the shaped quantization noise and so there is no distortion introduced by the integrator. Hence the linearity requirements on the opamps are relaxed. This is an important advantage for low-voltage operation with nonlinear amplifiers.

In the proposed modulator topology, this feed-forward architecture is implemented with half delay integrators. Since the integrators used the SRC circuits introduced in Chapter 3, they provide a $T/2$ delay between stages, as opposed to the usual T or 0 delay. This necessitates the inclusion of additional $T/2$ delays ($z^{-1/2}$ blocks) in the architecture, to insure synchronized charge transfer [10]. These delays are implemented in the SRC input branches of the comparators and in the digital feedback, and do not require extra amplifiers. Though additional $T/2$ delays are used for the synchronization, this proposed modulator topology with half delay integrator allows signal transfer from input to the integrator. This results in a first order shaped signal transfer function through the integrators. This shaping can be ignored if OSR is high enough. Inaccurate matching of gain coefficients of the modulator due to non-ideal parameters also causes residual input signal component in the loop filter. These signal terms propagating through the

integrator path will cause distortion and limit the linearity of the system.

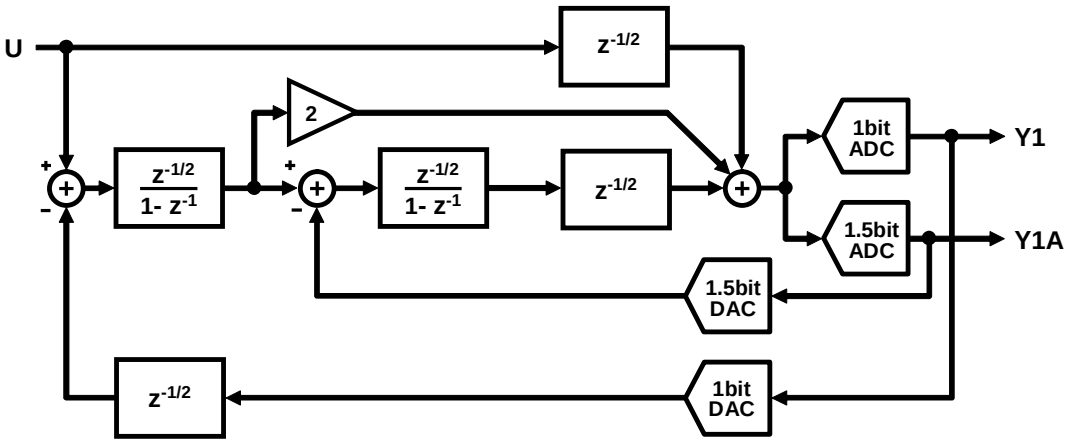


Figure 4.5: Low-distortion feed-forward second order delta-sigma modulator with local feedback.

For further linearity enhancement with large input signal, the nonlinear local feedback arrangement proposed by Fujimori *et al.* [19], containing a 1.5-bit quantizer, is used. The local feedback continuously monitors the integrator output and restricts the signal swing range by feeding back a quantized error signal to the input of the second integrator. The second stage overloading can be prevented by choosing proper decision levels of the 1.5-bit local feedback quantizer. Since the second stage is not overloaded, the distortion caused from the saturated integrator output of the first stage can be cancelled out by the cascaded second stage output with the digital noise cancellation logic. The quantization noise of the local feedback can be subtracted by a digital noise cancellation logic just as the 1-bit quantization error. The local feedback is not activated if the input signal of quantizer is between the decision levels of the two comparators used in the 1.5-bit internal quantizer. Note that the 1.5-bit DAC used in the local feedback loop has relaxed linearity requirements, since the nonlinear error at the input of the second

integrator is shaped by the loop. The resulting block diagram of the second-order stage is shown in Fig. 4.5. The combination of these two linearity enhancement techniques of the delta-sigma architecture improves both the distortion and noise immunity of the converter.

Fig. 4.6 illustrates the overall block diagram of the MASH ADC. Due to the low-distortion configuration used, the second integrator output of the first stage (V_1) can be directly connected to the second stage without using any additional subtraction. The coefficients of all integrators and feed-forward paths were found so as to maximize the input signal range without overloading the amplifiers. Fig. 4.7 shows the block diagram of the digital noise cancellation logic. It is implemented off-chip, using post-processing in MATLAB. The overall output signal of the ADC is given by

$$Y = z^{-3/2}(3 - 3z^{-1} + z^{-2})U + 15(1 - z^{-1})^4 Q_2 \,. \tag{4.7}$$

Note that the signal transfer function, in addition to a delay, has a small gain variation which is negligible in the signal band.

Behavioral simulations performed by modelling the amplifiers with 50 dB DC gain, 50 dB SFDR and 0.4% capacitor matching indicate higher than 100 dB SFDR of the complete converter. More than 1.5 dB improvement in the permissible peak input signal due to local feedback is also observed in these simulations.

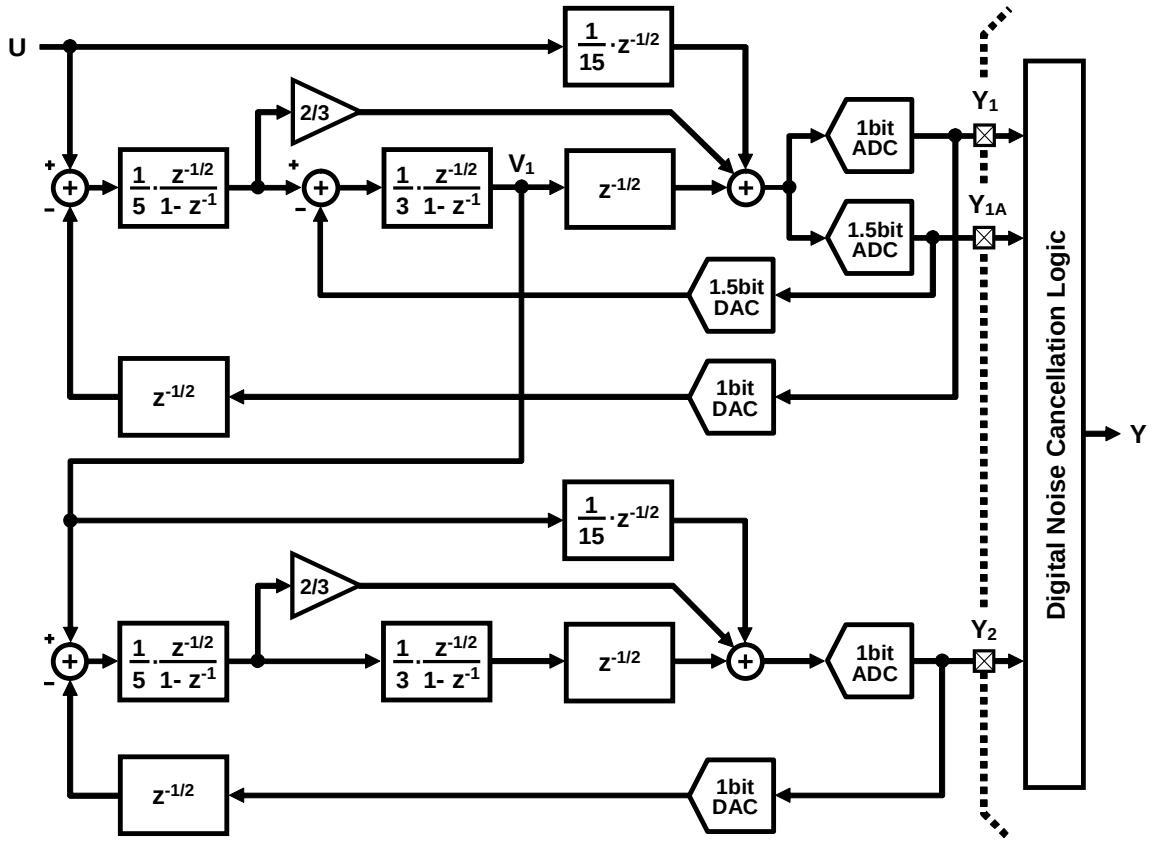


Figure 4.6: Block diagram of two-stage cascaded delta-sigma modulator.

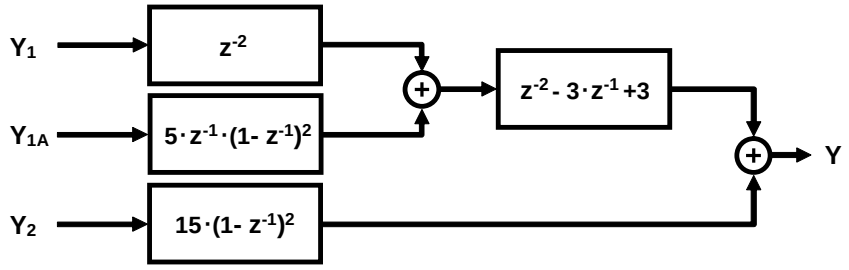


Figure 4.7: Digital noise cancelation logic.

4.3. Circuit Implementation

While the principle of the SRC circuit has been described in Chapter 3, its actual implementation in our ADC is somewhat different, since the input branches are also used for common-mode adjustments and feedback. The implemented circuits will be discussed next.

4.3.1. Split switched-RC input branch

In a low-voltage integrator, it is desirable to set the common-mode (CM) level of the input and output at the middle of the supply voltage, i.e., $V_{CM} = (VDD + VSS)/2$, to maximize signal swing. At the same time, any DC bias voltage connected to the sampling capacitors must be close to VDD or VSS in order avoid any floating switching problem. For this reason, two different input common-mode levels were applied to the integrator during the sampling and the integrating phases. Such use of two different input CM voltages resulted in a large amount of common-mode charge injection. Thus, the input or interstage branches of all integrators should also perform a level shifting operation, in addition to sampling and transfer/amplification of the input signal. Fig. 4.8(a) shows an earlier implementation of this level shifting in a low-voltage switched capacitor integrator [11]. A level-shifting capacitor C_{LS} is used to cancel the common-mode charge injection, by providing an opposite polarity charge. However, this added SC branch causes more kT/C noise and also increases the opamp noise gain.

In our implementation, a split input switched-RC branch is used to keep constant CM level of the integrator, as shown in Fig. 4.8(b). During the integrating

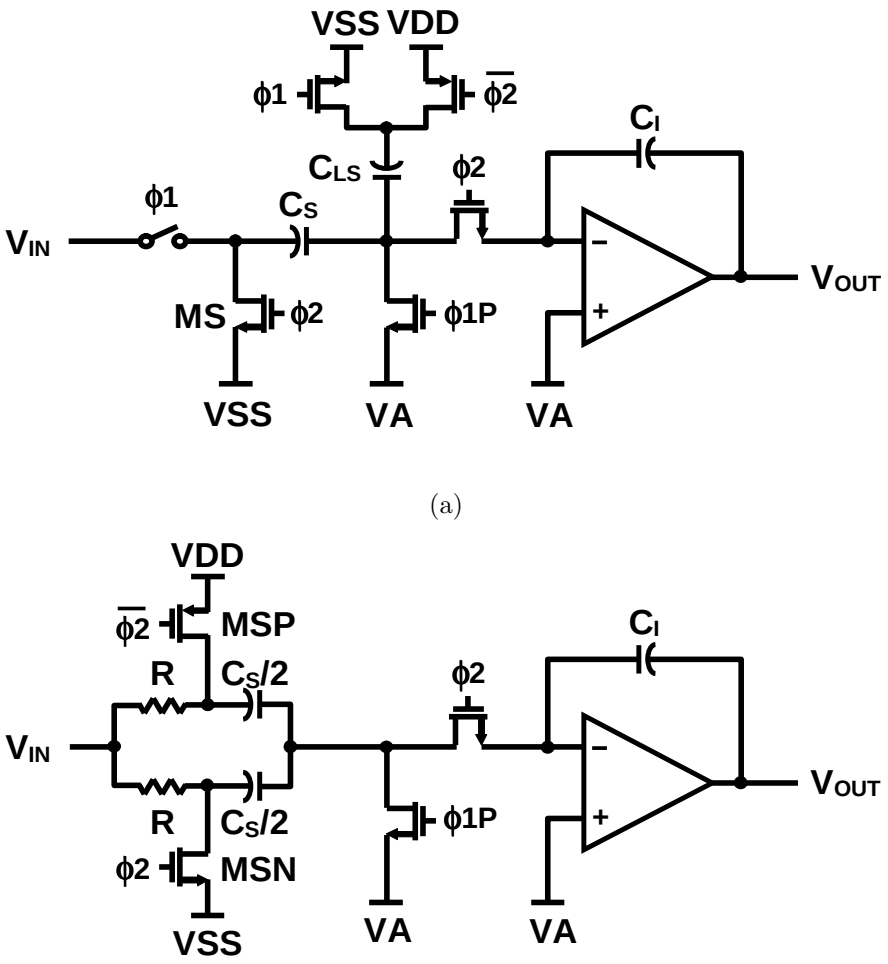


Figure 4.8: (a) Traditional low-voltage switched capacitor integrator. (b) Low-voltage integrator with split switched-RC technique.

phase, one half of the sampling capacitor is connected to VDD, while the other half is connected to VSS. This results in a constant input common-mode level of $VDD/2$ for the integrator during both phases, obviating the need for an additional level-shifting capacitor with noise penalty.

4.3.2. Pseudo-differential integrator using switched-RC technique

Fig. 4.9 shows the complete schematic of a pseudo-differential integrator using the switched-RC technique, and an example timing diagram. Split switched-RC input branches are used to maintain a constant input common-mode voltage. The effective DAC reference voltage is doubled by alternating the connection of the DAC capacitors C_{DAC1} from VDD to VSS or vice versa, depending on the comparator's output. This helps to reduce the size of C_{DAC1}, resulting in lower noise. Integrator input referred noise power due to the kT/C noise and the amplifier thermal noise are given in eq. 4.8 and eq. 4.9

$$v_{n\_kT/C}{}^2 = \frac{2kT(2C_{S1} + C_{DAC1} + 4C_{M1})}{4C_{S1}{}^2}\,, \tag{4.8}$$

$$v_{n\_Opamp}{}^2 = \left(\frac{2C_{S1} + C_{DAC1} + 4C_{M1}}{2C_{S1}}\right)^2 v_{niOp}{}^2\,, \tag{4.9}$$

where $v_{niOp}{}^2$ is the amplifier thermal noise power which is referred into the input of opamp. As shown in the equations, the input referred kT/C noise due to C_{DAC1} is scaled by $C_{S1}{}^2$, and the opamp noise will be amplified by the ratio of C_{S1} and the total capacitance connected to the virtual ground node.

A pseudo-differential architecture is used to circumvent the challenging design issues associated with low-voltage common-mode feedback circuit design. Capacitors C_{M1}, connected to the switched-RC branches of the next stage, are used for the common-mode feedback. The basic operation of the switched-RC common-mode feedback is similar to that proposed for pseudo-differential circuits earlier in [20], except for the use of switched-RC branches. Fig. 4.10 shows the operation during two different phases of the common-mode feedback loop formed with the following stage switched-RC branches. During $\phi 1$, the desired output common-mode

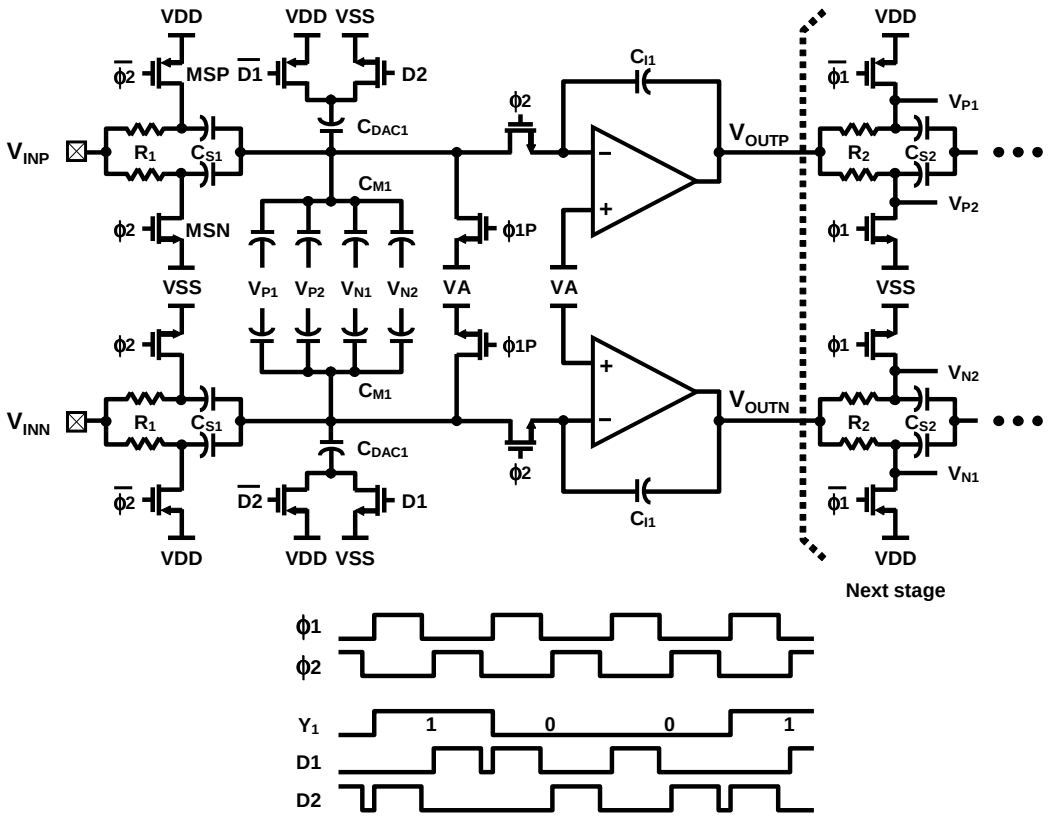
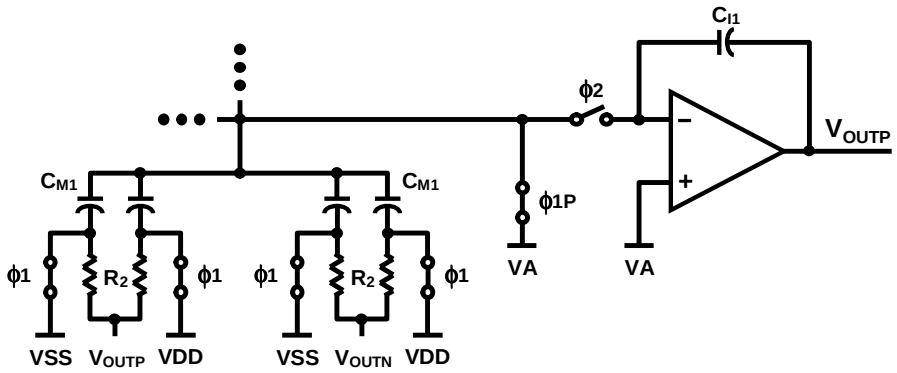


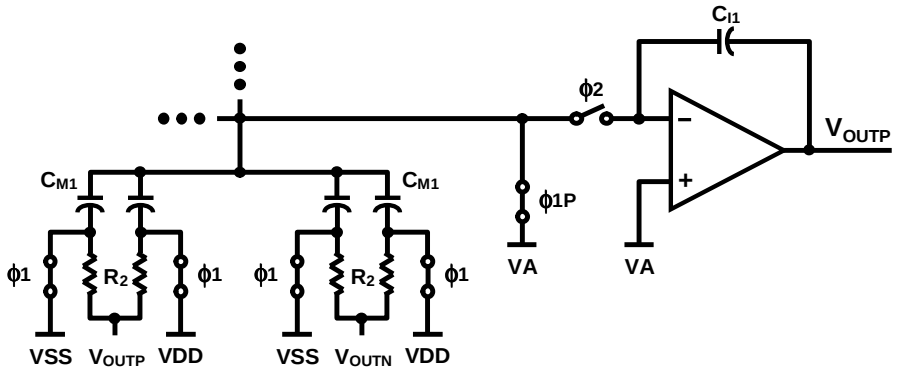
Figure 4.9: Schematic of pseudo-differential low-voltage integrator with switched-RC technique.

reference $V_{CM} = (VDD + VSS)/2$ is sampled onto capacitors C_{M1} by connecting half of them to VDD and the other half to VSS. During the following $\phi 2$ phase, the difference between V_{CM} and the actual output common-mode voltage is fed to all opamp inputs, and integrated in both pseudo-differential paths. This forces the output CM of all opamps to V_{CM}.

Fig. 4.11 shows the complete schematic of the first stage modulator, implemented in a pseudo-differential architecture. To insure less than -85 dB kT/C noise level, a total of 4.8 pF input sampling capacitance is used and $R_1 = 8$ kΩ is used to



(a)



(b)

Figure 4.10: Common-mode feedback with switched-RC technique. (a) $\phi 1$ phase. (b) $\phi 2$ phase.

guarantee linear input signal sampling. The 1.5-bit DAC needed for local feedback uses two capacitors C_{DAC2} to double the effective DAC reference voltage, each one acting as a 1-bit delay-free DAC. During the $\phi 2$ phase, each capacitor is charged to VDD or VSS. During the following $\phi 1$ phase, depending on the output (-1, 0 or 1) of the 1.5-bit local feedback quantizer, the voltage at the bottom plate of the C_{DAC2} capacitors will be changed. If output is "-1", then the capacitor earlier connected to VDD will be reconnected to VSS. If it is "1", then the capacitor

connected to VSS will be switched to VDD. However, if the quantizer output is "0", then the connection of the C_{DAC2} capacitors will not be changed.

The gain coefficients of the feed-forward paths from the ADC input and from the output nodes of each integrator to the quantizer input are realized simply by scaling the capacitors in the comparators, as shown in Fig. 4.12. The switched-RC output branches of the integrators are shared with the comparators' input sampling branches. Because of this, the input common-mode level of the comparators is also kept constant, together with the output CM level of the integrators. The output voltages V_{P21}, V_{P22}, V_{N21} and V_{N22} of the second integrator drive the second stage of the MASH directly.

4.3.3. Amplifier circuitry

To achieve high gain and large output swing, internally compensated two-stage amplifiers are used. Their circuit diagram is shown in Fig. 4.13. The amplifiers contain a folded-cascode first stage and a common-source second stage. Simulation result shows more than 60 dB SFDR with full scale output swing (0.8 Vpp fully differential) under 0.6 V supply voltage. Though this amplifier provides relatively modest linearity under low-supply voltage operation, its nonlinearity error is reduced by the architectural features of the modulator, as explained in Section 4.2. The main performance parameters of the opamp are given in Table 4.1.

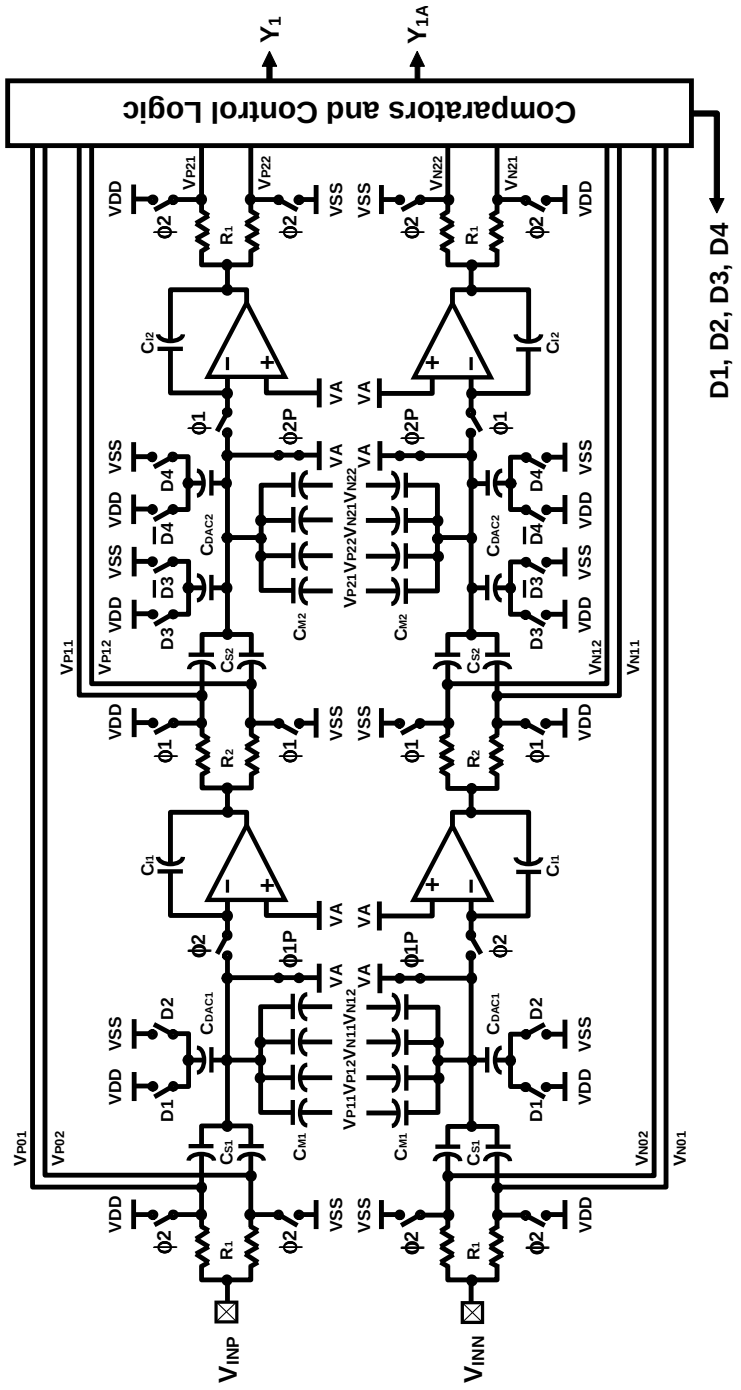


Figure 4.11: Schematic of the first stage delta-sigma modulator.

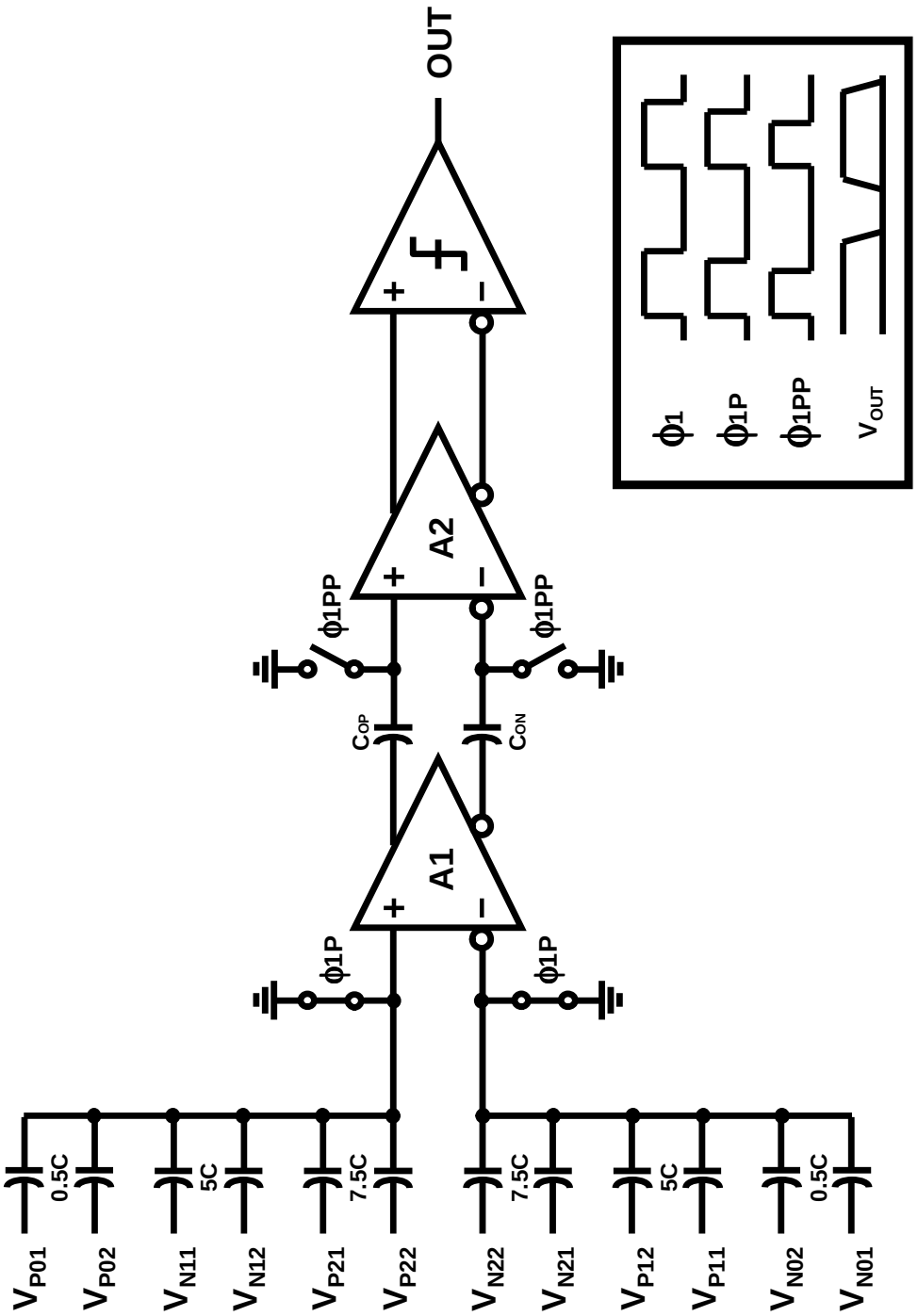


Figure 4.12: Schematic of the comparator.

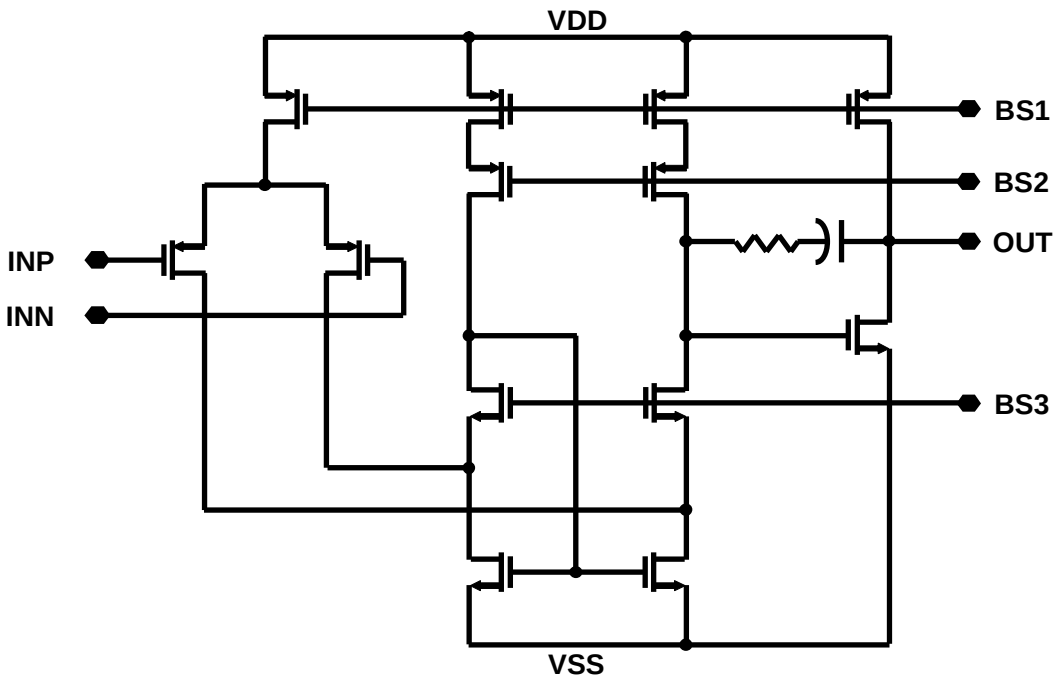


Figure 4.13: Schematic of the amplifier.

Table 4.1: Simulated performance of the amplifier.

Power supply voltage	0.6 V
DC gain	60 dB
Unity gain frequency	10 MHz
Phase margin	65 °
Slew rate	10 V/μs

4.3.4. Comparator

Using a low-offset comparator is important to achieve a large signal range in low-voltage delta-sigma modulator design. Depending on the comparator offset,

the center of the integrator output histogram can move out from the middle of the supply voltage range, resulting in overloading. Fig. 4.12 shows the schematic of the low-voltage comparator. The offset cancellation of the comparators is performed at the output of amplifier $A1$, while amplifier $A2$ is used as a preamplifier, to suppress the kickback from the latch. Amplifier $A2$ also provides a level shifting function for the proper input common-mode voltage of the latch.

4.4. Experimental Results

The prototype ADC was fabricated in a 0.35 μm CMOS technology, with double-poly and triple-metal layers. Fig. 4.14 shows the die photograph of the prototype IC. The core area, excluding bonding pads, is $1.8\times1.6\text{mm}^2$. Fig. 4.15 shows the measured power spectrum of the output for a 1 kHz, 0.57 V peak-to-peak differential input sine wave, with a 0.6 V power supply. 79 dB SNDR and 103 dB SFDR was achieved over the audio band, largely due to the proposed switched-RC technique and the low-distortion loop. The SNDR versus input amplitude curve is illustrated in Fig. 4.16. This result indicates linear operation, up to a -1 dBFS input level. The measured performance is summarized in Table 4.2. In the A-weighted audio band, the prototype achieved 81 dB peak SNDR and 82 dB dynamic range with a 0.6 V supply voltage and 1 mW power consumption. 3.072 MHz clock frequency was used, resulting in an OSR of 64. Fig. 4.17 shows the SFDR and SNDR versus power supply voltage curves (signal reference/swing fixed). The performance is unaffected by the variation of the supply voltage from 0.6 V to 1.8 V. Table 4.2 summarizes the performance of the converter.

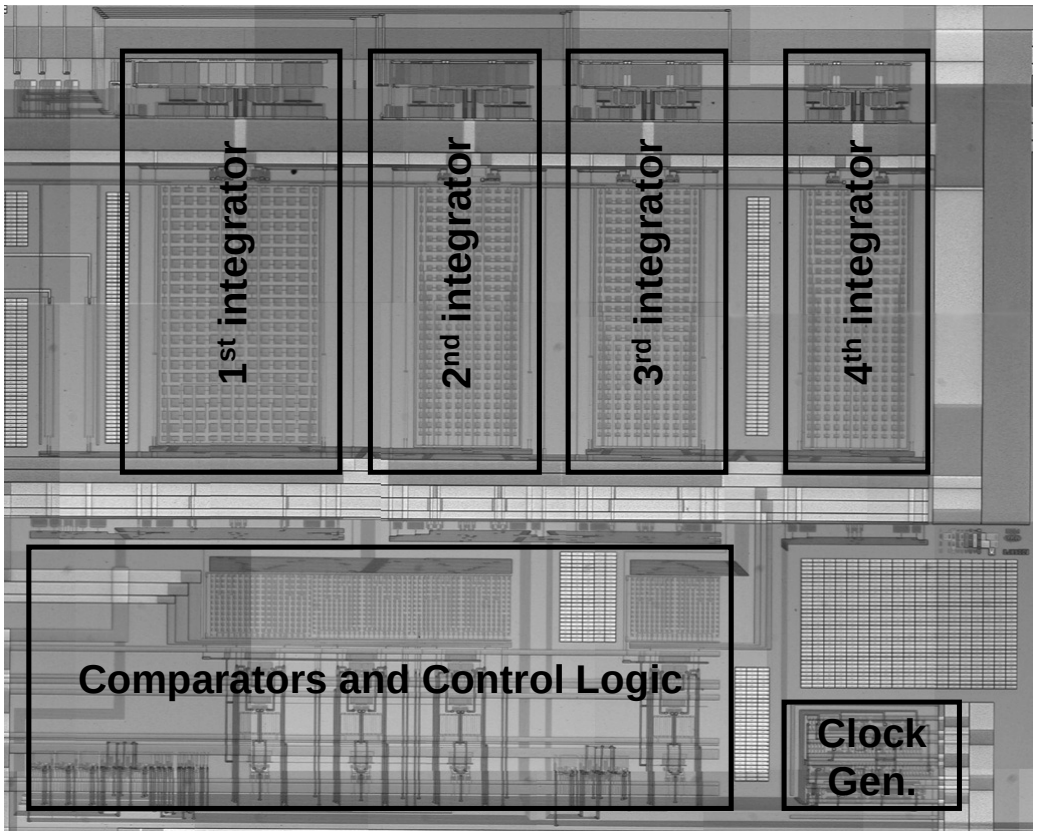


Figure 4.14: Die photograph.

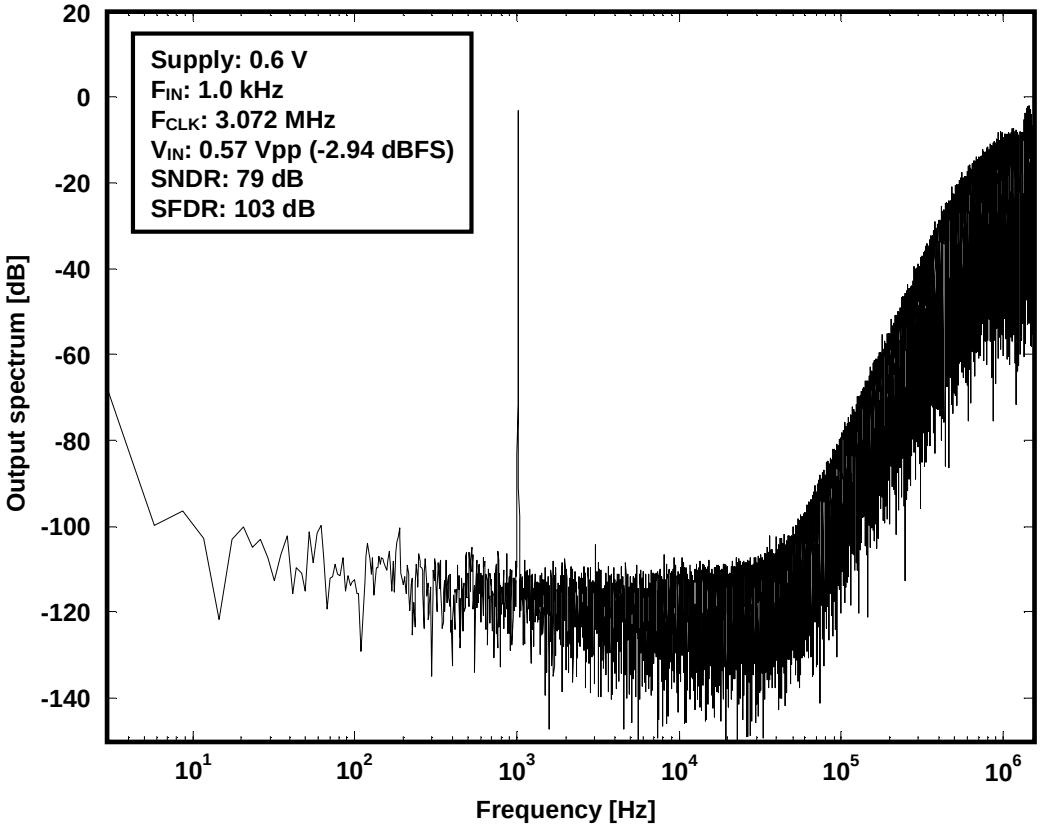


Figure 4.15: Measured output spectrum.

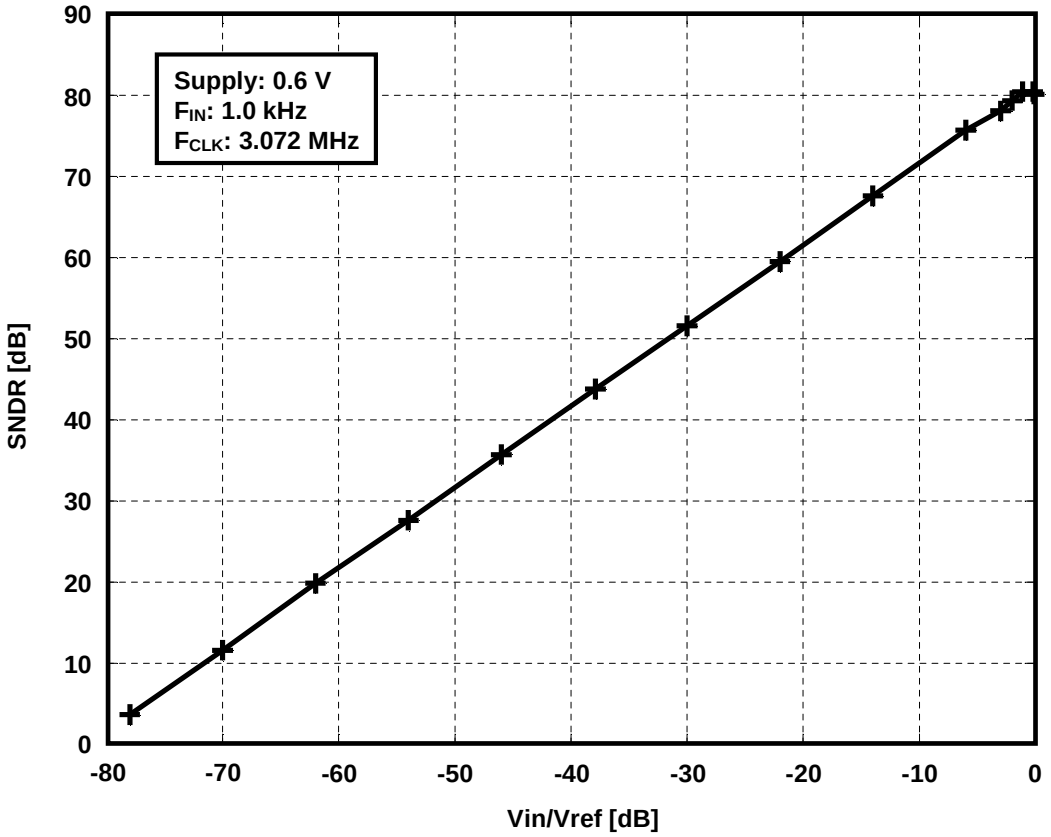


Figure 4.16: Measured SNDR.

Table 4.2: Performance summary of $\Delta\Sigma$ ADC.

Power supply voltage	**0.6 V**
Signal bandwidth	**24 kHz**
Clock frequency	**3.072 MHz**
Oversampling ratio	**64**
Total power consumption	**1 mW (including digital and I/O)**
Input range	**0.8 Vpp (differential)**
Peak SNR	**77 dB @ BW = 24 kHz** **78 dB @ BW = 20 kHz** **81 dB @ BW = 20 kHz, A-weighted**
Peak SNDR	**77 dB @ BW = 24 kHz** **78 dB @ BW = 20 kHz** **81 dB @ BW = 20 kHz, A-weighted**
Dynamic range	**78 dB @ BW = 24 kHz** **79 dB @ BW = 20 kHz** **82 dB @ BW = 20 kHz, A-weighted**
Active die area	**1.8 X 1.6 mm^2**
Technology	**0.35 µm CMOS (V_{TN}=0.34 V, V_{TP}=-0.31 V)**

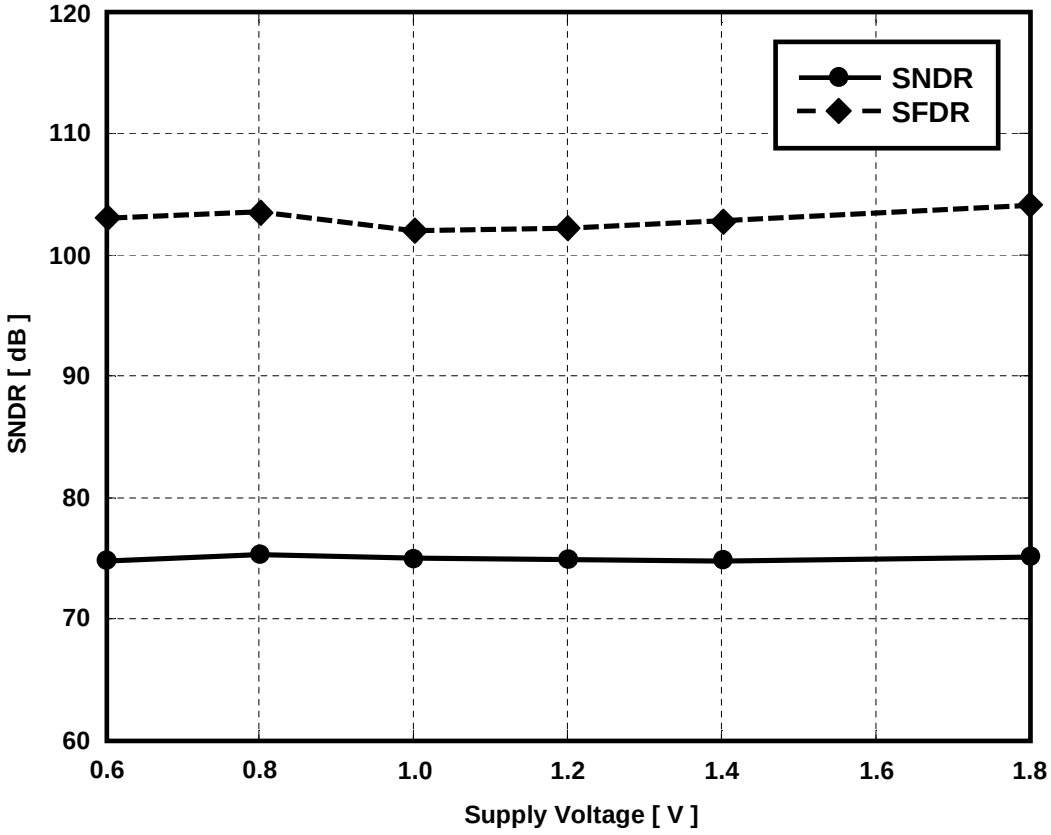


Figure 4.17: SNDR and SFDR vs. supply voltage.

CHAPTER 5. 0.9 V 10-BIT 20 MS/S CMOS PIPELINED ADC

The switched-RC technique used in the implementation of the low-voltage integrator can also be extended to several other low-voltage circuit blocks. In this chapter the design of low-voltage pipelined ADC using the switched-RC technique is described. Circuit design techniques for building switched-RC multiplying digital-to-analog converter (MDAC) circuit are presented. To demonstrate the proposed techniques, a 10-bit 20 MS/s pipelined ADC operating with 0.9 V supply and 10 mW power consumption was designed in a 0.13 μm CMOS process.

5.1. Fundamentals of Pipelined ADC

Pipelined ADC architecture offers the best trade-off between conversion rate, resolution, power consumption and chip size for the implementation of video-rate ADCs. Fig. 5.1 shows a conventional pipelined ADC architecture. It consists of cascaded stages that resolve $n_k - bit$. Input signal of each stage is sampled by the sample-and-hold (S/H) block and the held signal is quantized by the $n_k - bit$ sub-ADC. The multiplying digital-to-analog converter (MDAC) generates the residue by amplifying the quantization error of the sub-ADC by an appropriate gain. The residue voltage generated by the k-th stage V_{RESk} given by eq. 5.1:

$$V_{RESk} = 2^{n_k-1} \left(V_i - V_{DAC}(D_k)\right) , \tag{5.1}$$

where n_k is the number of output bits from k-th stage, D_k is the sub-ADC output of k-th stage and $V_{DAC}(D_k)$ is the sub-DAC output. This architecture enables the implementation of high-resolution, high-throughput ADC with low-power consumption and small area. This benefit is mainly attributed to the fact that the number of stages in the pipeline only grow linearly with bit resolution. Furthermore, the relaxed accuracy requirement of the sub-ADC enables the use of low-power comparators. However, to achieve high linearity, accurate interstage gain is required. To satisfy this condition, high-gain opamp and good capacitor matching should be guaranteed.

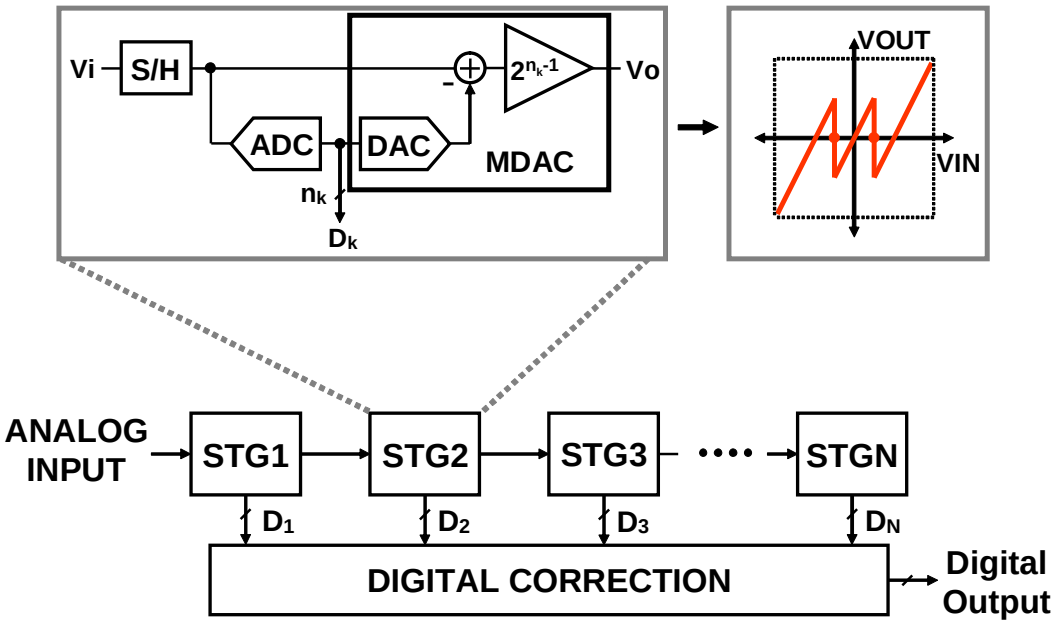


Figure 5.1: A conventional pipelined ADC architecture.

5.2. Architecture

The block diagram of the implemented 10-bit pipeline ADC is shown in Fig. 5.2. It consists of a cascade of nine 1.5-bit stages. The sub-ADC in each stage is composed of full flash type ADC with two comparators. Fig. 5.3 shows input (V_{IN}) and residue output (V_{RES}) relations of each stage.

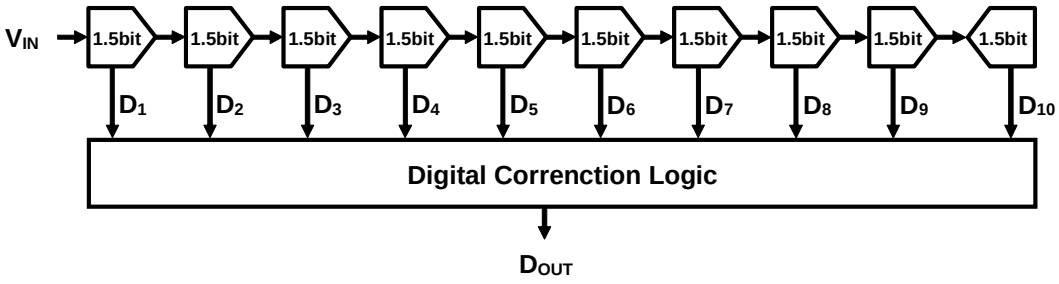


Figure 5.2: A 1.5-bit-per-stage pipelined ADC architecture.

This residue generation is expressed mathematically by the following equation.

$$\begin{aligned} V_{RES} &= 2V_{in} - V_{REF} \text{ if } V_{in} > \frac{1}{4}V_{REF} \\ &= 2V_{in} + V_{REF} \text{ if } V_{in} < -\frac{1}{4}V_{REF} \\ &= 2V_{in} \text{ otherwise} \end{aligned} \tag{5.2}$$

To determine the optimal number of bits resolved in each stage is a difficult optimization problem [21][22]. Typically a multi-bit first stage results in lower power consumption and also eases the matching and amplifier gain requirements of the following stages. However the implementation of multi-bit stage poses two major challenges. First, lower feedback factor limits the maximum sampling frequency

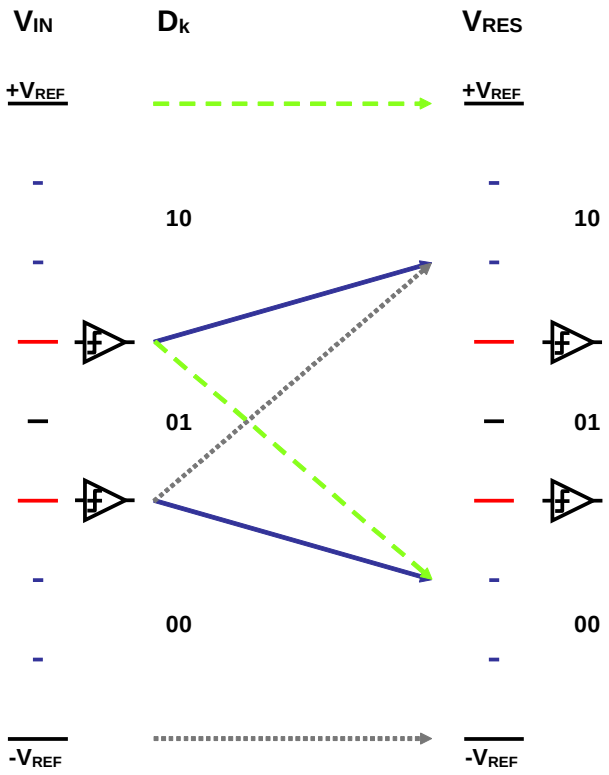


Figure 5.3: The residue transfer function of 1.5-bit stage.

to low-to-mid rates. Secondly, and more importantly, multi-bit DAC requires several floating switches. As mentioned earlier, these floating switches are a serious impediment to the design of low-voltage SC circuits. Due to this reason a conventional 1.5-bit stage was employed. Switched-RC technique was employed in the design of the multiplying digital-to-analog converter (MDAC) to obviate the need for floating switches.

5.3. Circuit Implementation

In this section, the circuit implementation details of all the building blocks of the pipelined ADC will be described. Switched-RC technique to design the low-voltage MDAC will be explained. And, the low-voltage amplifier design technique for the fully differential circuit implementation will be presented.

5.3.1. MDAC

Fig. 5.4 shows a schematic of conventional 1.5-bit MDAC with flip-over capacitor. The operation of this circuit is as follows. During $\phi 1$ phase, the input signal is sampled on both C_S capacitors. During the following $\phi 2$ phase, bottom plate of one capacitor is connected the amplifier output and the other capacitor is connected to $\pm V_{REF}$ or 0 depending on the sub-ADC output. Larger feedback factor of this topology results in faster operation with the same open-loop amplifier bandwidth. In this circuit implementation, three floating switches are required which are connected to input (V_{IN}) and output (V_{OUT}). However, under the low-voltage supply, it is hard to use floating switch as explained in chapter 2. Recall that the floating switch at the input of the conventional integrator was replaced by a passive resistor in the low-voltage integrator(see Fig. 4.8). In the integrator, no extra switch is required for the feedback capacitor C_I. The major difference between the integrator and the MDAC is the resetting of the feedback capacitor. In Fig. 5.4, flipped-over feedback capacitor is automatically reset during $\phi 1$ phase by sampling the input on this capacitor.

The operation of the proposed low-voltage sample-and-hold circuit will be

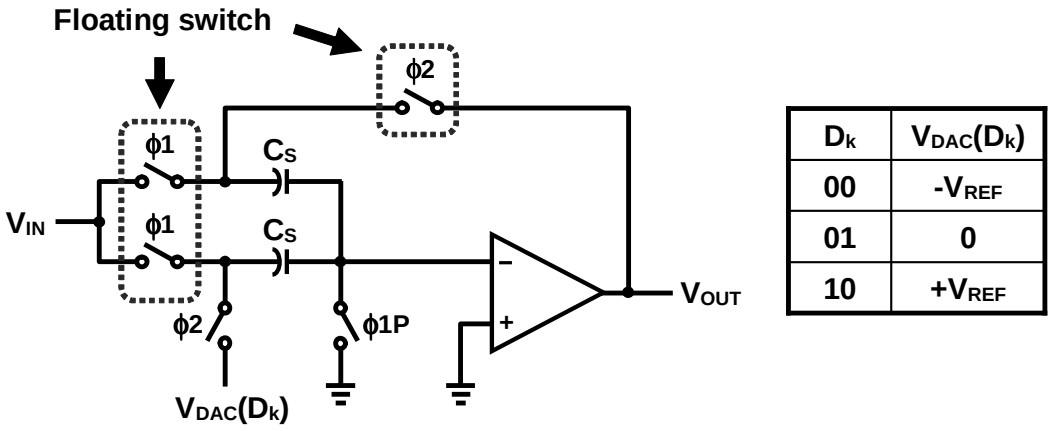
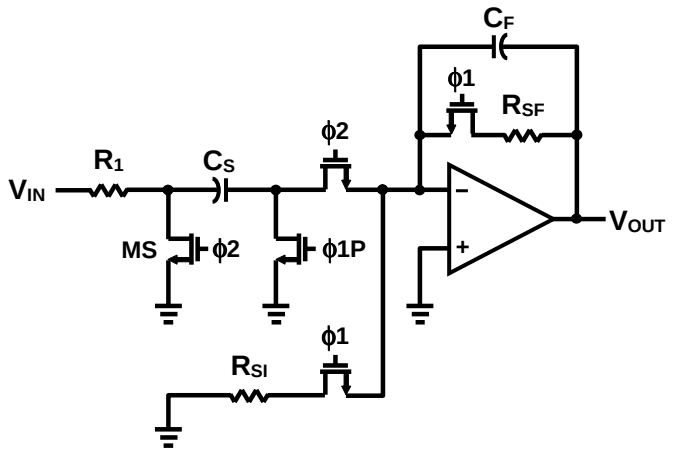


Figure 5.4: A schematic of conventional 1.5-bit MDAC.

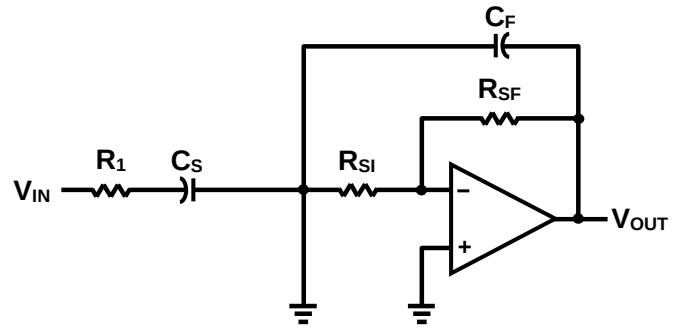
first described and these design principles will be extended to the design of low-voltage MDAC later. Fig. 5.5 shows a schematic of the switched-RC sample-and-hold circuit with resistive feedback reset technique. For the low-voltage operation, the switched-RC input branch was employed. To avoid the use of floating switch at the output of the amplifier, separate capacitors for the input sampling path and the feedback path were used. During $\phi 1$ phase, the input signal is sampled into the capacitor C_S through the resistor R_1. At the same time, feedback capacitor C_F is reset by connecting the its top plate to ground and the bottom plate to output common-mode level of amplifier. This output common-mode level is provided through the resistive feedback configuration with R_{SI} and R_{SF}. During the following $\phi 2$ phase, the signal charge in the C_S is transferred to the feedback capacitor C_F in the same way as in the switched-RC integrator.

In the pipelined ADC architecture, the interstage gain accuracy is a very important requirement to achieve high linearity. However, as explained in Chapter 3, the on-resistance of reset switch causes inaccurate interstage gain. To attenu-



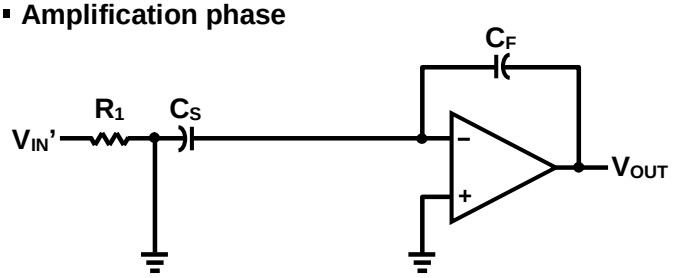
(a)

▪ **Sampling phase**



(b)

▪ **Amplification phase**



(c)

Figure 5.5: (a) A schematic of the switched-RC sample-and-hold circuit. (b) Sampling phase. (c) Hold phase.

ate this gain error, the cascaded switched-RC branches shown as in Fig. 5.6 was used for the implementation of first stage MDAC [23]. Separate DAC capacitors (C_{DAC1}) were used to avoid the floating switch.

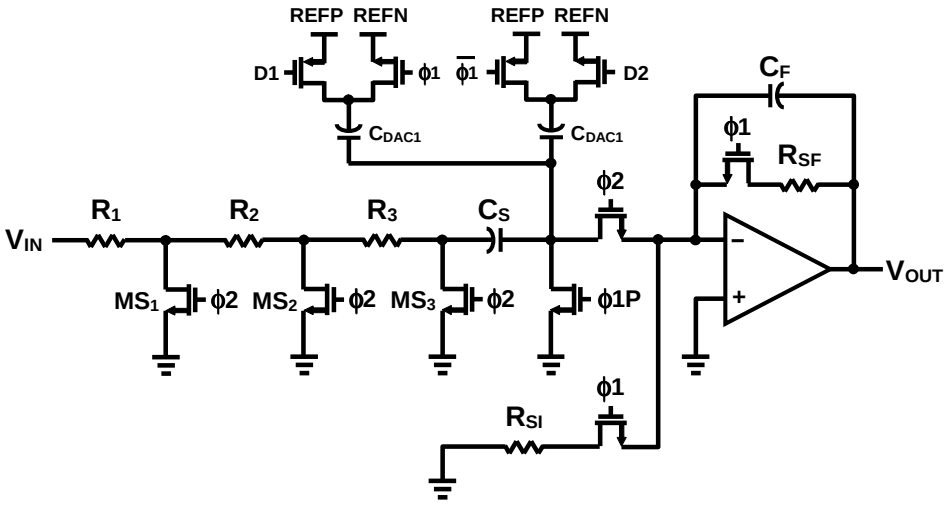


Figure 5.6: A schematic of the cascaded switched-RC MDAC.

Fig. 5.7(a) shows the schematic of low-voltage fully-differential switched-RC multiplying digital-to-analog converter with the resistive reset technique. To align the beginning of amplification phase different clock phase generated by Fig. 5.7(b) was used. Resistor values for R_{SI} and R_{SF} were chosen to bias the output common-mode and the amplifier virtual ground as shown in eq. 5.3:

$$VA = \frac{R_{SI}}{R_{SI} + R_{SF}}(V_{CMO} - VSS)\,, \tag{5.3}$$

where VA is the bias voltage for the amplifier virtual ground node and $V_{CMO} = (VDD + VSS)/2$ is the output common-mode level of the amplifier. Unlike switched-opamp (SO) and opamp-reset technique (ORST) which have different output common-mode level for each phase, the proposed resistive reset technique maintains constant output common-mode level during both phases. This feature

eases the design of common-mode feedback amplifier for fully differential implementation.

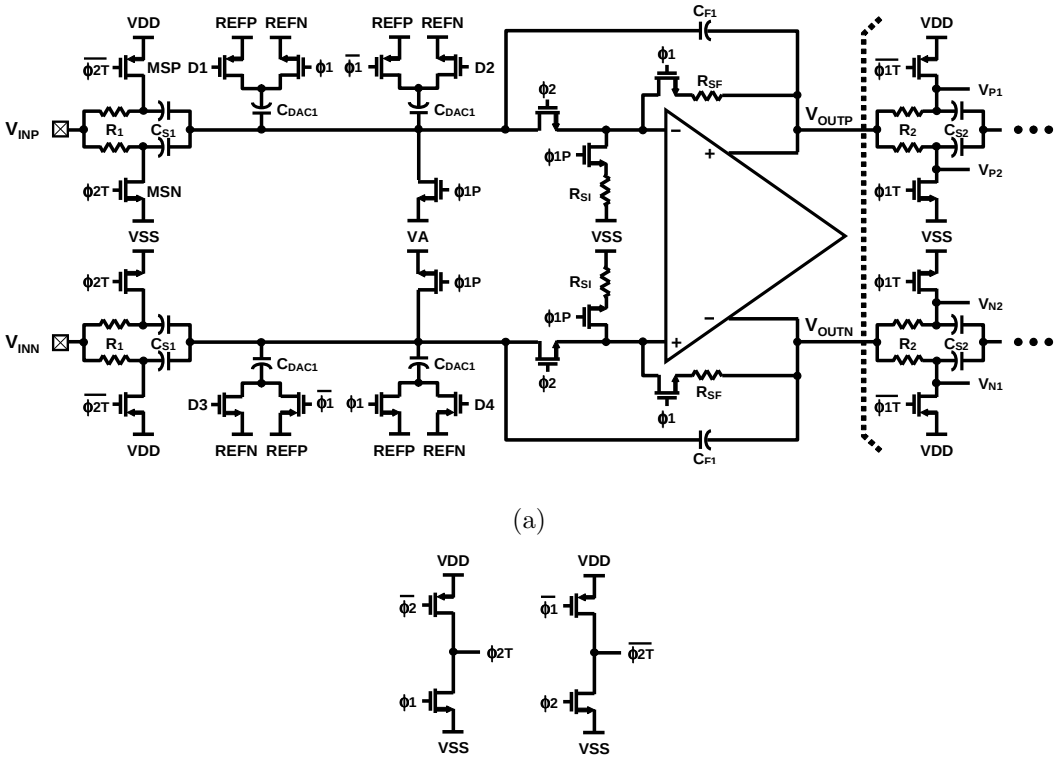


Figure 5.7: (a) A schematic of the low-voltage fully-differential switched-RC MDAC. (b) Clock generator for resetting.

5.3.2. Amplifier circuitry

The circuit diagram of the amplifier is shown in Fig. 5.8. Internally compensated two-stage fully-differential amplifier was used to achieve high gain and large output swing under low-voltage supply. The main difficulty in building a fully-differential low-voltage amplifier is the design of common-mode feedback (CMFB)

circuit. For the maximum output swing, typically $(VDD + VSS)/2$ is used as a output common-mode level. However, under low supply voltage, this output common-mode level cannot be directly fed to the input of CMFB amplifier due to its limited input common-mode range. To adjust proper input common-mode voltage for the common-mode feedback amplifier XA, the level shifting block consisting of resistor R_C and current source MC1, MC2 [24] was used. The output common-mode level of the main amplifier was shifted by the voltage drop across these resistors.

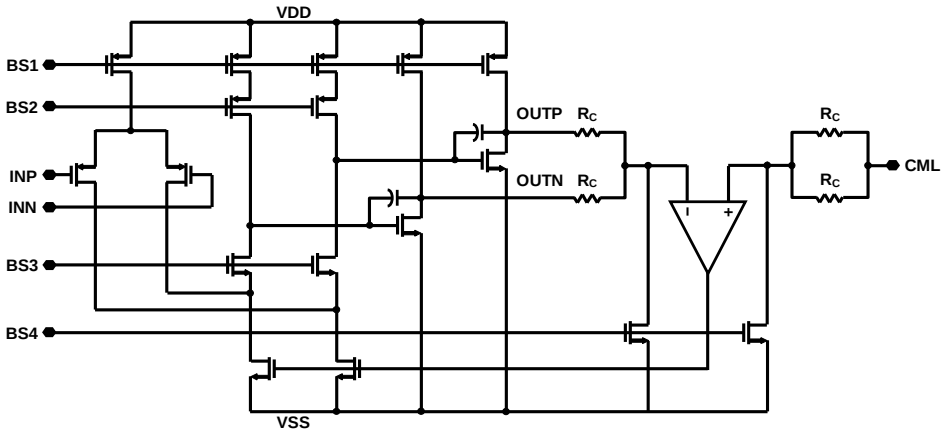


Figure 5.8: Fully-differential low-voltage opamp with CMFB.

5.3.3. Sub-ADC

Two comparators were required to implement the 1.5 bit sub-ADC. Threshold levels for each comparator are $\pm 1/4 V_{REF}$. Schematic of the comparator is shown in Fig. 5.9. Instead of sharing the resistor for input branch with MDAC, each sub-ADC block has its own resistor and switch for switched-RC sampling branch to reduce the coupled noise from comparator to MDAC input. It also uses

two preamps to cancel out offset and prevent kick-back noise from latch. Second amplifier A2 also provides level shifting function by using passive resistor with proper bias current. The common-mode level of the following latch input is set to $1/2I_{BIAS}R_L$ where I_{BIAS} is the bias current of the second amplifier A2.

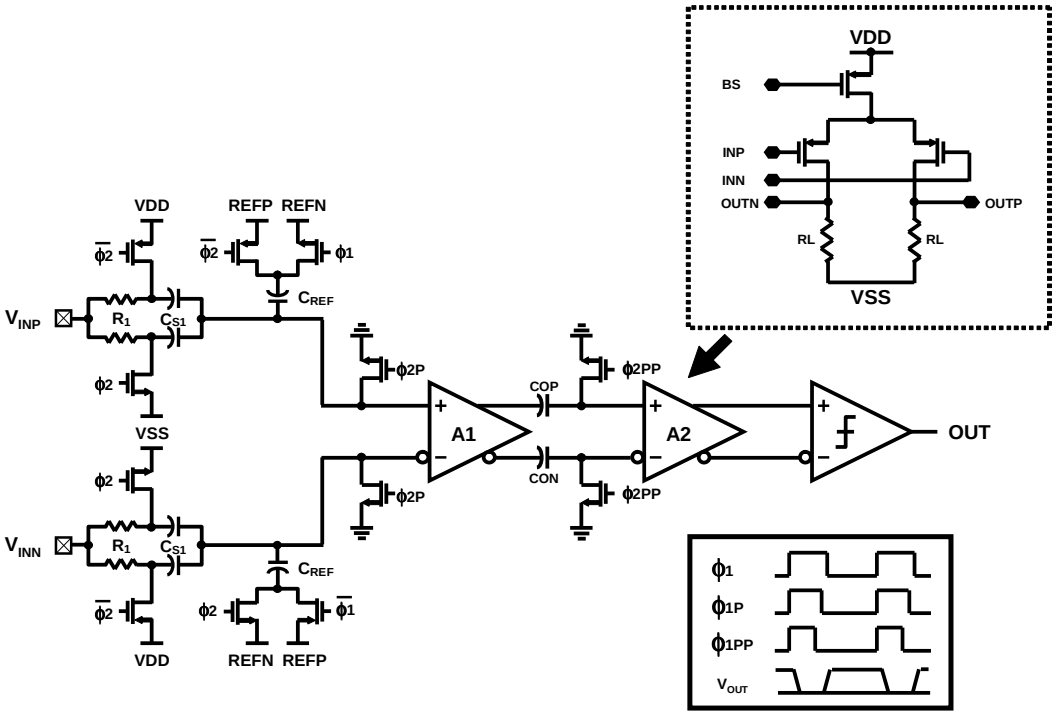


Figure 5.9: The schematic of the low-voltage comparator.

5.4. Simulation Results

The prototype 11-bit pipelined ADC was designed in 0.13 μm CMOS technology, and occupies $1.6 \times 1.2\text{mm}^2$ active die area. Fig. 5.10 shows the output spectrum of the transistor level simulation of the low-voltage pipelined ADC. This ADC achienves 66 dB signal-to-quantization-noise ratio (SQNR) with a 8.8 MHz

input sine wave at 20 MHz sampling frequency. The power consumption with 0.9 V supply is 10 mW. Fig. 5.11 shows the layout of the prototype ADC.

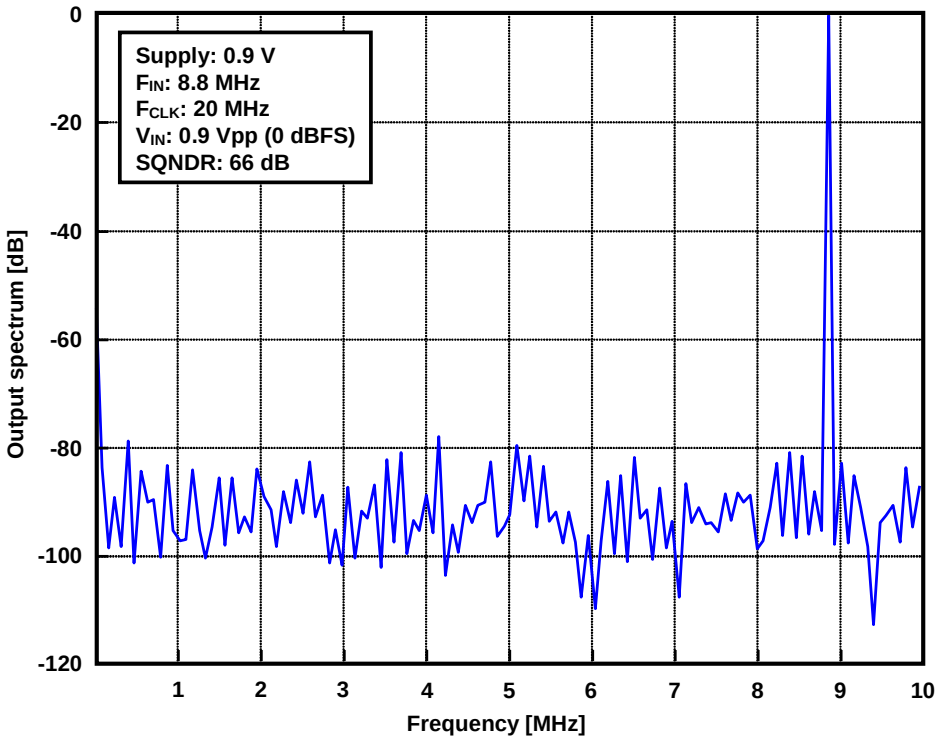


Figure 5.10: Simulated output spectrum of the prototype 11-bit ADC.

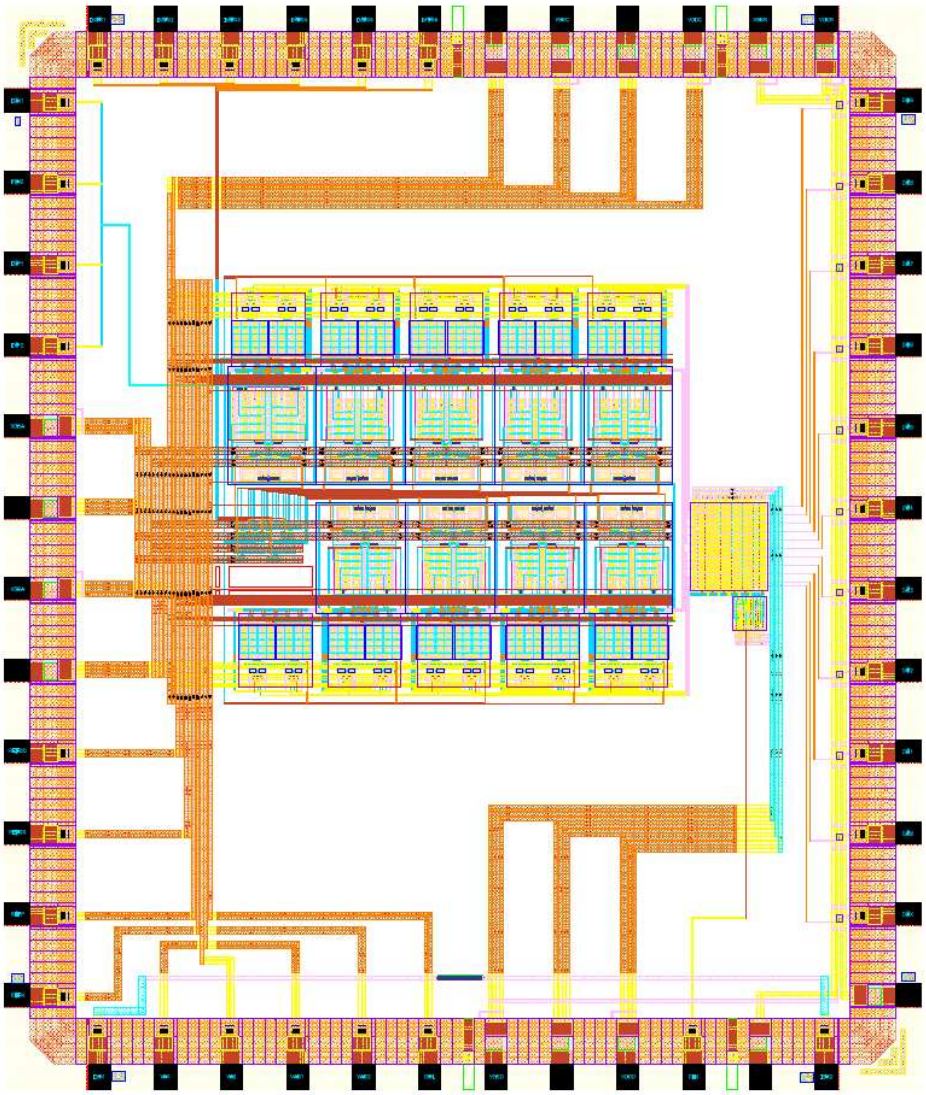


Figure 5.11: Layout of the prototype pipelined ADC.

CHAPTER 6. 2.4 V 12-BIT 10 MS/S CMOS PIPELINED ADC

The demand for portable applications such as wireless communications and multimedia consumer electronics, combined with the growing trend of performing all signal processing in the digital domain, created a need for high-resolution analog-to-digital converters (ADCs). At the same time, the need for low-power consumption becomes more important to achieve longer battery life. Pipelined ADC architecture offers the best trade-off between speed and power, and is therefore a popular choice for implementing wireless and video front-ends. In the traditional pipelined ADC design, high DC gain amplifier is required to achieve accurate closed loop gain of the inter-stage multiplying digital-to-analog converter (MDAC). Multi-stage topology [25] [26] or gain boosting [27] are the best-known techniques to achieve high amplifier gain. However, both these methods require large power consumption, and their performance is ultimately limited by the gain-bandwidth product of the process. In this Chapter, a new architecture is proposed to implement high-resolution ADC with a low-gain amplifier. To verify the proposed architecture, a 12b 10MS/s pipelined ADC was designed.

6.1. Architecture

6.1.1. Pipeline architecture

The pipelined ADC architecture employing the proposed reference scaling technique is shown in Fig. 6.1. It consists of a 2.5-bit first stage followed by eight 1.5-bit stages and is terminated by a 2-bit flash ADC. Similar to a conventional pipelined ADC, each stage resolves a fixed number of bits depending on the stage resolution, and passes on the amplified quantization error (residue) to the following stage. The linearity of this pipelined architecture is limited by the transfer gain accuracy of each stage. Inter-stage gain error during the residue amplification phase causes nonlinear transfer characteristics for the over-all ADC. In the proposed architecture, the reference voltage is also propagated through the stages to introduce the same gain error as the residue. By applying the same gain to both reference and signal, the interstage gain error is cancelled.

6.1.2. Reference scaling techniuqe

The two main sources of inter-stage gain error are capacitor mismatch and finite opamp gain. Since modern fine-line CMOS processes provide accurate matching up to 14 bits [25], only the gain error caused by low opamp gain is addressed in this design. The fundamental idea behind the proposed architecture arises from the following observation. In a conventional MDAC, the transfer gain accuracy is inversely proportional to the opamp gain. So by introducing the same gain error into the reference voltage, the distortion caused by the finite opamp gain can

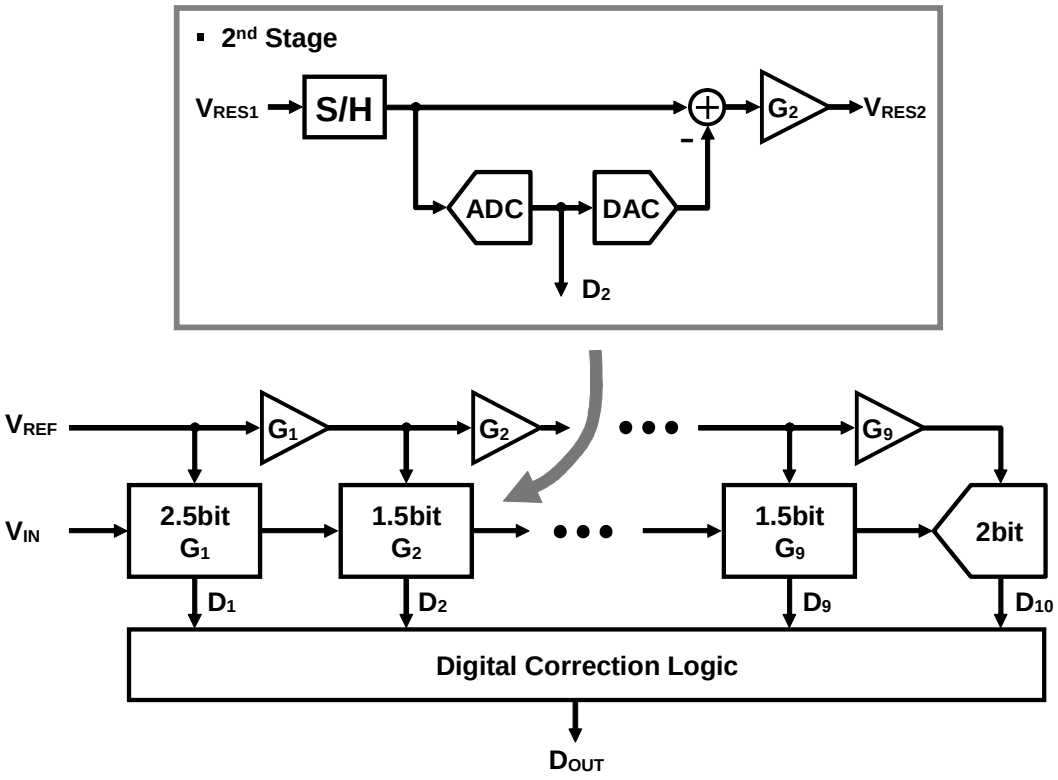


Figure 6.1: Block diagram of the proposed ADC architecture.

ideally be cancelled. As shown in Fig. 6.2, the gain error is introduced into the reference by utilizing an additional capacitor array and sharing the same opamp. During the residue amplification phase of the first stage, the capacitor array of C_{R1}s samples the reference input V_{REF}. At the same time, the following stage MDAC and the comparator sample the residue output onto capacitors C_{S2} and C_{L2} respectively. During the following phase, the sampled reference is amplified by the same opamp and feedback factor, to reproduce the same transfer gain error. This scaled reference is then fed to the following MDAC stage. The output voltage

of the MDAC for each phase can be found from charge conservation as:

$$V_{RES1} = \frac{1}{1+\frac{4}{A1}} \left(4V_{IN} - \sum_{k=0}^{2} D_k \cdot V_{REF} \right) , \tag{6.1}$$

$$V_{REF1} = \frac{1}{1+\frac{4}{A1}} V_{REF} . \tag{6.2}$$

Note that this technique enables the use of MDAC with a low-gain amplifier for building a high resolution ADC, as long as the gain of the amplifier is the same during both phases. As a result of this relaxed gain requirement, a simple single stage amplifier with an open loop gain of 45dB is employed in this design.

6.2. Circuit Implementation

6.2.1. MDAC

Fig. 6.3 shows the schematic of the fully differential 2.5-bit MDAC employed in the first stage. Two capacitor arrays, denoted by capacitors C_{R1} and C_{S1}, are used for sampling the reference and signal, respectively. The seven-level DAC was implemented with six capacitors connected to either $+V_{REF}$ or $-V_{REF}$ based on the sub-ADC output. One of the critical issues of the switched capacitor circuit using low-gain amplifier is the memory effect. The stored charge on the parasitic capacitor of the virtual ground node varies with the output signal, and causes harmonic distortion. To reduce this distortion, the input and the output of the amplifier are reset between the two clock phases, using the ϕ_R clock.

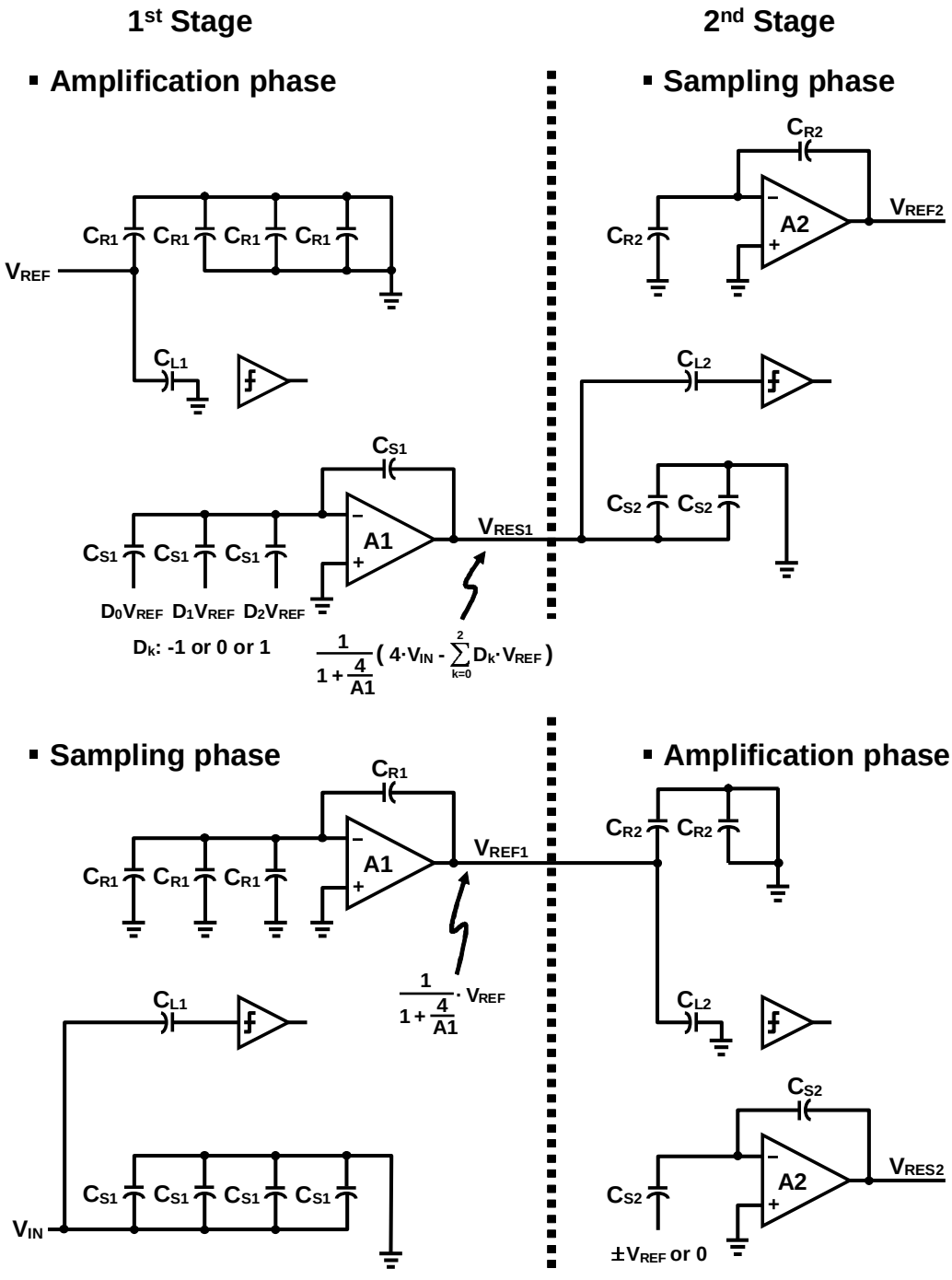


Figure 6.2: MDAC operation with the proposed reference scaling technique.

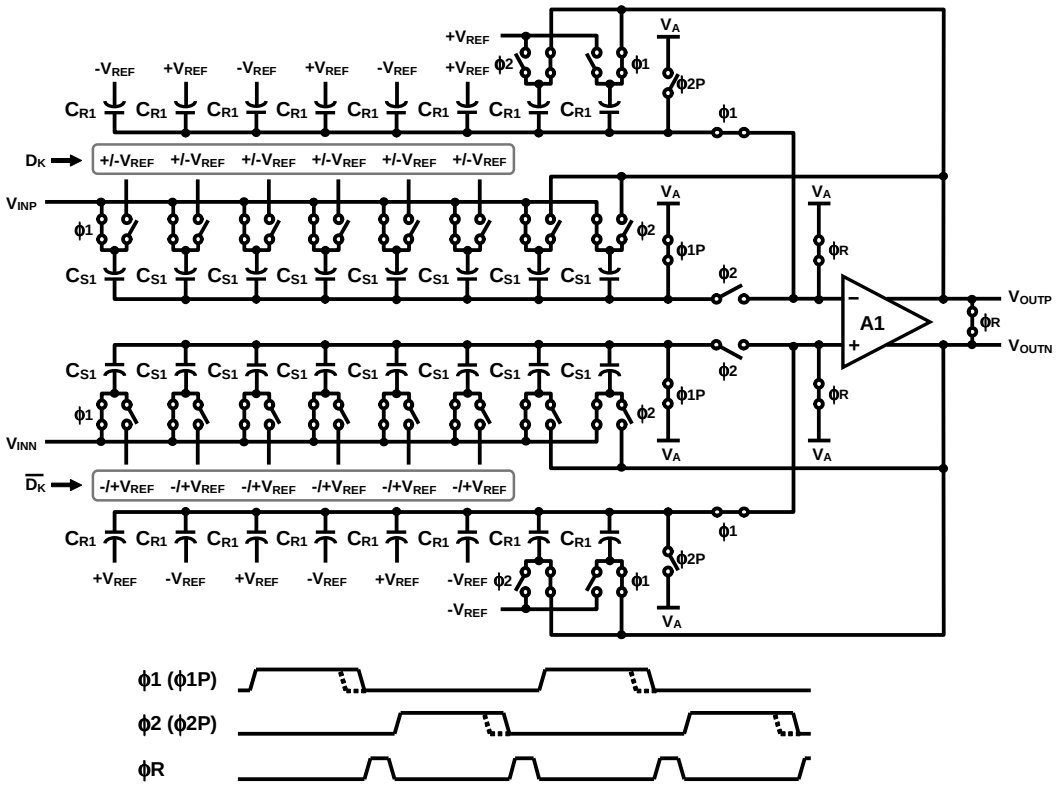


Figure 6.3: Schematic of the first stage MDAC.

6.2.2. Amplifier circuitry

In the conventional pipelined architecture, the effect of amplifier offset in the MDAC is mitigated by employing digital redundancy. However, in the proposed reference scaling scheme, the offset voltage of the opamp is amplified during the reference amplifying phase, and manifests itself as inter-stage gain error.

Fig. 6.4 shows the scaled reference output with amplifier offset and resulted interstage gain error is given as eq. 6.3.

$$\text{Interstage Gain Error} = \frac{\frac{1}{1+\frac{4}{A1}}(V_{REF}+4V_{OS})}{\frac{1}{1+\frac{4}{A1}}V_{REF}} = 1+\frac{4V_{OS}}{V_{REF}}. \tag{6.3}$$

To attenuate this gain error, the offset of the first MDAC stage was cancelled, by trimming the output current of the amplifier as shown in Fig. 6.5. However, measured results indicate that the linearity of the ADC can be further improved by cancelling the amplifier offset in second and third stages as well.

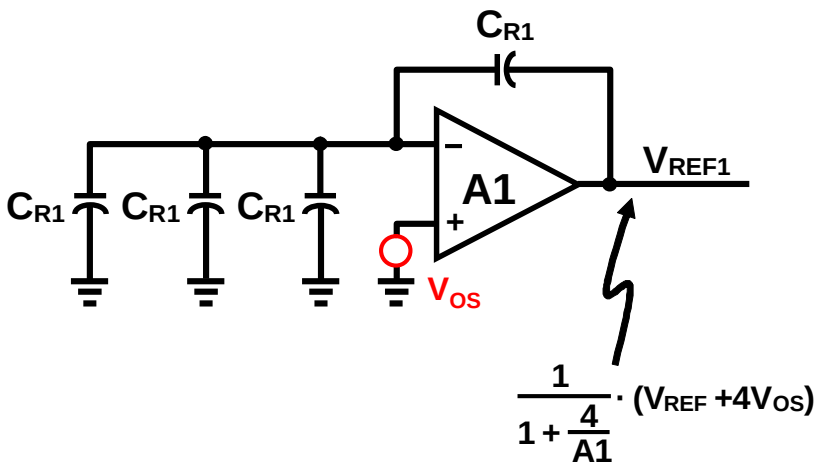


Figure 6.4: Scaled reference output with amplifier offset.

6.2.3. Comparator

Fig. 6.6 shows the schematic of comparator used for the first stage sub-ADC. Preamplifier was used to suppress the kickback from the latch as well as to amplify the input signal. In the first stage comparator, sampling capacitor C_S is switching between the signal input port and the reference input port. However, from the second stage, signal and reference come from the same previous output node. So, comparator input switching network was modified as shown in Fig. 6.7. During the $\phi 2$ phase it samples scaled reference voltage. While this phase, 3/4 of the sampling

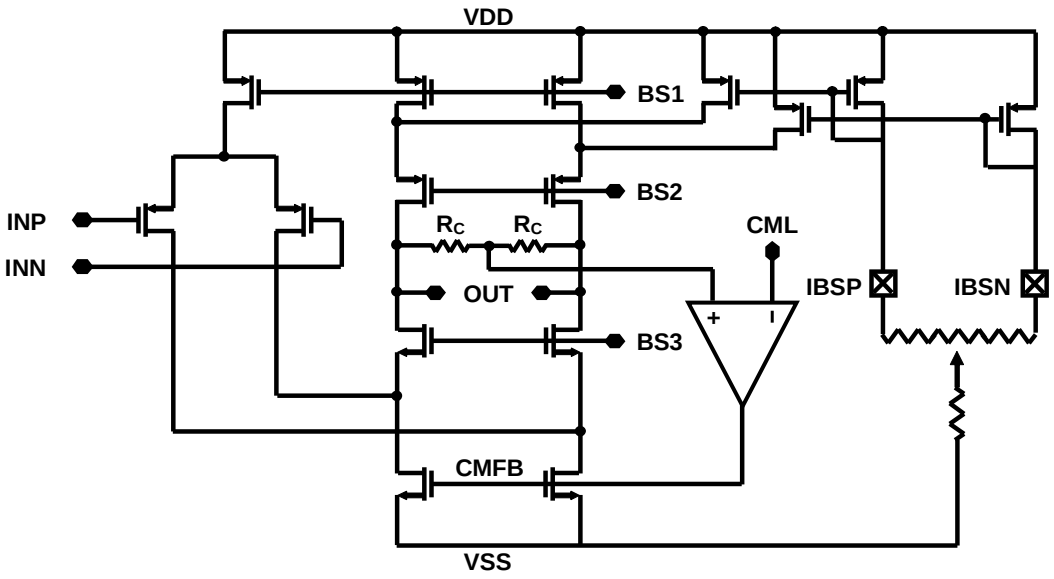


Figure 6.5: Schematic of the first stage opamp.

capacitor is connected to the common-mode level to create $1/4V_{REF}$ threshold level for the 1.5-bit sub-ADC.

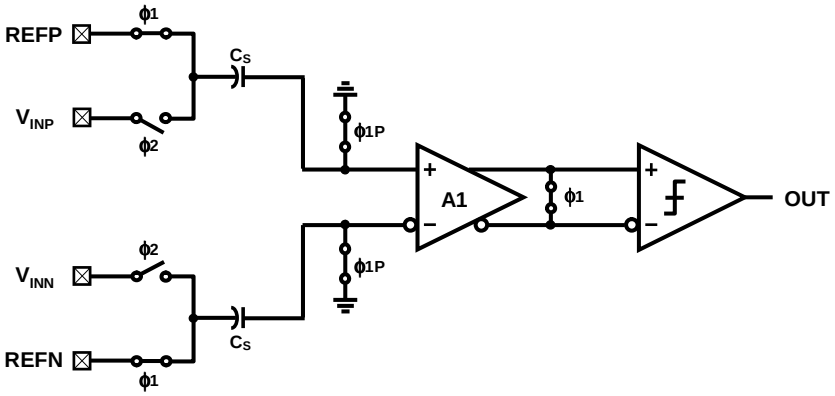


Figure 6.6: Schematic of the comparator for the first stage sub-ADC.

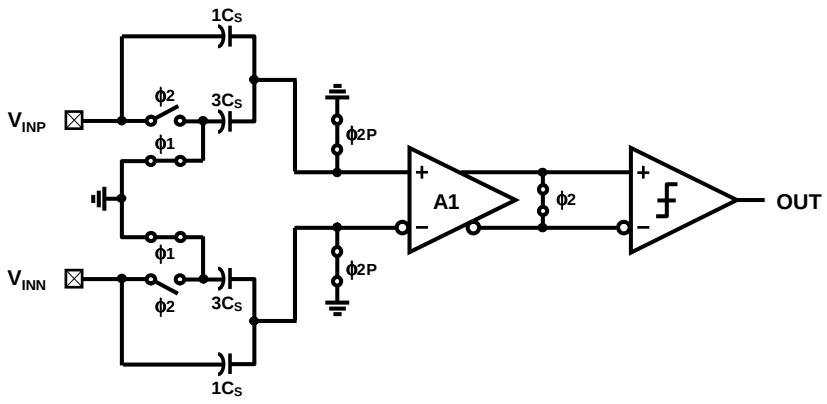


Figure 6.7: Schematic of the comparator for the remaining (2∼9) stages sub-ADC.

6.3. Experimental Results

The prototype 12-bit pipelined ADC was fabricated in 0.35 μm CMOS technology, and occupies 2.2 × 2.4 mm^2 active die area. Fig. 6.8 shows the measured DNL and INL of the ADC. The DNL is +0.52/-0.7 LSB, and the INL is +2.3/-3.1 LSB. Fig. 6.9 shows the measured power spectrum of the output for a 1MHz, 1.1V peak-to-peak differential sine wave input using a 10MHz sampling frequency. The achieved SNDR is 62dB, and the SFDR is 72dB. For a 5MHz input sine wave, the SNDR and SFDR reduces to 57dB and 68dB. The power consumption with 2.4V supply is 14mW for the analog section, and 5mW for comparators and the digital section. The performance is summarized in Table 6.1, and the die photograph is shown in Fig. 6.10.

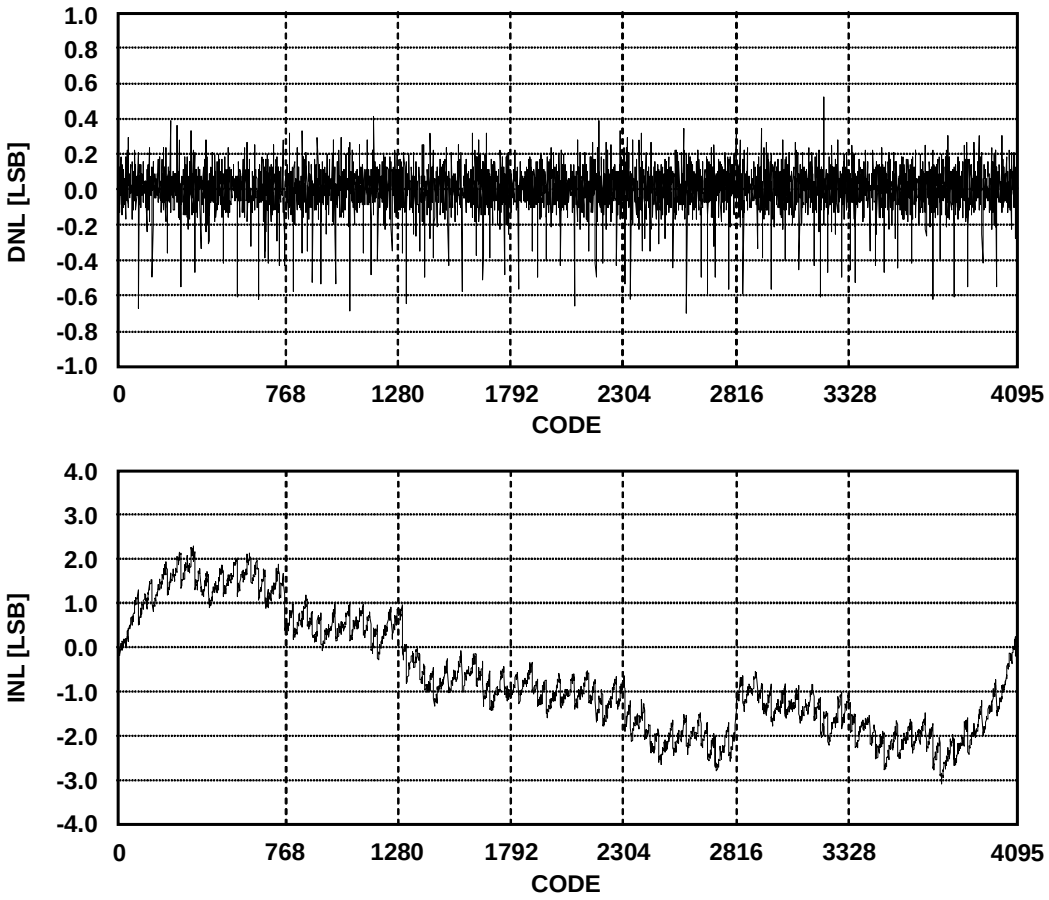


Figure 6.8: Measured DNL and INL of the prototype pipelined ADC.

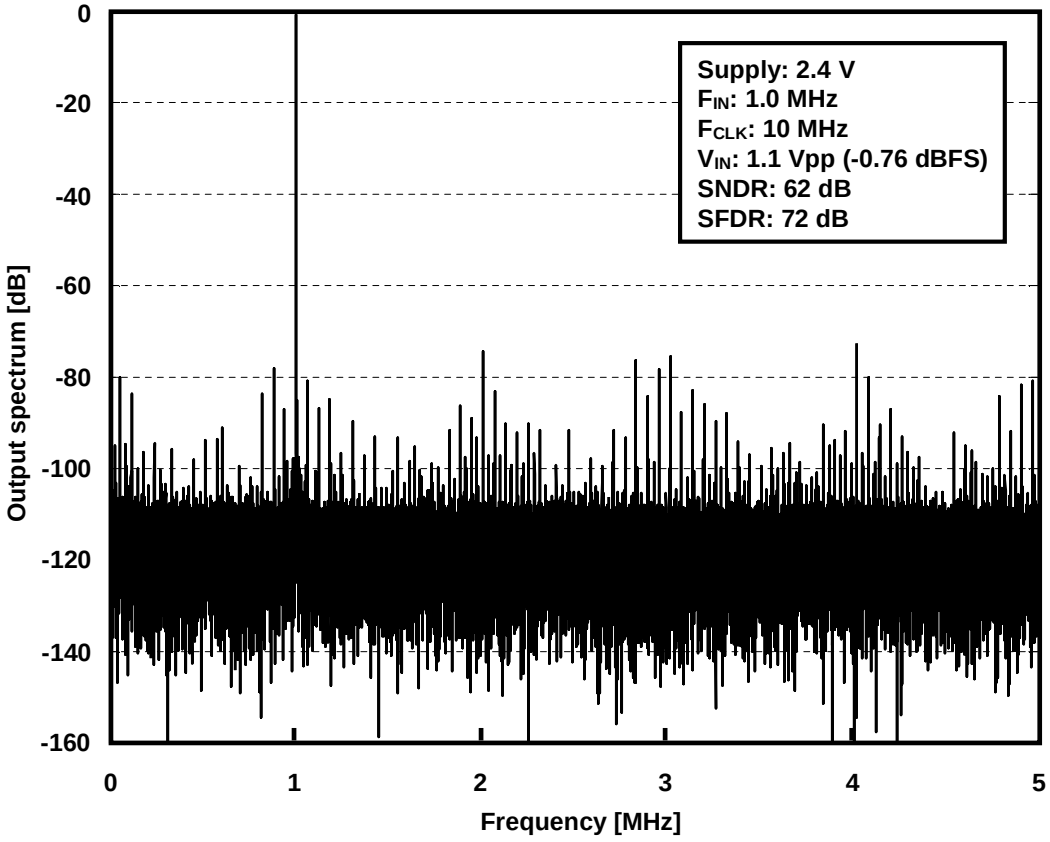


Figure 6.9: Measured output spectrum of the prototype pipelined ADC.

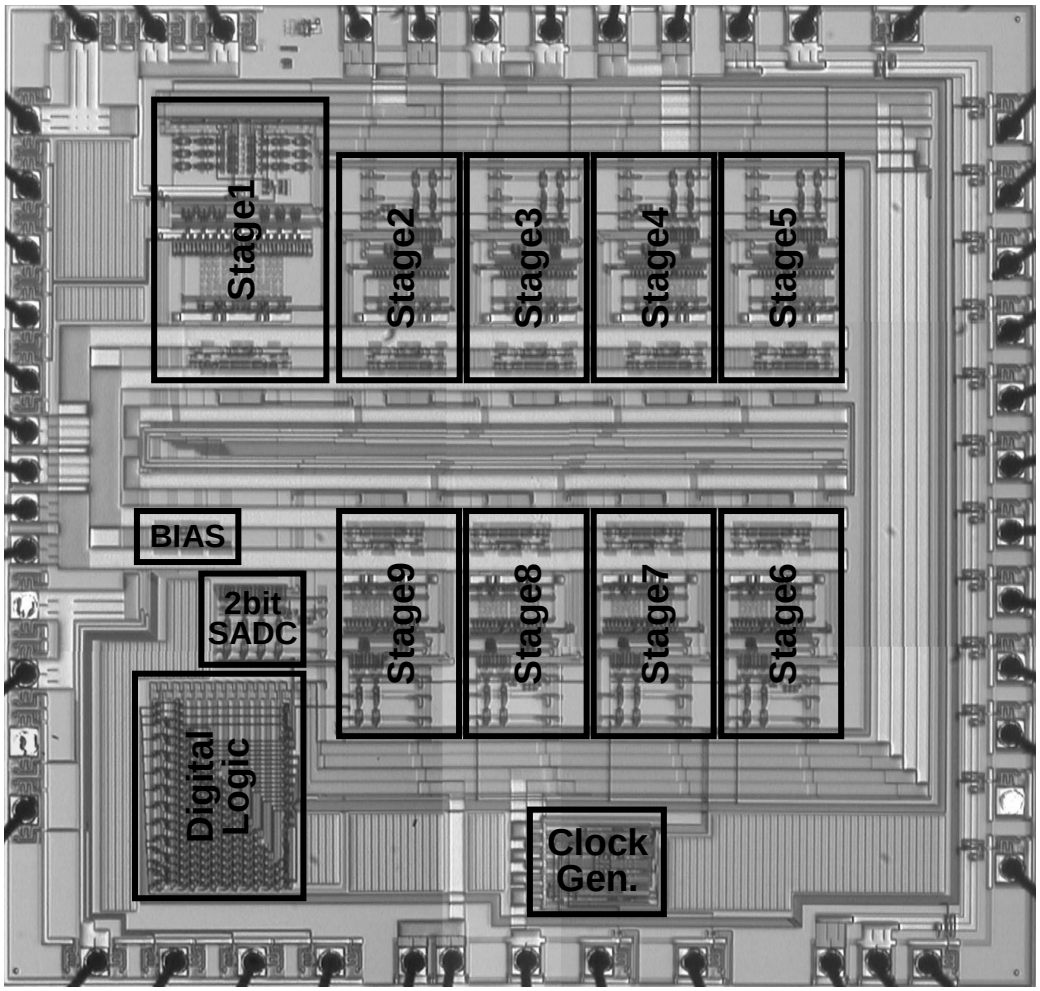


Figure 6.10: Die photograph of the prototype pipelined ADC.

Table 6.1: Performance summary of the prototype pipelined ADC.

Power supply voltage	**2.4 V**
Resolution	**12 bit**
Sampling frequency	**10 MHz**
Input range	**2.4 Vpp (differential)**
INL	**< 3.1 LSB**
DNL	**< 0.7 LSB**
SNDR	**62 dB @ F_{IN} = 1 MHz** **57 dB @ F_{IN} = 5 MHz**
Total power consumption	**19 mW (including digital and I/O)**
Active die area	**2.2 X 2.4 mm^2**
Technology	**0.35 µm CMOS**

CHAPTER 7. CONCLUSIONS

Design techniques were proposed for low-voltage and low-power analog CMOS integrated circuits. These techniques do not affect the reliability of fine-linewidth devices by over-stressing their gate oxides. Three analog-to-digital converters were designed to validate the proposed methods.

A 2-2 MASH delta-sigma audio ADC than can operate with a 0.6 V supply was implemented using the proposed switched-RC technique. This technique enabled highly linear input signal sampling over a broad signal range. The overall linearity of the modulator was improved by applying a low-distortion feed-forward topology, while the peak SNDR was enhanced by increasing the input signal range using quantized local feedback. The measured results of prototype IC fabricated in a 0.35 μm CMOS technology verify the validity of the proposed design techniques for low-voltage and high-performance operation.

A 0.9 V 20 MS/s CMOS pipelined ADC was designed. Resistive feedback reset and switched-RC techniques were employed in the design of low-voltage MDAC. Prototype ADC was implemented in 0.13μm CMOS technology and the simulation results indicate 11-bit linearity for the overall ADC.

A 2.4 V 12-bit 10 MS/s CMOS pipelined ADC was designed. The reference scaling architecture enabled the use of low DC gain opamp for building a high accuracy MDAC. Prototype ADC implemented in 0.35 μm CMOS technology achieves 72 dB SFDR and 62 dB SNDR with a 1 MHz input signal and 10 MHz sampling frequency.

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