# AN ABSTRACT OF THE THESIS OF

McKay W. Lindsay for the degree of Master of Science in Electrical and Computer Engineering presented on September 14, 2017.

Title: Co-planar Integration of Silicon Integrated Circuits and Microfluidic Networks for Biosensor Applications

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Silicon integrated circuit (IC) technology has enabled numerous electrical and optical sensors used in biological and chemical assays, where they can increase performance while decreasing cost and size compared to traditional detectors. There is significant potential to further leverage IC technology for lab-on-chip applications, creating affordable and portable medical diagnostic equipment by integrating sensors directly on the chip surface. This benefit is lost if chip makers must use large chip area to allow fluidic transport of biological or chemical sample to the sensors. In addition, traditional wire bond packaging creates a non-planar surface that is incompatible with traditional planar microfluidic structures. In this work, we use an industrial compression molding technique to embed CMOS integrated circuit dice in a planar epoxy substrate, which allows for the use of standard photolithographic processes for metallization, as well as the incorporation of planar

microfluidic delivery. We demonstrate combined fluidic and electrical routing over CMOS-integrated optical sensors in an accurate and reproducible way, as well as demonstrate an optical transmission experiment in the complete sensor platform. This scalable technique will enable a broad range of future IC-based biosensors and multi-sensor lab-on-chip systems.

# Co-planar Integration of Silicon Integrated Circuits and Microfluidic Networks for Biosensor Applications

by

McKay W. Lindsay

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McKay W. Lindsay, Author

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# TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

# LIST OF FIGURES

# LIST OF FIGURES (Continued)

# Chapter 1: Introduction

THERE have been continuous advances in combining solid-state sensors with microfluidics to create new ways of analyzing biological and chemical assays. These methods prove promising, less expensive solutions to typically expensive, slow, or labor intensive processes, but may not be conducive to modern mass production techniques. The problem lies in the cost of semiconductor processing, which is mitigated by the volume of chips produced at any given time. If silicon real estate is given up to enable microfluidic channels, the cost goes up proportionally. Likewise, the material and processing techniques for some sensors conflict with modern CMOS processing, making it difficult to take signals from sensors that may be in the nano-amp range and amplify them without significant distortion, when they are located on a different die. In this thesis, we will review technologies that may benefit from a reliable means of integrating fluidics with integrated circuits and what has been previously accomplished integrating ICs with microfluidics, and we will introduce a new scalable method we have developed for doing the same.

Modern CMOS chips, including sensors made in CMOS technology, put bonding pads at the edge of the chip for connecting to the outside world. Typically, this connection is done using a wire bonding procedure (Figure 1.1). A micro-wire is connected vertically to the pad, then to an external pin or other connector. This is a fragile connection, and commonly some form of glue or adhesive is placed to

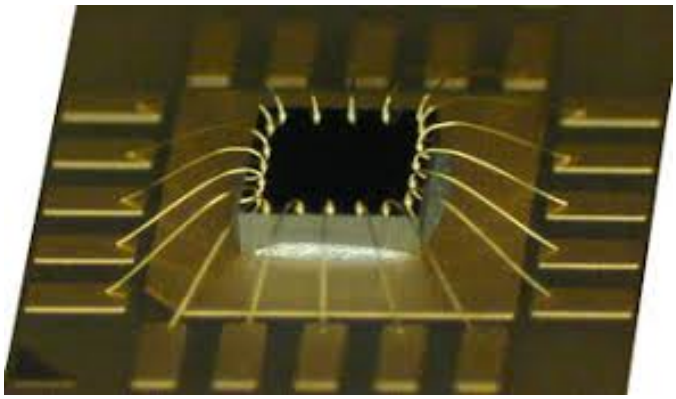

Figure 1.1: Wire bonds are a means of connecting an integrated chip to an external carrier. Wire bonds extrude vertically from the chip and are extremely fragile.

encapsulate the connection, supporting and protecting it. Sensors, located on the chip surface, and inside of these wire bonds, need physical access to the sample of interest; in the case of liquid material, this presents an added difficulty in getting the sample to and away from the sensor, as microfluidics are typically planar. As silicon processes become more efficient, the cost of creating these CMOS circuits and sensors has gone down, making their use more common and more cost effective. We are finding more, better, and cheaper ways of measuring, controlling and diagnosing disease every year using CMOS sensors, and fluidic integration is now the primary driver of the cost and size of the chip and system. A compromise must be made to effectively use these sensors, with two primary options:

1. We can increase the size of the sensor substrate, giving additional physical access space to route a fluidic sample down to the sensor and out again. If we do this, it means that a single silicon wafer, typically 5 to 12 inches in diameter, will be able to hold fewer chips on its surface. Therefore, to

create the same volume of chips will take a greater quantity of wafers, longer processing time, more energy, and much greater cost.

2. If we desire to keep the die as small, and therefore as inexpensive, as possible, we must find an alternative method of connecting the die to both electrical and fluidic sources. The primary challenge is developing a means of placing and connecting dice in a planar fashion, including planar metallization and fluidics. In this manner, where fluids need to be routed using channels, they may adhere to the silicon with a water-tight seal where the sample meets the sensor.

# Chapter 2: Background

There are numerous electrical sensors and electro-mechanical sensors that have been created with microfabrication technologies that have become useful tools for research and commercial applications in a number of different fields. Such technologies include detection of nucleic acid amplification [1] and hybridization [2] in fluids, quantification of protein-based and cell-based assays [3, 4], magnetically enhanced biosensors [5, 6, 7], multiplexed gravimetric and gas sensing [8, 9], nanopore sensors [10], opto-sensors [11, 12] and increasingly miniaturized electrochemical sensor systems [13]. There have also been a number of methods developed to incorporate a microfluidic delivery system into electrical and electromechanical sensors [14, 15, 16]. In this work, we focus on a number of biosensors and biomedical applications that require microfluidic delivery. Sometimes these needs can be met by simply applying a fluidic sample directly onto the sensor through bulk delivery [17], or applying a sample to a wicking device such as doing a blood sugar test [18], where the paper that the blood is applied to has two purposes: 1) it mixes the blood with an enzyme that creates a signal that is measurable, and 2) it limits the amount of sample that reaches the sensor. For context, I present a number of applications that use a fluid sample in conjunction with electrical sensors implemented in CMOS.

## 2.1 Previous work in CMOS-integrated fluidic biosensors

The following examples of IC biosensor applications all require fluidic delivery of a sample of interest. Most use bulk fluid transport transport, and each of these novel sensors would require microfluidic delivery to be useful in a real-world application.

### 2.1.1 Microelectromechanical detection of DNA

In an article entitled, "A CMOS Cantilever-Based Label-Free DNA SOC With Improved Sensitivity for Hepatitis B Virus Detection," [19] the authors develop the idea that a microelectromechanical system (MEMS) cantilever can be used to detect a specific DNA sequence, in this case the hepatitis B virus. Cantilever fabrication involves creating a layered substrate of polysilicon and metal layers with silicon dioxide ($SiO_2$) on a silicon substrate [20]. A passivation layer is used to define the structure of the cantilever, and the $SiO_2$ is removed. A layer of gold is applied to the top surface of the structure due to its biocompatibility with DNA probe molecules that are used to detect the virus. Finally, some of the silicon is removed from under the entire structure to release the cantilever. This creates a "diving-board" shaped sensor that includes a piezo-resistor, or a resistor that changes its resistivity based on how much it bends, as seen in Figure 2.1.

As complimentary DNA attaches to the probe DNA the sensor bends, causing a resistance change. This resistance change is converted to frequency using an RC oscillator, and then to a digital number through a series of CMOS-based amplifiers and logic. The DNA solution being tested needs to be exposed directly to the

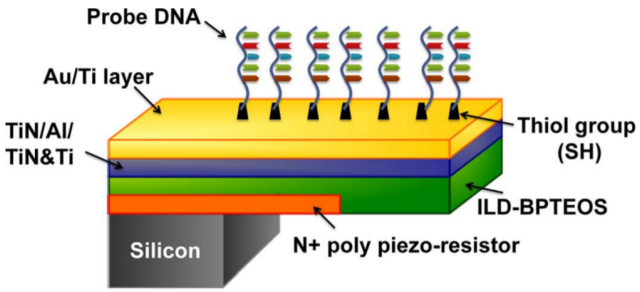


Figure 2.1: Cross-sectional view of micro-cantilever based piezo-resistor for the detection of DNA [19].

cantilever sensor, which requires a fluidic solution containing the sample to be delivered over the sensor without applying undue pressure directly to the sensor.

### 2.1.2 Ion-sensitive field-effect transistor

In "An integrated semiconductor device enabling non-optical genome sequencing," [17] the authors developed a method to use transistors to determine the sequence of DNA bases in an unknown sample. A sample of DNA is fragmented (Figure 2.2b), and each fragment attached to a magnetic bead (Figure 2.2c), amplified, and placed inside a well created in the CMOS structure. At the base of this well is an ion-sensitive field-effect-transistor (ISFET), which is used as a pH sensor for this process. With all of the elements in place, the sensor, magnetic bead, and DNA are exposed to a deoxyribonucleotide (dNTP). There are four dNTPs found in DNA, they are commonly referred to a A, T, G and C and are base pair units, A pairing with T, C pairing with G. When the correct nucleotide is exposed to the DNA on the beads, it attaches to the chain as seen in Figure 2.2d

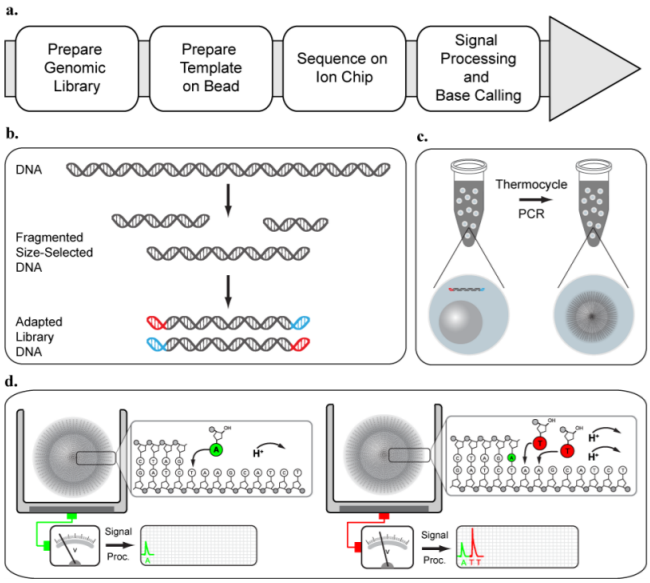


Figure 2.2: ISFET genome sequencing overview [17]: a) Overview of ion sequencing work flow. b) DNA is fragmented to appropriate size and forward and reverse adapters ligated. c) Identical DNA segments are attached to micro-beads. d) The micro-beads are placed onto the chip containing the ISFET wells. In an automated process the chips/micro-beads are exposed to one of the four dNTPs; if a complimentary base is found, the dNTP attaches to the DNA, releasing a hydrogen ion in the process. The hydrogen ion changes the pH of the system and is detected by the ISFET. The volume of hydrogen ions is measurable and correlates to the number of matching pairs. The substrate is rinsed and the next nucleotide is applied cyclically.

and releases a hydrogen ion in the process. A hydrogen ion in aqueous medium creates a change in pH of the system, which in turn creates a change in charge on the metal-oxide sensing layer above the ISFET. When enough of these reactions happen at the same time, a measurable difference can be recorded, and the next nucleotide of DNA can be determined. The chips were manufactured in packages with a disposable polycarbonate flow cell, which isolates the fluids to regions above

the sensors (Figure 2.3). While commercially successful, this cartridge still enables

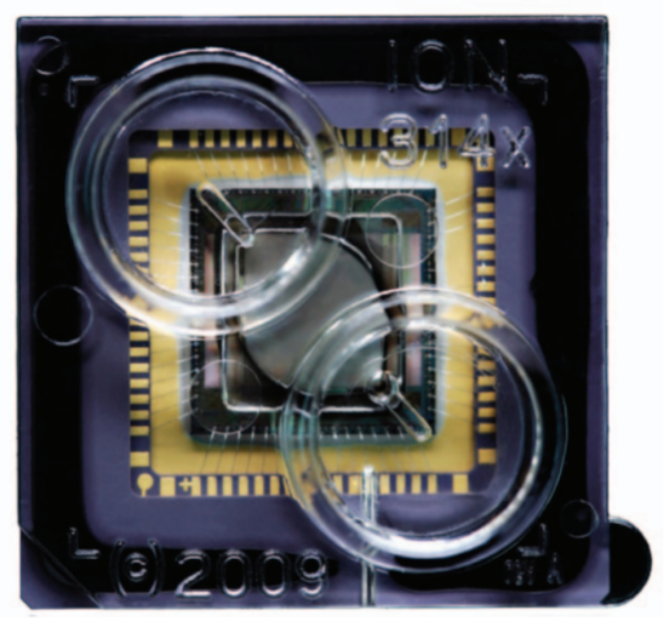


Figure 2.3: A polycarbonate cover to protect the wire-bonds and other electronic parts from the liquid that needs to get to the ISFET sensors in the center of the die. [17]

only bulk delivery of the fluidic reagent to a large array of sensors.

### 2.1.3 Microfluidic impedance cytometer

In "Resonance-enhanced microfluidic impedance cytometer for detection of single bacteria," [21, 22] the researchers expound on the idea that most biological assays are only able to analyze bulk samples, meaning that they can only detect something if it is in large enough concentration. Increasingly, there is the desire and need to develop techniques that provide single-cell resolution. The researchers have

developed a process that combines a microfluidic cytometer with impedance spectroscopy, and they are able to do this with label-free samples. The system consists of a front-end PCB that contains the microfluidic system, dielectrophoretic focusing electrodes, and measurement electrodes, as seen in Figure 2.4C. The back-end

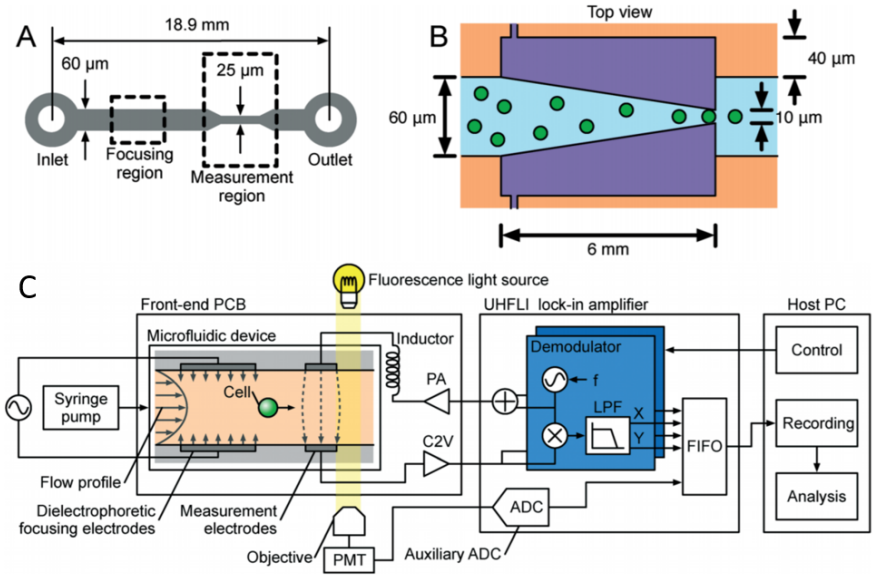


Figure 2.4: Schematic of the complete microfluidic cytometer [21]: A) A schematic of the microfluidic system. B) Schematic of the top view of the focusing region. The focusing electrodes are connected to the signal generator, These electrodes electrically (not mechanically) align the the cells to be measured in the measurement region. C) The lock-in amplifier drives the series resonance circuit, formed by the discrete inductor and the impedance between the measurement electrodes, with an alternating current (AC) signal at a frequency close to resonance. The resonance frequency shifts when cells or particles pass through the measurement area due to a change in the channel impedance.

comprises a lock-in amplifier and recording circuit. The focusing electrodes are located above and below the microfluidic channels, which is difficult to fabricate with scalable microfluidic techniques. The measurement electrodes intersect a narrow

(25 $\mu$m) fluidic channel.

While successful for a single channel, adapting this technique to multiple channels requires a more robust method for interfacing sensors and CMOS electronics with microfluidic delivery.

## 2.2 Previous methods for fluidic delivery to CMOS-integrated biosensors

The integration of fluid samples with CMOS is manageable in a laboratory setting through heterogeneous approaches [23], but an elegant, reliable fluid-IC interface solution continues to elude the lab-on-CMOS community. A common approach is to use bulk fluid delivery [2, 5, 10], which is robust but limits the ability to deliver nanoliter fluid volumes, or to route fluids to individual sensors in an array. In contrast, for microfluidic delivery, a primary challenge is the need to mesh planar microfluidic channels on a chip surface that, due to wire bonds, is not planar. Additionally, the integration of soft PDMS fluidics with rigid silicon substrates is a challenge for making reliable fluid seals, due to the small ($mm^2$) chip-side contact area, as well as the non-planar top-level topography of an IC.

Here we will discuss several of the approaches have been demonstrated for interfacing micron-scale fluid channels with chip surfaces.

### 2.2.1 Fluidic integration using a physical spacer

In "A Hybrid CMOS-microfluidic contact imaging microsystem," [24] the authors demonstrate an alternative to a planar approach to microfluidic CMOS integration. In this paper, the authors demonstrate contact imaging of a microfluidic sample volume, which requires fluidic channels located directly on top of optical sensors. The authors developed a multi-layered approach as shown in Figure 2.5. The fluids

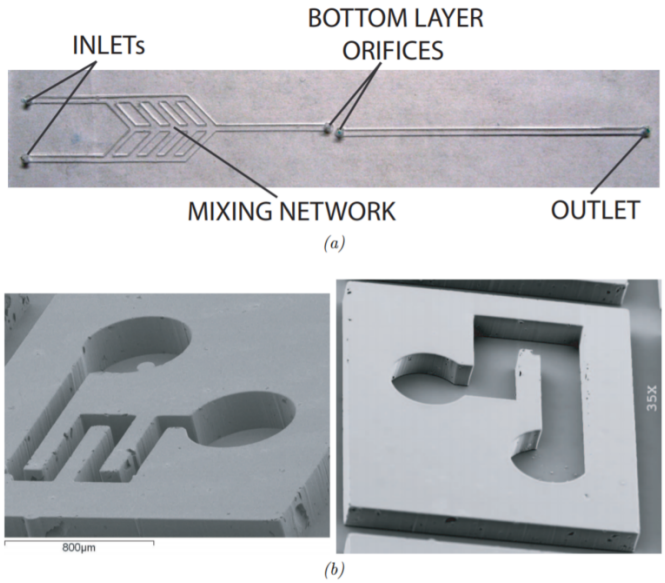


Figure 2.5: To avoid the wire-bonds and other electrical components a multilayered fluidic network is used [24]. a) The top layer contains the inlets, outlet, a mixing network, and orifices that connect to the lower layer. b) Two examples of lower layer networks, the whole of which is smaller than the silicon die.

are introduced, mixed, and travel to a point close to the imaging sensors, then travel down to a layer in contact with the sensor, then back up and away from the CMOS surface. This method of microfluidic integration makes it possible to interact with

the sensors while avoiding obstacles such as non-planar wire bonds. This method is successful, but as chips and sensors continue to shrink the microfluidic channels can not scale at the same rate.

Using this technique, the authors demonstrate chemiluminescence detection through the channel. As the material that was used to create the microfluidic channels is transparent, the chemiluminescence reaction was detected by sensors that were not directly in the path of the microuidic channel. A limitation of this approach is that the sensor chip must be large enough for the microfluidic channel, plus the orifices (for transporting between layers), to fit within wire bonds.

### 2.2.2 Fluidic delivery using flip-chip bonding

In "Seamless integration of CMOS and microfluidics using flip chip bonding," [25] the authors demonstrated a method for connecting a bare silicon die directly to a flexible polyamide PCB, as shown in Figure 2.6. This method consists of creating a copper contact on a flexible PCB, followed by application of a layer of SU-8 on the PCB, leaving open areas only around the copper pads. This creates a small well around each pad that can be filled with a solder paste. Then an IC chip is soldered to the underside of the flexible PCB, which has an opening cut out where the sensor lines up. The microfluidic layer is then attached to the top side of the PCB without any interference from the traces, which are being routed out on the PCB, as seen in Figure 2.6.

This work demonstrates a way to expand the adhesion area of the microfluidics

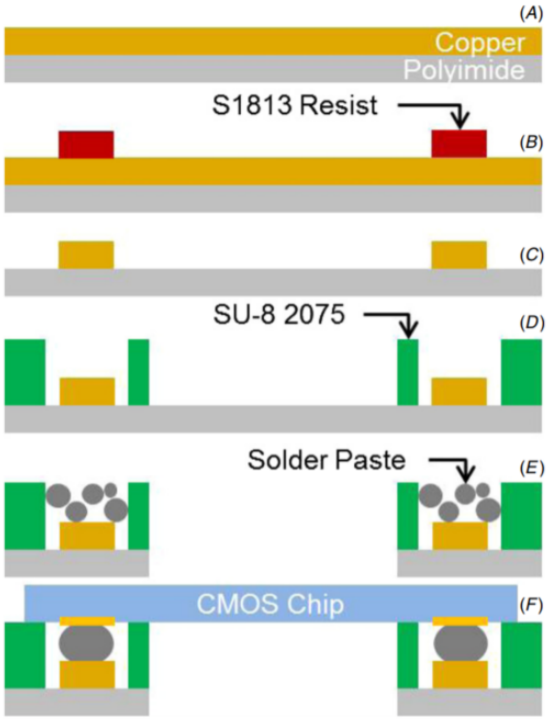


Figure 2.6: Electrical connections to a CMOS chip on a flexible PCB [25]: A) A Flexible PCB with unpatterned bare copper. B) Using S1813 positive resist pattern the copper. C) Etching copper to leave traces and bonding sites on the board. D) Patterning SU-8 to form the openings over the copper pads. E) Cavities above copper bonding areas are filled with a solder paste and an opening is cut in the polyimide to allow access to the sensing region of the chip. F) Finally a CMOS chip is flip-chip bonded while in contact with the SU-8 layer to simultaneously create electrical connections and insulate them from fluids.

without effecting the primary die area. In addition, soldering the silicon chip directly to a flexible PCB may be a very scalable approach. The contact pads on the die are 100 $\mu$m by 100 $\mu$m, which is possible to manufacture and purchase through commercial PCB vendors. This work demonstrates that SU-8 can be used both to guide solder ball formation, and for planarizing the surface, which reduces

the possibility of leakage and provides an electrical insulation between the pads. This method still provides only bulk fluid delivery to the IC surface.

### 2.2.3 Flexible PDMS substrate for electrical and fluidic contact

In "Flexible packaging of solid-state integrated circuits chips with elastomeric microfluidics," [26] the authors chose to use only flexible materials for fabrication. To accomplish this, they created a microfluidic layer for both the fluidic sample and the fluidic interconnects, as shown in Figure 2.7. The CMOS chip was aligned and adhered directly to a thick PDMS substrate. Embedded within the substrate were tubes or tunnels, in which not only the sample could flow but also a liquid metal, which is used for the electrical connections. The liquid metal, Galinstan, is a combination of gallium, indium, and tin, which is liquid at room temperature, non-toxic, and non-evaporative. Having this interconnect in fluidic channels allows them to bend and stretch while being used. This method could allow a sensor to be applied as a band-aid or other conformable shape.

The results showed that a primary limitation of this design is that the inlet for each input/output (I/O) is about 750 $\mu$m and needs to be separated by about 1 mm. The Galinstan itself is more conductive than mercury and has been used for antenna creation and RF circuits. Increased strain on the fluidic channels does not affect the $I_D S$ characteristics of a transistor embedded in the substrate, and with multiple photolithographic steps, multiple layers of fluidic channels can be created. This work demonstrates a method for combining rigid chips with non-

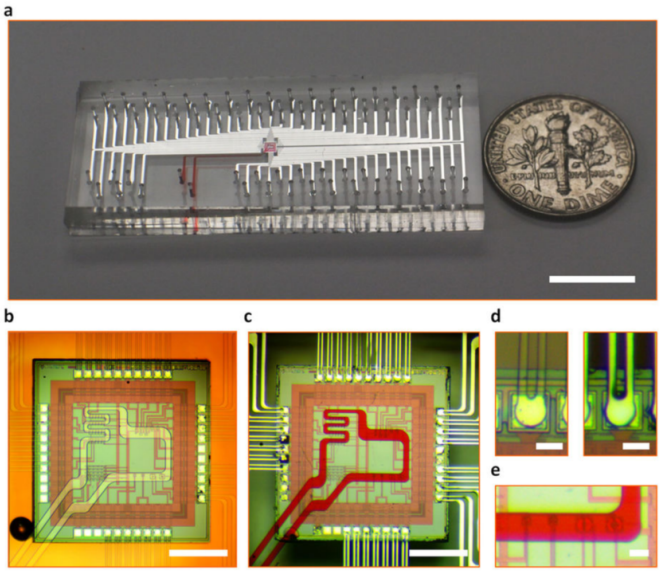


Figure 2.7: Flexible PDMS substrate for electrical and fluidic contact [26]: a) Image of the packaged CMOS/microfluidic integrated system with a dime for size comparison. b) Image showing the microfluidic channels (for traces and sample) are aligned with CMOS pads and sensors. c) Image showing the interconnect channels are filled with liquid metal and the microfluidic sample delivery channel filled with red food dye. d) Image of an interconnect channel aligned with a CMOS contact pad before (left) and after (right) liquid metal is injected. e) Image of the microfluidic channel accurately aligned with the sensor area.

rigid microfluidics, though it may be limited in utility for scalable manufacturing.

### 2.2.4 Fluid delivery and manipulation using electrowetting

In "An integrated CMOS quantitative-polymerasechain-reaction lab-on-chip for point-of-care diagnostics," [27] the authors created a surface that could take a small fluidic sample (1.2 nanoliter) and move it across and through a gridded area on a CMOS chip, as seen in Figure 2.7. While previous studies have demonstrated

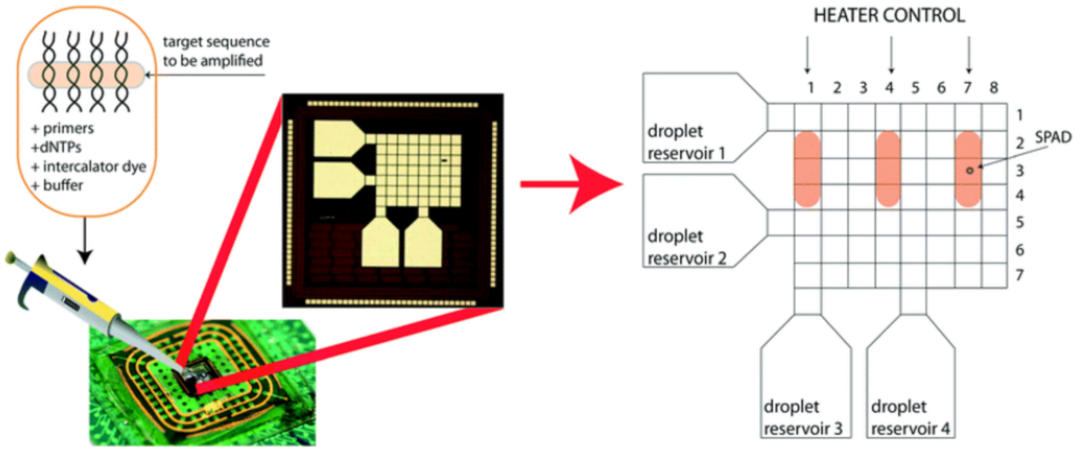


Figure 2.8: Droplets of the test sequence and PCR reagents are delivered to one of four reservoirs on the chip. The entire surface is heated with three heaters at columns 1 4, and 7. Measurements can be made from the photodiode located at (3,7) [27].

electrowetting, this work also included sensors on the array that could be used for sensing. Specifically, they included heaters to warm the sample, and photodiode sensors to detect phosphorescent tags within the sample. The authors describe an issue with evaporation of the sample when there was no cover slip, but as a proof of concept it was successful. This work demonstrates an alternate way to use CMOS and sensors in a microfluidic environment, without a confined channel, but does not provide true defined-channel sample delivery.

### 2.2.5 Planar integration in an epoxy carrier

In "Packaging commercial CMOS chips for lab on a chip integration," [3] the authors embed a sensor chip in the center of a epoxy disk, as shown in Figure

2.8a. They then pattern gold traces from the contact pads on the chip to outer

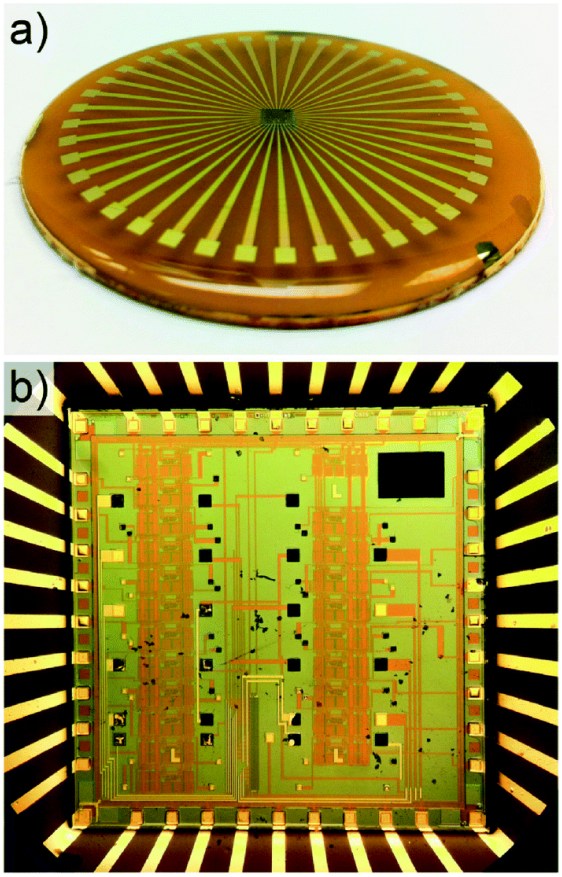


Figure 2.9: CMOS chip encapsulated in epoxy [3]: a) The die is connected to external pads in an Epoxy Molded Chip Carrier. b) close up view of the die and the connections along the chip-substrate interface.

probe pads on the epoxy disk. This method demonstrates metallization (Cr/Au) process from IC to carrier, even on a not completely planar surface, as well as the subsequent addition of microfluidic channels on top of the carrier. This approach requires only two additional masks for the electrical connections, and the authors show that the PDMS had a sufficiently smooth area to adhere to and create sealed

channels. This method also introduces molding the IC into an epoxy carrier; similar methods have been used using a silicon carrier [28, 29]. While promising as a general approach, this method is done chip-by-chip, and the pour-over process leaves large gaps at the IC edge. A more repeatable epoxy encapsulation method is needed for scalable and robust integration.

# Chapter 3: Wafer-level integration approach

> "..., there is a great need to integrate microfluidics with microelectronics for further signal processing, and an urgent necessity to co-join microfluidics and micromechanics to develop advanced physically based functionalities." [30]

The primary challenge combining integrated circuits with microfluidics is the non-planar surface created by wirebonding. To address this challenge, we have chosen a process that planarizes the entire substrate using a fan-out-wafer-level-packaging (FOWLP) [31, 32] process, while promoting access to sensors on the IC surface. FOWLP is a mature technology commonly used in ball-grid-array (BGA) IC packaging. FOWLP takes individual dice and embeds them in a low cost material such as epoxy mold compound (EMC) under compression, with space allocated for additional I/O connection points. This avoids the use of expensive silicon space to accommodate a high I/O count. Redistribution layers (RDL) are formed using physical vapor deposition (PVD) and subsequent electroplating/patterning to reroute I/O connections on the die to the mold compound regions in the periphery. We have adapted this method not to accommodate additional I/O, but rather to provide additional space for applying a microfluidic layer that is co-planar with the silicon/EMC substrate. The complete process flow uses common tools and methods used for silicon IC production. The basic process flow is similar to that which would be found in any foundry:

1. Clean the substrate, using wet and dry methods.
2. Use photolithography to apply patterned layers of photoresist and insulation or passivation on the wafer.
3. Deposit metal on the surface to define metal traces.
4. Use wet processing/etch to remove unwanted materials.

The following section summarizes the process flow by first reviewing the layers that comprise the final device, followed by greater detail on each process step.

## 3.1 Layer process flow for FOWLP and metalization

The material layer stack-up for integrating metal electrodes and fluidic channels on top of FOWLP-embedded integrated circuit chips is shown in Figure 3.1a. The primary layers and fabrication steps are summarized in this section, and optimization of selected process steps is described in additional detail in Section 3.2. A primary goal of this developed process flow is to create access to portions of the chip that require either electrical or physical access, while protecting and passivating those areas of the chip that do not need to be accessed. In addition, we must also minimize the interface height between layers, as subsequent metallization and fluidic layers need to contact across these interfaces.

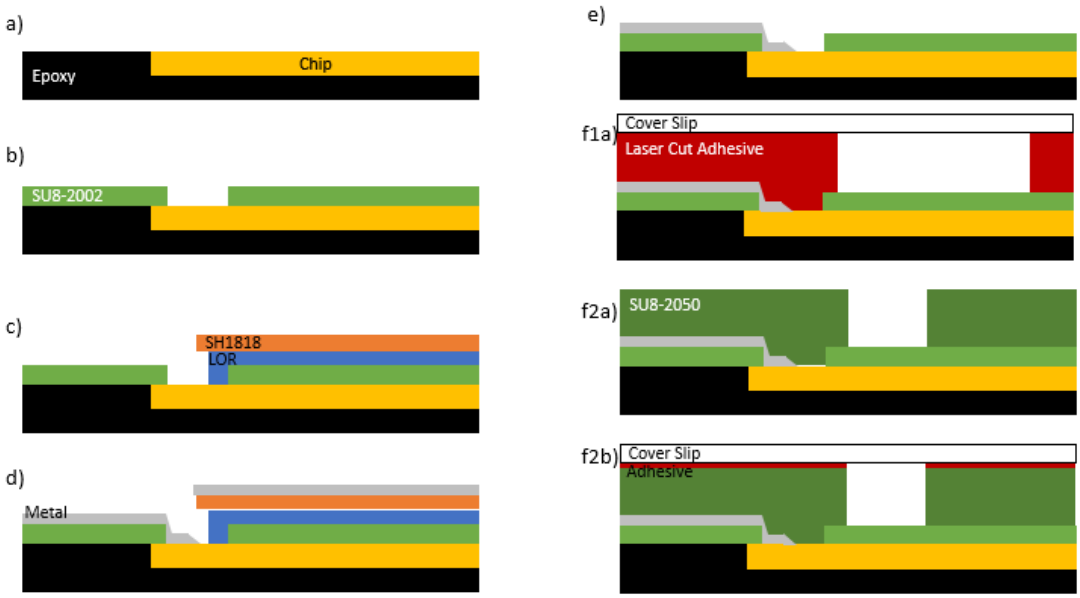


Figure 3.1: (a) Molded epoxy disk with embedded CMOS chip. (b) A 2 $\mu$m layer of SU-8 is applied as passivation and to smooth the epoxy and epoxy/chip interface. SU-8 is patterned to give access to pads on chip. (c) LOR is applied to help with lift-off. SH1818 is patterned to create traces that connect to the chip. (d) Metal is applied to the substrate through a sputter process; approximately 20 nm of chrome followed by approximately 200 nm of aluminum. (e) After lift-off, all LOR and SH1818, and any metal on top of the SH1818, is removed, leaving only the desired traces. Microfluidics are created in one of two methods: f1a) A laser cut adhesive is attached to a cover slip and adhered directly onto the prepared chip-substrate, or f2a), a 50 $\mu$m layer of SU-8 is patterned on the substrate and f2b) an adhesive layer and cover slip are placed directly on the SU-8.

### 3.1.1 Surface cleaning

In preparation for the application of different materials to the EMC and chip surfaces, we use an oxygen plasma treatment to clean the substrate. This has shown to help in the adhesion of the various materials to the epoxy disk, including both photoresist and metals. As the substrates are molded by an external collaborator,

we receive the prepared substrates and must remove any residual adhesive or other chemicals that remain on it after the compression molding process.

### 3.1.2 Patterned substrate passivation

The first layer in the process stack (Figure 3.1b) is the passivation layer, which is used to protect portions of the embedded chip from both environment and subsequent layers of the process-stack. The other benefit of the passivation layer is that it normalizes the surface height and smooths the interface between chip and substrate. We use SU-8 2002 (Microchem) for this layer, which provides about 2 $\mu$m of passivation when spun at 3000-4000 RPM. SU-8 is a permanent, inert, photo-patternable epoxy. When fully cured, it adheres well to both the chip and the epoxy substrate, smooths the surface of the epoxy, and minimizes the interface ridge or gap between the chip and the epoxy disk. SU-8 is also transparent to visible wavelengths and therefore does not affect light transmission to underlying photodiode sensors, and thus we are able to apply a fluidic layer directly on top of passivated diodes. We use a custom chrome-on-glass photolithography mask to pattern the SU-8, leaving openings in the passivation layer to access top-metal bond pads on the chip. An example of such passivation openings (or 'windows') is shown in Figure 3.2. We perform a second oxygen plasma ashing step after patterning, and we permanently cure the SU-8 at 165° C for 30 minutes.

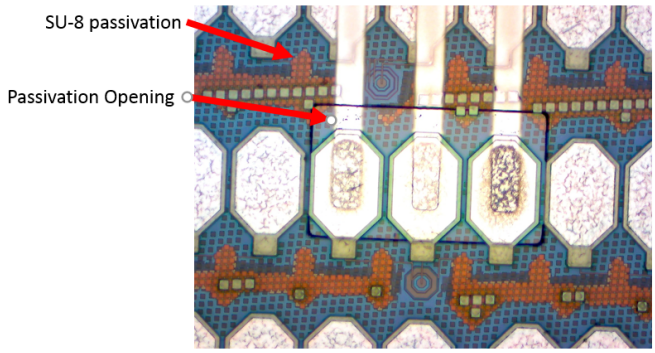


Figure 3.2: SU-8, a clear patternable epoxy, covers the entire surface of the chip with the exception of openings used to access bond pads on the chip.

### 3.1.3 Primary photolithography for metallization

After curing the passivation layer, we use a two-step photoresist process to create the pattern (Figure 3.1c) that defines the metallization pattern. We apply a lift-off-resist (LOR 30B, Microchem). This LOR assists in the metallization stage, where it allows the metal traces to have a smoother interface on their edges and aids the removal of excess metal during lift-off. This is especially important for thick metals. The LOR is spun on and soft-baked at 165° C for 10 minutes. After soft-baking the LOR, we spin on SH1818 photoresist (Microchem), and expose the photoresist through a custom mask that defines the electrical connections to the chip and, if necessary, between chips. A final oxygen plasma ash is performed to help prepare the surfaces for metallization.

### 3.1.4 Deposition and lift-off of metallic interconnects

After substrate patterning, metal traces are applied using either a sputtering deposition process or thermal evaporation (Figure 3.1d). Each of these provides advantages, whether to deposition rate, adhesion, or conformity. Metal deposition through evaporation is a fast way to apply thicker amounts of material (hundreds of nanometers thick). Melted metal evaporates from a single point, creating a very directional (anisotropic) deposition flux, as seen in Figure 3.3a. This direc-

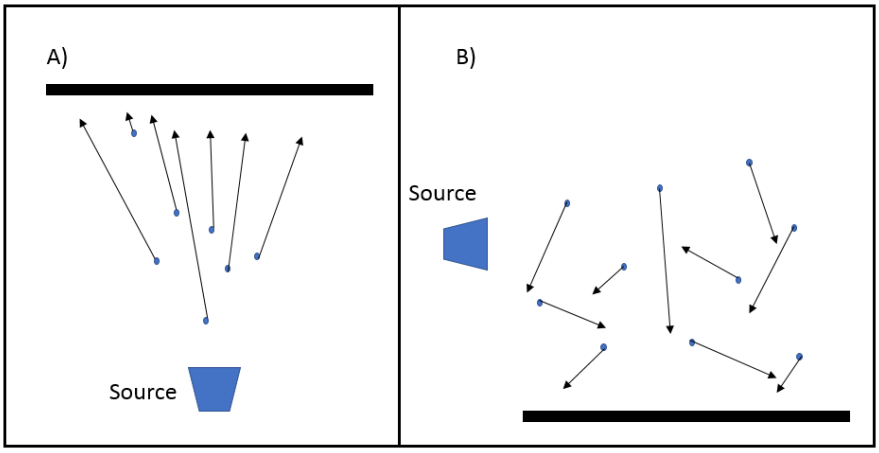


Figure 3.3: Metal deposition: a) Metal evaporation is emitted from a single point forming a monolithic layer of metal. b) In metal sputtering the metal particles approach the substrate from all directions, giving a more even distribution of metal on all surfaces.

tionality creates non-conformal deposition, and subsequent lift-off is much cleaner. Deposition through a sputter process is typically slower than evaporation, but the metal particles arrive from all directions, as seen in Figure 3.3b. Metal deposited through sputtering is conformal and creates a more consistent electrical connection

over ledges.

Aluminum is used as the primary metal for traces to interconnect encapsulated chips, and to connect to the outside world through redistribution of bond pad contacts. Unfortunately, aluminum does not adhere well to the SU-8 passivated substrate. For this reason, we deposit an initial layer of chromium (aproximately 30 nm), which has much better adhesion characteristics to both SU-8 and aluminum. The chromium is followed by aluminum deposition (approximately 200 nm) which is chosen for its lower resistance and lower stress in thick films.

Following blanket metal deposition across the substrate, we need to remove metal from the unwanted places, which is done through a lift-off process. The entire substrate is submerged in Remover PG (Microchem) heated to 40° C. The LOR is dissolved away, leaving only the metal that was not on top of the LOR (Figure 3.1e). This is the final step of the electrical connections. Additional process steps provide the microfluidic connections but do not affect the electrical properties.

### 3.1.5 Addition of fluidic layers to metallized EMC substrate

Once the electrical connections are fabricated, we can add a microfluidic delivery layer directly above the metallized IC. We have established two approaches for applying microfluidic channels to the prepared substrate. In the first method, we laser-cut channels in a double-sided, pressure sensitive, adhesive sheet, and cut a plastic cover-slip with the necessary inlets and outlets (Figure 3.1f1a). Using

the adhesive sheets, we can create fluidic channels with a height of 170 $\mu$m and width as small as 750 $\mu$m. The second method is to pattern microfluidic channels using SU-8 2025 or SU-8 2050 (Microchem). The SU-8 is again applied using a spin-on process, and a negative photolithographic mask is used to define the fluidic channels. After development, we can create microfluidic channels from 20 - 100 $\mu$m wide and approximately 25 - 50 $\mu$m deep (Figure 3.1f2a). Finally, a cover-slip of mylar, with openings for inlets and outlets, is adhered over the open channels (Figure 3.1f2b).

## 3.2 Fabrication process details

Significant process development iteration was required to develop optimized processes that were robust and reproducible. The following sections will detail results of experimentation on how to optimize passivation, metallization, and application of microfluidics on the co-planar IC encapsulated disks.

### 3.2.1 Co-planar CMOS IC encapsulation in EMC wafers

Starting with known good die from a conventional IC fabrication process (Figure 3.4a), ICs are placed face down onto a thermal release tape within a carrier (Figure 3.4b). The carrier is then filled with granuals of the epoxy compound, sifted through a gridded plate to form an even distribution on the carrier. The prepared carrier is compression molded at temperatures of less than 200° C, forming a

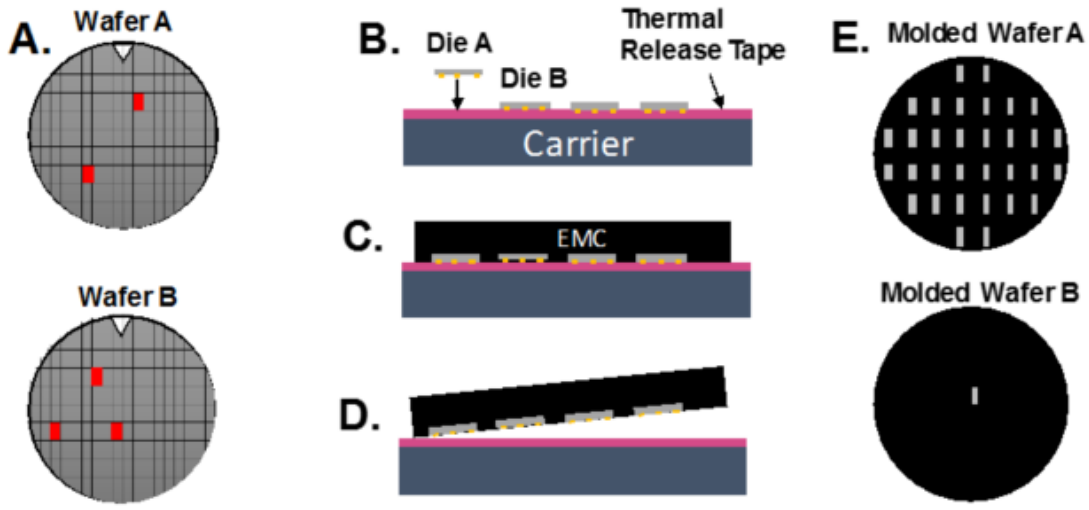


Figure 3.4: An overview of the co-planar CMOS encapsulation process is illustrated: (a) Two example IC wafers fabricated in different processes and different target designs; (b) a carrier substrate prepared with a thermal release tape allows temporarily bonding heterogeneous silicon dice ; (c) epoxy overmolding using a compression tool; (d) molded wafer de-bond from thermal-release tape; and, (e) reconstituted heterogeneous wafers with varying silicon density. Image provided by Chien-Hua Chen and Michael Cumbie

fused semi-conductor-grade epoxy mold compound (EMC), with a thickness of approximately 1 mm (Figure 3.4c). The EMC is then de-bonded from the carrier at an elevated temperature to activate the thermal release adhesive, followed by a hard bake to fully cure (Figure 3.4d). The EMC has been engineered to bring its thermal expansion coefficient closer to that of silicon, to minimize stress and warpage as the molded wafer returns to room temperature. At this point, the EMC substrate can be cut with a router or laser-cutting tool to the desired form factor. For this work, the EMC was cut into 75mm wafers with an IC centered in each substrate.

### 3.2.2 Passivation layer

The decision to apply a passivation layer was made following failed attempts to apply aluminum traces directly to an epoxy wafer. We found that adhesion of the metal to the substrate was difficult, and that when metal was applied the surface of the epoxy, it was not smooth enough for a 400 nm thick trace to be continuous (for details see Section 3.2.4.) The interface between the silicon IC and the epoxy was also found to be of an inconsistent texture. The decision to add a passivation layer also helped to protect portions of the IC that we did not want exposed (especially to liquid samples).

We applied a passivation layer of SU-8 2002 (Microchem) over the top of the chip and epoxy substrate. We found that 2 $\mu$m was enough to smooth the non-conformity of the substrate and remove the interface gap between the chip and epoxy. Again, the substrate is prepared by a 1-minute oxygen plasma ash before applying the SU-8 via a spin-on process. We expose the SU-8 with a custom mask to expose the pads on the chip. Before curing the SU-8 (30 minutes at 165° C), another oxygen plasma ash is performed in preparation for the next layers.

### 3.2.3 Patterning lift-off metallization mask

The next layer applied to the passivized substrate is a lift-off-resist (LOR 30B, Microchem). This was found to be necessary to ensure a clean lift-off and improve connectivity when a metal trace connects from the top of the passivation layer down into a connection well (Figure 3.5). On top of the LOR is applied SH1818

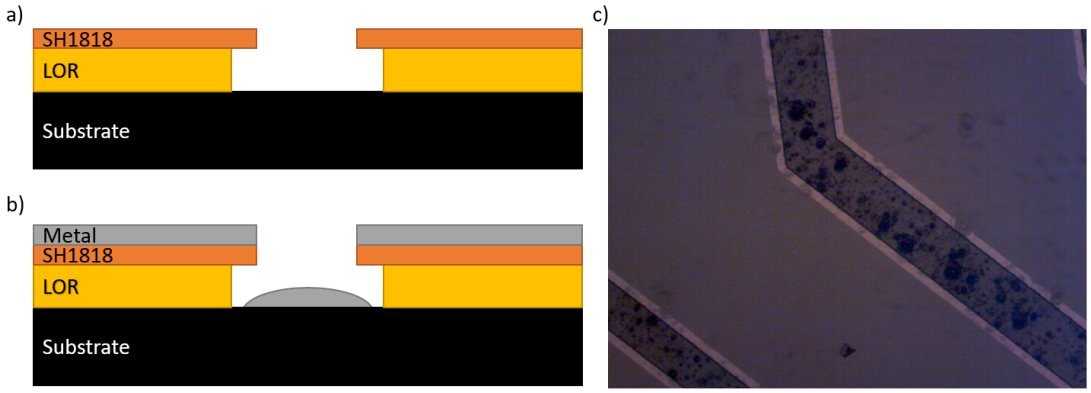


Figure 3.5: Lift-Off-Resist (LOR) process: (a) When SH1818 is developed LOR is also dissolved away faster than the SH1818 leaving an overhang. (b) When metal is sputtered on to the surface because the sputtering comes from all directions metal adheres under the overhang. (c) Image of bare epoxy disk with LOR and SH1818 patterned on top. The light area on the edge is the SH1818 overhanging the LOR.

photoresist (PR), which is patterned with a mask to define traces that connect to the chip. The LOR was found to be necessary, where aluminum's tensile strength tended to exceed the strength of its adhesion to the layers beneath it, resulting in poor lift-off. LOR is a sub-layer placed below standard SH1818 PR. When the SH1818 PR is developed, the LOR underneath is removed at the same time as the SH1818 with the same developer. Because the LOR is not photo-sensitive, even after the SH1818 has completed developing the LOR continues to dissolve, creating an overhang of SH1818 on top of the LOR (Figure 3.5a). This overhang has multiple benefits including improved metal adhesion and cleaner lift-off process.

In addition, we found that SH1818 PR and LOR will adhere will directly to the epoxy substrate as long as an oxygen plasma ash is performed beforehand. It should also be noted that acetone should never be used at any time to clean the

surface of the epoxy. Even after thorough rinsing, any photoresist we used, SU-8, LOR or SH1818 had a tendency to peal up at the edges after development on a desk exposed to acetone.

### 3.2.4 Metallization

There were two methods attempted for metallization of the patterned substrate. The first method used, thermal evaporation, was also used to determine what would adhere well to the substrate; the second method used was a sputtering process. The benefit of sputter deposition is that it is an omni-directional application of metal, although it is a much slower process. Figure 3.6 shows how deposition profile is different for each of the two different processes.

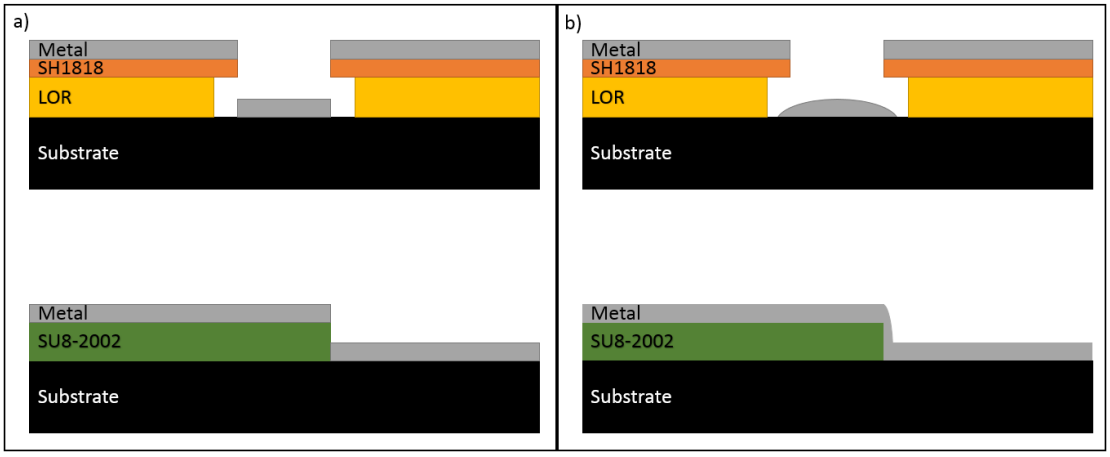


Figure 3.6: Difference between thermal metal evaporation and sputter deposition: (a) In thermal metal evaporation the metal comes from one direction (directly above) which can cause discontinuities. (b) Sputtered metal comes in from every direction, which improves connectivity.

Early testing of metal adhesion determined that evaporated aluminum would adhere to the patterned epoxy coupon but would not lift off cleanly. A plasma clean helped improve adhesion, but lift-off still had a tendency to cause traces to peel away, as the tensile strength of aluminum overcame the adhesion strength of aluminum to the epoxy. Figure 3.7 shown some of the early tests after lift-off.

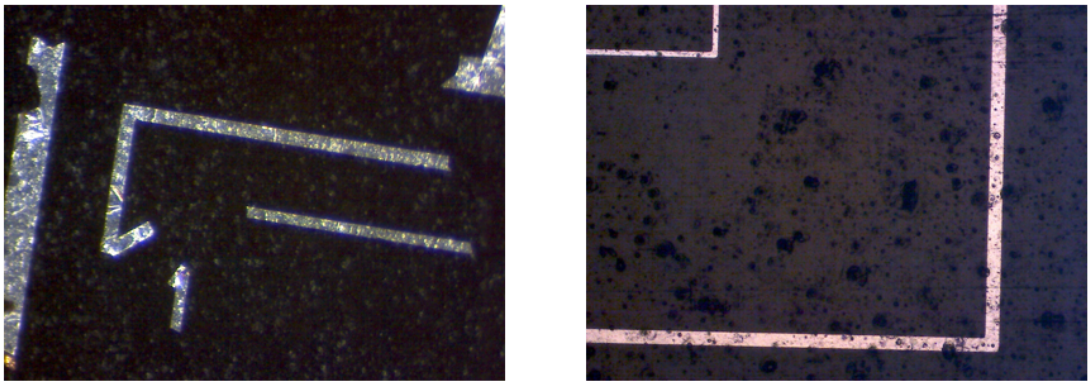

Figure 3.7: Early metal adhesion tests: (left) Metal tended to peel away before we used lift-off-resist in our photo-lithography process. (right) After using LOR, the traces were well defined but the topography and surface roughness of the epoxy caused challenges for connectivity.

To address this issue, we developed a two-step photolithography process using LOR and SH1818. This solved our metal to epoxy adhesion problem, but the problem of epoxy surface roughness remained (Figure 3.7b). Adding a passivation layer then created a more conformal surface, but aluminum alone does adhere well to SU-8. Thus, our final process for adhering metal to the substrate is to use a dual-metal sputter process. We start by sputtering a very thin layer of chromium (10 to 20 nm), which adheres to SU-8 much better than aluminum, onto the substrate, followed by a thicker layer of aluminum (greater than 200 nm.) We use this dual

metal process, as opposed to just using chromium alone, because chromium has much greater resistivity than aluminum (Cr = 13 x $10^8$ ohm $m^2/m$, Al = 2.65 x $10^8$ ohm $m^2/m$.)

### 3.2.5 Integration of planar fluidic delivery

To create a successful biosensor, fluid channels need to be added on top of an existing IC sensor encapsulated using EMC. We developed two different methods for applying microfluidic channels over the embedded IC sensors. The first method was to laser cut a double sided pressure sensitive adhesive (PSA) and acrylic cover to create the channels [33]. This was faster and easier to produce than the second method, but the channel sizes were much larger than traditional microfluidics. The second method uses a more traditional photolithography processes. This allows for smaller and more precise fluidic channels, but it is more time consuming and difficult to produce. Size comparison of microfluidic channelsn is shown in Figure 3.8.

#### 3.2.5.1 Laser-cut fluid channels

A method for building laser-cut channels was initially developed by two students at Oregon State University, Kevin Bishop and Megan Co. A laser-cut, double-sided adhesive sheet (3M 9474LE) is used to form fluid channel walls. After channel layout using open-source CAD software, patterns are cut out of the adhesive sheet

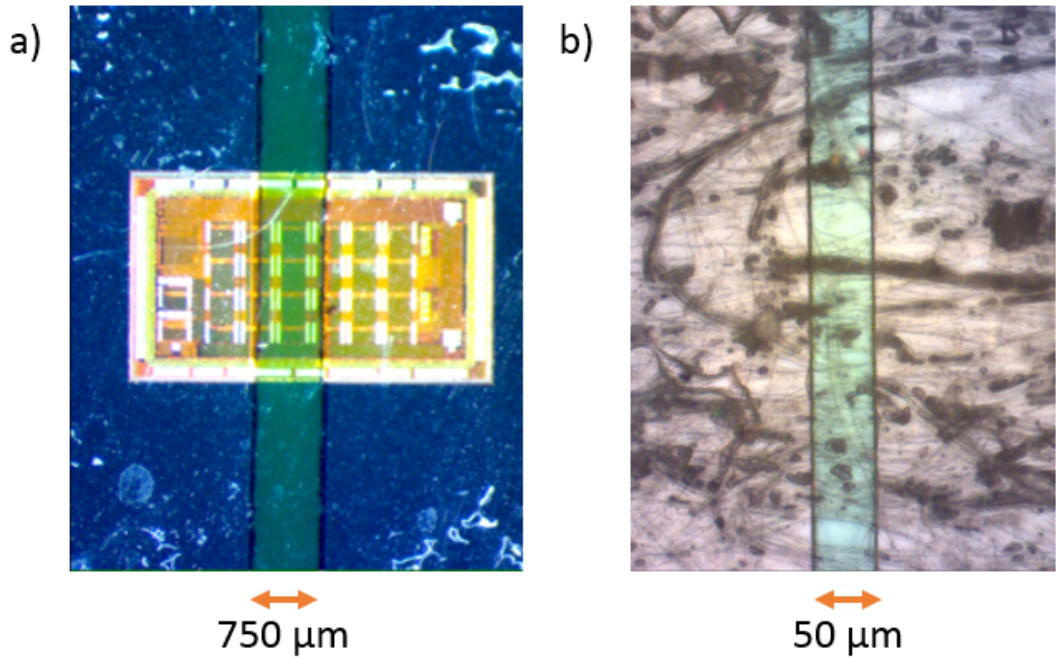


Figure 3.8: Size comparison of microfluidic channels: (A) Laser cut channels are fast and fast to produce, the narrowest channels are 750 $\mu$m wide and 170 $\mu$m tall. (B) Microfluidics created in SU-8 have been as small as 20 $\mu$m but the adhesive cover is not optically transparent.

using a consumer, bench-top laser cutter. For standalone fluidic devices, cutouts are placed on top of an acrylic or glass substrate, which forms the channel floor; a second acrylic piece is laser-cut with holes at each fluid entrance and exit point and placed on top of the adhesive sheet. Using this method we have demonstrated leak-free fluid channels with a minimum 750 $\mu$m width; channel height is defined by the sheet thickness of the pressure-sensitive adhesive (170 $\mu$m). Finally, adhesive tubing adaptors are placed over the access holes to allow fluid injection or removal via syringe. A complete standalone device is shown in Figure 3.9a-b. This method

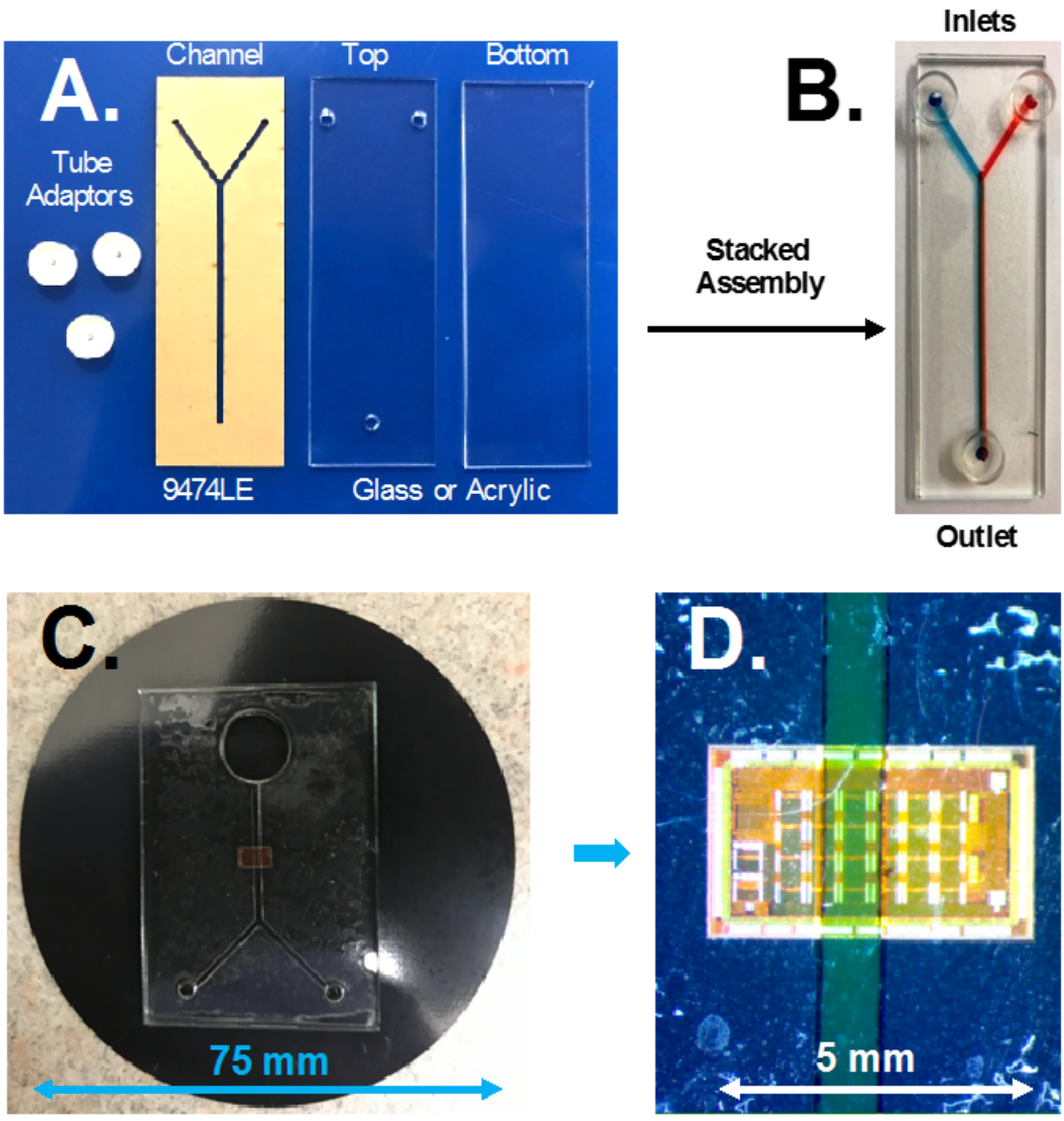


Figure 3.9: Laser-cut adhesive tapes and acrylic sheets (a) are aligned to form laminated fluidic devices. (b) By using a bare IC embedded in an EMC wafer using FOWLP as the bottom substrate, a channel can be rapidly fabricated above a sensor IC for fluid delivery to the chip (c-d).

can also be extended to multi-layer devices and 3D fluidic paths using aligned holes as fluidic vias. Laser-cut fluidic overlays were fabricated to demonstrate liquid routing to ICs embedded in EMC wafers. A typical device is shown in Figure 3.9c, where a 1 mm fluid channel is routed across a 3 x 5 $mm^2$ CMOS die; the device includes a Y-channel inlet and a collection reservoir at the output. Dye solution is injected into the channel to demonstrate leak-free operation (Figure 3.9d).

#### 3.2.5.2 Patterned SU-8 fluid channels

The SU-8 process used to define microfluidic channels requires the same preparation as any structural SU-8 layer. The substrate is put into a oxygen plasma ash for 1 minute and dehydrated for at least 10 minutes at 95° C. Different depths of the channels can be obtained by using different thicknesses of SU-8. SU-8 2025 will create channels of approximately 25 $\mu$m deep and SU-8 2050 will be approximately 50 $\mu$m. The desired SU-8 is spun on the the prepared substrate and soft baked to start the hardening process. The prepared coupon is then exposed to UV light through a custom mask with the desired microfluidic design and put through a post-exposure bake and then developed and cured.

The greatest benefit of this method is that, like all photo lithography processes, there is a greater level of accuracy and resolution that can be obtained as to the width and positioning of the channels with respect to the underlying sensors. It is possible to place channels as small as the resolution of the SU-8. We have

developed channels ranging from 100 $\mu$m to 20$\mu$m in width, in both 50 $\mu$m and 25 $\mu$m SU8 (Figure 3.10.)

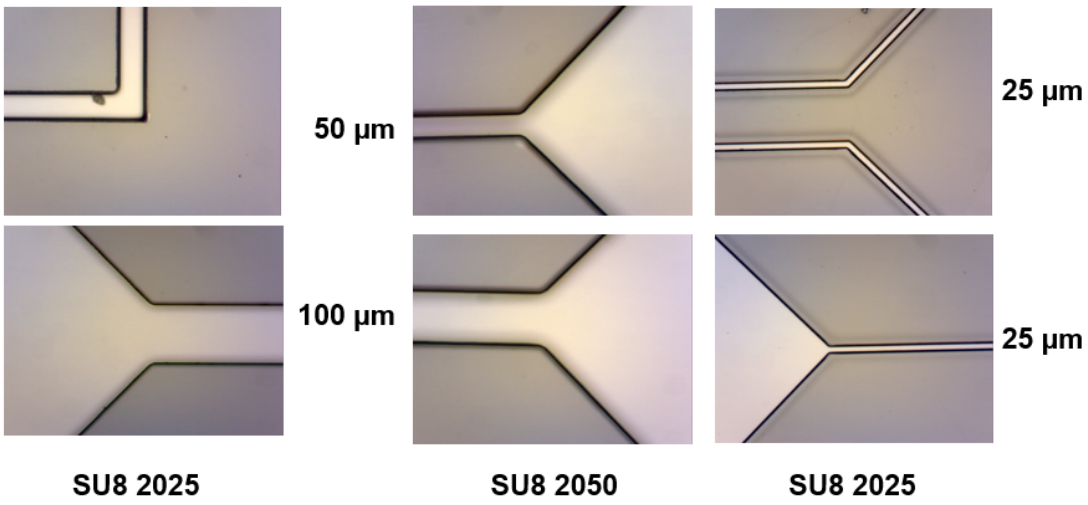


Figure 3.10: Microfluidic channels were fabricated in channel widths ranging from 20 to 100 $\mu$m and heights of 50 or 100 $\mu$m depending on the type of SU-8.

The final step is to put a lid on the open SU-8 channels, which is done by adhering a thin, double-sided pressure sensitive adhesive, which has been laser-cut with holes for the inlet and outlet, to a clean mylar sheet. Holes are then added to the mylar where the inlets and outlets are needed. This flexible cover can then be applied on top of the SU-8 channels, and adhesive tubing adapters are placed over the access holes.

# Chapter 4: Experiments using FOWLP-integrated ICs and fluidics

The experimental procedure for all of the experiments that follow uses the same general process: the prepared IC-encapsulated wafer was aligned on an enclosed probe station and connected to a parameter analyzer (HP4156B) using needle probes to connect to the metallized pads, discussed in Section 3.2.3. To determine proper diode function, which was performed before each experiment, we biased the photodiodes at voltage ranges from -13 to 2 volts, measured in steps of 0.25 mV; we limited the current through the diodes to $\pm 10\mu$A. This test allows us to see both the forward and reverse breakdown voltages, as seen in Figure 4.1. Once we

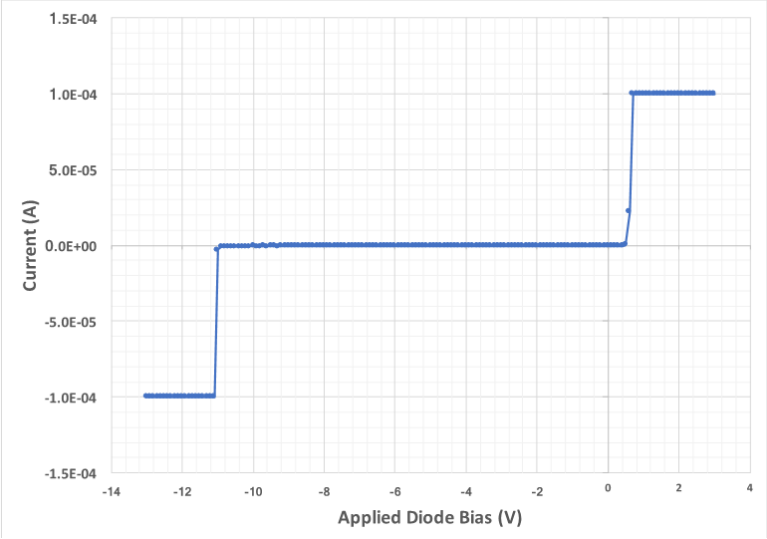


Figure 4.1: The photodiodes were found to have the forward and reverse bias curves at the same voltages as a chip that was not embedded in an epoxy wafer.

can confirm proper diode function, we adjust the measurement range to from -9 to 0 volts. At this time we also adjust the light source for the type of test we are performing. The light source differences are as follows:

- Metallization Tests - No light source change made. Microscope light used to measure current through photodiode at the given voltage ranges.
- Optical Transmission using Dye Solution – The microscope light is used but the intensity is reduced to the first marker on the light control box. We do this to prevent saturating the diode in our tests. We also close the probe station cabinet to minimize extraneous light sources.
- Optical Detection using Quantum Dots –Microscope light is turned off and UV light source is placed inside of a closed cabinet to illuminate the Q-dots (description of Q-dots in Section 4.3)

For the optical tests, measurements were performed, followed by a DI water rinse and an air dry of the channel before the next measurement is taken. Samples are introduced to the fluidic channels via a syringe pump and small tube. The epoxy disks and light source are not changed or moved in between measurements. Each measurement is made in as close to identical environment as possible.

## 4.1 Metallization validation

The first set of experiments we conducted were to determine if connection could be made to chips embedded in the substrate to verify continuity, impedance of the

traces, and the condition of the sensors (or other devices) after the encapsulation process. For these experiments, we used an array of CMOS-integrated photodiodes as the device under test. Following over-molding of the bare ICs, these experiments were intended to verify that the CMOS devices still worked as photodiodes, and that they could be measured remotely using the deposited electrical re-distribution.

### 4.1.1 Single-chip metallization

The initial test was with a single chip embedded in the epoxy wafer. We processed the chips using our stack up procedure, described in Section 3.1, up through the lift-off step (i.e. we did not put the microfluidics on top). While all of the diodes are functional, being able to probe multiple diodes provided redundancy. Electrical contacts were made to multiple diodes on the chip (Figure 4.2a). Using a parameter

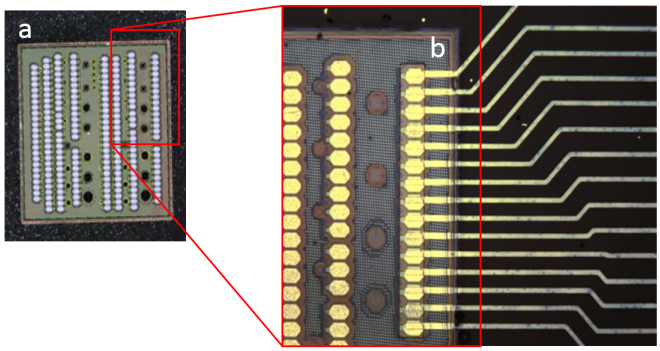


Figure 4.2: Fanout of metalized traces on a CMOS chip array of photo diodes. (a) Image of the bare photodiode array embedded in over-molded epoxy. (b) Traces were taken from both sides of the chip in a FOWLP process. Improved connectivity yield was found in traces from larger continuous openings in the passivation layer.

analyzer (HP4156B) we measured various photodiodes (Figure 4.2b). The light of

the probe station was left on to provide a light source for the diodes. Results from embedded, metalized CMOS photodiodes can be summarized as follows:

- Larger openings in the passivation layer provide better, more consistent contact over the ledge features. This may be due to insufficient access to fresh developer in the smaller cavities, which could be solved with a different development apparatus. Alternately, it could be caused by over exposure to the smaller details.

- The traces do not provide a substantial source of impedance in the lengths available, and can be decreased using thicker and wider traces.

- 2 $\mu$m of passivation proved to be more effective than the previously used 5 $\mu$m. The 2 $\mu$m was tall enough to smooth the rough surface of the epoxy and created smaller ledges where metallization needed to connect to the pads.

- Making the spacing between the traces larger (greater than 50$\mu$m) makes lift off easier and cleaner.

In summary, the established process for encapsulation of CMOS ICs, passivation, patterning, and metallization is successful.

### 4.1.2 Multiple-chip metalization

After demonstrating a reliable process for single chip metallization, we extend the process to demonstrate multiple chips interconnected on a single substrate. The

process for the layer stack was the same, with an initial passivation layer followed by planar metallization. For this demonstration, the metallization (Figure 4.3a) crosses the entire chip and connects to bond pads of a second embedded photodiode IC. We connected to four photo diodes on the two chips, two of the same device

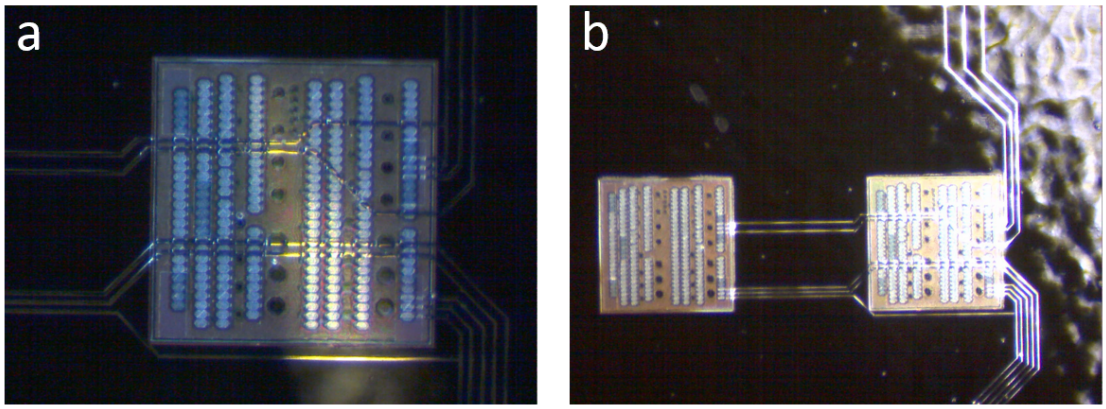


Figure 4.3: Two chips embedded in epoxy substrate. Four diodes, two from each chip, are traced out. (a) The metal traces go across the chip on top of the SU-8 passivation, so as not to interfere with any other part of the chip. (b) The traces start on one chip travel across the second then move away from the chip to probe points.

from each chip. The first two chips shared a common base connection but the N-wells and P-wells were traced out to separate pads. An example measured I-V curve from a connected photodiode is shown in Figure 4.4a. In Figure 4.3b, a pair of photodiodes is measured that shared common contacts for the base and P-well connections, and separate contacts for the two N-wells. Thus with three contacts (rather than six), we could measure the reverse bias on the two separate diodes (Figure 4.4b). The success of this experiment shows that the placement of the chips in the compression molded epoxy is within tolerances of our being able to

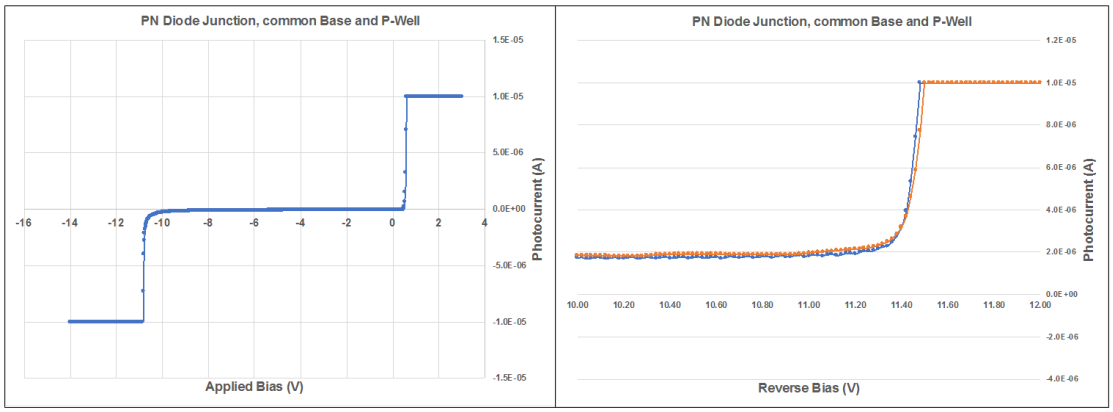


Figure 4.4: Bias measurements made to multi-chip photodiode chips (a) Bias measurement made on individually connected photodiode. (b) Reverse bias measurement of diodes with common bases and P-wells.

accurately route to the chips with a single, fixed photo mask.

## 4.2 Optical Transmission

We conducted a set of optical transmission experiments to demonstrate the fully-integrated combination of FOWLP-integrated sensor IC, planar RDL metallization, and laser-cut microfluidic overlay. The over-molded CMOS substrate contains an array of photodiode structures, and photo-current is measured under reverse bias. A microfluidic channel was placed over a row of contacted photodiodes (Figure 4.5). The photodiodes, located in the floor of the channel, were used to measure optical transmittance through clear and dyed solutions.

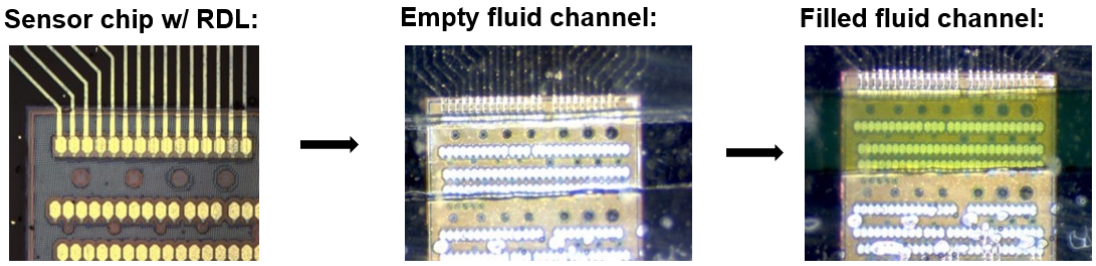


Figure 4.5: Laser-cut microfluidic overlay: (left) Co-planar encapsulated photodiode array IC with FOWLP connections to on-chip pads. (center) Prepared substrate with (empty) laser cut microfluidic channel. (right) Prepared substrate with die filled microfluidic channel.

### 4.2.1 Optical transmission through dye solution

To demonstrate the ability to detect light transmission through a dyed liquid, we start by getting a baseline measurement through an empty channel. We took five measurements (of each state) to confirm that the results were reproducible. We then measured the channel filled with DI water and found that results were essentially the same as the empty channel. Finally, we measured the channel filled with a dye solution; the averaged results are found in Figure 4.6.

### 4.2.2 Optical transmission using dye dilution series

To demonstrate broad utility of the hybrid integrated method for bioassay and lab-on-chip applications, we measured optical transmission across a broad dilution series. A dye solution was prepared that mimics the absorption spectrum of 2,2'-azino-bis(3-ethylbenzothiazoline-6-sulphonic acid) (ABTS), a common chromogenic substrate used in peroxidase-based immunoassays. A two-fold serial dilu-

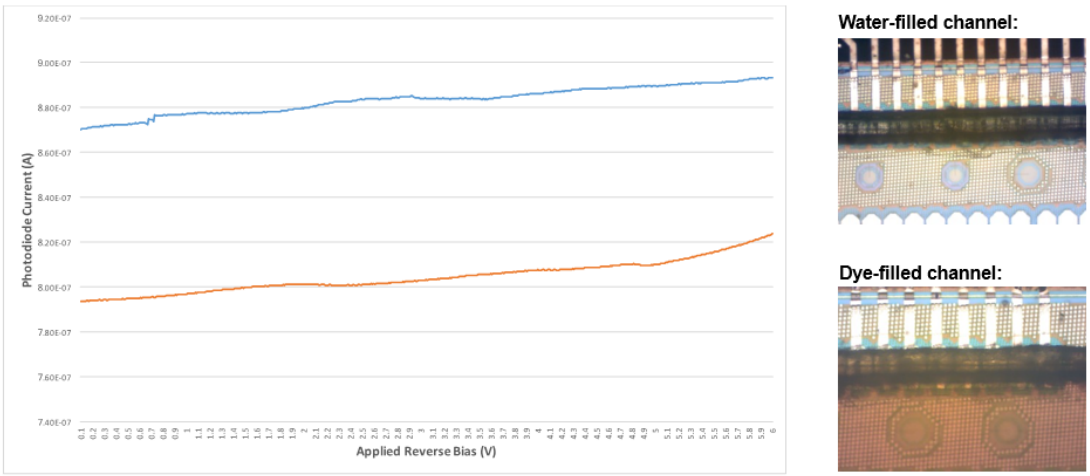


Figure 4.6: Measured IC photodiode current when illuminated through clear and tinted liquids under high illumination.

tion was performed to produce a sample set with a concentration range of 100% down to 0.01%; a subset is visible in the inset of Figure 4.7. A reverse bias of approximately 5.5 V was applied to each photodiode, and photocurrent was recorded using a parameter analyzer (HP4156B). Each dye sample was injected into the fluid channel. To minimize cross-contamination, the channel was flushed with deionized water and air between samples. Deionized water was used to established baseline transmission, followed by increasingly concentrated dye samples. The experiment was performed on a probe station using a white light source for illumination, and absorption of the dye samples was concurrently measured at 405 nm using a plate reader for reference. Photocurrent measurements from a CMOS-integrated photodiode across the full dilution series are shown in Figure 4.7.

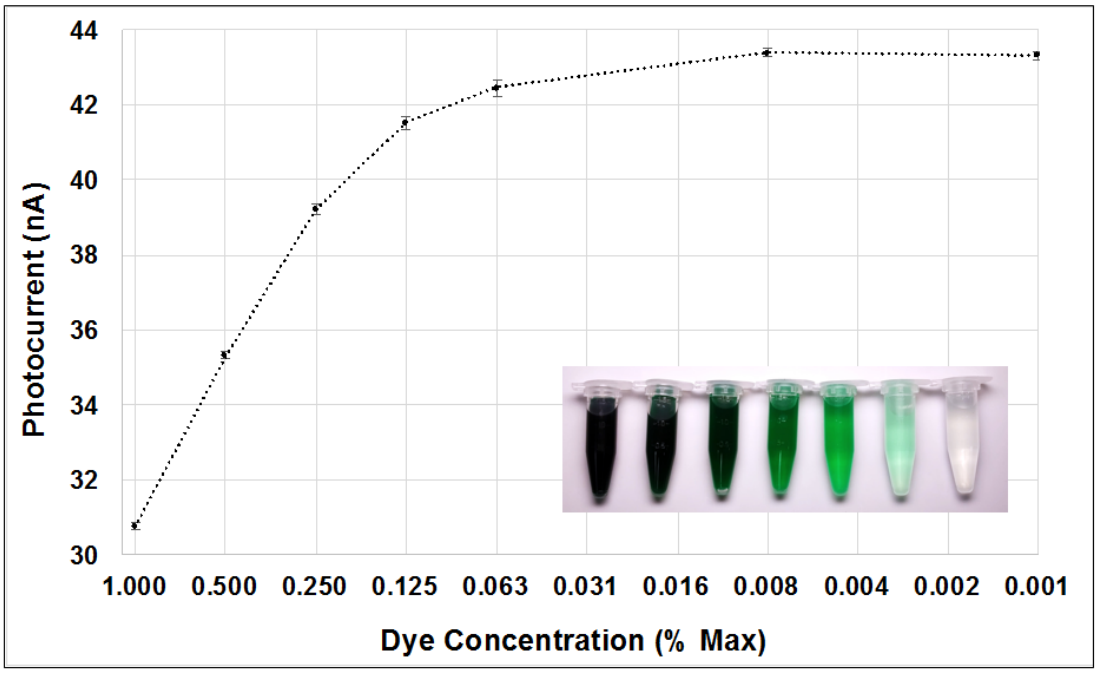


Figure 4.7: Measured IC photocurrent using a serial dilution series to measure optical transmission across a broad range of opacity for use in chromogenic immunoassays.

## 4.3 Optical detection using quantum dots

To further assess the potential of this set up to be used for bioassay quantification, optical experiments were performed using a solution containing quantum dots. Quantum dots (Q-dots) are nano-sized crystal semiconductor particles which have composition and size-dependent absorption and emission [34]. The particular dots we obtained absorb UV light and emit yellow light.

The photodiodes used in our experiments have a low sensitivity to light emitted in the UV range (300 - 350 nm). We can therefore expose the diodes to a UV source

and have minimal photocurrent going through the diode. For the optical detection experiment, we used the same setup as the transmission experiment, with the only difference being the light source used. A broad-spectrum UV illuminator was used for excitation in place of a white light source. A Q-dot solution was obtained that is a 1 gram of Q-dots in 1 ml of water. This was diluted to a 50% and 25% solution. In the past few years, Q-dots have been used successfully in immunofluorescence assays, DNA labeling, and cell biology [35].

Initial measurements were taken from the photo-diode without light and without liquid in the channel, to establish a baseline. All further measurements were taken with the UV light source on. We measured an empty channel and a channel injected with deionized water for reference. Each concentration of Q-dot was measured with the channel flushed with deionized water and air in between, to minimize cross contamination. A deionized water measurement was taken in between each sample, and results are shown in Figure 4.8.

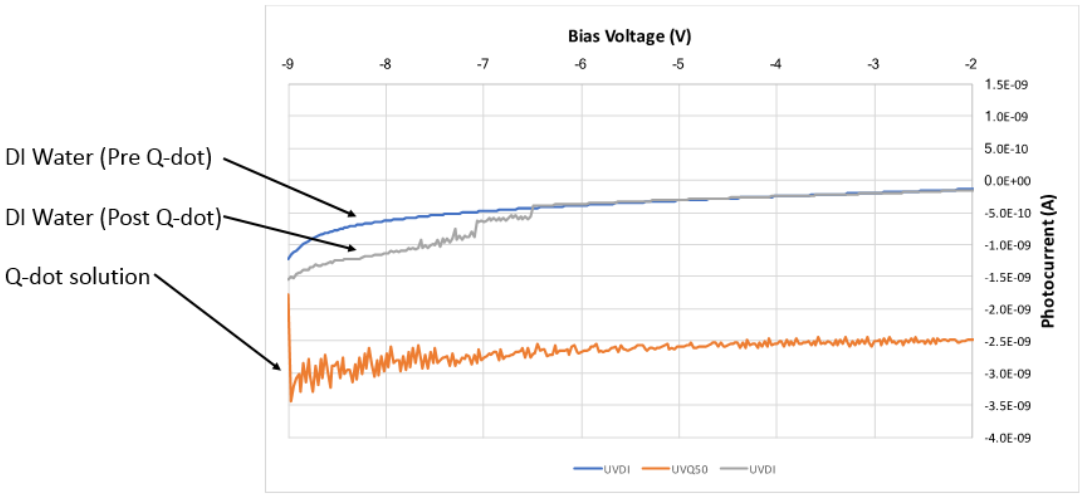


Figure 4.8: Optical detection using quantum dots. An increase of (negative) current was detected when 50% Q-dot solution was passed through the fluidic channels and excited by UV light.

# Chapter 5: Future Work

The work presented in this thesis represents a developed and repeatable processes for delivering a fluid to an IC-integrated sensor in an efficient and cost-effective manner. There is a long way to go to develop a true lab-on-a-chip device, but this work represents a comprehensive and scalable approach to a predominate integration hurdle. In this section we present a list of proposed future research based on this work:

1. We have a developed a viable reproducible method of patterning and metallizing multiple ICs embedded in compression-molded epoxy. In this process, we have added one additional routing layer to what was existing on the IC. It is often impossible to properly connect two (or more) chips together using a single routing layer. The next logical step is to develop a process to have multiple layers of patterned metallization on the prepared substrate to create true electrical networks.

2. In addition to laser-cut microfluidic devices, we have developed a process using SU-8 to create monolithic microfluidic channels. This process allows us to pattern small, micron-scale controlled channels. This work can also be combined with our laser-cut microfluidic channels to create multi-layer microfluidics.

3. We have embedded two sensor chips in a single substrate, and we have shown they can be connected. The next step is to combine a sensor chip with the necessary amplifiers and logic to collect (and possibly transmit) data directly from the integrated multi-chip device.

4. All of the microfluidic devices we have completed in SU-8 have been single channel systems, one path from input to output. Further development needs to be done with the SU-8 to create multi-path systems, for example two inputs, one output

5. Performing a more definitive bio-assay using the current processes and tools.

# Chapter 6: Conclusion

In this work, we have presented a highly scalable approach for the co-planar integration of CMOS integrated circuits using a fan-out-wafer-level-packaging technique, with integrated microfluidic sample delivery. By using the compression molded ICs as the basis for this work, we were able to form a near-seamless planar substrate. Metal interconnects were patterned, connected to multiple chips on the same substrate, and two methods of fabricating fluidics on this substrate were demonstrated. The rapid laser-cut fabrication was used for prototyping, and SU-8 microfluidic channels were developed as a more precise and accurate method of transporting fluids. We presented results for our development of the FOWLP process for both single and multi-chip IC. We also presented results for optical transmission experiments and an optical detection experiment using quantum dots with CMOS-integrated photodetectors.

This work demonstrates the applicability of the hybrid approach to lab-on-chip measurement of chromogenic assay chemistries, and can be extended to include additional electrical or optical sensors, logic, or communication hardware. The planar IC-EMC approach enables a broad spectrum of scalable lab-on-chip application devices that can be re-configurable, where a library of sensors, controllers, logic ICs, or transmitters can be arranged and developed on over-molded substrates with incorporated microfluidic sample delivery.

## 6.1 List of Contributions.

- New scalable method of integrating microfluidics and integrated circuits.
- Demonstrated measured light transmission and light emission through a fluidic channel using FOWLP.
- Published demonstration of co-planar integration of integrated circuits and microfluidics in IEEE BioCAS 2017 [36].

# Bibliography

[1] A. Manickam, A. Chevalier, M. McDermott, A. D. Ellington, and A. Hassibi, "A CMOS Electrochemical Impedance Spectroscopy (EIS) Biosensor Array," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 4, no. 6, pp. 379–390, dec 2010. [Online]. Available: http://www.ncbi.nlm.nih.gov/pubmed/23850755 http://ieeexplore.ieee.org/document/5625928/

[2] P. M. Levine, P. Gong, R. Levicky, and K. L. Shepard, "Real-time, multiplexed electrochemical DNA detection using an active complementary metal-oxide-semiconductor biosensor array with integrated sensor electronics," *Biosensors and Bioelectronics*, vol. 24, no. 7, pp. 1995–2001, mar 2009. [Online]. Available: http://www.ncbi.nlm.nih.gov/pubmed/19054661 http://www.pubmedcentral.nih.gov/articlerender.fcgi?artid=PMC2735726 http://linkinghub.elsevier.com/retrieve/pii/S0956566308005836

[3] T. Datta-Chaudhuri, P. Abshire, and E. Smela, "Packaging commercial CMOS chips for lab on a chip integration," *Lab on a Chip*, vol. 14, no. 10, p. 1753, apr 2014. [Online]. Available: http://xlink.rsc.org/?DOI=c4lc00135d

[4] D. L. Bellin, H. Sakhtah, J. K. Rosenstein, P. M. Levine, J. Thimot, K. Emmett, L. E. P. Dietrich, and K. L. Shepard, "Integrated circuit-based electrochemical sensor for spatially resolved detection of redox-active metabolites in biofilms," *Nature Communications*, vol. 5, p. 3256, feb 2014. [Online]. Available: http://www.ncbi.nlm.nih.gov/pubmed/24510163 http://www.pubmedcentral.nih.gov/articlerender.fcgi?artid=PMC3969851 http://www.nature.com/doifinder/10.1038/ncomms4256

[5] D. A. Hall, R. S. Gaster, K. Makinwa, S. X. Wang, and B. Murmann, "A 256 pixel magnetoresistive biosensor microarray in 0.18$\mu$m CMOS." *IEEE journal of solid-state circuits*, vol. 48, no. 5, pp. 1290–1301, may 2013. [Online]. Available: http://www.ncbi.nlm.nih.gov/pubmed/24761029 http://www.pubmedcentral.nih.gov/articlerender.fcgi?artid=PMC3993911

[6] H. Wang, A. Alborz Mahdavi, c. A. David Tirrell, and A. Hajimiri, "A magnetic cell-based sensor." *Lab on a chip*, vol. 12, no. 21, pp. 4465–71, 2012.

[7] H. Lee, Y. Liu, D. Ham, and R. M. Westervelt, "Integrated cell manipulation system–CMOS/microfluidic hybrid." *Lab on a chip*, vol. 7, no. 3, pp. 331–7, mar 2007. [Online]. Available: http://www.ncbi.nlm.nih.gov/pubmed/17330164

[8] M. L. Johnston, I. Kymissis, and K. L. Shepard, "FBAR-CMOS Oscillator Array for Mass-Sensing Applications," *IEEE SENSORS JOURNAL*, vol. 10, no. 6, 2010. [Online]. Available: https://www.bioee.ee.columbia.edu/downloads/2010/2010_Johnston_Sensors_Journal_IEEE

[9] M. L. Johnston, H. Edrees, I. Kymissis, and K. L. Shepard, "Integrated VOC vapor sensing on FBAR-CMOS array," in *2012 IEEE 25th International Conference on Micro Electro Mechanical Systems (MEMS)*. IEEE, jan 2012, pp. 846–849. [Online]. Available: http://ieeexplore.ieee.org/document/6170318/

[10] J. K. Rosenstein, M. Wanunu, C. A. Merchant, M. Drndic, and K. L. Shepard, "Integrated nanopore sensing platform with sub-microsecond temporal resolution," *Nature Methods*, vol. 9, no. 5, pp. 487–492, mar 2012. [Online]. Available: http://www.ncbi.nlm.nih.gov/pubmed/22426489 http://www.pubmedcentral.nih.gov/articlerender.fcgi?artid=PMC3648419 http://www.nature.com/doifinder/10.1038/nmeth.1932

[11] D. Zhang, L. Men, and Q. Chen, "Microfabrication and Applications of Opto-Microfluidic Sensors," *Sensors*, vol. 11, no. 12, pp. 5360–5382, may 2011. [Online]. Available: http://www.ncbi.nlm.nih.gov/pubmed/22163904 http://www.pubmedcentral.nih.gov/articlerender.fcgi?artid=PMC3231365 http://www.mdpi.com/1424-8220/11/5/5360/

[12] H. Ji, D. Sander, A. Haas, and P. A. Abshire, "Contact Imaging: Simulation and Experiment," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 8, pp. 1698–1710, aug 2007. [Online]. Available: http://ieeexplore.ieee.org/document/4282078/

[13] K. A. Al Mamun, S. K. Islam, D. K. Hensley, and N. McFarlane, "A Glucose Biosensor Using CMOS Potentiostat and Vertically Aligned Carbon Nanofibers," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 10, no. 4, pp. 807–816, aug 2016. [Online]. Available: http://ieeexplore.ieee.org/document/7497511/

[14] D. Mark, S. Haeberle, G. Roth, F. von Stetten, and R. Zengerle, "Microfluidic lab-on-a-chip platforms: requirements, characteristics and applications," *Chemical Society Reviews*, vol. 39, no. 3, p. 1153, 2010. [Online]. Available: http://xlink.rsc.org/?DOI=b820557b

[15] A. Rasmussen, M. Gaitan, L. E. Locascio, and M. E. Zaghloul, "Fabrication Techniques to Realize CMOS-Compatible Microfluidic Microchannels," *Journal of Microelectromechanical Systems*, vol. 10, no. 2, 2001. [Online]. Available: https://www.nist.gov/publications/fabrication-techniques-realize-cmos-compatible-microfluidic-microchannels

[16] G. M. Whitesides, "The origins and the future of microfluidics," *Nature*, vol. 442, no. 7101, pp. 368–373, jul 2006. [Online]. Available: http://www.nature.com/doifinder/10.1038/nature05058

[17] J. M. Rothberg, W. Hinz, T. M. Rearick, J. Schultz, W. Mileski, M. Davey, J. H. Leamon, K. Johnson, M. J. Milgrew, M. Edwards, J. Hoon, J. F. Simons, D. Marran, J. W. Myers, J. F. Davidson, A. Branting, J. R. Nobile, B. P. Puc, D. Light, T. A. Clark, M. Huber, J. T. Branciforte, I. B. Stoner, S. E. Cawley, M. Lyons, Y. Fu, N. Homer, M. Sedova, X. Miao, B. Reed, J. Sabina, E. Feierstein, M. Schorn, M. Alanjary, E. Dimalanta, D. Dressman, R. Kasinskas, T. Sokolsky, J. A. Fidanza, E. Namsaraev, K. J. Mckernan, A. Williams, G. T. Roth, and J. Bustillo, "An integrated semiconductor device enabling non-optical genome sequencing," *Nature*, vol. 475, 2011.

[18] I. Rennie, H. Keen, and A. Southon, "A RAPID ENZYME-STRIP METHOD FOR ESTIMATING BLOOD-SUGAR," *The Lancet*, vol. 284, no. 7365, pp. 884–886, oct 1964. [Online]. Available: http://linkinghub.elsevier.com/retrieve/pii/S0140673664907408

[19] Y. J. Huang, C. W. Huang, T. H. Lin, C. T. Lin, L. G. Chen, P. Y. Hsiao, B. R. Wu, H. T. Hsueh, B. J. Kuo, H. H. Tsai, H. H. Liao, Y. Z. Juang, C. K. Wang, and S. S. Lu, "A CMOS cantilever-based label-free DNA SoC with improved sensitivity for hepatitis B virus detection," *IEEE Transactions on Biomedical Circuits and Systems*, 2013.

[20] D. Nagel and M. Zaghloul, "MEMS: micro technology, mega impact," *IEEE Circuits and Devices Magazine*, vol. 17, no. 2, pp. 14–25, mar 2001. [Online]. Available: http://ieeexplore.ieee.org/document/920875/

[21] N. Haandbæk, O. With, S. C. Bürgel, F. Heer, and A. Hierlemann, "Lab on a Chip Resonance-enhanced microfluidic impedance cytometer for detection of single bacteria," *Lab on a Chip*, vol. 14, pp. 3313–3324, 2014.

[22] N. Haandbæk, S. C. Bürgel, F. Heer, and A. Hierlemann, "Characterization of subcellular morphology of single yeast cells using high frequency microfluidic impedance cytometer," *Lab Chip*, 2014.

[23] M. Muluneh and D. Issadore, "A multi-scale PDMS fabrication strategy to bridge the size mismatch between integrated circuits and microfluidics." *Lab on a chip*, vol. 14, no. 23, pp. 4552–8, dec 2014. [Online]. Available: http://www.ncbi.nlm.nih.gov/pubmed/25284502 http://www.pubmedcentral.nih.gov/articlerender.fcgi?artid=PMC4418800

[24] R. Singh and L. Leng, "A hybrid CMOS-microfluidic contact imaging microsystem," *SPIE*, 2009. [Online]. Available: http://www.eecg.toronto.edu/ roman/professional/pubs/pdfs/spie09_imager.pdf http://proceedings.spiedigitallibrary.org/proceeding.aspx?articleid=784702

[25] D. Welch and J. B. Christen, "Seamless integration of CMOS and microfluidics using flip chip bonding," *Journal of Micromechanics and Microengineering*, vol. 23, no. 3, p. 035009, mar 2013. [Online]. Available: http://stacks.iop.org/0960-1317/23/i=3/a=035009?key=crossref.d918b47bb1e642b5f38277bad4770285

[26] B. Zhang, Q. Dong, C. E. Korman, Z. Li, and M. E. Zaghloul, "Flexible packaging of solid-state integrated circuit chips with elastomeric microfluidics," *Scientific Reports*, vol. 3, no. 1, p. 1098, dec 2013. [Online]. Available: http://www.nature.com/articles/srep01098

[27] H. Norian, R. M. Field, I. Kymissis, and K. L. Shepard, "An integrated CMOS quantitative-polymerase-chain-reaction lab-on-chip for point-of-care diagnostics." *Lab on a chip*, vol. 14, no. 20, pp. 4076–84, oct 2014. [Online]. Available: http://www.ncbi.nlm.nih.gov/pubmed/25177916

[28] Y. Huang and A. J. Mason, "Lab-on-CMOS integration of microfluidics and electrochemical sensors," *Lab on a Chip*, vol. 13, no. 19, p. 3929, oct 2013. [Online]. Available: http://www.ncbi.nlm.nih.gov/pubmed/23939616

http://www.pubmedcentral.nih.gov/articlerender.fcgi?artid=PMC3793889
http://xlink.rsc.org/?DOI=c3lc50437a

[29] A. Uddin, K. Milaninia, C.-H. Chen, and L. Theogarajan, "Wafer Scale Integration of CMOS Chips for Biomedical Applications via Self-Aligned Masking," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 1, no. 12, pp. 1996–2004, dec 2011. [Online]. Available: http://ieeexplore.ieee.org/document/6119120/

[30] S.-S. Li and C.-M. Cheng, "Analogy among microfluidics, micromechanics, and microelectronics," *Lab on a Chip*, vol. 13, no. 19, p. 3782, oct 2013. [Online]. Available: http://www.ncbi.nlm.nih.gov/pubmed/23963526 http://xlink.rsc.org/?DOI=c3lc50732g

[31] T. Brettschneider, C. Dorrer, M. Bründel, R. Zengerle, and M. Daub, "Wafer-level packaging and laser bonding as an approach for silicon-into-lab-on-chip integration," *Journal of Micromechanics and Microengineering*, vol. 23, no. 5, p. 055005, may 2013. [Online]. Available: http://stacks.iop.org/0960-1317/23/i=5/a=055005?key=crossref.6965328c020194128b7281ce7474dd3d

[32] T. Meyer, G. Ofner, S. Bradl, M. Brunnbauer, and R. Hagen, "Embedded Wafer Level Ball Grid Array (eWLB)," in *2008 10th Electronics Packaging Technology Conference*. IEEE, dec 2008, pp. 994–998. [Online]. Available: http://ieeexplore.ieee.org/document/4763559/

[33] D. Patko, Z. Mártonfalvi, B. Kovacs, F. Vonderviszt, M. Kellermayer, and R. Horvath, "Microfluidic channels laser-cut in thin double-sided tapes: Cost-effective biocompatible fluidics in minutes from design to final integration with optical biochips," *Sensors and Actuators B: Chemical*, vol. 196, pp. 352–356, jun 2014. [Online]. Available: http://linkinghub.elsevier.com/retrieve/pii/S0925400514001324

[34] X. Michalet, F. F. Pinaud, L. A. Bentolila, J. M. Tsay, S. Doose, J. J. Li, G. Sundaresan, A. M. Wu, S. S. Gambhir, and S. Weiss, "Quantum Dots for Live Cells, in Vivo Imaging, and Diagnostics," *Science*, vol. 307, no. 5709, pp. 538–544, jan 2005. [Online]. Available: http://www.ncbi.nlm.nih.gov/pubmed/15681376 http://www.pubmedcentral.nih.gov/articlerender.fcgi?artid=PMC1201471 http://www.sciencemag.org/cgi/doi/10.1126/science.1104274

[35] P. Alivisatos, "The use of nanocrystals in biological detection," *Nature Biotechnology*, vol. 22, no. 1, pp. 47–52, jan 2004. [Online]. Available: http://www.ncbi.nlm.nih.gov/pubmed/14704706 http://www.nature.com/doifinder/10.1038/nbt927

[36] M. Lindsay, S. Sengupta, K. Bishop, M. Co, C.-H. Chen, M. Cumbie, and M. L. Johnston, "Scalable Hybrid Integration of CMOS Circuits and Fluidic Networks for Biosensor Applications," *IEEE BioCASS*, 2017, accepted.