

AN ABSTRACT OF THE THESIS OF

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Title: A Fully Integrated Bio-potential Low-noise Amplifier Utilizing Capacitor Multipliers.

Abstract approved:

David J. Allstot

In any biomedical signal acquisition system, a front-end amplifier is needed to amplify low amplitude bio-signals while filtering out any unwanted low-frequency artifacts. The design of low frequency poles within the sub-Hz range implies very large time-constants which goes against system integrability. In recent years, the pseudo resistor has been used to provide very large on-chip resistance to achieve sub-Hz pole frequency. However, the pseudo resistor behaves poorly across PVT variations and is highly non-linear which makes the low-frequency pole unpredictable.

In this thesis, a bio-LNA utilizing a differential difference amplifier structure along with gm-C filters is examined. The differential topology provides high CMRR while the negative feedback through the gm-C filter provides the low-frequency pole. A capacitor multiplier is also implemented to achieve a very high value effective on-chip capacitance. The functionality of the bio-LNA is validated through simulations in Cadence.

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A Fully Integrated Bio-potential Low-noise Amplifier Utilizing Capacitor Multipliers

by
OnnLim Yong

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OnnLim Yong, Author

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1 Introduction

1.1 Biomedical Signals

Biomedical signals are information-bearing signals that emanate from biological organisms. These signals shed light on the underlying biological and physiological processes that occur within the living organism. Amongst the many types of biomedical signals, the bioelectric signal can be measured through changes in electrical potential across a cell or an organ. These changes in action potential can be measured on the surface of the skin with electrodes which converts the ionic flow of currents in the biological tissue to the electronic flow of current in the amplifier. The fact that our muscles and nerves are stimulated by electrical signals makes the bioelectric signal the most widely used signal in most fields of biomedicine [1].

The three most common bioelectric signals are the electrocardiogram (ECG/EKG), the electromyogram (EMG) and the electroencephalogram (EEG). The ECG measures is the electrical activity of the cardiac muscles, the EMG measures the electrical activity of the skeletal muscles and the EEG measures the electrical activity of brain cells [2]. Each of these bioelectric signals help physicians diagnose and treat disorders related to the targeted organ.

1.2 Biopotential Low-Noise Amplifier

In any biomedical recording apparatus, bioelectric signals measured by electrodes require proper amplification to allow for signal processing and digitization [3]. Due to the weak amplitudes of the measured biopotential signals, the biopotential amplifier itself must contribute very little noise to prevent signal corruption, hence the term biopotential low-noise amplifier (BPA) or (bio-LNA).

Each bioelectric signal has different amplitude and frequency characteristics as shown in Table 1. Therefore, to achieve optimum signal quality, bio-LNAs are usually designed for the specific application with appropriate gain and bandwidth. In the case where multiple bioelectric signals are of interest, the bio-LNA must provide at least 40 dB gain with a passband from 50 mHz to 10 kHz to accommodate all bioelectric signals listed in Table 1 [4, 5, 6].

Table 1 Bioelectric signal characteristics [3]

Bioelectric signal	Frequency range (Hz)	Amplitude range (mV)
Electrocardiogram (ECG)	0.05 - 100	1 - 10
Electromyogram (EMG)	500 - 10k	0.02 - 0.01
Electroencephalogram (EEG)	0.5 - 100	0.02 - 0.1

Bio-LNAs are designed with a differential topology with high common-mode rejection ratio (CMRR) to reject common-mode noise and high power supply

rejection ratio (PSRR) to reject power line noise at 50/60 Hz. Bio-LNAs must also have high input impedance to minimize loading of the measured signal and to prevent source impedance unbalances caused by electrodes from deteriorating the overall CMRR [1, 3].

A common figure of merit that ties total noise and current consumption of bio-LNAs is the Noise Efficiency Factor (NEF) introduced by Stayaert et al. [7]. The NEF describes how many times the input-referred noise of a system is higher compared to that of an ideal bipolar transistor with the same current and bandwidth as shown in Eq. (1).

$$NEF = V_{rms,in} \sqrt{\frac{2 I_{total}}{\pi V_T 4kT BW}} \quad (1)$$

The NEF is a good figure of merit when comparing bio-LNAs with the same supply voltage. However, two different bio-LNAs with equal current consumption and input-referred noise will have the same NEF but different power dissipation due to the different supply voltages used. A more suitable figure of merit introduced by Muller et al. is the Power Efficiency Factor (PEF) which compares the total power consumption of the bio-LNA as shown in (2) [8].

$$PEF = NEF^2 V_{DD} = V_{rms,in}^2 \frac{2 P_{tot}}{\pi V_T 4kT BW} \quad (2)$$

Since most bioelectric signals are located at very low frequency, flicker noise becomes a major contributor for the total noise of the amplifier. The two most common solutions are to utilize the chopping technique or to utilize a topology with a bandpass frequency response. The chopper amplifier has been used by many to modulate flicker noise to the chopping frequency, however it requires additional circuitry which takes up a portion of the power budget [9, 10, 11]. On the other hand, utilizing a topology that provides a bandpass frequency response limits flicker noise contribution as well as filters out lower frequency artifacts [4, 5, 6, 12].

1.3 Pseudo Resistors

A bandpass frequency response can be obtained by introducing a zero followed by two poles. However, having a pole within the sub-Hz range implies that the circuit must have very large RC time-constants which may be achieved by off-chip components. In recent years, the focus has been to obtain a high valued on-chip resistor to achieve the sub-Hz pole frequency. Harrison et al. introduced a bio-LNA utilizing on-chip pseudo resistors to set the very low pole frequency as shown in Fig. 1 [13].

The pseudo resistor was first used in a photoreceptor circuit to adapt to different lighting conditions by providing huge effective resistance for small signals and small effective resistance for large signals [14]. When biased with positive V_{gs} , it behaves as a diode-connected pnp BJT and when biased with negative V_{gs} , it behaves as a

diode-connected PMOS transistor. As shown in the Fig. 2, the midband gain of the bio-LNA is given as C_1/C_2 with a first pole of $1/(2 R_{pseudo}C_2)$ and a second pole of g_m/C_L . The incremental resistance of the pseudo resistor achieved in [13] was greater than $10T\Omega$ which resulted in a first pole of 0.025Hz .

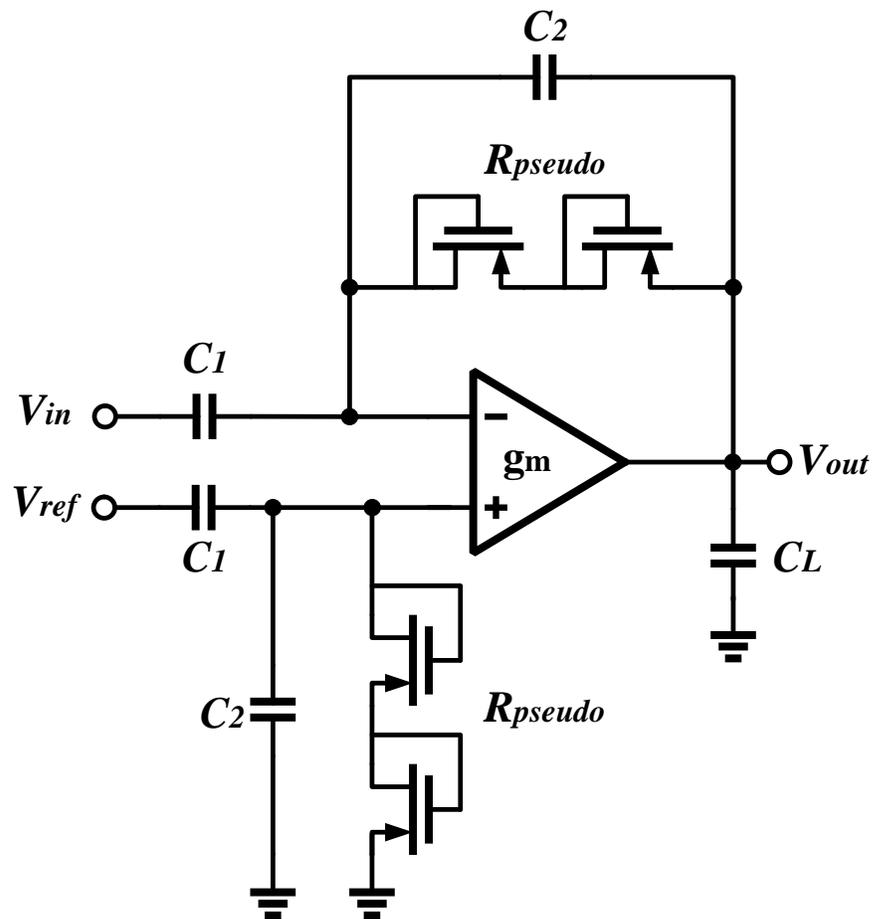


Figure 1 Low-noise neural amplifier [13]

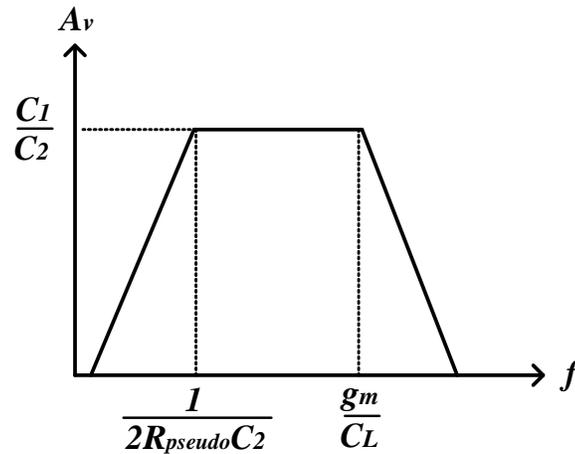


Figure 2 Frequency response of the low-noise neural amplifier

The prevalence of pseudo resistors in bio-LNAs, has made it possible to fabricate fully integrated biomedical acquisition systems [12, 13, 15]. However, one of the disadvantages of the pseudo resistor is that its effective resistance varies drastically across voltages [16]. The dependence of the pseudo resistor on its voltage drop coupled with PVT variations makes its effective resistance difficult to control. In essence, the variability of the pseudo resistor causes the first pole of the bio-LNA to wander across different chips.

Since its inception, multiple research groups have been investigating different approaches to solve the variability of pseudo resistors. A common theme amongst them is to make the pseudo resistor tunable so that its effective resistance can be accurately controlled manually or by means of feedback [17, 18, 19, 20, 21, 22].

Other intellectuals have moved away from pseudo resistors all together exploring other methods to achieve the sub-Hz pole frequency.

2 Capacitor Multiplier

Another way to achieve sub-Hz pole frequency is to utilize $g_m C$ filters with very low transconductance and/or very large capacitors [23]. Sub-nS transconductances can be obtained by employing series-parallel current mirrors [24]. However, large capacitors are difficult to implement on-chip since its capacitance is limited by the available area. Capacitor multipliers solve this issue by producing an effective capacitance which is many times larger than the implemented capacitor negating the need of off-chip elements.

2.1 The Miller Effect

The Miller Effect indicates that the effective capacitance, C_{eff} , of a capacitor, C_F , when placed across an inverting gain stage, $-A$, is approximately $(1 + A)C_F$ as shown in Fig. 3 [25]. The Miller Effect may be used to implement high-valued capacitors in $g_m C$ filters to obtain very low pole frequency as shown in Fig. 4. However, this implementation is impractical as it limits the voltage swing at the output node and requires proper DC biasing for the amplifier [26].

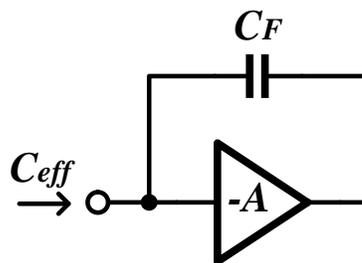


Figure 3 Miller effect stating that $C_{eff} = (1 + A) C_F$

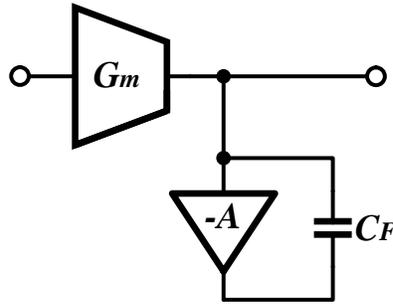


Figure 4 Impractical implementation of a capacitor multiplier

Instead of employing the Miller Effect in the voltage domain, capacitance scaling can be achieved in the current domain by sinking an amplified version of the current in the capacitor, $k i_c$, as shown in Fig. 5 [27]. The total current flow at the input node is $i_c(k + 1)$ achieving an effective capacitance of $C_F(k + 1)$. The capacitor multiplier has been used to increase the compensation capacitance in a linear regulator as well as to increase the capacitance of the loop filter in a phase-locked loop [28, 29].

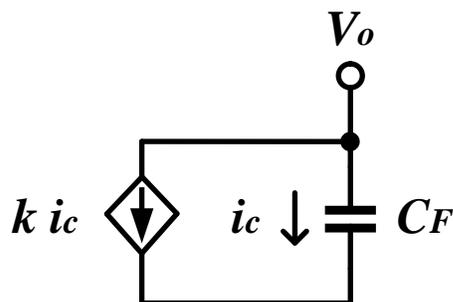


Figure 5 Current-mode Miller effect

2.2 Implementation

The simplest way to implement the capacitor multiplier is to utilize current mirrors as shown in Fig. 6 [28]. Devices M_X and senses the small-signal current flowing through the capacitor and scales the current to the output through M_Y which is k times larger than M_X . The effective capacitance looking in from the node V_o is $C_F(k + 1)$.

With $\frac{W}{L_Y} = k \frac{W}{L_X}$ the obvious disadvantage of this topology is that the current and area increases with the multiplication factor k .

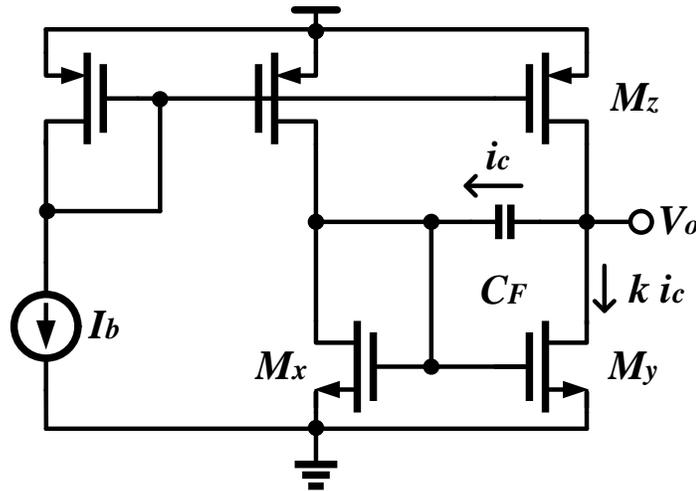


Figure 6 Current-mirror implementation of a capacitor multiplier

The equivalent circuit of the capacitor multiplier consist of a parallel load resistance (PLR), R_1 , and an equivalent series resistance (ESR), R_2 , as shown in Fig. 7. With $R_1 = r_{o_x} || r_{o_y}$ and $R_2 = 1/g_{m_x}$, the impedance looking in from V_o is now has a pole and zero at $1/kC_F(R_1 + R_2)$ and at $1/kC_F R_2$ respectively as shown in Eq. (3).

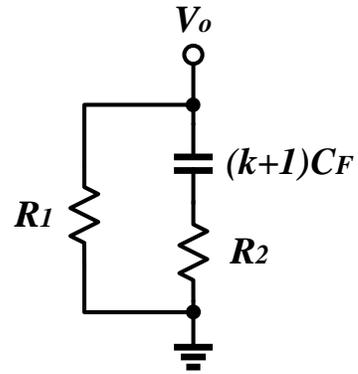


Figure 7 Equivalent circuit of the capacitor multiplier

$$Z_{in} \approx \frac{R_1(skC_F R_2 + 1)}{skC_F(R_1 + R_2) + 1} \quad (3)$$

3 Differential Difference Amplifier

The differential difference amplifier (DDA) operates in a similar fashion as the standard op amp. The only difference is that the standard op amp amplifies a single differential input whereas the DDA amplifies the difference of two differential inputs as shown in Fig. 8 Differential difference amplifier and Eq. (4). As with the conventional op amp, various feedback arrangements are available to cater to different applications [30].

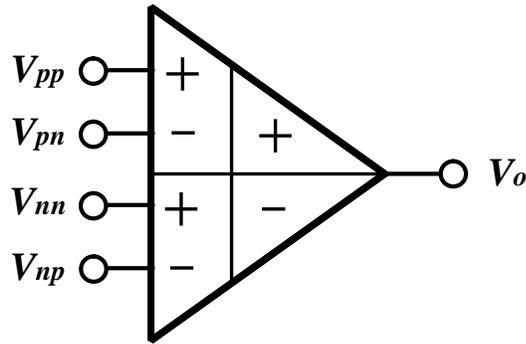


Figure 8 Differential difference amplifier

$$V_o = A_v [(V_{pp} - V_{pn}) - (V_{nn} - V_{np})] \quad (4)$$

In an attempt to conceive of a design without pseudo resistors, Oreggioni et al. introduced a bio-LNA using a DDA to provide high CMRR for neural recording applications as shown in Fig. 9 Proposed DDA configuration [31] [31]. The DDA

structure used is rather intriguing as it utilizes one differential input for amplification and the other for feedback to achieve the high-pass characteristic.

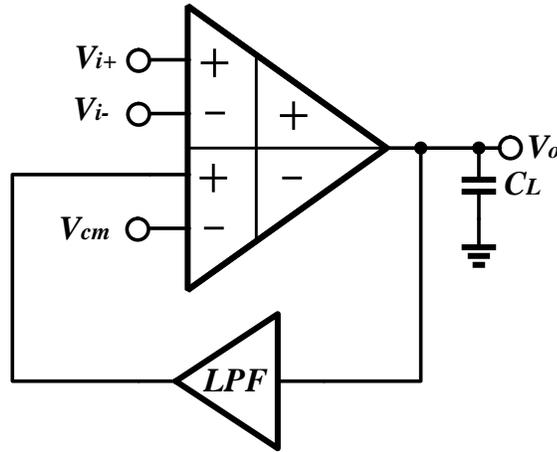


Figure 9 Proposed DDA configuration [31]

An intuitive way of understanding the high-pass characteristic of the feedback loop is shown in Fig. 10 High-pass characteristic of the DDA In Fig. 11(a), the input spectrum consist of the desired bio-signal (green) along with a DC component and lower frequency artifacts (red). As the signal passes through G_{m1} , each component is amplified but the spectrum is contaminated with flicker and thermal noise as shown in Fig. 11(b). The G_{mf} block has a low-pass response which can designed in such a way to filter out the signal of interest preserving only the DC component and lower frequency artifacts as shown in Fig. 11(c). When subtracted with the output of G_{m1} , the result will only contain the signal of interest and lower noise content as shown in Fig. 11(d). The resulting transfer function will have a bandpass nature which will be described in the next section.

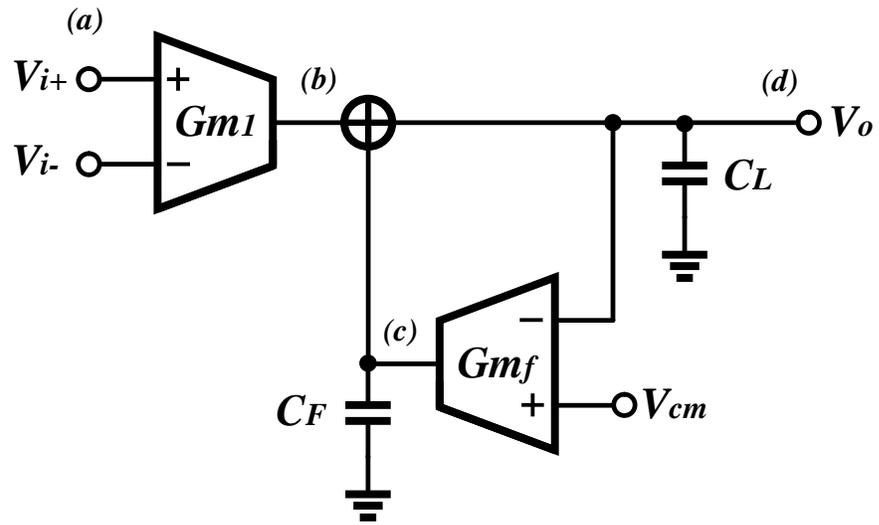


Figure 10 High-pass characteristic of the DDA

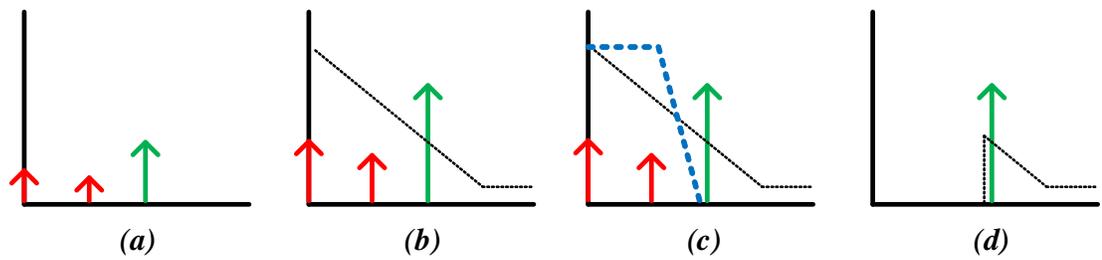


Figure 11 Plots of each stage in the DDA

3.1 Transfer Function

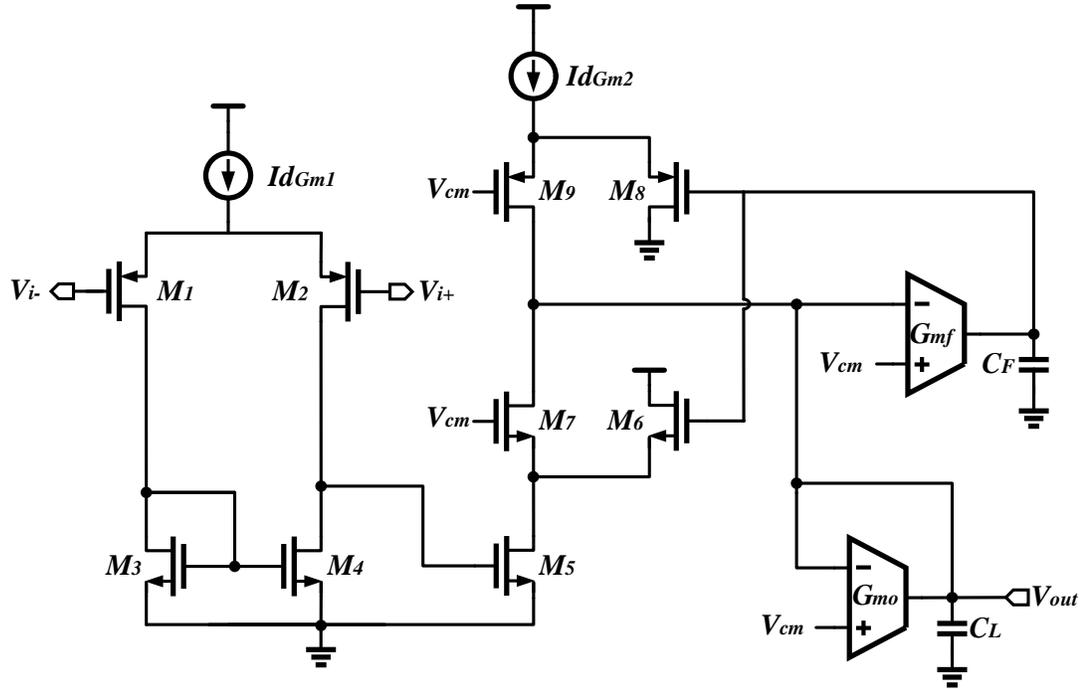


Figure 12 CMOS implementation of the DDA

The circuit in Fig. 12 features a two-stage OTA where G_{m1} and G_{m2} are the transconductance of the first and second stage respectively while R_{o1} is the output resistance of the first stage. The output of the second stage is taken into a negative feedback loop through G_{mf} and C_f which sets the first pole, f_{p1} . The ratio of G_{mo} to the transconductance of the two-stage OTA sets the midband gain, G , while the load capacitance C_L sets the second pole, f_{p2} as shown in (5)-(10). It is important to note that the zero, f_z , which is caused by the finite gain of G_{mf} affects the DC gain, G_{DC} , of the DDA and will be discussed in the next section.

$$\frac{V_{out}}{V_{in}} = \frac{\frac{G_{m1}G_{m2}R_{o1}}{C_L} \left(s + \frac{1}{r_{of}C_F} \right)}{s^2 + \frac{G_{mo}}{C_L} s + \frac{(g_{m6} + g_{m8})G_{mf}}{C_L C_F}} \quad (5)$$

$$G = \frac{G_{m1}G_{m2}R_{o1}}{G_{mo}} \quad (6)$$

$$G_{DC} = \frac{G_{m1}G_{m2}R_{o1}}{(g_{m6} + g_{m8})G_{mf}r_{of}} \quad (7)$$

$$f_z = \frac{1}{2\pi r_{of}C_F} \quad (8)$$

$$f_{p1} = \frac{(g_{m6} + g_{m8})G_{mf}}{2\pi C_F G_{mo}} \quad (9)$$

$$f_{p2} = \frac{G_{mo}}{2\pi C_L} \quad (10)$$

The appeal of this architecture is the implementation of the feedback loop producing the high-pass characteristic. Consider an undesirable low frequency small-signal voltage at the input of the DDA, a small-signal current of $\Delta i g_{m1}$ will flow

3.2 Design Procedure

The design of the DDA starts with the gain specification which states that a high valued G_{m1} is required to provide high pass-band gain. In order to keep current consumption to the minimum, M_1 and M_2 are biased in weak inversion to yield a high g_m/I_d ratio. Having high G_{m1} is also crucial for lowering the input-referred noise. Depending on the choice of g_m/I_d value, G_{m1} and G_{m2} are determined from the current budget of the bio-LNA. Once G_{m1} and G_{m2} is determined, G_{mo} is chosen to meet the pass-band gain, G .

After selecting G_{mo} , the required load capacitance, C_L , is calculated to set the required low-pass cut-off frequency, f_{p2} . For the high-pass cut-off frequency, f_{p1} , the feedback capacitor, C_F , needs to be large and therefore is determined from the available area on-chip. G_{mf} along with g_{m6} are then designed to meet the required high-pass cut-off frequency.

It is important to note that M_6 drains a portion of the AC signal current. To mitigate this issue, g_{m7} must be designed to be greater than g_{m6} so that the source impedance of M_7 is lower than that of M_6 . However, g_{m6} must not be too low as it plays a role in setting the DC gain as shown in (7). The design process is reiterated until all specifications are met.

3.3 Loop Gain

The loop gain of the negative feedback loop contains two poles, one at $1/C_F r_{of}$ and another at G_{mo}/C_L as shown in Eq. (11). The first and second pole represents the zero and the low-pass pole of the overall transfer function respectively. Therefore, a dominant single pole assumption can be made which states that the loop is stable with a phase margin of 90° . The loop gain plays an important role in setting the DC gain of the DDA, G_{DC} , because it is defined as the ratio of the pass-band gain of the DDA, G , and the loop gain, LG_{DC} , as shown in Eq. (13) which agrees with (7). Thus, achieving high loop gain is synonymous to obtaining low DC gain for the DDA.

$$LG \approx \frac{G_{mf} r_{of} (g_{m6} + g_{m8})}{G_{mo} (s C_F r_{of} + 1) \left(\frac{s C_L}{G_{mo}} + 1 \right)} \quad (11)$$

$$LG_{DC} = \frac{G_{mf} r_{of} (g_{m6} + g_{m8})}{G_{mo}} \quad (12)$$

$$G_{DC} \approx \frac{G}{LG_{DC}} = \frac{G_{m1} G_{m2} R_{o1}}{(g_{m6} + g_{m8}) G_{mf} r_{of}} \quad (13)$$

By plotting the transfer function of the DDA in Matlab (see appendix), the effect of the zero on the DC gain is observed. As the loop gain is reduced by reducing r_{of} , the DC gain increases and the DDA no longer has a band-pass characteristic as

shown in the Fig. 14. Hence, the output impedance of the G_{mf} is crucial in rejecting DC components as well as lower frequency artifacts.

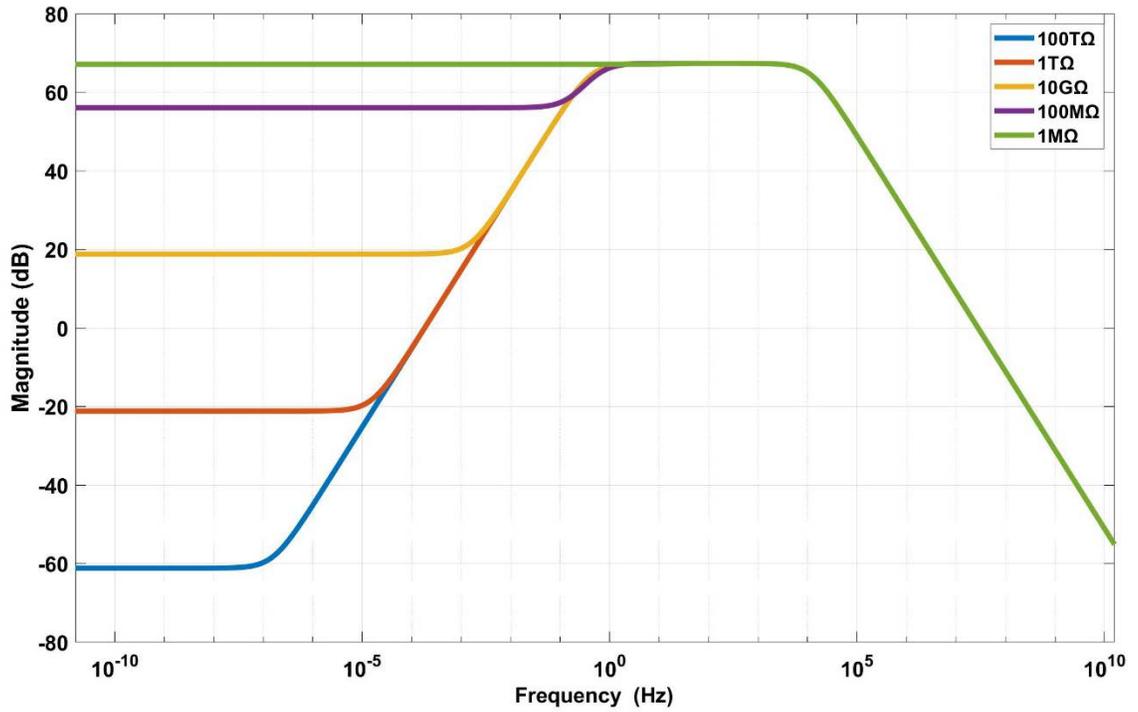


Figure 14 Transfer function with different r_{of} values

3.4 Implementation

Iterating through the design process for the specifications in Table 2, the design parameters are obtained as shown in Table 3.

Table 2 Design specifications

Spec	Value
G (dB)	>40
G_{DC} (dB)	<-40
f_{p1} (mHz)	<50
f_{p2} (kHz)	>10

Table 3 Design Parameters

Design Parameters	Value
Technology (nm)	180
V_{DD} (V)	1.8
$G_{m1}G_{m2}R_{o1}$ (mS)	3.5
G_{mo} (μS)	1.5
G_{mf} (nS)	10
$g_{m6,8}$ (μS)	2
C_L (pF)	20
C_F (pF)	200
k	50
$I_{d_{G_{m1}}}$ (μA)	4
$I_{d_{G_{m2}}}$ (μA)	1
$I_{d_{G_{mo}}}$ (nA)	100
$I_{d_{G_{mf}}}$ (nA)	1
I_{bias} (nA)	1
I_{total} (μA)	5.38

3.4.1 Two-stage OTA

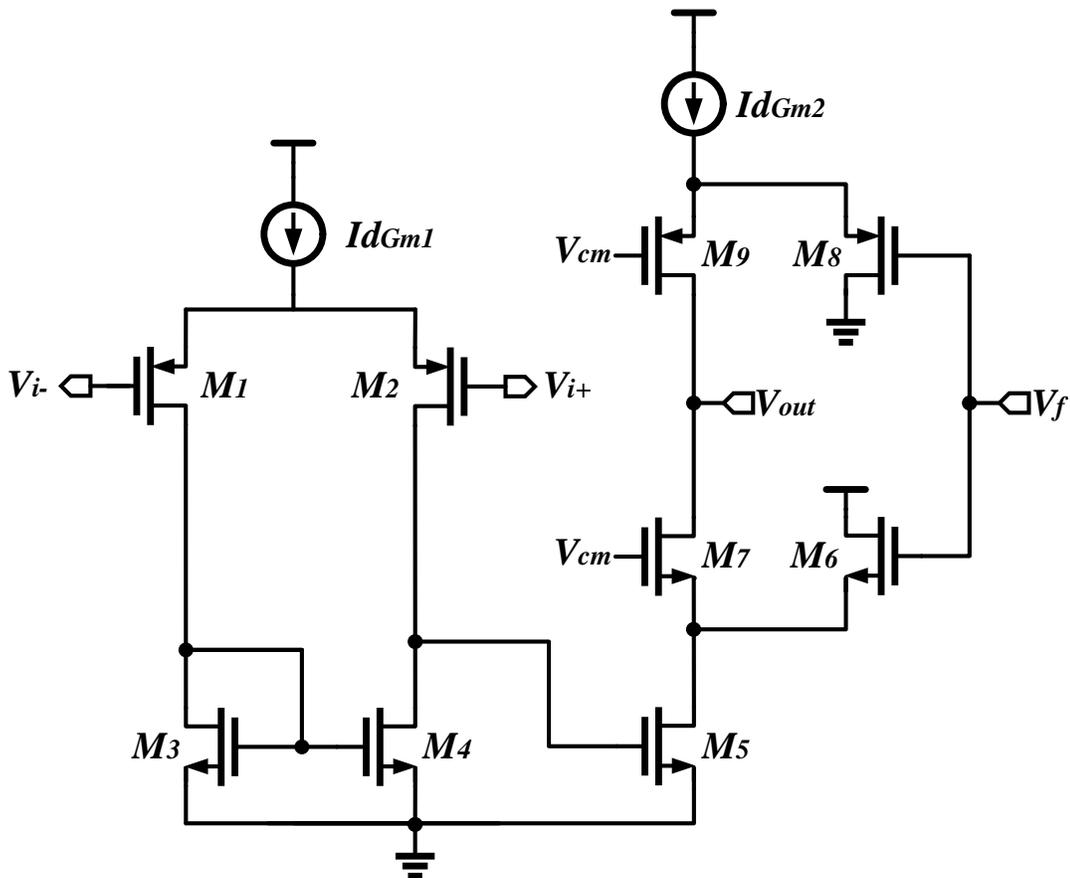


Figure 15 Two-stage DDA structure

The two-stage OTA was chosen primarily to provide high pass-band gain. A single stage OTA can be used as in [31] to lower current consumption. However, stacking five transistors lowers the voltage headroom for the current source which will degrade CMRR for lower supply voltages.

As mentioned in the previous section, the ratio of g_{m6} to g_{m7} determines how much pass-band gain is lost. For example, if $g_{m6} = g_{m7}$, half of the AC signal is lost and hence the pass-band gain is lowered by 6dB. In this design, g_{m6} is designed to be 10 times less than g_{m7} .

It is important to note that the output node of the first stage OTA contains a pole, f_{p3} , which can be less than f_{p2} if the output resistance, R_{o1} , or the parasitic capacitances at that node is too large as shown in Eq. (14). Therefore, it is important to keep that in mind when sizing the devices.

$$f_{p3} = \frac{1}{2\pi R_{o1}(C_{gs5} + C_{gd2} + C_{gd4})} \quad (14)$$

3.4.2 G_{m_o}

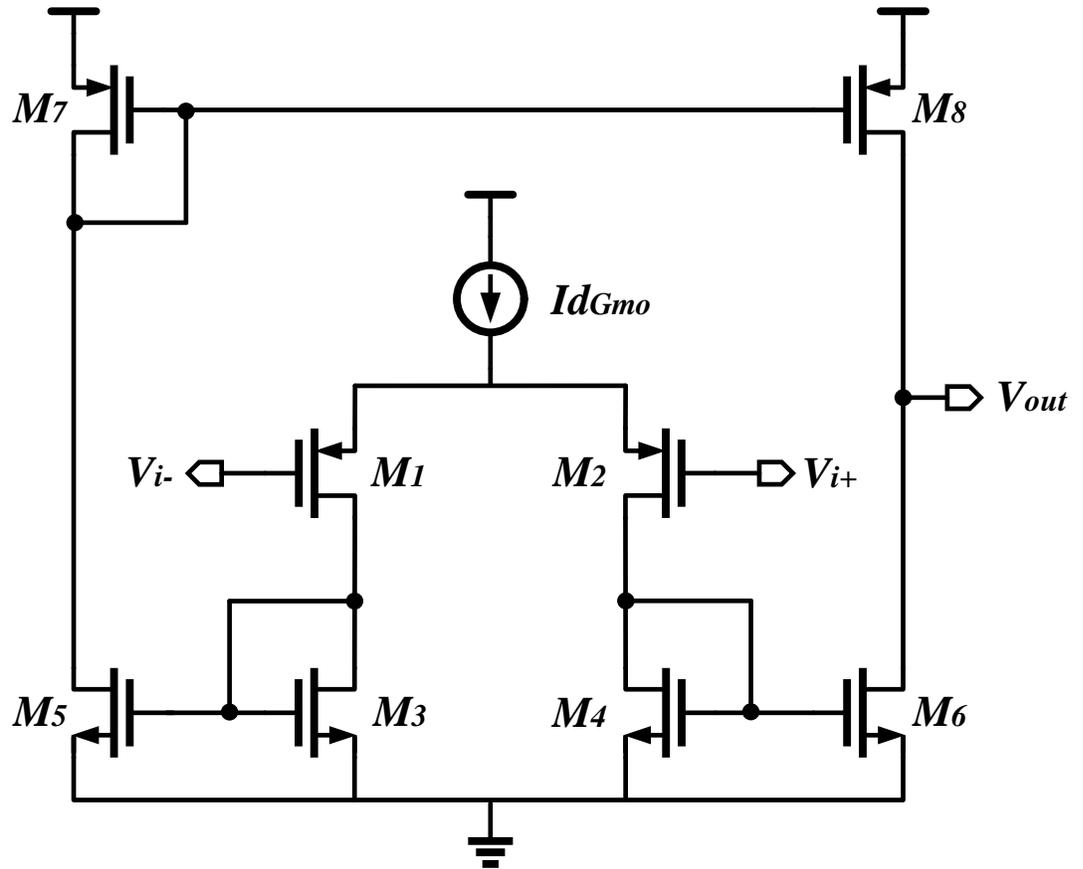


Figure 16 Current-mirror OTA

A current-mirror OTA was chosen to implement the output transconductance block. As with the two-stage OTA, the G_{m_o} block can be implemented with a single-stage OTA.

3.4.3 G_{mf}

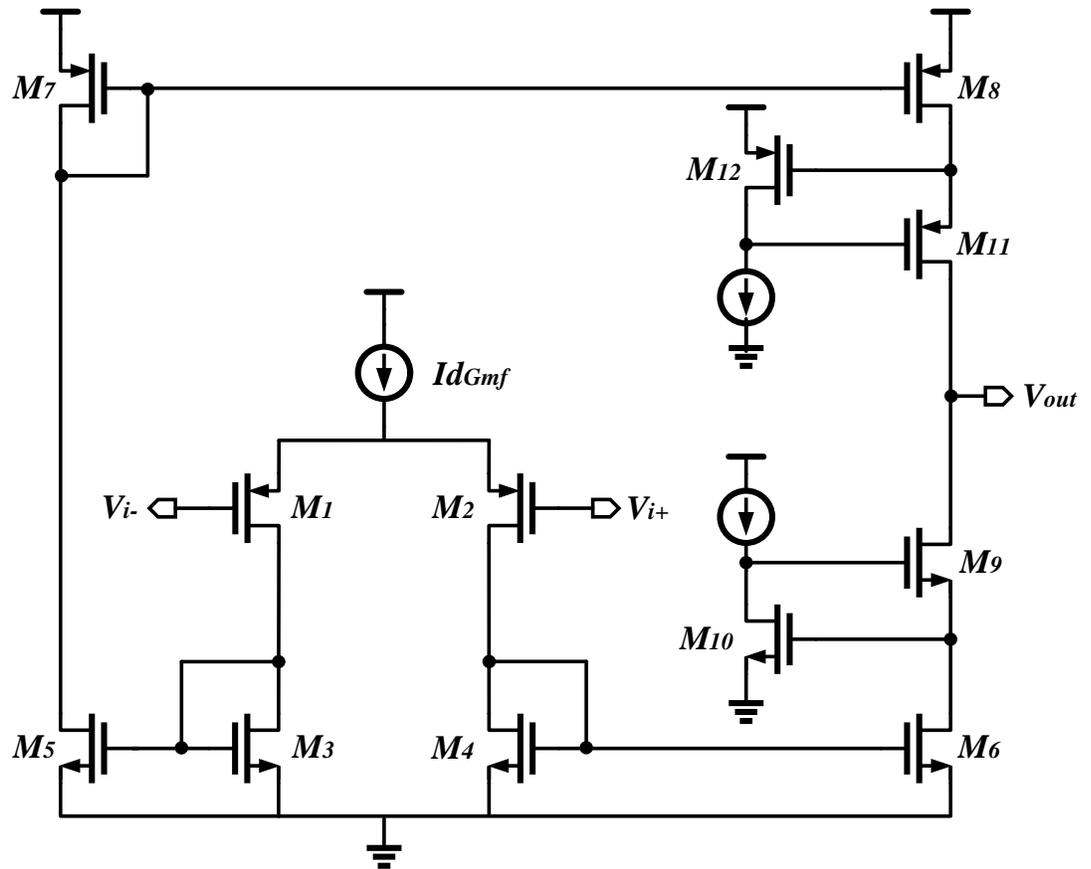


Figure 17 Gain-boostered current-mirror OTA

The G_{mf} block is implemented with a current-mirror OTA with gain-boosted cascodes to increase the output impedance, r_{of} , as shown in Fig. 17. A common source configuration is used to boost the impedance of the output. In the case where output swing is limited, a folded cascode gain boost amplifier may be used.

3.4.4 Capacitor Multiplier

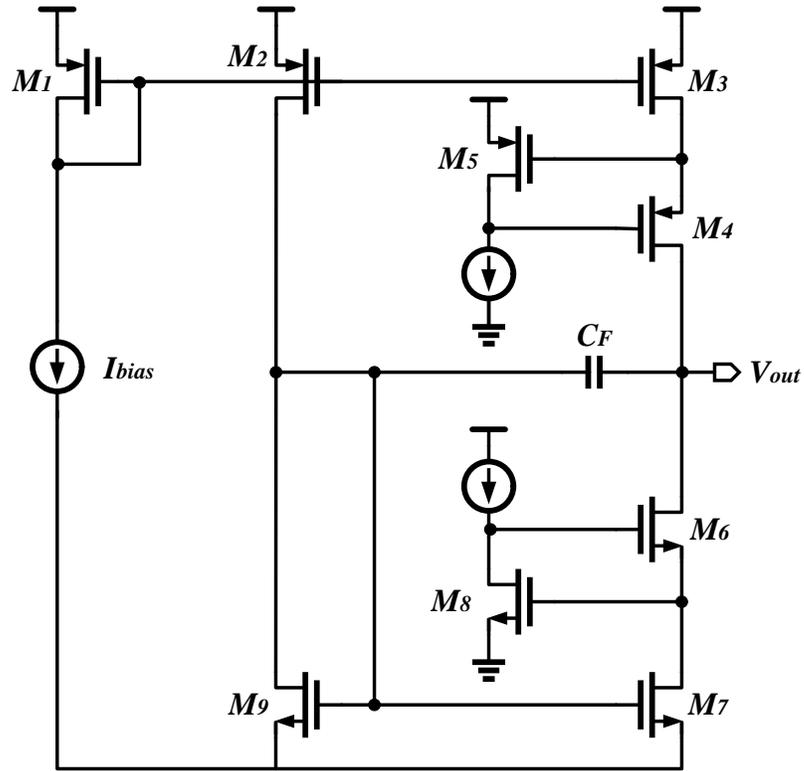


Figure 18 Gain-boosted capacitor multiplier

The capacitor multiplier is implemented with current-mirrors with gain-boosted cascodes to reduce the loading on the output node of G_{mf} as shown in Fig. 18. With a bias current of 1nA, g_{m_9} will be in the order of a few tens of nS. As a result, the equivalent series resistance, R_{ESR} , of $1/g_{m_9}$ will have an effect on the overall transfer function. As R_{ESR} increases, G , f_{p1} and f_{p2} is scaled with a factor α as shown in Eq. (15)-(18). Referring to the design parameters in Table 3 Design Parameters, a

R_{ESR} of $1\text{G}\Omega$ yields an α of 27.67 which reduces the pass-band gain by 28.8dB and shifts the poles by the same factor as shown in Fig. 19 Effect of the ESR on the transfer function. The ESR also introduces a zero in the loop gain at $1/R_{ESR}C_F$ as shown in Eq. (19).

$$G = \frac{1}{\alpha} \left(\frac{G_{m1}G_{m2}R_{o1}}{G_{mo}} \right) \quad (15)$$

$$f_{p1} = \frac{1}{\alpha} \left[\frac{(g_{m6} + g_{m8})G_{mf}}{2\pi C_F G_{mo}} \right] \quad (16)$$

$$f_{p2} = \alpha \left(\frac{G_{mo}}{2\pi C_L} \right) \quad (17)$$

$$\alpha \approx 1 + \frac{G_{mf}(g_{m6} + g_{m8})R_{ESR}}{G_{mo}} \quad (18)$$

$$LG \approx \frac{G_{mf}r_{of}(g_{m6} + g_{m8})(sC_F R_{ESR} + 1)}{G_{mo}(sC_F r_{of} + 1) \left(\frac{sC_L}{G_{mo}} + 1 \right)} \quad (19)$$

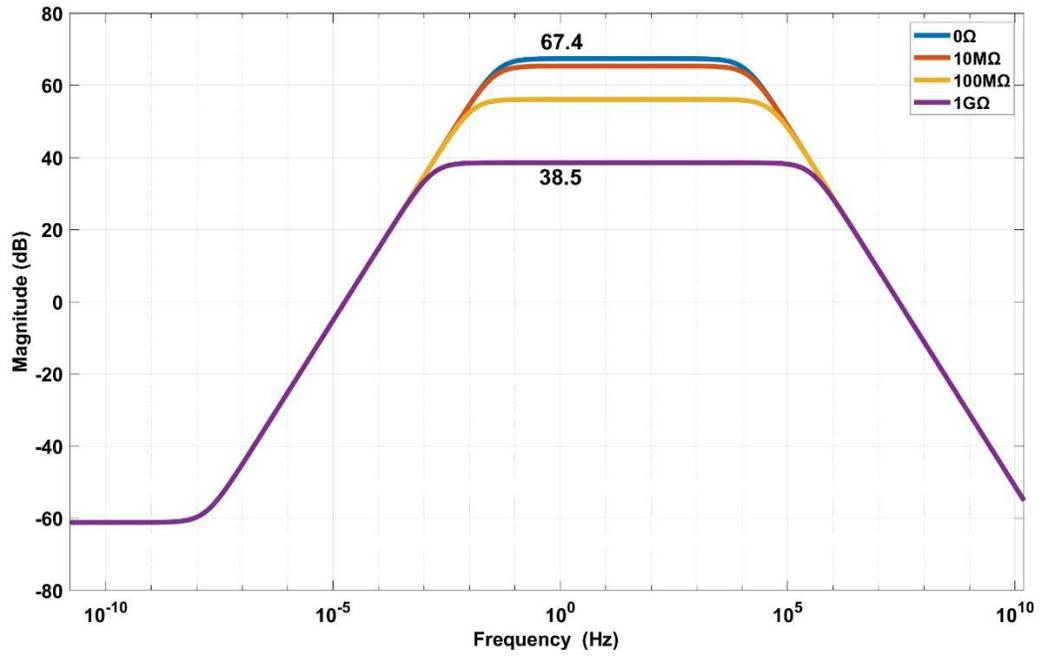


Figure 19 Effect of the ESR on the transfer function

4 Simulation Results

The bio-LNA was simulated with PVT variations of $\pm 10\%$ V_{DD} (1.62, 1.8, 1.98V), 5 process corners (tt, ss, ff, sf, fs), and temperatures of 0, 27 and 100°C. The minimum, typical and maximum simulation results are shown in Table 4.

Table 5 Simulation results

Spec	Min.	Typical	Max.
G (dB)	65.91	66.24	69.16
G_{DC} (dB)	-61.88	-60.22	-29.23
f_{p1} (mHz)	441.2	452.1	486.7
f_{p2} (kHz)	8.26	12.6	13.60
I_{total} (μA)	5.33	5.38	5.47
V_{ni} (μV)	2.99	3.33	3.72
NEF	2.43	2.65	3.23
PEF	9.58	12.60	20.59
CMRR @ 13kHz (dB)	94.74	97.37	98.72
PSRR @ 60Hz (dB)	105.8	109.8	111.2

4.1 Frequency Response

The simulated f_{p1} was not able to achieve the desired value of less than 50mHz because the multiplication factor, k , is limited by matching as well as the loop gain. As k increases, mismatches in the current-mirror will worsen which will vary the location of f_{p1} . Furthermore, a high k lowers r_{of} which increases the DC gain of the DDA, G_{DC} . In the end, a k of 50 was used to multiply C_F to produce an effective capacitance of 10nF.

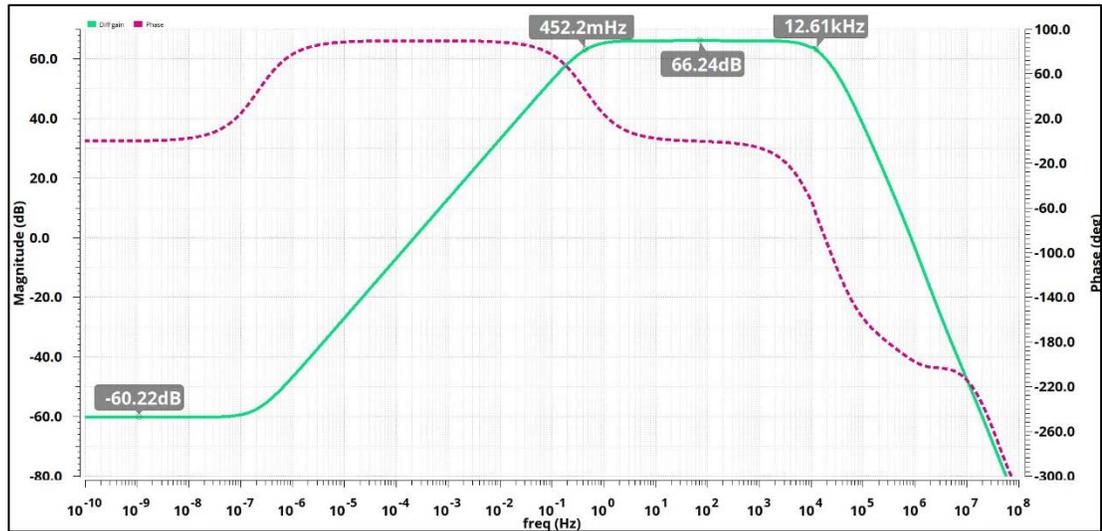


Figure 20 Magnitude and phase response of the DDA

The existence of the zero due to the ESR of the capacitor multiplier is seen in the loop gain plot in Fig. 21. Since the zero is at least a decade away from the unity gain

bandwidth, it does not affect the phase margin at all. Fig. 22 shows the relationship between the loop gain, pass-band gain and the DC gain as stated in (13).

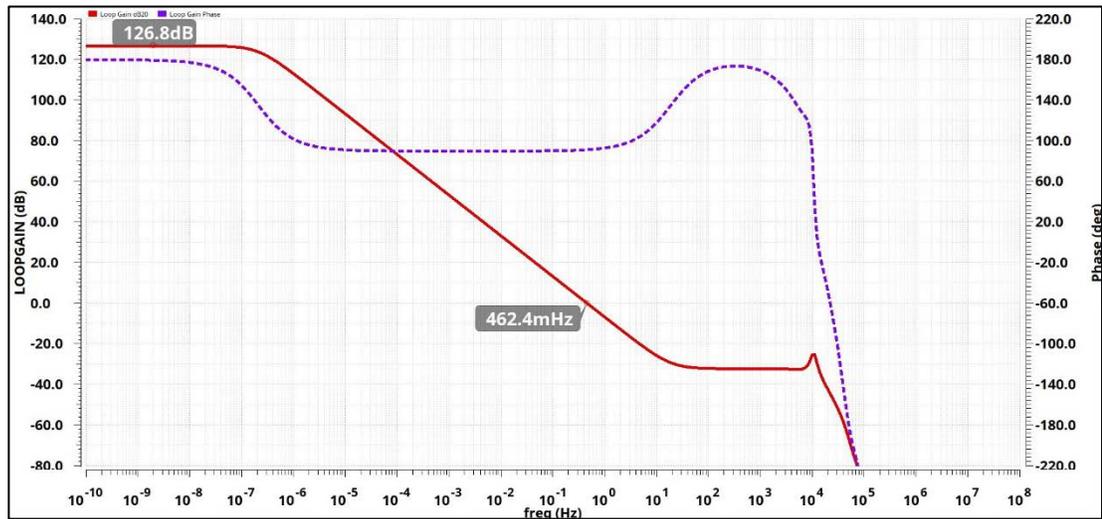


Figure 21 Magnitude and phase response of the feedback loop

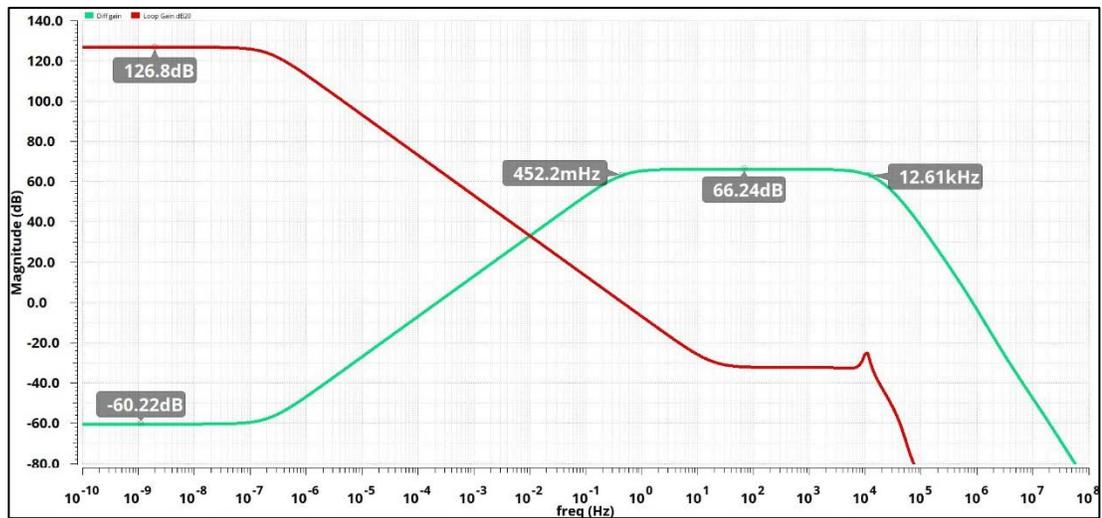


Figure 22 DDA transfer function with loop gain

4.2 Noise

Fig. 23 Input-referred noise with the DDA transfer functions shows the input-referred noise of the DDA plotted in log scale. Before the zero, f_z , the $1/f$ slope due to flicker noise is -10dB/dec. After f_z , the slope decreases to -30dB/dec due to the 20dB/dec slope of the transfer function. In the passband, flicker noise of -10dB/dec is observed until the corner frequency which is around 1kHz. The input-referred noise was integrated with a bandwidth from the first pole to the second pole to yield a NEF of 2.65 and a PEF of 12.6.

The devices in the first stage of the G_{m1} block dominated the overall noise contribution as shown in Table 6 Noise contribution. M_1 and M_2 contributed the most thermal noise followed by M_3 and M_4 because the noise current of $M_{3,4}$ is divided by the transconductance of $M_{1,2}$. The flicker noise of $M_{1,2}$ is lower $M_{3,4}$ because the sizes of $M_{1,2}$ are larger to increase the value of G_{m1} .

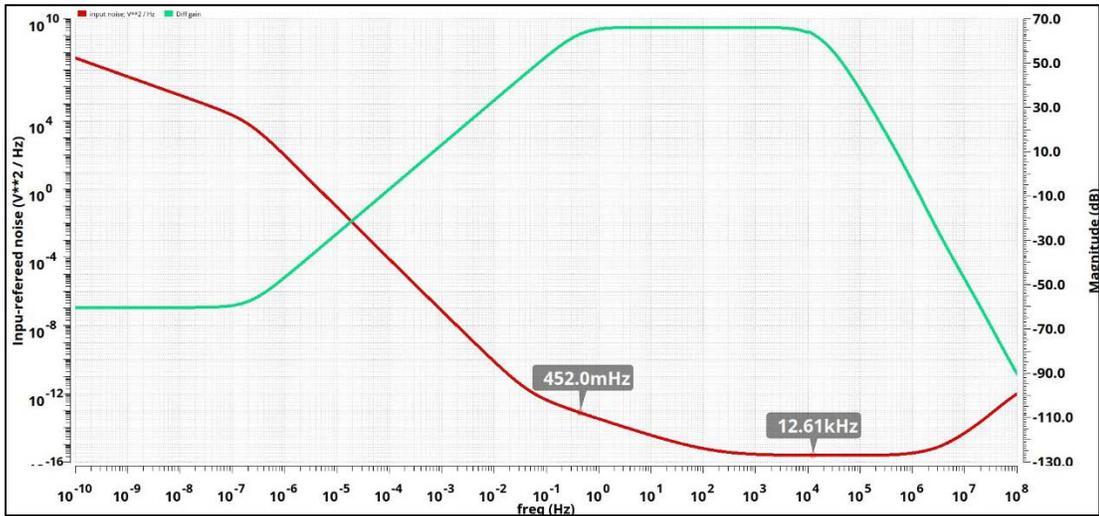


Figure 23 Input-referred noise with the DDA transfer function

Table 6 Noise contribution

Device	Noise Type	Noise Contribution
M _{1,2}	Thermal	60.8%
M _{3,4}	Thermal	25.8%
M _{3,4}	Flicker	9.8%
M _{1,2}	Flicker	3.6%

4.3 CMRR

The common-mode rejection ratio is taken at 13kHz as it is the location of the second pole. As shown in Fig. 24, a CMRR of 97.4dB is obtained.

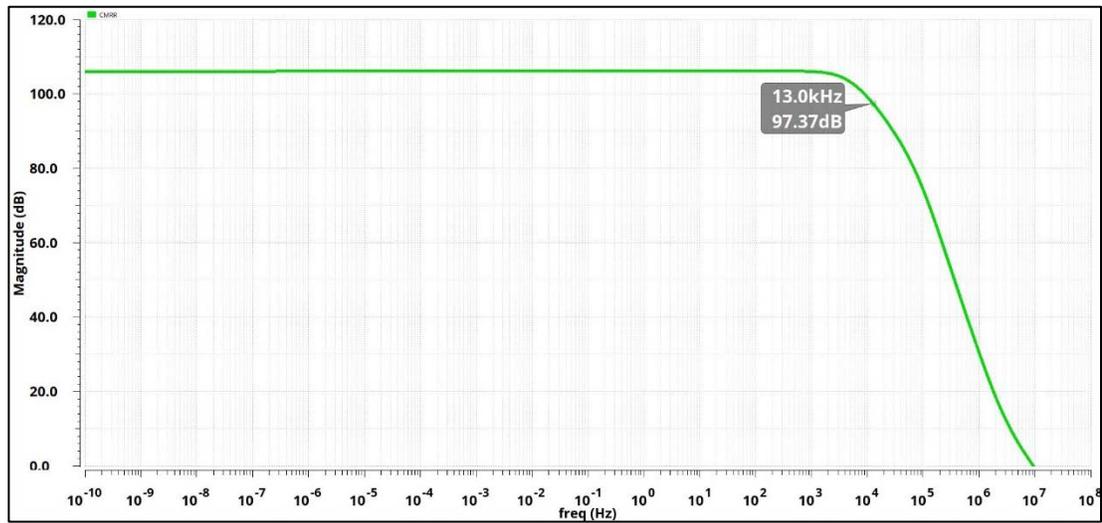


Figure 24 Common-mode rejection ratio of the DDA

4.4 PSRR

A power supply rejection ratio of 109.8dB is obtained at 60Hz as shown in Fig. 25.

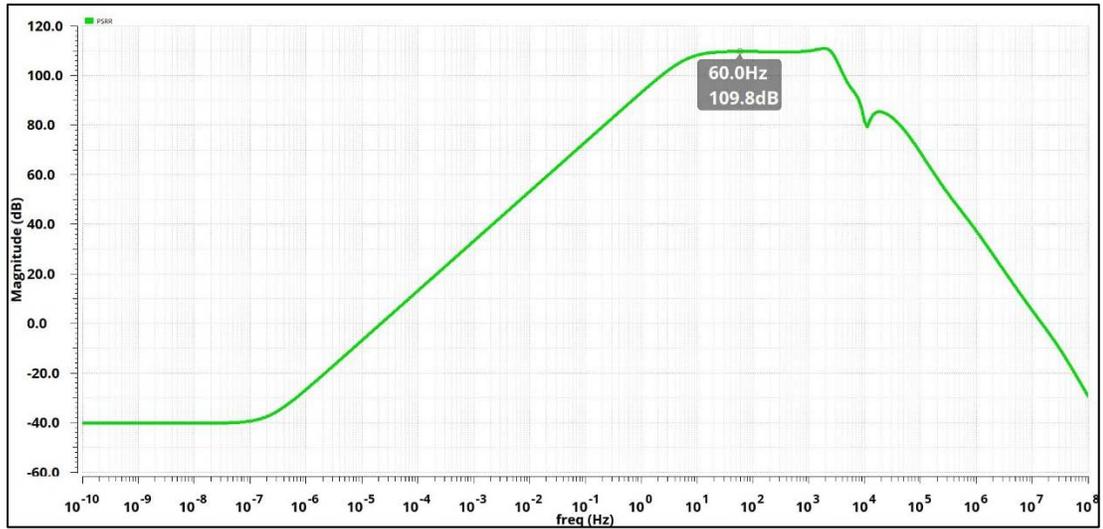


Figure 25 Power supply rejection ratio of the DDA

4.5 Monte Carlo

The monte carlo simulations were done with 200 samples. Out of the 200 samples 4 cases had mismatches that were too large for the feedback loop to handle which resulted in very low gain and erroneous pole locations.

4.5.1 Pass-band Gain

The pass-band gain has a mean of 64.65dB as shown in Fig. 26.

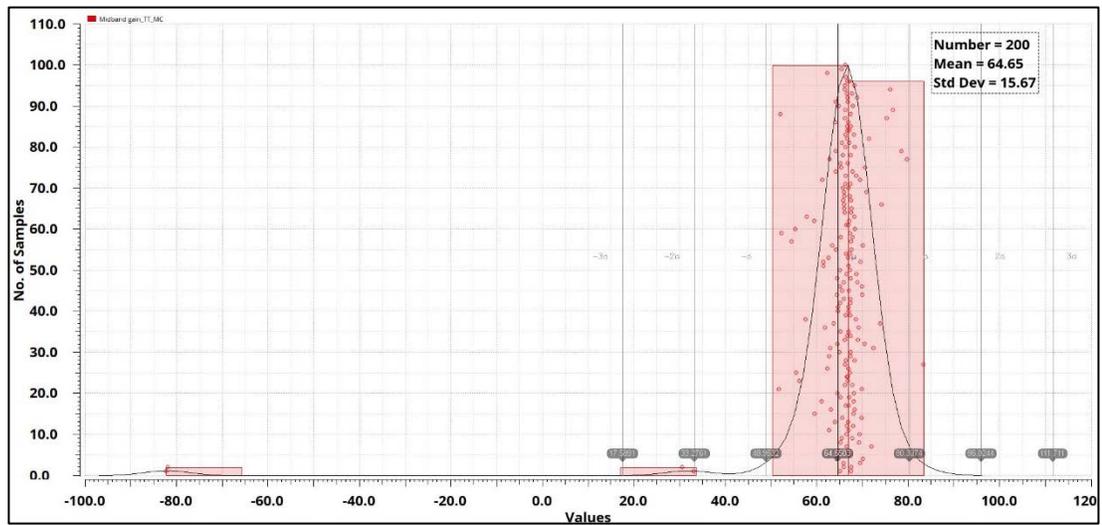


Figure 26 Pass-band gain monte carlo plot

4.5.2 Loop Gain

The loop gain has a mean of 124.73dB as shown in Fig. 27.

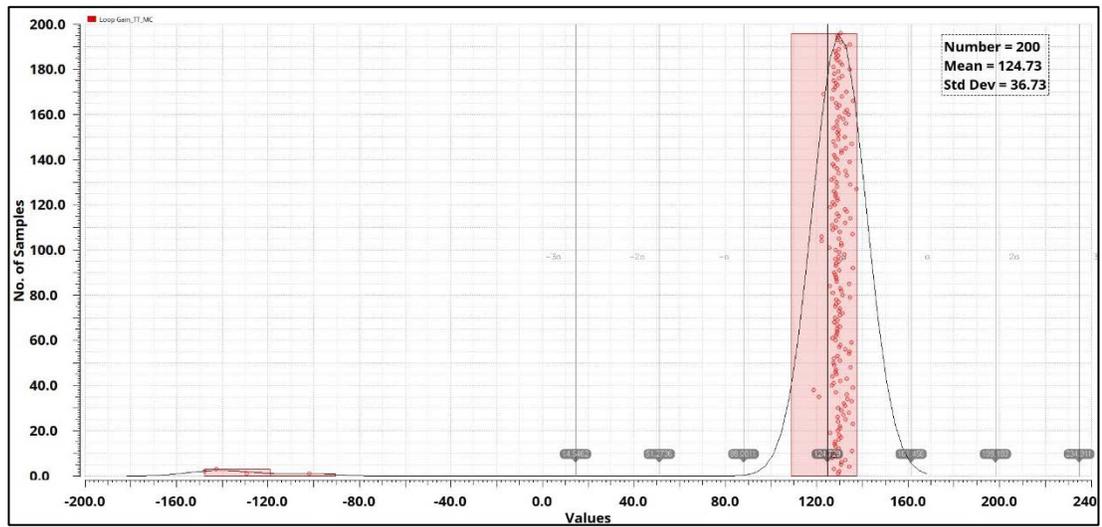


Figure 27 Loop gain monte carlo plot

4.5.3 DC Gain

The DC gain has a mean of -62.4dB as shown in Fig. 28.

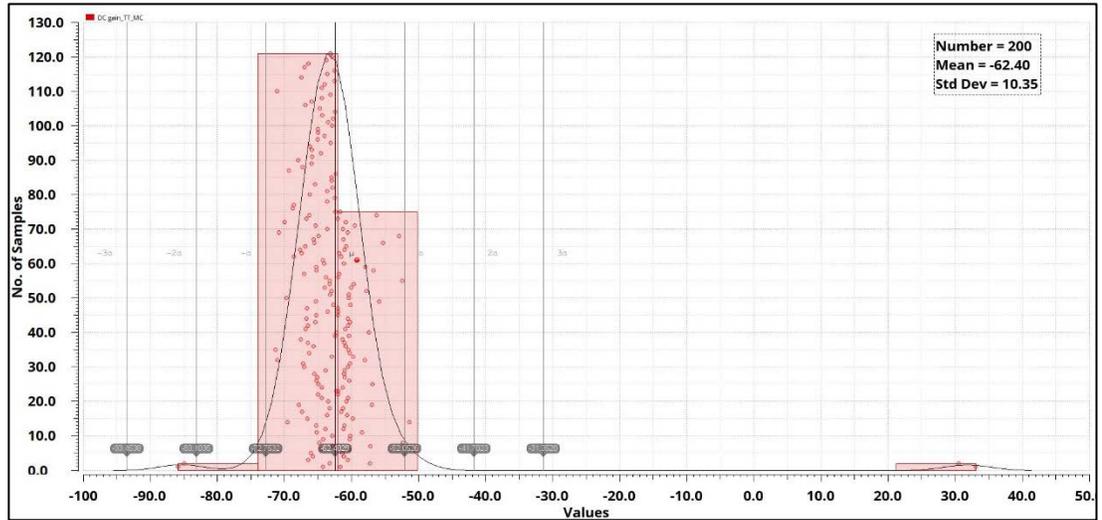


Figure 28 DC gain monte carlo plot

4.5.4 First Pole

The mean and standard deviation in this case does not apply for the first pole as the circuit is not working properly under extreme mismatch cases. Shown in Fig. 30 is a zoomed version of the first pole variations. In some cases, the first pole is 3 times the designed value which is due to the mismatches in the capacitor multiplier.

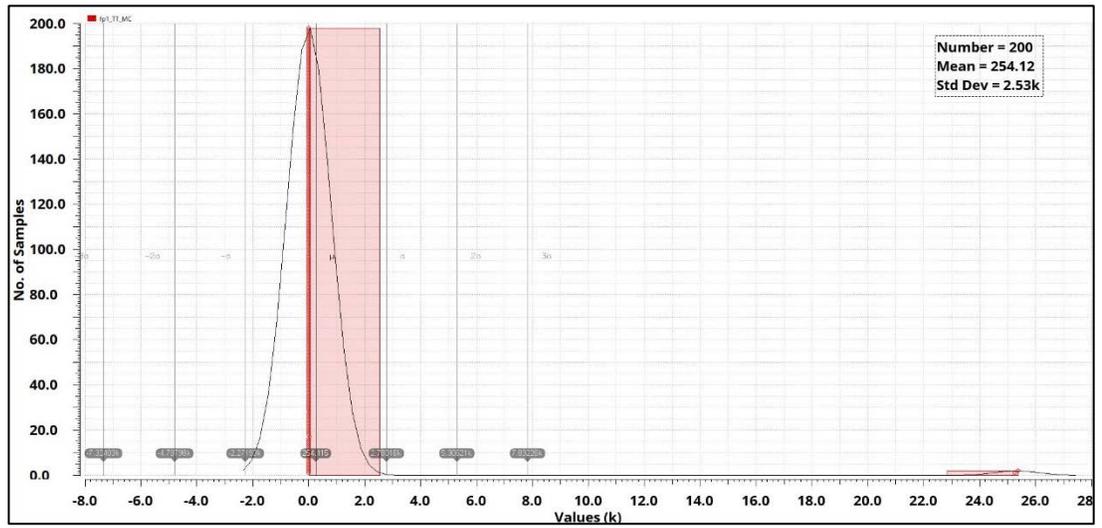


Figure 29 First pole monte carlo plot

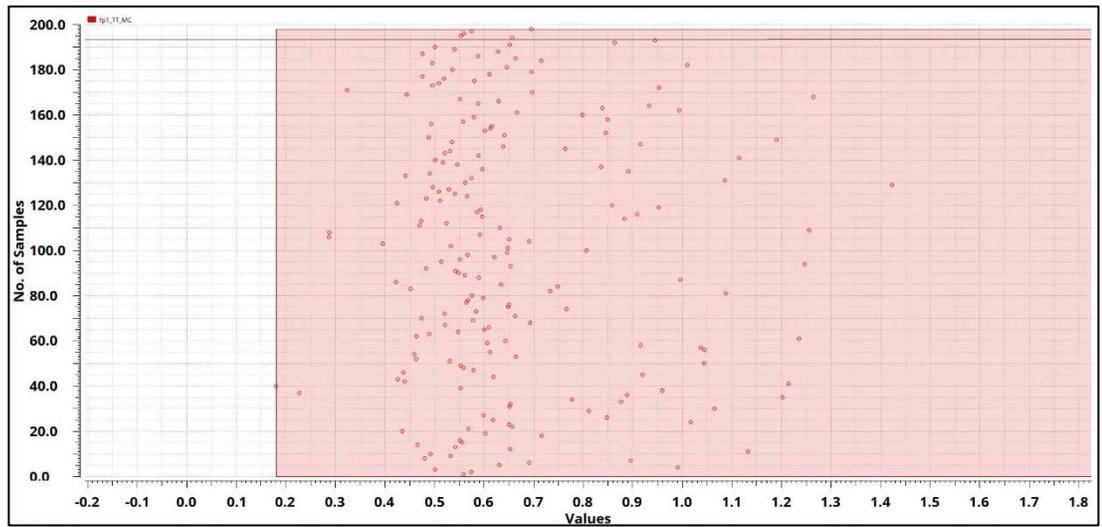


Figure 30 Zoomed version of first pole monte carlo plot

4.5.5 Second Pole

As with the first pole, the second pole monte carlo plot shows a few outliers due to the extremely low loop gain. The second pole varies as low as 2kHz for the worst case due to mismatches in G_{m0} as shown in Fig. 32.

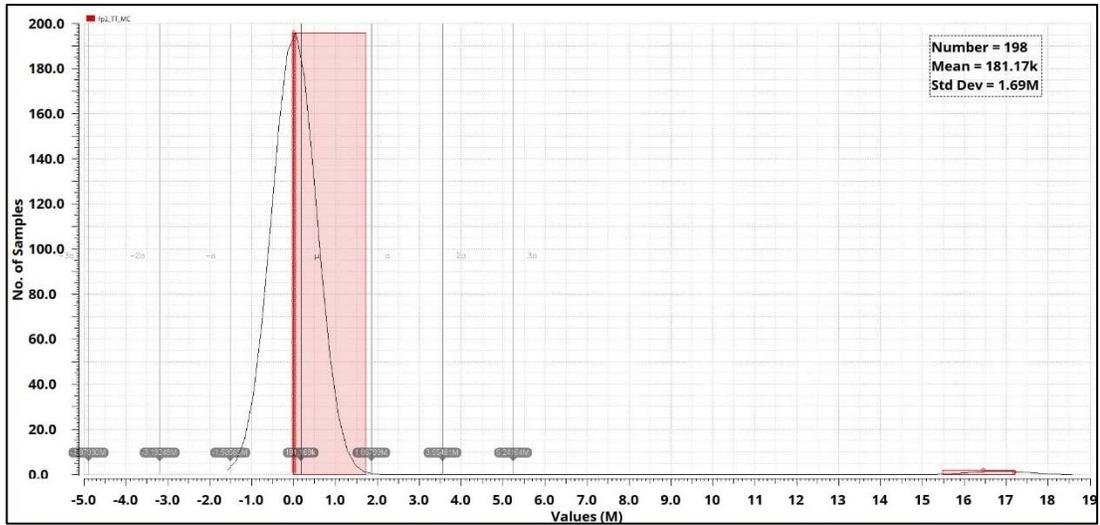


Figure 31 Second pole monte carlo plot

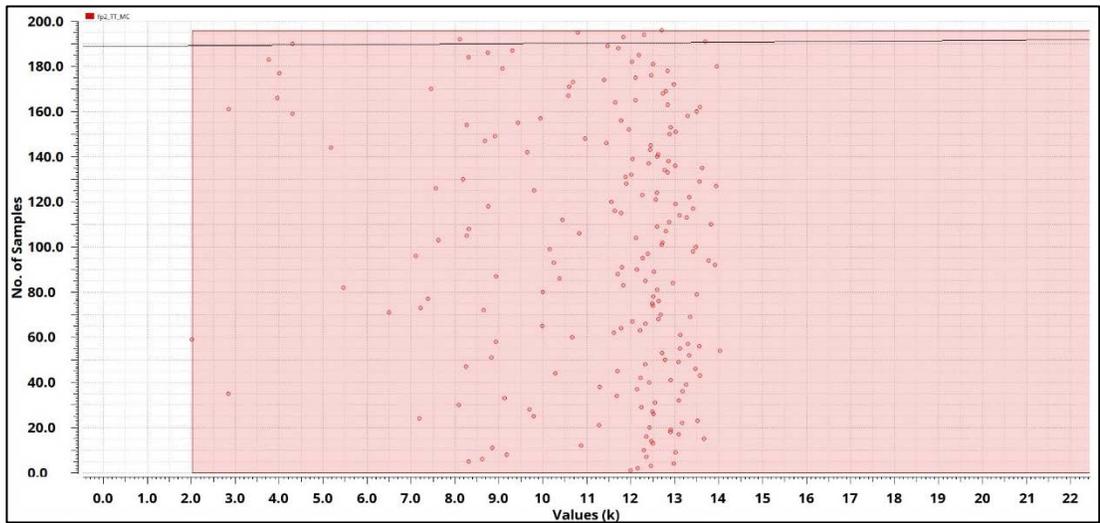


Figure 32 Zoomed version of second pole monte carlo plot

4.5.6 CMRR

The CMRR obtained has a mean of 91.35dB as shown in Fig. 33.

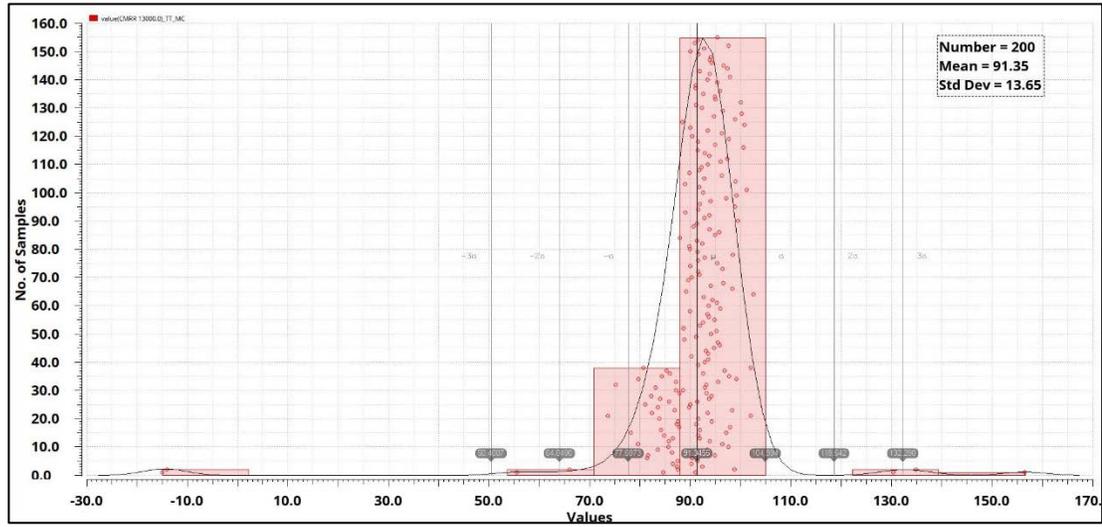


Figure 33 CMRR monte carlo plot

4.5.7 PSRR

The PSRR has a mean of 104.51dB as shown in Fig. 34.

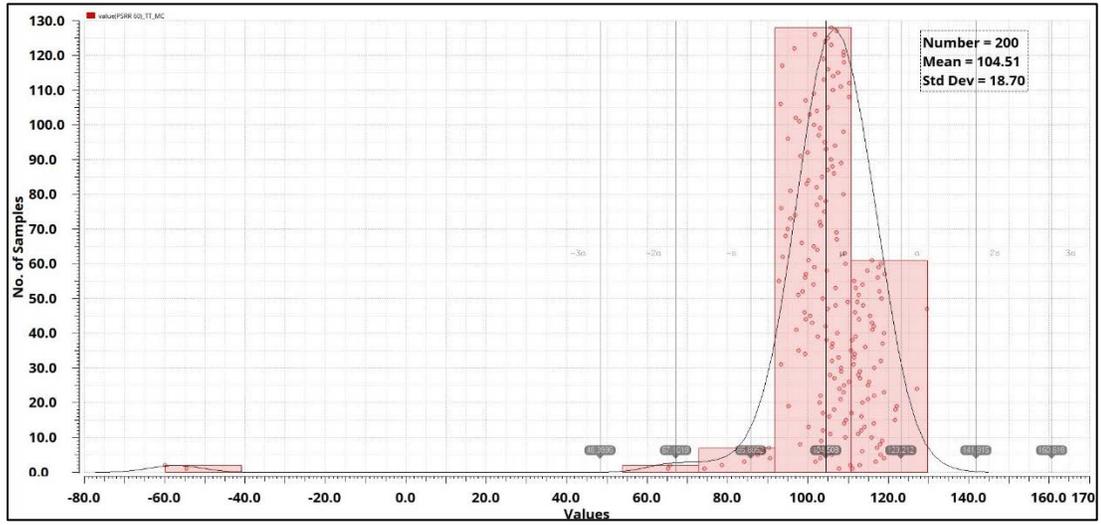


Figure 34 PSRR monte carlo plot

5 Conclusion

In conclusion, a bio-LNA with a DDA structure is verified with simulations obtaining a pass-band from 452mHz to 12.6kHz with a pass-band gain of 66.24dB. The bio-LNA suppress lower frequency artifacts and DC components by 60.22dB while achieving a CMRR and PSRR of 97.37dB and 109.8dB respectively. The total current consumption is 5.28 μ A which resulted in a NEF of 2.65 and PEF of 12.6.

This bio-LNA is not suitable for ECG signals as the first pole is too high in frequency. However, this bio-LNA can be used to acquire EEG and EMG signals as described in Table 1 Bioelectric signal characteristics [1].

5.1 Future Work

Future works of this bio-LNA includes exploring other topologies that could take advantage of the feedback loop structure which may be beneficial to other applications. A more robust capacitor multiplier is also required to eliminate the issue of matching and the effect of the equivalent series resistance. More efficient transconductance blocks is also needed to lower power consumption and input-referred noise which will lower the NEF and PEF.

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Appendices

```

1-  clc
2-  clear
3-  % close all
4-  hold on
5-  format shortEng
6
7-  syms Gm1 Gmo Gmf gm8 gm6 Vi Vo Vf ZL Zf Igml
8
9-  eq_Igml = Gm1*Vi+(gm6+gm8)*Vf;
10
11-  eq_1 = Igml == Vo/ZL + Vo*Gmo;
12
13-  eq_Vo = Vo == solve(eq_1, Vo);
14
15-  eq_Vf = -Vo*Gmf*Zf ;
16
17-  eq_Vo = Vo == solve(subs(eq_Vo,Igml,eq_Igml),Vo);
18
19-  eq_Vo = solve(subs(eq_Vo,Vf,eq_Vf),Vo)
20
21
22
23-  syms rof CL ro2 s Cf rgm
24
25-  ZL = ro2/(1+s*CL*ro2);
26-  Zf = rof/(1+s*Cf*rof);
27-  % Zf = (rof*(1+s*Cf*rgm))/(1+s*Cf*(rof+rgm));
28
29-  % This equation is taken from the output of the Matlab command window
30-  % (eq_Vo) and removing the Vi term
31-  a4 = expand( (Gm1)/(((Gmf*Zf*(gm8 + gm6))/(Gmo + 1/ZL) + 1)*(Gmo + 1/ZL) ) );
32
33-  disp('Vo/Vi = ')
34-  pretty(collect(simplifyFraction(a4)));

```

```
35
36 % a4 = subs(a4,Cf,100e-9/(2*3.142));
37 a4 = subs(a4,Cf,100e-9);
38 % a4 = subs(a4,CL,10e-12/(2*3.142));
39 a4 = subs(a4,CL,20e-12);
40 a4 = subs(a4,Gmo,1.5e-6);
41 a4 = subs(a4,Gmf,10e-9);
42
43 % a4 = subs(a4,rgm,10e6);
44 a4 = subs(a4,rof,100e12);
45 a4 = subs(a4,ro2,100e9);
46 a4 = subs(a4,Gm1,3.5e-3);
47 a4 = subs(a4,gm8,2e-6);
48 a4 = subs(a4,gm6,2e-6);
49 |
50 [n4,d4] = numden(a4);%vo/vi
51
52 sys = tf(sym2poly(n4),sym2poly(d4));
53 [z,p,k] = tf2zpk(sym2poly(n4),sym2poly(d4));
54
55 z = z/(2*pi)
56 p = p/(2*pi)
57
58 opts = bodeoptions;
59 opts.FreqUnits = 'Hz';
60 opts.Ylim = [-80 80];
61 w = logspace(-10,11,1e6);
62 bodemag(sys,w,opts);
63 grid on
```