# AN ABSTRACT OF THE THESIS OF

Yu-Wen Kuo for the degree of Master of Science in Electrical and Computer Engineering presented on May 28, 2020.

Title: Low-voltage Tracking RC Compensated OTA and a Rail-to-Rail Input and Output Operational Amplifier

Abstract approved:

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David J. Allstot

The operational transconductance amplifier (OTA) is a fundamental building block in analog and mixed-signal systems. This research describes a process-, voltage-, and temperature- (PVT) insensitive low-voltage tracking RC compensation scheme considered for two-stage CMOS OTAs, which cancels the pole due to the load capacitance using a Miller zero generated by the frequency compensation network. A low-voltage current source with no back-gate effect (a "k' generator" or a peaking current source) is used to generate the bias currents for the OTA. This architecture implemented in a TSMC 180nm CMOS process, achieves a 2X power reduction compared to a widely-used active-RC compensation scheme. Also, a rail-to-rail input and output operational amplifier is designed in a 180nm process with a complementary input pair and a class-AB output stage.

# Low-voltage Tracking RC Compensated OTA and a Rail-to-Rail Input and Output Operational Amplifier

by

Yu-Wen Kuo

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Dean of the Graduate School

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# Chapter 1: Introduction

## 1.1 Overview

The operational transconductance amplifier (OTA) is a basic building block in many analog and mixed-signal integrated circuit systems. It is widely used in feedback amplifiers, filters, analog-to-digital converters (ADCs), linear regulators, etc. The specification requirements in those systems are highly dependent on amplifier performance. Even though the amplifier applications are many, the OTA topologies available for use in them are relatively limited. The most popular topology of a CMOS operational transconductance amplifier is the two-stage amplifier which consists of a differential-to-single-ended input stage and a common-source second stage. In order to meet the specifications of unity-gain bandwidth, phase margin, and small-signal settling-time, the Miller compensation technique for pole-splitting has evolved over many decades of research. Subsequently, the compensation technique that uses an MOS nulling resistor and achieves PVT, process, voltage, and temperature, insensitive pole-zero tracking was introduced in 1980 [1]. This technique achieves significant power reduction comparing to other designs, and it is still being used in the industry nowadays. Also, another improved frequency compensation technique which removed the RHP zero by introducing a current buffer was described by Ahuja [2]. Frequency compensation in amplifiers is one of the most critical topics in analog design, and some of them are reported in the literature.

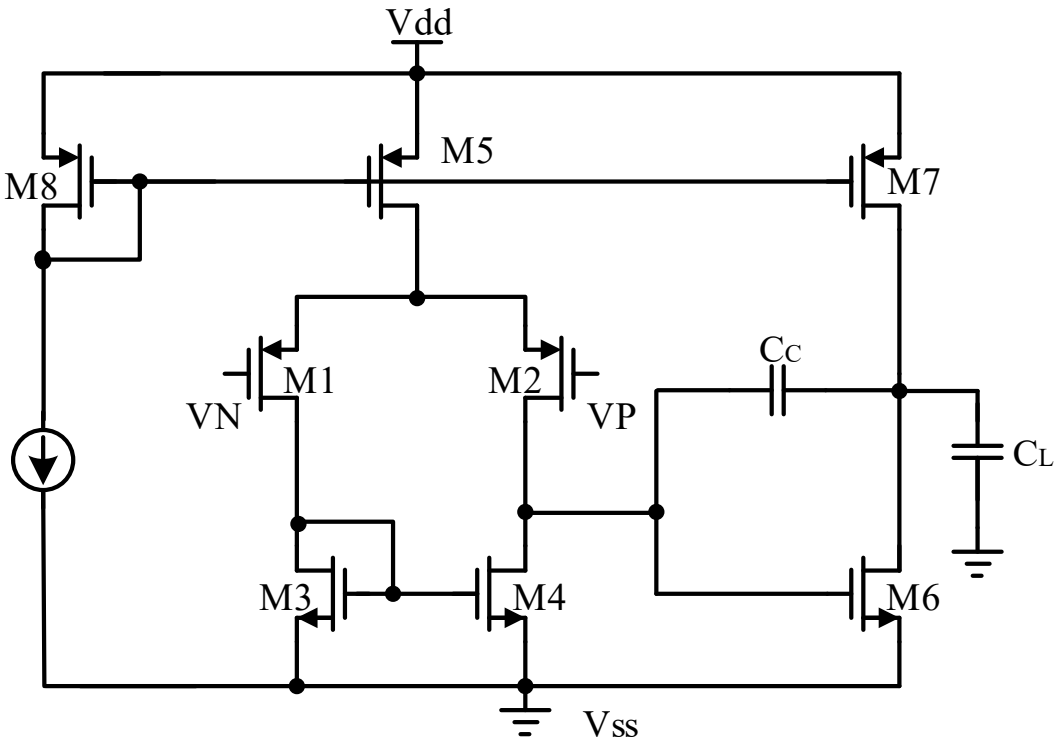


Figure 1.1: Conventional Miller compensated two-stage operational amplifier

## 1.2 Literature Review of CMOS Amplifiers

The most popular CMOS two-stage operational transconductance amplifier (OTA) is shown Fig. 1.1 consists of a first stage, a second stage, a bias circuit, and a frequency compensation network. Fig. 1.2 shows the small-signal model for the conventional Miller compensated amplifier. In the equivalent circuit, $C_1$ represents the total capacitance at the output of the first stage.

$$C_1 = C_{GD2} + C_{DB2} + C_{GD4} + C_{DB4} + C_{GS6} \tag{1.1}$$

Besides, $C_2$ stands for the capacitance between the output of second stage and ground.

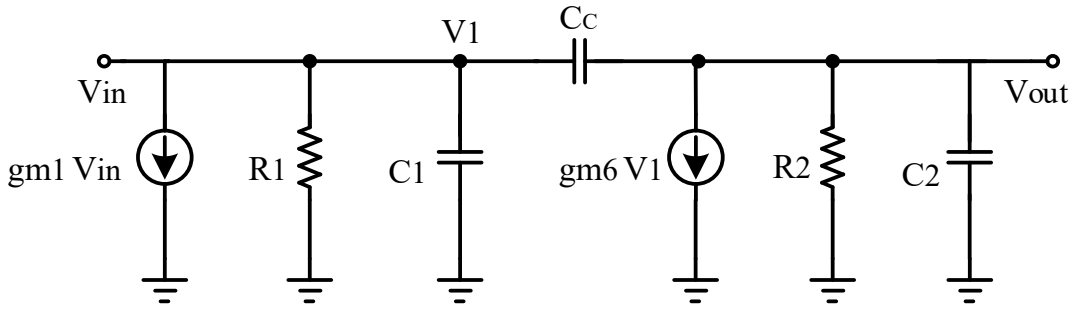


Figure 1.2: Small-signal model of conventional Miller compensated OTA

$$C_2 = C_{DB6} + C_{DB7} + C_{GD7} + C_L \tag{1.2}$$

Generally, $C_L$ is greater than the other parasitics so $C_2$ is much greater than $C_1$. By KCL, Eqns. (1.3) and (1.4) can be obtained as:

$$gm_1 V_{in} + \frac{V_1}{R_1} + sC_1 V_1 + sC_C\left(V_1 - V_{out}\right) = 0 \tag{1.3}$$

$$gm_6 V_1 + \frac{V_{out}}{R_2} + sC_2 V_{out} + sC_C\left(V_{out} - V_1\right) = 0 \tag{1.4}$$

The transform function of the two-stage Miller compensated amplifier can be derived by solving two equations above as:

$$\frac{V_{out}}{V_{in}} = \frac{gm_1\left(gm_6 - sC_C\right)R_1R_2}{s^2\left\{\left[C_1C_2 + C_C\left(C_1 + C_2\right)\right]R_1R_2\right\} + s\left[C_1R_1 + C_2R_2 + C_C\left(gm_6R_1R_2 + R_1 + R_2\right)\right] + 1} \tag{1.5}$$

From the equation, the approximate pole and zero frequencies are :

$$z_1 = \frac{gm_6}{C_C} \tag{1.6}$$

$$p_1 = -\frac{1}{R_1 R_2 gm_6 C_C} \tag{1.7}$$

$$p_2 = -\frac{gm_6}{C_L} \tag{1.8}$$

After considering $z_1$ in the phase domain the right-half-plane (RHP) zero behaves the same as left-half-plane (LHP) pole which degrades the performance of the phase margin. On the other hand, the compensation capacitance $C_C$ needs to be increased in order to split the poles to maintain the stability of the circuit. However, the frequency of the RHP zero will decrease at the same time which sacrifices the phase margin. To mitigate the effect of the RHP zero, there are some techniques published to address the issue.

### 1.2.1 Pole-Zero Tracking using MOS Nulling Resistor

RC compensation is a very famous techniques used for the compensation network in amplifiers. Usually, in amplifier designs, the unity-gain bandwidth should not be greater than the settling time requirements too much in order to minimize broadband noise. In [1], a PVT-insensitive compensation technique is achieved. There is no large bandwidth needed to meet the settling time requirement. Fig 1.3 shows the equivalent circuit in [1], from which it can be found that

$$p_2 = -\frac{gm_2}{C_L} \tag{1.9}$$

$$z_1 = -\frac{1}{R_f C_f - \frac{C_f}{gm_2}} \tag{1.10}$$

The compensation in this paper is placing the zero atop the non-dominant pole, which occurs for

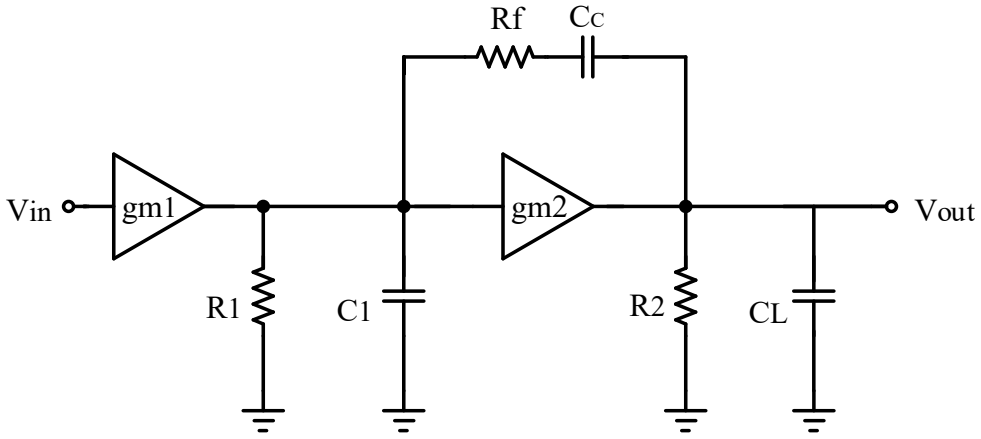


Figure 1.3: Small-signal model of RC compensation method

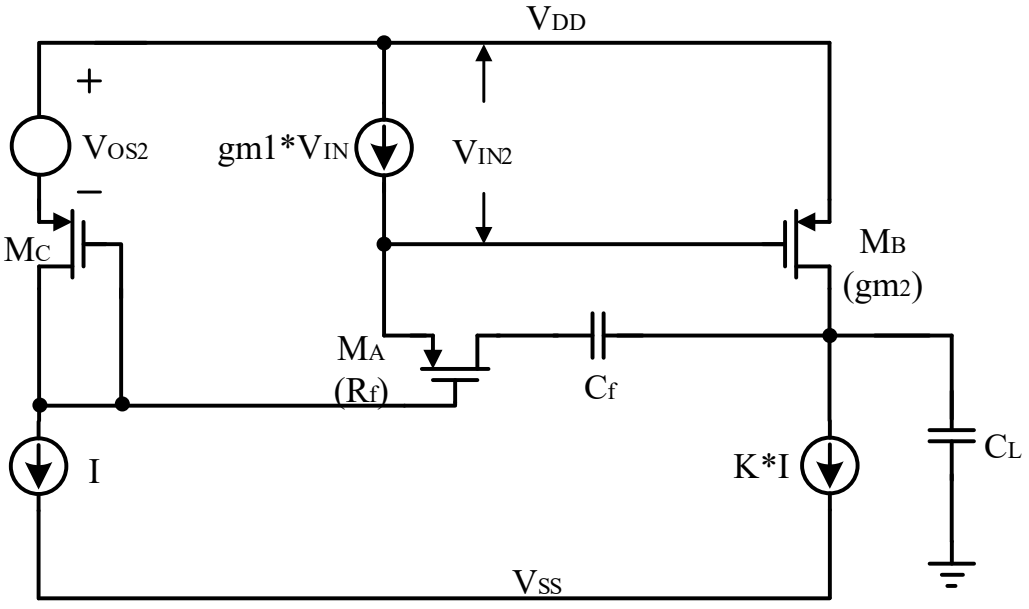


Figure 1.4: Tracking RC compensation

$$R_f = \left( \frac{C_L + C_f}{C_f} \right) \times \frac{1}{gm_2} \tag{1.11}$$

For the same stability requirement, the pole-zero cancellation technique requires a smaller compensation capacitance compared to the pole-split amplifier which makes the noise performance better. In Figure 1.4, the transistor $M_A$ biased by the transistor $M_C$ and current I acts as a compensation resistance, which in series with the compensation capacitor $C_f$ forms the compensation network. $V_{IN2}$ stands for input voltage to the of output stage, and its quiescent value is equal to $V_{OS2}$. The output stage comprises a transistor $M_B$ biased by current K*I, and the output node is connected to a load capacitor, $C_L$. By the MOS model, Eqn. 1.12 can be obtained

$$\left( \frac{W}{L} \right)_A = \left[ \left( \frac{W}{L} \right)_B \times \left( \frac{W}{L} \right)_C \times K \right]^{\frac{1}{2}} \times \left( \frac{C_f}{C_L + C_f} \right) \tag{1.12}$$

Eqn. 1.12 is independent of PVT so a robust pole-zero cancellation is achieved which has no settling time issues. Moreover, this technique allows for a small bias current and a small compensation capacitor to reach the same performance.

## 1.2.2 Embedded Tracking Compensation

Another technique that guarantees the tracking compensation in the circuit is using a real resistor as compensation resistor and relating the transconductance of the output stage with a resistor which matches the compensation resistor [3]. Fig. 1.5 indicates the method of defining gm7 with respect to RS. The relationship of the bias current is

$$I_B \propto \left( K_n' R_S^{\,2} \right)^{-1} \tag{1.13}$$

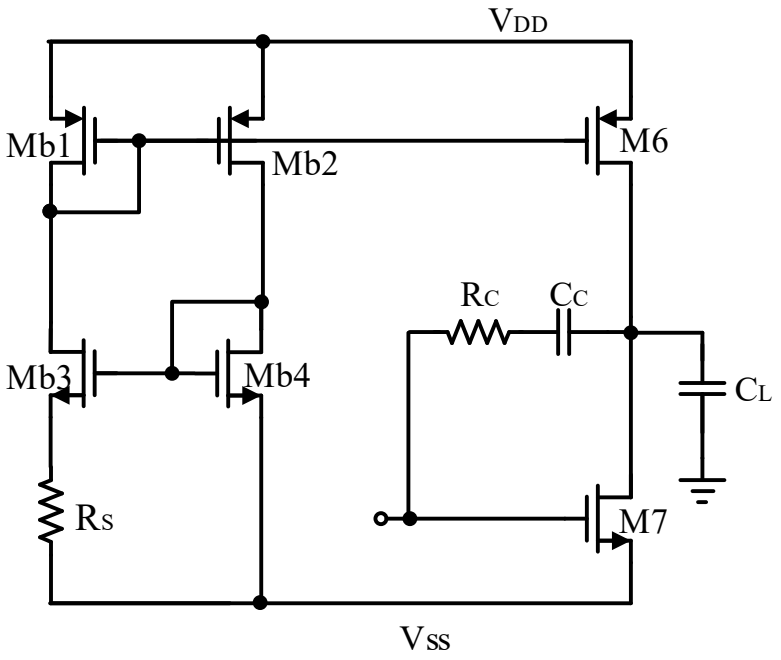


Figure 1.5: Method of relating $g_{m7}$ with $R_S$

Therefore, the frequency of the second pole is inversely proportional to $R_S$ (Eqn. 1.14), and also the frequency of the zero is inversely proportional to $R_C$ (Eqn. 1.15).

$$P_2 \propto \left(R_S\right)^{-1} \tag{1.14}$$

$$Z_1 \propto \left(R_c\right)^{-1} \tag{1.15}$$

With the two equations above, it is obvious that the frequency compensation does not vary with process, voltage, and temperature variations if $R_S$ and $R_C$ are of the same type and match each other. In conclusion, a tracking pole-zero cancellation with a fast settling time is maintained.

## 1.3 Thesis Organization

In this research, Chapter 1 illustrates a process-, voltage-, and temperature- (PVT) insensitive low-voltage tracking RC compensation scheme which cancels the pole due to the load capacitance using a Miller zero generated by the frequency compensation network. In Chapter 2, the fundamental knowledge of the conventional tracking frequency compensation design is described. In Chapter 3, a proposed architecture for low-voltage frequency compensation is shown. The comparisons of simulation results between the conventional design and the low-voltage one are given. In Chapter 4, a detailed design procedure for a rail-to-rail amplifier is presented. With a design example, the operation principles for rail-to-rail input and output are illustrated. Chapter 5 concludes this thesis and presents future research in the frequency compensation of amplifiers and rail-to-rail amplifier techniques.

# Chapter 2: Conventional Tracking Frequency Compensated OTA

## 2.1 Overview

In the Miller-capacitor-compensated OTA, the dominant pole moves to a lower frequency and the non-dominant pole pushes to higher frequency which degrades the bandwidth. Besides, a right-half-plane (RHP) zero is created owing to its direct feedforward path from the output of first stage to the output of amplifier which reduces the gain and phase margins severely. Solutions have been proposed to mitigate it by implementing unity-gain voltage/current buffers [2], [4]. Furthermore, pole-zero cancellation techniques also eliminate this issue by cancelling the non-dominant pole [1], [3], [5]-[6]. This technique is more popular since it consumes less power and requires a smaller die area.

## 2.2 Small Signal Analysis

In Fig. 2.1, where an NMOS biased in the triode region acts as a resistor in series with the compensation capacitor $C_C$, the RHP zero is moved into the LHP to cancel the non-dominant pole (Fig. 2.2). The pole and zero frequencies are shown in Eqn. 2.1 and 2.2 respectively.

$$p_2 = -\frac{gm_7}{C_L} \tag{2.1}$$

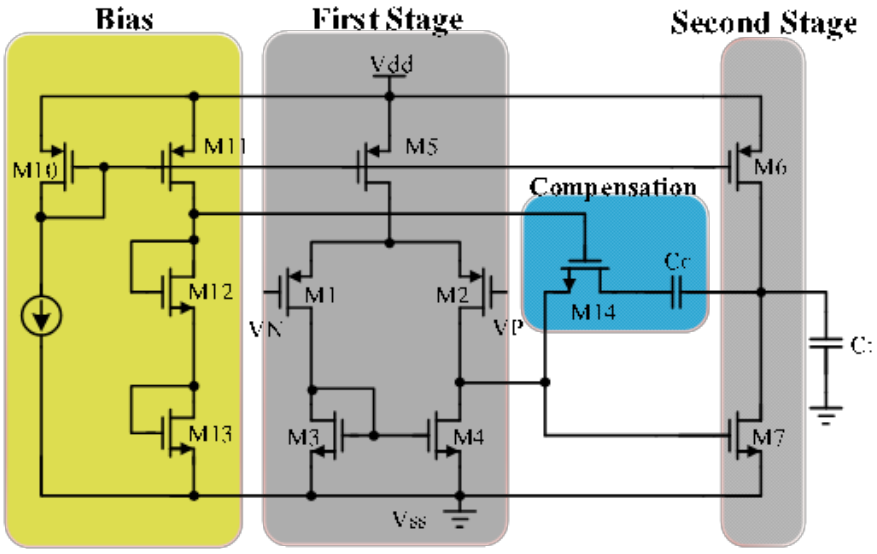


Fig 2.1: Conventional PVT-insensitive tracking frequency compensated OTA

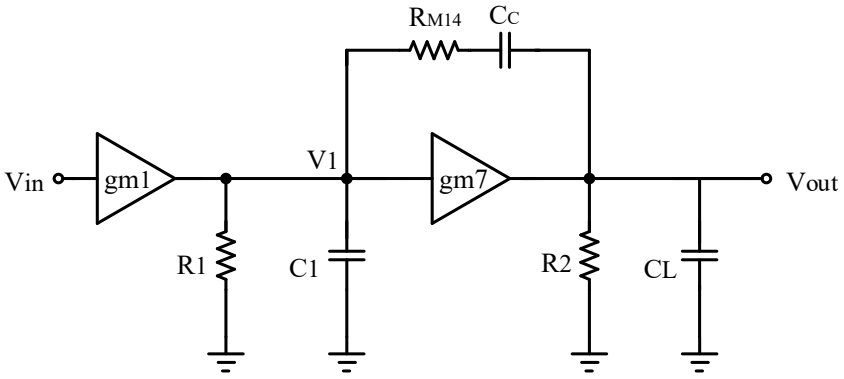


Fig 2.2: Block-level schematic of a Conventional PVT-insensitive tracking frequency compensated OTA

$$z_1 = -\frac{1}{C_C(R_{M14} - \frac{1}{gm_7})} \tag{2.2}$$

The frequency of the non-dominant pole is proportional to the transconductance of transistor $M_7$ in the second stage (Eqn 2.1). Therefore, if $R_{M14}$ can be realized to track the inverse of transconductance which is $1/g_{m7}$ (Eqn. 2.2), the zero will also be proportional to $g_{m7}$ as is the non-dominant pole. That is, the zero frequency will remain relative to the non-dominant pole frequency which achieves process and temperature insesitive frequency compensation. The resistance $R_{M14}$ in Eqn. 2.2 is implemented using a triode-mode NMOS biased by the same current source as the NMOS second stage $M_7$ (Fig. 2.1). In this way, $R_{M14}$ will be proportional to $1/g_{m7}$ which leads the pole-zero cancellation technique to be PVT-insensitive. The proof is shown as follows [7].

The equivalent resistance of $R_{M14}$ is given by Eqn. 2.3, and the transconductance of $g_{m7}$ is shown in Eqn. 2.4

$$R_{M14} = \frac{1}{\mu_n C_{OX}\left(\frac{W}{L}\right)_{14} V_{OV14}} \tag{2.3}$$

$$gm_7 = \mu_n C_{OX}\left(\frac{W}{L}\right)_7 V_{OV7} \tag{2.4}$$

The product of $R_{M14}$ $g_{m7}$ can be obtained as

$$R_{M14} gm_7 = \frac{(\frac{W}{L})_7 V_{OV7}}{(\frac{W}{L})_{14} V_{OV14}} \tag{2.5}$$

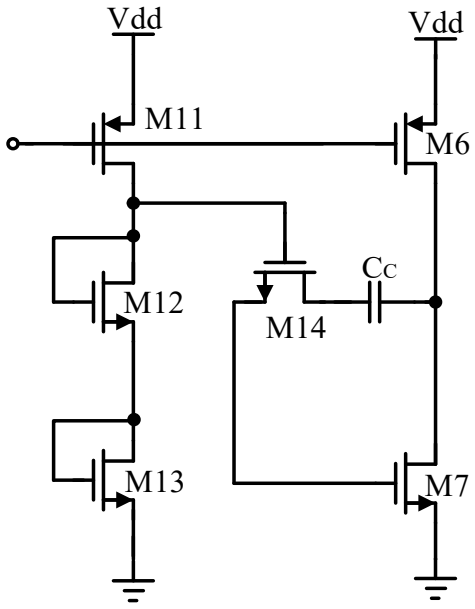


Fig 2.3: The bias circuit, second stage, and compensation network of the two-stage OTA

In order to ensure Eqn. 2.5 is PVT insensitive, $V_{OV14}/V_{OV7}$ has to be independent of temperature and process variations. Therefore, $M_{14}$ is biased by the same current source as NMOS $M_7$ in the second stage. Firstly, the gate-to-source voltages of $M_7$ and $M_{13}$ should be equal.

$$V_{GS7} = V_{GS13} \tag{2.6}$$

Since gate-to-souce voltage equates to the overdive voltage ($V_{OV}$) plus the thresheld voltage ($V_{TH}$), Egn. 2.6 can be implenmented by setting

$$V_{OV7} = V_{OV13} \tag{2.7}$$

By calculaiton, the following equation is derived

$$\sqrt{\frac{2I_{D7}}{\mu_n C_{OX}\left(\frac{W}{L}\right)_7 V_{OV7}}} = \sqrt{\frac{2I_{D13}}{\mu_n C_{OX}(\frac{W}{L})_{13} V_{OV13}}} \tag{2.8}$$

Rearranging Eqn. 2.8, it can be obtained that

$$\frac{I_{D7}}{I_{D13}} = \frac{(\frac{W}{L})_7}{(\frac{W}{L})_{13}} \tag{2.9}$$

The current ratio is realated to the sizes of current mirror transistors $M_6$ and $M_{11}$

$$\frac{I_{D7}}{I_{D13}} = \frac{(\frac{W}{L})_6}{(\frac{W}{L})_{11}} \tag{2.10}$$

To ensure that $V_{OV7} = V_{OV13}$ the following equation must be satisfied:

$$\frac{(\frac{W}{L})_6}{(\frac{W}{L})_7} = \frac{(\frac{W}{L})_{11}}{(\frac{W}{L})_{13}} \tag{2.11}$$

$V_{GS7} = V_{GS13}$ will be satisfied if Egn 2.11 is set. The gate voltages of $M_{12}$ and $M_{14}$ are the same so $V_{OV12} = V_{OV14}$. Assuming that the current flows through $M_{11}$ and $M_6$ are identical,

$$\frac{V_{OV7}}{V_{OV14}} = \frac{V_{OV13}}{V_{OV12}} = \frac{\sqrt{\frac{2I_{D13}}{\mu_n C_{OX}(\frac{W}{L})_{13} V_{OV13}}}}{\sqrt{\frac{2I_{D12}}{\mu_n C_{OX}(\frac{W}{L})_{12} V_{OV12}}}} = \sqrt{\frac{(\frac{W}{L})_{12}}{(\frac{W}{L})_{13}}} \tag{2.12}$$

Lastly, substituting Eqn. 2.12 into Eqn. 2.5, gives equation shown below

$$R_{M14}gm_7 = \frac{(\frac{W}{L})_7}{(\frac{W}{L})_{14}}\sqrt{\frac{(\frac{W}{L})_{12}}{(\frac{W}{L})_{13}}} \tag{2.13}$$

In Eqn. 2.13, the compensation resistor $R_{M14}$ realized by a transistor biased in the triode region is inversely proportional to the transconductance of $M_7$. Also, the pole-zero cancellation occurs for

$$R_{M14} = \frac{1}{gm_7}\left(1+\frac{C_L}{C_C}\right) \tag{2.14}$$

Thus, if $C_C$ and $C_L$ are of the same type, the pole and zero frequencies track each other which ensures that the frequency compensation is independent of PVT variations.

## 2.3 Design Considerations

Although the conventional approach is robust against PVT variations with an on-chip resistor, it is supply-voltage-limited because of the two diodes ($M_{12}$ and $M_{13}$) in the bias network. Thus, the minimum $V_{DD}$ value required is

$$V_{DD,\min} = V_{OV11} + V_{GS12} + V_{GS13} = 2V_T + 3V_{OV} \tag{2.15}$$

The pole zero cancellation is within the unit-gain frequency so any mismatches in frequency cancellation creates a doublet which degrades the settling time performance. With $V_{DD}$ below this minimum value (Eqn. 2.15) the pole-zero cancellation is lost, which results in a doublet that causes significant settling-time issues [8]. The output voltage in response to a step of voltage is

$$V_{out}(t) = V_{step}\left(1 - k_1 e^{-\omega_\mu t} + k_2 e^{-\frac{t}{t_z}}\right) \tag{2.16}$$

According to Eqn. 2.16, since the zero is within the unit-gain frequency, the zero will result in slow settling. Also, the tracking technique involves matching the small-signal square-law transconductance of the second-stage transistor with a linear (square-law) ON resistance of the transistor that realizes $R_C$.

# Chapter 3: Low-Voltage Tracking Frequency Compensated OTA

## 3.1 Overview

A major challenge in analog circuit design during recent times is the ever-smaller power supply voltages owing to technology scaling. With short channel effects, the intrinsic gain of the amplifier is degraded dramatically. It is difficult to achieve the same performance with a low supply voltage since it reduces many circuit performances such as gain, output swing, and slew rate. One solution is to use the multistage topologies for amplifiers [10-12]; however, it makes the frequency compensation more complicated and reduces the gain bandwidth performance.

The low-voltage tracking frequency compensation technique described in this thesis enables operation at a lower supply voltage and eliminates the requirement for square-law operation, both of which are attractive for deeply scaled technologies. Instead of using an NMOS transistor biased in the (square law) linear region ($M_{14}$ in Fig. 2.1), the Miller resistance is realized using a resistor $R_C$ of the same type as a bias resistor, $R_B$, in the bias circuit. The architecture, implemented in a TSMC 180nm CMOS process, achieves a 2X power reduction compared to an equivalent active-RC compensated design. The low-voltage RC tracking frequency compensation scheme for two-stage CMOS OTAs is presented.

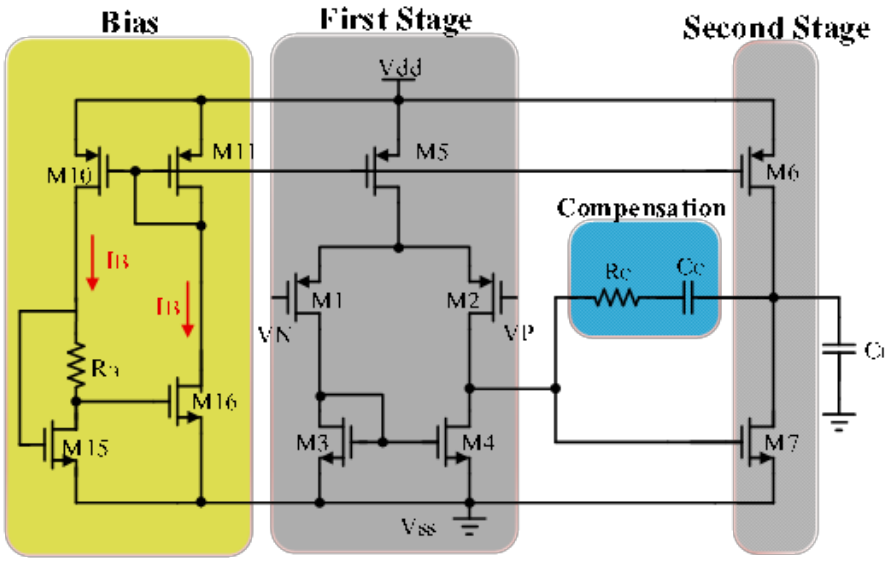


Fig 3.1: Low-Voltage PVT-insensitive tracking frequency compensated OTA

## 3.2 Bias Circuit

Fig. 3.1 shows the complete circuit of the OTA including the k'-generator bias circuitry. $M_{10}$ and $M_{11}$ comprise a simple current mirror which biases the first stage current mirror transistor $M_5$ and second stage current mirror transistor $M_6$. $M_{15}$ in the bias circuitry is a self-biased using $R_B$ which sets the DC bias current and $g_{m15}$ in the circuit. The current mirror $M_{11}$ and $M_{10}$ forces the bias current flow through $M_{15}$ and $M_{16}$ to be equal.

$$I_B = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_{15}\left(V_{GS15} - V_{TH}\right)^2 = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_{16}\left(V_{GS16} - V_{TH}\right)^2 \quad (3.1)$$

Eqn. 3.2 can be derived from the circuit as

$$V_{GS16} = V_{GS15} - I_B R_B \quad (3.2)$$

With Eqn. (3.1) and (3.2), the following eqation can be found:

$$\sqrt{\frac{2I_B}{\mu_n C_{OX}(W/L)_{16}}} = \sqrt{\frac{2I_B}{\mu_n C_{OX}(W/L)_{15}}} - I_B R_B \tag{3.3}$$

By rearranging (3.3), the DC bias current is derived as:

$$I_B = \frac{2}{\mu_n C_{OX} R_B^{\,2}} \left( \sqrt{\frac{1}{(W/L)_{15}}} - \sqrt{\frac{1}{(W/L)_{16}}} \right)^2 \tag{3.4}$$

Eqn. 3.4 can also be rewritten as

$$R_B = \frac{2}{\sqrt{2\mu_n C_{OX}(W/L)_{16} I_B}} \left( \sqrt{\frac{(W/L)_{16}}{(W/L)_{15}}} - 1 \right) \tag{3.5}$$

$$gm_{16} = \sqrt{2\mu_n C_{OX}(W/L)_{16} I_B} \tag{3.6}$$

Substituing Eqn. 3.6 into Eqn. 3.5,

$$gm_{16} = \frac{2}{R_B} \left( \sqrt{\frac{(W/L)_{16}}{(W/L)_{15}}} - 1 \right) \tag{3.7}$$

From (3.4), the bias current is determined by the bias resistance, $R_B$, process parameter $\mu_n C_{OX}$, the aspect ratios of $M_{15}$ and $M_{16}$, and is independent of the power supply voltage, $V_{DD}$. As for Eqn. 3.6, the transconductance of $M_{16}$ only depends on the bias resistor value and the aspect ratios of $M_{16}$ and $M_{15}$.

One significant advantage is shown by comparing the compensation circuit with $R_{M14}$ in Fig. 2.1 to the compensation circuit with $R_C$ in Fig. 3.1. Since $R_C$ does not require a bias voltage, the minimum power supply voltage can be reduced to

$$V_{DD,\min} = V_{SG11} + V_{OV16} = V_T + 2V_{OV} \tag{3.8}$$

Hence, this low voltage compensated OTA can operate at a lower supply voltage than widely-used RC compensation circuit. Another advantage of using the k'-generator bias circuit shown is no body effect because the sources of both $M_{15}$ and $M_{16}$ are connected to $V_{SS}$. Without the second-order effect, the current source is more accurate than other topologies. The last interesting attribute is that the gate voltage of $M_7$ is derived from and can be made the same as the gate voltage of $M_{16}$. These gate voltages are applied to the compensation resistor $R_C$ and bias resistor $R_B$, respectively. Therefore, the resistance variations due to resistor voltage coefficients are similar with respect to PVT variations. That is, resistance variations due to the voltage coefficient track and do not affect the pole-zero cancellation. However, since there are two stable operating points in the k'-generator bias circuit, a startup circuit is essential for it, which moves the operating point from zero current to the desired DC bias point.

## 3.3 PVT Tracking Compensation

The transconductance of $M_7$ in Fig. 3.1 is given by

$$gm_7 = \sqrt{2\mu_n C_{OX}(W/L)_7 I_7} \tag{3.9}$$

and the DC bias currents through $M_7$ and $M_{11}$ are related as:

$$I_7 = \frac{(W/L)_6}{(W/L)_{11}} I_B \tag{3.10}$$

From Eqn. 3.9 and 3.10, we obtain

$$gm_7 = \sqrt{2\mu_n C_{OX}(W/L)_7 \left(\frac{(W/L)_6}{(W/L)_{11}} I_B\right)} \tag{3.11}$$

Substitution of $I_B$ from (3.4) into (3.11) gives:

$$gm_7 = \sqrt{2\mu_n C_{OX}(W/L)_7 \frac{(W/L)_6}{(W/L)_{11}} \left[ \frac{2}{\mu_n C_{OX} R_B^{\,2}} \left( \sqrt{\frac{1}{(W/L)_{15}}} - \sqrt{\frac{1}{(W/L)_{16}}} \right)^2 \right]} \quad (3.12)$$

Simplifying the above equation, $g_{m7}$ is given as a function of $R_B$ as

$$gm_7 = \frac{2}{R_B} \left( \frac{1}{\sqrt{(W/L)_{15}}} - \frac{1}{\sqrt{(W/L)_{16}}} \right) \times \sqrt{\frac{(W/L)_7 (W/L)_6}{(W/L)_{11}}} \quad (3.13)$$

Hence, the transconductance $g_{m7}$ depends only on $R_B$ and the transistor aspect ratios. For pole-zero cancellation, $R_C$ is found from Eqn. 2.14 to be:

$$R_C = \frac{1}{gm_7} \left( 1 + \frac{C_L}{C_C} \right) \quad (3.14)$$

Finally, substituting for $g_{m7}$ from (3.14) gives:

$$\frac{R_C}{R_B} = \frac{1 + \frac{C_L}{C_C}}{2 \left( \frac{1}{\sqrt{(W/L)_{15}}} - \frac{1}{\sqrt{(W/L)_{16}}} \right) \times \sqrt{\frac{(W/L)_7 (W/L)_6}{(W/L)_{11}}}} \quad (3.15)$$

It can be noted that $R_C/R_B$ only depends on a capacitance ratio, primary determined by gate oxide, and aspect ratios which do not vary significantly across PVT. As a result, if $R_C$ and $R_B$ are of the same type, the compensation will be independent of PVT, and a robust pole-zero cancellation is achieved.

## 3.4 Simulation Result Comparisons with Conventional Amplifier

The low-voltage tracking frequency compensated OTA was designed and implemented using the TSMC 180nm CMOS process. We also designed a conventional RC-compensated OTA with identical specifications to compare the circuit performances. The power supply voltages were scaled down from 1.8V to 1V to analyze the differences between those two schemes. The conventional compensated OTA does not work functionally at a lower supply since there are two diode voltages required to bias the current mirror in the bias circuitry.

The desired specifications and transistor sizes of the low-voltage compensated OTA design are shown in the following tables, respectively.

| Specification | Value |
|---|---|
| DC Gain | $> 60dB$ |
| UGB | $> 20MHz$ |
| Phase Margin | 60° |
| CL | $5pF$ |

Table 3.1: Specifications of the two compensation topologies

### 3.4.1 Stability

The stability performances of the conventional and low-voltage compensated OTAs were simulated in unity-gain buffer configurations. The loop frequency responses of the schematic and extracted for both approaches are shown in Fig. 3.2 and 3.3,

| | |
|---|---|
| M1, M2 | 5.2um x 5 / 1um |
| M3, M4 | 5.2um x 1 / 1um |
| M5 | 7um x 4 / 1um |
| M6 | 7um x 4 / 1um |
| M7 | 5um x 2 / 1um |

Table 3.2: Transistors' sizes of low-voltage compensated OTA

respectively. For the conventional compensated OTA, the loop gain is 73.5dB, UGB is 28.4MHz, and the phase margin is 63.9°. As for the low-voltage compensated OTA, the loop gain is 73.5dB, UGB is 28.8MHz, and the phase margin is 64.1°. Both designs show nearly identical specifications.

### 3.4.2 Pole and Zero Frequencies

As the supply voltage scales down, the conventional compensated OTA can no longer sustain sufficient voltage for the bias network which biases the compensation resistor realized as a triode region MOS ($M_{14}$ in Fig. 2.1). While $V_{DD}$ decreases, $M_{11}$ will go into the triode region $M_{12}$ and $M_{13}$. Fig. 3.4 shows the relationship between the gate voltage of $M_{14}$ and its equivalent resistance $R_{14}$ versus supply voltage. As shown in Eqn. 3.16, as the supply voltage decreases, the gate-to-source voltage of $M_{14}$ goes down as well. As $V_{DD}$ decreases, $R_{14}$, the equivalent resistance of $M_{14}$, dramatically increases by more than 25X. Therefore, the pole-zero frequency mismatches occur,

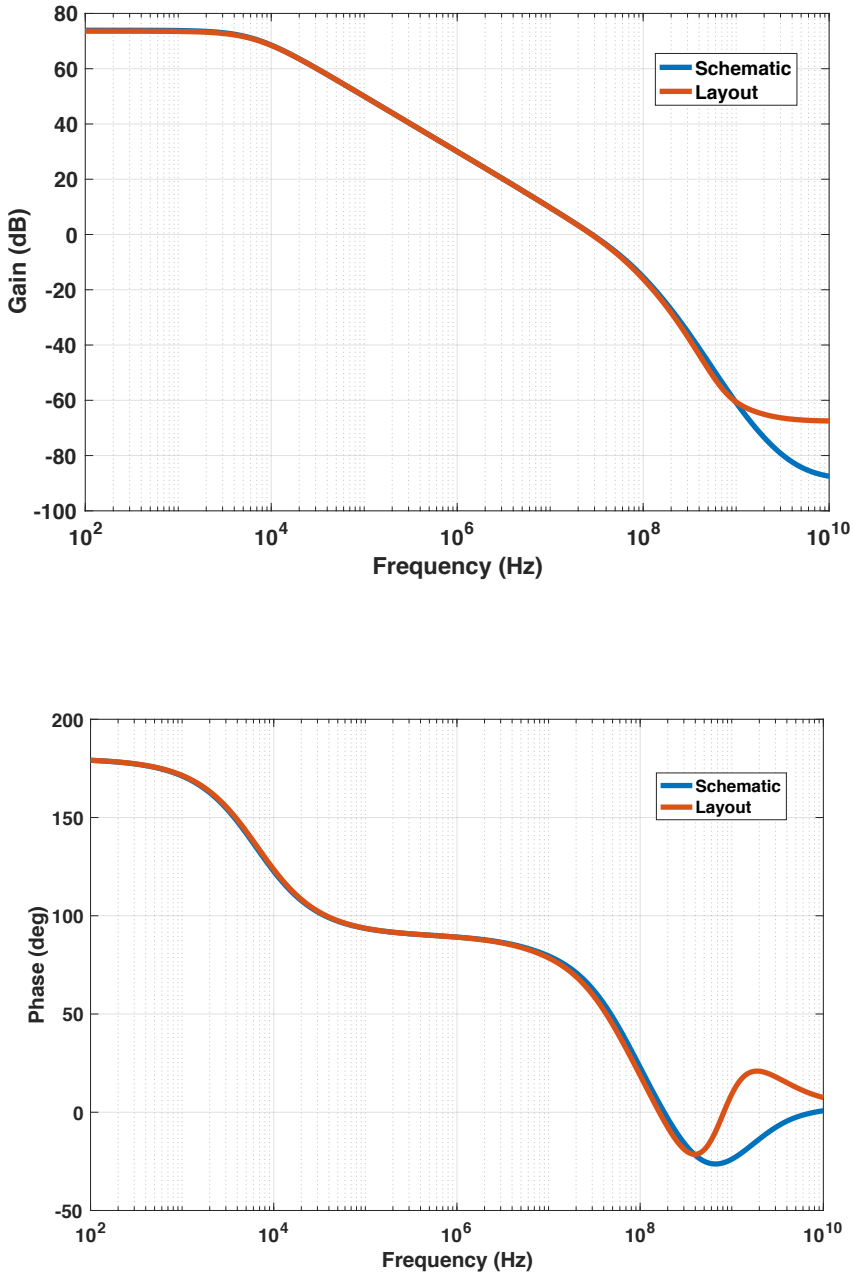


Fig 3.2: Loop gain bode plot of conventional OTA

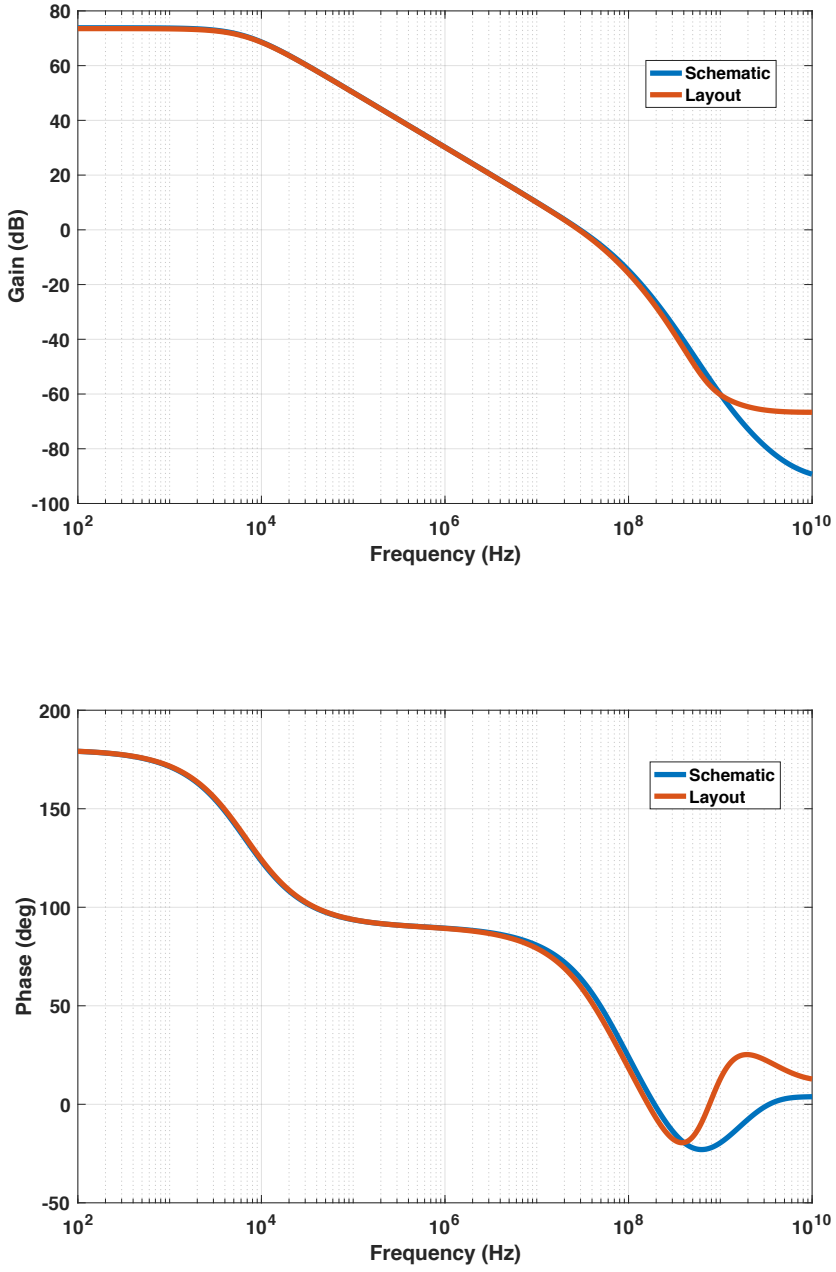


Fig 3.3: Loop gain bode plot of low-voltage OTA

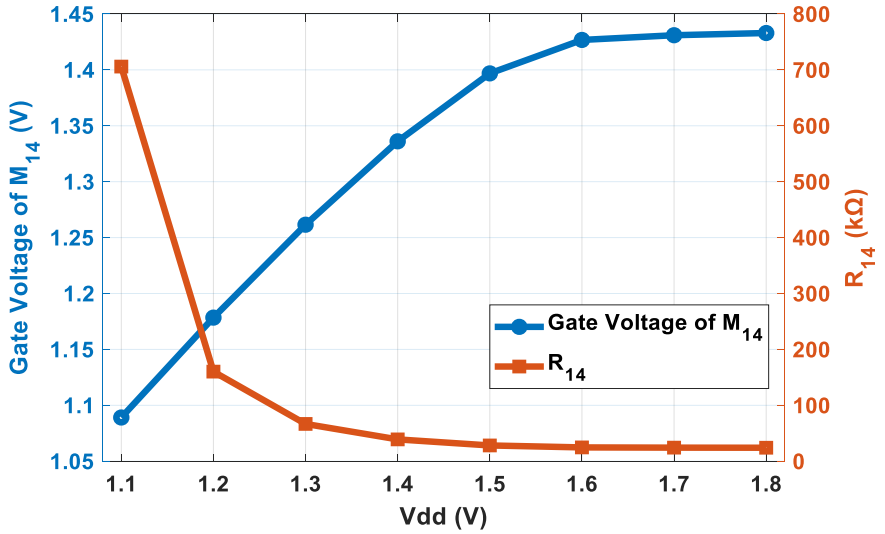


Fig 3.4: Relationship between gate voltage of $M_{14}$ and its equivalent resistance, $R_{14}$, of the conventional OTA with respect to supply voltage. $R_{14}$ = 24.2kΩ at $V_{DD}$ = 1.8V

$$R_{M14} = \frac{1}{\mu_n C_{OX} \left(\frac{W}{L}\right)_{14} \left(V_{GS14} - V_{TH}\right)} \tag{3.16}$$

and the frequency compensation does not work function anymore. The confirmation can be made by Fig. 3.5 and 3.6. Both of plots represent the pole-zero pair in frequency cancellation as a function of frequency for the conventional and low-voltage architectures, respectively. The cancellation of the conventional OTA will be inaccurate at supply voltages less than 1.6V. On the other hand, the low-voltage design can still operate down to 1.1V. In Fig. 3.7, the phase responses of low-voltage and conventional schemes are compared at $V_{DD}$ = 1.4 V. It's clear that inaccurate pole-zero cancellation causes a doublet with settling-time issues [8-9]. For the low-voltage compensated OTA, the phase response simulations across PVT is shown in Fig. 3.8.

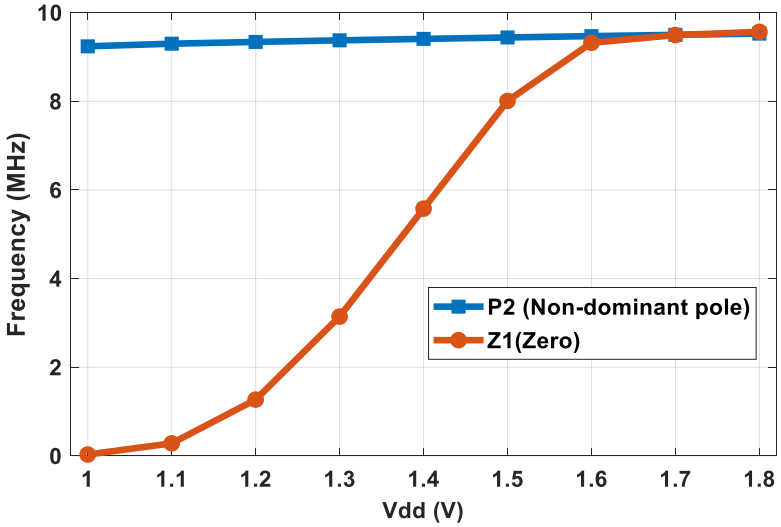


Fig 3.5: Non-dominant pole and zero frequencies of the conventional compensated OTA across different $V_{DD}$

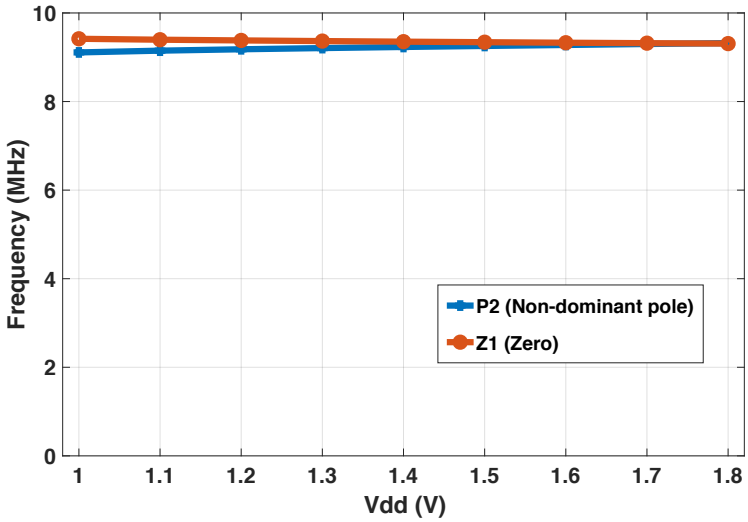


Fig 3.6: Non-dominant pole and zero frequencies of the low-voltage compensated OTA across different $V_{DD}$

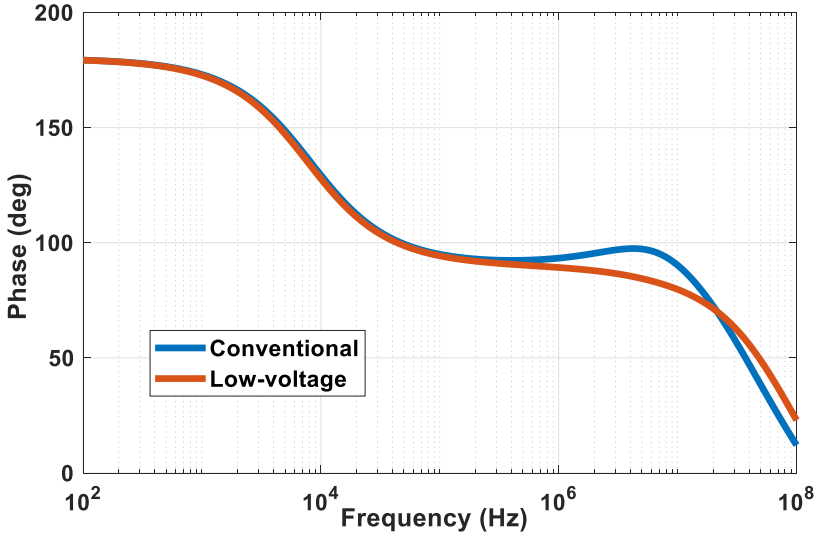


Fig 3.7: Comparison of the phase responses between conventional OTA and low-voltage OTA at $V_{DD}$ = 1.4V

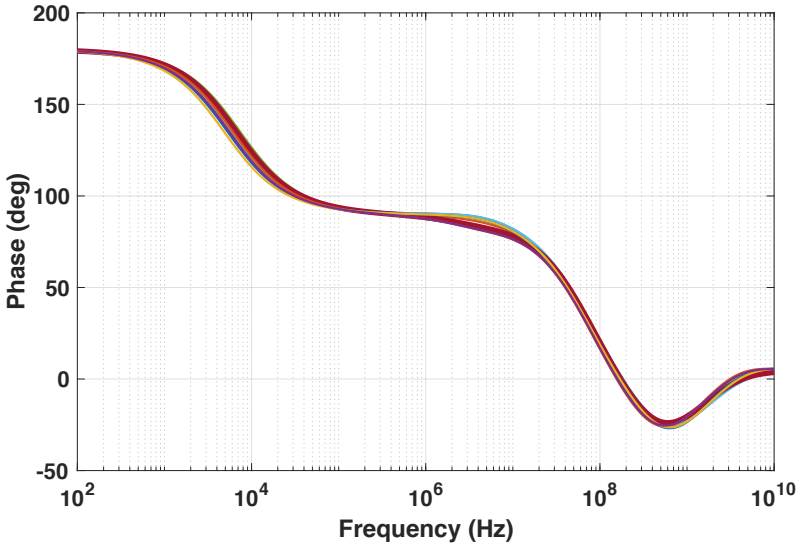


Fig 3.8: Phase responses of low-voltage OTA across PVT variations

There is no doublet seen in the phase plot.

### 3.4.3 Transient Response

One of the most important advantages in the low-voltage tracking compensation scheme is illustrated by the plots of the 1% small-signal settling times across different process corners using a 1.25V power supply. The step response comparisons between different architectures can be clearly shown in Fig. 3.9. Table 3.1 illustrates that the pole-zero frequencies mismatches result in slow setting time issues for some process corners. A low-frequency doublet is evident for the conventional architecture. The conventional scheme, the active RC compensated OTA, fails to be functional since there is not enough headroom in the bias circuit.

## 3.5 Layout

The layouts of the conventional compensated OTA and low-voltage compensated OTA in TSMC 180nm are shown in Fig. 3.10 and Fig. 3.11, respectively. The die sizes of the conventional compensated OTA is 65.8 um x 48.7 um, and the low-voltage compensated OTA is 85.4 um x 47.7 um.

## 3.6 Performance Summary

Both designs are compared in Table 3.2 showing identical specifications. The new topology consumes half power of the conventional one because it operates at low $V_{DD.}$

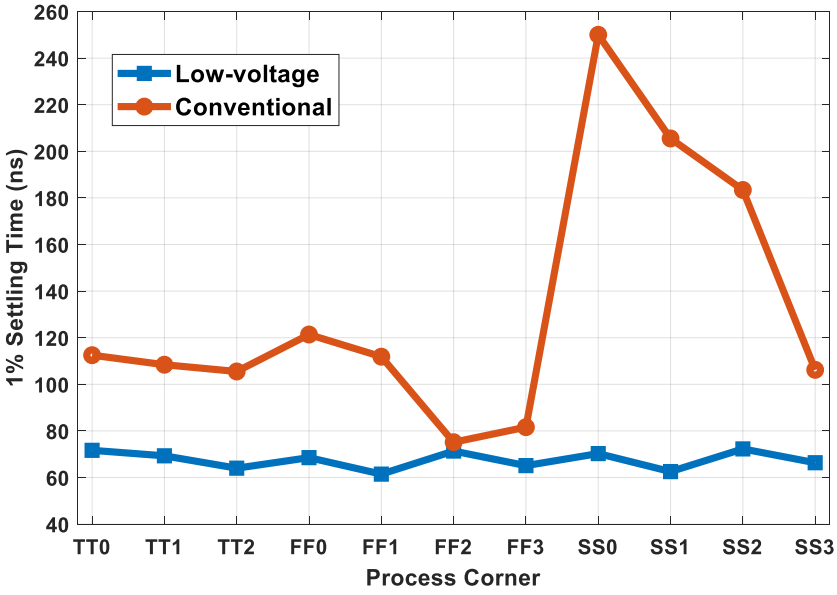


Fig 3.9: 1% settling time comparisons between the conventional and low-voltage compensated OTA

| *Corner* | *Process* | *Voltage* | *Temperature* |
|---|---|---|---|
| TT0 | TT | 1.4V | 0°C |
| TT1 | TT | 1.4V | 25°C |
| TT2 | TT | 1.4V | 80°C |
| FF0 | FF | 1.25V | 0°C |
| FF1 | FF | 1.25V | 80°C |
| FF2 | FF | 1.55V | 0°C |
| FF3 | FF | 1.55V | 80°C |
| SS0 | SS | 1.25V | 0°C |
| SS1 | SS | 1.25V | 80°C |
| SS2 | SS | 1.55V | 0°C |
| SS3 | SS | 1.55V | 80°C |

Table 3.3: Process Corners

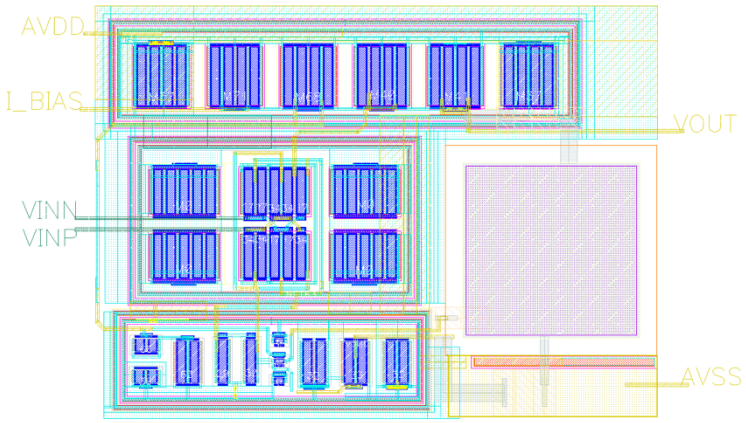


Fig 3.10: Layout of the conventional compensated OTA

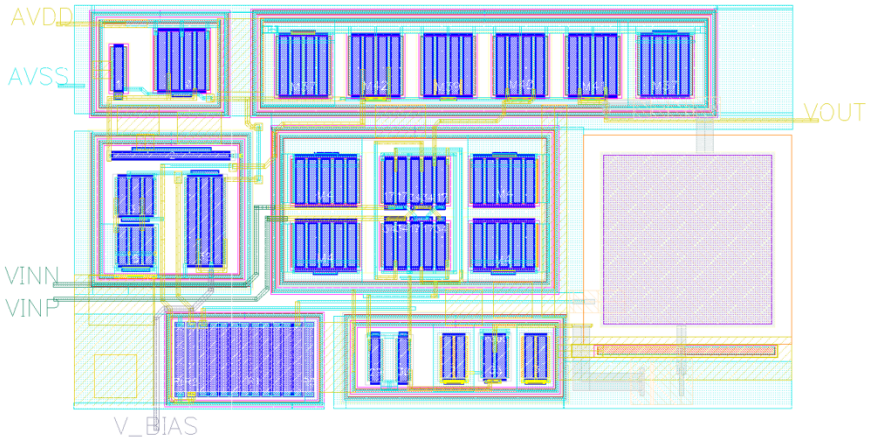


Fig 3.11: Layout of the low-voltage compensated OTA

| Parameter | Low-voltage Compensation | Conventional Compensation |
|---|---|---|
| $V_{DD}$ ($V$) | 1 | 1.8 |
| Gain ($dB$) | 69 | 73 |
| UGB ($MHz$) | 25 | 29.56 |
| Phase Margin (°) | 66 | 64 |
| CL ($pF$) | 5 | 5 |
| Power ($mW$) | 0.089 | 0.18 |

Table 3.4: Performance summary of both approaches

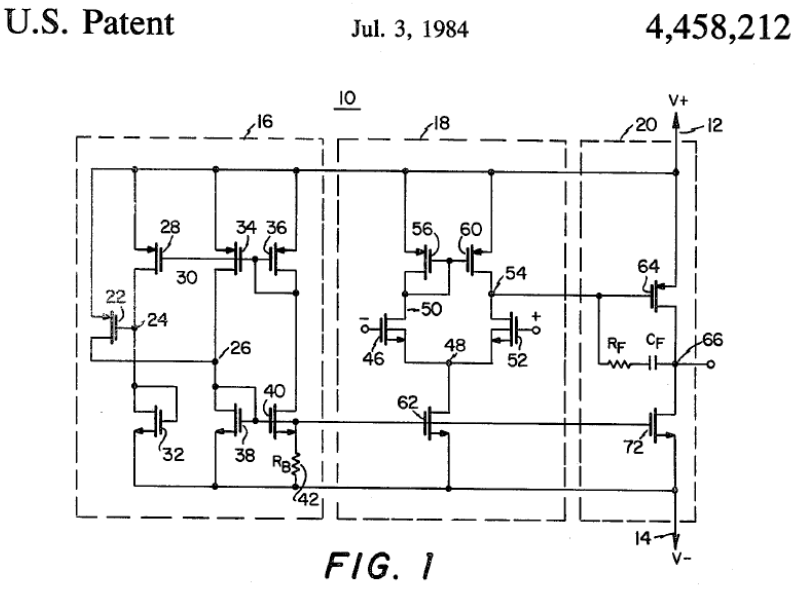


Fig 3.12: The two-stage compensated amplifier with pole-zero tracking [6]

Fig. 3.12 shows the two-stage amplifier with pole-zero tracking frequency compensation [6]. However, the circuit is not implemented correctly. Since the k' of NMOS in the bias circuit will not track the k' of PMOS in the second stage. Our research topic successfully fixes this long-standing mistake.

# Chapter 4: Rail-to-Rail Input and Output Amplifier

## 4.1 Overview

The power supply voltage keeps scaling down with the reduced sizes of CMOS processes. While the trend of power efficiency evolves, VLSI cells gain benefit from this pace. Using the design of minimum length transistors, digital system cells can meet small area and power reduction requirements at the same time. On the other hand, analog design becomes more complex than before since low supply, short-channel, and other side effects limit the circuit performances. Therefore, low-voltage analog design with great performances is essential in recent times. One thing to notice is that the signal swing is shrinking with the reduction of the power supply. It is required that the signals are processed with maximum signal ranges for a certain power supply voltage. An operational amplifier that features rail-to-rail operation is able to obtain a reasonable signal-to-noise ratio (SNR) in low voltage conditions. The signal range is fully covered from the negative supply rail to the positive rail. In other words, a rail-to-rail amplifier makes great usage of the signal range even with smaller supply voltages. Also, the rail-to-rail input stage is usually necessary for buffer designs [13]. In the unity-gain configuration, the input voltage is required to follow the rail-to-rail output voltage. It can be widely seen that the buffer is implemented as a class-AB amplifier, and that is the reason why most class-AB amplifiers process rail-to-rail input.

## 4.2 Literature Review of Rail-to-Rail Amplifiers

A major problem in the rail-to-rail input stage is the transconductances of the input pairs vary across the common-mode voltage range. The transconductance of the input stage has to be constant across the entire common-mode input voltage ranges to ensure a robust frequency compensation. One solution is found in [14] which adds additional current using current switches to control the transconductance of the input stage. In Fig. 4.1 [15], the dashed line represents the rail-to-rail input stage without current switches, and the solid line represents the rail-to-rail input stage with current switches. While only NMOS input pairs operate or only PMOS input pairs operate, the gm is required to be boosted. By the square law equation, the $g_m$ is known to be proportional to the square root of the current. To get a double $g_m$, the tail current of the input pairs should be increased by four times.

The three-times current mirror circuit is realized in Fig. 4.2. The circuit operation principle will be divided into three parts with different input voltage ranges. First, at the lower common-mode input voltage, only PMOS input pairs one operating (red line shown in Fig. 4.2). The N-switch, $M_5$, turns on and takes the current of $I_{ref1}$. With the three times current mirror, the current flows through $M_5$ and $M_6$ to the three times current mirror, $M_7$, is added to the current source $I_{ref2}$. With $I_{ref1} = I_{ref2}$, the tail current of the PMOS input pairs is multiplied by four so the $g_m$ is doubled. Second, with the common-mode input voltage in the middle range, PMOS and NMOS input pairs are both operating. The N-switch $M_5$ and P-switch $M_8$ turn off so there is no current boosted. Finally, at the upper common-mode input voltage, only NMOS input pairs are operating (green line shown in Fig. 4.2). The P-switch, $M_8$, turns on and takes the current of $I_{ref2}$. With the three times current mirror, the current flows through $M_8$ and

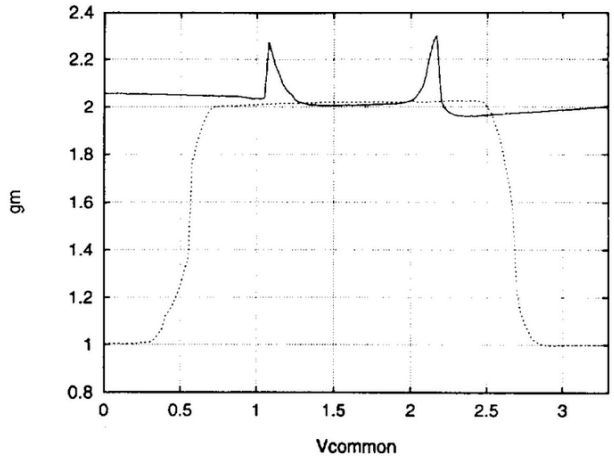


Fig 4.1: Normalized transconductance, $g_m$, across common mode input voltage [15]

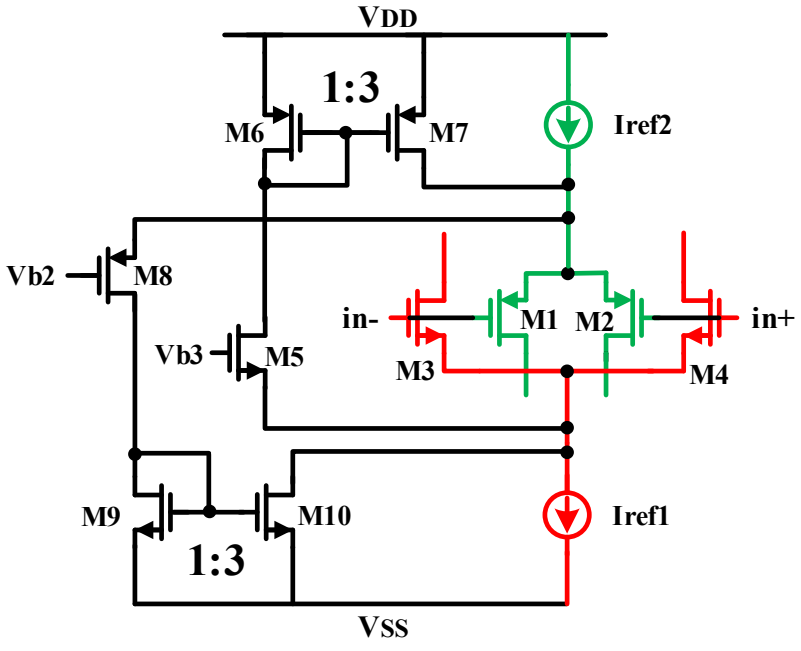


Fig 4.2: $G_m$ control by current switches of rail-to-rail input stage

$M_9$ to the three times current mirror, $M_{10}$, is added to the current source $I_{ref1}$. With $I_{ref1} = I_{ref2}$, the tail current of NMOS input pairs is multiplied by four so the $g_m$ is doubled. The transconductances of the NMOS and PMOS inputs are,

$$gm_n = \sqrt{\mu_n C_{OX} (\frac{W}{L})_n I_{ref}} \tag{4.1}$$

$$gm_p = \sqrt{\mu_p C_{OX} (\frac{W}{L})_p I_{ref}} \tag{4.2}$$

To obtain the constant $g_m$ of the input stage, it is required that

$$\frac{\mu_p}{\mu_n} = \frac{(\frac{W}{L})_n}{(\frac{W}{L})_p} \tag{4.3}$$

The drawback of this technique is shown in (4.3); there is an additional error of $g_m$ with process variations which implies that the technique is not process insensitive.

## 4.3 Design of A Rail-to-Rail Input and Output Amplifier

A Rail-to-rail amplifier is a widely-used category of amplifiers. The signal swing can reach from the positive rail to the negative rail. For example, if the power supply for an amplifier is 3V, the signal does not suffer from distortion issues while the supply is as low as 0V or as high as 3V. Thus, it greatly improves the dynamic range of amplifier, especially in low-voltage applications. There are several papers [16-17] discussing the rail-to-rail output stage. However, those methods are too complicated and area consuming. In this thesis, a compact rail-to-rail input and output amplifier will be discussed [15]. The target specifications of this design are shown in Table 4.1.

| Specification | Value |
|---|---|
| $V_{DD}$ | $3.3V$ |
| Input | $0.3V \sim 3V$ |
| Power | $1mW$ |
| DC Gain | $> 60dB$ |
| Phase Margin | 60° |
| UGB | $> 500KHz$ |
| Settling Time | $10us$ |
| $R_L$, $C_L$ | $30k\Omega$,$30pF$ |

Table 4.1: Specifications of the rail-to-rail amplifier

### 4.3.1 Overall Circuit

Fig. 4.3 shows the overall rail-to-rail input and output circuits. It is a two-stage amplifier using two folded cascodes in parallel. $M_1$-$M_3$ comprise the NMOS input while $M_4$-$M_6$ comprise the PMOS input. Also, $M_7$-$M_{10}$ represents the PMOS cascode current mirror load and $M_{15}$-$M_{18}$ represents the NMOS cascode current mirror load. $M_{11}$ and $M_{13}$ forma floating current source which bias as the class-AB control and cascode summing circuits. $M_{12}$ and $M_{14}$ are floaing class-AB control biases for the output stage $M_{19}$ and $M_{20}$. The bias scheme can be obtained in Fig. 4.4. With different aspect ratios of $M_{b1}$ and $M_{b2}$, the resulting gate-to-source voltage difference between those two transistors transforms to the voltage across the bias resistor. Therefore, the bias current in Eqn. 4.4 can be derived as

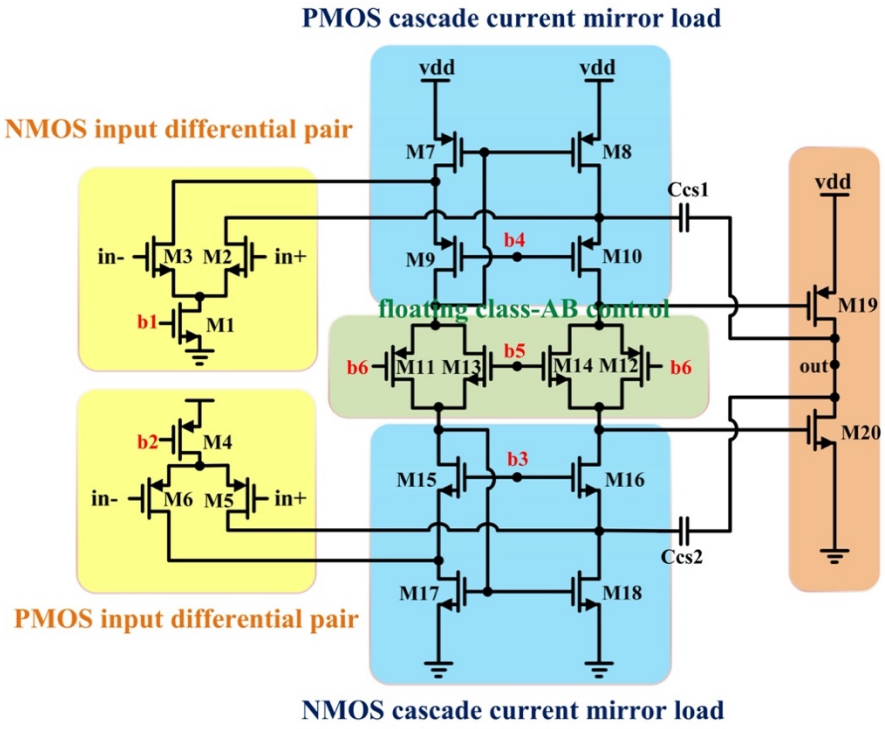


Fig 4.3: Overall circuit of rail-to-rail amplifier

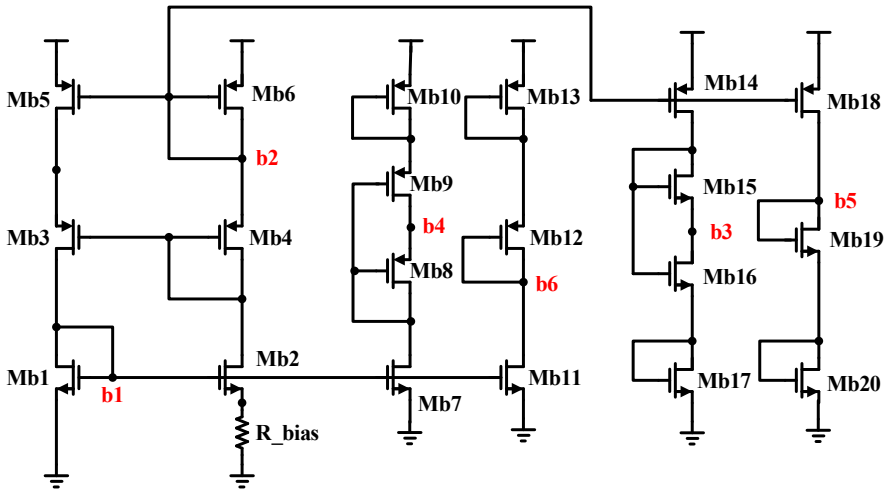


Fig 4.4: Bias circuit of rail-to-rail amplifier

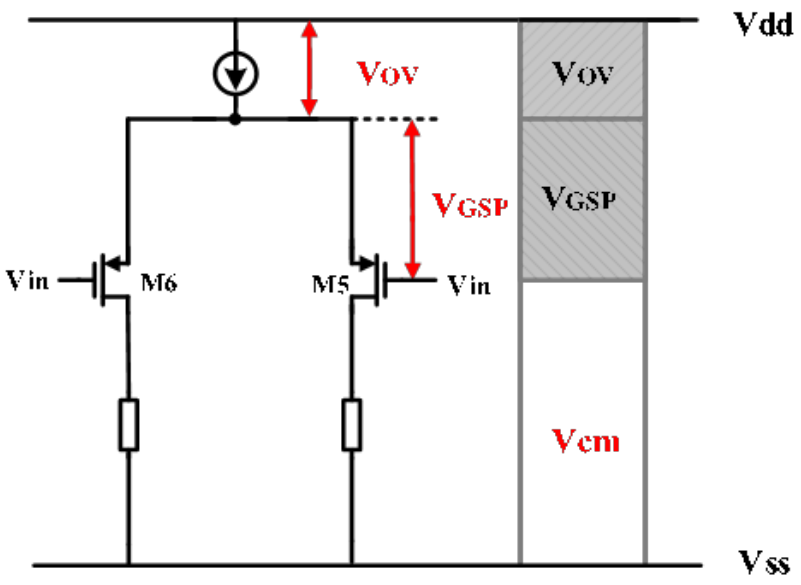


Fig 4.5: Common-mode input voltage range of PMOS input pairs

$$I_B = \frac{2}{K_p (W/L)_1 R_{bias}{}^2} \left( \sqrt{\frac{(W/L)_1}{(W/L)_2}} - 1 \right)^2 \tag{4.4}$$

Again, this bias current only depends on process parameters, bias resistance, and transistor sizes of $M_1$ and $M_2$ which are independent of the supply voltage $V_{DD}$.

## 4.3.2 Rail-to Rail Input Stage

Rail-to-rail operation is a realization of an ideal op-amp which provides the entire voltage range. Using PMOS in input terminals allow the input common-mode voltage to operate near the negative rail (Fig. 4.5). Using NMOS in input terminal

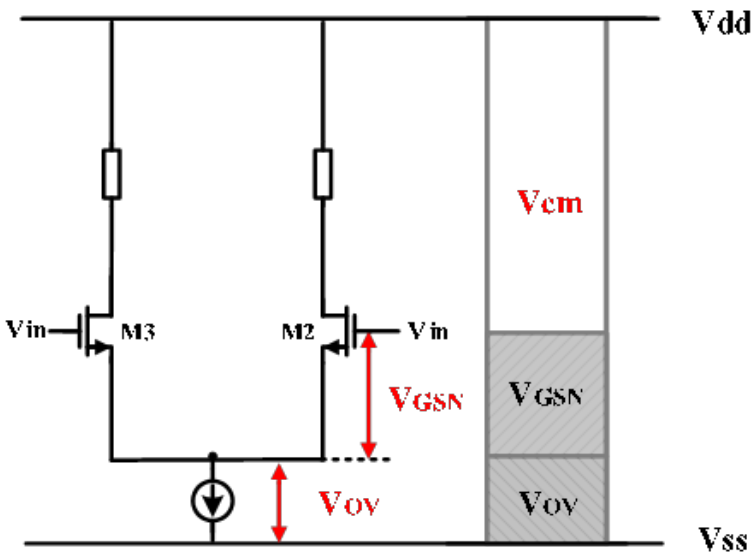


Fig 4.6: Common-mode input voltage range of NMOS input pairs

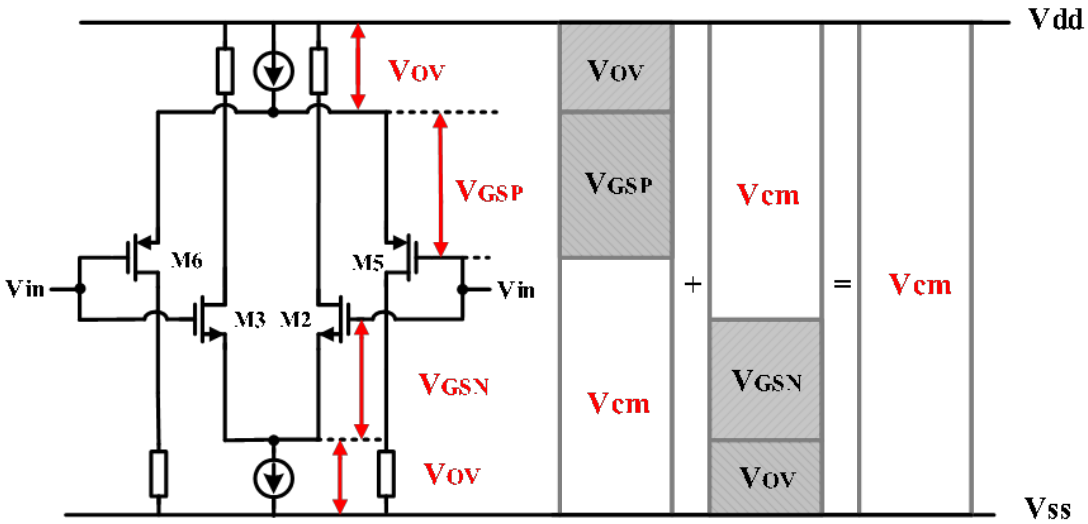


Fig 4.7: Common-mode input voltage range of rail-to-rail input

allows the input common-mode voltage to operate near the positive rail (Fig. 4.6 and Eqn. 4.6).

$$V_{ss} \leq V_{cm} \leq V_{dd} - V_{OV} - \left|V_{GSP}\right| \tag{4.5}$$

$$V_{ss} + V_{OV} + V_{GSN} \leq V_{cm} \leq V_{dd} \tag{4.6}$$

Fig. 4.7 places NMOS and PMOS differential pairs in parallel. Combining the advantages of both NMOS and PMOS configuration, the input common-mode range becomes rail-to-rail. The supply voltage in this scheme should be larger than in (4.7) for functional operation.

$$V_{dd} \geq V_{GSN} + V_{GSP} + 2V_{OV} \tag{4.7}$$

### 4.3.3 Rail-to Rail Output Stage

The floating class-AB control couples the signals to the gate of $M_{19}$ and $M_{20}$ (Fig. 4.8). $M_{b12}$ and $M_{b13}$ provide two diode-connected voltages below the positive supply to bias the gate of $M_{12}$. Also, $M_{b19}$ and $M_{b20}$ provide two diode-connected voltages above the negative supply to bias the gate of $M_{14}$. Besides, the class-AB control is performing as a voltage level shifter. The gate of $M_{19}$ is required for a certain voltage level shift to bias the other output transistor $M_{20}$. This can be realized with a floating class-AB control circuit acting as a voltage level shifter to keep the gate voltage between output transistors $M_{19,}$ $M_{20}$ at a reasonable voltage which determines the quiescent current at the output. An additional advantage of the floating current source is that no extra current is needed to bias floating class-AB control since it is placed into the first stage of amplifier, which makes design less complicated.

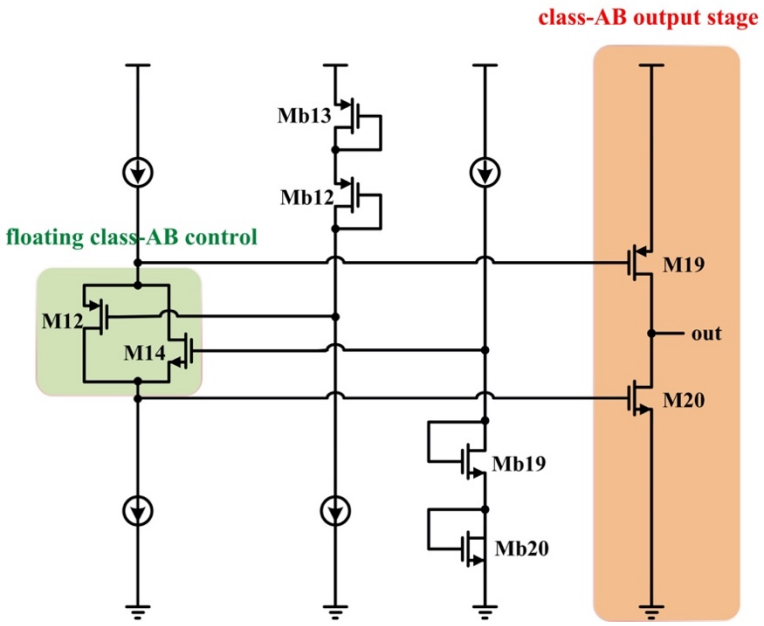


Fig 4.8: Output stage with floating class-AB control

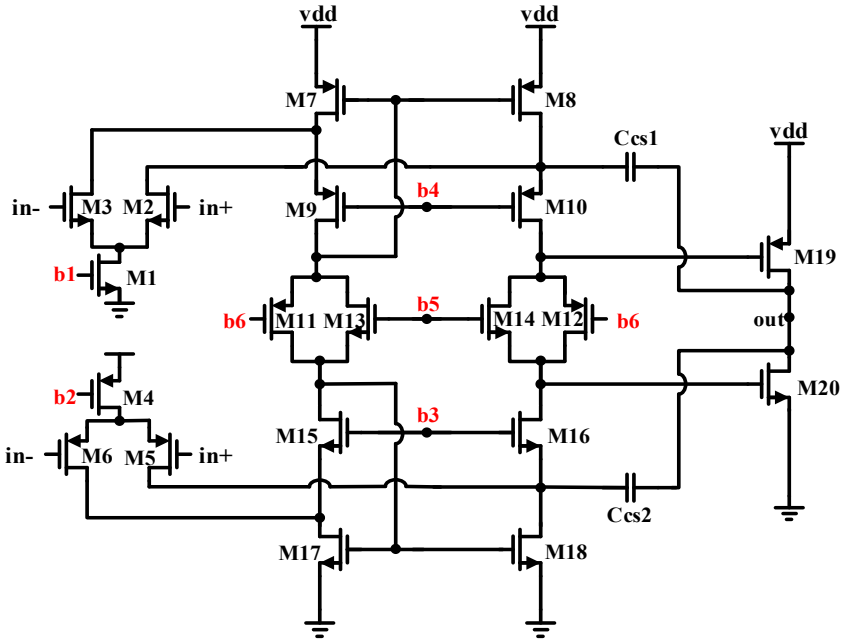


Fig 4.9: Cascode frequency compensation

### 4.3.4 Frequency Response

This rail-to-rail amplifier is designed using cascode Miller compensation [18] shown in Fig. 4.9. It basically included the cascode transistor $M_{10}$ and $M_{16}$ of first stage in the Miller loop [15]. This compensation method puts the pole at the output at a higher frequency than the conventional Miller compensation,

$$\omega_{Out} = \frac{C_M}{C_{GS,OUT}} \frac{g_{mo}}{C_L} \tag{4.7}$$

Where $g_{mo}$ is the transconductance of output stage, and $C_L$ represents the load capacitance. $C_M = C_{CS1} + C_{CS2}$ the total compensation capacitance, and $C_{GS,\,OUT} = C_{GS19} + C_{GS20}$ the total gate-to-source voltage of the output transistors. The output pole of the conventional Miller compensation is equal $g_{mo}/C_L$. It can be seen the output pole frequency with the cascode Miller compensation is $C_M/C_{GS,OUT}$ times greater than with conventional Miller compensation.

## 4.4 Simulation Results

The stability analysis of the rail-to-rail input and output amplifier is shown in Fig. 4.10. The loop gain is 84.5dB, UGB is 1.2MHz, and the phase margin is 69° at a 3.3V supply voltage, 30KΩ load resistor and 30pF load capacitor. Table 4.2 summarizes the performance of this design. All specifications meet within the target values.

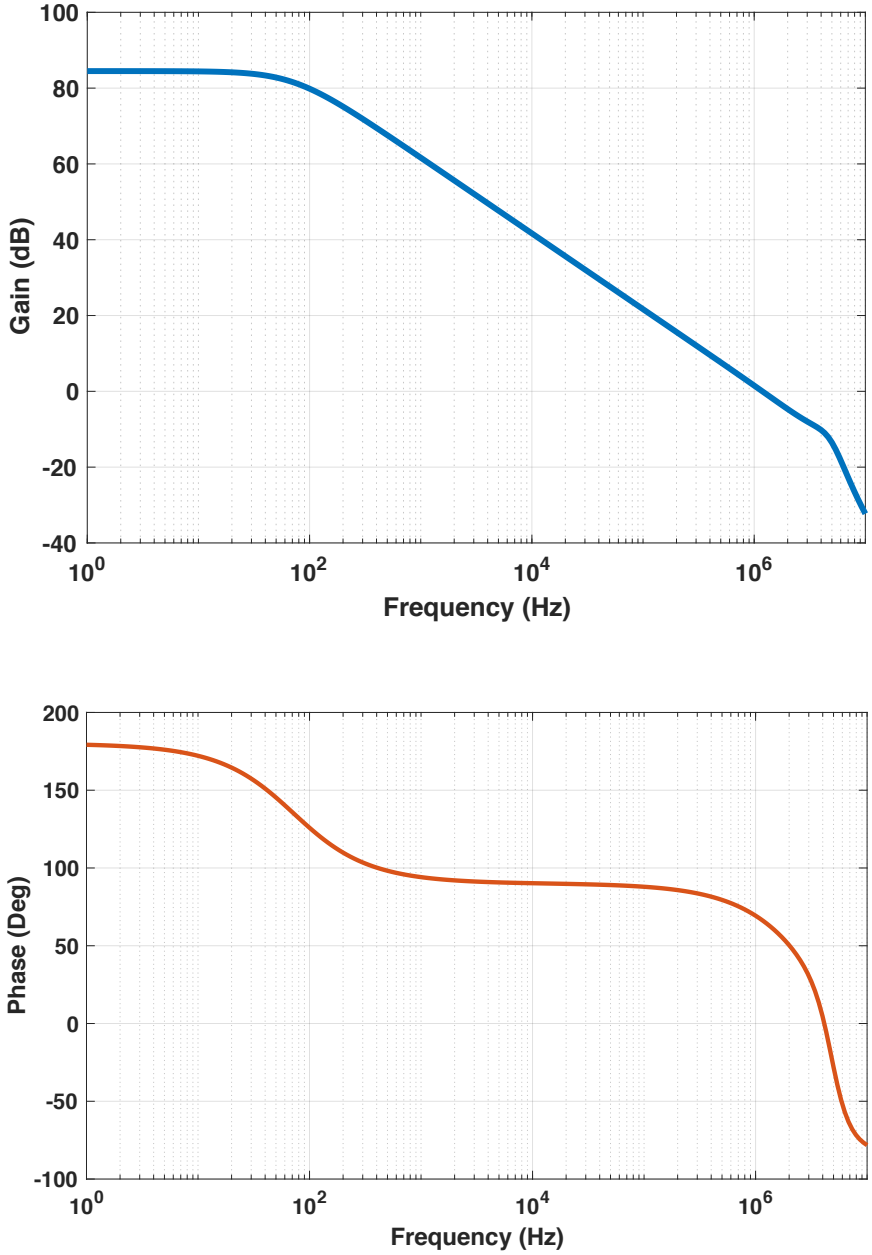


Fig 4.10: Loop gain bode plot of rail-to-rail operational amplifier

| Specification | Value |
|---|---|
| $V_{DD}$ ($V$) | 3.3 |
| Gain ($dB$) | 84.5 |
| UGB ($MHz$) | 1.2 |
| Phase Margin (°) | 66 |
| CL ($pF$) | 30 |
| Power ($mW$) | 0.2 |

Table 4.2: Performance summary of the rail-to-rail amplifier

# Chapter 5: Conclusion

A low-voltage RC-tracking Miller compensation scheme for a two-stage OTA is achieved by making use of a low-voltage k'-generator with no substrate bias effects. A power saving of 2X has been realized and verified in a 180nm TSMC CMOS process compared to the conventional RC Miller compensated OTA for a 5pF load capacitance. The design is shown to be robust across PVT corners even at low supply voltages whereas the conventional architecture ceases to be functional because of the higher headroom requirements in the bias circuitry. Settling times are compared with process variations for both techniques. The low-voltage approach is more robust than the conventional one which suffers from slower settling due to the creation of pole-zero doublets. Therefore, future work on the proposed architecture will focus on deep sub-micron technologies operating from sub-1.0V supply voltages. Moreover, a rail-to-rail input and output amplifier is designed and fabricated using a 180nm process. The input consists of complementary differential pairs, and the output stage is chosen to be class-AB. The future research will focus on the design of a $g_m$ control technique for the input stage.

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