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Title: MOS Switched-Current Biquadratic Filters

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David J. Allstot

A MOS biquadratic (biquad) filter employing the switched-current technique is reported. The circuit uses current-mode processing which can offer wide bandwidth, low voltage operation, and can be implemented with standard CMOS technology. Examples of lowpass, highpass, and bandpass filters are given which illustrate the synthesis procedures and the versatility of the filter topologies.

MOS Switched-Current Biquadratic Filters

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I. INTRODUCTION

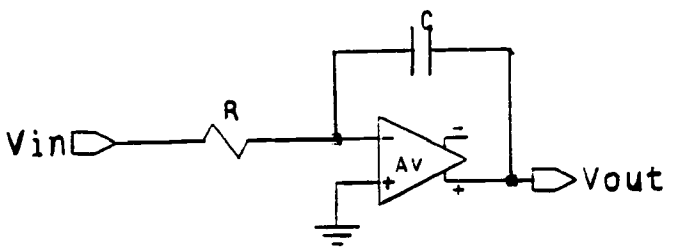
Resistor-capacitor (RC) and switched-capacitor (SC) techniques to implement biquadratic filters have been reported [1]. However, an RC-filter is not very accurate in the frequency response since the absolute value of resistors and capacitors vary independently over process, temperature and voltage variation. In SC filters, the accuracy is improved since ratioed capacitors are used, but additional processing steps are required to realize the precision linear capacitors. Also, its speed is limited to the high gain region of the operational amplifiers. In this paper, a new technique called switched-current (SI) [2] is used to realize biquadratic filters. SI filters can be implemented in a standard CMOS technology. Because of the low impedence nodes of current mirrors, SI filters can operate at a higher frequency than SC filters. Also, everything in the cirucit is manipulated in the current mode, therefore a lower voltage supply is possible. The design technique of SI filters is not well-established, and further development of the design method is discussed here based on what is known from RC and SC circuits. Lowpass, highpass, and bandpass SI biquad filters are designed and integrated in a two micron n-well CMOS technology.

II. GENERAL FILTER TOPOLOGY

A) Active Resistor and Capacitor (RC) Filter Concept

The active RC-filter consists of op amps, resistors and capacitors. The value of integrated resistors and capacitors vary independently over process, temperature and voltage variations. The inaccuracy of the product RC is about ± 35%. In addition to low precision, the resistor of the RC filter requires excessively large die area for low frequency applications.

Fig. 1: Active RC Filter



$$H(s) = \frac{Vout}{Vin}(s) = -\frac{\omega_o}{s} \qquad \text{where } \omega_o = \frac{1}{RC}$$

$$R = \frac{1}{\omega_o C} \qquad \omega_o = 2\pi f_o$$

As f_o decreases, then the value of R increases. Therefore, the area for realizing this R also increases, so it is not appropiate for low frequency operation [3].

B) Active Switched-Capacitor (SC) Filter Concept

The SC filter consists of op amps, capacitors and switching MOSFETs. The main reason for using SC filter is that we can implement the resistance using a sampling capacitor and some switching MOSFET transistors. By doing this it uses less area, but requires added processing steps for the linear capacitors:

Fig. 2: Active SC Filter

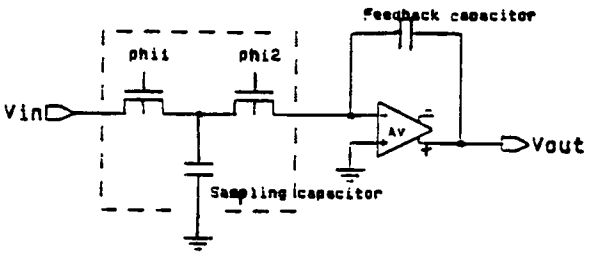
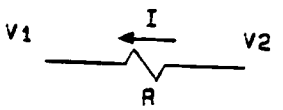


Fig.3 : Figure illustrates the means for the charge transfer over a period of time



$$I = \frac{V_2 - V_1}{R} = \frac{\Delta Q}{\Delta t}$$

$$\Delta Q = I\Delta t = \frac{(V_2 - V_1)}{R}\Delta t$$

Fig. 4: Switching scheme for replacing Resistor with sampling capacitor and MOSFET switches

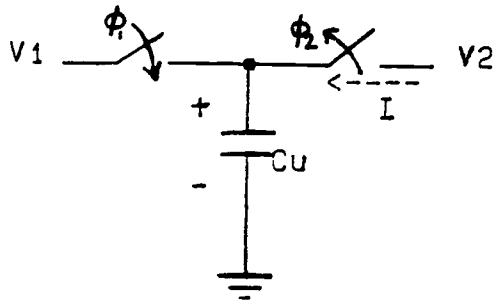
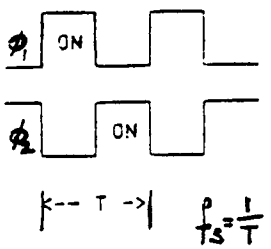


Fig. 5: Non-overlapping clock phases for SC filter



During ϕ_1 : $Q_1 = C_u V_1$

During ϕ_2 : $Q_2 = C_u V_2$

The charge difference on Cu is equal to the difference of voltages multiplied by the value of sampling capacitor Cu

$$I = \frac{\Delta Q}{\Delta t} = \frac{C_u (V_2 - V_1)}{T} = f_s C_u (V_2 - V_1)$$

$$R_{eq} = \frac{T}{C_u} = \frac{1}{f_s C_u}$$

($f_s >> f_{max}$ valid for high sampling rate)
where f_{max} is the maximum input signal frequency.

The charge difference on Cu is equivalent to the difference of voltage multiplied by the sampling capacitance Cu. The switches and capacitor together act as a resistor whose value equals the inverse of the value of the sampling frequency multiplied by the value of the sampling capacitor. The switched capacitor can realize a very large effective resistance in a very small chip area.

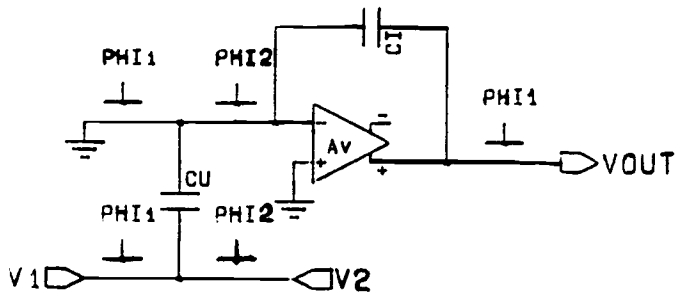
$$H(s) \cong -\frac{\omega_o}{s}$$

$$\omega_o = \frac{1}{RC_I} = \frac{1}{(\frac{1}{f_s C_U})\, C_I} = f_s (\frac{C_U}{C_I})$$

The sampling frequency f_S is derived from a high precision crystal oscillator external to the integrated circuit [2]. The SC filter precision now depends on the capacitor ratio (C_U/C_I) which can be easily controlled on a MOS IC, since SC-filters are monolithic. Individual capacitors may vary about 10% in term of absolute value. If they match together, the ratio of inaccuracy becomes only 0.1%. Moreover, the temperature variation is also cancelled.
Below is an SC integrator:(output sampled on phi1)

$$Vout = \frac{(\frac{CU}{CI})\, z^{-1} V1}{1 - z^{-1}} - \frac{(\frac{CU}{CI})\, z^{-\frac{1}{2}} V2}{1 - z^{-1}} \qquad \text{----------(1)}$$

Fig. 6: SC integrator



C) Switched-Current (SI) Filter Concept

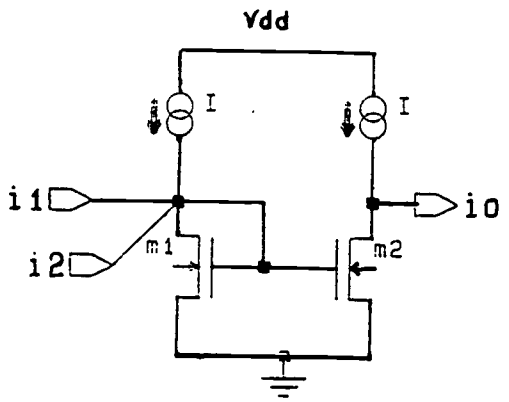
SI-filter can be implemented with standard CMOS technology, because the circuit does not require a precision linear capacitor as in SC-filter in order to perform linearly. Instead of operating in voltage domain, we manipulate everything in currents which allows low voltage operation. This circuit can also operate at high frequencies, due to the low impedence nodes of the current mirror [3]. There is an implicit gain-bandwidth tradeoff in any circuit. SI circuits use current mirrors with approximately unity gain. While in SC circuits high gain amplifiers are required for accuracy and thus, the -3dB bandwidth is very low compared to SI current mirror -3dB bandwidth.

This switched-current technique can be used in analog sampled-data signal processing, because it can perform the basic signal processing operations of summation, scaling, inversion, and delay under clock control. Now, these characteristics are introduced as follows:

i) Summation and Inversion

Assuming we have an ideal circuit, AC signal currents i1 and i2 enter the input node. Apply Kirchhoff's current law at the output, $-I + (I + i1 + i2) + io = 0$, therefore $io = -(i1 + i2)$, assuming m1 and m2 have the same size, and m2 operates in saturation.

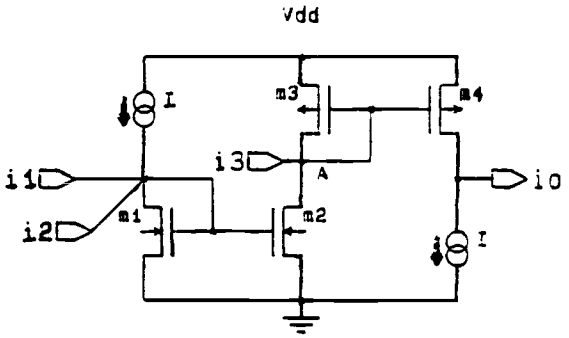
Fig. 7: A switched-current inverting summer amplifier



ii) Non-inversion

A non-inversion cell can be obtained by cascading current mirrors. All transistor sizes are assumed the same. Applying Kirchhoff's current law at A, the drain current of m2 equal to I + i1 + i2 - i3, and then applying Kirchhoff's current law at the output, it is evident that io = i1 + i2 - i3.

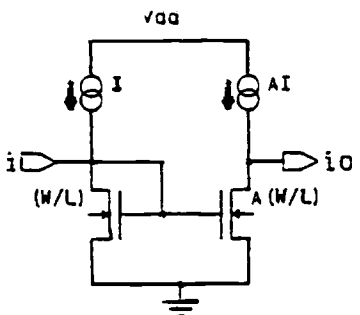
Fig. 8: A switched-current non-inverting summer amplifier



iii) Scaling

The output signal current is scaled by introducing a ratio of W/L for two devices of the current mirror. Additionally, the DC bias current must also be appropriately ratioed. In figure 9, the current mirror ratio and bias current ratios are A. Thus, io = - Ai .

Fig.9: A switched-current inverting amplifier with a scaling factor of A

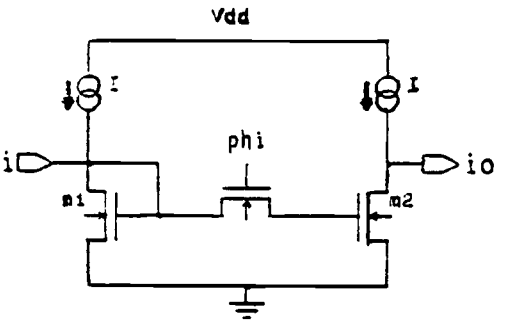


iv) Delays

Delays can be implemented by using a MOSFET switch to sample the voltage, which is then converted to a sampled current.

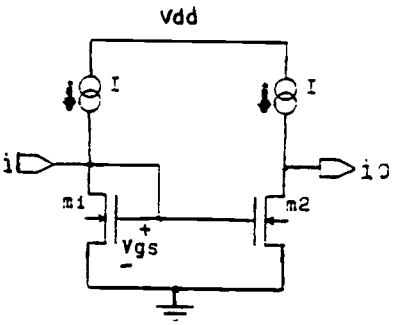
$io = - i z^{-1/2}$

Fig. 10: An inverting switched-current track-and-hold circuit



When phi is high, the NMOS switch is ON , and the circuit becomes

Fig. 11: An equivalent circuit when the switch is turned on



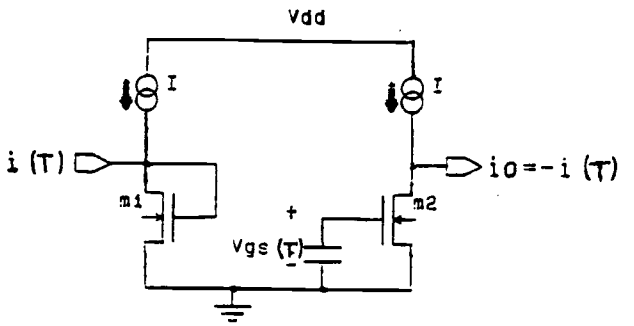
The output signal here is tracking the input signal with inversion, and note that

$$V_{GS}(t) = V_T + \sqrt{\frac{2(I+i)}{k'(\frac{W}{L})}} \qquad \text{----------(2)}$$

is also tracking i.

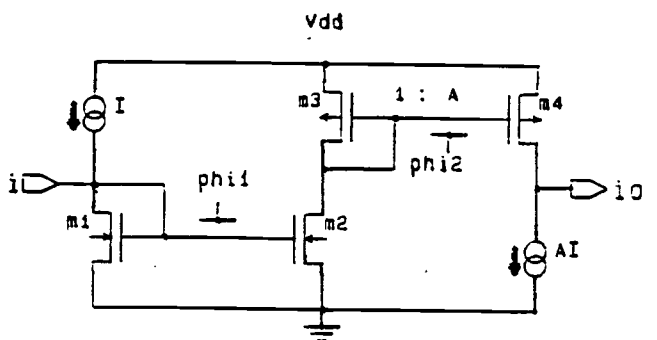
The switch is turned OFF at time t = T when phi is low, then the value of $V_{gs}(T)$ is held on the gate capacitance of m2. The current $i_o = -i(T)$ is maintained at the output. This track-and-hold function in the current domain performs linearly even though C_{gs} is a non-linear capacitor, since this C_{gs} is used only to hold the sampled value of V_{gs}.

Fig. 12: An equivalent circuit when the switch is turned off



A full period of delay is obtained by adding a second clock phase, as shown below:

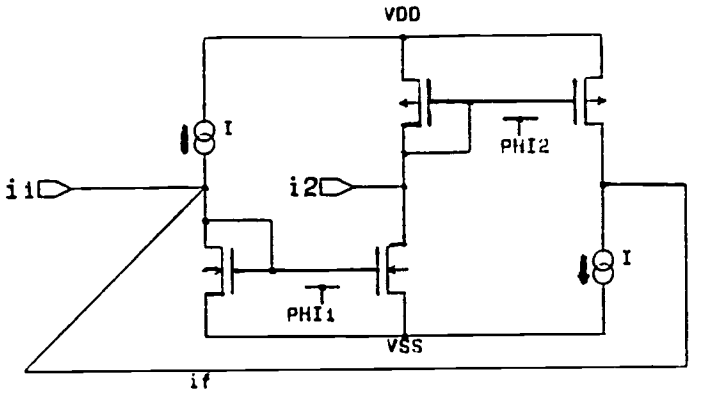
Fig. 13: A circuit showing a full-period of delay



Here the output current is $i_o = Az^{-1} i$, which gives a non-inverted, scaled signal with a full period of delay.

The SI integrator uses the basic signal processing elements described previously. From figure 14, the transfer function for SI integrator can be derived.

Fig. 14: SI integrator for deriving a current transfer function



$$i_f = z^{-1}(i_1 + i_f) - z^{-\frac{1}{2}} i_2 \qquad \text{----------(3a)}$$

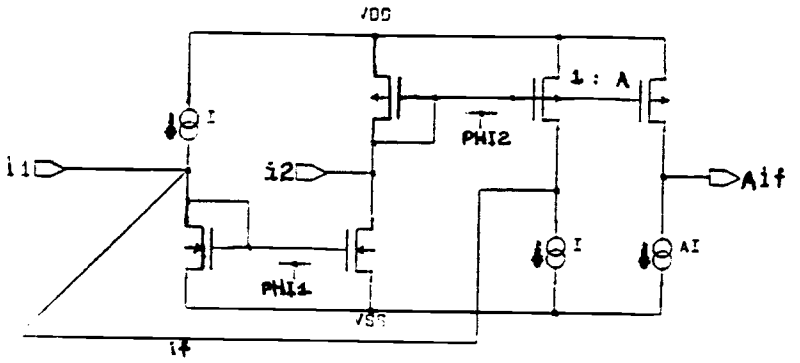
so

$$i_f = \frac{z^{-1} i_1}{1 - z^{-1}} - \frac{z^{-\frac{1}{2}} i_2}{1 - z^{-1}} \qquad \text{----------(3b)}$$

From equation (3b), we see that i1 has a full period of delay and i2 has a half delay. This looks very much like a differential switched-capacitor integrator except for not having a scaling factor in the numerators. We scale using additional current mirrors.

For this circuit,

Fig. 15: SI integrator with a scaling factor



$$i_{out} = Ai_f = \frac{Az^{-1} i_1}{1 - z^{-1}} - \frac{Az^{-\frac{1}{2}} i_2}{1 - z^{-1}} \qquad \text{----------(4)}$$

(assuming that i_f is sampled at phi1)
For the SC integrator shown in figure 6, (output sampled phi1)

$$Vout = \frac{(\frac{Cu}{CI}) z^{-1} V1}{1 - z^{-1}} - \frac{(\frac{Cu}{CI}) z^{-\frac{1}{2}} V2}{1 - z^{-1}} \qquad \text{----------(5)}$$

Therefore, the scaling factor in SI circuits is the same as the capacitance ratio, (C_U/C_I) in SC circuits for a given sampling frequency.

$$A = (\frac{Cu}{CI})$$

This simple relationship makes it very easy to translate existing SC implementations into new SI filters.

III. DESIGN PROCEDURE

The differentional integrator is the primary building block for filter design. First we start from the z-domain transfer function for the SC biquad filter. Then convert all the voltage nodes in the transfer function to current nodes. From this transfer function which is current mode, we can implement the SI biquadratic filter. The following design procedure for obtaining the unscaled value of capacitors is based on the reference [1]. Below is the general biquad voltage transfer function:

$$H(s) = H_o \frac{s^2 + (\frac{\omega_z}{Q_z})s + \omega_z^2}{s^2 + (\frac{\omega_p}{Q_p})s + \omega_p^2} \qquad \text{----------(6)}$$

where H_o is the scale factor, $\omega_p(\omega_z)$ is the pole (zero) frequency, and $Q_p(Q_z)$ is the quality factor for the pole (zero).

In an SC biquad, we need to put things in the discrete-time domain. By using the bilinear transformation, the stability of the filter and shape of the response can be preserved. We obtain the z-domain transfer function as follows, where $s = (2/\tau)(1-z^{-1})/(1+z^{-1})$ and $\tau = 1/f_{sampling}$.

$$H(z) = \frac{V_{out}}{V_{in}}(z) = \frac{N(z)}{D(z)} = \frac{\gamma + \varepsilon z^{-1} + \delta z^{-2}}{1 + \alpha z^{-1} + \beta z^{-2}} \qquad \text{----------(7)}$$

By choosing the appropiate numerator coefficients, the different transfer functions can be realized, such as lowpass (LP), bandpass (BP), highpass (HP). [1]

Referring to Figure 24, the transfer function for each integrator can be derived as follows:

From Vin to Vout':

$$Vout' = \frac{-(\frac{G}{D})}{1-z^{-1}} z^{-\frac{1}{2}} Vin + \frac{(\frac{H}{D})}{1-z^{-1}} z^{-1} Vin - (\frac{E}{D}) Vout - \frac{(\frac{C}{D})}{1-z^{-1}} z^{-\frac{1}{2}} Vout \quad ---(8a)$$

From Vout' to Vout:

$$Vout = \frac{(\frac{J}{B})}{1-z^{-1}} z^{-\frac{1}{2}} Vin - \frac{(\frac{I}{B})}{1-z^{-1}} Vin + \frac{(\frac{A}{B})}{1-z^{-1}} z^{-\frac{1}{2}} Vout' - \frac{(\frac{F}{B})}{1-z^{-1}} Vout \quad ---(8b)$$

When the two transfer functions are combined, the biquadratic transfer function is obtained after some algebraic manipulation.

$$T = \frac{Vout}{Vin} = -\frac{DI + (AG - DI - DJ)z^{-1} + (DJ - AH)z^{-2}}{D(F + B) + (AC + AE - DF - 2DB)z^{-1} + (DB - AE)z^{-2}} \quad ---(9a)$$

and

$$T' = \frac{Vout'}{Vin} = \frac{(IC + IE - GF - GB) + (FH + BH + BG - JC - JE - IE)z^{-1} + (EJ - BH)z^{-2}}{D(F + B) + (AC + AE - DF - 2DB)z^{-1} + (DB - AE)z^{-2}}$$

---(9b)

Before going any further, we set A=B for easier analysis, though we lose the control of the gain constants related with T and T'. However, the degree of freedom can be put back to the circuit through scaling techniques. Capacitors (C, D, E, G, H) and (A, B, F, I, J) can be scaled independently and arbitrarily without interfering with the transfer function, since each stage has an arbitrary impedence scaling. Now, we set

$$A = B = D = 1.$$

Substituting these into (9a) and (9b) yields the following simplified transfer functions:

$$T = -\frac{I + (G - I - J)z^{-1} + (J - H)z^{-2}}{(F + 1) + (C + E - F - 2)z^{-1} + (1 - E)z^{-2}} \qquad \text{----------(10a)}$$

and

$$T' = \frac{(IC + IE - FG - G) + (FH + H + G - JC - JE - IE)z^{-1} + (EJ - H)z^{-2}}{(F + 1) + (C + E - F - 2)z^{-1} + (1 - E)z^{-2}} \qquad \text{---(10b)}$$

We can simplify further by eliminating either E or F from the circuit, because both E and F just provide damping. This means the value of Q in equation (6) is finite. It would be redundant to use both E and F together.
The transfer function for the E-circuit and F-circuit are:

$$T_E = \frac{I + (G - I - J)z^{-1} + (J - H)z^{-2}}{1 + (C + E - 2)z^{-1} + (1 - E)z^{-2}} \qquad \text{----(11a)}$$

$$T'_E = \frac{(IC + IE - G) + (H + G - JC - JE - IE)z^{-1} + (EJ - H)z^{-2}}{1 + (C + E - 2)z^{-1} + (1 - E)z^{-2}} \qquad \text{----(11b)}$$

and

$$T_F = -\frac{\hat{I} + (\hat{G} - \hat{I} - \hat{J})z^{-1} + (\hat{J} - \hat{H})z^{-2}}{(\hat{F} + 1) + (\hat{C} - \hat{F} - 2)z^{-1} + z^{-2}} \qquad \text{----(11c)}$$

$$T'_F = -\frac{(\hat{G}\hat{F} + \hat{G} - \hat{I}\hat{C}) + (\hat{J}\hat{C} - \hat{F}\hat{H} - \hat{H} - \hat{G})z^{-1} + \hat{H}z^{-2}}{(\hat{F} + 1) + (\hat{C} - \hat{F} - 2)z^{-1} + z^{-2}} \qquad \text{----(11d)}$$

The "hats" are put on the F-circuit elements to distinguish from the E-circuit elements.

The unscaled capacitor values are found by combining equation (7) and (11) for the E- or F-circuit, respectively. After getting all the necessary capacitor values, the final step is to scale the capacitors for obtaining the maximum dynamic range at the output of the other operational amplifier.

Now, start with the E-circuit. Comparing (7) & (11a) yields

$$\alpha = E + C - 2 \qquad \text{----------(12)}$$

$$\beta = 1 - E \qquad \text{----------(13)}$$

α and β are related to the location of the poles, and which are determined by ω_p and Q. Therefore the unknown capacitor value for C and E can be obtained from the equation below.

$$E = 1 - \beta \qquad \text{----------(14)}$$

and

$$C = 1 + \beta + \alpha \qquad \text{----------(15)}$$

Similarly, for the F-circuit, the unknown value of F and C are found below.

$$\hat{F} = \frac{1 - \beta}{\beta} \qquad \text{----------(16)}$$

and

$$\hat{C} = \frac{C}{1 - E} \qquad \text{----------(17)}$$

We should take a look at the z-domain transfer functions for those well-known generic forms such as low-pass (LP), high-pass (HP), bandpass (BP), low-pass notch (LPN), high-pass notch (HPN), and all-pass (AP). The numerators, with reference to equation (7), for these generic forms are listed in Table 1.

The numerator of TE (transfer function for the E-circuit) is given below for convenience.

$$N(z) = -I + (G - I - J)z^{-1} + (J - H)z^{-2} \qquad \text{-------(18)}$$

Now, we can see there are enough degrees of freedom to select the three coefficients independently and hence realize arbitrary zero locations. In Table 2, a entire set of design equations is given for the special generic transfer functions of Table 1.

For the F-circuit capacitors $\hat{G}$, $\hat{H}$, $\hat{I}$ and $\hat{J}$ are related to G, H, I and J by $\hat{x} = (1 + \hat{F})x$, where x=G, H, I, J.

Therefore, there is no need to have another table for the synthesis of the zeros of TF. When the value of E, C for TE case and $\hat{F}$, $\hat{C}$ for TF case are known, then we can use Table 3 and Table 4 for the synthesis of the zeros of T'E and T'F, respectively.

Up to this point, all the circuit techniques are for switched-capacitor biquadratic filters. In order to convert to a switched-current biquadratic filter, we have to convert all the voltage nodes in the z-domain transfer function to current nodes. We can do this by using a scaling resistor Rs, and setting its value to 1 ohm for simplicity. Equations (8a) & (8b) become

$$Iout' = \frac{-(\frac{G}{D})}{1-z^{-1}} z^{-\frac{1}{2}} Iin + \frac{(\frac{H}{D})}{1-z^{-1}} z^{-1} Iin - (\frac{E}{D}) Iout - \frac{(\frac{C}{D})}{1-z^{-1}} z^{-\frac{1}{2}} Iout \quad ---(19a)$$

$$Iout = \frac{(\frac{J}{B})}{1-z^{-1}} z^{-\frac{1}{2}} Iin - \frac{(\frac{I}{B})}{1-z^{-1}} Iin + \frac{(\frac{A}{B})}{1-z^{-1}} z^{-\frac{1}{2}} Iout' - \frac{(\frac{F}{B})}{1-z^{-1}} Iout \quad ---(19b)$$

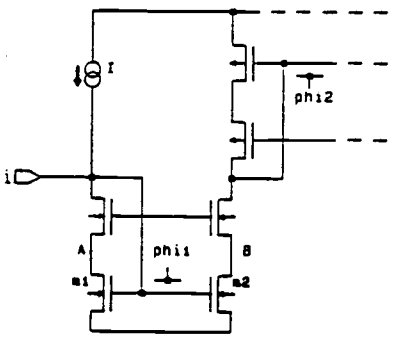
From the above two transfer functions, a switched-current circuit can be realized. Figure 25 is the SI biquadratic filter. In this biquad filter, current mirrors are used to generate the multiplication factors (Equivalent to SC capacitor ratios).

IV. IMPLEMENTATION OF SI BIQUADRATIC FILTER

A) Using high swing cascoded configuration for the current mirrors and the integrators

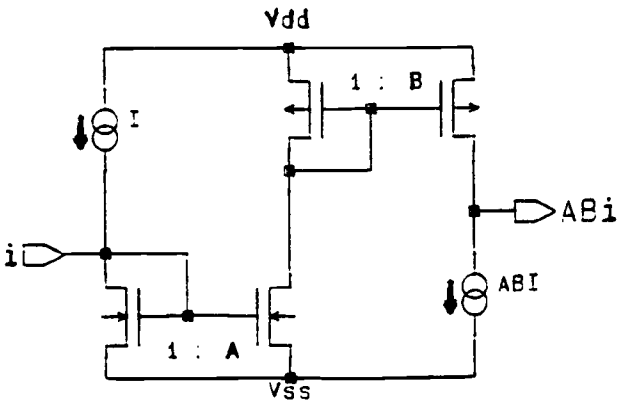
For the current mirrors and the integrators, there are inaccuracies introduced due to the finite output conductance of the MOS transistor. The drain of m2 biased differently from m1 and therefore, the mirroring action when the switch is turned on is non-ideal. This causes current offset and gain errors [4] [5] [6]. The performance can be improved by using a cascoded configuration as shown below.

Fig. 16: High swing cascoded current mirror



If the ratio of the capacitor or the coefficient is very small, we can cascade more current mirrors with different ratios to get the desired coefficient. The resulting coefficient is A*B.

Fig. 17: Cascaded current mirrors for realizing very large or very small current gains.



B) Layout technique for reducing the ratio-matching error due to edge effect from etching

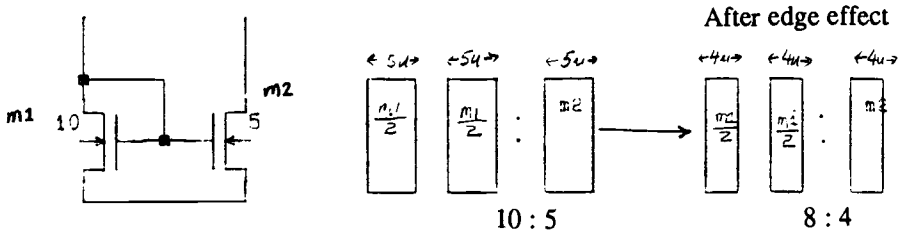
For the layout of the circuit, the edge effects are addressed here. There are three general layout approaches. For example, if the ratio of the current mirror is 2 : 1 as shown in Fig. 20 on page 21, the three general layout techniques are described below.

1) The first approach is trying to break down the transistor m1 into two transistors and each has a size of W equal to 5 μm. Assume that the edge effect gives 1 μm error. After the edge effect, the transistor m1 has two seperate transistors of size 4 μm. However, the ratio for m1 and m2 stays the same as shown in figure 20. This technique is used here to implement the biquadratic filter.

2) The second approach is to have a size of 10 μm for m1 and size 5 μm for m2. As it is noted in figure 21, the ratio is changed after the edge effect.

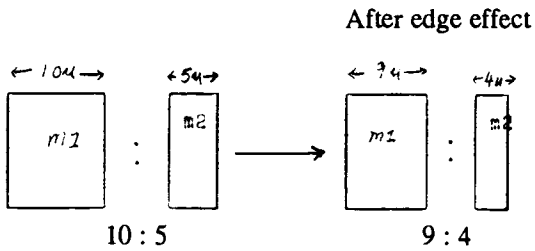
3) The third method is called common centroid technique (averaging technique). By arranging m1 and m2 as shown in figure 22, the edge effect due to gradients in the oxide thickness and processing errors can be eliminated. However, it is difficult to layout a big circuit, and also time consuming.

Fig. 18: Illustration of method 1 for the layout of the circuit



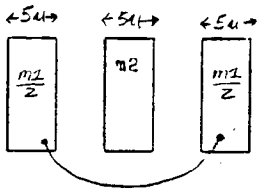
ratio of m1 and m2 is the same
after the edge effect

Fig. 19: Illustration of method 2 for the layout of the circuit



ratio of m1 and m2 is different
after the edge effect

Fig. 20: Common centroid technique for the layout of the circuit



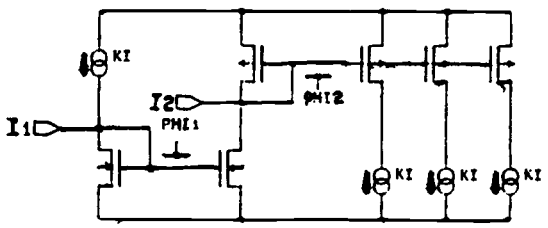
processing error due to long-range gradient in the oxide thickness can be eliminated.

C) Scaling for maximum dynamic range is done by scaling the input current signal

Dynamic range is defined to be 20 log[$I_{in_{rms}}(max)/I_{noise_{rms}}$]. In order to obtain maximum dynamic range, we need to scale so that the peak current of all the output stages are the same. There are two ways to identify how much the output of each op amp needs to be scaled before we implement an SI filter. The first one is to use DINAP [7]. The second one is to use SWITCAP [8] or other SC simulation program to simulate the SC version of the circuit.

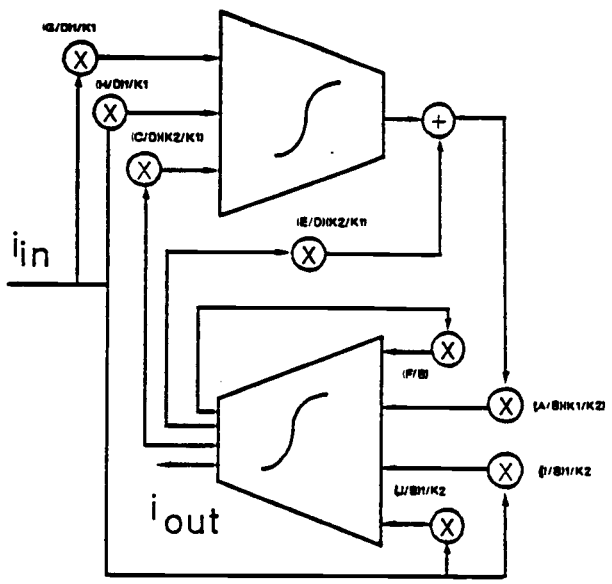
1) In the SC network, where we are concerned with the ratio Vout(peak)/ Vsupply, we use node voltage scaling to adjust all Vout(peak) values to be equal. By analogy, in switched-current filters, we scale the ratio Iout(peak)/ Ibias. It is much easier to simply scale up the bias currents by the amount of peaking at a given stage.

Fig. 21: A circuit that illustrates the scaling of the bias current for obtaining maximum dynamic range



2)We also can scale the input signal, or scale both input signal and bias current.

Fig. 22: A circuit that illustrates the scaling of the input current signal. K1 and K2 are the scaling factors for stage 1 and stage 2, respectively.



V. DESIGN EXAMPLES

In this section, some illustrative design examples will be given. The first example is a lowpass filter whose design is followed through, step by step, to illustrate the design procedure. The second example is a highpass, and the third example is a bandpass.

The transfer function for a lowpass to be realized will be based on the s-domain transfer function shown below:

$$T(s) = \frac{493.48\times10^{6}}{s^{2} + 44.4288\times10^{3}\, s + 986.96\times10^{6}} \quad \text{----(20)}$$

The transfer function provides a cutoff frequency 5kHz, and the sampling frequency is 25kHz, i.e., $\tau = 40\text{x}10^{-6}$ s.

The z-domain transfer function is obtained through the bilinear transformation.

$$T(z) = \frac{0.0869 + 0.17289z^{-1} + 0.0869z^{-2}}{1 - 0.53z^{-1} + 0.2217z^{-2}} \quad \text{---(21)}$$

The peak values for the first and second stages are

$$T'_E \approx -6.97 \text{ dB}, \qquad T_E \approx -5.98 \text{ dB}$$

We decided to scale the peak of both outputs to 0 dB.
Scaling factor for the first stage K1 is 1/2.23 and for the second stage K2 is 1/2.
Capacitors (A, D) are scaled by K1, and capacitors (B, C, E) are scaled by K2.
SWITCAP simulation program and result are shown in the appendix A.

The SC circuit is shown in Figure 26.

Table 5 --- low pass TE realization

Capacitor (pf)	Dynamic Range initial	Adjusted
A	1.000	0.4484
B	1.000	0.5
C	0.692	0.346
D	1.000	0.4484
E	0.778	0.389
F	----	----
G	0.3476	0.3476
H	---	---
I	0.0869	0.0869
J	0.0869	0.0869

Looking at the equation (19a) & (19b), realize that the ratio of the capacitors is neccessary to implement the switched-current circuit; so the ratio is calculated below:

$$\frac{G}{D} = \frac{0.3476}{0.4484} = 0.775 \qquad \frac{I}{B} = \frac{0.0869}{0.5} = 0.173$$

$$\frac{C}{D} = \frac{0.346}{0.4484} = 0.772 \qquad \frac{J}{B} = \frac{0.0869}{0.5} = 0.173$$

$$\frac{E}{D} = \frac{0.389}{0.4484} = 0.867 \qquad \frac{A}{B} = \frac{0.4484}{0.5} = 0.897$$

The biquadratic switched-current circuit consists of current mirrors and integrators. Current mirrors are used to take care of all the multiplication of the capacitors ratio, and then switched-current integrators are used to generate the delay of the clock. The complete SI lowpass TE circuit is shown in figure 27.

The second example is a highpass filter, the transfer function to be realized is based on the s-domain shown below:

$$T(s) = \frac{0.5s^2}{s^2 + 51374.32s + 1319.66\times10^6} \qquad \text{-------(22)}$$

The transfer function provides a cutoff frequency 5kHz, and the sampling frequency is 25kHz, so the z-domain transfer function is obtained through the bilinear transformation;

$$T(z) = \frac{0.1959 + 0.392z^{-1} + 0.1959z^{-2}}{1 - 0.3699z^{-1} + 0.1959z^{-2}} \qquad \text{------(23)}$$

$$T'_E \approx -11.37 \text{ dB}, \qquad T_E \approx -13.37 \text{ dB}$$

For both peaks of the output to be equal to 0 dB, the scaling factor K1 is 1/3.7 and K2 is 1/4.613.

SWITCAP simulation program and result are shown in the appendix A.

The SC circuit is shown in Figure 28.
The required capacitor values are calculated and shown in Table 6.

Table 6--- highpass TE realization

Capacitor (pf)	Dynamic Range initial	Adjusted
A	1.000	0.267
B	1.000	0.217
C	0.826	0.179
D	1.000	0.267
E	0.8041	0.174
F	---	---
G	---	---
H	---	---
I	0.1959	0.1959
J	0.1959	0.1959

the capacitor ratios for the SI transfer functions are figured out below;

$$\frac{C}{D}=\frac{0.179}{0.267}=0.67 \qquad \frac{J}{B}=\frac{0.1959}{0.217}=0.90$$

$$\frac{E}{D}=\frac{0.174}{0.267}=0.65 \qquad \frac{A}{B}=\frac{0.267}{0.217}=1.23$$

$$\frac{I}{B}=\frac{0.1959}{0.217}=0.90$$

and the SI biquadratic circuit for this highpass filter TE circuit is shown in Figure 29.

The last example is a bandpass filter with TE as the desired transfer function;
the s-domain transfer function is as following;

$$T(s) = \frac{3141.59s}{s^2 + 3141.59s + 9.869\times10^8} \qquad \text{----------(24)}$$

after the prewarp, $\hat{\omega}=\frac{2}{\tau}\tan(\frac{\omega\tau}{2})$,

$$\hat{T}(s) = \frac{4803.9s}{s^2 + 4803.9s + 13.236\times10^8} \qquad \text{----------(25)}$$

with Q = 10, f_p = 5k, and f_s = 25k.

and the z-domain transfer function is

$$T(z) = \frac{0.0591 - 0.0591z^{-2}}{1 - 0.5789z^{-1} + 0.88z^{-2}} \qquad \text{---------(26)}$$

$T'_E \approx 12.67$ dB, $T_E \approx 11.14$ dB

For obtaining the maximum dynamic range with 0 dB for both the output peaks, K1 is 4.3 and K2 is 3.606. The final capacitor values are shown in Table 7. SWITCAP simulation program and result are shown in the appendix and the SC circuit is shown in Figure 30.

Table 7 --- bandpass T'E realization

Capacitor (pf)	initial	Dynamic Range Adjusted
A	1.000	4.3
B	1.000	3.606
C	1.3	4.688
D	1.000	4.3
E	0.12	0.432
F	----	----
G	0.758	0.758
H	----	----
I	0.492	0.492
J	0.492	0.492

the capacitor ratios for the SI transfer function is calculated below;

$$\frac{G}{D} = \frac{0.758}{4.3} = 0.18 \qquad \frac{I}{B} = \frac{0.492}{3.606} = 0.14$$

$$\frac{E}{D} = \frac{0.432}{4.3} = 0.10 \qquad \frac{J}{B} = \frac{0.492}{3.606} = 0.14$$

$$\frac{C}{D} = \frac{4.688}{4.3} = 1.09 \qquad \frac{A}{B} = \frac{4.3}{3.606} = 1.19$$

The SI biquad circuit for bandpass T'E transfer function is in Figure 31.

VI. CONCLUSION

The switched-current biquadratic filter is reported, which realizes any of the stable second order z-domain transfer functions. Using the switched-current technique for implementing the biquadratic filter can allow operation in low voltage supply and at high frequency. The circuit is fabricated with a two micron n-well CMOS technology. Figure 23a on page 30 shows a die photo of a low pass SI biquadratic filter and figure 23b shows the frequency response of this low pass filter. Testing of the chip will be done in the near future, and results will be presented [9].

Fig. 23a: Die photo of the low pass SI biquadratic filter

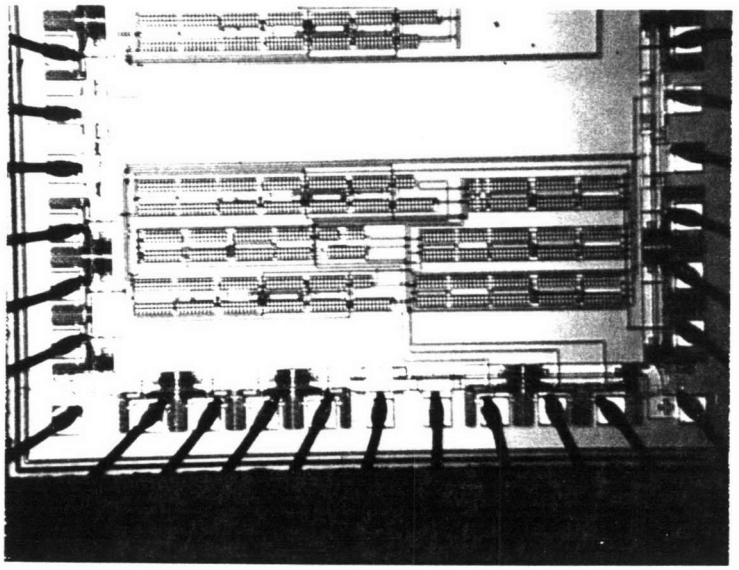


Fig. 23b: Frequency response of a low pass SI biquadratic filter

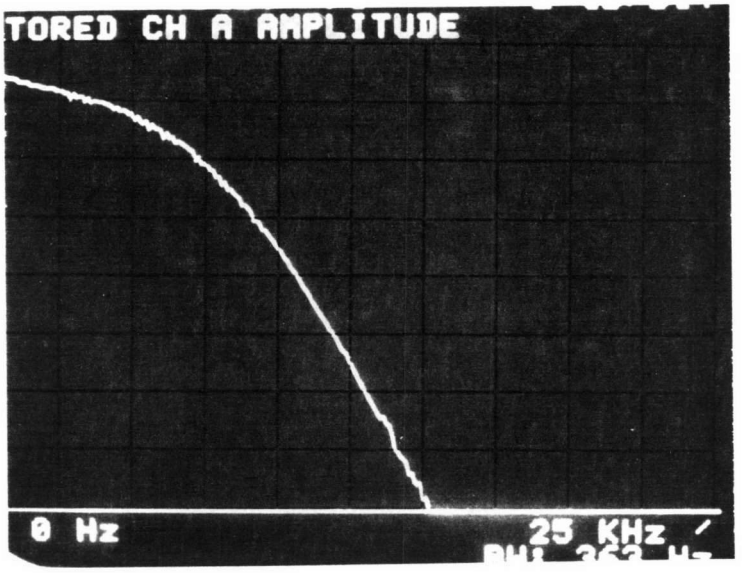


Table 6—Generic biquadratic transfer functions [1]

Generic Form	Numerator $N(z)$
LP 20 (bilinear transform)	$K(1 + z^{-1})^2$
LP 11	$Kz^{-1}(1 + z^{-1})$
LP 10	$K(1 + z^{-1})$
LP 02	Kz^{-2}
LP 01	Kz^{-1}
LP 00	K
BP 10 (bilinear transform)	$K(1 - z^{-1})(1 + z^{-1})$
BP 01	$Kz^{-1}(1 - z^{-1})$
BP 00	$K(1 - z^{-1})$
HP	$K(1 - z^{-1})^2$
LPN	$K(1 + \epsilon z^{-1} + z^{-2})$, $\epsilon > \alpha/\sqrt{\beta}$, $\beta > 0$
HPN	$K(1 + \epsilon z^{-1} + z^{-2})$, $\epsilon < \alpha/\sqrt{\beta}$, $\beta > 0$
AP	$K(\beta + \alpha z^{-1} + z^{-2})$
General	$\gamma + \epsilon z^{-1} + \delta z^{-2}$

Table 2—Zero placement formulas for T_E and T_F [1]

Filter Type	Design Equations	Simple Solution
LP 20	$I = \|K\|$ $G - I - J = 2\|K\|$ $J - H = \|K\|$	$I = J = \|K\|$ $G = 4\|K\|, \quad H = 0$
LP 11	$I = 0$ $G - I - J = \pm\|K\|$ $J - H = \pm\|K\|$	$I = 0, \quad J = \|K\|$ $G = 2\|K\|, \quad H = 0$
LP 10	$I = \|K\|$ $G - I - J = \|K\|$ $J - H = 0$	$I = \|K\|, \quad J = 0$ $G = 2\|K\|, \quad H = 0$
LP 02	$I = 0$ $G - I - J = 0$ $J - H = \pm\|K\|$	$I = J = 0$ $G = 0, \quad H = \|K\|$
LP 01	$I = 0$ $G - I - J = \pm\|K\|$ $J - H = 0$	$I = J = 0$ $G = \|K\|, \quad H = 0$
LP 00	$I = \|K\|$ $G - I - J = 0$ $J - H = 0$	$I = \|K\|, \quad J = 0$ $G = \|K\|, \quad H = 0$
BP 10	$I = \|K\|$ $G - I - J = 0$ $J - H = -\|K\|$	$I = \|K\|, \quad J = 0$ $G = H = \|K\|$
BP 01	$I = 0$ $G - I - J = \pm\|K\|$ $J - H = \mp\|K\|$	$I = 0, \quad J = \|K\|$ $G = H = 0$
BP 00	$I = \|K\|$ $G - I - J = -\|K\|$ $J - H = 0$	$I = \|K\|, \quad J = 0$ $G = H = 0$
HP	$I = \|K\|$ $G - I - J = -2\|K\|$ $J - H = \|K\|$	$I = J = \|K\|$ $G = H = 0$
HPN and LPN	$I = \|K\|$ $G - I - J = \|K\|\epsilon$ $J - H = \|K\|$	$I = J = \|K\|$ $G = \|K\|(2 + \epsilon), \quad H = 0$
AP ($\beta > 0$)	$I = \|K\|\beta$ $G - I - J = \|K\|\alpha$ $J - H = \|K\|$	$I = \|K\|\beta, \quad J = \|K\|$ $G = \|K\|(1 + \beta + \alpha) = \|K\|C$ $H = 0$
General ($\gamma > 0$)	$I = \gamma$ $G - I - J = \epsilon$ $J - H = \delta$	$I = \gamma$ $J = \delta + x$ $G = \gamma + \delta + \epsilon + x$ $H = x \geq 0$

Note: $\hat{G} = G(1 + \hat{F})$, $\hat{H} = H(1 + \hat{F})$, $\hat{I} = I(1 + \hat{F})$, and $\hat{J} = J(1 + \hat{F})$.

10

Table 3—Zero placement formulas for T'_E [1]

Filter Type	Design Equations	Simple Solution
LP 20	$IC + IE - G = \pm\lvert K\rvert$ $H + G - JC - JE - IE = \pm 2\lvert K\rvert$ $EJ - H = \pm\lvert K\rvert$	$I = \frac{\lvert K\rvert(4E + C)}{EC}$, $J = \frac{\lvert K\rvert}{E}$ $G = \frac{\lvert K\rvert(2E + C)^2}{EC}$, $H = 0$
LP 11	$IC + IE - G = 0$ $H + G - JC - JE - IE = \pm\lvert K\rvert$ $EJ - H = \pm\lvert K\rvert$	$I = \frac{\lvert K\rvert(2E + C)}{EC}$, $J = \frac{\lvert K\rvert}{E}$ $G = \frac{\lvert K\rvert(E + C)(2E + C)}{EC}$, $H = 0$
LP 10	$IC + IE - G = \pm\lvert K\rvert$ $H + G - JC - JE - IE = \pm\lvert K\rvert$ $EJ - H = 0$	$I = \frac{2\lvert K\rvert}{C}$, $J = 0$ $G = \frac{\lvert K\rvert(E + C)^2}{EC}$, $H = 0$
LP 02	$IC + IE - G = 0$ $H + G - JC - JE - IE = 0$ $EJ - H = \pm\lvert K\rvert$	$I = \frac{\lvert K\rvert(E + C)}{EC}$, $J = \frac{\lvert K\rvert}{E}$ $G = \frac{\lvert K\rvert(E + C)^2}{EC}$, $H = 0$
LP 01	$IC + IE - G = 0$ $H + G - JC - JE - IE = \pm\lvert K\rvert$ $EJ - H = 0$	$I = \frac{\lvert K\rvert}{C}$, $J = 0$ $G = \frac{\lvert K\rvert(E + C)}{C}$, $H = 0$
LP 00	$IC + IE - G = \pm\lvert K\rvert$ $H + G - JC - JE - IE = 0$ $EJ - H = 0$	$I = \frac{\lvert K\rvert}{C}$, $J = 0$ $G = \frac{\lvert K\rvert E}{C}$, $H = 0$
BP 10	$IC + IE - G = \pm\lvert K\rvert$ $H + G - JC - JE - IE = 0$ $EJ - H = \mp\lvert K\rvert$	$I = J = \frac{\lvert K\rvert}{E}$ $G = \frac{\lvert K\rvert(2E + C)}{E}$, $H = 0$
BP 01	$IC + IE - G = 0$ $H + G - JC - JE - IE = \pm\lvert K\rvert$ $EJ - H = \mp\lvert K\rvert$	$I = J = 0$ $G = 0$, $H = \lvert K\rvert$
BP 00	$IC + IE - G = \pm\lvert K\rvert$ $H + G - JC - JE - IE = \mp\lvert K\rvert$ $EJ - H = 0$	$I = 0$, $J = 0$ $G = \lvert K\rvert$, $H = 0$
HP	$IC + IE - G = \pm\lvert K\rvert$ $H + G - JC - JE - IE = \mp 2\lvert K\rvert$ $EJ - H = \pm\lvert K\rvert$	$I = J = 0$ $G = H = \lvert K\rvert$
HPN and LPN	$IC + IE - G = \pm\lvert K\rvert$ $H + G - JC - JE - IE = \pm\lvert K\rvert\epsilon$ $EJ - H = \pm\lvert K\rvert$	See general solution below
AP	$IC + IE - G = \pm\lvert K\rvert\beta$ $H + G - JC - JE - IE = \pm\lvert K\rvert\alpha$ $EJ - H = \pm\lvert K\rvert$	See general solution below
General $\delta > 0$	$IC + IE - G = \gamma$ $H + G - JC - JE - IE = \epsilon$ $EJ - H = \delta$	$I = \frac{\gamma + \delta + \epsilon}{C} + \frac{\delta}{E}$, $J = \frac{\delta}{E}$ $G = I(C + E) - \gamma$ $H = 0$

Table 4 —Zero placement formulas for T'_F [1]

Filter Type	Design Equations	Simple Solution
LP 20	$\dot{G}\dot{F} + \dot{G} - \dot{I}\dot{C} = \lvert K\rvert(1+\dot{F})$ $\dot{J}\dot{C} - \dot{F}\dot{H} - \dot{H} - \dot{G} = 2\lvert K\rvert(1+\dot{F})$ $\dot{H} = \lvert K\rvert(1+\dot{F})$	$\dot{I} = 0, \quad \dot{J} = \dfrac{\lvert K\rvert(2+\dot{F})^2}{\dot{C}}$ $\dot{G} = \lvert K\rvert, \quad \dot{H} = \lvert K\rvert(1+\dot{F})$
LP 11	$\dot{G}\dot{F} + \dot{G} - \dot{I}\dot{C} = 0$ $\dot{J}\dot{C} - \dot{F}\dot{H} - \dot{H} - \dot{G} = \lvert K\rvert(1+\dot{F})$ $\dot{H} = \lvert K\rvert(1+\dot{F})$	$\dot{I} = 0, \quad \dot{J} = \dfrac{\lvert K\rvert(1+\dot{F})(2+\dot{F})}{\dot{C}}$ $\dot{G} = 0, \quad \dot{H} = \lvert K\rvert(1+\dot{F})$
LP 10	$\dot{G}\dot{F} + \dot{G} - \dot{I}\dot{C} = \pm\lvert K\rvert(1+\dot{F})$ $\dot{J}\dot{C} - \dot{F}\dot{H} - \dot{H} - \dot{G} = \pm\lvert K\rvert(1+\dot{F})$ $\dot{H} = 0$	$\dot{I} = 0, \quad \dot{J} = \dfrac{\lvert K\rvert(2+\dot{F})}{\dot{C}}$ $\dot{G} = \lvert K\rvert, \quad \dot{H} = 0$
LP 02	$\dot{G}\dot{F} + \dot{G} - \dot{I}\dot{C} = 0$ $\dot{J}\dot{C} - \dot{F}\dot{H} - \dot{H} - \dot{G} = 0$ $\dot{H} = \lvert K\rvert(1+\dot{F})$	$\dot{I} = 0, \quad \dot{J} = \dfrac{\lvert K\rvert(1+\dot{F})^2}{\dot{C}}$ $\dot{G} = 0, \quad \dot{H} = \lvert K\rvert(1+\dot{F})$
LP 01	$\dot{G}\dot{F} + \dot{G} - \dot{I}\dot{C} = 0$ $\dot{J}\dot{C} - \dot{F}\dot{H} - \dot{H} - \dot{G} = \pm K(1+\dot{F})$ $\dot{H} = 0$	$\dot{I} = 0, \quad \dot{J} = \dfrac{\lvert K\rvert(1+\dot{F})}{\dot{C}}$ $\dot{G} = 0, \quad \dot{H} = 0$
LP 00	$\dot{G}\dot{F} + \dot{G} - \dot{I}\dot{C} = \pm\lvert K\rvert(1+\dot{F})$ $\dot{J}\dot{C} - \dot{F}\dot{H} - \dot{H} - \dot{G} = 0$ $\dot{H} = 0$	$\dot{I} = \dfrac{\lvert K\rvert(1+\dot{F})}{\dot{C}}, \quad \dot{J} = 0$ $\dot{G} = 0, \quad \dot{H} = 0$
BP 10	$\dot{G}\dot{F} + \dot{G} - \dot{I}\dot{C} = -\lvert K\rvert(1+\dot{F})$ $\dot{J}\dot{C} - \dot{F}\dot{H} - \dot{H} - \dot{G} = 0$ $\dot{H} = \lvert K\rvert(1+\dot{F})$	$\dot{I} = \dfrac{\lvert K\rvert(1+\dot{F})}{\dot{C}}, \quad \dot{J} = \dfrac{\lvert K\rvert(1+\dot{F})^2}{\dot{C}}$ $\dot{G} = 0, \quad \dot{H} = \lvert K\rvert(1+\dot{F})$
BP 01	$\dot{G}\dot{F} + \dot{G} - \dot{I}\dot{C} = 0$ $\dot{J}\dot{C} - \dot{F}\dot{H} - \dot{H} - \dot{G} = -\lvert K\rvert(1+\dot{F})$ $\dot{H} = \lvert K\rvert(1+\dot{F})$	$\dot{I} = 0, \quad \dot{J} = \dfrac{\lvert K\rvert\dot{F}(1+\dot{F})}{\dot{C}}$ $\dot{G} = 0, \quad \dot{H} = \lvert K\rvert(1+\dot{F})$
BP 00	$\dot{G}\dot{F} + \dot{G} - \dot{I}\dot{C} = \pm\lvert K\rvert(1+\dot{F})$ $\dot{J}\dot{C} - \dot{F}\dot{H} - \dot{H} - \dot{G} = \mp\lvert K\rvert(1+\dot{F})$ $\dot{H} = 0$	$\dot{I} = \dot{J} = \dfrac{\lvert K\rvert(1+\dot{F})}{\dot{C}}$ $\dot{G} = \dot{H} = 0$
HP	$\dot{G}\dot{F} + \dot{G} - \dot{I}\dot{C} = \lvert K\rvert(1+\dot{F})$ $\dot{J}\dot{C} - \dot{F}\dot{H} - \dot{H} - \dot{G} = -2\lvert K\rvert(1+\dot{F})$ $\dot{H} = \lvert K\rvert(1+\dot{F})$	$\dot{I} = 0, \quad \dot{J} = \dfrac{\lvert K\rvert\dot{F}^2}{\dot{C}}$ $\dot{G} = \lvert K\rvert, \quad \dot{H} = \lvert K\rvert(1+\dot{F})$
HPN and LPN	$\dot{G}\dot{F} + \dot{G} - \dot{I}\dot{C} = \lvert K\rvert(1+\dot{F})$ $\dot{J}\dot{C} - \dot{F}\dot{H} - \dot{H} - \dot{G} = -\lvert K\rvert\epsilon(1+\dot{F})$ $\dot{H} = \lvert K\rvert(1+\dot{F})$	See general solution below
AP	$\dot{G}\dot{F} + \dot{G} - \dot{I}\dot{C} = \lvert K\rvert\beta(1+\dot{F})$ $\dot{J}\dot{C} - \dot{F}\dot{H} - \dot{H} - \dot{G} = \lvert K\rvert\alpha(1+\dot{F})$ $\dot{H} = \lvert K\rvert(1+\dot{F})$	See general solution below
General	$\dot{G}\dot{F} + \dot{G} - \dot{I}\dot{C} = \gamma(1+\dot{F})$	$I = x \geq 0$
$\delta > 0$	$\dot{J}\dot{C} - \dot{F}\dot{H} - \dot{H} - \dot{G} = \epsilon(1+\dot{F})$	$\dot{J} = \dfrac{\delta(1+\dot{F})^2 + \epsilon(1+\dot{F}) + \gamma}{\dot{C}} + \dfrac{x}{1+\dot{F}}$
	$\dot{H} = \delta(1+\dot{F})$	$\dot{G} = \gamma + \dfrac{C}{1+\dot{F}}x$ $\dot{H} = \delta(1+\dot{F})$

Fig. 24 SC-biquadratic filter

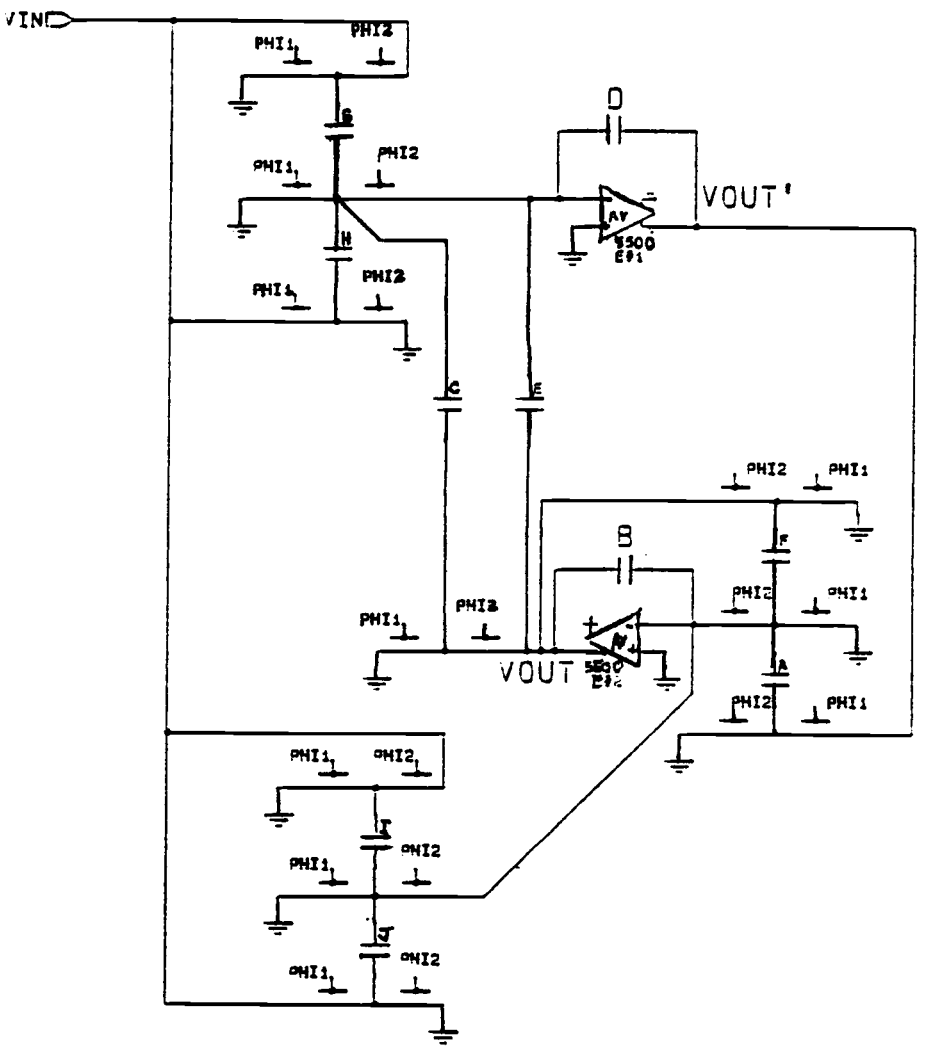


Fig.25 : SI-biquadratic filter

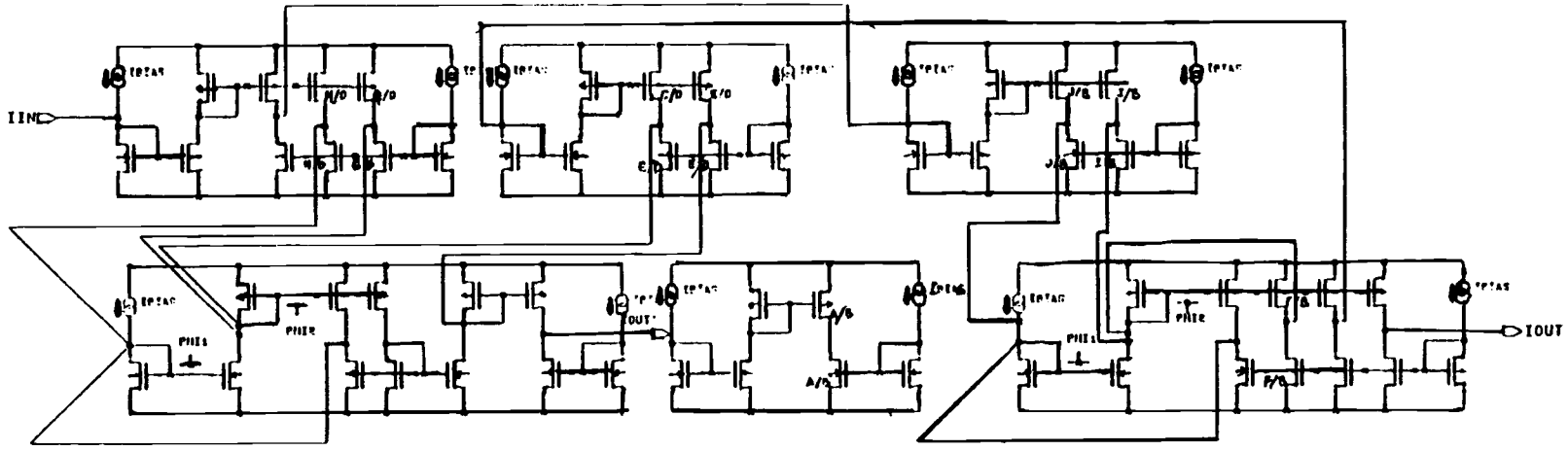


Fig.26 SC lowpass(20): E-circuit with the desired output at the 2nd stage

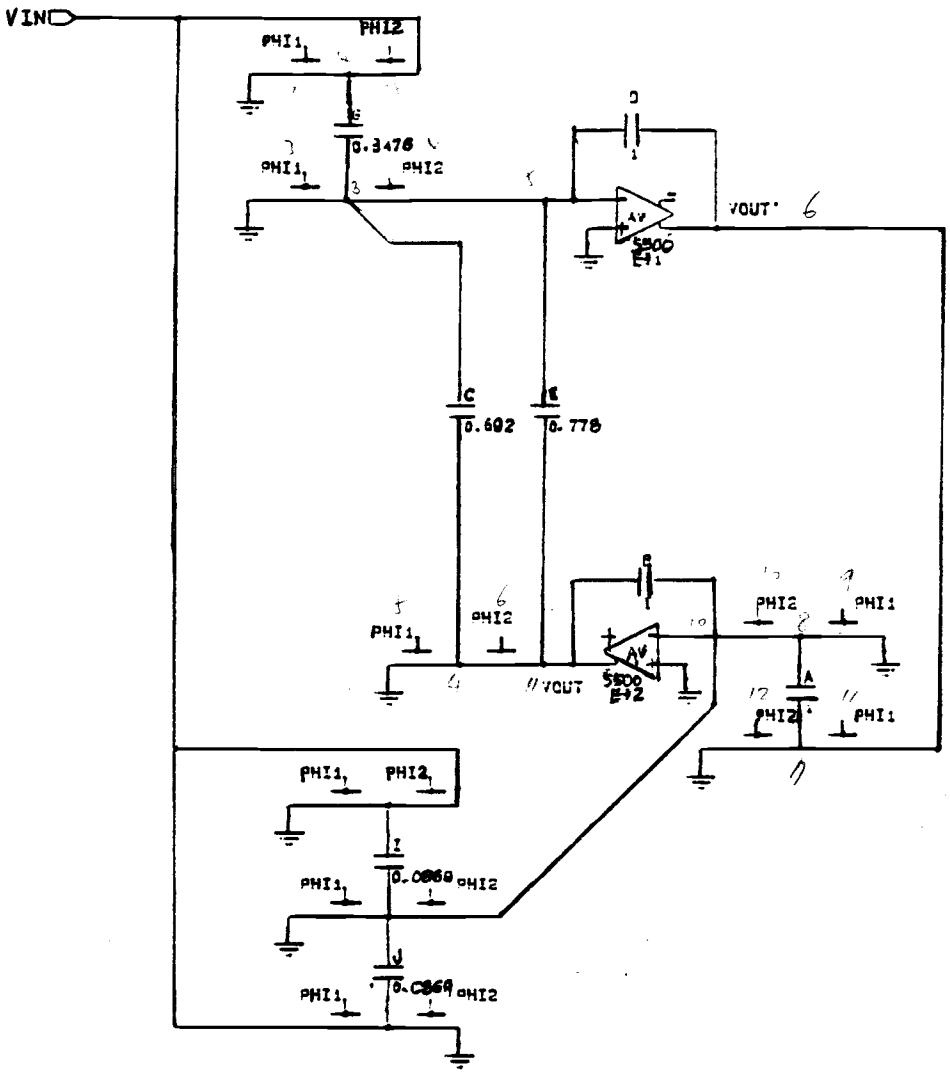


Fig. 27: SI lowpass(20): E-circuit with the desired output at the 2nd stage

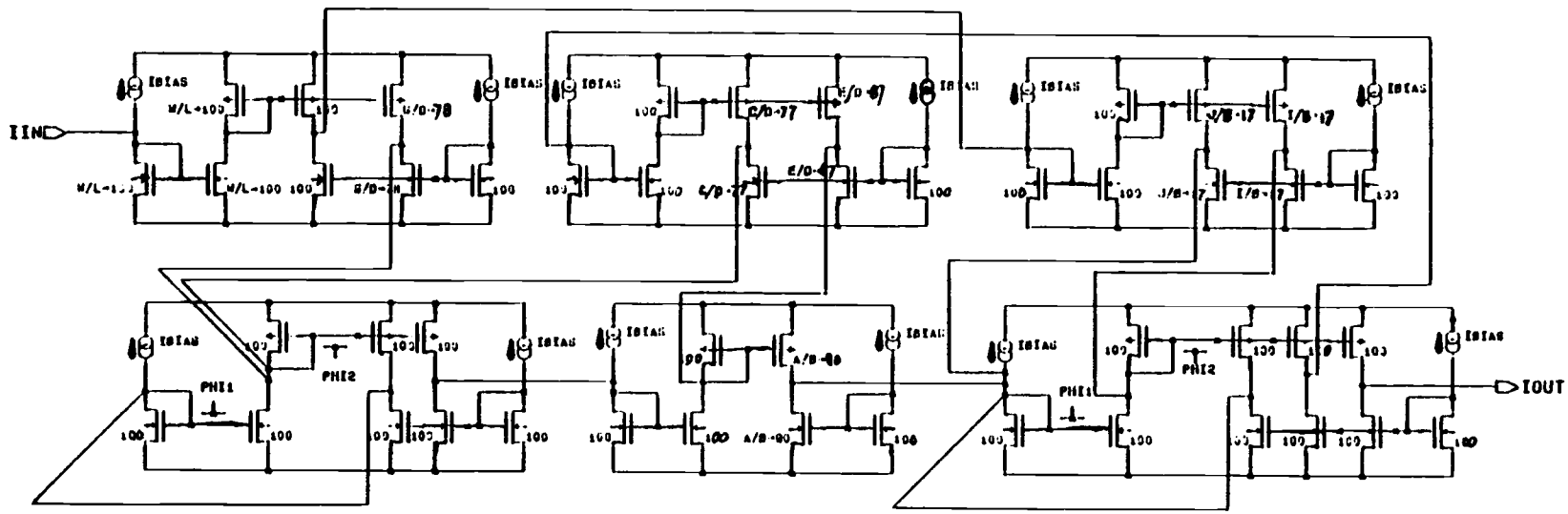


Fig. 28 : SC highpass: E-circuit with the desired output at the 2nd stage

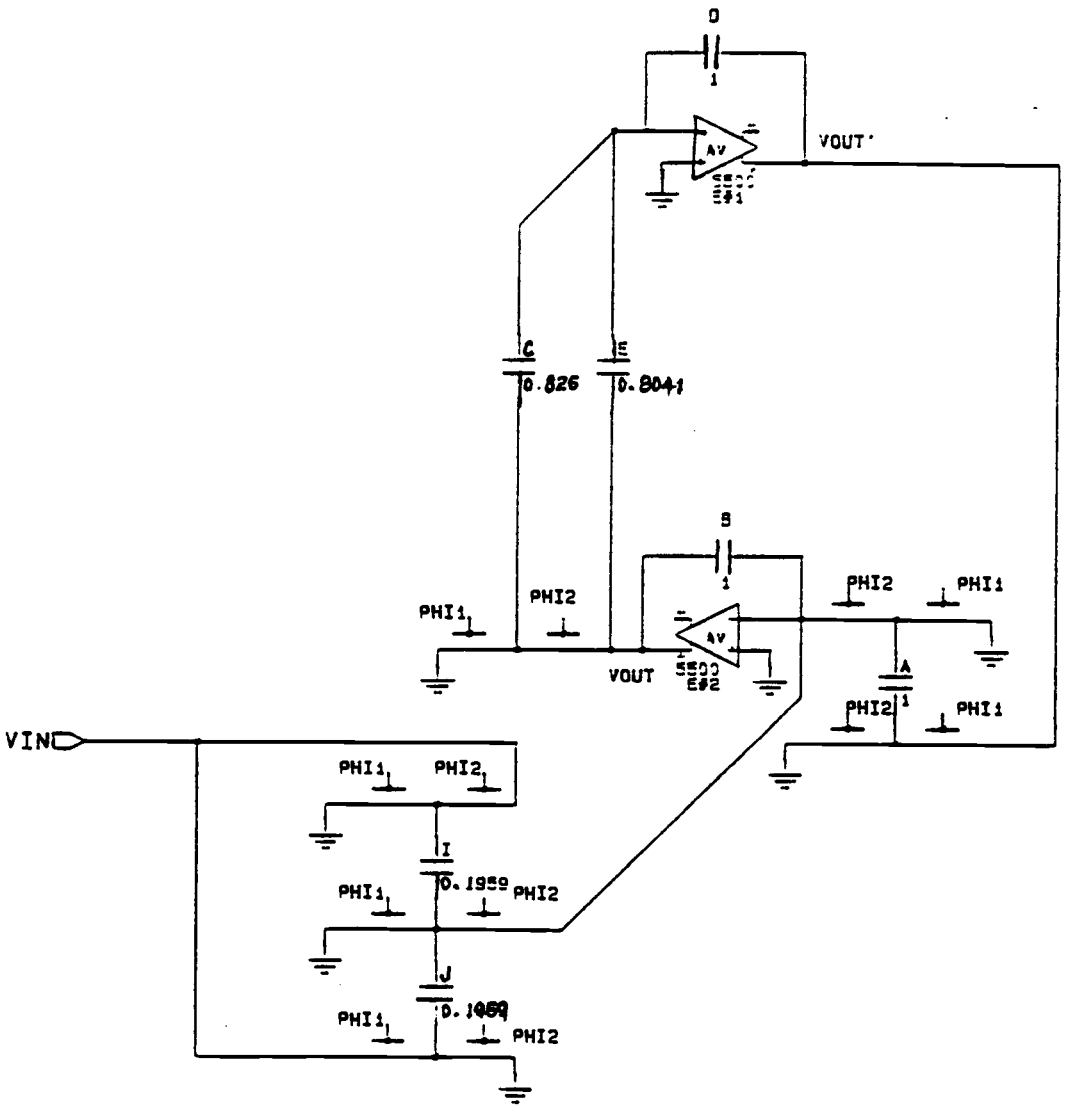


Fig. 29: SI highpass: E-circuit with the desired output at the 2nd stage

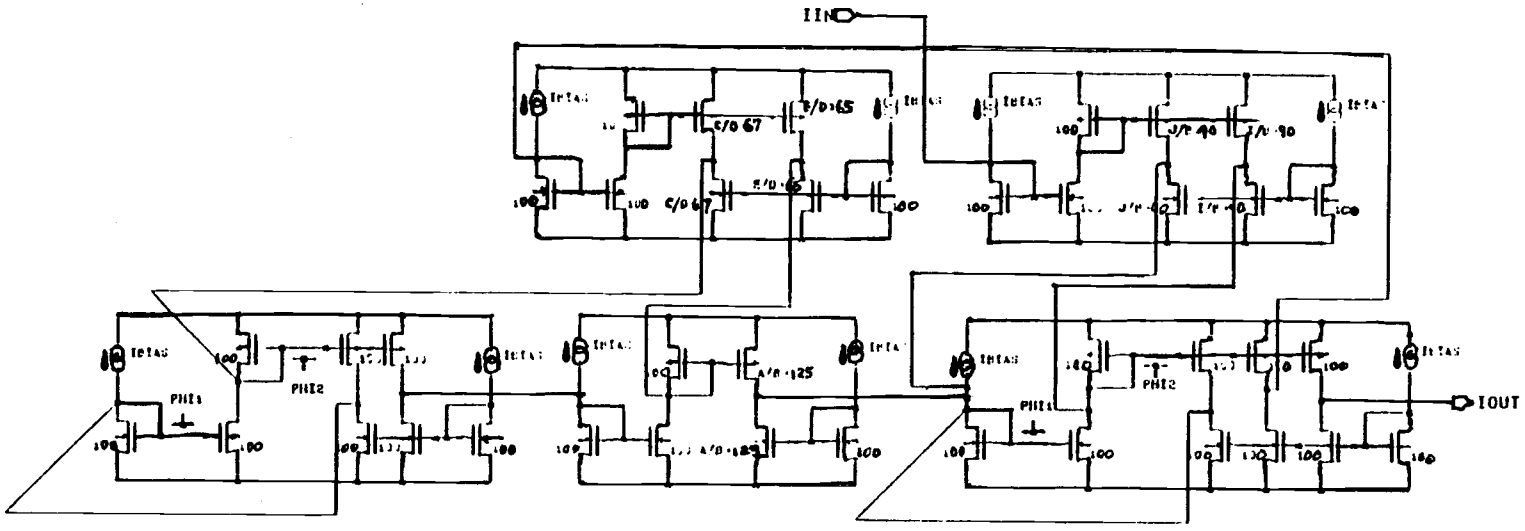


Fig.30: SC bandpass(10): E-circuit with the desired output at the 1st stage

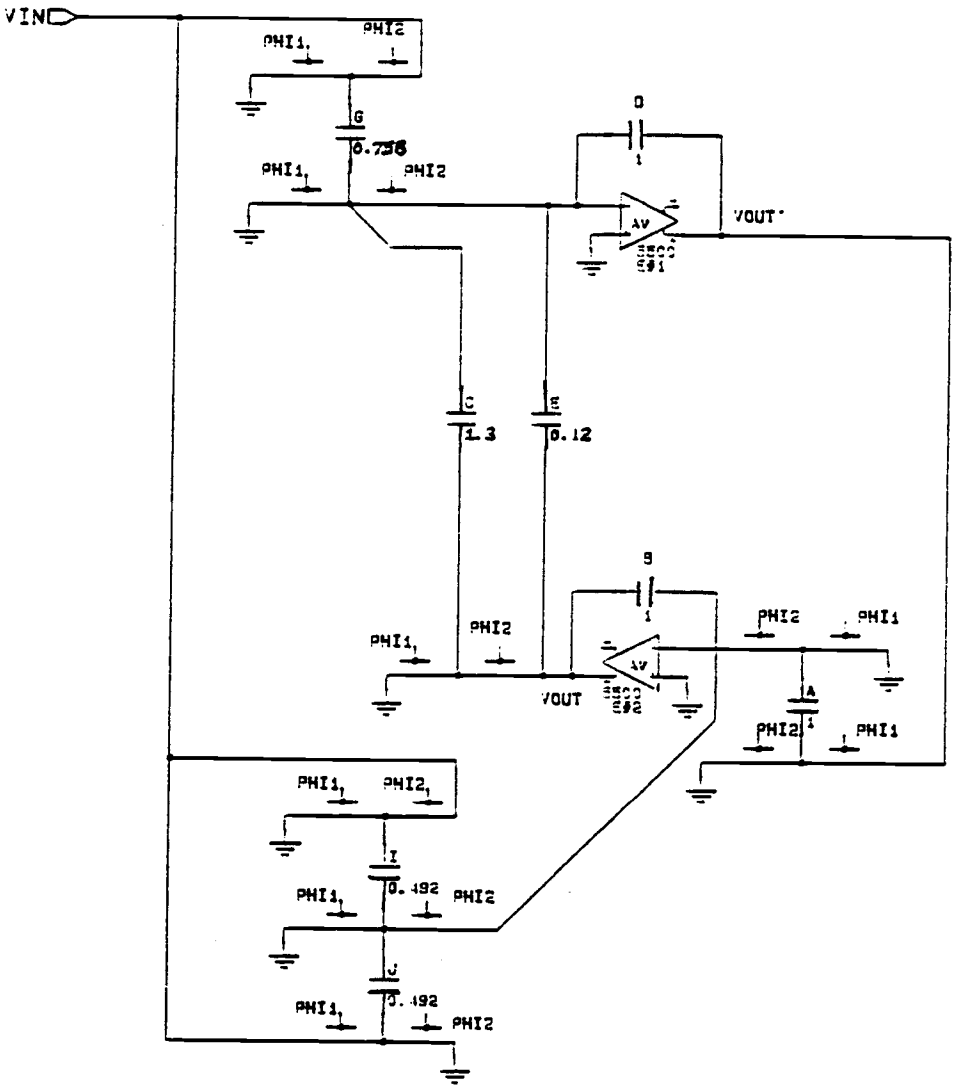
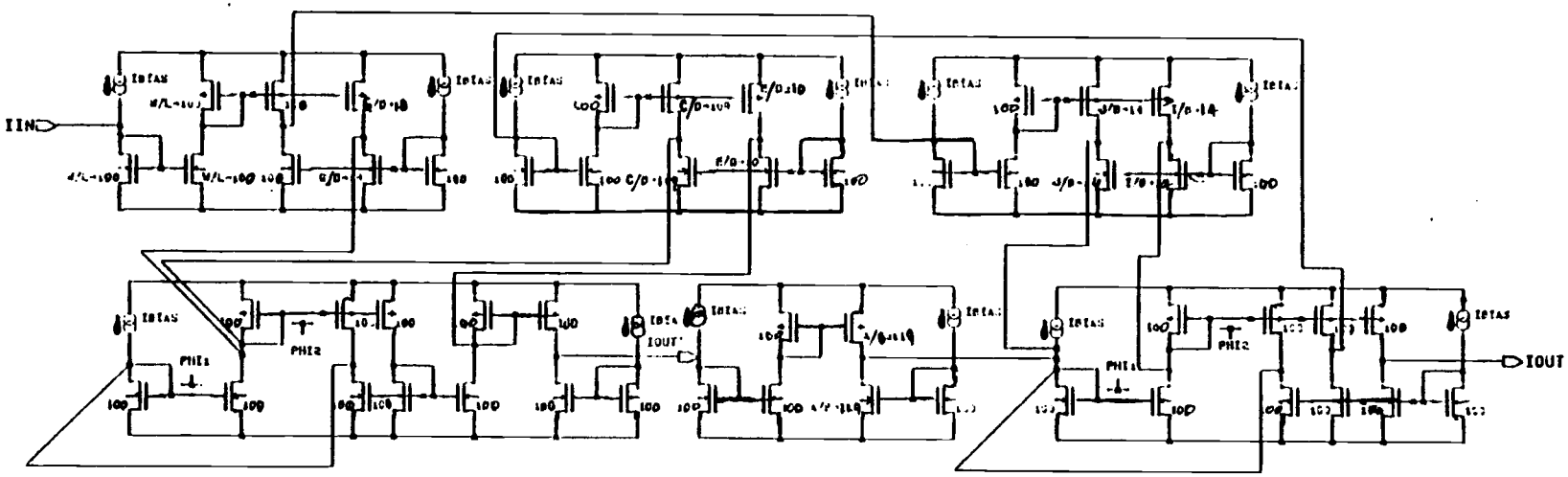


Fig. 31: SI bandpass(10): E-circuit with the desired output at the 1st stage



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[3] David J. Allstot, Robert W. Brodersen, and Paul R. Gray, "MOS Switched Capacitor Ladder Filters", IEEE JSSC, Vol. SC-13, No. 6, pp.806-814, Dec. 1978.

[4] Terri S. Fiez and David J. Allstot, "Design of CMOS Switched-Current Filters", IEEE International Solid-State Circuits Conference, Feb. 1990. (To be published)

[5] Ringo W. Lee, Terri S. Fiez, Howard C. Yang and David J. Allstot, "Distortion Analysis for a Switched-Current Track-and-Hold Circuit", IEEE International Symposium on Circuit and Systems, May 1990. (In review)

[6] Howard C. Yang, Terri S. Fiez and David J. Allstot, "Current-Feedthrough Effects and Cancellation Techniques in Switched-Current Circuits", IEEE International Symposium on Circuit and Systems, May 1990. (In review)

[7] Bass Steven, Digital Network Analysis Program, Purdue University, 1939.

[8] S.C. Fang, SWITCAP Program, Department of Electrical Engineering, Columbia University, 1982.

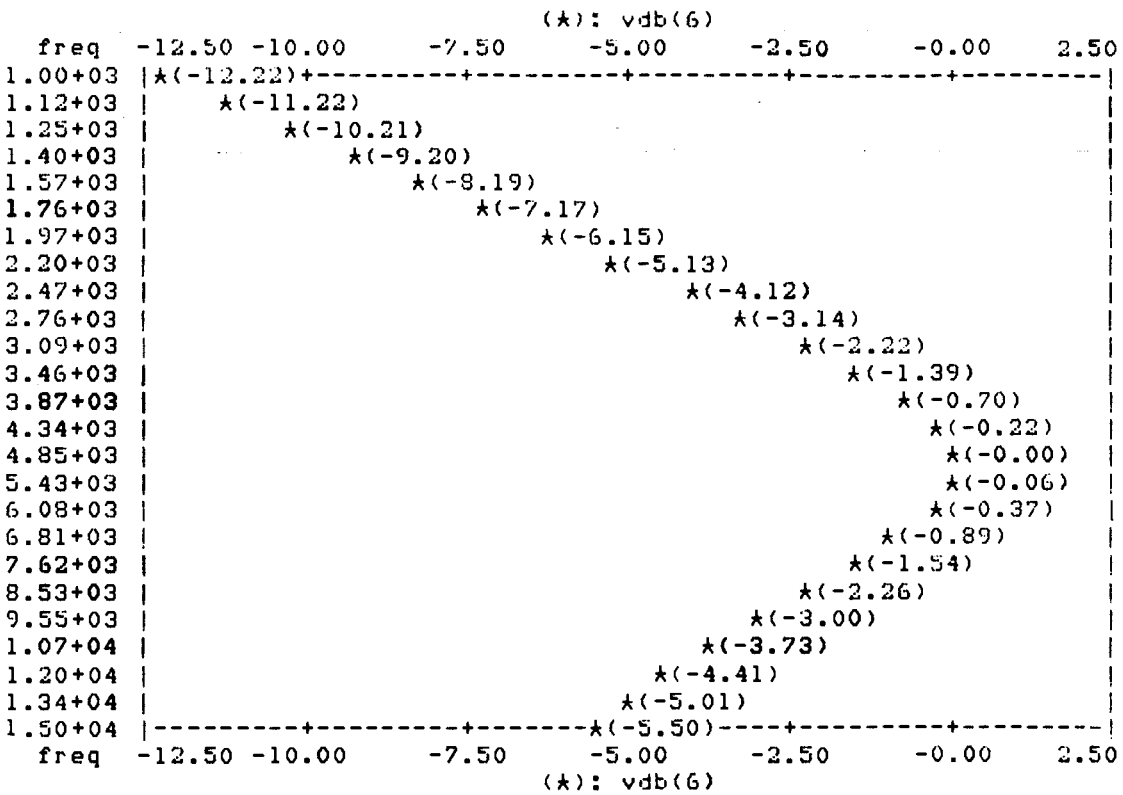
[9] Bor Lee, Terri S. Fiez and David J. Allstot, "CMOS Switched-Current Biquadratic Filters", IEEE International Solid-State Circuits Conference, Feb. 1990. (In review)

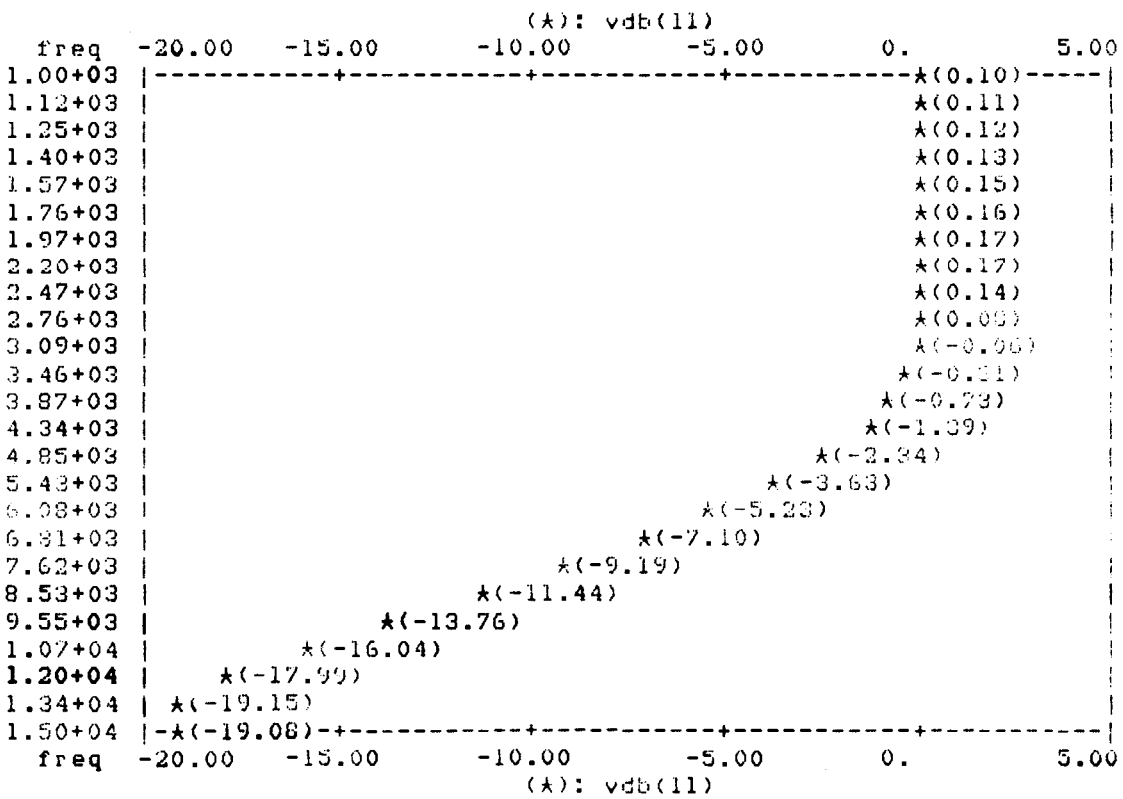
APPENDIX

VIII. APPENDIX

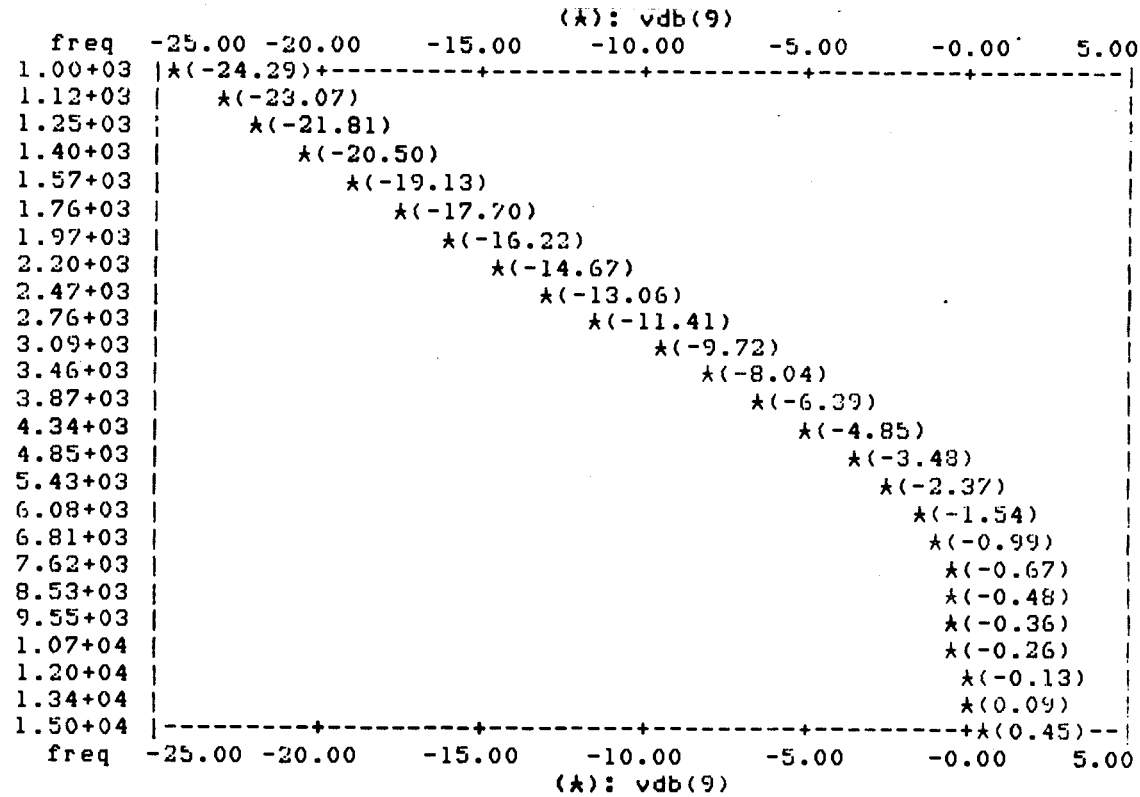
Appendix A. SWITCAP simulation programs and results for the design examples

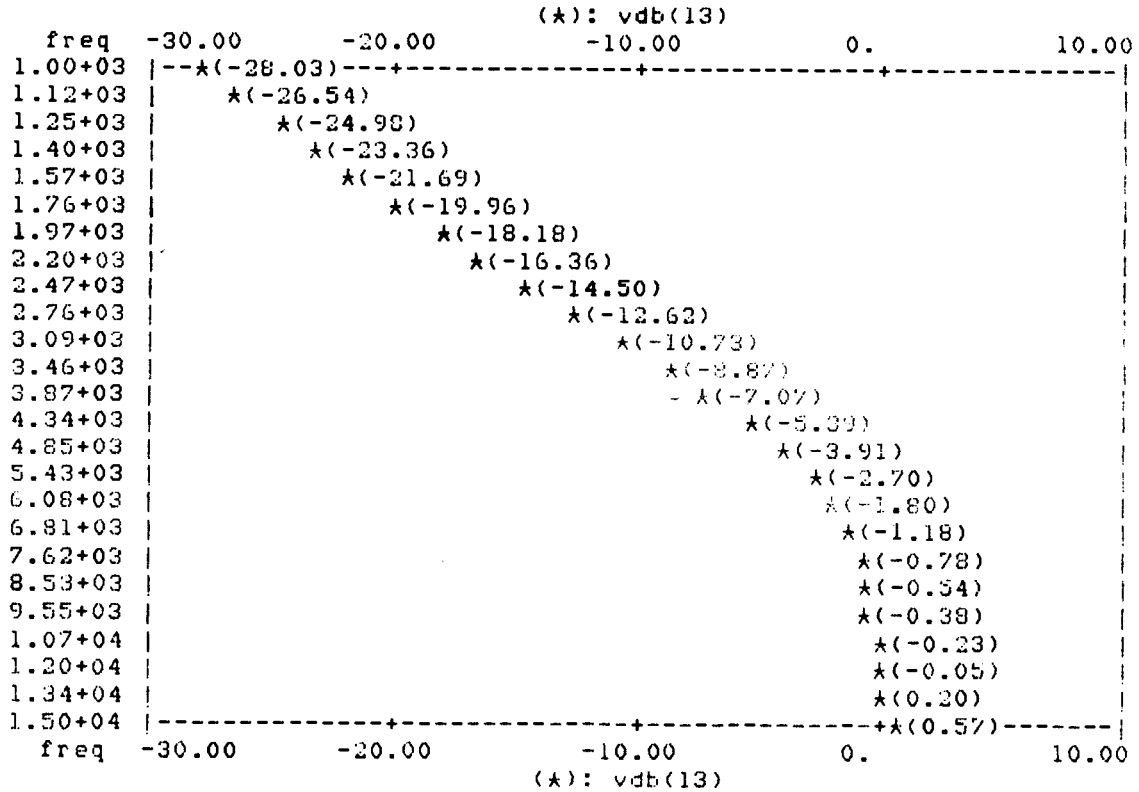
```
******* 5-Nov-89********SWITCAP A5R1 (27-Dec-84)********

Input Listing
**************************************************
 TITLE LPTE2;
 TIMING;
 PERIOD 40E-6;
 CLOCK CLK 1 (0 1/2);
 END;

 CIRCUIT;
 S1 (0 2) *CLK;
 S2 (1 2) CLK;
 S3 (0 3) *CLK;
 S4 (5 3) CLK;
 S5 (0 4) *CLK;
 S6 (4 11) CLK;
 S9 (0 8) *CLK;
 S10 (8 10) CLK;
 S11 (6 7) *CLK;
 S12 (7 0) CLK;
 S13 (0 12) *CLK;
 S14 (1 12) CLK;
 S15 (0 13) *CLK;
 S16 (10 13) CLK;
 S17 (1 14) *CLK;
 S18 (0 14) CLK;

 CG (2 3) 0.3476;
 CC (3 4) 0.346;
 CE (5 11) 0.389;
 CA (7 8) 0.448;
 CI (12 13) 0.0869;
 CJ (13 14) 0.0869;
 CD (5 6)  .448;
 CB (10 11) .5;
 E1 (6 0 0 5) 5500;
 E2 (11 0 0 10) 5500;
 V1 (1 0);
 END;

 ANALYZE SSS;
 INFREQ 1000 15E3 LOG 25;
 SET V1 AC 1 0;
 PLOT NOOVRLAY VDB(6) NUMBER VDB(11) NUMBER;
 END;
 END;
```


(★): vdb(6)
freq -12.50 -10.00 -7.50 -5.00 -2.50 -0.00 2.50
1.00+03 ★(-12.22)
1.12+03 ★(-11.22)
1.25+03 ★(-10.21)
1.40+03 ★(-9.20)
1.57+03 ★(-8.19)
1.76+03 ★(-7.17)
1.97+03 ★(-6.15)
2.20+03 ★(-5.13)
2.47+03 ★(-4.12)
2.76+03 ★(-3.14)
3.09+03 ★(-2.22)
3.46+03 ★(-1.39)
3.87+03 ★(-0.70)
4.34+03 ★(-0.22)
4.85+03 ★(-0.00)
5.43+03 ★(-0.06)
6.08+03 ★(-0.37)
6.81+03 ★(-0.89)
7.62+03 ★(-1.54)
8.53+03 ★(-2.26)
9.55+03 ★(-3.00)
1.07+04 ★(-3.73)
1.20+04 ★(-4.41)
1.34+04 ★(-5.01)
1.50+04 ★(-5.50)
freq -12.50 -10.00 -7.50 -5.00 -2.50 -0.00 2.50
(★): vdb(6)

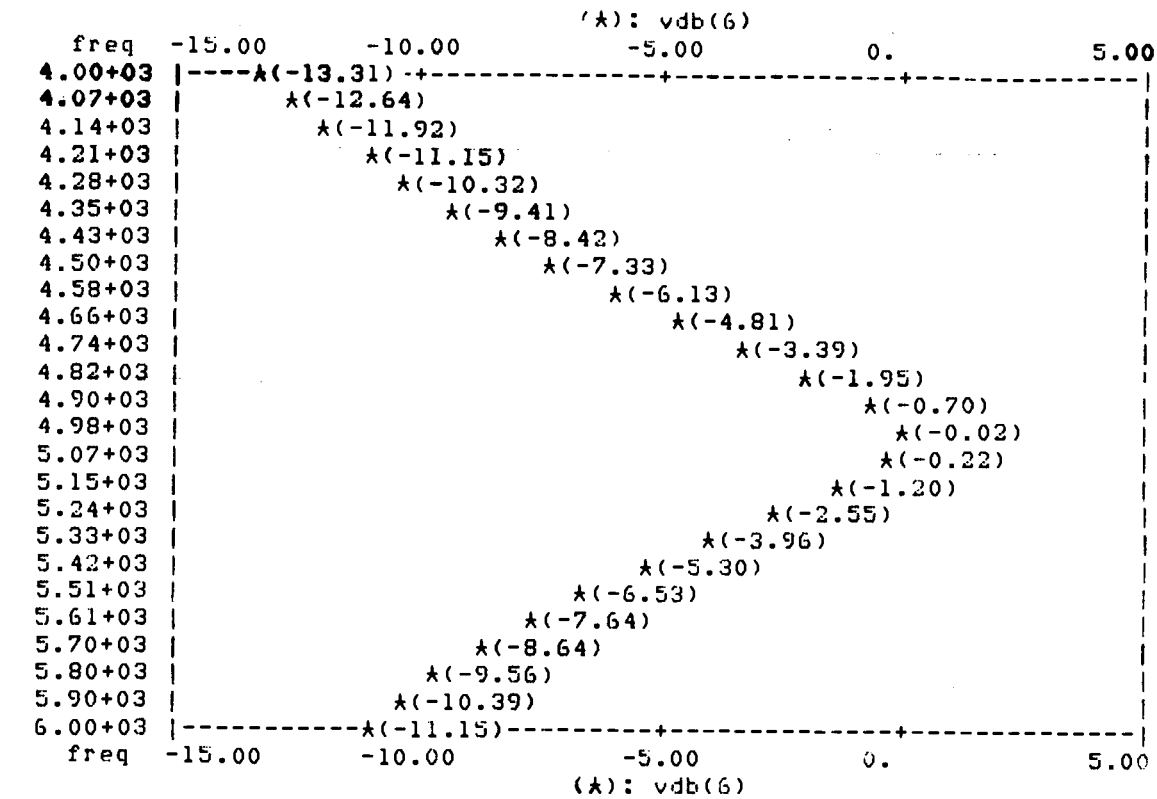

(★): vdb(11)
freq -20.00 -15.00 -10.00 -5.00 0. 5.00
1.00+03 ★(0.10)
1.12+03 ★(0.11)
1.25+03 ★(0.12)
1.40+03 ★(0.13)
1.57+03 ★(0.15)
1.76+03 ★(0.16)
1.97+03 ★(0.17)
2.20+03 ★(0.17)
2.47+03 ★(0.14)
2.76+03 ★(0.09)
3.09+03 ★(-0.06)
3.46+03 ★(-0.31)
3.87+03 ★(-0.73)
4.34+03 ★(-1.39)
4.85+03 ★(-2.34)
5.43+03 ★(-3.63)
6.08+03 ★(-5.23)
6.81+03 ★(-7.10)
7.62+03 ★(-9.19)
8.53+03 ★(-11.44)
9.55+03 ★(-13.76)
1.07+04 ★(-16.04)
1.20+04 ★(-17.99)
1.34+04 ★(-19.15)
1.50+04 ★(-19.08)
freq -20.00 -15.00 -10.00 -5.00 0. 5.00
(★): vdb(11)

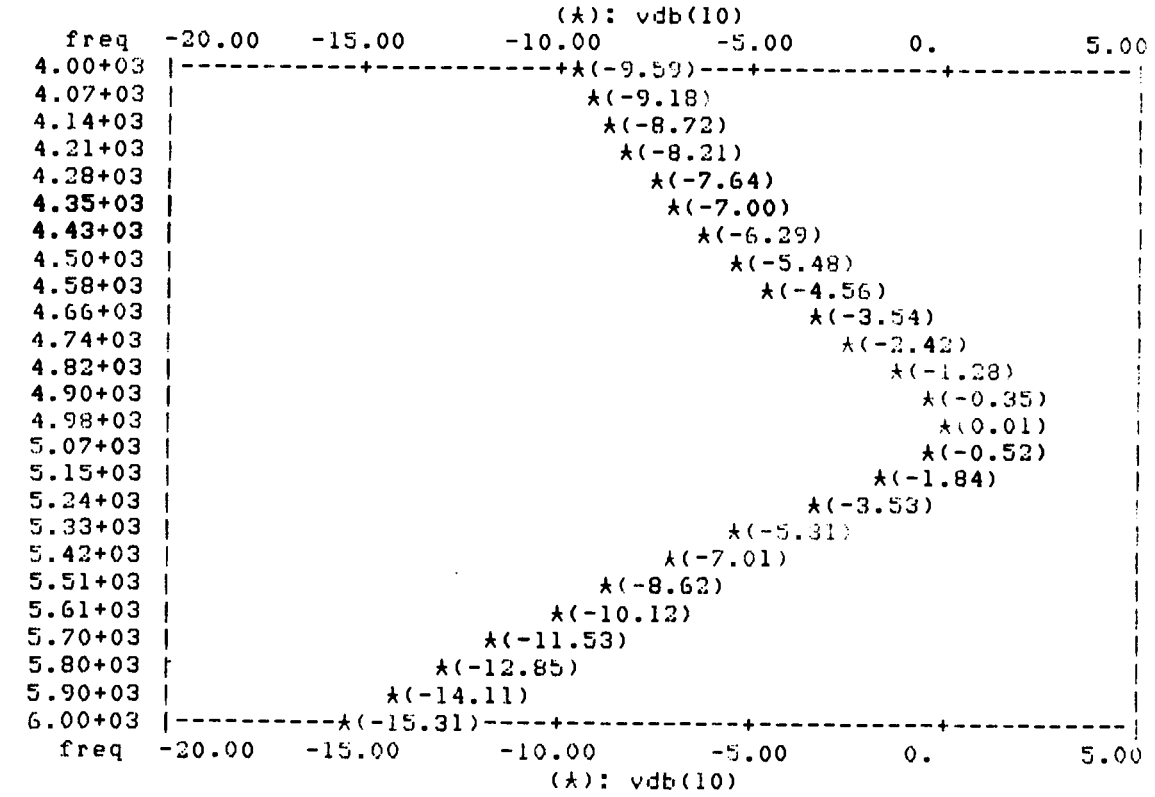
```
******* 5-Nov-89********SWITCAP A5R1 (27-Dec-84)*****

Input Listing
**************************************************
 TITLE HPTE2;
 TIMING;
 PERIOD 40E-6;
 CLOCK CLK 1 (0 1/2);
 END;

 CIRCUIT;
 S1 (0 10) #CLK;
 S2 (10 12) CLK;
 S3 (0 11) #CLK;
 S4 (11 13) CLK;
 S7 (0 7) #CLK;
 S8 (4 7) CLK;
 S9 (8 9) #CLK;
 S10 (0 8) CLK;
 S11 (0 2) #CLK;
 S12 (1 2) CLK;
 S13 (0 3) #CLK;
 S14 (3 4) CLK;
 S15 (1 5) #CLK;
 S16 (5 0) CLK;

 CC (10 11) 0.179;
 CE (12 13) 0.174;
 CI (2 3) 0.1959;
 CJ (3 5) 0.1959;
 CD (12 9) 0.2695;
 CB (4 13) 0.2167;
 CA (7 8) 0.27;
 E1 (9 0 0 12) 5500;
 E2 (13 0 0 4) 5500;
 V1 (1 0);
 END;

 ANALYZE SSS;
 INFREQ 1000 15E3 LOG 25;
 SET V1 AC 1 0;
 PLOT NOOVRLAY VDB(9) NUMBER VDB(13) NUMBER;
 END;
 END;
```


(★): vdb(9)
freq -25.00 -20.00 -15.00 -10.00 -5.00 -0.00 5.00
1.00+03 ★(-24.29)
1.12+03 ★(-23.07)
1.25+03 ★(-21.81)
1.40+03 ★(-20.50)
1.57+03 ★(-19.13)
1.76+03 ★(-17.70)
1.97+03 ★(-16.22)
2.20+03 ★(-14.67)
2.47+03 ★(-13.06)
2.76+03 ★(-11.41)
3.09+03 ★(-9.72)
3.46+03 ★(-8.04)
3.87+03 ★(-6.39)
4.34+03 ★(-4.85)
4.85+03 ★(-3.48)
5.43+03 ★(-2.37)
6.08+03 ★(-1.54)
6.81+03 ★(-0.99)
7.62+03 ★(-0.67)
8.53+03 ★(-0.48)
9.55+03 ★(-0.36)
1.07+04 ★(-0.26)
1.20+04 ★(-0.13)
1.34+04 ★(0.09)
1.50+04 ★(0.45)
freq -25.00 -20.00 -15.00 -10.00 -5.00 -0.00 5.00
(★): vdb(9)


(★): vdb(13)
freq -30.00 -20.00 -10.00 0. 10.00
1.00+03 ★(-28.03)
1.12+03 ★(-26.54)
1.25+03 ★(-24.98)
1.40+03 ★(-23.36)
1.57+03 ★(-21.69)
1.76+03 ★(-19.96)
1.97+03 ★(-18.18)
2.20+03 ★(-16.36)
2.47+03 ★(-14.50)
2.76+03 ★(-12.62)
3.09+03 ★(-10.73)
3.46+03 ★(-8.87)
3.87+03 ★(-7.07)
4.34+03 ★(-5.39)
4.85+03 ★(-3.91)
5.43+03 ★(-2.70)
6.08+03 ★(-1.80)
6.81+03 ★(-1.18)
7.62+03 ★(-0.78)
8.53+03 ★(-0.54)
9.55+03 ★(-0.38)
1.07+04 ★(-0.23)
1.20+04 ★(-0.05)
1.34+04 ★(0.20)
1.50+04 ★(0.57)
freq -30.00 -20.00 -10.00 0. 10.00
(★): vdb(13)

```
******* 5-Nov-89********SWITCAP A5R1 (27-Dec-84)******

Input Listing
**************************************************
 TITLE BPTE1;
 TIMING;
 PERIOD 40E-6;
 CLOCK CLK 1 (0 1/2);
 END;

 CIRCUIT;
 S1 (0 2) *CLK;
 S2 (1 2) CLK;
 S3 (0 3) *CLK;
 S4 (3 4) CLK;
 S7 (0 8) *CLK;
 S8 (8 9) CLK;
 S9 (6 7) *CLK;
 S10 (0 7) CLK;
 S11 (0 12) *CLK;
 S12 (1 12) CLK;
 S13 (0 13) *CLK;
 S14 (9 13) CLK;
 S15 (0 11) *CLK;
 S16 (10 11) CLK;
 S17 (1 14) *CLK;
 S18 (0 14) CLK;

 CG (2 3) 0.758;
 CC (3 11) 4.688;
 CE (4 10) 0.4327;
 CD (4 6) 4.3;
 CB (9 10) 3.606;
 CA (7 8) 4.3;
 CI (12 13) 0.492;
 CJ (13 14) 0.492;
 E1 (6 0 0 4) 5500;
 E2 (10 0 0 9) 5500;
 V1 (1 0);
 END;

 ANALYZE SSS;
 INFREQ 4E3 6E3 LOG 25;
 SET V1 AC 1 0;
 PLOT NUOVRLAY VDB(6) NUMBER VDB(10) NUMBER;
 END;
 END;
```





*SWITCAP: end of run