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Min Shen for the degree of Master of Science in Electrical and Computer Engineering presented on March 10, 1998.

Title: Analysis and Measurement of Charge Injection in Switched-Capacitor Circuits.

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Gabor C. Temes

It has been verified by theoretical analysis, circuit simulation and test that two switch transistors in parallel in a simple sample and hold circuit can be achieve high speed with low error voltage due to charge injection. The wide transistor provides low RC time constant when it is closed and the narrow one ensures a low error voltage. However, trade-off can be made in a specific application. A concise analytical expression for switch-induced error voltage on a switched capacitor is derived in this thesis. It can help designer to make the optimum decision. Experimentally, it was found that the optimum size of the wide transistor is several times wider than the narrow one.

Delayed clock scheme can be used to make charge injection signal-independent in a basic integrator structure. Using two transistors with different sizes and clock duty cycles in parallel can take advantage of the fast speed of the wide transistor and the small charge injection error of the small transistor. However, the combination of the two devices, including the size and clock duty cycles, should be chosen carefully to achieve the improvement.

Analysis and Measurement of Charge Injection in Switched-Capacitor Circuits

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Chapter 1. Introduction

This thesis presents the analysis and measurement of charge injection in switched-capacitor circuits. Performance of the structure that has two switch transistors with different sizes in parallel is analyzed by a derived closed-form expression and verified by a test circuit. This switch structure can also be used to improve the performance of other switched-capacitor circuits, such as a basic integrator circuit with a delayed clock scheme.

1.1 Background

Presently, the most popular technology for realizing microcircuits makes use of MOS transistors. MOS transistors are actually four-terminal devices, with the substrate being the fourth terminal. The simplified cross section of an N-channel enhancement MOSFET is shown in Figure 1.1. When the gate-source voltage V_{GS} is larger than the threshold voltage V_T, the channel is present. The channel charge density is proportional to V_{GS}-V_T. When the MOSFET is being turned off, the channel charge will flow from under the gate out through the terminals to other elements in the circuit. This phenomenon is called charge injection.

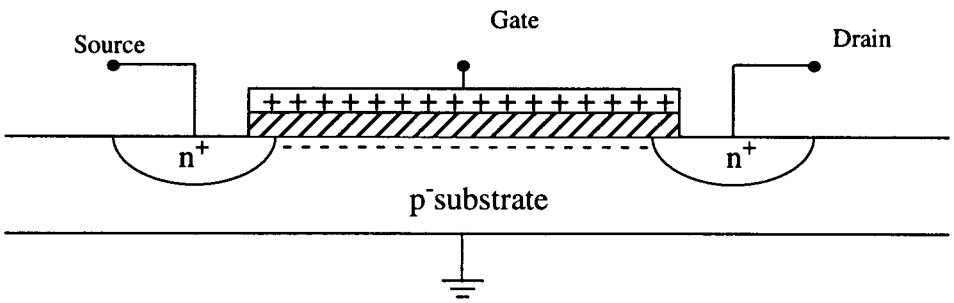


Figure 1.1: An n-channel MOS transistor

The charge injection error in switches is one of the factors limiting the accuracy of high-speed circuits. This effect reduces the performance and maximum clock frequency of the circuits in applications such as sample-and-hold stages, A/D converters, switched-capacitor and switched-current filters. The accuracy of instrumentation circuits also suffers from this error.

The simplest way to reduce errors due to charge injection is to use large capacitors. However, this needs large silicon area and slows down the circuit as well.

An alternative approach for minimizing errors is to use fully differential design techniques. The errors now are due to mismatches in the charge injection of the circuit structure, which will typically be at least ten times smaller than in the single-ended case [1].

Some techniques, such as dummy switches [2], are based on the fact that channel charges flow to the source and drain equally when the fall rate of clock signal is very high. Transmission gates also obtain better performance against charge injection.

Other than making the error voltage level lower, another goal is to make the charge injection signal-independent so that there is no nonlinearity and distortion problem. Normally the delayed clock scheme is used to solve this problem [1][3].

1.2 Outline

Chapter 2 describes modeling, simulation and some experimental results for charge injection in a simple sample-and-hold circuit. A concise model for the parallel switches is derived. Chapter 3 analyzes and simulates charge injection of a critical switch in a basic integrator circuit. Conclusion and direction for future work are given in Chapter 4.

Chapter 2. Charge Injection in a Sample and Hold circuit

The next two chapters deal with the analysis and measurement of charge injection in two basic switched-capacitor circuits, sample and hold (S/H) circuits and integrators. This chapter describes the modeling, simulation and some experimental results for charge injection in an RC S/H circuit, while the next chapter describes the analysis and simulation of charge injection of a critical switch in the basic integrator circuit.

2.1 Introduction

In a monolithic sample-and-hold circuit, the signal is stored on a capacitor. The accuracy of sample-and-hold circuits is disturbed by charge injected when the sampling switch turns off. The majority of sample-and-hold circuits are implemented using MOS technologies because the high input impedance of MOS devices allows an excellent holding function. An example of these circuits is show in Figure 2.1. When the switch

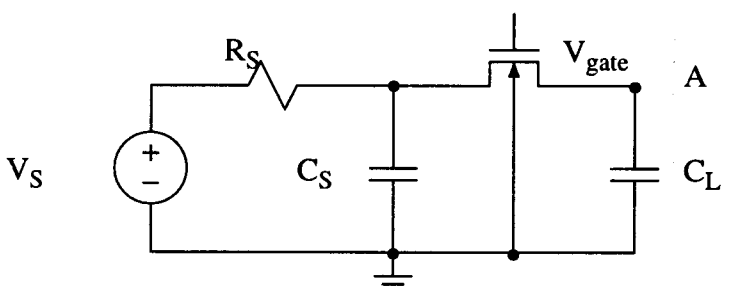


Figure 2.1: A sample-and-hold circuit with signal source resistance and capacitance

connecting the signal-source node and the data-storage node is turned on, the data stored in C_L at the storage node A will be held until the next operation occurs. However, a MOS switch is not an ideal switch. Mobile carriers are stored in the channel when an MOS transistor conducts. When the transistor turns off, the channel charge exits through the source, the drain, and the substrate. Experiment in [4] showed that when the fall time of the

clock signal is much larger than the longest time needed by mobile charges to reach one end of the channel, the charges leaking to the substrate could be neglected. Therefore, the switch transistors with short-channel lengths can make use of this feature. However, the charge transferred to the data node during the switch turning-off period superposes an error component on the sampled voltage. In addition to the charge from the intrinsic channel, the charge associated with the feedthrough effect of the gate-to-diffusion overlap capacitance also adds to the error voltage after the switch turns off [5].

2.2 Modeling the Switch Charge Injection

There have been some attempts to model the switch charge injection. A qualitative observation regarding a simplified case was made by Macquig [6]. Equations for the general case were derived and solved numerically by J.H. Shieh et al. [5]. This model was also validated with experimental evidence and its limitations were delineated by G. Wegmann et al. [4]. These results are based on an equivalent lumped model for the transistor, which guarantees node charge conservation. This configuration of the lumped model is not arbitrarily chosen but results from an exact analysis of the distributed MOSFET model as discussed in [7]. Analysis has shown that a slow switching slope (especially falling slope) and small transistor size can help to reduce the charge injection error. Another solution, introduced by Vittoz [2], is to step down the gate voltage first to a value just above V_T. Most of the channel charge is then released but is still able to flow back to the signal source capacitance before the transistor is fully opened in a second step. Simulation shows that this method works but the error voltage caused by the charge injection is very sensitive to the intermediate voltage. Also, it is not easy to implement the two-step signal. These solutions reduce the maximum possible frequency of operation. Therefore, an alternative method should be found to maintain or improve the accuracy while increasing the clock signal frequency.

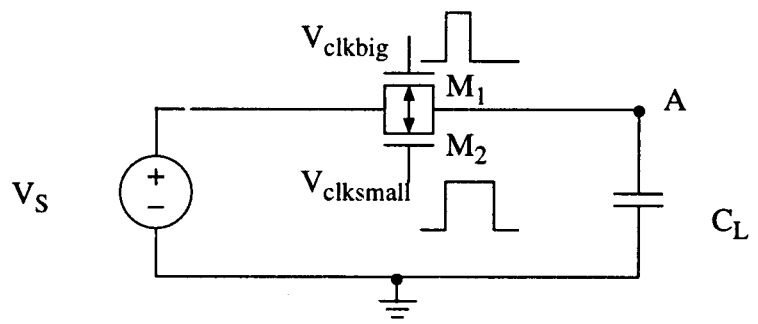


Figure 2.2: A sample and hold circuit with two switch transistors in parallel

If a wide transistor is used as the main switch to achieve a sufficiently high value of on-conductance and charging speed, a minimum width transistor may be placed in parallel with it, which is switched off in a second step only after the channel charge is released by the main transistor [3]. The circuit is shown in Figure 2.2. Zero source resistance and source capacitance are assumed so that the switch transistor is connected directly to the voltage source. During the sample period, both switch transistors are on and the output voltage is charged up to the signal voltage V_S within t_1, which is determined by the transistor size and the signal. Normally t_1 is much smaller than the clock period. Accurately speaking, the voltage over the load capacitor can approach V_S; however, it never reach V_S. So t_1 is usually defined as the time period needed for the circuit for obtaining a certain accuracy. Its expression is as follows:

$$t_1 = -\frac{C_L}{g_{ds1} + g_{ds2}} \ln\left(\frac{V_s - V_s \cdot percent_1}{V_s - V_0}\right) \tag{2.1}$$

where $percent_1$ is the accuracy which the sampled voltage can reach before the wide transistor opens and V_0 is the initial voltage on the load capacitor.

At the end of the sample stage, the wide switch begins to open first. The equivalent lumped model is shown in Figure 2.3.

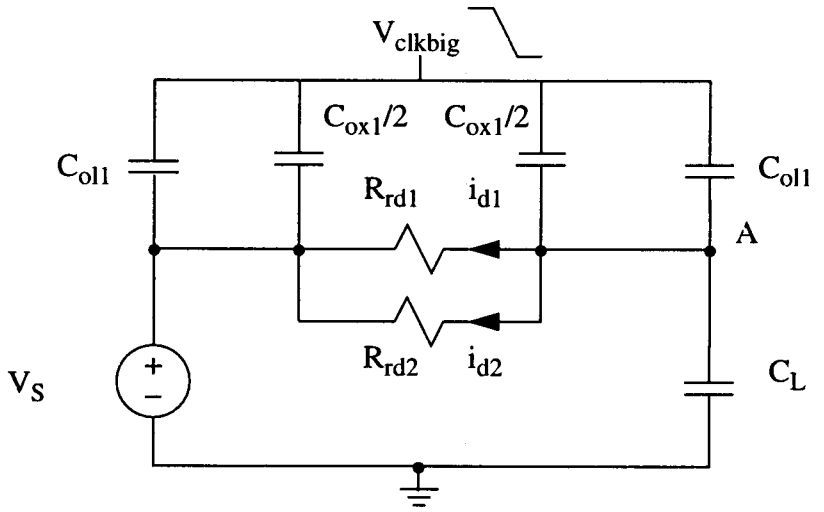


Figure 2.3: Equivalent lumped model during the time the wide switch is open.

The Kirchhoff's current law at node A requires

$$C_L \cdot \frac{dv_d}{dt} = -i_{d1} - i_{d2} - \left(C_{oli} + \frac{C_{ox1}}{2}\right) \cdot U \tag{2.2}$$

where

$$i_{d1} = \beta_1 (V_{HT} - U \cdot t) v_d , \tag{2.3}$$

$$i_{d2} = \beta_2 V_{HT} v_d , \tag{2.4}$$

$$V_{HT} = V_H - V_S - V_T , \tag{2.5}$$

In Eqs. (2.3), (2.4) and (2.5), the threshold voltage V_T for the two transistors is assumed to be the same. v_d is the error voltage at node A and V_s is the input voltage. β is the transistor conductance coefficient ($\mu \cdot C_{ox} \cdot \frac{W}{L}$). U is the gate voltage fall slope dv/dt.

The closed-form solution to Eq. (2.2) before the wide switch opens is

$$v_d(t) = \sqrt{\frac{\pi U C_L}{2\beta_1}} \cdot \frac{C_{ol1} + \frac{C_{ox1}}{2}}{C_L} \exp\left(\frac{\beta_1 U}{2C_L}\left(t - \frac{(\beta_1 + \beta_2)V_{HT}}{\beta_1 U}\right)^2\right) \qquad (2.6)$$

$$\left(erf\left(\frac{(\beta_1 + \beta_2)V_{HT}}{\sqrt{2\beta_1 U C_L}}\right) - erf\left(\frac{(\beta_1 + \beta_2)V_{HT}}{\beta_1 U}\right)\right)$$

Thus when $t_{11} = \frac{V_{HT}}{U}$, i.e., the wide switch transistor just turns off,

$$v_d(t_{11}) = \sqrt{\frac{\pi U C_L}{2\beta_1}} \cdot \frac{C_{ol1} + \frac{C_{ox1}}{2}}{C_L} \exp\left(\frac{\beta_2^2 V_{HT}^2}{2C_L\beta_1 U}\right) \qquad (2.7)$$

$$\left(erf\left(\frac{(\beta_1 + \beta_2)V_{HT}}{\sqrt{2\beta_1 U C_L}}\right) - erf\left(\frac{\beta_2 V_{HT}}{\sqrt{2C_L\beta_1 U}}\right)\right)$$

and while the gate voltage is falling from V_S+V_T to zero, the error voltage is mainly caused by the voltage coupling through the overlapping capacitance. Thus when the wide switch is completely open, the error voltage will be

$$v_d(t_{12}) = -\frac{C_{ol1} U}{\beta_2 V_{HT}} + \left(v_d(t_{11}) + \frac{C_{ol1} U}{\beta_2 V_{HT}}\right) \cdot \exp\left(-\frac{\beta_2 V_{HT}}{C_L} t\right) \qquad (2.8)$$

where $V_{clkbig} = 0$ when $t = t_{12}$ (Figure 2.4).

At this point only the small switch transistor is conducting. The load capacitor will be charged to the sampled voltage. During this procedure, the small transistor could be regarded as a resistor whose resistance is $1/g_{ds}$. If the ultimate output voltage is a fraction of the input signal, $V_S \cdot percent_2$, the charge up time is

$$t_2 = \frac{C}{g_{ds2}} \ln\left(\frac{V_S - V_S \cdot percent_2}{-v_d(t_{12})}\right) \qquad (2.9)$$

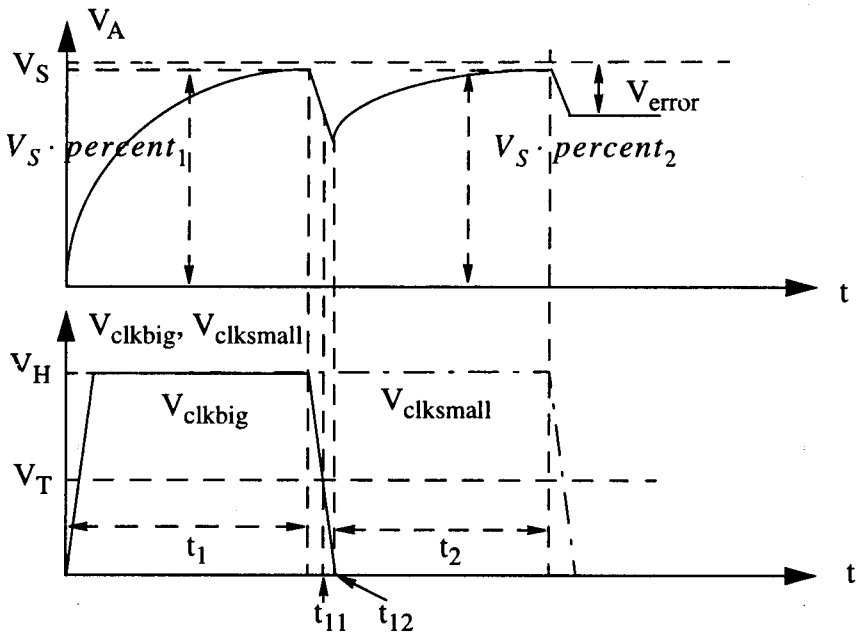


Figure 2.4: Output voltage and corresponding clock signals

A typical output voltage and corresponding time interval is shown in Figure 2.4. The maximum clock frequency is limited by the sum of t_1 and t_2, if we assume that the transition intervals of clock signal can be neglected compared with t_1+t_2.

The final error voltage, decided by the small transistor size, is

$$V_{error} = -\sqrt{\frac{\pi U C_L}{2\beta_2}}\frac{\left(C_{ol2}+\frac{C_{ox2}}{2}\right)}{C_L} erf\left(\sqrt{\frac{\beta_2}{2UC_L}}V_{HT}\right) - \frac{C_{ol2}}{C_L}(V_S+V_T) \quad (2.10)$$

$V_{error} < 0$ means that the final output voltage is less than the sampled voltage. So a trade-off has to be made between speed and error voltage. Here, the error voltage is the absolute value of V_{error}. Using Eq. (2.10), we can find a optimal combination of the two transistors, i.e., the small transistor decides the final error voltage while both switches will determine t_1+t_2 and the minimum clock period as well. As shown in Eq. (2.1) and Eq. (2.9), both t_1 and t_2 are functions of g_{ds1} and g_{ds2} in the triode region. Therefore, they are affected by the size of the two transistors. According to (2.10), V_{error} is influenced by the slope, U,

of the clock signal and the overdrive of the switch transistor V_{HT}. In the following simulations, U is fixed at a high value, 3 V/ns, since a high-speed application is under investigation. The input signal is also kept constant for simplicity.

2.3 Simulations

The preceding section described the theoretical and quantitative analysis of the charge injection in the sample and hold circuit. In this section, MATLAB and HSPICE simulation is done to verify the agreement between the model and the real circuit.

2.3.1 MATLAB Simulation

Since we have the closed-form solution, we try to find the optimal combination of the two switch transistors to meet the speed and accuracy requirement. Here we assumed the HP 0.6 μm CMOS technology. The input signal is DC 0.5 V. The range of wide switch width is from 2.7μm to 42μm. The small one is between 0.9 μm and 2.7 μm. The load capacitor is 1 pF. The lengths of the transistors discussed here are all 0.9 μm. As mentioned in the previous section, the charge times t_1 and t_2 determine the maximum clock frequency for a given switch combination. Their sum is taken as an index for speed, where t_1 is decided by the size of the two transistors and t_2 is decided by the instant error voltage due to the opening of the wide switch and the RC constant when only the small transistor is closed. The composite index $(t_1 + t_2) \cdot v_{error}$ is the product of the charge up time and the error voltage. However, for a specific application, these two indexes should be weighed differently.

In simulation, percent_1 in Eq. (2.1) and percent_2 in Eq. (2.9) are both chosen as 99.9% (10 bit accuracy). We assume that the wide transistor is opened just after the output accuracy is reached. Therefore the final error voltage mainly depends on the size of the

small transistor. This situation is not the optimum case in consideration of speed and error voltage as discussed later. The simulation results are shown in Figure 2.5.

According to Figure 2.5 (i), in the optimal combination the small transistor pair has the minimum product of error voltage and charging time. This means that if the speed and

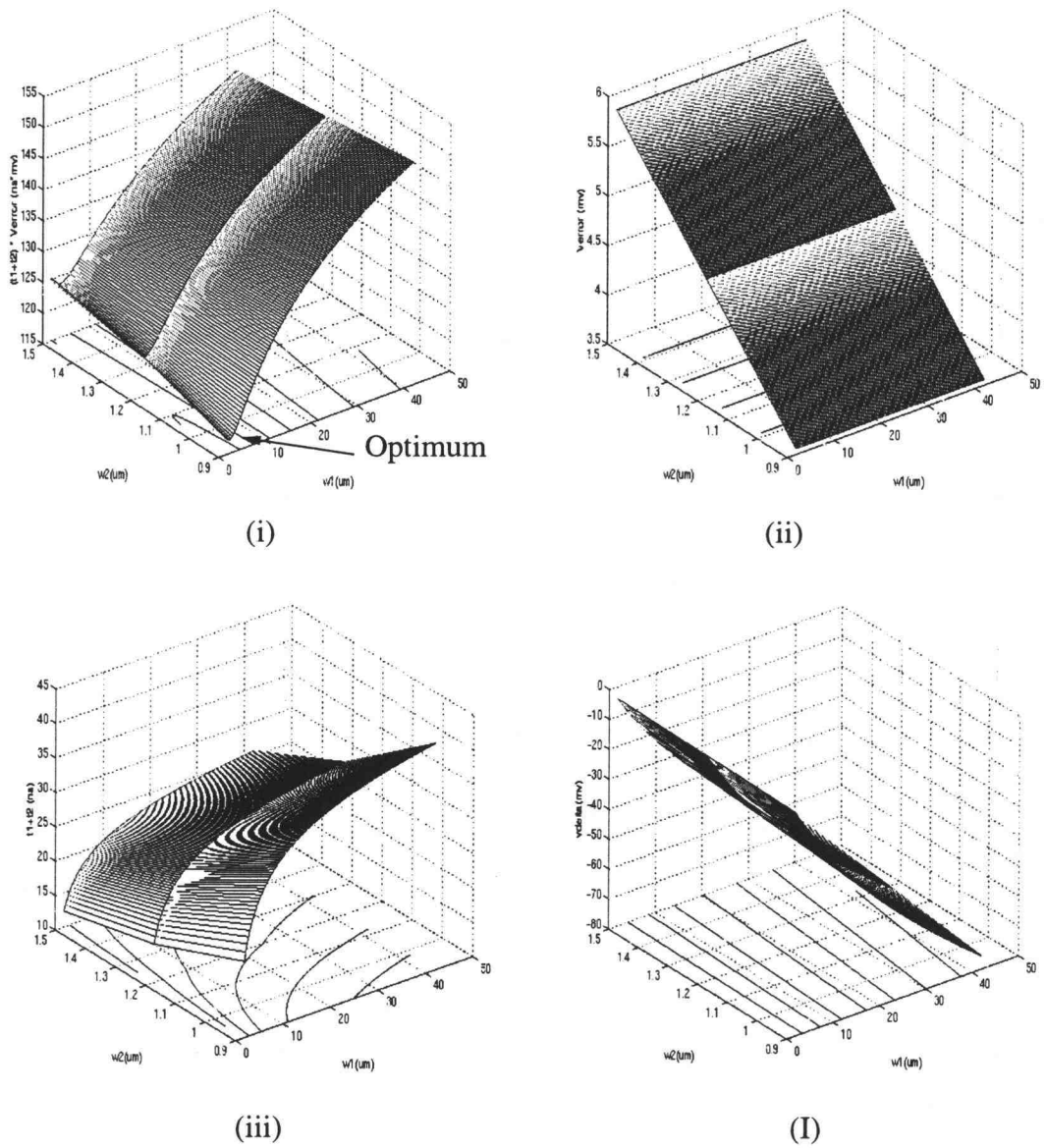


Figure 2.5: Simulation Results
i) $(t_1+t_2)*v_{error}$ ii) v_{error}
iii) (t_1+t_2) I) $v_d(v_{clkbig}=0)$

error voltage are equally important in an application, the switch transistor pair should be as small as possible. If the error voltage is given higher priority, pick the minimum size of the transistor and decide if it meets speed specification. If not, do a simulation as in Figure 2.5, compare the performance for the independent wider switch and that for a combination of minimum transistor and a parallel wider switch. Choose the better one as your circuit configuration.

2.3.2 HSPICE Simulation

Using HSPICE, we picked the several combinations of the two switch transistors and did transient analysis for the sample-and-hold circuit shown in Figure 2.2. Input signal is DC 0.5 V and clock signal frequency is 20 MHz. The clock signal and output voltage are

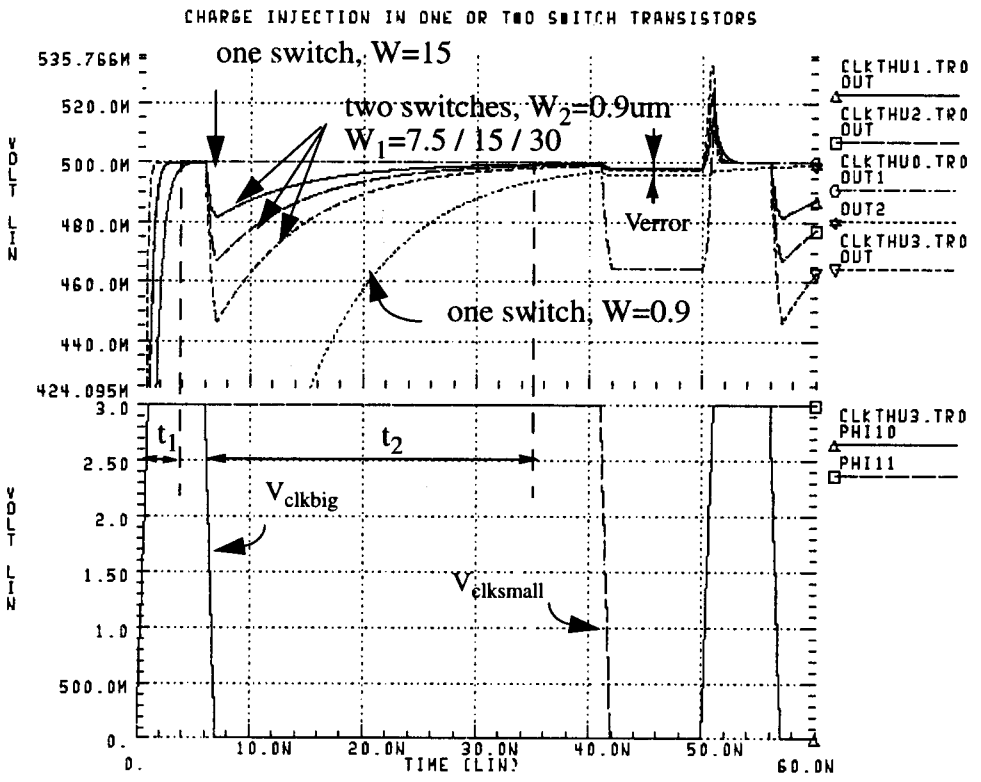


Figure 2.6: Simulation comparison for one and two switch scheme

shown Figure 2.6. The charge-up time after the wide switch opened, t_2, and the error voltage, v_{error}, were measured from Figure 2.6. and put in Table 2.1.

Table 2.1:Comparison of simulation and analysis

(W/L_2)	$(W/L)_1$	$v_d(V_{clkbig}=0)$(mV)		t_1+t_2(ns)	
		Analysis	Simulation	Analysis	Simulation
0.9/0.9	7.5/0.9	20.4	18.6	35.1	33.8
	15/0.9	36.0	33.0	37.7	36.3
	30/0.9	59.8	53.7	40.9	40.1

2.3.3 Summary

Comparing the simulation result shown in Figure 2.6 with the closed-form solution by MATLAB, we get the result in Table 2.1. Despite the discrepancy between the simulation and analysis, the charge injection model built in Figure 2.3 gave a good approximation of the circuit performance. One of the reasons which cause the disagreement is the subthreshold effect which plays a more important role when the load capacitance is small [10].

2.4 Optimization

For the simple sample-and-hold circuit, the accuracy and the speed are the most important. However, for a specific application, they are given different priorities.

It may be noticed that the parameter, $percent_1$, in Eq. (2.1) was fixed in the previous simulation, which means that for different combination of parallel transistors, the wide transistor is opened only after output is charged up very near to the sampled signal. In a real circuit, this is not necessary since the wide transistor is used only to speed up charging.

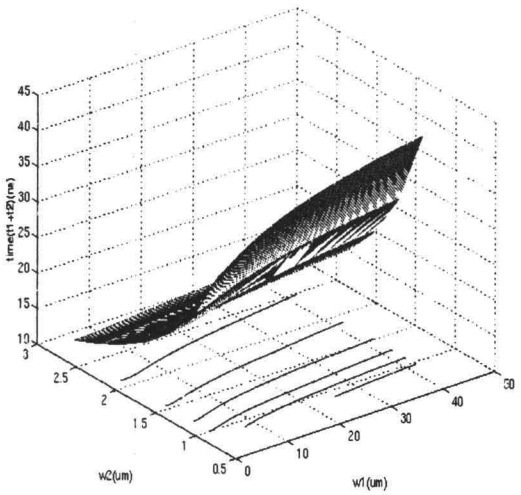
When the output capacitor is being charged, the voltage change is decreasing during the same period of time. In other word, the charging speed is decreasing as a exponential function. At some point, it could be even slower than the charging up speed when only the small transistor is closed. Therefore, it is possible that an optimum value of $percent_1$ exists which can make the charging up speed the fastest. This means to choose the optimal instant to open the big switch to make the circuit operate faster.

2.4.1 Error Voltage

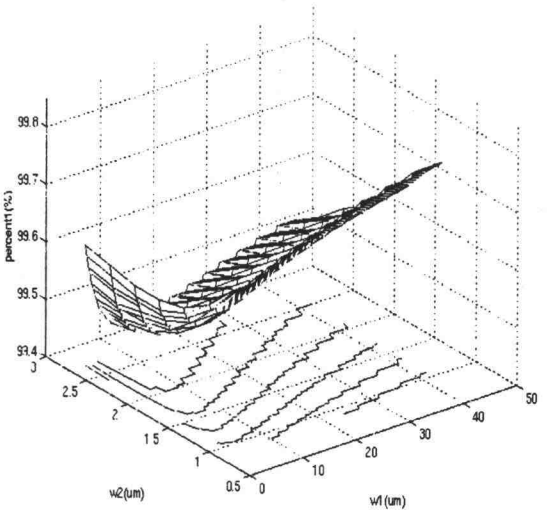
In some high-accuracy applications, the error voltage caused by charge injection should be minimized. Therefore, the transistor is chosen as small as possible. Using the two clock scheme shown in Figure 2.2., it is possible to speed up the operation. However we try to determine when is the best time to open the wide switch. In other word, how to spend the shortest time to reach the given accuracy.

The model in Figure 2.3 with MATLAB is used to do this job. In our simulation, the input signal is 0.5 V DC and the high level of clock signal is chosen as 3 V. The goal of the error is 0.1%, which means 10-bit accuracy. The simulation results are shown in Figure 2.7.

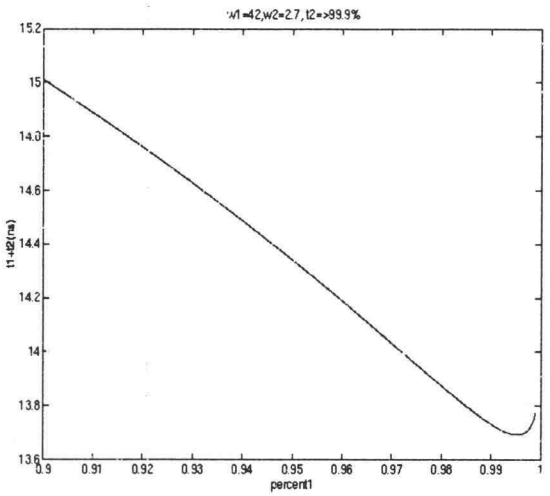
From (i), it could be concluded that for a given accuracy, the charge-up time, t_1+t_2, or the maximum clock signal frequency is mainly determined by W_2, the small transistor. The bigger W_2 is, the larger the maximum clock frequency could be. From previous simulation results, it is true that the second charge-up period, t_2, takes longer time than the first one, t_1, while it mainly depends on the size of the small transistor. According to Figure 2.7 (i), the maximum clock signal can be about 15 MHz (T=70 ns) with the minimum error voltage (W_2=0.9 μ m). It is also concluded that choosing too wide transistor does not help the speed improvement. For example, when W_2 is 0.9μ m, the maximum



(i) (w_1, w_2, t_1+t_2)



(ii) (w_1, w_2, $percent_1$)



(iii) ($percent_1$, t_1+t_2)

Figure 2.7: Optimization for error voltage with analytical model

(i) t_1+t_2, the shortest time period which the output take to reach 99.9% accuracy for different big and small transistors;
(ii) $percent_1$, the output voltage in term of percentage of the input when the wide switch is open corresponding to (i);
(iii) the time period which the output takes to reach 99.9% accuracy for a pair of specific transistors.
w_1 is the width of the wide transistor;
w_2 is the width of the small transistor;

clock frequency could be achieved when W_1 is 2.7μm, the smallest of the large transistors in our simulation. The reason is that although a bigger W_1 could make t_1 small, it also generates a bigger voltage drop at the output. It will take the small transistor more time to recover to the sample voltage, i.e., t_2 is bigger.

According to (ii), $percent_1$, the output in term of percentage of the input when the wide switch is open corresponding to (i), is in the range of 99.4%-99.8%.(The reason why

the graph looks discrete is that we sweep percent$_1$ with fixed step 0.01% to find the shorted t_1+t_2.) It means that if the maximum clock frequency is desired, the wide switch should be opened when the output approaches to the input signal. It is reasonable because if the wide transistor is opened too early, it leaves more voltage gap for the small transistor to charge. It will be slow. If the wide transistor is opened too late, the voltage drop caused by its charge injection happens delayed. The output voltage changes a little due to the exponential function during the period. So the circuit speeds up a little. Figure 2.7 (iii) shows an example. As the wide transistor is open later and later, percent$_1$ becomes bigger, but t_1+t_2 decreases until percent$_1$=99.6% and then increases again.

HSPICE was used to verify the model and the simulation results are used for comparison with the results from MATLAB. An example is shown in Figure 2.8. The optimum percent$_1$ is found to achieve the maximum speed. The area included in the circle

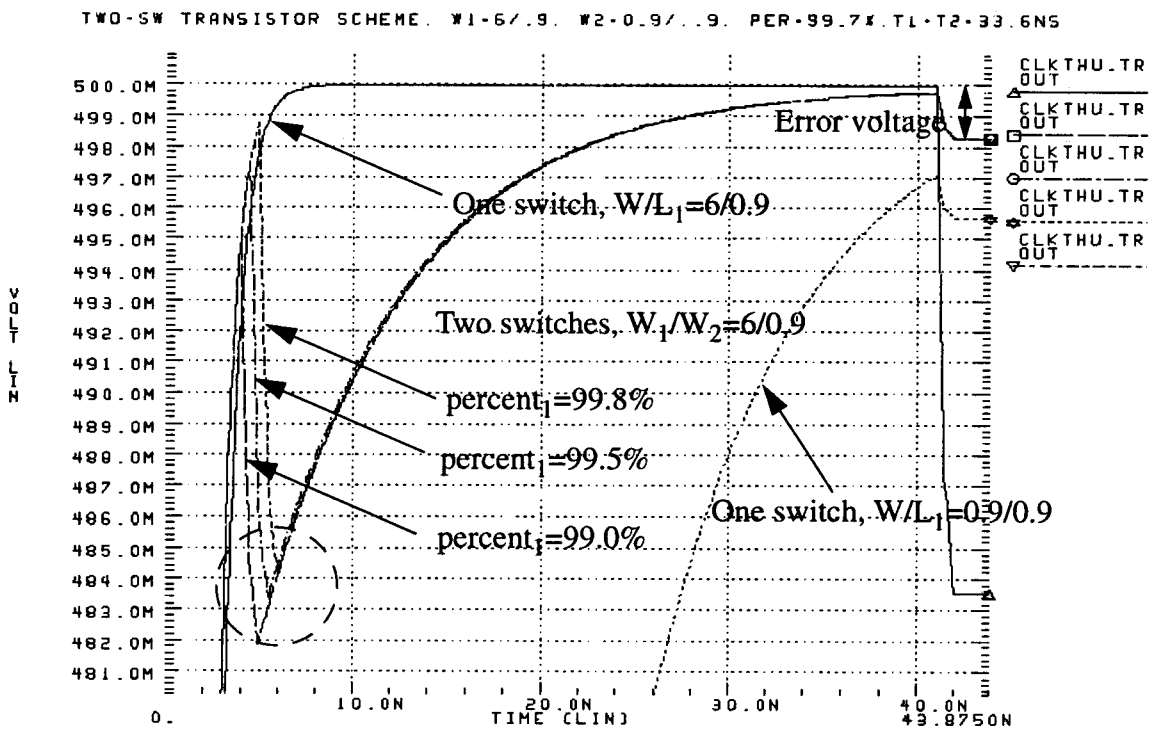


Figure 2.8: Optimization for error voltage

shows the optimum instant when the wide switch is opened. The curve with $percent_1$=99.5% is higher than the other two. Since the RC time constant is the same when only the small transistor is closed, it is concluded that 99.5% is the best value. It is also shown that the error voltage remains almost unchanged with different $percent_1$ if the output has been charged very near to the input signal before the small switch is opened. For a specific combination of W_1 and W_2, the optimal t_1+t_2 can be found in the simulation result like Figure 2.8.

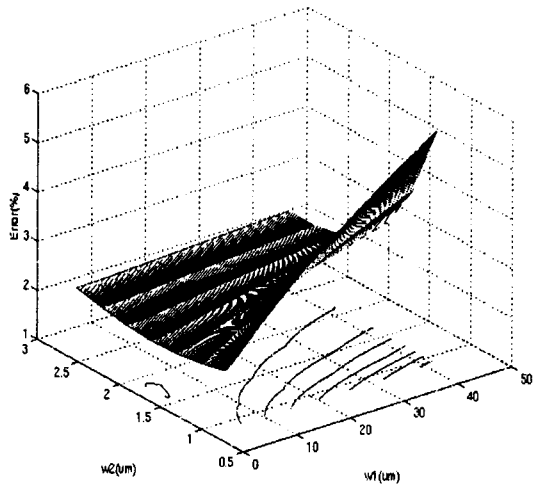
Table 2.2:Optimization by analysis and simulation

$W_1+W_2(\mu m)$	2.7+0.9		6+0.9		12+0.9	
	analysis	simulation	analysis	simulation	analysis	simulation
$percent_1$(%)	99.7	99.7	99.7	99.5	99.7	99.0
t_1+t_2(ns)	34.0	33.6	32.4	32.3	36.7	37.2

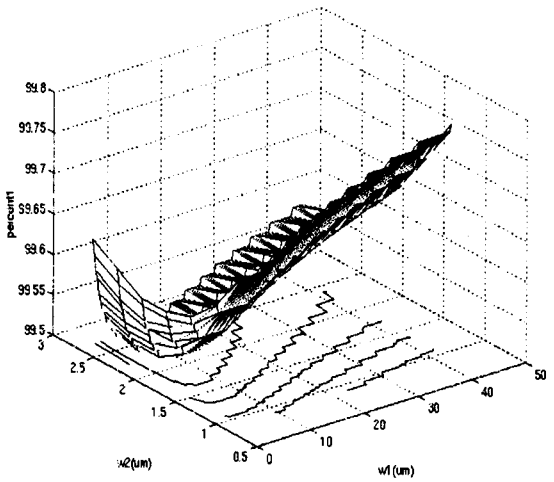
Table 2.2 shows the comparison of some simulation results with the analysis results using the model previously introduced. The model gives us a good approximation for t_1+t_2. By using this model, it is possible to find the proper time instant for opening the wide transistor. From Table 2.2 and Figure 2.8, the optimum $percent_1$ may be in the range 99.0%-99.9%. And in this range, t_1 and t_2 is not very sensitive to when the wide transistor is opened. It can been seen that in Figure 2.8 the curves with different $percent_1$ are almost combined into one when they are approaching the input signal level.

2.4.2 Fixed Clock Frequency

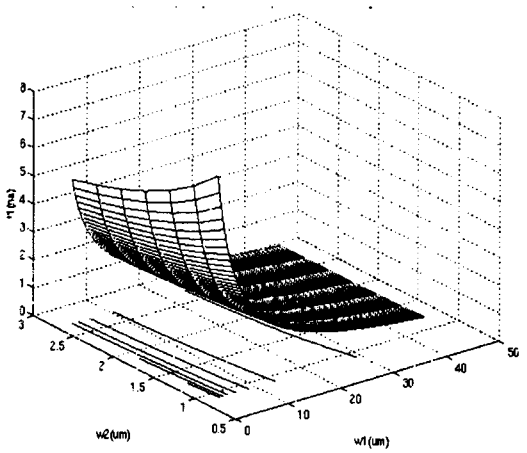
In some application, the system has to work at a fixed high frequency. For a sample and hold circuit, it means that it is impossible to wait for too long to charge up the load capacitor to the input signal level. In this situation, the combination of the big and small transistor can be chosen and the time instant when the wide transistor is opened need be adjusted so that the minimum error voltage could be achieved for the holding phase.



(i) (w_1,w_2, error)



(ii) (w_1,w_2, $percent_1$)



(iii) (w_1,w_2, t_1)

Figure 2.9: The minimum error voltage for the clock frequency 50 MHz with 50% duty cycle

(i) The minimum error voltage in term of the percentage of the sampled signal;
(ii) $percent_1$, the output voltage in term of percentage of the input when the wide switch is open corresponding to (i);
(iii) t_1, the time period when the wide transistor is closed, corresponding to $percent_1$ in (ii).

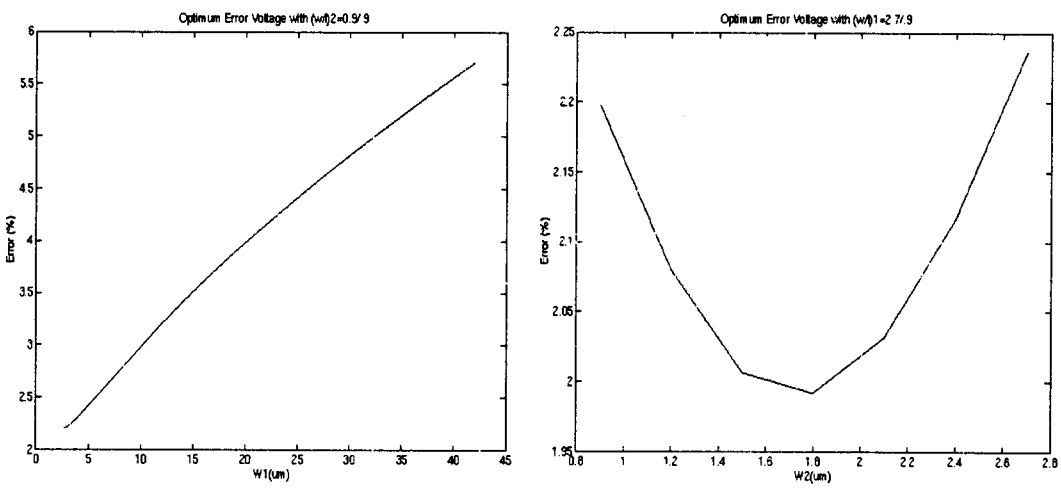
As in Section 2.4.1, MATLAB is used to find the optimum transistor pair and time instant. Similarly, the input signal is 0.5 V DC, the high level of the clock signal is 3 V, and the load capacitor is 1 pF.

Figure 2.9 (ii) and (iii) indicate that when the optimum error voltage is found for a given pair of transistor, the corresponding $percent_1$ is also in the range between 99.0%-99.9%. The time period t_1 when the wide transistor is closed is reduced as the wide transistor increases. This means that it is more difficult to control the time instant of

opening the wide switch when its size is too large, because the rising edge of the charge curve is very sharp.

Figure 2.9 (i) shows that the minimum error voltage for a sample-hold circuit working in 50MHz clock frequency with 50% duty cycle is about 2% for 0.5 V DC input, i.e., 10 mV. The width of the wide transistor is 3.3 μm and the width of the small transistor is 1.8 μm.

The explanation of the curve is the following: we assume that the RC time constant for two transistors in parallel is short enough to ensure that in half a clock period, the load capacitor could be charged up to the input signal with a certain accuracy. When the width of the small transistor is minimum, 0.9 μm in this case, the error voltage is mainly determined by the voltage drop when the wide transistor is opened. If the wide transistor is small, the voltage drop caused by charge injection of the wide switch is small, which allows the small transistor have more time to charge up in a fixed clock period. Thus the error voltage is small. When the wide transistor becomes larger, it will generate a large voltage drop. Although it could charge up more quickly and it saves some time for the small



(i) (ii)

Figure 2.10:Two cross sections of Figure 2.9
(i) $W_2 = 0.9\mu m$ (ii) $W_1 = 2.7\mu m$

transistor to recover, the large voltage drop causes the small transistor to take more time to charge the load capacitor to a certain accuracy. So at the end of the clock, the error voltage is even larger. That is exactly what (i) of Figure 2.10, tells.

When the wide transistor is relatively small, the time slot which the large transistor left for the small transistor was not big enough to recover to the input voltage level with a high accuracy. The error voltage will be decided by two factors. One is the voltage level just before the small transistor opens. The other is the voltage drop caused by the charge injected from the transistor channel. At first the first error source is dominant. As the small transistor increases, the charging speed is faster and the error voltage is smaller. When it reaches a critical value, the RC constant is small enough for the small transistor to charge the load capacitor to a very high accuracy. The second factor then takes control. The error voltage begins to be determined by the charge injection of the small transistor. Therefore as W_2 increases, the error voltage increases. That is what happens in (ii) of Figure 2.10.

When the big and small transistor are both relatively big, charging is fast when they are both on. After the wide switch opens, the small transistor can make the output recover to the input signal quickly. At that time, the error voltage is decided by the charge injection of the small transistor. For a given small transistor, the error voltage does not change too much, which is also shown in Figure 2.9.

We can predict that when the wide transistor is very big, the error voltage will be increased again, since the voltage drop caused by it is too large for the small transistor to charge the load capacitor in a small time period.

Therefore the optimum pair of the transistor may be several times bigger than the minimum transistor. In our case, for 0.5V DC input, the optimum combination is 1.8 μm

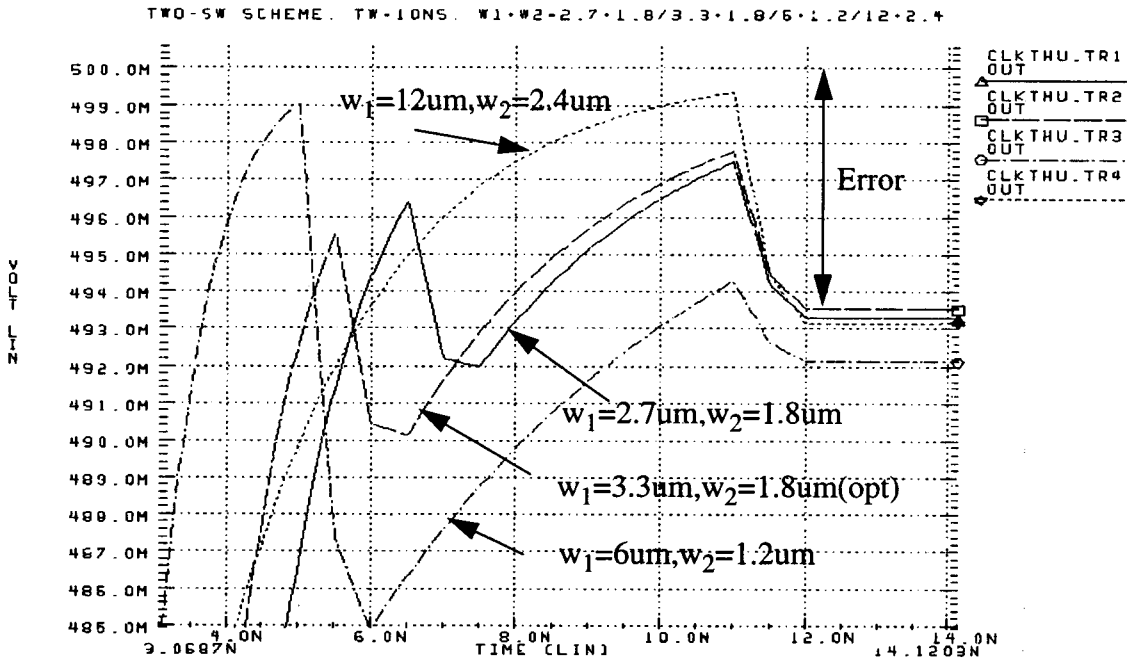


Figure 2.11:Hspice simulation result indicating the optimum size of transistor pair in a fixed time period

and 3.3 μm, according to the simulation. HSPICE simulation result in Figure 2.11 agrees with the prediction. This result also shows that t_1 could be controlled since it is around 20% of the clock period if its duty cycle is 50%. The error voltage is not very sensitive to t_1 in this case, because the wide transistor is not very large and the rising edge of the charging curve is not too sharp.

2.4.3 Summary

The model in Figure 2.3 can be used to predict an optimal combination of parallel transistors in purpose of the error voltage or the speed. The HSPICE simulation agrees well with the MATLAB analysis using the model (see Table 2.2).

2.5 Experimental Results

Since a MOSFET array in a IC-package is not available commercially, discrete devices had to be used for the verification of the scheme and the model.

The NTE465 N-channel enhancement-mode MOSFET IC was used as switch transistors to build the test circuit (Figure 2.12). C_d was chosen a parallel combination of an electrolytic capacitor with 100 μF and a ceramic capacitor 0.01 μF. The electrolytic capacitor is used to keep the source voltage of the switch as constant as possible so that the input node can be regarded as being connected to an ideal voltage supply. The ceramic capacitor is used to filter the high frequency noise. C_L is a paper dielectric capacitor with 1100 pF. It is big enough because the parasitic capacitance of NTE465 is 5 pF according to the data sheet and it is much less than C_L. The capacitance is also chosen so that the error voltage is big enough for measurement. M_{reset} is a power MOSFET, ZDM4306N, used for

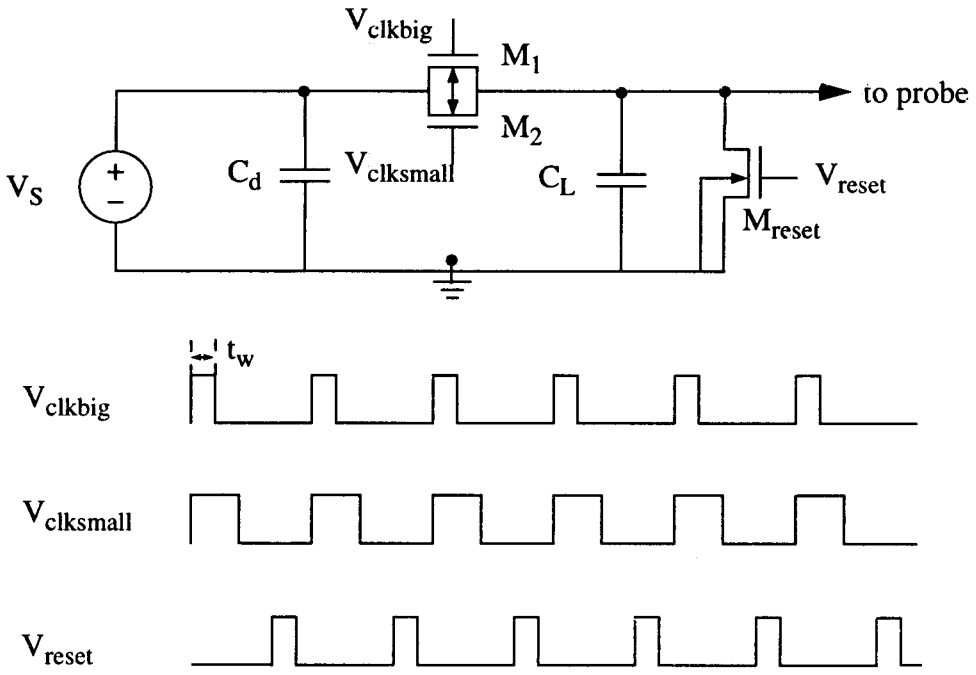


Figure 2.12:Test circuit with clock signals

discharging the load capacitor. Since the on drain-to-source resistance of ZDM4306N is typically 1 Ω, the discharging speed is very fast compared with the clock period. The two clock signals, V_{clkbig} and $V_{clksmall}$, are synchronized at the rising edge (Figure 2.12) and generated by a HFS 9030 precision pulse generator. V_{reset} is also synchronized with V_{clkbig} and generated by a HP8112A pulse generator.

The timing sequence is also shown in Figure 2.12. The input voltage is a 0.4 V DC signal from a Tektronix PS503A dual power supply. When V_{clkbig} and $V_{clksmall}$ are both high, the load capacitor is charged to the input signal. After both parallel transistors are switched off, the load capacitor is discharged by M_{reset}. The procedure repeats in every clock cycle.

The wide switch was obtained by combining several NTE465 MOSFETs in parallel. If these transistors are not too different from each other, the combined transistor could be regarded as one MOSFET with the size several times bigger than each one. The transconductance of each MOSFETs and on-state drain-to-source resistance were measured with a Tektronix 370 programmable curve tracer to show the validity of this assumption. The measurement results are shown in Table 2.3.

Table 2.3:Transconductance and conductance of MOSFETs

Device No.	1	2	3	4	5	6
g_m(mS)	1.4	1.6	1.5	1.5	1.7	1.5
g_{ds}(mS)	3.7	4.2	3.8	4.0	4.3	4.4
$r_{on}(\Omega)$	270	238	263	250	233	227

Here, g_m was measured for V_{ds} = 5 V and g_{ds} was measured for V_{gs} = 3.4 V. As shown in Table 2.3, the transconductances and conductances vary in the range of ±10 %. Therefore each transistor can be regarded as identical.

2.5.1 One Switch

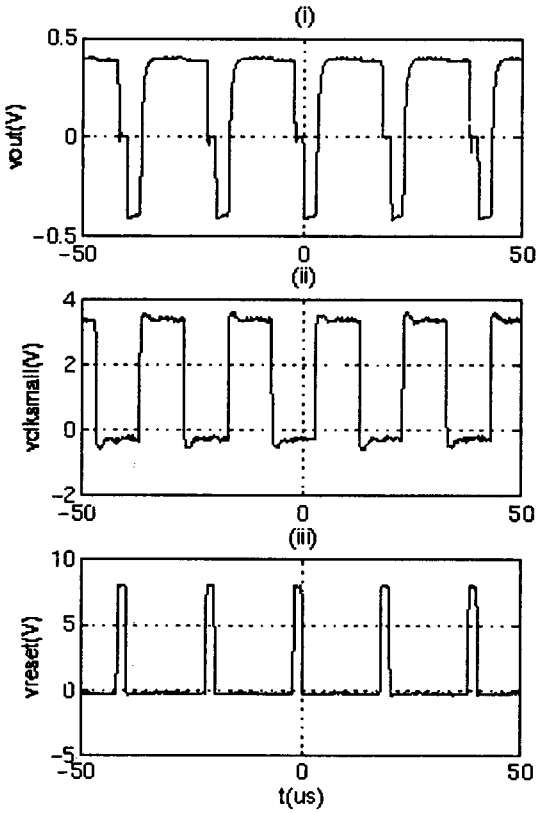
First, only one switch was used in the sample and hold circuit (Figure 2.1). Different number of MOSFETs were put in parallel. The input was a 0.4 V DC signal. Since r_{on} is around 250Ω, the RC time constant of this circuit is 0.3μs. Hence, the clock time-period is chosen 20μs, i.e., clock frequency is 50 kHz.The error voltage values are listed in Table 2.4. The measurement is made on a Tektronix TDS420A digital oscilloscope

Table 2.4:Error voltage in one switch scheme

No. of FETs	1	2	3	4	5
V_{error}(mV)	8.9	16.7	24.2	36.0	47.8
$t_{rise}(\mu s)^{(*)}$	2.42	1.23	0.81	0.64	0.50
(*): t_{rise} is the time period when the output voltage is charged from 0 V to 396 mV.					

(Figure 2.13). It shows that the error voltage increases as the number of MOSFETs in parallel increases, which agrees to what Eq. (2.10) indicates. The more charge is stored in the channel, the more ends up in the load capacitor if the signal source and load capacitance remain unchanged. Therefore, it could be concluded that if high accuracy is required and the sample-and-hold circuit as Figure 2.1 is used, the switch transistor should be as small as possible. Of course the transistor size is also limited by the sampling frequency so that RC time constant should be about 1/7 of the clock period [11].

According to Eq. (2.1), t_{rise} is proportional to the RC time constant when the initial and destination voltages are given. In the one-switch scheme, R is the drain-to-source on-resistance of the switch transistor and thus inversely proportional to the size of the transistor. Therefore in our case, t_{rise} is proportional to the number of the transistor. The test result agrees well with this statement.



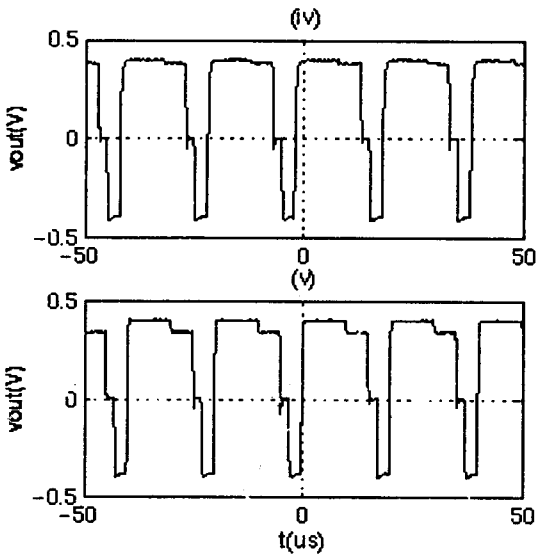


Figure 2.13:A typical measured output in one switch scheme.
(i)(iv)(v) the output voltage with different switch width (1/2/6);
(ii) gate voltage of the switch transistor
(iii) reset signal

2.5.2 Two Switches

The two transistor scheme was also tested as Figure 2.12 shows. The test parameters were the same as those used in Section 2.5.1. The pulse width of the clock signal for the wide switch, t_w, was tuned so that we could get different $percent_1$ values, which is the accuracy the sampled voltage can reach when the wide switch opens.

2.5.2.1 Error Voltage

If the accuracy in an application is the highest priority, the minimum transistor size has to be chosen. The wide transistor is used to speed up the settling.

Typical waveforms for the combination with different width of the wide transistors are shown in Figure 2.14. From the graph, we can see that the error voltages are almost the

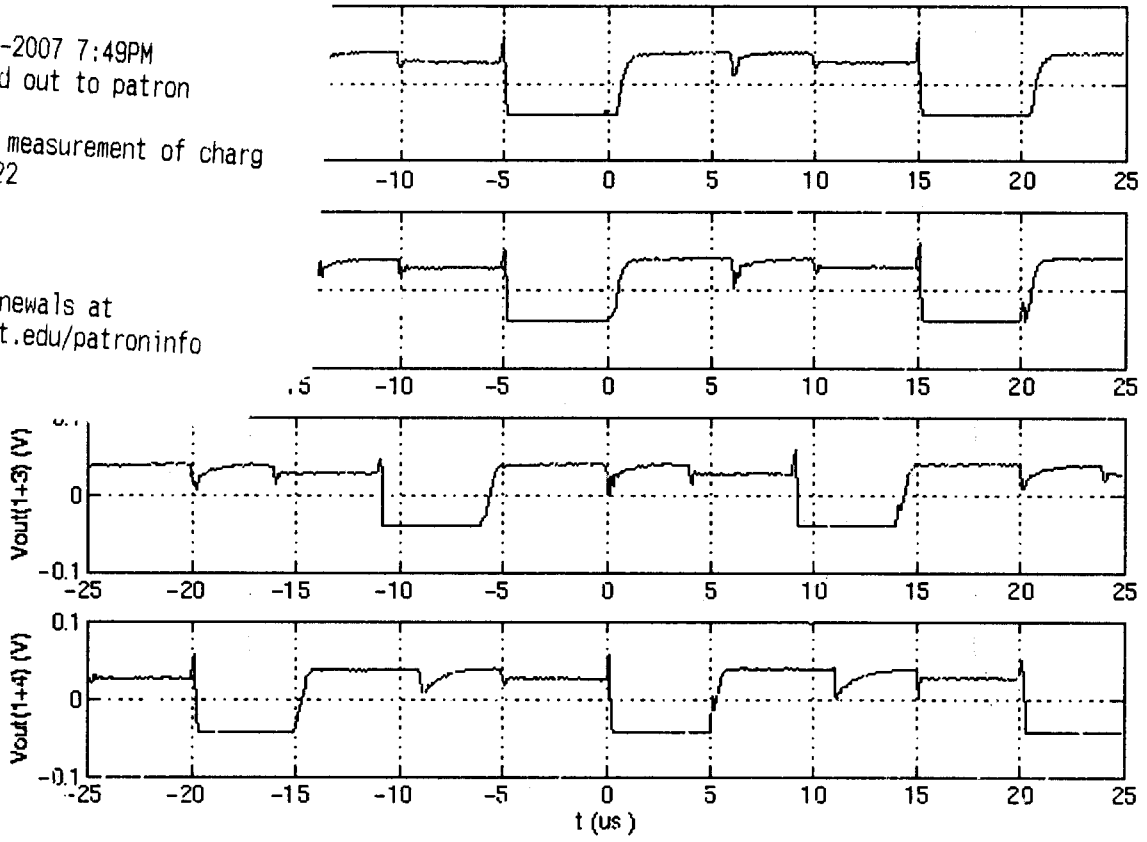


Figure 2.14:Typical waveforms for the two transistor scheme

same due to the same small switch while the charging speed is different due to the wide transistor. It indicates that the small switch transistor generates the small error voltage due to its charge injection while the RC constant is large. The wide transistor can charge faster; however, it causes a bigger error voltage. If these two transistors are in parallel, the two advantage are combined, the fast speed with small error voltage. This is what was expected.

Measurements were made to find the optimum instant when to open the wide transistor so that the time to reach a given accuracy(99.9%) is the shortest.

The test results are shown in Table 2.5. Figure 2.15 shows the measurement result for '1+1' in MATLAB. The curve does look like that one in Figure 2.7 (iii).

Table 2.5: Test result for the two switch scheme

1+1[1]	V_{error}(mV)	10.4				
	t_w (duty)	2%	3%	4%	5%	6%
	$percent_1$	*88%*	*92%*	*96%*	*98%*	*99.5%*
	t_{rise}[2](μs)	*2.01*	*1.85*	*1.74*	*1.71*	*1.80*
1+2	V_{error}(mV)	10.4				
	t_w (duty)	2%	3%	4%	5%	6%
	$percent_1$	85%	93%	95%	99.5%	>99.9%
	t_{rise}(μs)	2.0	1.73	1.61	**1.47**	1.74
1+3	V_{error}(mV)	10.2				
	t_w (duty)	2%	3%	4%	5%	6%
	$percent_1$	93%	98%	99.2%	>99.9%	>99.9%
	t_{rise}(μs)	2.12	2.0	1.80	1.98	2.05
1+4	V_{error}(mV)	10.2				
	t_w (duty)	2%	3%	4%	5%	6%
	$percent_1$	93%	99.0%	>99.9%	>99.9%	>99.9%
	t_{rise}(μs)	2.16	2.04	1.97	2.04	2.08

Note:
(1) 1+1 denotes that the narrow switch consists of 1 MOSFETs and the wide one consists of 1;
(2) t_{rise} is the time period when the output voltage is charged from 0 V to 396 mV.

From these results, we can draw the following conclusions:

i) The error voltage is determined by the small switch transistor since the error voltage stays unchanged when the different size of wide transistor is applied;

ii) It will decrease the charge-up time if the wide switch is opened just after the output voltage is approaching the saturation level (input signal). Too long pulse

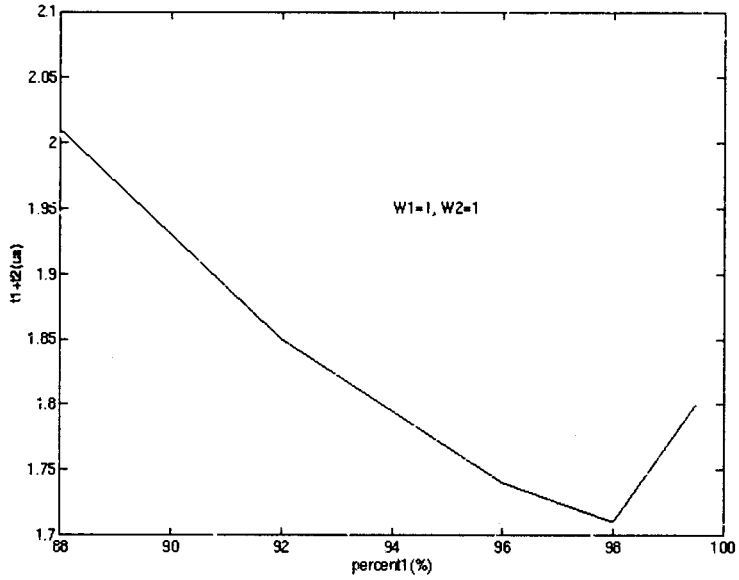


Figure 2.15:The time period which the output takes to reach 99.9% accuracy for '1+1' test circuit.

width of the clock signal for the wide switch does not improve the speed performance. We can see that t_{rise} changes little after $percent_1$ is larger than 99.9%.

iii) Comparing all the t_{rise} values in Table 2.5, the minimum charge-up time is found when the wide transistor is twice as large as the small one and $percent_1$ is 99.5%. The result agrees with the analysis in Section 2.4.2. The optimum is achieved when the large transistor is several times wider than the small. The statement that "the wider are the transistors in parallel, the faster the circuit is", is incorrect.

2.5.2.2 Clock Frequency

In some application the clock frequency is fixed and too fast for the minimum transistor to settle to the given accuracy within the clock period. If a wider transistor is used, however, it will cause a big error voltage, just as shown in Figure 2.16. The measurement shows that the error voltages for one switch transistor with 1, 3 and 6 MOSFETs in parallel are 68 mV, 22 mV, 52 mV respectively.

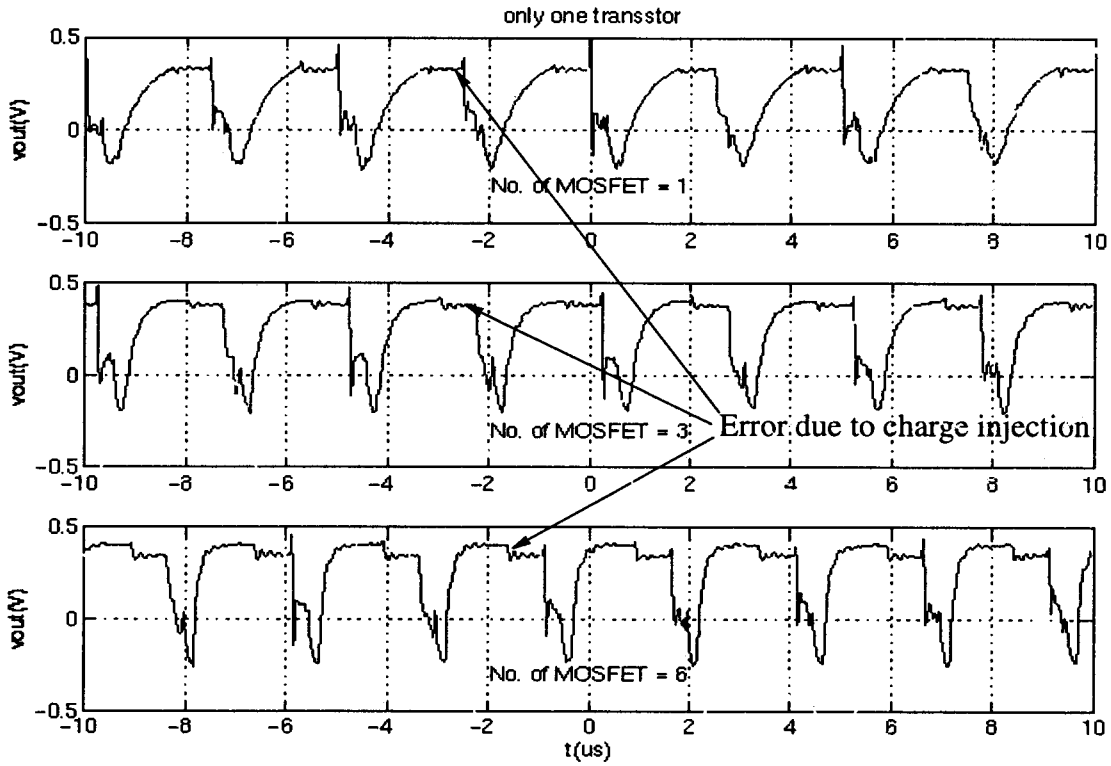


Figure 2.16:Error voltage with one switch transistor (f_s=400 KHz)

Therefore, an additional transistor in parallel is used to help faster settling. Table 2.6 shows the error voltages for different sizes of the wide transistor working at a sampling frequency 400 KHz. As expected, the optimum combination of the two transistor is '1+3'. The reason we think '1+3' is better than '1+2' although their minimum level is the same is that the error voltage is low within a wider range.The measurement shown in Figure 2.17 indicates that although a wider transistor could make the circuit settle faster in the first period of time, it does generate too big voltage drop due to the charge injection, which makes the conducting small transistor not be able to settle to a high enough accuracy. It should be mentioned that the error voltage is of the same order as when only the wide transistor is used. That is what we suggested in Section 2.3.1, where Figure 2.5 compared the performances of the two switch scheme and only one wide switch. The two switch scheme is not supposed to make much improvement when the clock frequency is too high.

Table 2.6:Error voltages for fs=400 kHz

V_{error}(mV)		two transistors					
		1+1	1+2	1+3	1+4	1+5	1+6
duty cycle	5%	64	58	36	32	46	44
	10%	56	44	36	24	30	28
	15%	48	34	28	24	26	28
	20%	42	28	22	24	26	28
	25%	38	24	22	24	26	32
	30%	32	22	20	24	32	36
	35%	30	22	22	28	36	42
	40%	28	20	24	30	40	52
	45%	28	20	24	30	40	52
minimum V_{error}		28	20	20	24	26	28

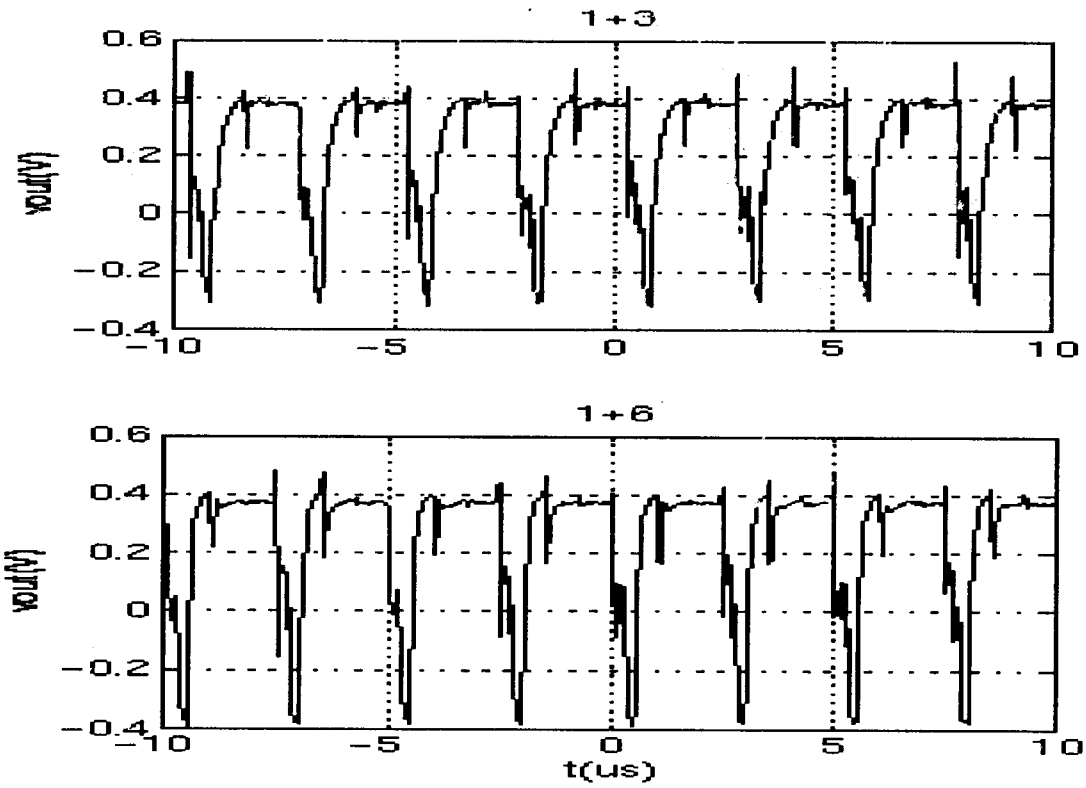


Figure 2.17:Error voltages for two switch transistors

2.6 Summary

It has been verified by theoretical analysis, circuit simulation and experiments that two switch transistors in parallel in a sample and hold circuit shown in Figure 2.1 can be expected to achieve high speed with low error voltage. The wide transistor provides low RC constant when it is closed and the narrow one ensures a low error voltage. However, trade-offs can be made in a specific application. The simplified model proposed in this section can help the designer to make the optimum decision. Experimentally the optimum size of the wide transistor is several times bigger than the narrow one.

Chapter 3. Charge Injection in a SC Integrator

The previous chapter dealt with the analysis and measurement of charge injection in a simple sample and hold circuit. This chapter describes the analysis and simulation of the charge injection of the switches in a stray-insensitive integrator circuit.

3.1 Introduction

An integrator is a key block in analog integrated circuits, especially in switched-

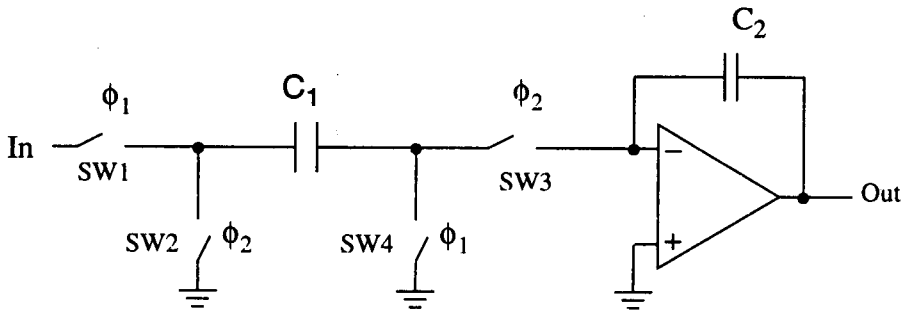


Figure 3.1: A non-inverting stray-insensitive integrator

capacitor filters and delta-sigma modulators. It is critical to build an integrator as ideal as possible. A switched-capacitor stray-insensitive integrator contains an operational amplifier, an integrating capacitor C_2, an input capacitor C1 and four switches with two non-overlapping phases ϕ_1 and ϕ_2 as shown in Figure 3.1. There are several error sources in this structure. The opamp's finite gain, finite bandwidth and dc offset can reduce the integrator's performance. Therefore, some circuit techniques, such as correlated double sampling (CDS) and gain-offset-compensation (GOC), were proposed to solve these problems. Another error source is non-ideal switches. Normally MOSFETs working in their linear region are used as switches. When the overdrive voltage is larger than zero, a MOSFET switch can be regarded as a resistor (typically 100Ω - $1k\Omega$), otherwise the branch is cut off. It is generally recognized that parasitic capacitances are present associated with

the desired circuit element and due to the low values of capacitors permitted on an integrated circuits, these parasitic capacitances cause unacceptable deviations. All overlap

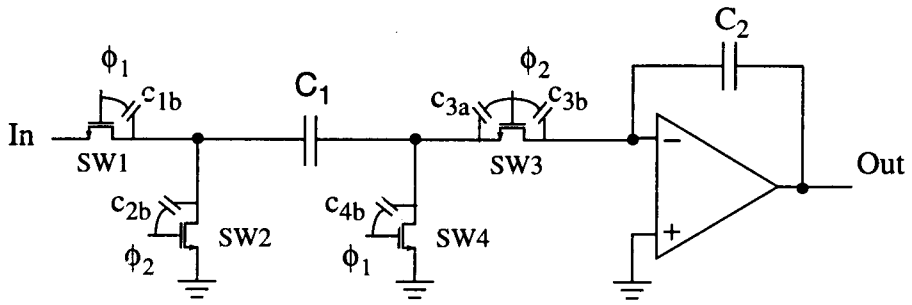


Figure 3.2: Parasitic capacitance in the integrator

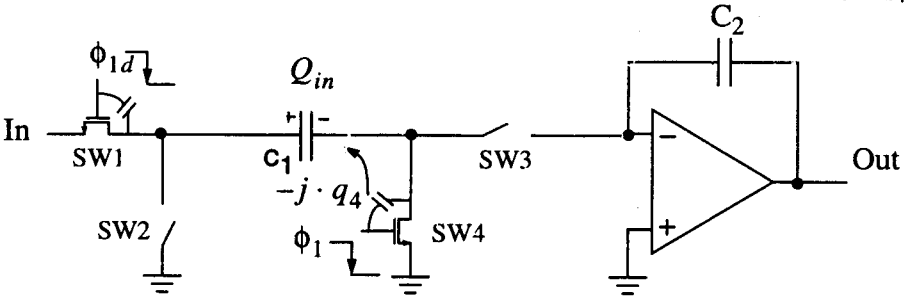
capacitances are shown in Figure 3.2 except those which are connected to only ground or signal source.

There are two kinds of capacitances associated with MOSFETs. One is the overlap capacitance, which is generated by the overlapping area between the gate and the source/ drain diffusion area. The other is the gate-channel capacitance. When the gate voltage is dropping, the charge in the these capacitors is moving away. If the fall time of the gate voltage is very small, the amount of charges in the channel moving to the drain and source can be regarded as the same [2]. To a first order approximation, when the overdrive voltage is less than zero, the channel is cut off completely and there is no charge flowing through the channel. The remaining charges in C_{3b} have to flow into the feedback capacitor.

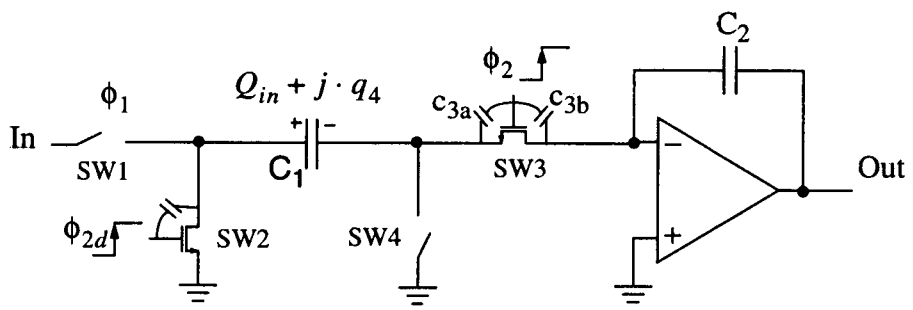
3.2 Charge Transition in the Integrator

Now we analyze the operation of each switch one by one. When ϕ_1 is high, C_1 is charged to the input voltage. Meanwhile, charge is stored in the channels of SW1 and SW4 and the overlap capacitors C_{1b} and C_{4b}. It is important to note that the charge related to SW1 is signal dependent while that of SW4 is signal-independent. When ϕ_1 goes low, all

of these charges will be transferred to C_1, or to the signal source or to ground. When the overdrive voltage of SW1 and SW4 is below zero, the switches are completely open, and part of charge in the channels of SW1 and SW4 will be stored on the input capacitor C_1. Ideally, if the amounts of charges transferred to each side of C1 are equal, they must be zero, and the charge transfer described above does not introduce error. Unfortunately, the charge transfer at the side of signal source is signal-dependent and at the other side it is signal-independent (because voltage levels of the gate, source and drain of SW4 are fixed). Therefore the cancellation could not be achieved in reality and an extra charge (positive or negative) is stored on C_1.But a delayed clocking scheme [3] can be used to eliminate the signal-dependent error related to SW1. The clock signals applied to the gates of SW1 and SW4 are then ϕ_1 and ϕ_{1d} (Figure 3.3), which means that the clock signal applied to SW1 is a delayed version of that of SW4. The key point is that SW4 is opened earlier than SW1. When SW4 is opened, part of the channel charge and overlapping charge, $-j \cdot q_4$, will enter



(i) When ϕ_1 falls earlier than ϕ_{1d}

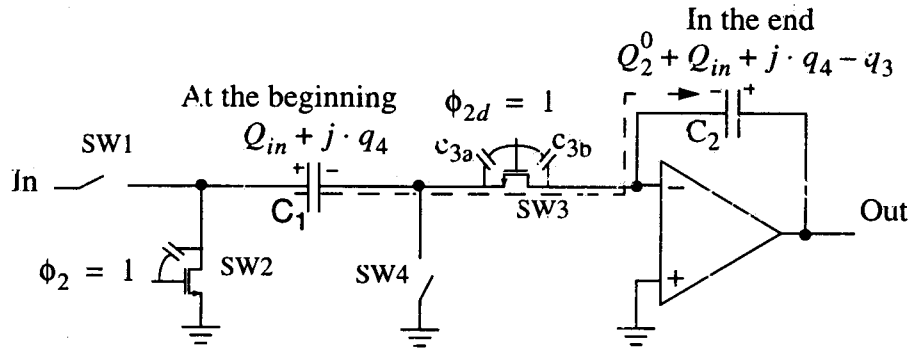


(ii) Just before ϕ_{2d} and ϕ_2 goes high.

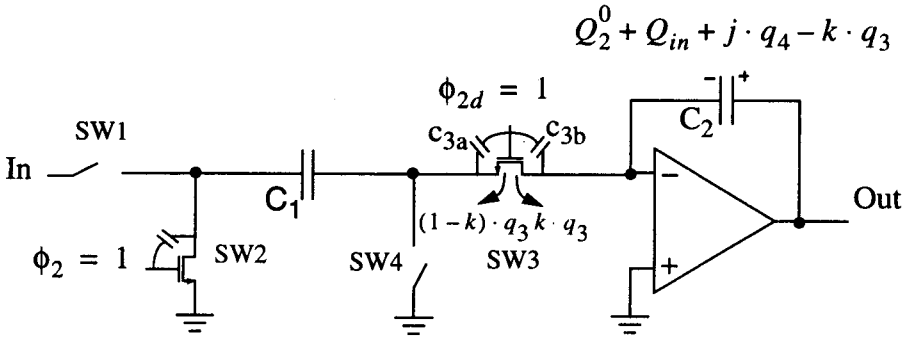
Figure 3.3: Sample period of the non-inverting integrator

the input capacitor C_1 (Figure 3.3, i), which will cause an error. Here, q_4 stands for the charge trapped in the switch when SW4 is on and j is the fraction of q_4 injected into the input capacitor C_1. The amount of charge injection is not a function of the signal because the gate-to-source voltage is fixed. So the error source can be regarded as a dc offset and cancelled by a fully differential configuration. A little later, SW1 will be opened, and since the other terminal of C_1 is open-circuited (SW3 and SW4 are both open), all the charge in the parasitic capacitors will flow back to the signal source. Therefore, the charge on C_1 remains unchanged, $Q_{in} + j \cdot q_4$, where $Q_{in} = C_1 V_{in}$ as illustrated in Figure 3.3 (ii).

After SW1 and SW4 are completely cut off, SW2 and SW3 will be closed. The



(i) charge transition when sw2 and sw3 are closed



(ii) When sw3 is opened.

Figure 3.4: Integrating period of the non-inverting integrator
Note: The amount in parenthesis is the stable value after switch operation

rising edges of the clock signals applied to them do not need to be synchronized. After they

are both high, the charge on the input capacitor C_1 begins to flow into the integrating capacitor C_2. However, some charge, q_3, is trapped in the channel of SW3 and its parasitic capacitors C_{3a} and C_{3b}. Hence, when the charge transition ends, the charge on C_2 is $Q_2^0 + Q_{in} + j \cdot q_4 - q_3$ (see Figure 3.4, i), and the output voltage is $(Q_2^0 + Q_{in} + j \cdot q_4 - q_3)/C_2$ instead of $(Q_2^0 + V_{in} \cdot C_1)/C_2$, where Q_2^0 is the charge stored earlier in C_2. Then the gate voltage of SW2 and SW3 goes low, and a fraction of the charge in the SW3 channel and its parasitic capacitors, $k \cdot q_3$, will be injected to C_2, where $0<k<1$. How big k is or what the distribution of injected charge related to q_3 looks like depends on the clock waveform, and the impedance seen looking towards the input capacitor C_1 and towards the opamp. This situation is as discussed in [5]. Also, if the gate voltage of SW2 falls earlier than that of SW3, the charge injection associated with SW2 will increase the output voltage by coupling into C_1 and C_2. So the clock signal of SW2, ϕ_{2d}, has to be a delayed version of that of SW3, ϕ_2, so that another error source, the injected charge from SW2, could be removed.

Thus, when the next stage is sampling the output, the value of the integrator output is $(Q_2^0 + Q_{in} + j \cdot q_4 - k \cdot q_3)/C_2$, where $j \cdot q_4$ and $k \cdot q_3$ are the charges injected from the channel and overlapping capacitances of SW4 and SW3. As we can see, the two error sources can be made to cancel each other if the delayed clock scheme is used. They are time-invariant and signal-independent and hence will not cause harmonic distortion.

Simulations (Figure 3.5) show that the charge injection related to SW1 and SW2 does not cause output error if the delayed clock scheme is used. In the simulation, a dc input of 0.1 V is applied to a non-inverting integrator shown in Figure 3.1, with $C_1 = C_2 = 1$ pF and sampling frequency is 5 MHz. Each curve stands for a pair of SW1 and SW2 with different widths (the channel length of all the devices is 0.9 μm). $Q_2^0 = 0$ was assumed. SW3 and SW4 are assumed ideal.

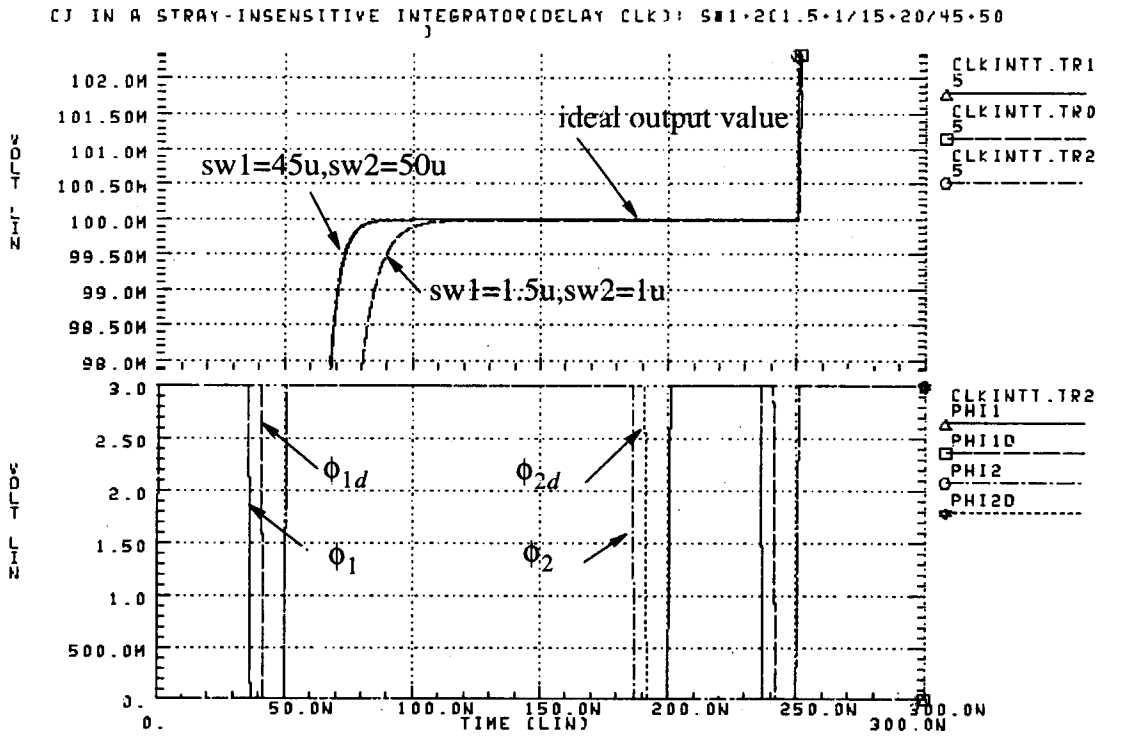


Figure 3.5: Charge injection of SW1 and SW2
(above) output signal; (below) clock signal

According to the analysis above, the charge injection related to SW3 and SW4 is signal-independent. Therefore, after the two capacitors are chosen, it is possible to find a pair of transistors which will contribute the same amount of charges to the integrating capacitor with opposite signs. Thus, they are cancelled in the first order. Figure 3.6 shows that a pair of transistors (SW4=1.2u/0.9u, SW3=0.9u/0.9u) can be found for cancellation in a specific fabrication process, HP 0.6um CMOS technology. Before SW3 is opened, the output voltage will be stabilized at $(Q_{in} + j \cdot q_4 - q_3)/C_2$. If we want the output voltage during the holding period to be accurate as with ideal switches, $j \cdot q_4$ should be equal to $k \cdot q_3$. Since the charge stored in the channel of SW4 is more likely to flow back to ground, j tends to be a little less than k. Hence, the size of SW4 should be a little larger than SW3. Just before SW3 opens, the output level, $(Q_{in} + j \cdot q_4 - q_3)/C_2$, is a little below the ideal voltage. When SW3 cuts off, a fraction of q3 will flow back to the input capacitor and the other part will disperse to the output and it generates a voltage jump. Now in the holding phase, the output voltage could turn out to be accurate due to the charge injection.

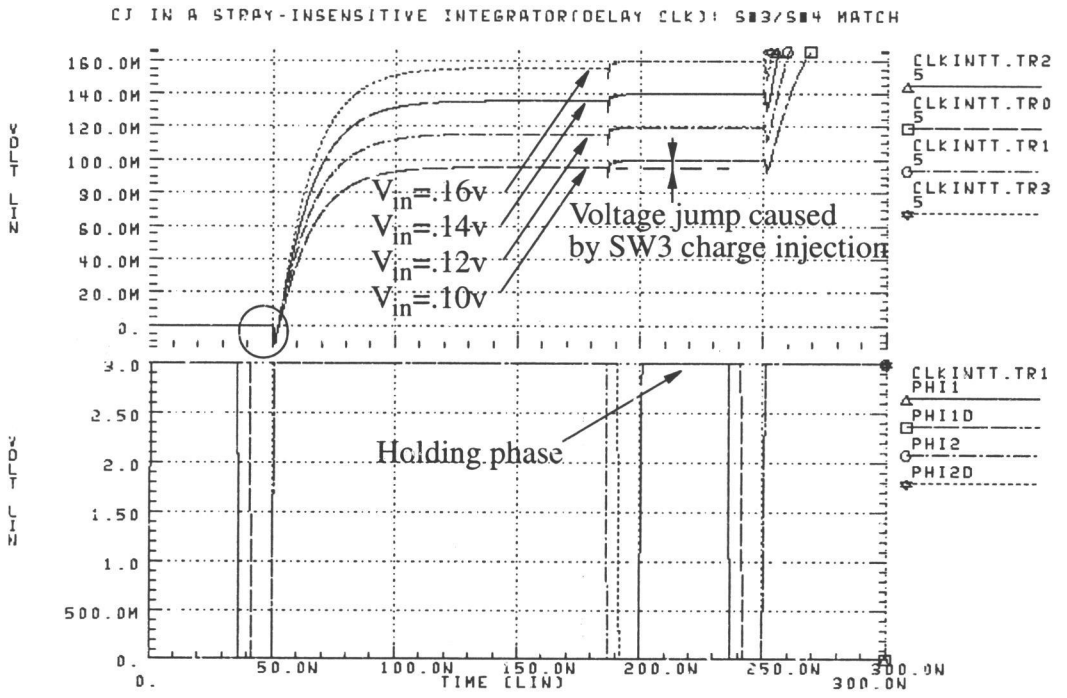


Figure 3.6: Match of SW3 and SW4
(above) output signal, (below) clock signal

It may be noticed that output voltage drops at first when ϕ_2 and ϕ_{2d} go high, i.e., SW1 and SW3 close, and then goes up, as indicated in the circle in Figure 3.6. Our explanation is as following: when SW1 and SW3 change from open to closed state, the voltage across the input capacitor can change instantly. And at this point, the opamp is not fast enough to respond to this change, therefore, the voltage jump in the left side of the input capacitor will be coupled directly to the output via C_1 and C_2.

3.3 Two Switch Scheme in the Stray-Insensitive Integrator

As discussed in Section 3.2, it is possible to find a matched transistor SW4 to cancel the charge injection of SW3. To make the error minimum, normally a minimum size transistor is chosen as SW3. However, this will cause the problem in some high-speed applications. For example, a delta-sigma modulator needs an integrator with short settling

time. A small-size switch transistor usually cannot provide the necessary small RC constant. Therefore, the technique discussed in Chapter 2 may be used here.

In order to prevent a big on-resistance of SW3 from reducing speed, a wide switch, SW3a, can be put in parallel with SW3 as indicated in Figure 3.7. The clock signal applied

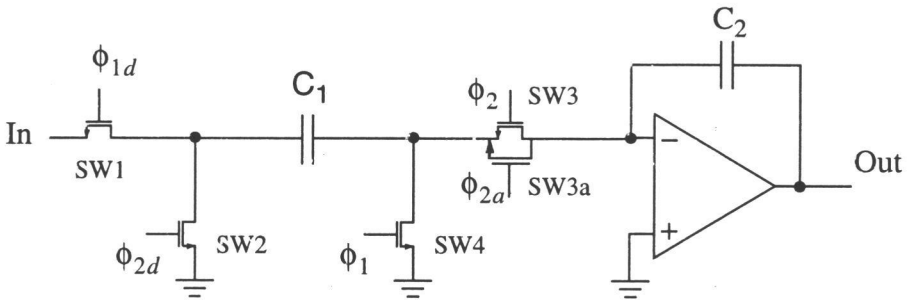


Figure 3.7: Two parallel switch transistor in the integrator

to this transistor is ϕ_{2a}, which goes high at the same time as ϕ_2 and falls to the low level earlier than ϕ_2. The idea is that when both transistors are working in the triode region, the impedance of the switch is low, which makes the settling of the output faster than that when there is only SW3. When SW3a opens, there is no charge injection effect since all the charge in the channel of SW3a will flow to the output capacitor C_2. These charges form part of the input signal because they were trapped in the channel during the charge transition from C_1 to C_2 when SW2 and SW3 were closed. The simulation results shown in Figure 3.8 show that the two-switch structure does speed up the charging up time. The same input voltage as in Figure 3.5, a dc signal of 0.1 V, was assumed.

As shown in Figure 3.8, before the switch SW3 opens, the output signal will saturate at a voltage level far below the ideal value if only the wide transistor is used as the switch SW3. Our explanation is as follows: when the sample phase ends, the input signal is stored on C_1 resulting in a charge, $V_{in} \cdot C_1 + j \cdot q_4$, assuming the delayed clock is used. When the holding phase begins, the charge will be transferred from C_1 to C_2. Some charge

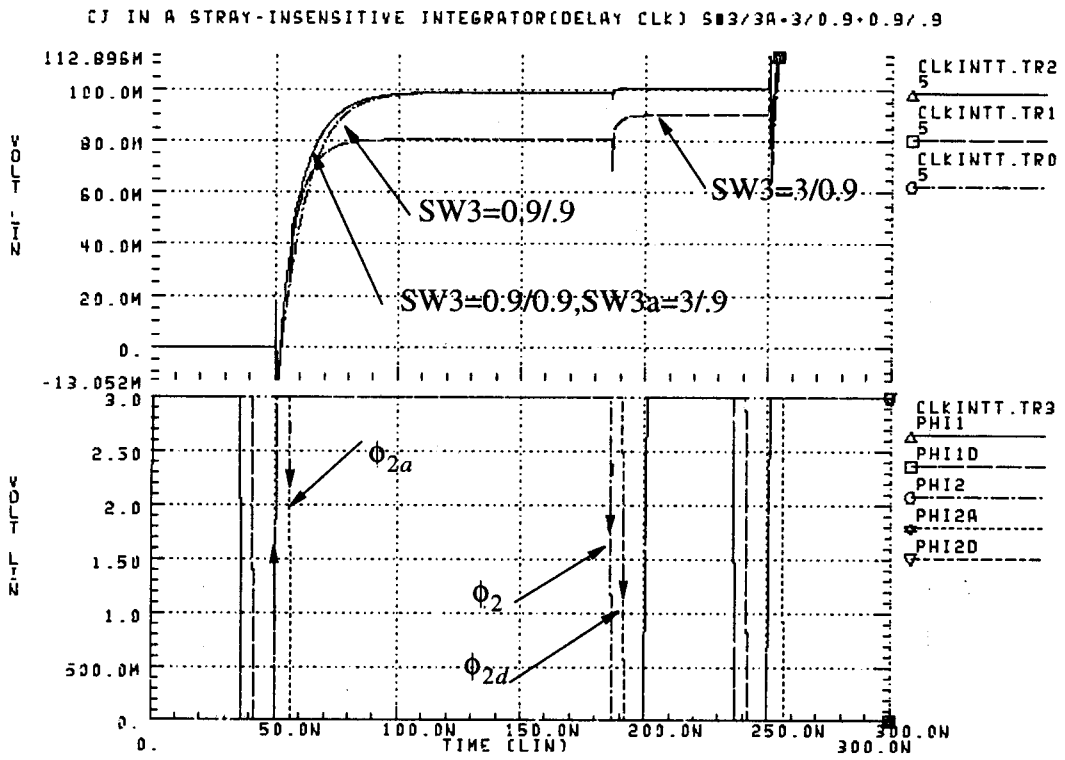


Figure 3.8: Simulation result of Figure 3.7
(above) output signal, (below) clock signal

will be trapped in the channel of SW3 as previously explained. If the amount is more than $j \cdot q_4$, the maximum output signal voltage will be less than the ideal value. When the switch is opened, part of trapped charge will be injected into the feedback capacitor. Some of charge which contains input signal will be injected into the input capacitor. Since k is constant for a given circuit, the wider the width of transistor SW3 is, the more of the input signal charge is lost. Figure 3.9 shows what happens when SW3 is wide, for $V_{in} = 0.1$ V.

This situation also happens for the two-switch scheme when both transistors SW3 and SW3a are on. The two switches can be regarded as one with the total width of the two. If the wide switch leaves a large voltage gap for the small one to settle, the circuit will be worse in speed rather than better. As shown in Figure 3.10, the two-switch scheme does not help the circuit. Although a wide switch has a smaller RC constant, the circuit speed is still

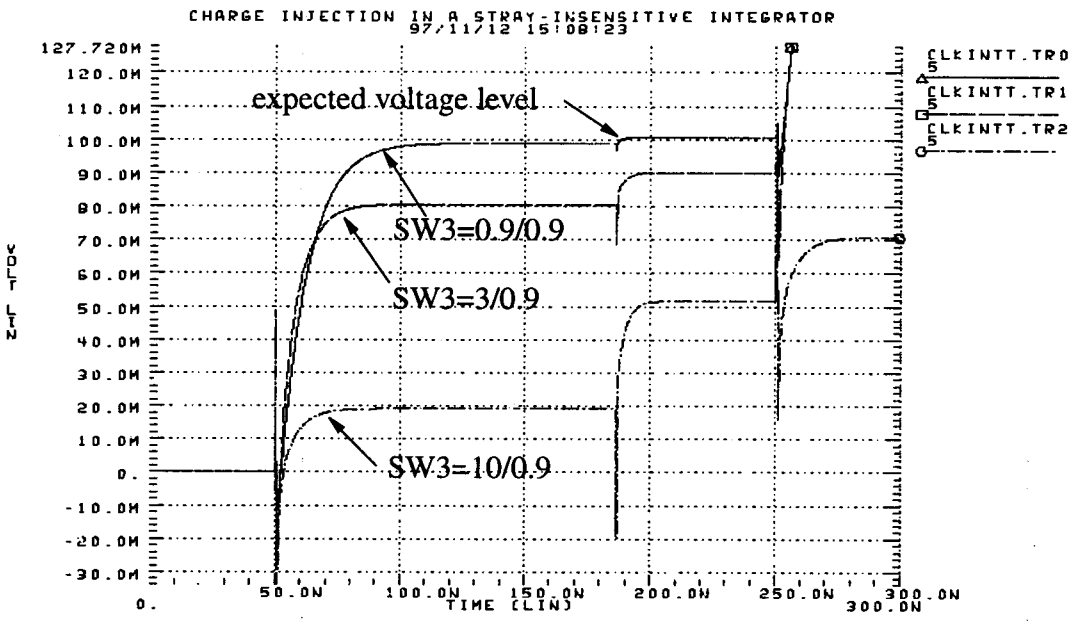


Figure 3.9: The problem caused by too wide SW3 with SW4=1.2/0.9

low since the output saturates at a much lower level. The voltage difference left for settling by the small switch is even larger.

Therefore, a not too wide transistor should be used to help the small transistor to

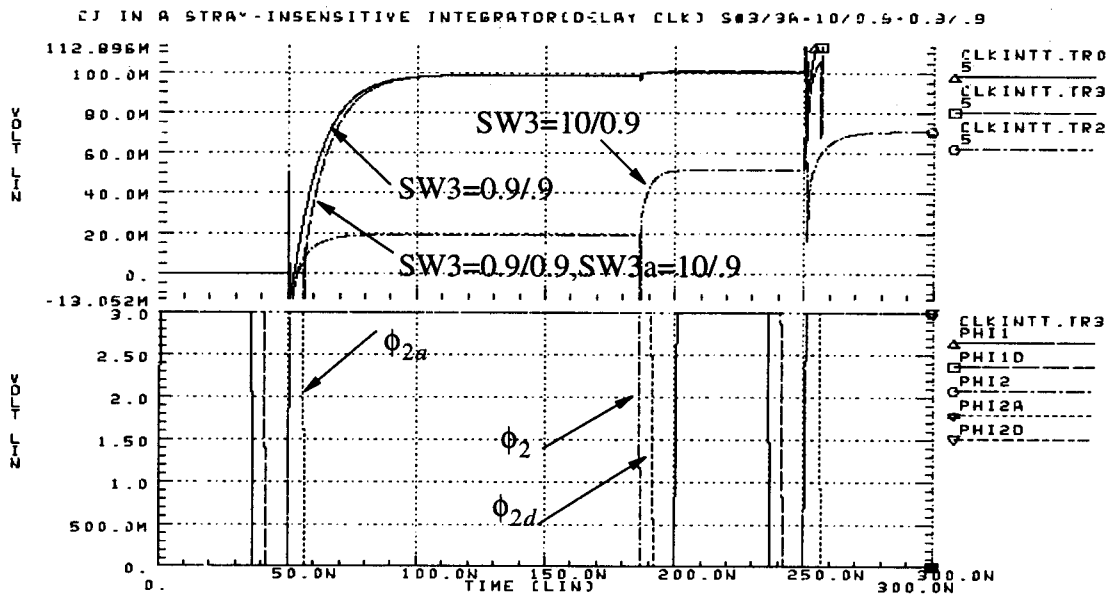


Figure 3.10: The same problem for the two switch scheme
(above) output signal; (below) clock signal

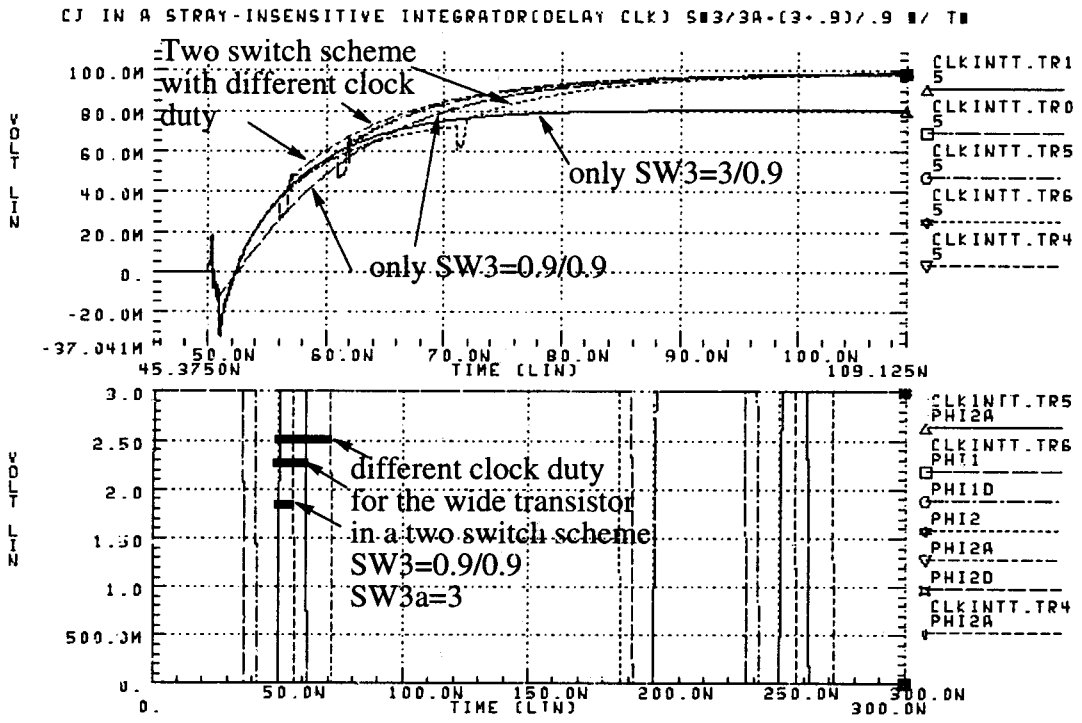


Figure 3.11:Choice of the clock duty cycles for the wide transistor in two switch scheme (above) output signal, (below) clock signal

settle at the beginning of the sample phase, and the wide transistor should be opened before V_{out} saturates. As shown in Figure 3.11, there are three curves corresponding to different clock duty cycles for the wide transistor in the two switch scheme. The first two does help to speed up settling, however, the third one shows that the wide transistor opens too late because it has begun to saturate.

3.4 Summary

Delayed clock scheme can be used to make charge injection signal-independent in a basic integrator structure. Using two transistors with different sizes and clock duty cycles in parallel can take advantage of fast speed from the wide transistor and a small error charge injection from the small transistor. However, the combination of the two devices, including the size and clock duty cycles, should be chosen carefully to achieve the improvement.

Chapter 4. Summary and Future Work

4.1 Summary

In this thesis, a method is described and analyzed for reducing the charge injection error in a switched-capacitor circuit while increasing the operation frequency. pIt has a wider transistor in parallel with a minimum-size switch transistor; the wide transistor helps fast settling and the minimum-size transistor reduces charge injection. This idea is applied to a simple sample-and-hold circuit and a basic integrator circuit. A simplified lumped model was constructed for the sample-and-hold circuit to find the optimum combination of these two transistors.

A simple sample-and-hold circuit was built on a PCB board using discrete devices. The test results agreed well to what the simulation predicts. To achieve optimum performance, the width of the large transistor must be several times wider than that of the other switch transistor. Speed can be increased by 40%-80% compared to only using a minimum-size switch transistor.

The two switch transistors in parallel can also be used in a non-inverting integrator circuit with the delayed clock scheme. However, the sizes and the clock duty-cycles should be chosen carefully for achieving the better performance.

4.2 Future Work

Nonlinearity is another important issue in switched-capacitor circuits. Transmission gates can be used to increase the input range and improve the linearity of the circuits. The circuit performance using transmission gates in parallel can be investigated using the lumped model.

Since the performance of the circuit which the thesis introduces and analyzes is still not optimum, other circuit structures should be searched for to reduce charge injection in high-speed high-performance applications.

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