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Title: Feedback Design for Sampled Analog Phase and Gain Detection in MDFE

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John G. Kenney

Multi-level decision feedback (MDFE) is a sampled analog system for disk data recovery. Correct sampling and gain of the equalized signal is essential for achieving low bit error rates. The timing information is recovered from the received signal. The clock is acquired by reading a known initial sequence. Perturbations in the magnetic recording channel are being tracked during random data operation. Automatic control of the equalizer gain is also required. In this thesis, a phase-locked loop for the timing recovery and automatic gain control customized for MDFE will be presented. An analog hardware implementation is proposed for the involved phase and gain detection.

A description of the run-length limited coding used for facilitating timing recovery and automatic gain control is given as basis for symbol patterns and signal levels in MDFE. Decision-directed phase and gain detection schemes are developed as simplified approximations of a minimum-mean square error gradient algorithm. The dynamic behavior of the joint operation of the phase-locked loop and automated gain control is studied in computer simulations. Filters providing phase-lag

The dynamic behavior of the joint operation of the phase-locked loop and automated gain control is studied in computer simulations. Filters providing phase-lag compensation are incorporated in the phase-locked loop to optimize the trade-off between settling time and clock jitter. Finally, low-power-consuming sampled analog circuitry is presented for the detection of phase and gain in switched-current mode.

The resulting phase-locked loop and automatic gain control exhibit fast transient behavior and zero steady-state errors The fully-differential hardware implementation in CMOS technology is capable of fast operation in low-voltage-domain and provides charge-injection cancellation to a first order.

Feedback Design for Sampled Analog Phase and Gain Detection in MDFE

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Volker Schmid, Author

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1. INTRODUCTION

Multi-level decision feedback equalization (MDFE) was developed by J.G. Kenney, L.R. Carley and R. Wood [1]. It is a sampled analog signal processing scheme for the recovery of data from hard disk drives. The data is stored by alternating the polarity of the magnetic flux on a track. The playback head senses changes in the flux polarity and outputs a pulse based upon a transition. For correct detection of the symbols by MDFE, the sampling of the signal and the clocking of the sampled analog components in the system are essentially dependent on the timing intervals of the readback signal. The recovery of this timing information by a phase-locked loop is a crucial issue for the functionality of MDFE. In this thesis, simple functions for determining timing information will be examined. Another essential building block within MDFE is the automatic gain control. Detection of the signal gain and adjustment is required for obtaining distinct signal levels. This necessity emerges from the principles of digital communication systems which require specific signal levels for correct operation.

Decision feedback is one of the basic concepts for symbol detection within a magnetic recording system. As the upcoming information age has created an enormous demand for the storage of digital data, the density stored in a single system needs to be increased to meet these demands. Besides technological issues like the design of the magnetic head and suitable disk media, the storage density

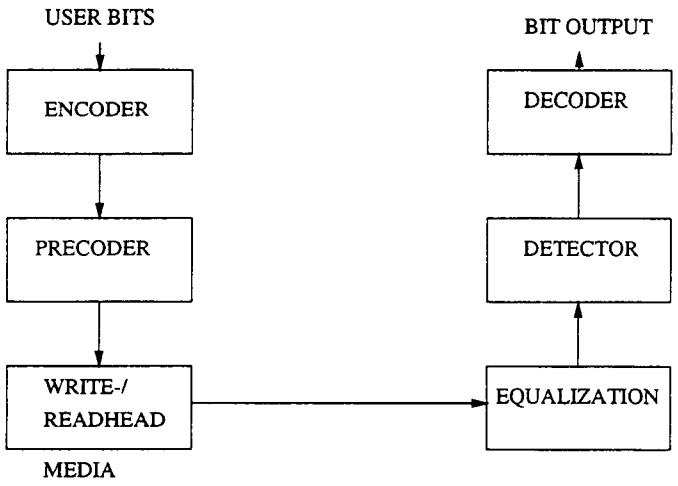


Figure 1.1. System for magnetic recording

is highly related to the signal processing techniques available for the problem of data recovery. The general similarity of the disk read and write processes to data-detection and transmission in communication systems has spawned considerable interest in applying coding and equalization methods for magnetic recording and developing similar signal processing schemes.

The entire system for magnetic recording described in general is shown in figure *1.1* and consists of six main parts: (1) Data encoding (2) symbol generation by the precoder (3) the magnetic recording channel (4) equalization and shaping of the received signal (5) symbol detection device and finally (6) data decoding.

One of the first and widely used concepts is peak detection [2]. As shown in figure *1.2*, the write head changes the polarity of the flux on the disk when an encoded data value of 1 is to be stored. Consequently the detection method retrieves these peaks of the readback current. An implementation is shown in figure *1.3*. Transitions are detected via computation of the derivative of the readback signal and checked on zero crossings. A clock is necessary for enabling this checking, which has to be retrieved from the readback signal. To improve the perfomance,

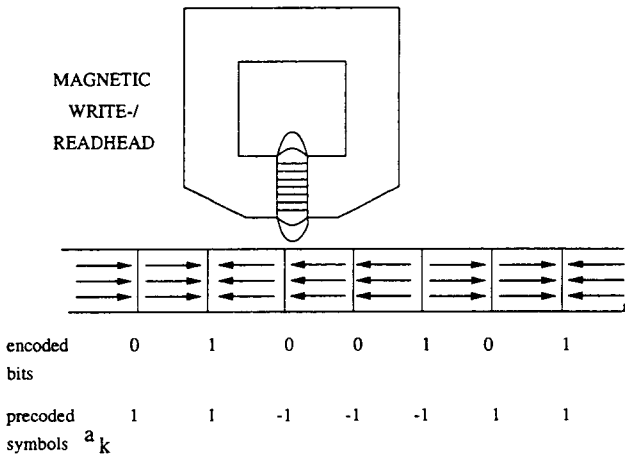


Figure 1.2. Reading and Writing process - Magnetic Head

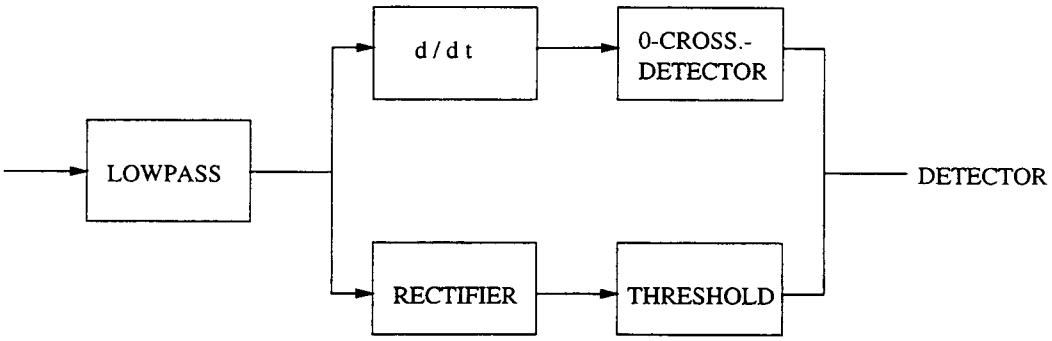


Figure 1.3. Peak detection system

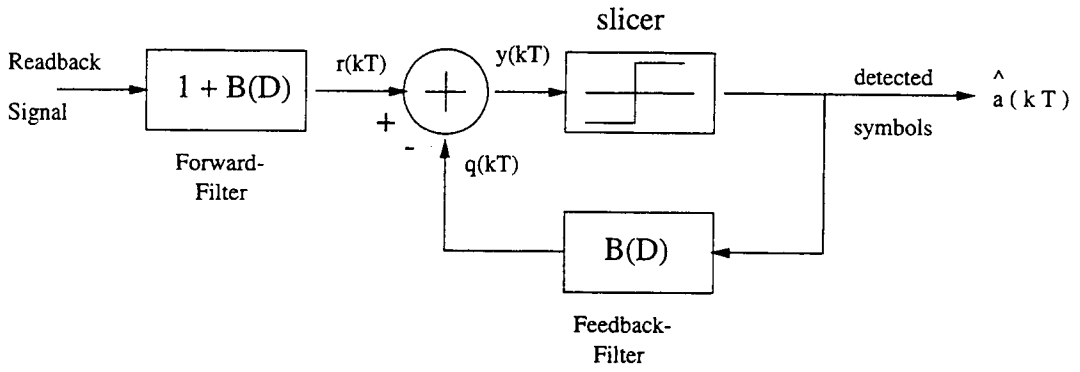


Figure 1.4. Decision Feedback system

a minimum number d of sample clock cycles between transitions is used. This contributes to a reduction of linear Intersymbol Interference (ISI) in the readback channel and nonlinear ISI during the writing process. Peak detection has inherent deficiencies, when the density of the stored symbols is increased and the minimum run length limitation d no longer sufficiently separates transitions. Peak shifts or missing peak errors may result from the ISI.

A more advanced concept to cope with ISI is called Decision Feedback Equalization (DFE), which is explained in [4]. DFE cancels post-cursor ISI by convolving previously detected symbols with the estimated impulse response of the caused ISI. A block diagram is displayed in figure *1.4*. The forward path consists of a matched filter which matches the step response of the magnetic recording channel. The readback signal is equalized to minimum phase yielding causal intersymbol interference. The causal intersymbol interference is introduced by previous symbols. A cancellation of this ISI can be achieved by subtracting the output of a feedback filter from the signal at the end of the forward equalizer. The feedback filter uses the already

detected symbols for shaping the corresponding cancellation signal. The complexity of this filter increases linearly with the impulse-response length of the allowed ISI. Detection of the symbols is performed by a single threshold slicer which is an advantage over systems implementing complex detection algorithms. The cancellation of ISI is very effective and achieved with limited complexity of the equalization filters. Complexity impacts power consumption of the system and required chip area. Both are important factors for a practical design.

The bit error rate can be improved significantly if the detection scheme implements knowledge of the symbol coding. A highly recognized detection algorithm is referred to Viterbi detection and is described in [3]. Viterbi detection is based on maximum likelihood schemes comparing the possible symbol paths (trellis) back until the paths converge. The depth of this search may vary depending on the symbol sequence and requires a large number of additions.

A simplification of this algorithm proposed by Moon et al. [5] is called Fixed Delay Tree Search with Decision Feedback (FDTS/DF). The block structure is shown in figure *1.5*. It merges the concept of DFE combined with a simplified maximum likelihood detector implemented as a linear comparator stage in combination with a single threshold slicer. While the depth of the tree search is limited to two symbols, there remains considerable complexity in the linear comparator stage, as several multiplications and additions have to be carried out which demands considerable effort for a fast realization.

Multi-level Decision Feedback Equalization (MDFE) is a more recent development which performs within 2dB of the matched filter-bound for channels using the 2/3(1,7) run length limited code. Its power has been demonstrated in several publications [5] [1]. The concept of MDFE is based upon FDTS/DF with a considerably simpler detector than FDTS/DF while it achieves exactly the same perfor-

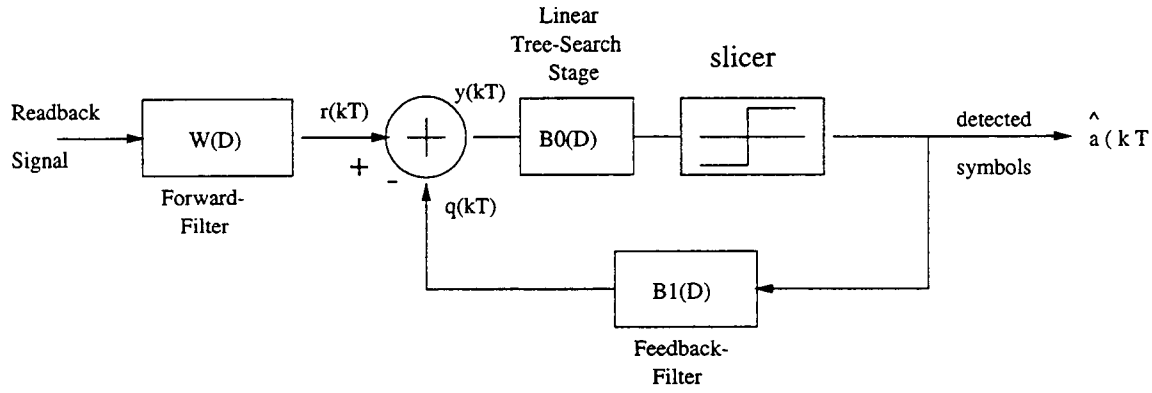


Figure 1.5. FDTS/DF system

mance. MDFE advantageously integrates the functionality of the linear comparator stage used in FDTS/DF for realizing the tree search into the forward and backward path. The forward path of MDFE is implemented in contiuous-tim analog analog architecture rendering fast and simple circuits. As the detection scheme operates on a sampled basis in discrete-time domain, the output of the forward equalizer has to be sampled at the appropriate instants to ensure the detection capability and prober cancellation of post-cursor ISI. Furthermore, as the signal levels of the feedback path are determined by the FIR coefficients and the detected symbols with fixed amplitude of ± 1, the gain of the forward path has to be set accordingly to preserve the multi-level eye of the detection scheme.

This thesis presents suitable phase and gain detection schemes and the filters included in the phase locked loop for the timing recovery and the automatic gain control. In the next chapter the structure and signal processing of MDFE is described as background of the sample and phase detection. In a third chapter, the coding scheme is briefly explained as well as its statistical properties which can be

used for simplified evaluation of the system behavior. The symbol patterns during both acquisition and tracking mode are explained. Noise and ISI characteristics of MDFE are given. With this knowledge an optimal point for sampling the mainlobe in the pulse response of the forward path is computed and optimal backward equalizer coefficients are selected. Chapter 4 describes concepts for the phase and gain detection derived from a minimum mean square criterion and evaluates the perfomance of different concepts. Then the loop filters for both the timing recovery and the automatic gain control are designed and their transient behaviors displayed. For the case of acquisition mode the transfer-functions are developed and their frequency behavior evaluated. A hardware implementation in CMOS technology for both the phase and the gain detection is presented in Chapter 5. The applied switched current mode technique ensures fast and low power consuming circuits. Additionally a discussion of nonideal effects is given. Chapter 6 contains the conclusion and in the Appendix the SABER simulator and the MATLAB simulation are described.

2. BACKGROUND - MDFE

One of the advantages of MDFE proposed in its most recent version [6] is its analog architecture of most components implying low complexity. The complete architecture is displayed in the appendix.

2.1. FORWARD PATH

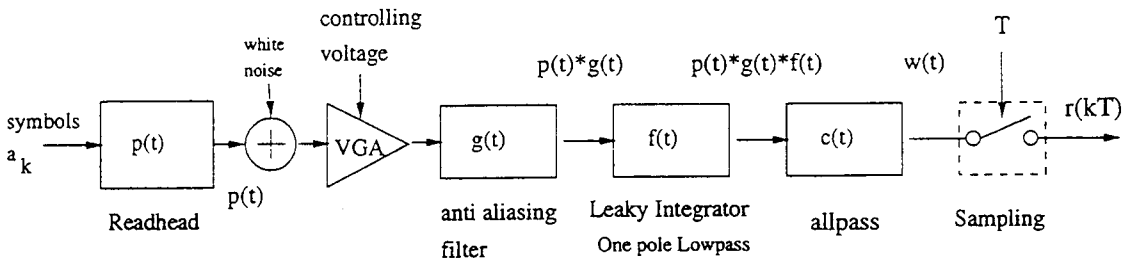


Figure 2.1. Forward path of MDFE

The block diagram of the forward path is pictured in figure *2.1.* A thorough understanding of the underlying signal processing is an essential prerequisite for the design of the phase and gain detection. The starting point for a detailed analysis of the MDFE system is the input of the forward path. The RLL coded symbols a_k form a symbol stream consisting of $+1$ and -1. The data symbols are fed into the recording channel at a rate of 100 Mbit/s which equals a symbol spacing of 10 ns. Each symbol can assume an amplitude of $+1$ or -1. The recording process can be characterized by the response of the readhead to a unit positive transition. It is a

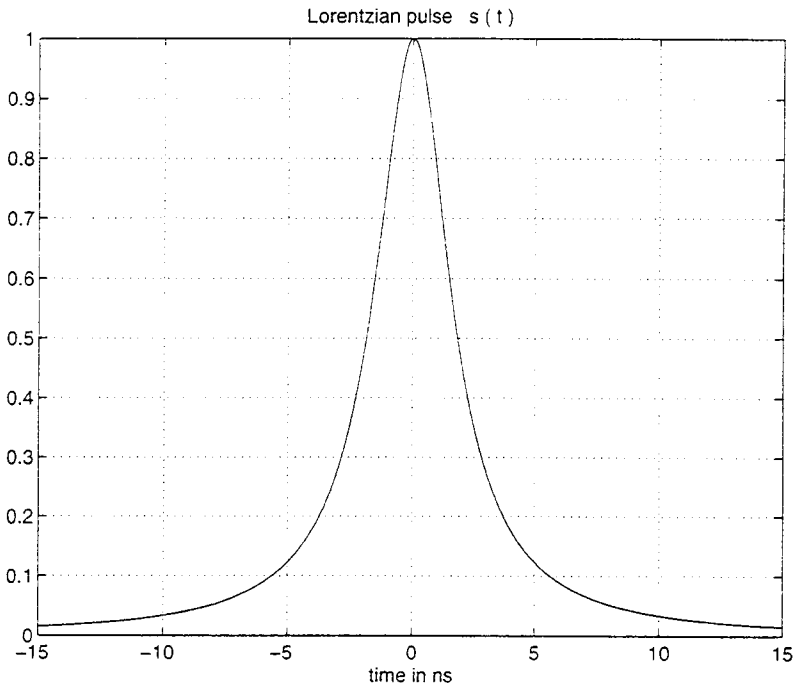


Figure 2.2. Step response s(t)

common practice to model the step response $s(t)$ of the magnetic read head by the symmetric Lorentzian pulse, which is given as

$$s(t) = \frac{1}{1 + \left(\frac{2t}{PW50}\right)^{2x}} \qquad 1 \leq x \leq 1.5 \tag{2.1}$$

The parameter $PW50$ is called the 'half-height-width' of the Lorentzian pulse, while t stands for the time variable. For the original Lorentzian, parameter x is set to 1. However, $x \geq 1$ can yield a more accurate model [2]. The response to a data symbol pulse can be expressed by a convolution with the term $(1 - D)$, where D refers to a unit delay. This renders the so-called dibit response $p(t)$:

$$p(t) \;=\; s(t) \;-\; s(t - T) \tag{2.2}$$

The dibit response is implemented in the simulation as FIR filter. The real behavior

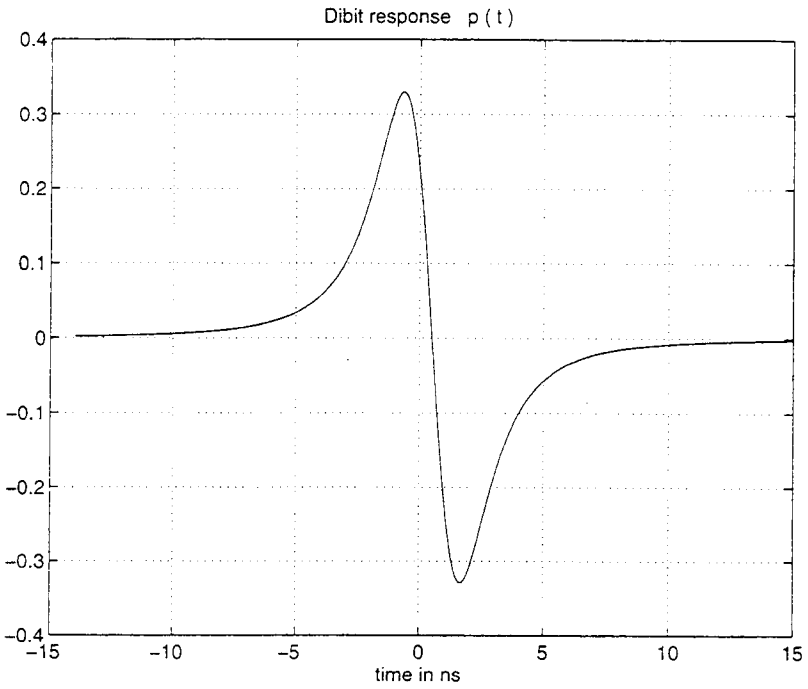


Figure 2.3. Dibit response p(t)

of the readhead is transformed into a valid model by introducing an oversampling factor of four for the head response. In sampled data systems oversampling effects an interpolation between the regularly spaced samples [7]. The frequency characteristics of the readback signal exhibits bandpass behavior with the bulk of energy shifted towards lower frequencies as the storage density $PW50$ increases.

As the amplitude levels may vary due to changes of tracks or flying height variations of the readhead, the gain has to be adjusted dynamically according to the measured gain error. The appropriate control of the variable-vain amplifier (VGA), which is used for this purpose, is a major part of this thesis.

At the output of the VGA the signal $u(t)$ is obtained as

$$u(mT_{ov}) = \sum_n a_{k-n} p(kT - mT_{ov}) \cdot v(kT) \quad + \quad n(kT)v(kT); \qquad T_{ov} = \frac{T}{M} \quad (2.3)$$

$$m = 4 \cdot k + \{0, 1, 2, 3\}$$

The variable v expresses the gain of the VGA. T is the symbol period, while M stands for the oversampling factor.

It has been shown in [8] that high density recording channels using a 2/3 (1,7) run-length limited code are sufficiently bandlimited. An anti-aliasing filter is used to attenuate high-frequency noise, which is implemented as a fourth-order Butterworth low-pass filter with a cutoff frequency of $\frac{2}{5T_{ov}}$, where T_{ov} denotes the symbol period divided by the oversampling factor. This filter achieves a reduction of high frequency noise.

It has been found [6] that an additional leaky integrator with impulse response $f(t)$ provides better equalization. Allpass-equalization, which follows next, has been shown to be an advantageous forward filter for decision feedback equalization [9]. The allpass filter $c(t)$ is designed to achieve a minimum phase system by

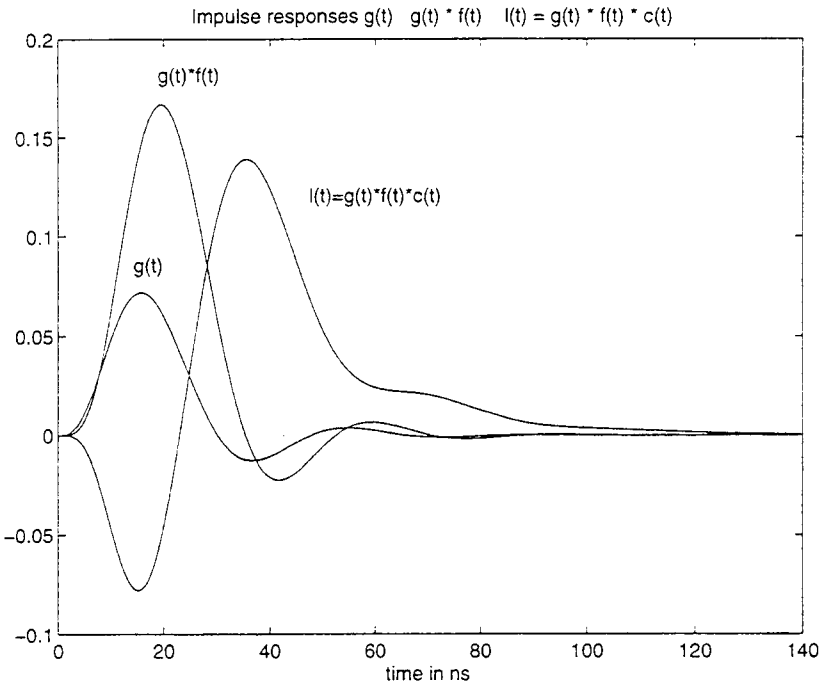


Figure 2.4. Impulse responses of $g(t)$ $g(t) * f(t)$ $l(t)$

a pole-zero cancellation. The output is characterized by a sharpened leading edge compared to the pure dibit response to reduce uncancellable pre-cursor ISI. The bulk of energy is moved to the mainlobe and the trailing end, where the concept of DFE can cancel this post-cursor ISI. Hereby an asymmetric response is shaped. Unfortunately, a slight pre-cursor undershoot is evident in the signal from the allpass filter.

The impulse response of the anti-aliasing filter (AAF) $g(t)$, together with the following intergrator $f(t)$ and the allpass $c(t)$ form the impulse response $l(t)$ of the entire forward equalizer

$$l(t) \quad = g(t) * f(t) * c(t) \tag{2.4}$$

The impulse responses are shown in figure *2.4*. At the output of the forward

equalizer, the signal is sampled. This is a decisive point for the performance of the detector. As the phase and the frequency of the received signal may vary as a result of phase jitter and noise, the timing of the sampling has to be adjusted in a dynamic manner to guarantee the functionality of the following detection process. The oversampled channel response to a pulse a_k is determined by the equation

$$w(kT) = [u(mT_{ov}) * l(mT_{ov})]_{kT} = [u(mT_{ov}) * g(t) * f(t) * c(t)]_{kT} \tag{2.5}$$

The graph of $w(t)$ together with the other impulse responses appearing in the forward path is shown in figure *2.5*. For a symbol sequence $\{a_k\}$ we obtain at the output of the Forward-path, shown in figure *2.6*:

$$r(kT) = \sum_n a_{k-n} w(T_0 + nT) + n'(kT) \tag{2.6}$$

The sampling phase is denoted by T_0; coloured noise is represented by n'.

2.2. FEEDBACK AND DECISIONS

Past decisions $\hat{a}_k \in \{+1, -1\}$ serve as input to the backward equalizer. The goal of the feedback path is to cancel as much intersymbol interference as possible. The bulk of the intersymbol interference was shifted by the forward equalizer to the trailing end of the pulse response $w(t)$ where it causes post-cursor ISI. This is desired, as the corresponding symbols have already been detected. The principle of DFE provides compensation of this ISI by convolution of the past decisions with the corresponding values of w_k in an FIR filter. The coefficients b_k of the backward equalizer im MDFE are then determined in the following way:

$$b_k = \begin{cases} w_1 - w_{-1} & k = 1 \\ w_k & 2 \leq k \leq L \end{cases} \tag{2.7}$$

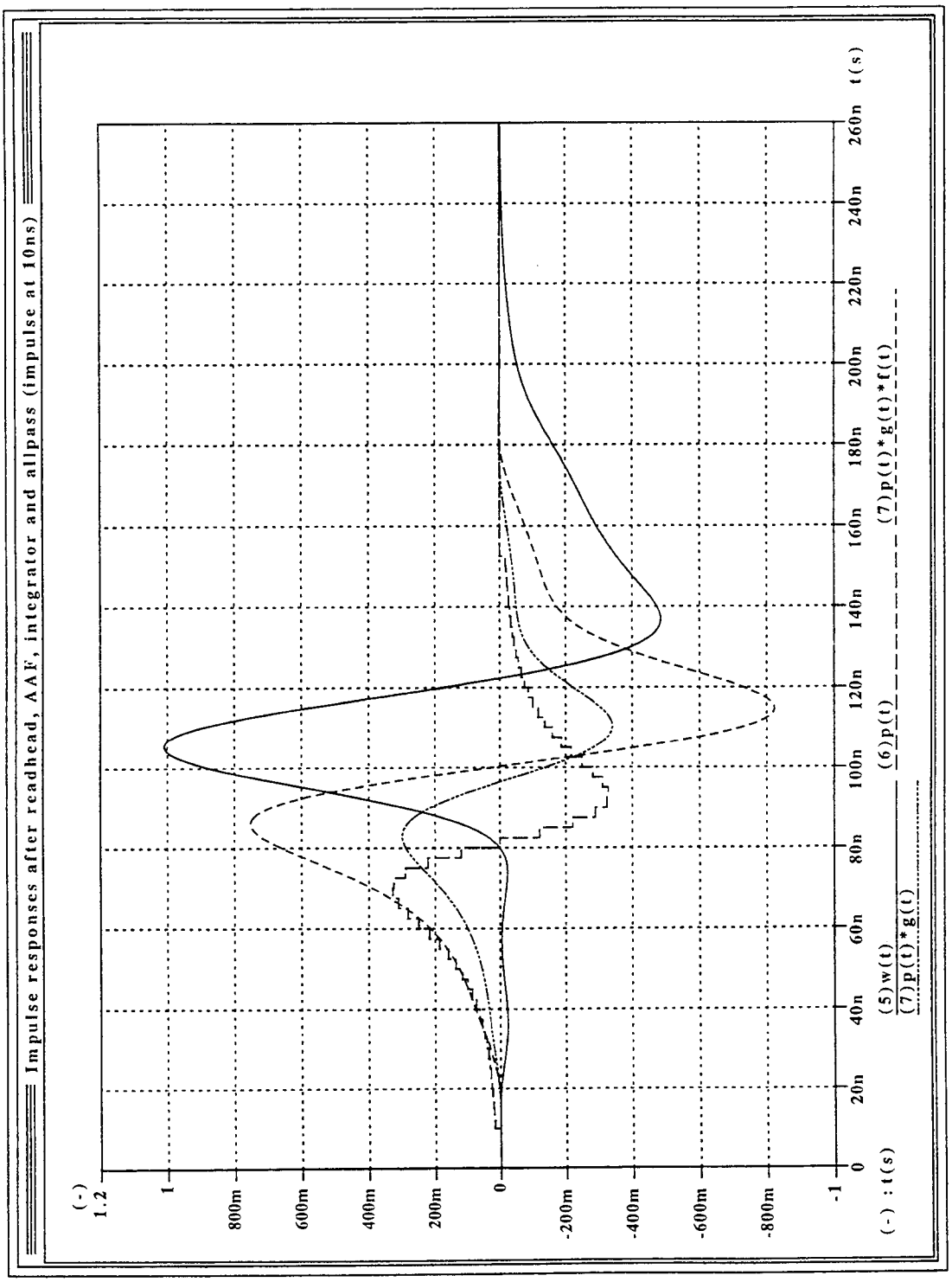


Figure 2.5. Impulse responses in the forward path

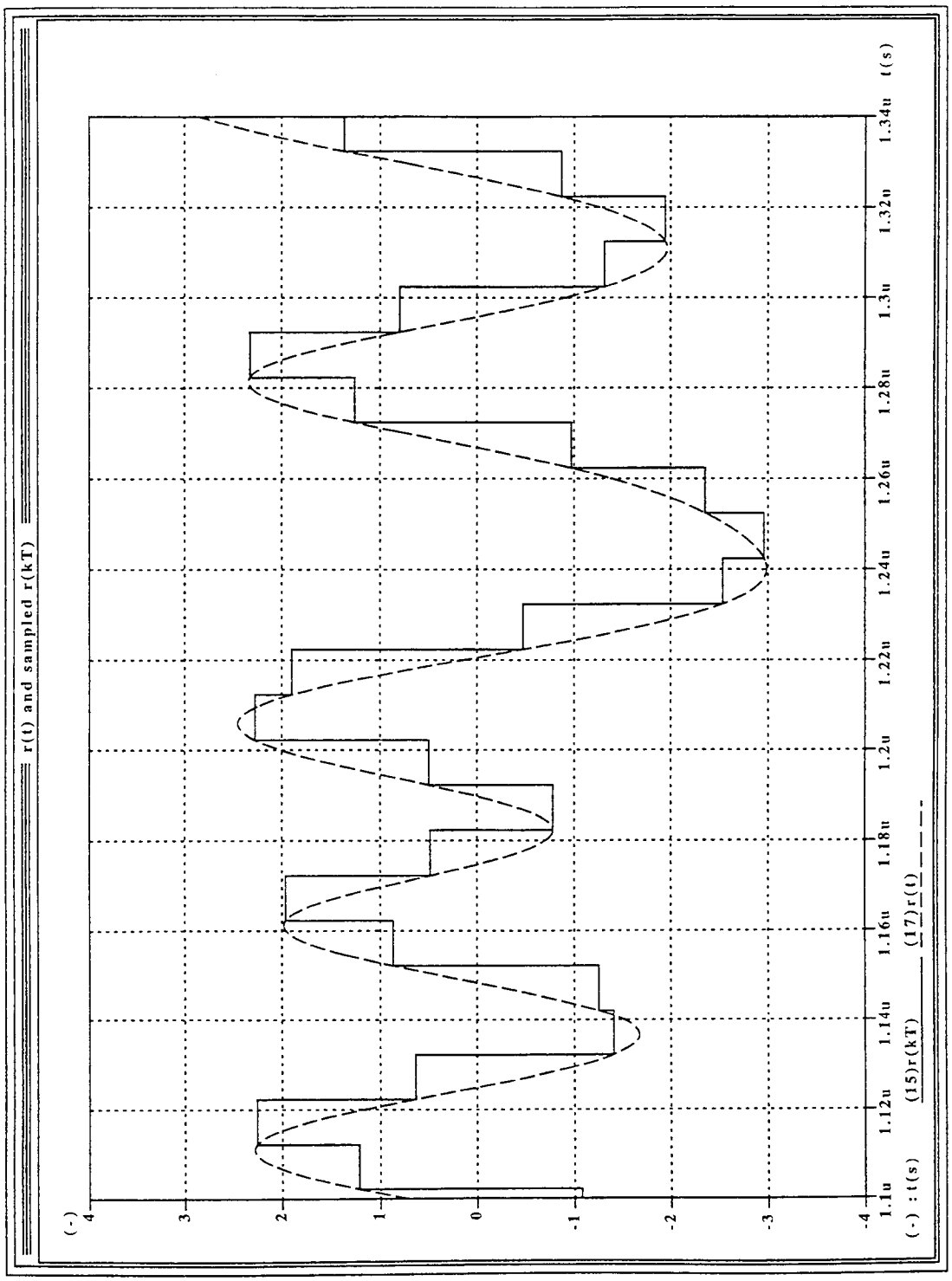


Figure 2.6. r(t) and sampled r(kT)

It is shown in [6] that the entire tree search of the Viterbi maximum likelihood detection can be expressed by a 2-tap FIR-Filter. In MDFE, this filter is contained in the forward and backward path, which jointly shape the multi-level eye. The summed slicer-input takes the form 3.7

$$y(kT) = w_{-1}(a_{k+1} + a_{k-1}) + a_k + ISI_u + n'(kT) \tag{2.8}$$

where the term ISI_u denotes uncancelled intersymbol interference. This is illustrated in figure *3.7* and further explained in chapter 3. Decisions are made on the middle symbol according to the decision rule

$$\hat{a}_k \quad = \begin{cases} +1 & y(kT) \geq 0 \\ -1 & y(kT) < 0 \end{cases} \tag{2.9}$$

Because the symbols are coded with a minimum run-length constraint in 2/3(1,7) RLL code, there must be at least $d = 1$ symbols between transitions $a_{k-1} = +1 \rightarrow a_k = -1$ and $a_{k-1} = -1 \rightarrow a_k = +1$, respectively, such that at least two sequent symbols a have the same polarity. For that reason the sequences $\{-1, +1, -1\}$ and $\{+1, -1, +1\}$ are not allowed.

Neglecting the uncancelled ISI and the noise, the input to the slicer can take on the following four values

$$y_k \in \{-2w_{-1} - 1; \quad -1; \quad +1; \quad +2w_{-1} + 1\} \tag{2.10}$$

This leads to the characteristic waveforms for the slicer-input. A simulation plot of the sampled forward equalizer response, the output of the feedback filter and the slicer-input as summation is displayed in figure *2.7*.

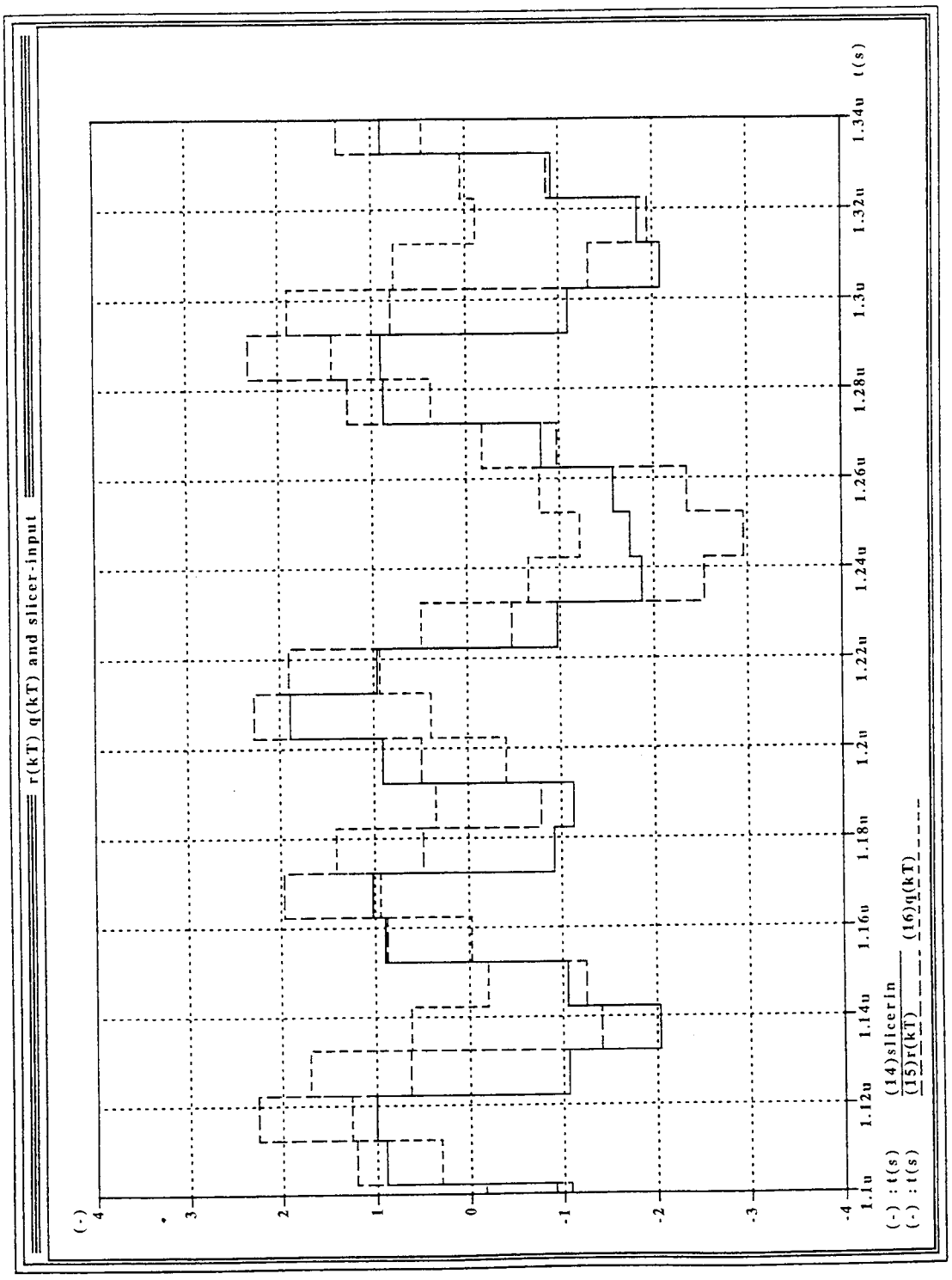


Figure 2.7. Forward equalizer $r(kT)$, feedback-output $q(kT)$, slicer-input

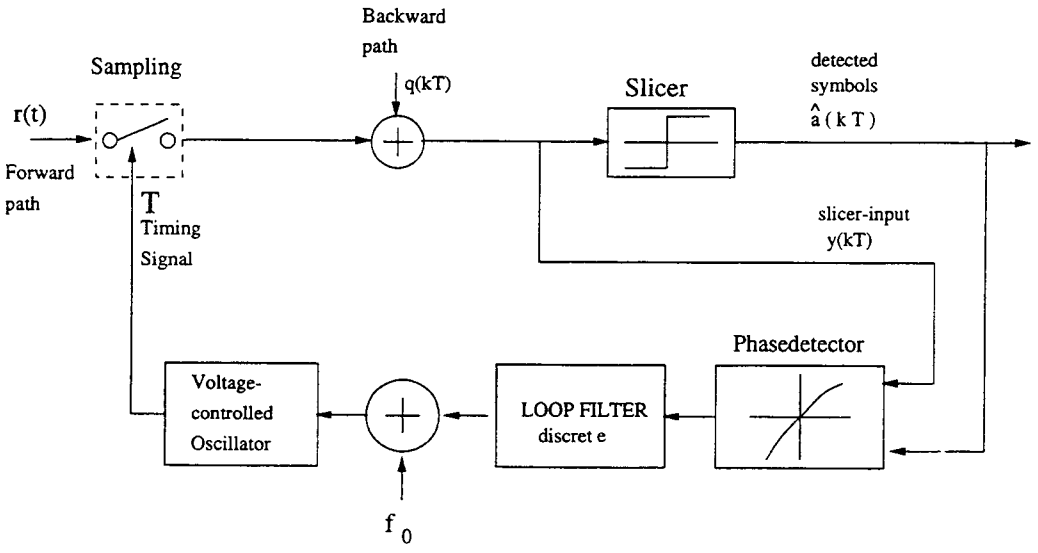


Figure 2.8. Block diagram of the Timing Recovery system

2.3. TIMING RECOVERY AND GAIN ADJUSTMENT

All the discrete-time operated blocks in MDFE are clocked by the timing recovery system. It uses the block diagram depicted in figure *2.8*. Phase detection is performed based on the prior decisions $\hat{a}_k$ and the slicer-input values y_k. The phase error ϕ is passed to the loop filter which is a sampled filter with impulse response $ph(z)$. In the following voltage-controlled oscillator (VCO) the sampling frequency is added as basic frequency and the adjusted clock signals are obtained as output.

The slicer-input and past decisions are also passed on to the automatic gain control as can be seen from figure *2.9*. The gain error Δg is modified in the sampled analog loop filter; an integrator is a necessary component for noisy gain error signals. The controlling voltage for the VGA is comprised of a constant nominal gain and the output of the loop filter.

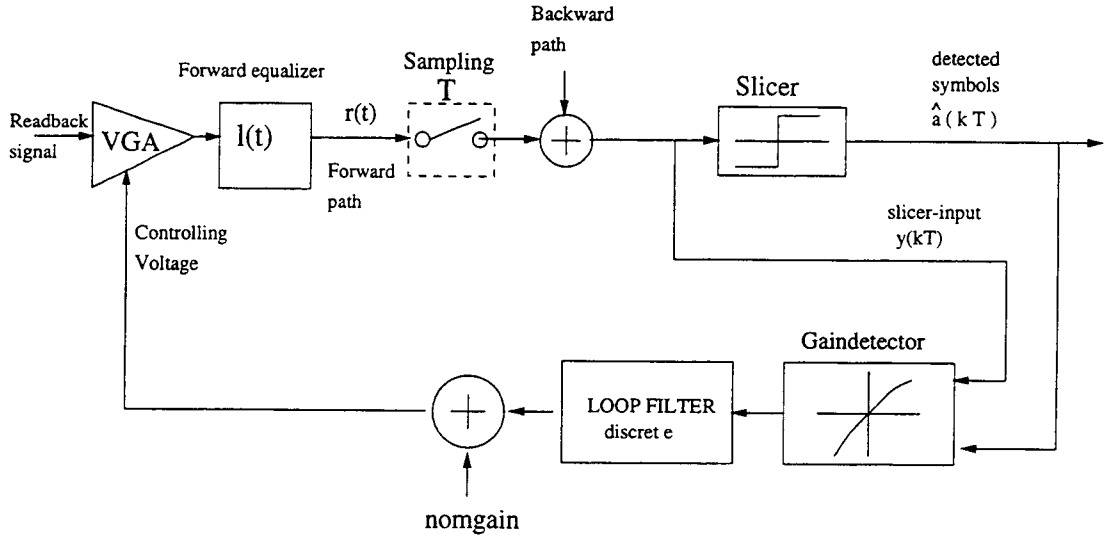


Figure 2.9. Block diagram of the Automatic Gain Control

3. SIGNALS AND SYMBOLS IN MDFE

3.1. 2/3 (1,7) RLL CODING

Incoming user bits are encoded in two steps into symbols a_k which are suitable for transmission and detection in a communication system. The input consists of user bits 0 and 1, which are equally likely. It has become a common practice to use $m/n(d,k)$ run-length limited codes, specifying both the minimum and maximum number of data symbols 0 between two symbols 1 in the encoded symbol string. The minimum run-length constraint d was introduced to increase the minimum spacing between magnetic transitions; as already mentioned, this contributes to attaining a reliable detection of peaks. MDFE depends on the presence of this constraint. The maximum run-length constraint k puts an upper limit on the number of consecutive zeros. As the phase and the gain updating depend on the occurence of transitions, this ensures that these values can be updated within reasonable time periods. The rate m/n indicates the ratio between the number of symbols n used to encode m user bits; an upper limit for this ratio is inherently determined by the run-length constraints (d,k). In our case, 3 symbols are used to encode 2 user bits. Given these constraints, we can draw the run-length-diagram shown in the appendix. The coding of the user bits into the actual symbol sequences is defined by a look-up table shown in table *3.1*, which incorporates the coding rules. Certain combinations of user bits would lead to violations of the constraints. In this case, the assignment of the current and preceding codewords are changed according to the substitution table. A finite state description is found in the appendix. By this coding scheme there is an inherent correlation between symbols introduced which is explained in more

User Bits	Code (Basic)	User Bits	Code (Violations)
00	101	00.00	101.000
01	100	00.01	100.000
10	001	10.00	001.000
11	010	10.01	010.000

Table 3.1. RLL 2/3(1,7) Look-up table

a_0	a_1	a_2	a_3	a_4	a_5	a_6	a_7	a_8
(-1) (trans.)	1	1	0.2185	-0.2816	-0.2816	-0.0813	0.048	0.046
1	0.3909	-0.2180	-0.3427	-0.1612	0.0169	0.0843	0.0637	0.032

Table 3.2. Mean values for symbols a_k given $a_0 = -1$ and transition

detail in the appendix. After the encoding, the coded sequences $01001000\cdots$ are converted into the binary symbol sequence $a \in \{1, -1\}$ by the precoder to achieve a zero mean value suitable for the magnetic recording operation. Each 1 translates into a change of polarity, while a 0 keeps the same polarity, e.g.

$$\{\cdots 01001000\cdots\} \quad \longrightarrow \quad \{\cdots 1,1,-1,-1,-1,1,1,1\cdots\}$$

Expected values $E\{a_m \mid a_0 = 1\}$ were calculated for the sequence $a_{k+1}, a_{k+2}, \cdots$ based upon the inherent correlation provided by the coding. This was done both for the case of just one detected symbol $\hat{a}_k$ in general and also if a transition has occured between $\hat{a}_{k-1}$ and $\hat{a}_k$. The results are stated in table *3.2.* An important quantity is the average run-length, which is well confirmed by the random sequences generated for the SABER simulation and given in [11] as

$$E_{run-length} = \frac{240}{73} = 3.2877 \qquad \text{compare to SABER:} \quad E = 3.28322 \tag{3.1}$$

Those results allow a convenient computation of average behaviors of the system which can be used advantageously for evaluating phase error curves quickly; thereby giving a true representation of the behavior with actual random data as the summed variance decreases with the inverse of the number of data symbols. The knowledge about correlated symbols can also be used to introduce a compensation for precursing undershoot, as from the detected symbol $\hat{a}_k$ the mean values for $\hat{a}_{k+1}, \hat{a}_{k+2} \cdots$ canbe used as prediction.

3.2. NOISE AND INTERSYMBOL INTERFERENCE

Noise may be generated in the recording channel as an effect of track changes, unequally spaced transitions and by noisy components. Further discussion of noise is found e.g. in [20]. In the simulation model, noise is introduced as white noise in front of the VGA and then passes through the anti-aliasing filter, the integrator and the allpass. The power-spectrum of the white noise at the input is denoted as

$$N_0 = \sigma_n^2 = constant \tag{3.2}$$

The power spectrum of the colored noise after the forward equalizer $l(t) = g(t) * f(t) * c(t)$ can be written as

$$\sigma_{nc}^2 = \frac{1}{2\pi} \int_{-\infty}^{+\infty} \sigma_n^2 \cdot \mid G(j\omega)F(j\omega)C(j\omega) \mid^2 d\omega \tag{3.3}$$

$$= \sigma_n^2 \cdot \int_{-\infty}^{+\infty} l(t)^2 \, dt \tag{3.4}$$

$$= \frac{\sigma_n^2}{w^2(T_0)} \cdot \sum_m l(mT + T_0 + \tau)^2 \tag{3.5}$$

Eqn. 3.4 can be written in accordance to Parseval's Theorem due to the fact that the noise at the input is assumed to be white and uncorrelated, the integral of eqn. 3.4 simplifies in the discrete-time domain to the sum of eqn. 3.5 scaled by the normalization factor $\frac{1}{w^2(T_0)}$. Parameter T_0 stands for the desired sampling point and τ represents a phaseshift within the range of a half time interval. The noise is not affected seriously by a small phaseshift, as can be seen from figure *3.1.* Intersymbol interference (ISI) is present in the system as a result of the superposition of the responses of the readhead to symbol transitions. Equation 3.6 gives an expression for the ISI at the slicer-input as a function of sampling point T_0 and phaseshift τ.

$$\bar{y}^2_{ISI} = \frac{1}{w^2(T_0)} \cdot \Big[\sum_{n=-\infty;n\neq 0}^{\infty}{}' \Big[(a_{k-n} \cdot w(nT + T_0 + \tau)\Big] - a_0 \cdot w(T_0 + \tau) - \sum_{i=1}^{N} \hat{a}_{k-i} \cdot b_i \Big]^2 \tag{3.6}$$

Reasonable upper and lower bounds for the summation $\sum a \cdot w$ are $+14$ and -7, respectively, as only the samples $w_{-7} \cdots w_{14}$ contribute nonnegligible values. The backward equalizer is assumed to be shorter than the causal ISI. Undershoot caused by post-cursor ISI is responsible for the lower margin of the ISI, so that even in the case of perfect settling at the sampling point T_0 selected by the backward equalizer coefficients at phaseshift $\tau = 0$ a small amount of ISI remains, which was measured to be -14 dB. The ISI and the noise as a function of phaseshift τ are depicted in figure *3.1.* This plot was taken at a Signal-to-Noise-Ratio (SNR) of -20 dB. It becomes clear that the correct timing recovery and dynamic adjustment of the sampling phase is a major requirement for proper functionality of MDFE: i.e. the signal suffers severe of ISI when it is not sampled at the optimum phase. Therefore a fast and reliable timing adjustment is necessary. A variation of the gain gives a deviation proportional to the value of $v(kT)$.

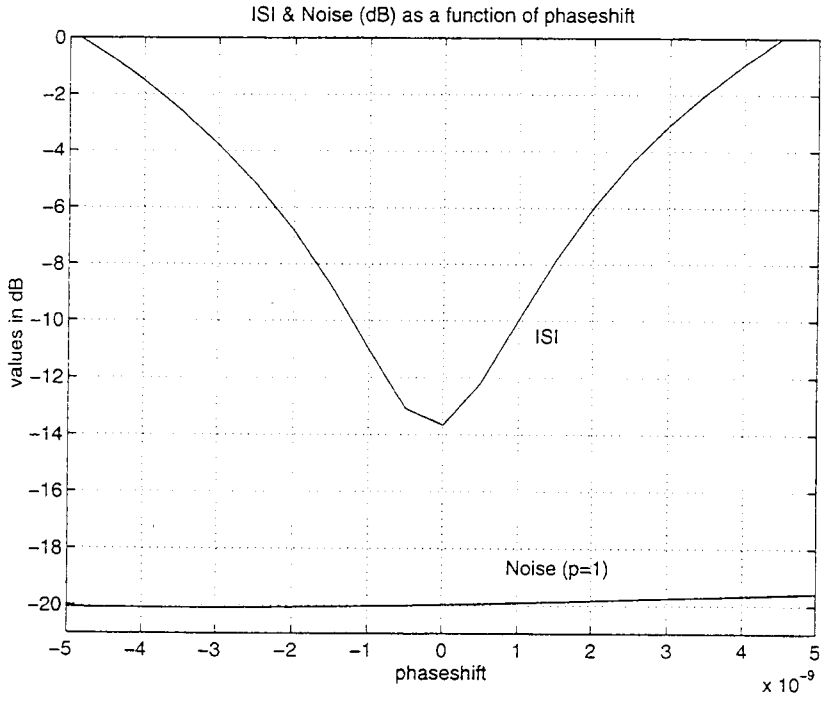


Figure 3.1. ISI^2 and noisepower as a function of phaseshift τ

For the Signal-to-noise-ratio (SNR) we use the sum of the colored noise power and the power of the ISI present at the input to the phase and gain detectors. MDFE uses the slicer-input to generate gain phase errors. We define

$$SNR = \frac{\bar{y}^2}{\sigma_{nc}^2(\text{noise}) + \bar{y}_{ISI}^2} \tag{3.7}$$

using for the signal-power $\bar{y}^2$ the contribution of the symbol upon which a decision is carried out

$$\bar{y}^2 = (a_k \cdot w_0)^2 = 1 \quad \text{for correct sampling phase} \tag{3.8}$$

The bit error rate P_e and the power of ISI and noise are related by the Q-function, using a Gaussian random variable with $\sigma_{ISI}^2 = \bar{y}_{ISI}^2$ as approximation for the influence of ISI as presented in [14]. If we let the sum of ISI and noise

$$S = \sum_{n=-\infty;n\neq 0}^{\infty}{}' \Big[(a_{k-n} \cdot w(nT + T_0 + \tau) - a_0 \cdot w(T_0 + \tau) - \sum_{i=1}^{N} \hat{a}_{k-i} \cdot b_i + n'(kT) \tag{3.9}$$

then with $\sigma_S^2 = \sigma_{nc}^2 + \sigma_{ISI}^2$ the worst-case probability P_e for a biterror is defined approximately by

$$P_e = P\Big[\mid S \mid > 1\Big] \tag{3.10}$$

$$= \int_1^{+\infty} p_e(u)du \tag{3.11}$$

$$= \frac{1}{\sqrt{2\pi}\sigma_S} \cdot \int_1^{+\infty} e^{-\frac{1}{2}\left(\frac{u}{\sigma_S}\right)^2} du \tag{3.12}$$

Applying the Q-function

$$Q_e(\alpha) = \frac{1}{\sqrt{2\pi}} \cdot \int_{\alpha}^{+\infty} e^{-\frac{1}{2}u^2} du$$

we obtain finally

$$P_e = \frac{1}{\sqrt{2\pi}} \cdot \int_{\frac{1}{\sigma_S}}^{+\infty} e^{-\frac{1}{2}u^2} du \tag{3.13}$$

$$= Q_e\Big(\frac{1}{\sigma_S}\Big) \tag{3.14}$$

The bit error probability as a function of phaseshift is shown in figure *3.2.*

3.3. SYMBOL PATTERNS AND SIGNAL SHAPES

3.3.1. Tracking mode

In tracking mode, user bits are received from the magnetic recording channel. Assuming them to be completely random, the properties in terms of the probabilities

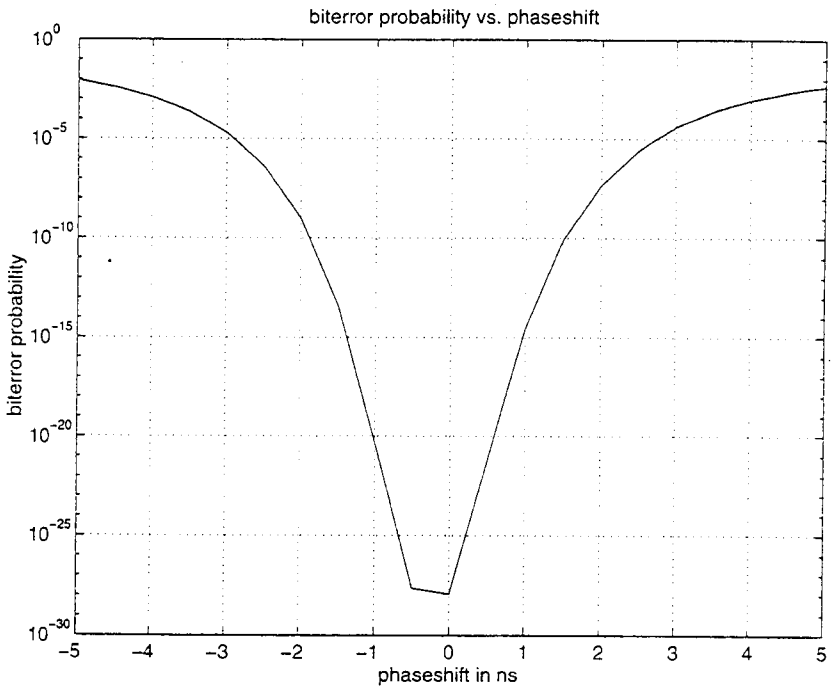


Figure 3.2. P_e as a function of phaseshift

derived in chapter 3.1 apply. Resulting from eqn. 2.8 the multi-level eye can take on all of the values of

$$\hat{y} \in \{-2w_{-1} - 1; \quad -1; \quad +1; \quad +2w_{-1} + 1\}$$

for the sequences listed in table *3.3*: Changes in these levels occur only between adjacent levels. Hence the steepest slopes will appear in jumps from $+1 \rightarrow -1$ and $-1 \rightarrow +1$. For that reason, a phase detection scheme will focus only on these parts of the received signal.

3.3.2. Acquisition mode

For fast initial adjustment of gain and timing phase, a known preamble is stored. During the acquisition phase, the preamble is fed synchronously to the

a_{k-1}	a_k	a_{k+1}	$\hat{y}$
-1	-1	-1	$-2w_{-1}-1$
-1	-1	+1	-1
-1	+1	-1	not allowed
-1	+1	+1	+1
+1	-1	-1	-1
+1	-1	+1	not allowed
+1	+1	-1	+1
+1	+1	+1	$+2w_{-1}+1$

Table 3.3. Ideal values $\hat{y}$ for slicerin

backward-equalizer. By the choice of the minimum run-length of $d = 1$, i.e. just two consecutive symbols share the same polarity, the largest number of transitions is achieved and hence the maximum number of phase- and gain updates can be carried out. By usage of the preamble $\{1, 1, -1, -1, 1, 1, -1 \cdots\}$, these equations hold: Equation 2.1 defines the stepresponse $s(t)$; the Fourier transform of this Lorentzian pulse is described by

$$s(t) \quad \circ\!\!-\!\!\!-\!\!\!\bullet^{\mathcal{F}} \quad S(\Omega) = \frac{\pi APW50}{4} \cdot \exp(-PW50 \cdot \frac{\omega}{\omega_s}) \tag{3.15}$$

with radians sampling frequency $\omega_s = 2\pi 100\text{MHz}$, the normalized frequency $\Omega = \frac{\omega}{\omega_s}$ and Sampling interval T_s. The readback-signal, assuming no noise, is a superposition of step responses in distances of $2 \cdot T_s$ with amplitude 2 as shown in figure *3.3*:

$$u(t) = \cdots - 2s(t + 2T_s) + 2s(t) - 2s(t - 2T_s) + 2s(t - 4T_s) \cdots \tag{3.16}$$

or in the frequency domain

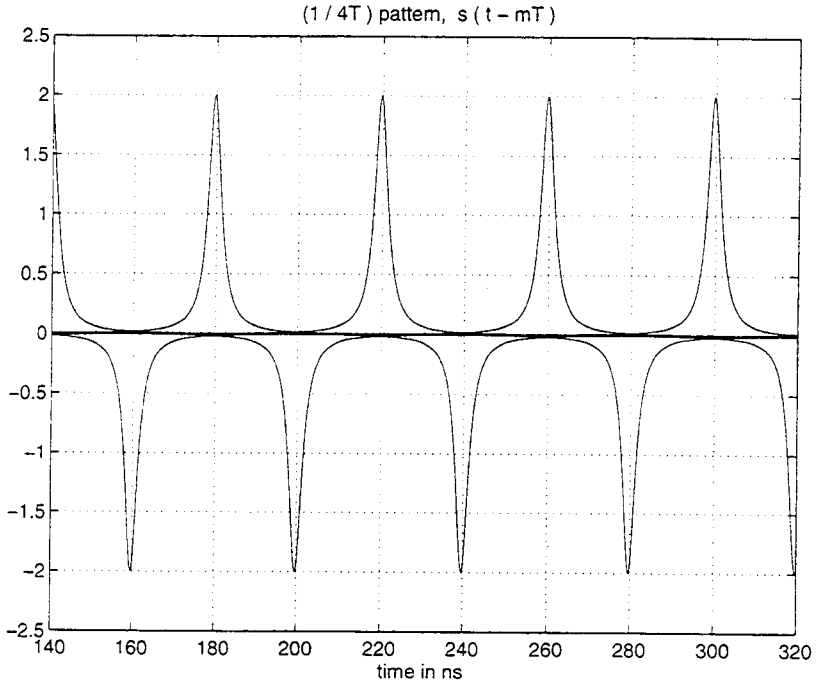


Figure 3.3. Superposition of step responses in readback signal

$$U(\omega) = \cdots - 2S(\Omega) \cdot e^{\jmath\omega 2T_s} + 2S(\Omega) - 2S(\Omega) \cdot e^{-\jmath\omega 2T_s} + 2S(\Omega) \cdot e^{-\jmath\omega 4T_s} \cdots \quad (3.17)$$

$$= 2S(\Omega)(1 - e^{-\jmath\omega 2T_s}) \cdot \sum_{\nu=-\infty}^{+\infty} e^{-\jmath\nu\omega 4T_s} \quad (3.18)$$

It can be shown via Fourier-Series

$$AA(\omega) = 2S(\Omega)(1 - e^{-\jmath\omega 2T_s}) \cdot \frac{\omega_s}{4} \sum_{\nu=-\infty}^{+\infty} \delta(\omega - \nu\frac{\omega_s}{4}) \quad (3.19)$$

The anti-aliasing Filter, with $M = 4$ has a cutoff-frequency of $\frac{M \cdot 2}{5T_s} = \frac{4\omega_s}{5\pi}$. As it is of order four and $AA(\omega)$ is a line spectrum, the limits of the integration in the Fourier-integral can be approximated by the cutoff frequency. The magnitudes in the frequency domain are shown in figure *3.4*. Filtering yields for the Fourier-backtransformation of the signal at its output

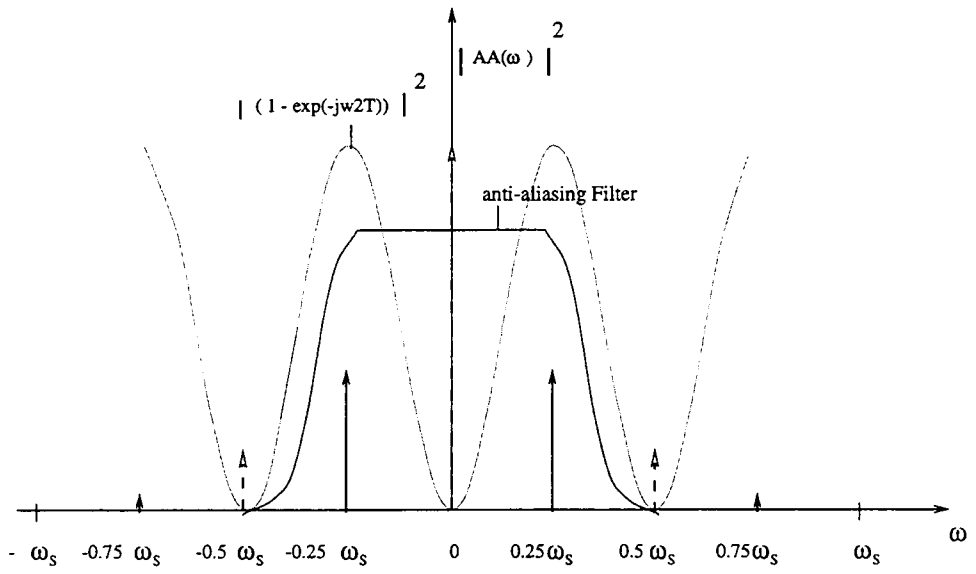


Figure 3.4. Magnitudes of $AA(\omega)$, anti-aliasing filter

$$aa(t) = 2 \cdot \frac{1}{2\pi} \int_{-\frac{\omega_s}{5\pi}}^{+\frac{4\omega_s}{5\pi}} \frac{\pi APW50}{4} \exp(-PW50 \cdot \frac{\omega}{\omega_s})(1 - e^{-j\omega 2T_s}) \frac{\omega_s}{4} \sum_{\nu=-1}^{+1} \delta(\omega - \nu \frac{\omega_s}{4}) e^{j\omega t} d\omega \tag{3.20}$$

leading to

$$aa(t) \;=\; \frac{APW50}{16} \cdot exp(\frac{-PW50}{4}) \cdot \cos\Big(\frac{\omega_s}{4} \cdot t\Big) \tag{3.21}$$

and hence, the output of the forward-path is a sinusoidal wave with frequency $\frac{\omega_s}{4}$. A verification is provided by the output of the SABER- Simulator for the acquisition period in figure *3.5.* This can be used for some examples and explanations later on, where the following equation with $\eta = const.$, a selected phase T_1 and feedback q_k is used for the slicer-input

$$y(kT) = y_k = \eta \cdot \sin\Big(\frac{\omega_s}{4} T_1\Big) - q_k \tag{3.22}$$

The signal $r(t)$ during the acquisition phase together with the slicer-input is plotted in figure *3.5.* After the summing node the slicer-input signal during acquisition is rectangular with widths $2 \cdot T_S$ if phase and gain are adjusted correctly.

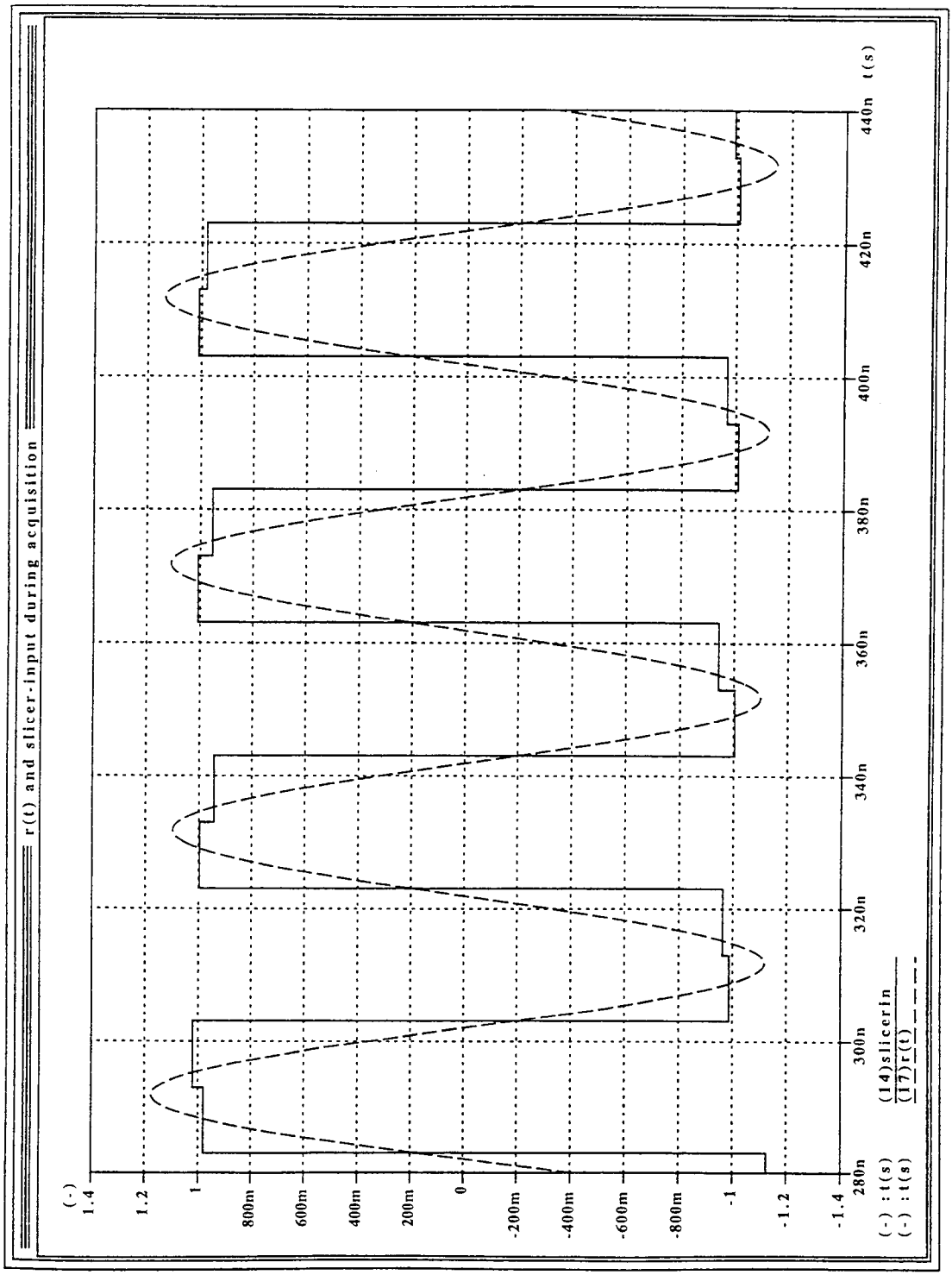


Figure 3.5. Slicer-input and r(t) during acquisition

3.4. DETERMINATION OF SAMPLING POINT T_0

For a given set of values in the the backward equalizer, an optimal sampling point T_0 exists. The factor $A = \frac{1}{w(T_0)^2}$, where $w(T_0) = w_0$ denotes a scaling factor, determined by the height of the main-sample, by which the entire response is scaled. Three criteria have to be taken into consideration:

1. The energy contained in the mainlobe-sample w_0 upon which decisions are made should be as large as possible, expressed as

$$E_{\text{main-sample}} = \frac{w(T_0)^2}{\sigma_{nc}^2 \cdot A^2} = \frac{w(T_0)^4}{\sigma_{nc}^2} \tag{3.23}$$

   By choosing the scaling factor A, the noise is scaled as well.

2. Pre-cursor ISI caused by undershoot in the transition response of the forward path has to be minimized, i.e. a small value for the sum

$$E_{\text{pre-cursor}} = \sum_{n=-m}^{n=-2} \left[w(T_0 - n * T)\right]^2 \tag{3.24}$$

   A value of $m = 7$ works well.

3. The signal $r(kT)$ exhibits steep slopes at the times a transition is transmitted. For the timing recovery this can be exploited to extract phase error information. A selection for the sampling point in the middle of a region of steep slope renders a maximal range in which phaseshift causes a fairly linear error. If the signal $r(t)$ is sinusoidal, for example, the region around a zero-crossing is suitable for placing a sampling point to extract the phase error. This is especially important during the acquisition period where this can be written in an analyical expression as SNR_{ph}:

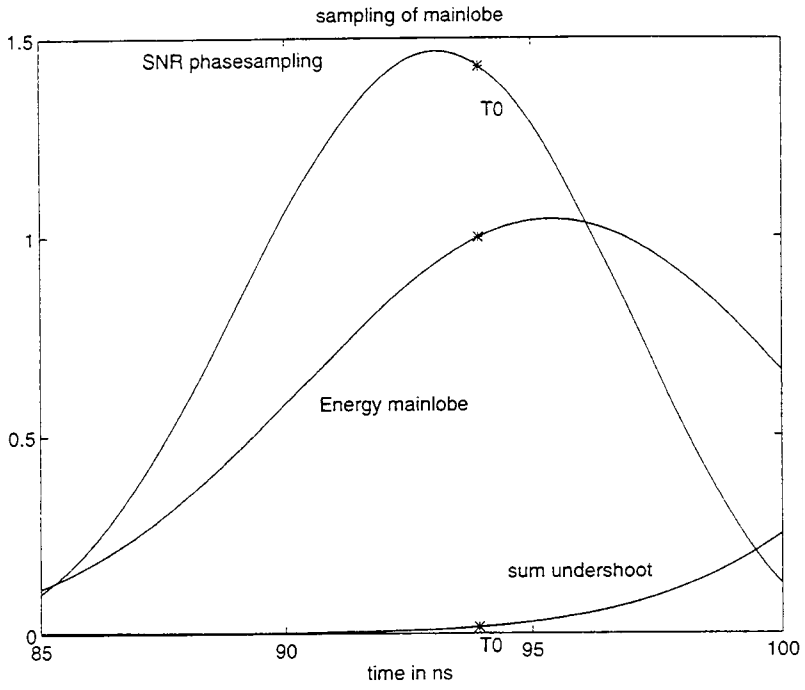


Figure 3.6. Criteria for sampling point T_0

$$SNR_{ph} = \frac{\left[\sum_n (-1)^{i+1}[w(T_0+2nT)+w(T_0+(2k+1)T)]\right]^2}{\sigma_{nc}^2 A^2} \tag{3.25}$$

All three criteria are depicted in figure *3.6* with a reasonable sampling point. The distribution of the sample values along $w(t)$ are displayed in figure *3.7* together with the corresponding backward-equalizer coefficient values shown as crosses. Additional improvement of ISI due to undershoot in the leading edge of $w(t)$ is achievable by applying the knowledge about the correlation of sequent symbols a_k. The expected values from chapter 3.1 can be used to compute estimation for the post-cursor ISI $z(t)$, given a detected $\hat{a}_{k-1}$ as

$$E\{z(t)\} = \sum_{n=2}^{6} E\{\hat{a}_{k+n}\} \cdot w_{-n} \tag{3.26}$$

In tracking mode with random data a value of $E\{z(t)\} = -0.0188$ is obtained, during the acquisition phase the value is $E\{z(t)\} = 0.0362$ for $\{1,-1,-1,1,1\}$ and

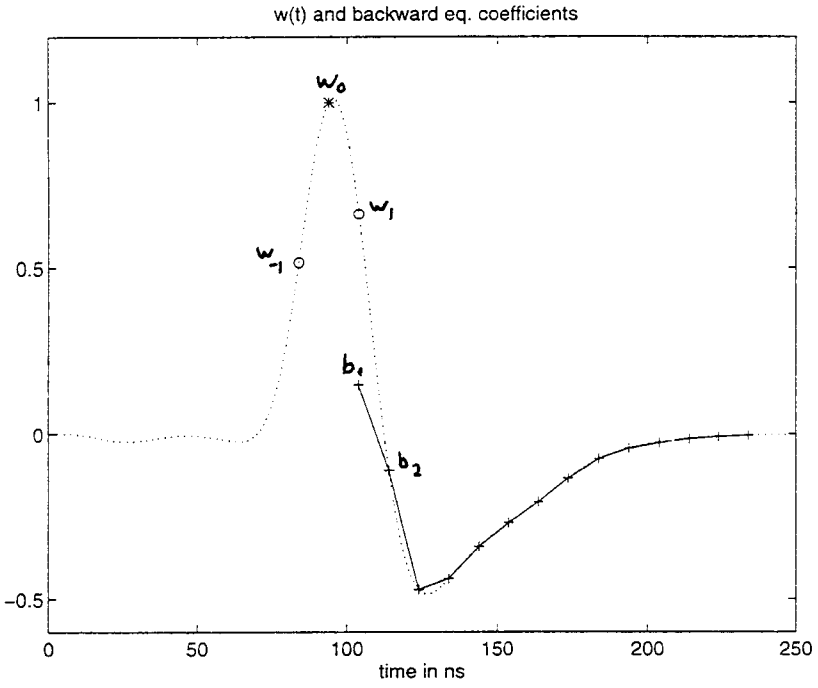


Figure 3.7. Pulse response $w(t)$ with sampling instants nT and backward equalizer

$E\{z(t)\} = -0.0699$ for $\{1, 1, -1, -1, 1\}$. An undershoot-correction can be accomplished by changing the first coefficient of the backward-equalizer into

$$b_1' = b_1 - 0.0203 \tag{3.27}$$

The selection of the Backward-equalization FIR filter coefficients can be seen from figure *3.7*. Slicer-input signals are well equalized, if they show the described eye-levels. As the decision is made in comparison with 0, especially the levels ± 1 around transitions are taken into consideration for the worst case limit on the bit-error and should therefore be kept at their prescribed levels very closely. Figure *2.7* shows an example of the slicer-input during tracking mode. Scaling-factor $A = \frac{1}{w(T_0)^2}$ of the entire response is 1.002 with $w_0 = 0.998$. For a user density of 2.5PW50 and a symbol density of 3.75PW50 and the forward equalizer as described in chapter 2, the following values are suitable for the backward equalizer:

b_1	b_2	b_3	b_4	b_5	b_6	b_7
0.1265	-0.1117	-0.4721	-0.4382	-0.3406	-0.2682	-0.2051
b_8	b_9	b_10	b_11	b_12	b_13	b_14
-0.1341	-0.0757	-0.0436	-0.0266	-0.0156	-0.0089	-0.0053

Table 3.4. Backward equalizer coefficients for a user density of $2.5PW50$

4. TIMING RECOVERY AND AUTOMATIC GAIN CONTROL

Timing recovery is done by a phase-locked loop which tries to maintain the correct phase and frequency of the sampling clock. A general description can be found, for example, in [18]. The block structure of the PLL used in MDFE is shown in figure *2.8*. It will be shown later, that the slicer-input and the detected symbols $\hat{a}_k$ are relevant signals for the phase detection. While the VCO is a given element, the loop filter is besides the phase detector the other crucial block which has to be designed.

The automatic gain control requires at first a gain detector to extract reliable information about the deviation caused by amplitude mismatch between the output of the forward and backward equalizers. As the backward equalizer works with the detected symbols as input, the output of the decision-feedback FIR filter has constant amplitudes. Irregularities in the amplitude of the readback signal in the forward path have to be adjusted by a variable gain amplifier (VGA) so that the multi-level eye at the slicer-input is not distorted.

4.1. DETECTION CONCEPTS

4.1.1. Phasedetector

The PLL has two modes. During acquisition, the clock has to be settled correctly by recovery from the readback signal. In the tracking mode, variations of

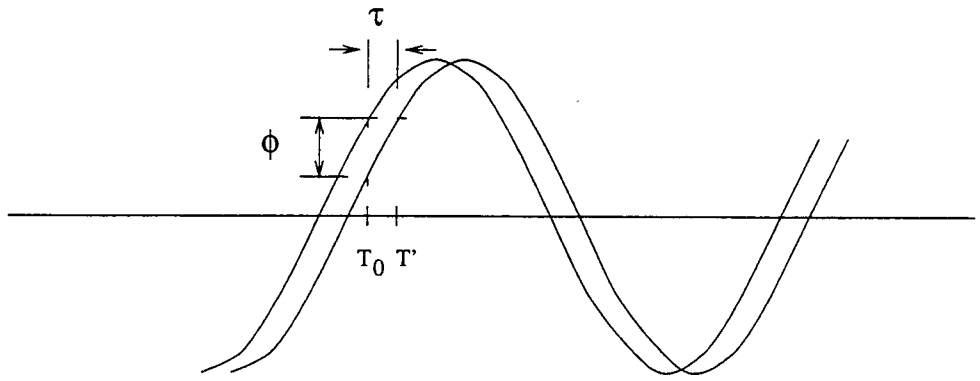


Figure 4.1. Example for phase error

the timing information in the readback signal have to be followed by the clock. The phase of the sampling and clocking of the digital components has to be adjusted to reject possible perturbations in the forward path such as track changes of the read head and thin-film media nonlinearities on the disk translating into a phase step and (white) noise in the circuitry. So the system should be able to detect phase steps in a noisy environment. The computation of the phase error can be explained by an example of a shifted sine-wave plotted in figure *4.1* as it may occur during acquisition. Assuming that the phase is shifted by τ, we encounter a deviation in the signal of e_k from the ideal level for the slicer-input. A phaseshift increases the ISI and thereby lowers the SNR.

The essential requirements for the phasedetector are a suitable output and additionally that the complexity stays in a low level. Possible strategies were proposed for DFE in detection schemes in [13] and for a PRML system in [3]; a timing recovery processing in the case of a digital Forward equalizer was described in [15]. The most suitable technique for retrieving a phase error uses the derivative of the mean square error with respect to the phaseshift τ. It is pointed out in [16], that the obtained curve for the phase error signal should exhibit a monotonic characteristic and a unique zero-crossing, moreover it is desirable if the function yields

linear behavior and has a fair amount of slope. For fulfilling these criteria, it is advantageous to pick the sampling points where transitions occur for a phase update, as mentioned in chapter 3.3. By inspection of the signal $r(t)$ as sketched in figure *2.7* and the corresponding slicer-input curves, it becomes clear, that the slicer-input after a transition-jump is suited best for this purpose. Additionally, a function can be designed for computation of the phase error. Using the following abbreviation where $v(t)$ stands for the current gain value

$$\tilde{w}(t) = \frac{w(t+T_0)}{v(t)}$$

and for the output of the backward-equalizer $q(kT)$

$$q(kT) = \sum_{i=1}^{L} b_i \hat{a}_{k-i} \neq f(\tau) \tag{4.1}$$

the slicer-input can be written including gain, colored noise n' and phaseshift τ as

$$y(kT+\tau) = r(kT+\tau) - q(kT) \tag{4.2}$$

$$= \tilde{w}(\tau)\Big[a_k v_k + \frac{1}{\tilde{w}(\tau)} \sum_{n=-7;n\neq 0}{}' a_{k-n} v_{k-n} \tilde{w}(nT+\tau) + \frac{n'(kT)v_k}{\tilde{w}(\tau)}\Big] - q(kT) \tag{4.3}$$

It has been stated in [17] that the value v for the gain can be regarded as slowly varying and therefore as a multiplicative constant in terms of the phase error for a first order approximation. The slicer-input is an inherently nonlinear function of the phaseshift τ because it is driven by recovered data. A feasible approach is the minimum-mean-square error (MMSE) timing recovery explained in [18]. MMSE time recovery adjusts the phaseshift τ to minimize the expected square error between the slicer-input and the correct symbol $\hat{a}_k$. In the presence of noise, estimate values are used; e_k denotes the error:

$$E\{e_k(\tau_k)^2\} = E\Big\{(y(kT+\tau_k) - \hat{a}_k \cdot w_0)^2\Big\} \tag{4.4}$$

1. **Direct gradient algorithm**

An expression for the phase error ϕ can be derived as

$$\phi_A = \nabla_{\tau k} = E\{\frac{\delta}{\delta\tau_k}[e_k(\tau_k)]^2\} \tag{4.5}$$

$$\phi_A = 2 \cdot E\{e_k(\tau_k) \cdot \frac{\delta y(kT+\tau_k)}{\delta\tau_k}\} \tag{4.6}$$

where

$$\frac{\delta y(kT+\tau_k)}{\delta\tau_k} = \sum_n a_{k-n} \cdot \frac{\delta\tilde{w}(nT+\tau_k)}{\delta\tau_k} \tag{4.7}$$

previous work [15] has shown that 4.7 can be simplified using

$$\frac{\delta\tilde{w}(nT+\tau_k)}{\delta\tau_k} = \tilde{w}'(nT+\tau_k) = \sum_{m;n\neq m}{}' \frac{\tilde{w}(nT+\tau_k)(-1)^{n-m}}{n-m} \tag{4.8}$$

With $w_0 = 1$, ϕ_A is rewritten as

$$\phi_A = 2 \cdot [(y(kT+\tau_k) - \hat{a}_k] \cdot \sum_n a_{k-n} \sum_{m;n\neq m}{}' \frac{\tilde{w}(nT+\tau_k)(-1)^{n-m}}{n-m} \tag{4.9}$$

Using this method directly would require a large number of multiplications to compute the derivative of $\tilde{w}(kT+\tau_k)$ and is therefore not suitable for direct applications. However, its performance was evaluated for several settings of the gain v in figure *4.2*. These plots were created using the expected values of table *3.2* for the symbols a_{k-n} as a fixed sequence. This is a fast method to obtain the curves and justified, since over a large number of runs the estimate for the mean value would also converge to this same mean value.

2. **Baud-rate technique**

A simple approximation to eqn. 4.9 whose result follows is described in [16].

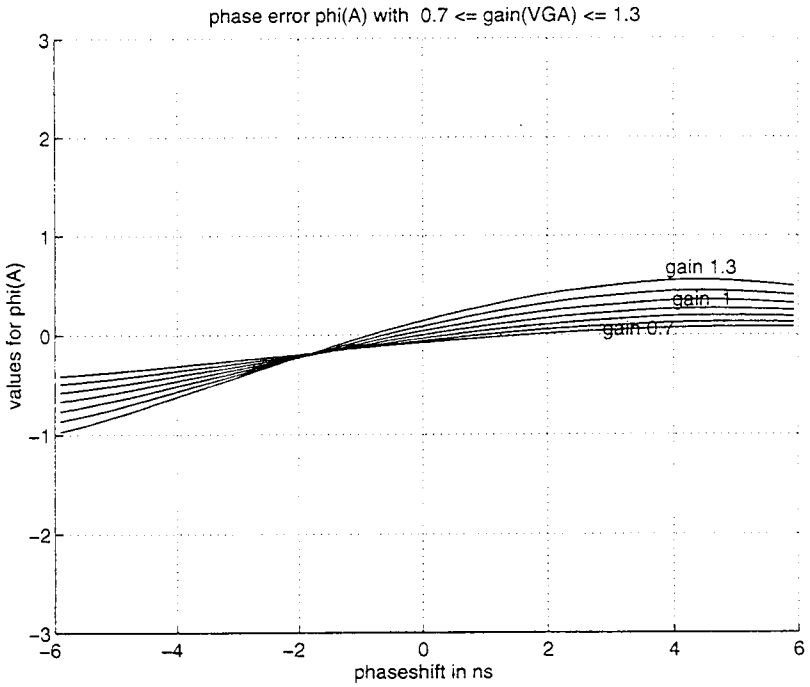


Figure 4.2. Phase error ϕ_A

$$\phi_B = -\hat{a}_{k-1}y(kT+\tau_k) + \hat{a}_k y((k-1)T+\tau_k) \tag{4.10}$$

In case of correct detection, $\hat{a}_k, \hat{a}_{k-1}$ are opposite in signs at transitions in MDFE, i.e.

$$\hat{a}_k = -\hat{a}_{k-1}$$

so 4.10 changes into

$$\phi_B = \hat{a}_k\Big(y(kT+\tau_k) + y((k-1)T+\tau_k)\Big) \tag{4.11}$$

A first-order estimate of the slicer-input as a function of timing phase is

$$y(kT+\tau_k) = \hat{a}_k \cdot 1 + e_k(\tau_k)$$

this leads to the following expression for the phase error

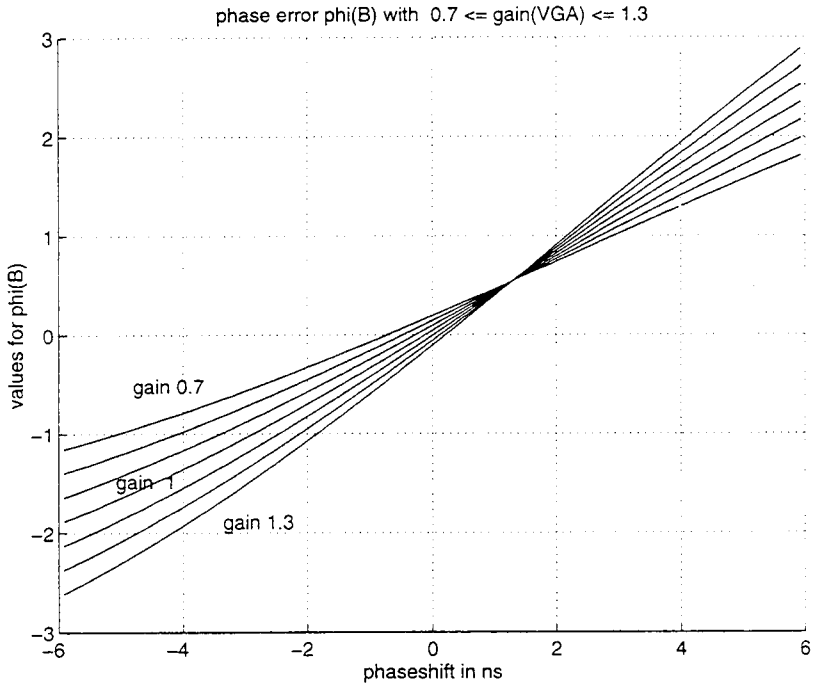


Figure 4.3. Phase error ϕ_B

$$\phi_B = -\hat{a}_{k-1}e_k(\tau_k) + \hat{a}_k e_{k-1}(\tau_{k-1}) \tag{4.12}$$

when a transition occurs the phase error is

$$\begin{cases} \hat{a} = -1 \rightarrow +1 : & \phi_B = e_k(\tau_k) + e_{k-1}(\tau_{k-1}) \\ \hat{a} = +1 \rightarrow -1 : & \phi_B = -e_k(\tau_k) - e_{k-1}(\tau_{k-1}) \end{cases}$$

under the assumption that $e_k(\tau_k) \approx e_{k-1}(\tau_{k-1})$ and with the signum-function $\mathrm{sgn}\{\cdots\}$ indicating the sign of the argument within the braces, this can be written as

$$\phi_B \approx 2 \cdot e_k(\tau_k) \cdot \mathrm{sgn}\Big(\frac{\delta y(kT+\tau_k)}{\delta \tau_k}\Big) \tag{4.13}$$

it easily can be seen that this has a similar structure to equation 4.6. The curves generated by this function are displayed in figure *4.3.*

3. **Fixed reference**

   A feasible alternative to the formula for ϕ_B can be attained by replacing the argument $y((k-1)T+\tau_k)$ in eqn. 4.11 with the ideal reference value. A scaling factor A normalizes the amplitude of the slicer-input around the transitions to ± 1. The above term can be substituted in 4.11 using

$$y((k-1)T+\tau_k) \approx \text{sgn}[y((k-1)T+\tau_k)] = \text{sgn}[a_{k-1}] = \hat{a}_{k-1}$$

   which leads for both possible combinations $\hat{a}_k, \hat{a}_{k-1}$ to the approximation

$$\phi_C = \hat{a}_k \cdot y(kT+\tau_k) - 1 \tag{4.14}$$

   This equation yields for transition events

$$\begin{cases} a = -1 \rightarrow +1: & \phi_C = +y(kT+\tau_k) - 1 \\ a = +1 \rightarrow -1: & \phi_C = -y(kT+\tau_k) - 1 \end{cases}$$

   In eqn. 4.14 just one value of $y(kT+\tau_k)$ is used which provides advantages in terms of circuit design for the detectors compared to the usage of two values in eqn. 4.11. A performance analysis with different gain settings is shown in figure *4.4*.

All three phase error expressions applying a gain value of $v = 1$ and SNR of -20dB are plotted with normalized gains with mean and standard deviation in figure *4.5* and figure *4.6*, respectively. Comparing the curves it is obvious to see that all concepts pass thru the origin. The expression for ϕ_A shows a poor linearity and monotonity behavior as well as a high standard deviation. Concepts ϕ_B and ϕ_C are similar in terms of linearity and their standard deviations show only slight differences. Having the goals of low power consumption and low complexity in mind, the third concept ϕ_C of eqn. 4.14 satisfies these principles best, as no addition of two variables, which

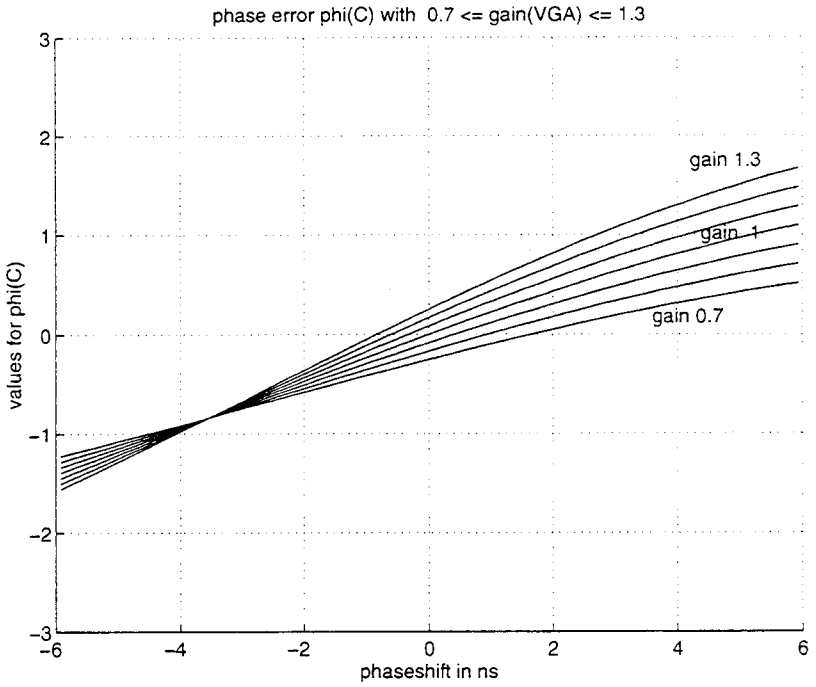


Figure 4.4. Phase error ϕ_C

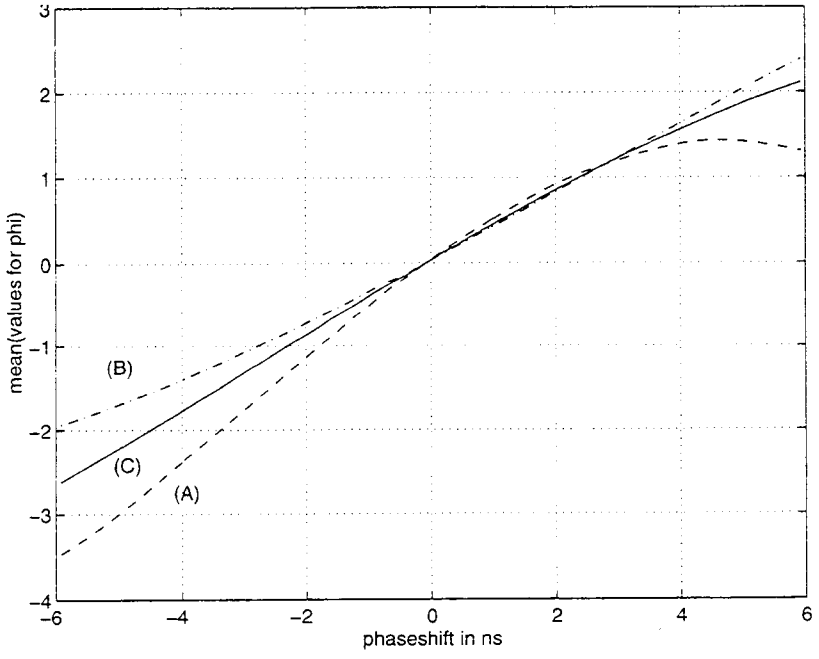


Figure 4.5. Phase error ϕ - mean

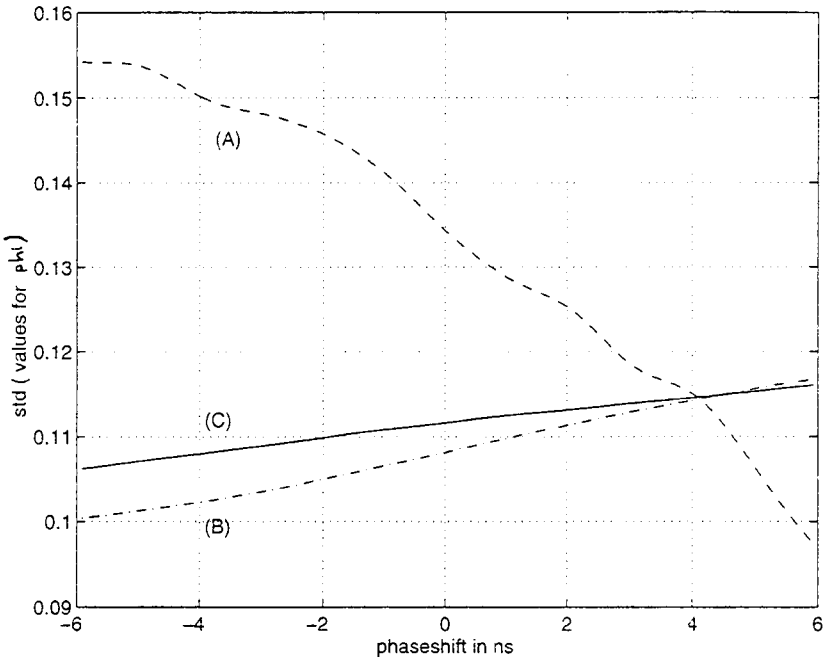


Figure 4.6. Phase error ϕ - std

will be carried out by summing of currents, has to be performed and therefore the magnitude of the current will be limited to this of one current alone. Furthermore, this also yields an effective decoupling of the circuits for phase and gain detection as will be seen in chapter 5. The selected concept ϕ_C also performs well during acquisition mode, when the known preamble sequence is being detected; the result is depicted in figure *4.7*.

4.1.2. Gaindetector

Gain updates should be generated from signals which have large amplitude as they leave the forward equalizer. From figure *2.7* it can be seen that the output of the forward equalizer is large just prior to a transition. The effect of a gain error is shown in figure *4.8*. A rectification has to be done to retrieve the correct sign for

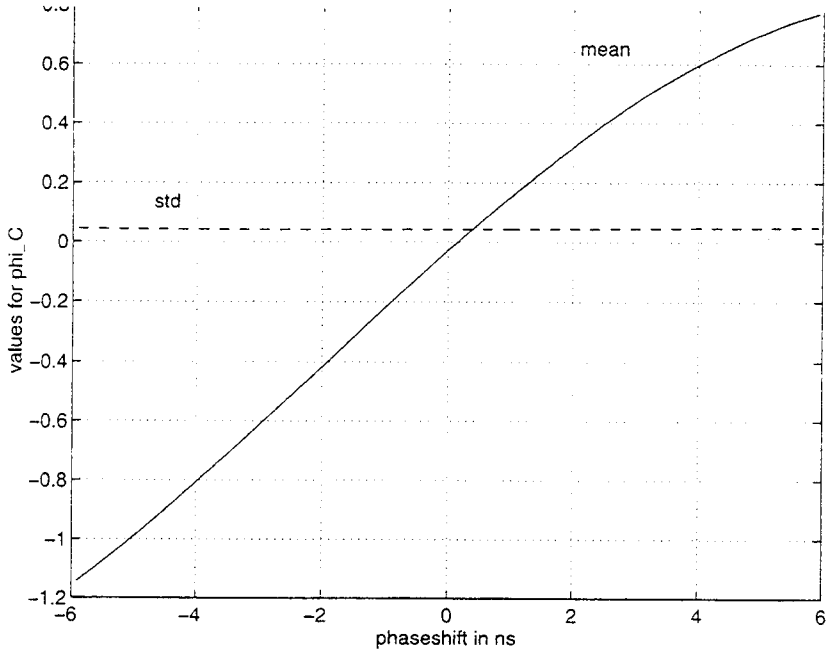


Figure 4.7. Phase error ϕ_C during Acquisition - mean and std

the gain error Δg because the direction of the transition has to be considered. This will be achieved by a multiplication with $\hat{a}_k$. Assuming that the gain is set too high, the amplitudes are overamplified leading to miscancellation of ISI in the summing node. A simple and straightforward error-function also derived from a minimum mean-square error renders an expression for the gain error. Starting with the error e_k we can write

$$e_k = y(kT) - \hat{y}_k \tag{4.15}$$

A gradient of the mean-square error is then obtained as

$$\Delta g \sim \nabla_v = E\{\frac{\delta}{\delta v_k}[e_k(v_k)]^2\} \tag{4.16}$$

$$\approx 2E\{e_k(v_k)\} \cdot \mathrm{sgn}\Big(\frac{\delta y(kT)}{\delta v_k}\Big) \approx 2E\{e_k(v_k)\} \cdot \mathrm{sgn}\Big(y(kT)\Big) \tag{4.17}$$

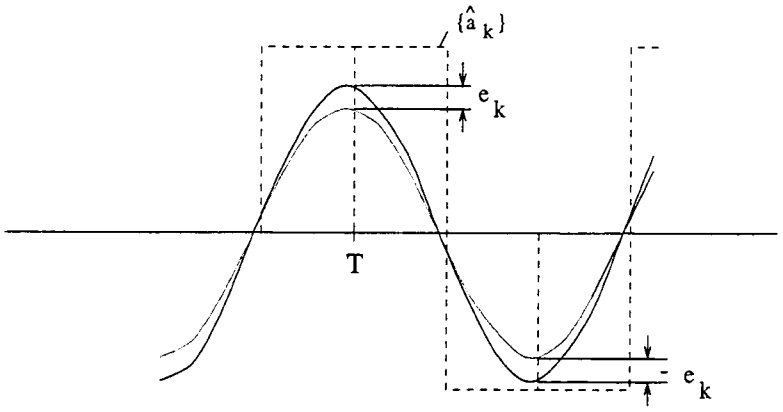


Figure 4.8. Example for gain error

The derivative of $y(kT))$ with respect to the gain v_k is replaced by the sign of the slicer-input as a first order approximation. This expression in eqn. *4.17* can be substituted in MDFE by $\hat{a}_k$. Therefore a proper equation for the gain error is provided as follows, where for the ideal slicer-input value holds $\hat{a}_k = \hat{y}_k$:

$$\Delta g = \hat{a}_k \cdot [y(kT) - \hat{y}_k] = \hat{a}_k \cdot y(kT) - 1 \tag{4.18}$$

The results of measuring the gain error according to eqn. 4.18 as a function of gain is shown in figure *4.9* for a range of phaseshifts. These curves are very linear for a large range of phaseshifts.

For a phaseshift of zero, the estimation of the gain error is approximately zero for a gain of $v = 1$. The statistical behavior is demonstrated in figure *4.10*, where the mean value and standard deviation were taken with an SNR of -20dB over 50 runs . The standard deviation shows very slight variation, while the mean value is identical to the noiseless simulation of figure *4.9*.

4.1.3. DC Offset detection

DC Offset can occur as a result of write current offset in the MR head as explained in [24]. A DC Offset results in a bit error performance degradation, as the

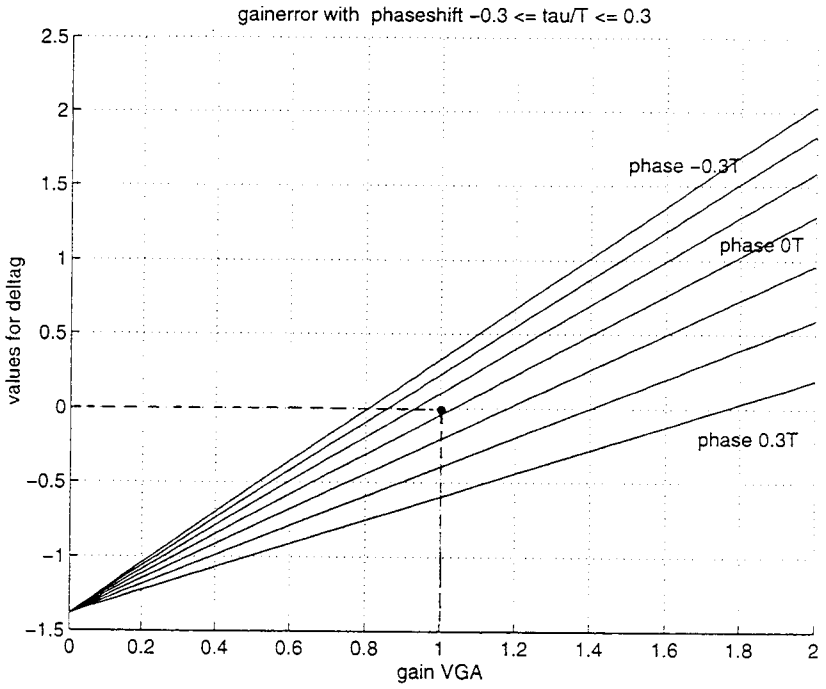


Figure 4.9. Gain error for different phaseshifts

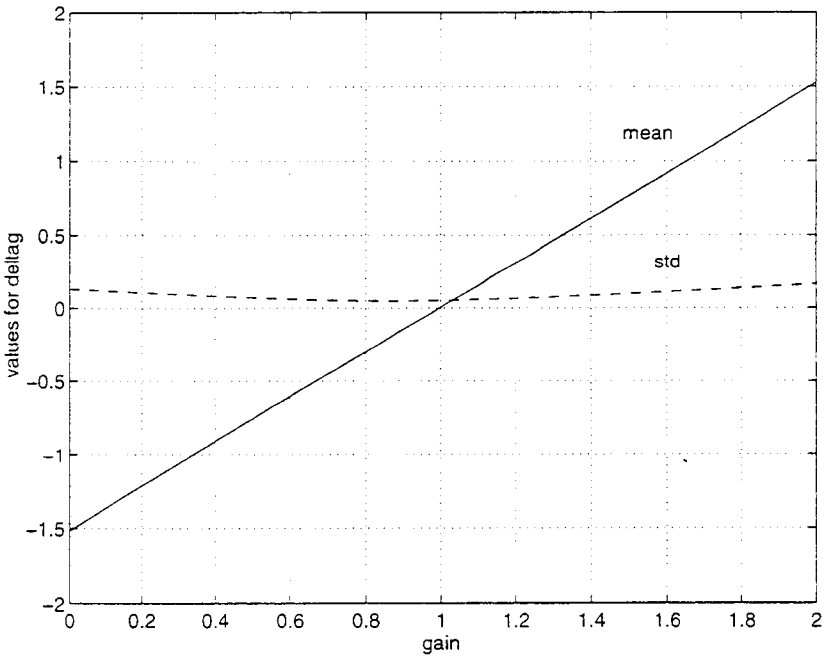


Figure 4.10. Gain error mean and standard deviation

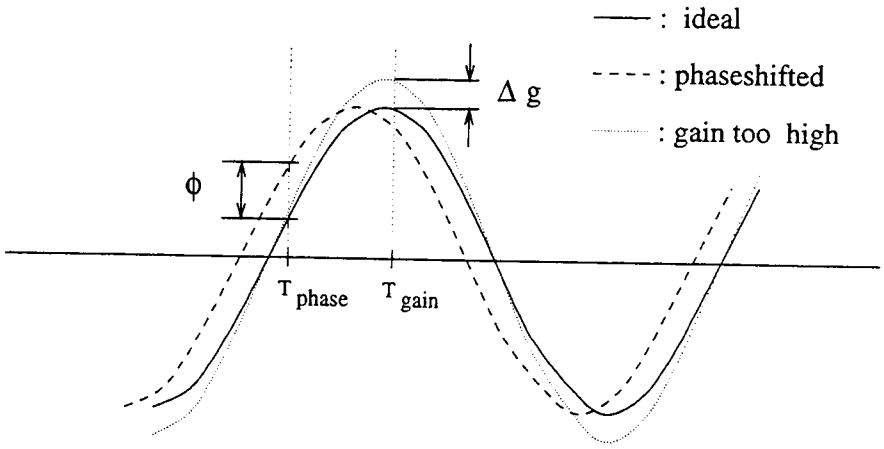


Figure 4.11. Selection of phase and gain error updating instants

margins for the zero- threshold slicer to the levels $+1$ and -1 will become smaller in one direction. A feasible detection may employ

$$\Delta_{DC} = \Big(y(kT + \tau_k) + y((k-1)T + \tau_k)\Big) \tag{4.19}$$

This formula is identical to the one for the phase error for positive transitions, however, as it does not contain $\hat{a}$, the result is a true indication for a dc offset error if the negative transition is taken into account as well.

4.1.4. Sampling instants for Phase- and Gain detection

Timing and gain errors are independent over time. They cannot be distinguished on a sample by sample basis. A phase error might show up as gain error and vice versa. But these interferences are rather small, resulting from the selection of the instants when phase and gain error updates are taken as shown in figure *4.11.* It shows the sinusoidal output $r(t)$ of the forward equalizer and the instants for taking phase and gain updates. The phase error is updated by slicer-input values

at instants T_{ph} in areas of low amplitude and high slope of the sinusoidal forward equalizer output curve. A change of amplitude does not have much effect whereas a phaseshift causes a large error signal. The gain error vice versa is updated at the instants T_g, where the amplitude is maximum and the slope very small, so that a gain different from one causes mainly gain error.

4.2. DIGITAL PHASE LOCKED LOOP FOR TIMING RECOVERY

The joint behavior of the PLL and AGC is a non-linear, highly correlated process, thereby analysis is difficult. For this reason, the whole system was simulated in MATLAB. The block diagram of the model used is provided in Appendix A. The SIMULINK toolbox offers a convenient way of implementing control systems on a block diagram level while allowing the opportunity of having customized Matlab functions. Data export and -import to/from the Matlab workspace is easily possible and thereby enabling output evaluation with the full Matlab facilities. The entire system comprised of forward and backward equalizer is completely represented in the Matlab-functional block *'combierr'* by impulse responses. The actual data are presented as input to the system as well as power-adjustable, bandlimited white noise. The bandlimiting hereby is introduced by a zero-hold function with length of one sampling interval. The phase of the sampling clock generated by the VCO is compared to the ideal phase generated by a digital clock with a staircase output; the VCO was modeled by cascading an inverting function which converts the frequency-information into a sampling time followed by a discrete-time integrator.

The automatic gain-control loop was realized by a gaindetector realizing eqn. 4.18 followed by an integrating filter. The output of this filter together with a constant nominal gain comprises the gain by which the readback signal is amplified.

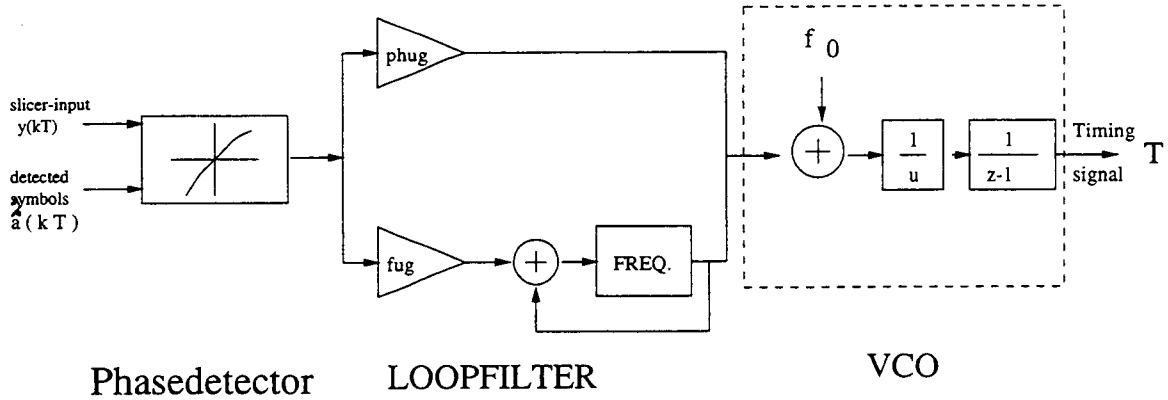


Figure 4.12. Architecture of the Loop filter for Timing Recovery

This is carried out within the system-function *'combierr'* which also processes the phaseshift information. The observed variables are *phdiff* for the difference between ideal and actual phase and *gain* as the current gain setting valid for the mainsample a_k.

4.2.1. Loop filter architecture for DPLL

This next section will deal with the design of the loop filter in the phase-locked loop. Conflicting objectives are fast settling time to zero-phaseshift and nominal gain and small steady-state error. The bandwith of the filter should not be unnecessarily wide, otherwise the influence of noise, especially high frequency noise, will get too high. Also the stability of the system should be preserved for phase ranges within a sampling interval around the point of zero-phase shift. The functionality of the loop filter is discussed in [19]. An architectural sketch is shown in figure *4.12*. The phase error ϕ generated in the phasedetector, is amplified by fug

which stands for "frequency-update-gain" and is integrated in the frequency register. The lower path of the filter takes care of phaseshifts of the signal due to underlying frequency shifts. In the upper path an amplification by "the phase-update-gain" *phug* takes place. Both paths are added to the reference voltage resembling the sampling frequency f_0. In the real system and also in the SABER-implementation, the VCO follows. The VCO is modelled by a block $1/u$ for conversion of frequency into timing information; the timing instants are obtained as the result of integration which leads to a staircase-like function for the phase in the discrete-time simulation. A simple model of the VCO can be approximated by a first-order Taylor expansion. The following equation holds for the signal ΔT after this element:

$$\Delta T = \frac{1}{f_0 + \Delta f} \approx \frac{1}{f_0 + \Delta f}\,|_{\Delta f=0} + \frac{-1}{(f_0 + \Delta f)^2}\,|_{\Delta f=0} \cdot \Delta f = \frac{1}{f_0} - \frac{1}{f_0^2} \cdot \Delta f \quad (4.20)$$

with $\frac{1}{f_0} = T_0$:

$$\Delta T = T_0 - \frac{1}{f_0^2} \cdot \Delta f \sim \Delta f \quad (4.21)$$

Now the equation for the integration within the VCO is written as

$$T_k = T_{k-1} + \Delta T \quad (4.22)$$

Applying the Z-transform for the loop filter, we get easily

$$\Delta f(z) = phug \cdot \phi(z) + \frac{fug}{1 - z^{-1}} \cdot \phi(z) \quad (4.23)$$

$$= (phug + fug) \cdot \frac{z - \frac{phug}{phug+fug}}{z - 1} \cdot \phi \quad (4.24)$$

Equations 4.21, 4.22 and 4.24 describe a second order discrete-time phase-locked loop. Transformation of the parameters to the actual loop filter coefficients are carried out by substituting

$$(phug + fug) = K \cdot \frac{10^6}{fs} \qquad \text{and} \qquad \frac{phug}{phug + fug} = a$$

As a starting point for investigations, the values suggested in [3] are taken as

$$\left.\begin{array}{l} phug = 2 \cdot 10^{-3} \\ fug = 2 \cdot 10^{-6} \end{array}\right\} \longrightarrow \left\{\begin{array}{l} K = 0.5 \\ a = 0.999 \end{array}\right.$$

The VCO reacts much slower to frequency variations than phase variation, because $fug \ll phug$. Simulations were performed using the program *Combisys* in MATLAB, measuring the phase difference $phdiff$ as a controlled variable. $phdiff$ is the difference between the sampling phase from the VCO and the ideal sampling phase. To compare different responses of the system, a suitable quantity has to be defined which focusses on both the steady-state error and the settling time. This is the motivation for selecting a costfunction in discrete-time domain as follows, commonly referred to in control engineering as Integral of Time-multiplied square value of Error (ITSE) criterion:

$$cost = \sum_k (phdiff)^2 \cdot (kT) \tag{4.25}$$

4.2.2. Results for uncompensated DPLL

A first series of investigations was done by applying a step in phase of 3.9ns. The noise power was calibrated such that the SNR at the input of the phasedetector equals -20dB for a setting of the system's noise power coefficient $p = 1$. A variation of the noise power with the gain K as parameter renders as results for the cost function figure *4.13*: Low values for K fail to respond quickly enough to the phase step and for that reason their costfunction is high; the PLL is not able to adequately respond to perturbations in the sampling clock. In the disk drive application, sampling clock variations are due to changes in the speed at which the disk spins. By increasing the size of K, a minimum of the cost function is reached when K is in range between

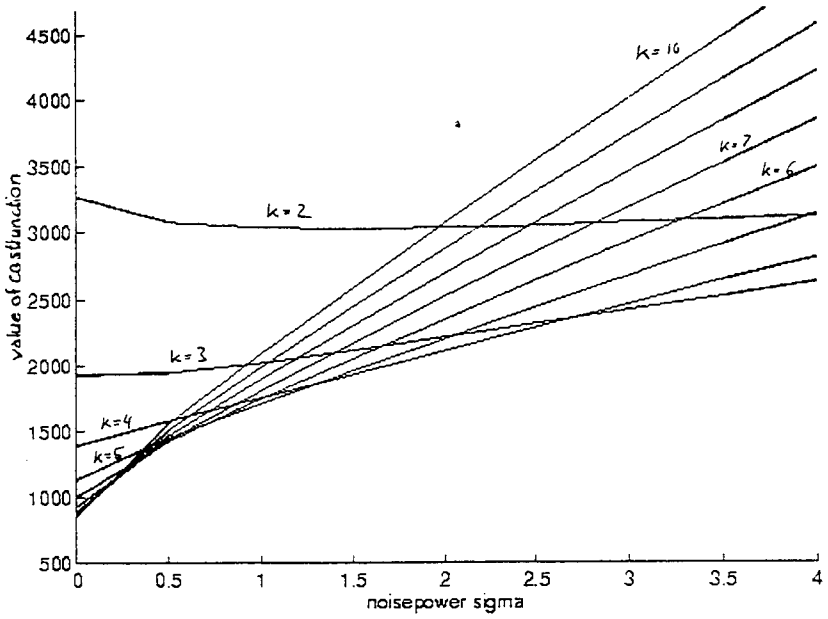


Figure 4.13. Cost function of noise, parameter K

6 and 7. Here, a good balance has been achieved between good settling behavior and low noise amplification. When K is larger than 7, the noise is amplified causing jitter in the sampling clock. Too large values for K may also cause the PLL to become unstable.

For the parameter a there is a trade off between overshoot in the stepresponse and steady state error. For small values of a in the range up to 0.95, an overshoot occurs after the first zero crossing before the signal settles in. This tends to happen faster the smaller the a values are. However, if a is below 0.5, oscillating grows large. When a is selected above 0.95, the overshoot becomes small, but the rise time, i.e the time to the first zero-crossing increases as well as the final settling time, which yields a steady state error. A joint variation of parameters a and K leads to a chart for the costfunction like figure *4.14*

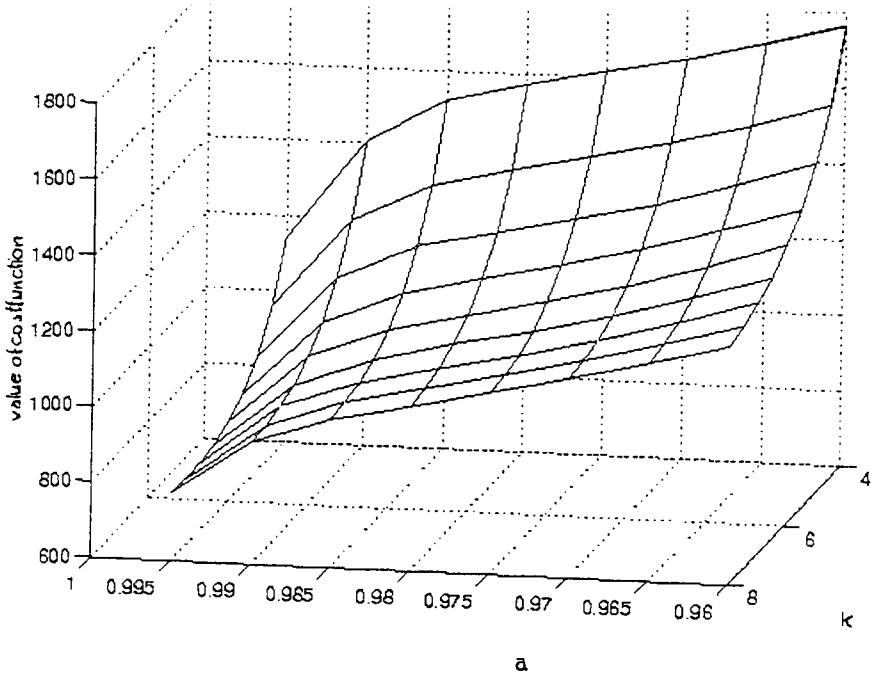


Figure 4.14. Cost function with parameters a, K

4.2.3. DPLL during Acquisition mode

During clock acquisition, phase errors are generated every other clock cycle. The samples that are used have high slope as they leave the forward equalizer, while the samples that are ignored are peaks. The simplified block diagram of the PLL is drawn in figure *4.15*. The block containing the sequence $\{10101\cdots\}$ indicates transition/no transition. In the cycles of no transitions, no phase update is taken and the value of phase error ϕ is set to zero. This leads to a power of two in the equation for the loop filter. With $K' = -\frac{K \cdot 10^6}{f_S^2}$, the functionality of the PLL is described by the following equations, starting with the loop filter:

$$\Delta T(z) = K' \cdot \frac{z^2 - a}{z^2 - 1}\phi(z) \tag{4.26}$$

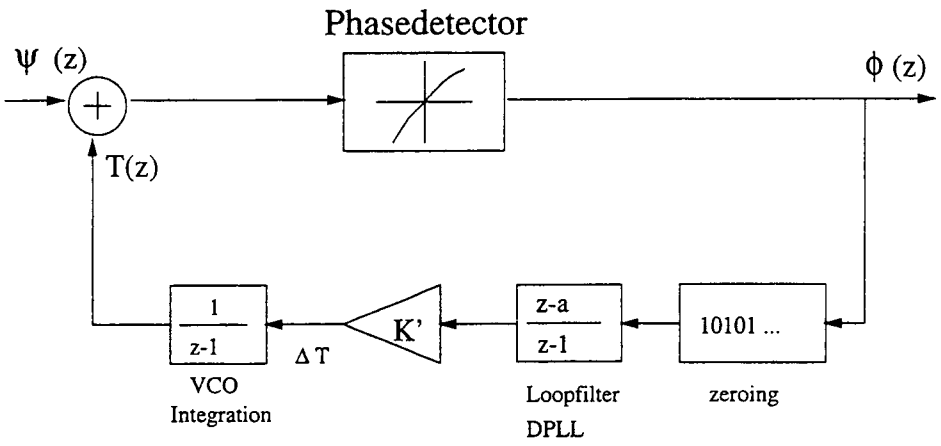


Figure 4.15. Block diagram of DPLL, during acquisition

Replacing $\sin\left(\frac{\omega_s}{4}(T_1+\tau)\right)$ in eqn. 3.22 by the approximation $[\sin(\frac{\omega_s}{4}T_1) + \sin'(\frac{\omega_s}{4}T_1)\cdot\frac{\omega_s}{4}\tau]$, the equation for the phase error is modified, starting from 4.14 into

$$\phi = \underbrace{\eta\cdot\sin(\frac{\omega_s}{4}T_1) - q_k}_{=1} + \eta\cdot\sin'(\frac{\omega_s}{4}T_1)\cdot\frac{\omega_s}{4}\tau \; - \; 1 \tag{4.27}$$

$$= \eta\cdot\cos(\frac{\omega_s}{4}T_1)\cdot\frac{\omega_s}{4}\tau \tag{4.28}$$

The VCO is modelled using eqn. 4.22 as

$$T_k = (k-1)\cdot T_0 + \Delta T_k \;\longrightarrow\; \Delta T_k = \Delta T_{k-1} - \frac{1}{f_S^2}\cdot\Delta f \tag{4.29}$$

The transfer function from $\tau(z)$ to $\phi(z)$ is

$$G(z) = \frac{\phi(z)}{\tau(z)} = \eta\cdot\cos(\frac{\omega_s}{4}T_1)\cdot\frac{\omega_s}{4}\tau \tag{4.30}$$

while the transfer function from $\phi(z)$ to $T(z)$ is

$$H(z) = \frac{T(z)}{\phi(z)} = \frac{K'}{z-1}\cdot\frac{z^2-a}{z^2-1} \tag{4.31}$$

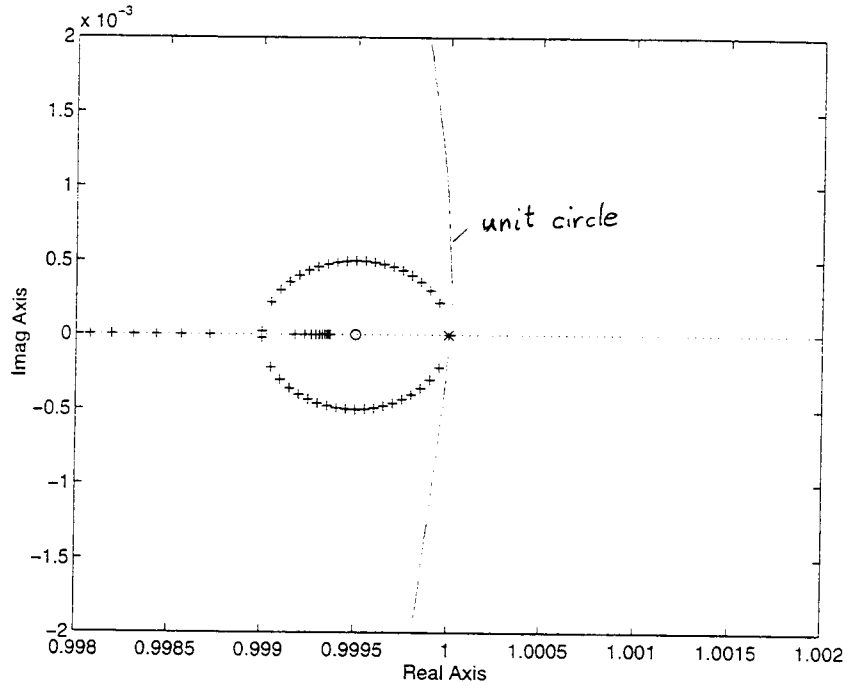


Figure 4.16. Root-locus diagram for DPLL open-loop during acquisition

The open loop transfer function is

$$\frac{T(z)}{\tau(z)} = G(z) \cdot H(z) \tag{4.32}$$

$$= \eta \cdot sin'(\frac{\omega_s}{4} T_1) \cdot \frac{\omega_s}{4} \cdot \frac{K'}{z-1} \cdot \frac{z^2-a}{z^2-1} \tag{4.33}$$

Open loop poles are from eqn. 4.33 located at $z_1 = 1$ and $z_{2/3} = \pm 1$. The root-locus diagram is shown in figure *4.16*. The steady-state error is calculated according to the expression which was taken from [21] p. 357

$$e^*_{SS0} = \lim_{z \to 1} \Big[(1 - z^{-1}) \cdot \frac{1}{G \cdot H(z) - 1} \cdot \frac{1}{1 - z^{-1}} \Big] \tag{4.34}$$

$$= \lim_{z \to 1} \frac{1}{G \cdot H(z) - 1} \tag{4.35}$$

$$= \lim_{z \to 1} \frac{(z-1)(z^2-1)}{\eta \cdot \sin'(\frac{\omega_s}{4} T_1) \cdot \frac{\omega_s}{4} \cdot K' \cdot (z^2 - a) - (z-1)(z^2-1)} \tag{4.36}$$

$$= 0 \qquad \text{for } a \neq 1 \tag{4.37}$$

As shown here, the steady-state error due to a step input is zero. The same is true for the steady-stae error due to a ramp input as shown below:

$$e^*_{SS1} = \lim_{z \to 1} \frac{T_S}{(1 - z^{-1}) \cdot G \cdot H(z)} = 0 \tag{4.38}$$

By this means we have demonstrated that the steady-state response to steps in phase and frequency can be exactly tracked. This is also valid for tracking mode, as the poles at $z = 1$ remain in case of a replacement of $(z^2 - 1)$ by $(z^m - 1)$. The PLL during tracking mode is not easily analysed as phase errors only are computed after transitions whose intervals are stochastic and thus the timing of phase updates as well. The closed loop transferfunction for the block diagram of figure *4.15* in acquisition mode is obtained from

$$\phi(z) = \frac{G(z)}{G(z)H(z) - 1} \cdot \psi(z) \tag{4.39}$$

which renders

$$\Phi(z) = \frac{\phi(z)}{\psi(z)} = \frac{\eta \cdot sin'(\frac{\omega_s}{4}T_1) \cdot \frac{\omega_s}{4} \cdot (z-1)(z^2-1)}{\eta \cdot sin'(\frac{\omega_s}{4}T_1) \cdot \frac{\omega_s}{4} \cdot K' \cdot (z^2 - a) - (z-1)(z^2-1)} \tag{4.40}$$

4.2.4. Phase-lag compensation of the DPLL

Due to some inherent delays in the response to a phase or frequency jump introduced by the fact that updates can only be taken when transitions occur, a varying amount of lag is present in the DPLL. In the area of discrete-time control phase-lag compensation can improve the response of the system [21] [22]. Phase-lag compensation increases the low frequency gain of the system while at the same time reducing the high frequency gain. Thus the high frequency noise entering the PLL is attenuated. Therefore the gain of the system can be increased. Phase-lag compensation adds a stage of the form

$$L(z) = \frac{z - z_0}{z - z_P} \quad \text{with} \quad 0 < z_0 < z_P < 1 \tag{4.41}$$

A continuous-time equivalent is determined by the bilinear W-transformation.

$$w = \frac{2}{T_s} \cdot \frac{z-1}{z+1} \tag{4.42}$$

which will allow the plotting of Bode diagrams:

$$L(w) = W0 \cdot \frac{1 + \frac{w}{w_Z}}{1 + \frac{w}{w_P}} \qquad w_Z > w_P \tag{4.43}$$

$$= W0 \cdot \frac{1 + \kappa\beta w}{1 + \beta w} \tag{4.44}$$

the parameters transform into

$$\beta = \frac{T_S}{2} \cdot \frac{1 + z_P}{1 - z_P} = \frac{1}{w_P} \tag{4.45}$$

$$\kappa = \frac{1 + z_0}{1 - z_0} \frac{1 - z_P}{1 + z_P} = \frac{w_P}{w_Z} < 1 \tag{4.46}$$

$$W0 = \frac{1 - z_0}{1 - z_P} \tag{4.47}$$

A Bode-plot showing the influence of w_Z and w_P is shown in figure *4.17*. In [23] it is asserted that the gain crossover of the uncompensated system can be moved to a lower frequency to achieve the desired phase margin. Phase-lag compensation places a zero to the left of a real-axis pole. To ensure good phase margin at the crossover frequency, the pole at $w = \frac{-1}{\beta}$ should be significantly below the unity gain frequency. An exhaustive search was done over w_p and w_z using the program *combisys* for SIMULINK within the MATLAB Software package. A detailled description of the used simulation system is given in Appendix B.

4.2.5. Results for compensated DPLL

The coefficients for the tracking-mode PLL were varied over the ranges stated in table *4.5*. Evaluation of the result was performed simulating the joint adjustment

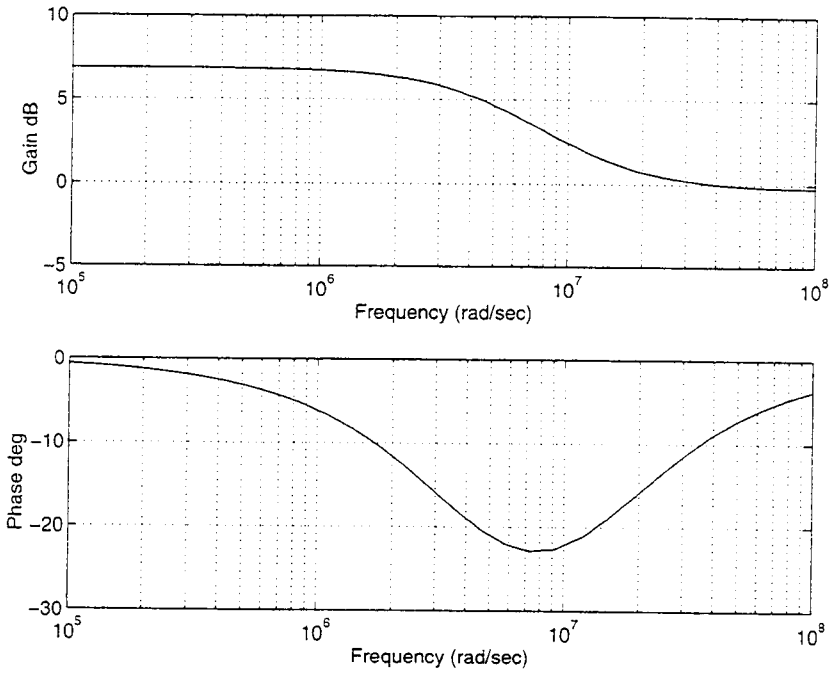


Figure 4.17. Bode plot of Phase-lag compensating stage $L(w)$

Coefficient	from	step	to
k	0.1	0.1	1.0
a	0.99	0.001	0.999
b ($= z_0$)	0.2	0.01	0.98
c ($= z_P$)	b+0.01	0.01	0.99

Table 4.5. Variation range for parameter search (DPLL, tracking mode)

Tracking	k	a	b	c	COST
(1T)	0.7	0.998	0.89	0.95	2.05
(2T)	0.7	0.998	0.95	0.99	2.24
(3T)	0.5	0.999	0	0	5.37

Table 4.6. Set of best coefficients (DPLL, tracking mode)

of phase and gain after a timing phase step of $\frac{\tau}{T} = 0.25$, applying the costfunction defined in equation 4.25. The SNR was set to -20dB. The best results were obtained for the settings listed in table *4.6.* The PLL was characterized using the settings in table *4.6.* The AGC was also enabled. Figure 4.18 shows the mean time-domain response of the PLL to a step in phase of $\tau = \frac{T}{4} \rightarrow \tau = 2.5$ns with a symbol period $T = 10$ns. An ensemble was generated by running the PLL 50 times and averaging the results. Similarly, the standard deviation of the timing phase which indicated clock jitter is plotted in figure *4.19.* For the settings named "(1T)", a fast response is observed and the steady-state error as well as the overshoot are minimal. In curve "(2T)" the settling time is lengthed by a dramatic undershoot and subsequent ringing. The response without compensation stage is fairly slow but does not oscillate. Coefficients $b = z_0$ and $c = z_P$ in the set "(1T)" relate to values κ and β in eqn. 4.43 via the W-Transform as

$$b = z_0 = 0.89 \rightarrow \kappa = 0.4406 \text{ and } c = z_P = 0.95 \rightarrow \beta = 39{\cdot}5e^{-9} \qquad \Longrightarrow W0 = 2.2$$

A similar search was conducted for the acquisition mode; the parameters providing good results in SIMULINK are listed in table *4.7.* The SIMULNIK transient responses are plotted for these settings of coefficients in *figure 4.20.* Phase-lag

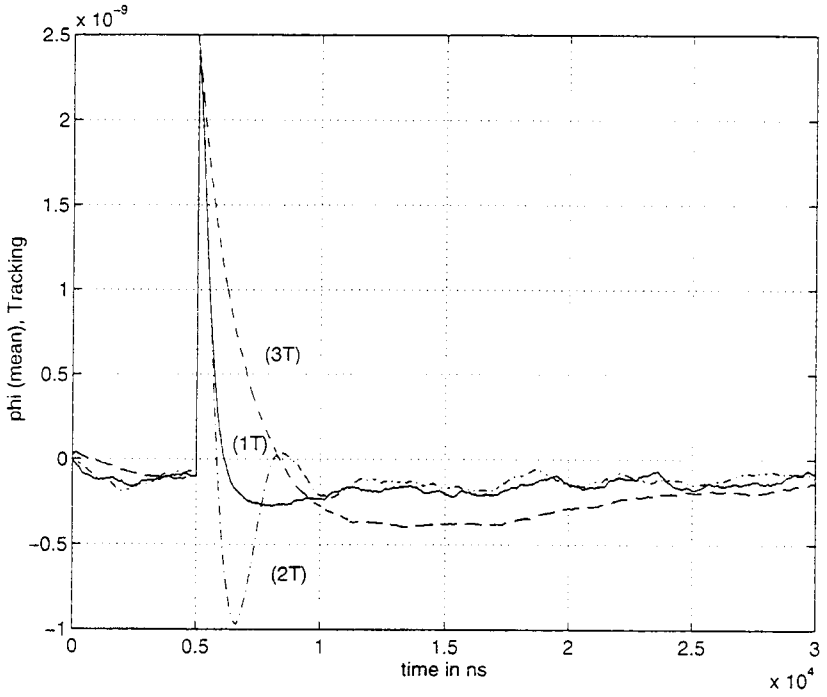


Figure 4.18. Phase step, mean values (Tracking mode)

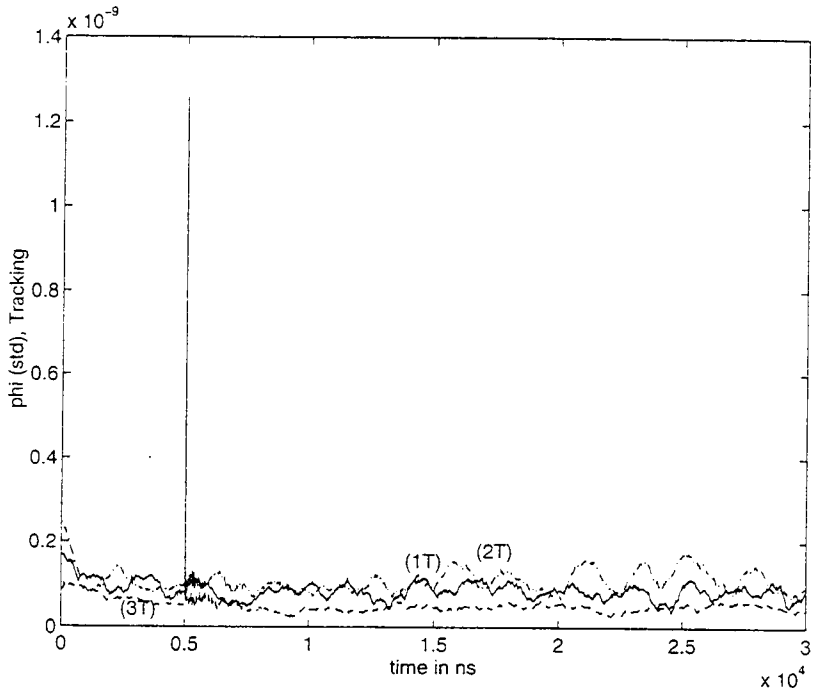


Figure 4.19. Phase step, standard deviation (Tracking mode)

Acquisition	k	a	b	c	COST
(1A)	5	0.999	0.89	0.95	1.76
(2A)	7	0.994	0.81	0.85	1.59
(3A)	5	0.999	0	0	1.85

Table 4.7. Set of best coefficients (DPLL, acquisition mode)

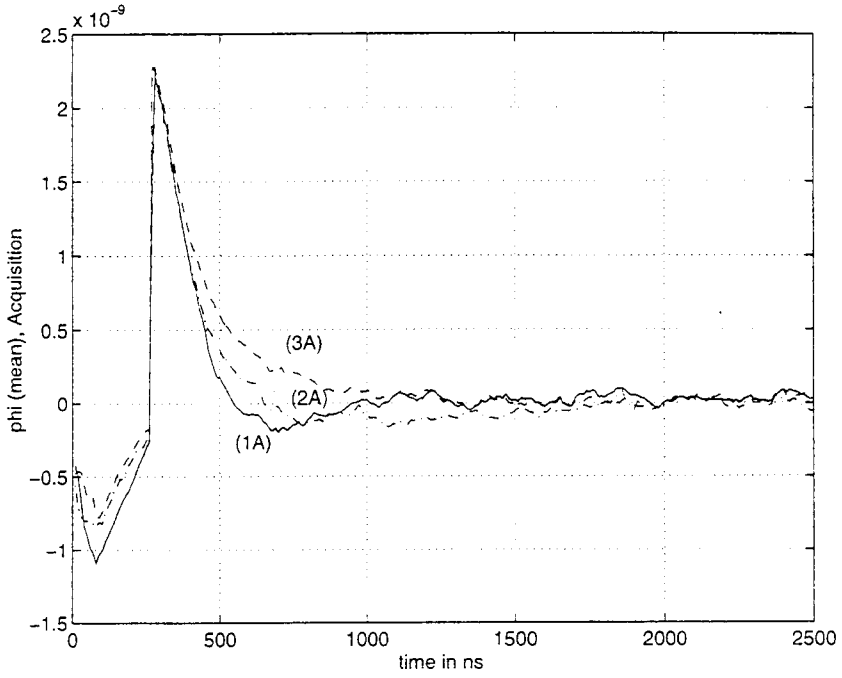


Figure 4.20. Phase step, mean values (Acquisition mode)

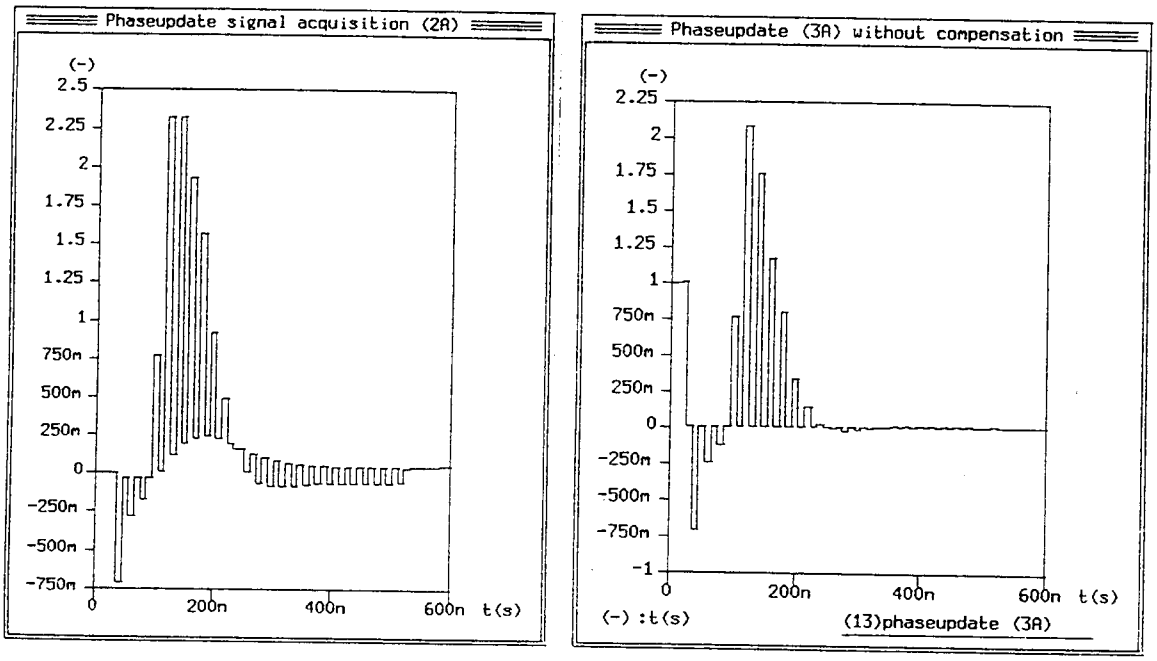


Figure 4.21. Phase error in SABER-Simulation during acquisition for sets (2A) and (3A)

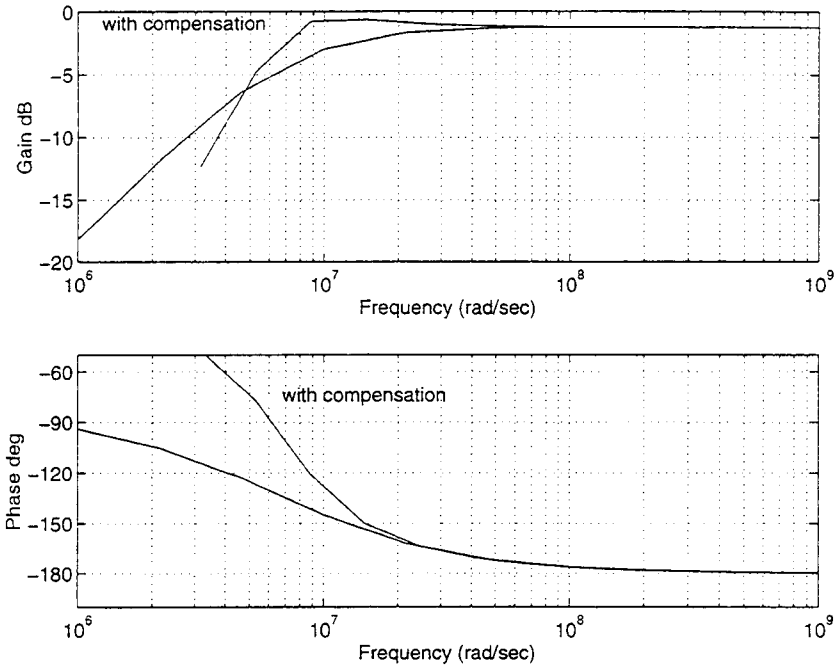


Figure 4.22. Bode plot of Phase-lag uncomp./compensated system $\Phi(z)$

compensation provides advantages when the updates are irregularly and largely spaced. However, in the acquisition mode more memory in the system introduced by the phase-lag compensation stage implies slower settling time if operated in a real acquisition process, simulated with SABER, as can be seen from 4.21. Therefore the phase-lag compensation should be disabled during acquisition mode and the gain K be switchable between acquisition and tracking mode. Extra complexity is introduced into the system by the addition of the phase-lag compensation stage. However, the faster responses during tracking mode justify this extra expense. The Bode plots for the both uncompensated and compensated system $\Phi(z)$ of eqn. *4.40* are shown in figure *4.22*. The plots were performed without the scaling factor $\frac{w_S}{4}$ in the numerator. From these Bode plots it is visible, how the gain is enhanced

and therefore a higher stability margin achieved, while the higher frequencies are attenuated.

4.3. AUTOMATIC GAIN CONTROL

The next section will deal with the design of the loop filter in the automatic gain control. Gain updates are performed when transitions have occured and are taken at the instants T_g in figure *4.11*. The loop filter carries out an integration and provides a gain kg. No dependencies on derivatives of time are expected for the gain, so the loop filter is designed using

$$\Delta G(z) = \frac{kg}{z-1} \cdot \Delta g(z) \tag{4.48}$$

After this filter, a constant nominal gain is added and this sum renders the amplification factor for the forward equalizer. The multiplication actually realized however causes some problems for linear control analysis.

4.3.1. AGC during Acquisition

Transitions occuring every other clock cycle lead to a gain-update on every second sampling period; otherwise the updating value is set to zero. The simplified block diagram is drawn for this case in figure *4.23*: Zeroing every second gaindetector output is contained in the subsequent equation by a power of 2 for z:

$$\Delta G(z) = \frac{kg}{z^2-1} \cdot \Delta g(z) \tag{4.49}$$

The whole system is described by the following equations:

$$\Delta g = [\, v \cdot sin(\frac{\omega_s}{4} T_1) - \underbrace{q\big(\frac{\omega_s}{4} T_1\big)}_{=const.}] \; - \; 1 \tag{4.50}$$

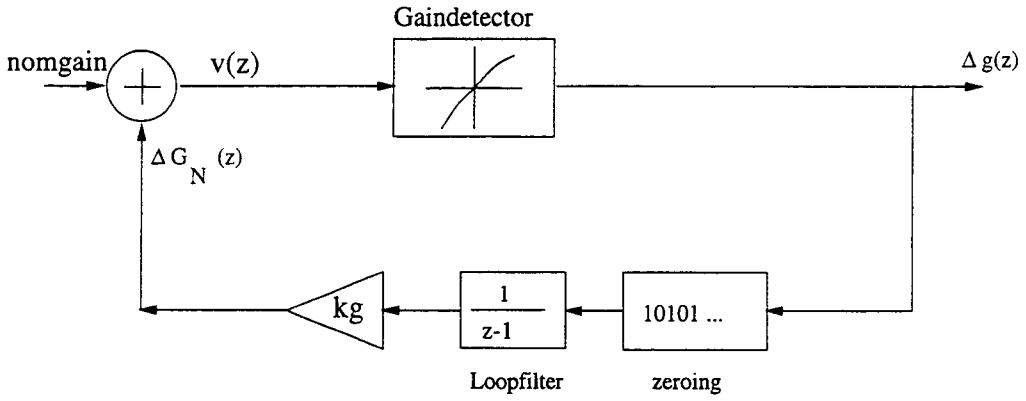


Figure 4.23. Block diagram of AGC, during acquisition

Using the z-Transform

$$\Delta g(z) = v \cdot sin(\frac{\omega_s}{4}T_1) - [1 + q(\frac{\omega_s}{4}T_1)] \cdot \frac{z}{z-1} \tag{4.51}$$

$$\Delta G_N(z) = \frac{kg}{z^2-1} \cdot \Big[v \cdot sin(\frac{\omega_s}{4}T_1) - [1 + q(\frac{\omega_s}{4}T_1)] \cdot \frac{z}{z-1} \Big] \tag{4.52}$$

The expression for $\Delta G_N(z)$ can be considered an open loop response to an input signal v.

4.3.2. Results for AGC

Phase-lag is generated in the loop for the AGC as well by updating the gain only after transitions. It seems feasible to introduce a phase-lag compensation block like the one used for the DPLL:

$$LG(z) = \frac{z-bg}{z-cg} \qquad \text{with } bg < cg \tag{4.53}$$

Simulations were performed with the SIMULINK as a joint adjustment of phase and gain. Evaluations were based on the cost function defined in 4.25 after a gain

kg	$bg = 0/cg = 0$	0.72/0.79	0.83/0.88	0.89/0.94	0.92/0.97
0.01	5.93	4.67	4.76	3.42	3.24
0.02	3.37	2.45	2.60	2.47	2.42

Table 4.8. Cost function for AGC coefficients (tracking mode)

	kg	bg	cg	COST
(1T)	0.02	0	0	3.37
(2T)	0.02	0.72	0.79	2.45
(3T)	0.02	0.89	0.94	2.47

Table 4.9. Best sets for AGC coefficients (tracking mode)

step of 0.2 with a SNR of 20dB in tracking mode. After a big parameter search, the coefficients listed in table *4.8* with their values for the cost function were examined statistically in a larger number of runs for each set. Including the shape of the curves into the performance evaluation, the following sets of coefficients are chosen for a graphical visualization: The transient responses of the joint phase and gain adjustment after a gain step are plotted in figure *4.24* and *4.25*. The set (3) performs slightly faster than (1) and (2); the steady state is found to be virtually identical for all three plots of the mean values. Implementing an additional stage has to be well justified by the improvement accomplished by its insertion, as extra expenses in terms of complexity, area and power consumption are related. Comparison of the results for the cost function in table *4.8* shows just a small enhancement of a factor 1.39 for the effect of the compensational stage. Before a decision about inserting a phase-lag compensation stage is made, the acquisition

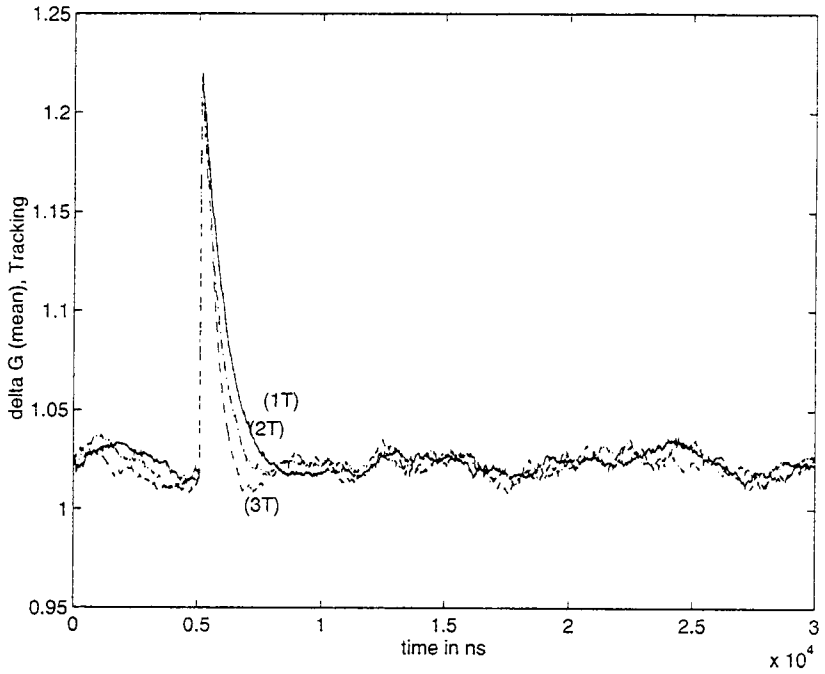


Figure 4.24. Gain step, mean values (tracking mode)

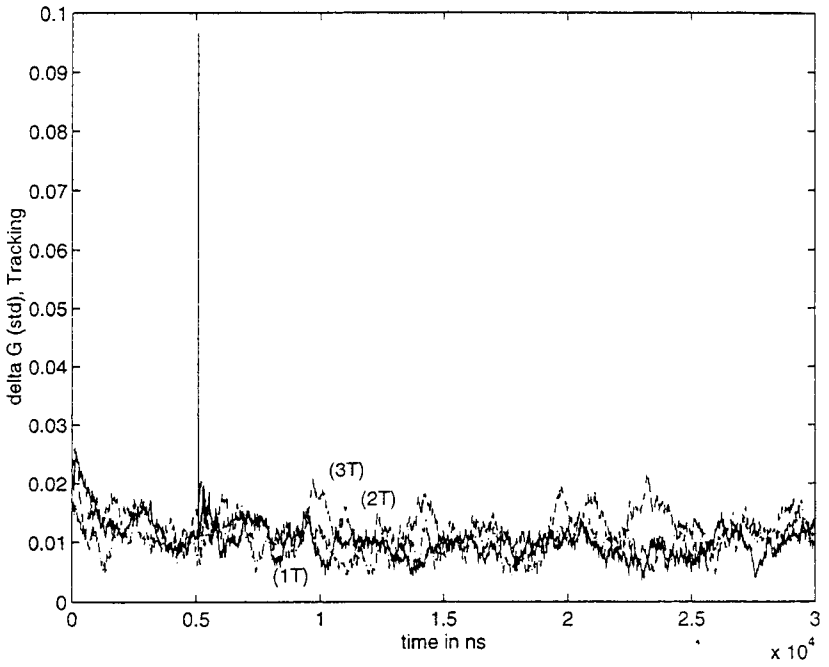


Figure 4.25. Gain step, standard deviation (tracking mode)

	kg	bg	cg	COST
(1A)	0.2	0	0	5.79
(2A)	0.1	0.89	0.94	9.30
(3A)	0.2	0.89	0.94	9.19

Table 4.10. Best sets for AGC coefficients (Acquisition mode)

mode is evaluated as well. The transient behavior after a gain pulse of 0.2 was examined with an SNR of 20dB. Sets of coefficients yielding the best results for the acquisition mode are shown in table *4.10*. Including the shape of the curves into the performance evaluation, the following sets of coefficients are chosen for a graphical visualization: The charts are given as figure *4.26*. The response (1A) without any compensation exhibits the best trade off between settling speed and an overshoot at the top. This behavior suggests omitting an additional stage for phase-lag compensation, especially if the additional implementation costs are considered. The best choice for the filter of the AGC are the coefficients

$$k = 2 \text{ for acquisition} \quad \text{and} \quad k = 0.2 \text{ for tracking}$$

4.4. JOINT SETTLING OF PHASE AND GAIN

With the filters designed it is possible to obtain a dynamic behavioral chart by extracting the values $phdiff$ and $gain$. Various pulses for gain and phase were selected. The obtained trajectories are shown as figure *4.27*.

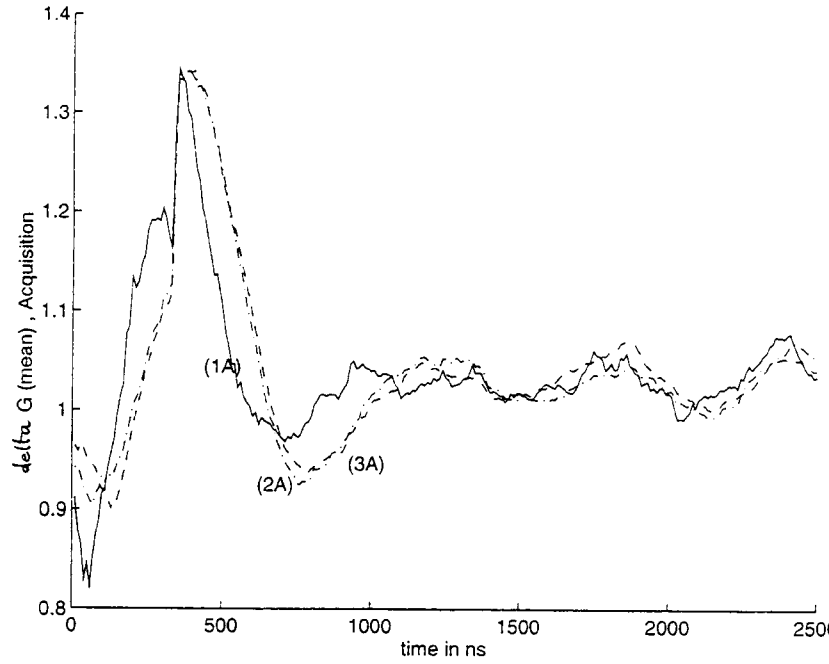


Figure 4.26. Gain step, mean values (Acquisition mode)

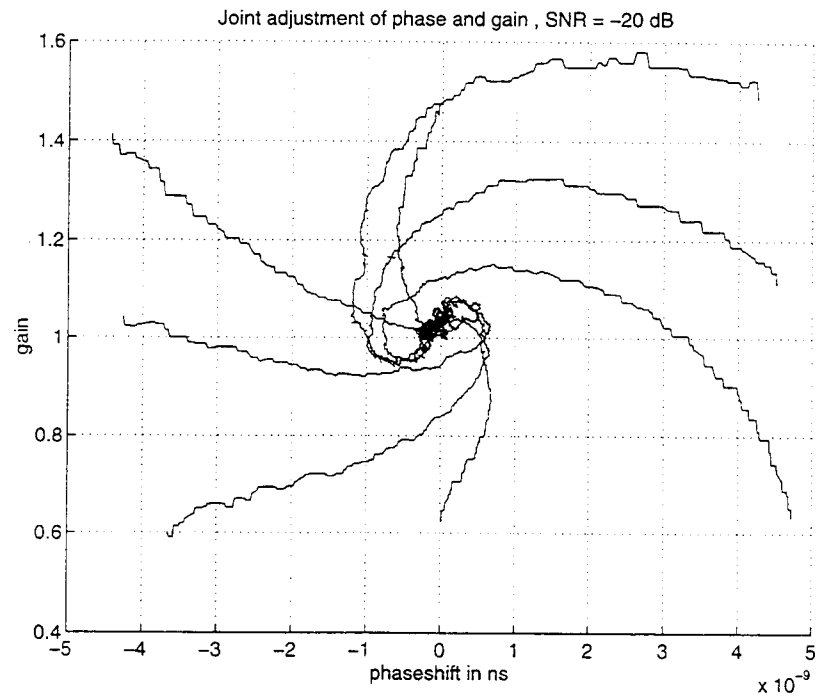


Figure 4.27. Joint adjustment of phase and gain - trajectories

5. HARDWARE IMPLEMENTATION FOR DETECTION OF PHASE AND GAIN

This chapter examines hardware implementation issues for the phase-, gain- and dc offset detection. Architectures are presented using analog circuitry. The necessary operations are additions, subractions and switching which are all fairly well manageable in CMOS technology. The proposed circuits operate in current mode and thus can be designed using CMOS.

5.1. SI-CIRCUITS

Since its introduction, the current copier technique has been implemented in various applications such as data converters and filters. Enormous complexity is available in state-of-the-art CMOS processing and hence an integration of complete systems has been made possible. As the level of integration rises, the scaling of feature sizes into the sub-micron range is likely to demand lower working voltages, as the issue of power consumption and cooling becomes more and more serious. A supply voltage of 3.3V is likely to become a future industry standard. Opamps and analog switches required to operate in the voltage domain will therefore suffer. Future analog circuits for VLSI applications have to adopt strategies capable of operating at low voltages. A sampled data technique called switched-current circuits was proposed for that purpose in [26]. Switched-current circuits are based on the principles of current mirroring and copying. A basic current copier cell displayed in figure *5.1* consists of a single MOSFET with switches implemented as MOS transitors. When $S1$ is closed, the gate-to-source voltage V_{GS} is adujsted by charging up

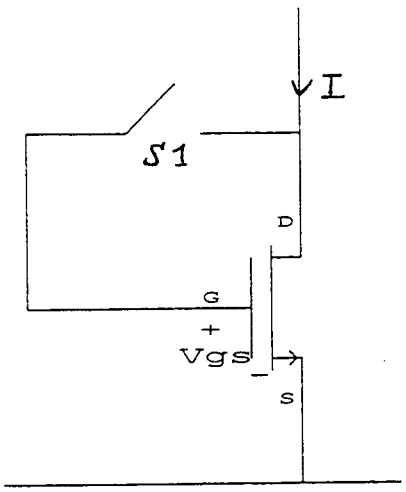


Figure 5.1. Current copier cell

the gate-capacitance, until the current I is passed through the transistor. When the switch is opened, the charge remains on the gate capacitance and by this means the current I is "stored" in this basic memory cell, though there are some shortcomings like charge-injection caused by the opening of the switch. An important advantage switched-current (SI) circuits have over switched-capacitor (SC) circuits is that they do not require linear capacitors. In addition, there is no need to completely charge or discharge the capacitances in the signal path. These circuits provide the necessary speed, because the symbol timing interval is only 10ns long. The power consumption is comparatively low in integrated switched-current circuits. Work is being done on the summing-node, the comparator and the forward and backward equalizer. In this chapter an analog circuit approach for generating phase, gain and dc offset errors will be presented together with the corresponding timing for the correct sampling and switching.

	A	B	C	D
TH 1	5	0	0	0
TH 2	0	5	0	0
TH 3	0	0	5	0
TH 4	0	0	0	5

Table 5.11. Commutator signaling

5.2. SAMPLING ARRAY AND SWITCHING

5.2.1. Track-and-Hold stages

Analog signals are desired as output of the AGC and DPLL. Since the slicer-input is already in sampled analog form, an entire analog path for the timing recovery circuitry and automatic gain control is feasible. Thus a strategy in which a bank of Track-and-hold stages is used in conjuntion with a finite state machine to generate the requisite phase, gain and dc offset information is employed. These error-signals have been formulated in such a way that simple current-steering principles can be utilized. A current-mode Track-and-hold is implemented by sampling the gate voltage of a signal carrying transistor onto the gate of a mirroring device. Figure *5.2* shows a differential Track-and-hold.

Sampling of the slicer-input is done by 4 Track-and-holds (TH), realized as fully-differential, low power switched-current circuits. The commutator, whose state-diagram is shown in table *5.11*, sequences through the bank of TH's such that each one samples every fourth symbol. When the corresponding controlling signal is high, the switches at the intersection of the branches labeled I_1, I_2, I_3 and I_4 and the

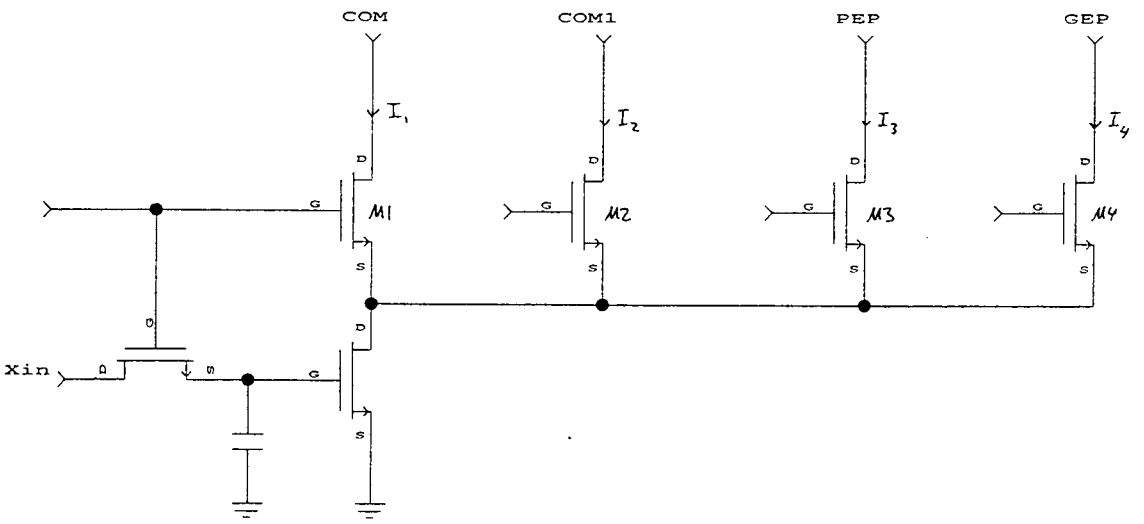
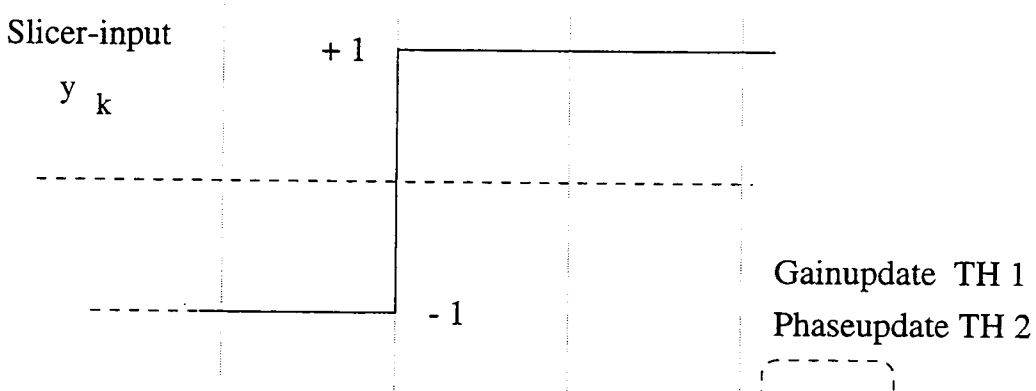


Figure 5.2. Track-and-Hold circuit

outputs of the Track-and-holds close. For a better understanding of the operation of the Track-and-holds, we monitor the operations of TH1 and TH2. The timing relation between the slicer-input, the detected signals $\hat{a}_k$ and the controlling signals for the Track-and-holds are depicted in figure *5.3*, indicating a positive transition from $\hat{a}_{k-1}$ to $\hat{a}_k$.

1. Starting with a slicer-input of y_{k-1}, the signal A is high. So TH1 samples the slicer-input y_{k-1} in state COM while the drains of the MOS transistors comprising TH1 are tied off to a reference voltage. The drains of M_1, M_2, M_3 and M_4 are therefore at the same potential. TH2 has its output node GEP connected to the subsequent gain detector circuit.

2. When A goes low, the slicer-input signal is sampled and the comparator begins to resolve the input into a bit resembling the decision $\hat{a}_{k-1}$. During B, we cannot do anything with the signal in TH1, because its corresponding decision



Slicer-input	y_{k-1}	y_{k}	y_{k+1}	...
Detected symbol	...	a_{k-1}	a_{k}	...
T H 1	COM	COM1	PEP	GEP
T H 2	GEP	COM	COM1	PEP

Figure 5.3. Timing of slicer-input and phase/gain detection

$\hat{a}_{k-1}$ is unknown. Thus it cannot be determined whether a transition has occured. Therefore the drains of the transistors in the Track-and-hold are tied off to a reference voltage during state $COM1$. TH2 samples the slicer-input y_k in this commutator period.

3. When the control signal C is high, the output of TH1 in state PEP may be used to generate a phase or dc offset error. In this example, we do not generate a phase error, as the slicer-input y_{k-1} before a transition is not used for phase error updating. TH2 is in its holding phase $COM1$.

4. In the next commutator cycle, TH1 in state GEP can be used to generate a gain error, while TH2 in PEP can be used for phase error. The switch connecting M_4 of TH1 to the input node of the gain detector circuitry is now closed and thus a gain error on the slicer-input value y_{k-1} can be done. At the same time a closed switch between M_3 of TH2 and the input node of the phase detector circuitry makes a phase update using the slicer-input value y_k possible. This is done in accordance with the rules for taking the sample values stated in chapter 3.

To simplify the logic and the design of the circuits implementing the various error detectors, the outputs of the Track-and-holds are always connected. Glitches during switching do not have a negative impact as they do not change the voltages stored on the (unconnected) gate-source capacitances.

5.2.2. Array of switches

The objective of the Track-and-hold stages and the detection circuits is to provide an analog implementation for the signal processing required to determine phase and gain errors, computed in 4.11 and 4.18:

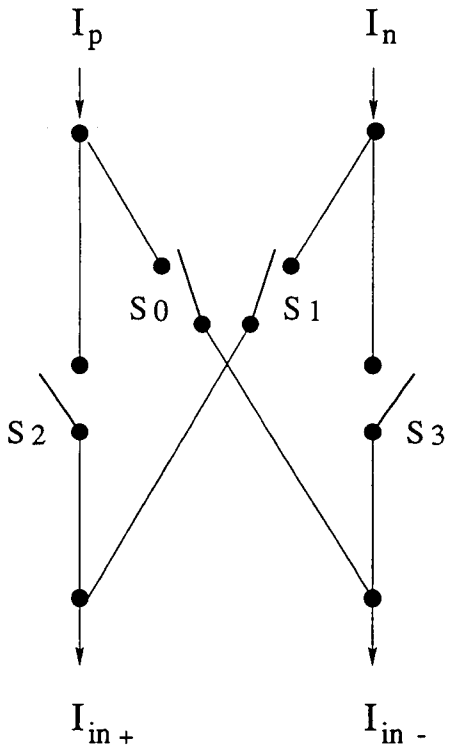
$$\phi_C = \hat{a}_k \cdot y(kT) - 1$$

$$\Delta g = \hat{a}_{k-1} \cdot y((k-1)T) - 1$$

Both equations have a similar structure, with the difference being that the gain error is taken from the slicer-input value before the transition whereas the phase error refers to the symbol after the transition, i.e. one clock cycle later, indicated by indices $(k-1)$ and k. From figure *5.3* we note that the phase and gain errors are computed simultaneously; this is during the clock cycle where the detected symbol $\hat{a}_k = -\hat{a}_{k-1}$ is present at the slicer-output. Therefore equation 4.18 for the gain error is rewritten as

$$\Delta g = -\hat{a}_k \cdot y((k-1)T) - 1 \tag{5.1}$$

Realization of the rectification $\pm\hat{a}_k$ is achieved by introducing the array of switches shown in figure *5.4* at the input of each detector circuit. Timing of the switches is displayed in figure *5.12*. When no transition has occurred, all four switches are "ON". Assuming that I_{in+} and I_{in-} drive equal impedances, the differential current is zero. This corresponds to the zero output in the block level diagram in this case. Outputs I_{in+} and I_{in-} are delivered as fully differential currents to the inputs of the detector stages described in the next section. The switching signal *Petrans* is generated for steering the switches of the dynamic current copiers within the detector circuitry itself. It is in the "ON" position after a transition has occured



	S 0/S 1	S 2 /S 3
phase detector	P+	P-
gain detector	P-	P+

Figure 5.4. Array of switches for phase- and gainerror detector

	$\hat{a}_k > \hat{a}_{k-1}$	$\hat{a}_k = \hat{a}_{k-1}$	$\hat{a}_k < \hat{a}_{k-1}$
P_+	ON	ON	OFF
$P\_$	OFF	ON	ON
$Petrans$	ON	OFF	ON

Table 5.12. Timing signals for switches

and enables current copying to the output of the detector. This procedure allows the updating circuitry to be operated as Track-and-holds.

5.3. DETECTOR CIRCUIT

5.3.1. Architecture

The same circuit topology can be used for generating both the phase and gain error due to the similarity in the equations 4.11 and 4.18. The topology is depicted in figure *5.5*. The fully-differential circuit topology proposed in this thesis provides first-order cancellation of clock-feedthrough/charge-injection effects and power-supply rejection ratio (PSRR). The input current I_{in+} and I_{in-} are translated into voltages on the gates of transistors $M1$ and $M5$. When a transition occurs, switches $sw12$ and $sw56$ close thereby sampling the gate voltages of $M1$ and $M5$ onto $M2$ and $M6$ respectively. Ideal switches are used in the initial simulations and they are replaced later by NMOS devices. When the switches open, the currents in the middle branches are therefore kept constant, only affected by a small amount of charge-injection in case of MOS switches. All current mirrors in figure *5.5* use cascoding to reduce the channel-length modulation. The current flowing through $M6, M11, M10$ is mirrored onto the gates of $M9$ and $M12$. The basic mirroring blocks including cascoding stages are symmetric in their sizes. For reasons of symmetry transistors $M9 - M12$ are implemented as p-channel devices, while the other mirroring blocks are implemented as n-channel devices. The output current I_{out} of the stage flows over a voltage source, steering a current-controlled voltage source modelling a low-impedance output stage following. This output signal can easily be sampled during the hold mode for further processing in the PLL and the AGC, respectively. The constant -1 in equations 4.11 and 4.18 is considered as a common

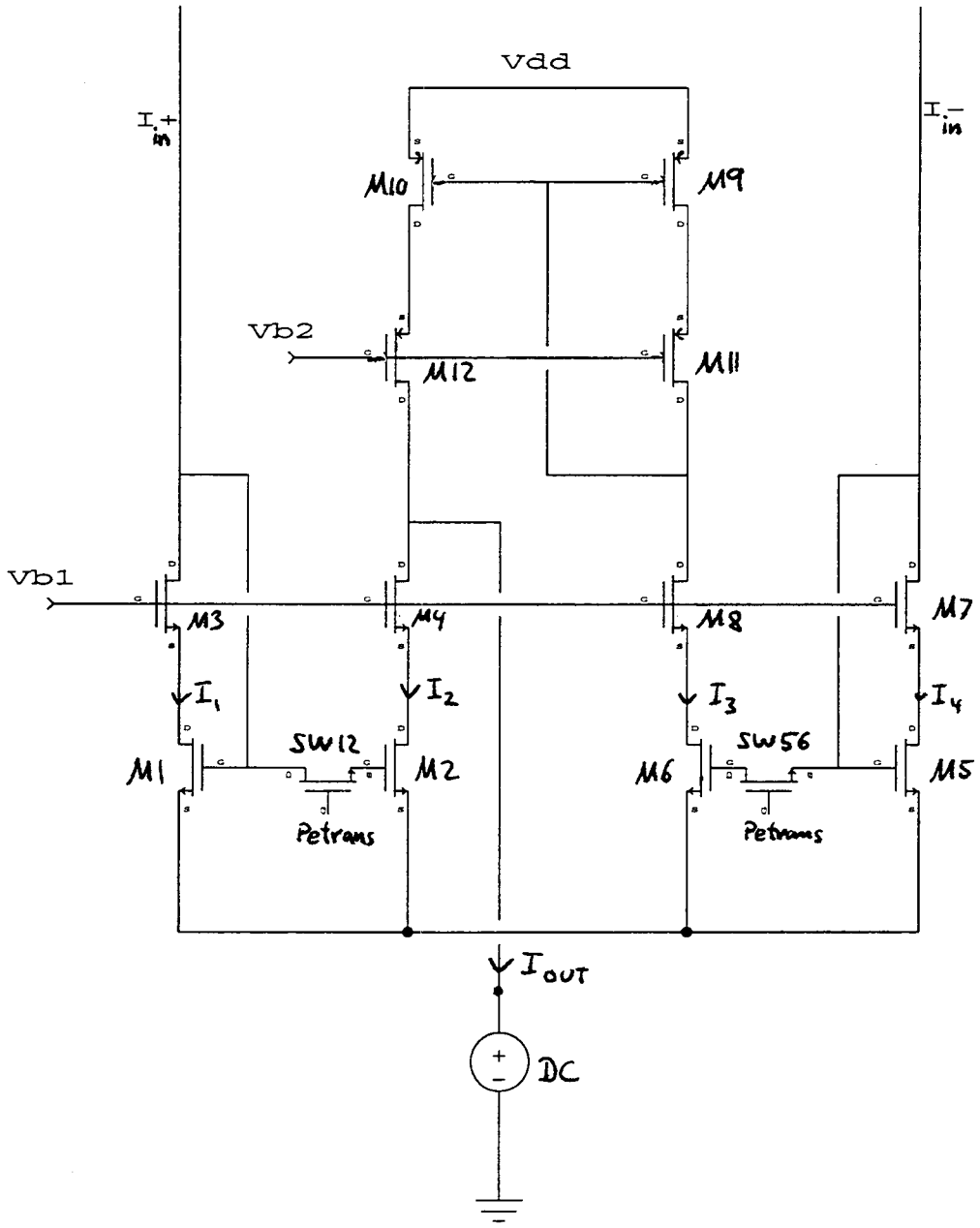


Figure 5.5. Circuit topology for Detection of phase and gainerror

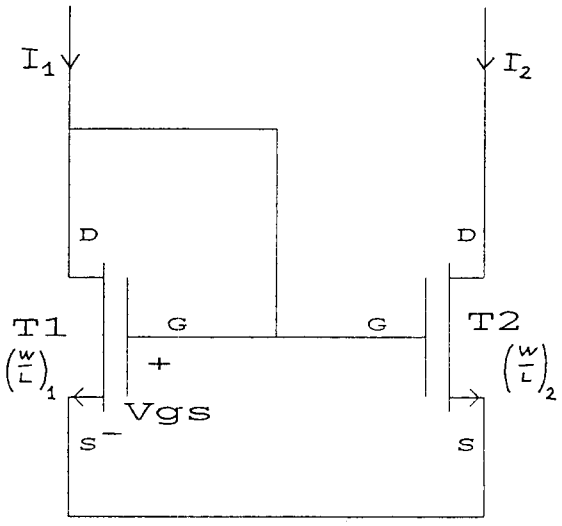


Figure 5.6. Basic current mirror cell

mode reference current and eliminated by a suitably chosen operating point of the following stages.

5.3.2. Functionality and nonidealities

The proposed circuit realizes the equations for the phase and gain error by addition and subtraction of currents. The functionality of a basic mirroring stage shown in figure *5.6* is described by the equations

$$V_{GS} = \sqrt{\frac{I_1}{\mu C_{ox}\left(\frac{W}{L}\right)_1}} \tag{5.2}$$

$$I_2 = \mu C_{ox} \cdot \left(\frac{W}{L}\right)_2 \cdot (V_{GS} - V_T)^2 \tag{5.3}$$

The constants W and L stand for the width and the length of a MOS device. V_T represents the threshold voltage of the device. C_{ox} and μ are material constants. All devices operate in saturation. A proper choice of transistor sizes and parameters is indicated by a settling of the saturation voltage $V_{SAT} = V_{GS} - V_T$ of the mirroring

devices at a value around 0.5V. The gate width W of the transistors used in the current mirrors has to be large enough to cope with the maximum possible drain current I_{max}. An approximation for the selection of the ratio $\frac{W}{L}$ is proposed in [32] as

$$\frac{W}{L} \approx \frac{I_{max}}{\frac{\mu C_{ox}}{2} \cdot (V_{GS} - V_T)^2} \tag{5.4}$$

Suitable ratios $\frac{W}{L}$ have been found to be in the range from 15-20. This determines the gate length L for a particular choice of W. Applying these criteria, the sizes of the mirroring transistors were selected as $W = 69u$ and $L = 3.8u$. The switches $sw12$ and $sw56$ should be sized very small for fast transient response and were chosen as $W = 2.4u$ and $L = 1.2u$.

The input currents I_{in+} and I_{in-} are mirrored to the middle branches 2 and 3 during periods of closed switches as

$$i_2 = I_{in+} + \Delta i_{12} + \delta i_{12} \tag{5.5}$$

$$i_3 = I_{in-} + \Delta i_{56} + \delta i_{56} \tag{5.6}$$

The terms Δi_{jk} stand for additional currents caused by charge-injection. The expressions δi_{jk} represent the additional currents due to device mismatches and channel-length modulation. Mirroring i_3 to i_6 yields

$$i_6 = i_3 + \delta i_{910} \tag{5.7}$$

The output current i_m as subtraction of i_6 and i_2 is used later on as input to a low-impedance output stage. It is obtained as

$$I_{out} = i_6 - i_2 \tag{5.8}$$

$$= [I_{in-} - I_{in+}] + [\Delta i_{56} - \Delta i_{12}] + (\delta i_{56} - \delta i_{12} + \delta i_{910}) \tag{5.9}$$

For a complete realization of the equations 4.11 and 5.1, a common-mode current representing the subtracted term 1 in these equations has to be considered as reference current I_{REF}. Without nonidealities, for I_{REF0} holds therefore

$$[I_{in-} - I_{in+}] \Leftrightarrow I_{REF0} \tag{5.10}$$

As for the same phaseshift the same input currents $I_{in-} - I_{in+}$ are obtained, the partly signal dependent nonidealities also take on the same value. The terms Δi_{jk} and δi_{jk} denoting nonidealities in eqn. *5.9* can thus be eliminated by calibrating the reference current I_{REF} suitably at zero phaseshift ($\tau = 0$) in the following way:

$$I_{REF} = I_{REF0} + \left[(\Delta i_{56} - \Delta i_{12}) + (\delta i_{56} - \delta i_{12} + \delta i_{910})\right]_{\tau=0} \tag{5.11}$$

This operation preserves the monotonity of the error in the presence of even signal-dependent error currents due to circuit nonidealities and by calibration the correct zero-crossing is also guaranteed while the nonidealities affect only the linear characteristic in a slight way. Once calibrated, the functionality of the detector circuit is ensured therefore regardless of possible device mismatches and charge-injections.

5.3.2.1. Channel-length modulation

Channel-length modulation in the MOSFETs has to be considered for correct operation of current mirrors. A MOSFET in saturation can be modelled according to [27]:

$$I_D = \mu \frac{C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \frac{\lambda}{L} \cdot V_{DS}) \tag{5.12}$$

The output conductance g_{ds} is, with I_{D0} denoting the drain current without channel-length modulation

$$g_{ds} = \frac{\delta I_D}{\delta V_{DS}} = \frac{\lambda}{L} \cdot I_{D0} \tag{5.13}$$

while the transconductance g_m is

$$g_m = \frac{\delta I_D}{\delta V_{GS}} = \cdots = 2 \cdot \sqrt{\mu \frac{C_{ox}}{2} \cdot \frac{W}{L} I_D} \tag{5.14}$$

combining equations 5.13 and 5.14 yields

$$g_{ds} = \lambda g_m \frac{\sqrt{\frac{I_D}{\mu \frac{C_{ox}}{2} \cdot \frac{W}{L}}}}{2 \cdot L} \tag{5.15}$$

A reduction of g_{ds} is proposed in [28] by increasing L thereby also increasing W as $\mu \frac{C_{ox}}{2} \cdot \frac{W}{L}$ is fixed.

The additional current δi_λ due to channel-length modulation is written according to [28] as

$$\delta i_\lambda \approx \frac{\lambda}{L} \cdot V_{DS} = g_{DS} \cdot V_{DS} \tag{5.16}$$

It can be seen, that a small value of g_{ds} should be achieved. Eqn. 5.13 shows that the voltage V_{DS} should be constant therefore. Cascoding transistors with constant dc bias voltages at their gates act to keep V_{DS} constant and to reduce the gate-to-source conductance g_{ds}.

5.3.2.2. Device mismatch

Matching components in a current mirror is an important issue. One principle is the symmetric layout of the transistors. But the technology parameter $\beta = \mu \frac{C_{ox}}{2} \cdot \frac{W}{L}$ can differ due to small inaccuracies during the fabrication process as well as the threshold voltages of the devices in a current mirror are never exactly the same. Both effects are commonly referred to as device mismatch. A difference ΔV_T in the threshold voltages of the transistors shows up in eqn. 5.3:

$$I_2 = \mu C_{ox} \cdot \left(\frac{W}{L}\right)_2 \cdot (V_{GS} - V_T + \Delta V_T)^2 \tag{5.17}$$

The resulting error current δI_T can be approximated in the following way as shown in [32]:

$$\delta I_T \approx \frac{2}{V_{GS} - V_T} \cdot \Delta V_T \cdot I_{in} \tag{5.18}$$

while the error current δI_{beta} resulting from differences of paramter β are written as

$$\delta I_{beta} = \frac{\Delta\beta}{\beta} \cdot I_{in} \tag{5.19}$$

These error currents are included in eqn. 5.9 as

$$\delta i_{jk} = \delta i_\lambda + \delta I_T + \delta I_{beta} \tag{5.20}$$

A large value of g_m helps here to attain error currents due to device mismatch. Further improvements can be achieved by usage of cascode current mirrors proposed in [30].

5.3.2.3. Charge-injection

A major shortcoming of switched-current circuits in general is the effect of signal-dependent charge-injection. In [25] is stated as approximation for the error current due to charge injection

$$\Delta i_{ci} = g_{m1} \Delta V_{GS} \tag{5.21}$$

where V_{GS} denotes the voltage across the gate-source capacitance of the signal storing transistor. The signal dependency is contained in g_m according to eqn. 5.14. The charge-injection is significant as can be seen in figure *5.7*. The signal-dependency of charge-injection is visible, as the current jumps caused by this clock feedthrough

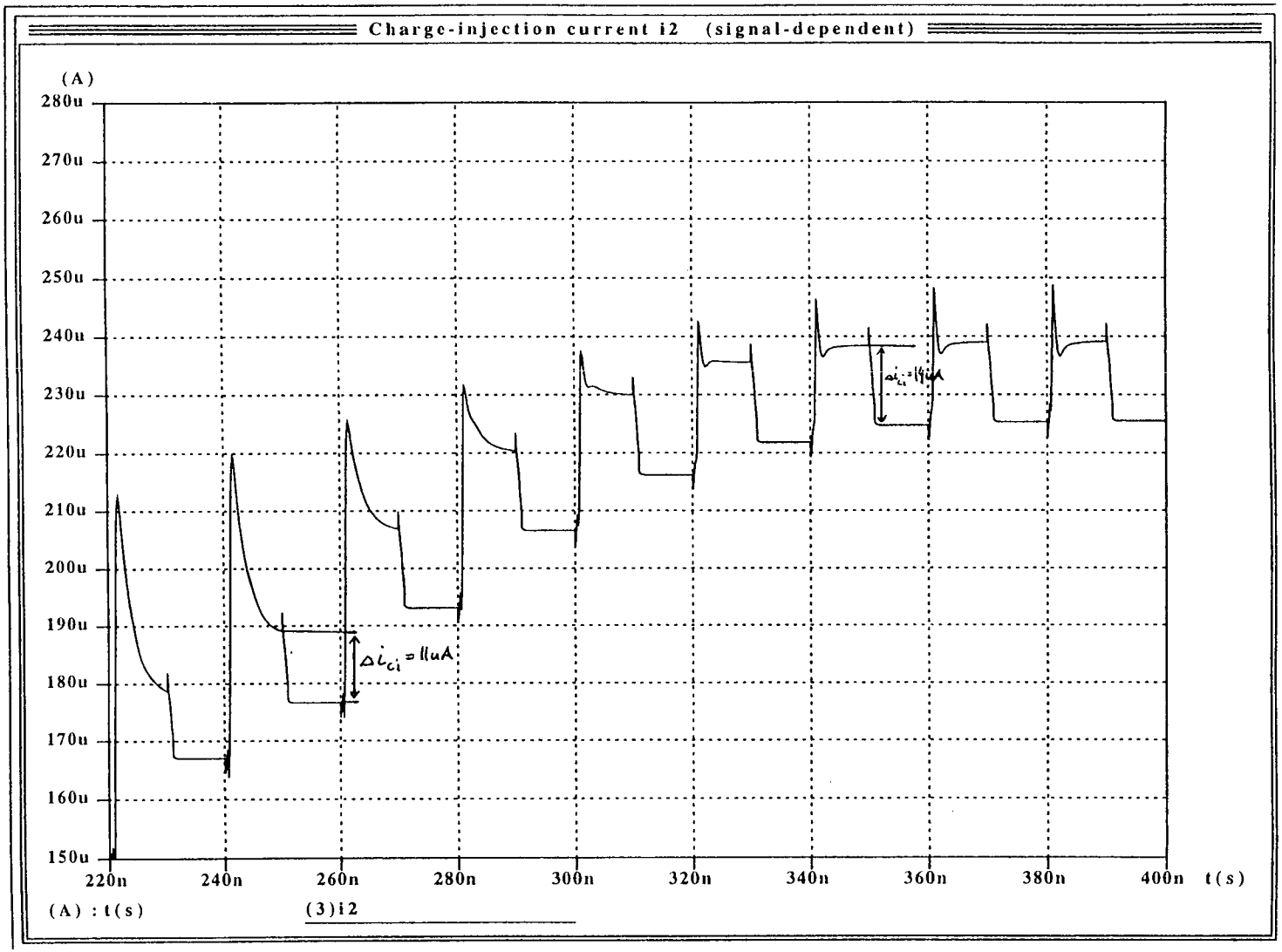


Figure 5.7. Current i_2: charge-injection by switch $sw12$

increase with the signal current. However, the fully-differential architecture of this circuit provides first-order cancellation of charge-injection [29] expressed in eqn. 5.9 as Δi_{56} and Δi_{12} . The plot of the mirrored current i_2 given in figure *5.7* shows the charge-injection deviations. However, the effects of this charge-injection do not put major limitations on the functionality of the error detection, as the error current only needs to exhibit monotonic behavior and calibration is used to eliminate the effect of charge-injection at the zero-crossing.

5.3.2.4. Speed

The symbol spacing of 10ns requires fast circuitry. The decisive time-constant τ for the speed of the current mirrors is determined by the gate-source capacitance and the transconductance as

$$\tau = \frac{C_{GS}}{g_m} \cdot 2\pi \tag{5.22}$$

The value of τ should be very small. For the selected transistor sizes, $\tau \approx 2.24$ns was achieved. The time for settling of the current mirrors to a new value with a specified error ε can be expressed according to [31] as

$$t_S = \tau \cdot \ln\left(\frac{I_b - I_a}{\varepsilon}\right) \tag{5.23}$$

Small differences of the current I_b and the previous current I_a helps to increase the speed. The selected switching array supports this.

The objectives of small values for g_{DS} and large ones for g_m are in some papers jointly expressed as gain $A = \frac{g_m}{g_{DS}}$ of the current mirror. In the simulations, a value of $A = 87.5$ was achieved.

5.4. RESULTS

The performance of the current mirrors is shown in figure *5.8*, where the currents I_1 and I_2 are plotted. What can be seen is the close tracking with a device mismatch error of less than $0.5uA$. Figure *5.8* shows that the currents are mirrored with only a negligible device mismatch error for the selected sizes of the transistors.

A comparison of the obtained phase error implementing NMOS switches with the approach using ideal switches is given in figure *5.9*. A limitation of the performance is related to the speed of the current mirror in the middle branch: The current I_{in-} is in fact two times mirrored and thus the settling time of the PMOS current mirror is slower than the NMOS on the left side. The switches $sw12$ and $sw56$ provide holding of the current once the charge-injection error current settles. Especially in tracking mode, the speed issue is thereby only a minor problem, as in average almost two clock cycles are available for sampling of the error signal. The obtained signal still yields the desired characteristics in terms of proportionality to the ideal error determined by the equations and a steady-level for zero error. More advanced switches comprised of a NMOS and the complementary PMOS device called transmission gates may be implemented to reduce the amounts of charge injection. In figure *5.10* a comparison with the phase error obtained from the ideal equation is shown. The monotonity is preserved, and a common mode current will be chosen to represent zero phase error and the nonideal effects at a phaseshift of zero.

One of the objectives is low power consumption by the circuit. By putting out the reference currents at the bottom of the circuit rather than inserting them on top of the stage, the total power consumption of the circuit is reduced. The dynamic range of the currents through the mirroring devices extends from 105uA to

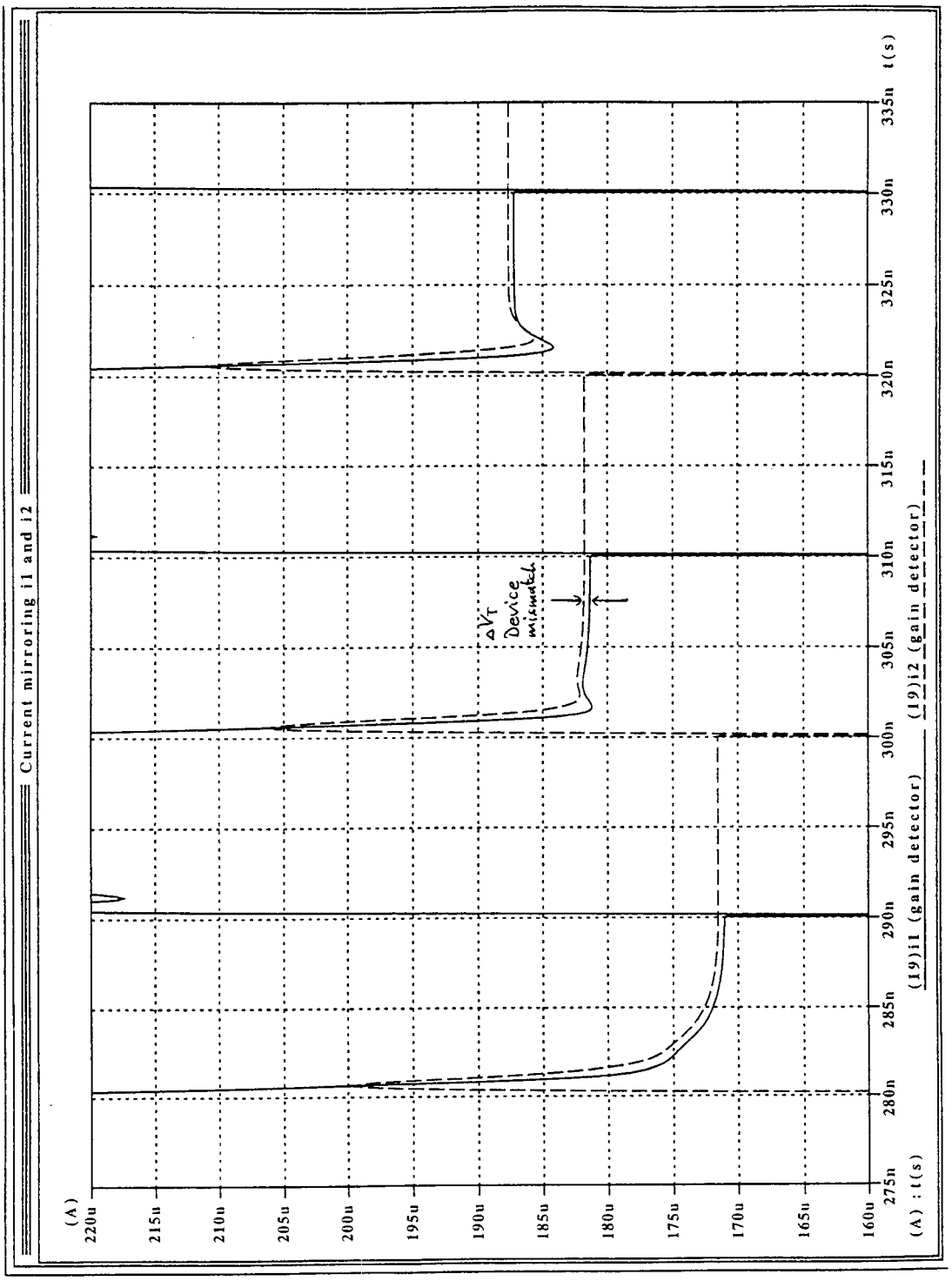


Figure 5.8. Currents I_1 and I_2 in switched-current mirror

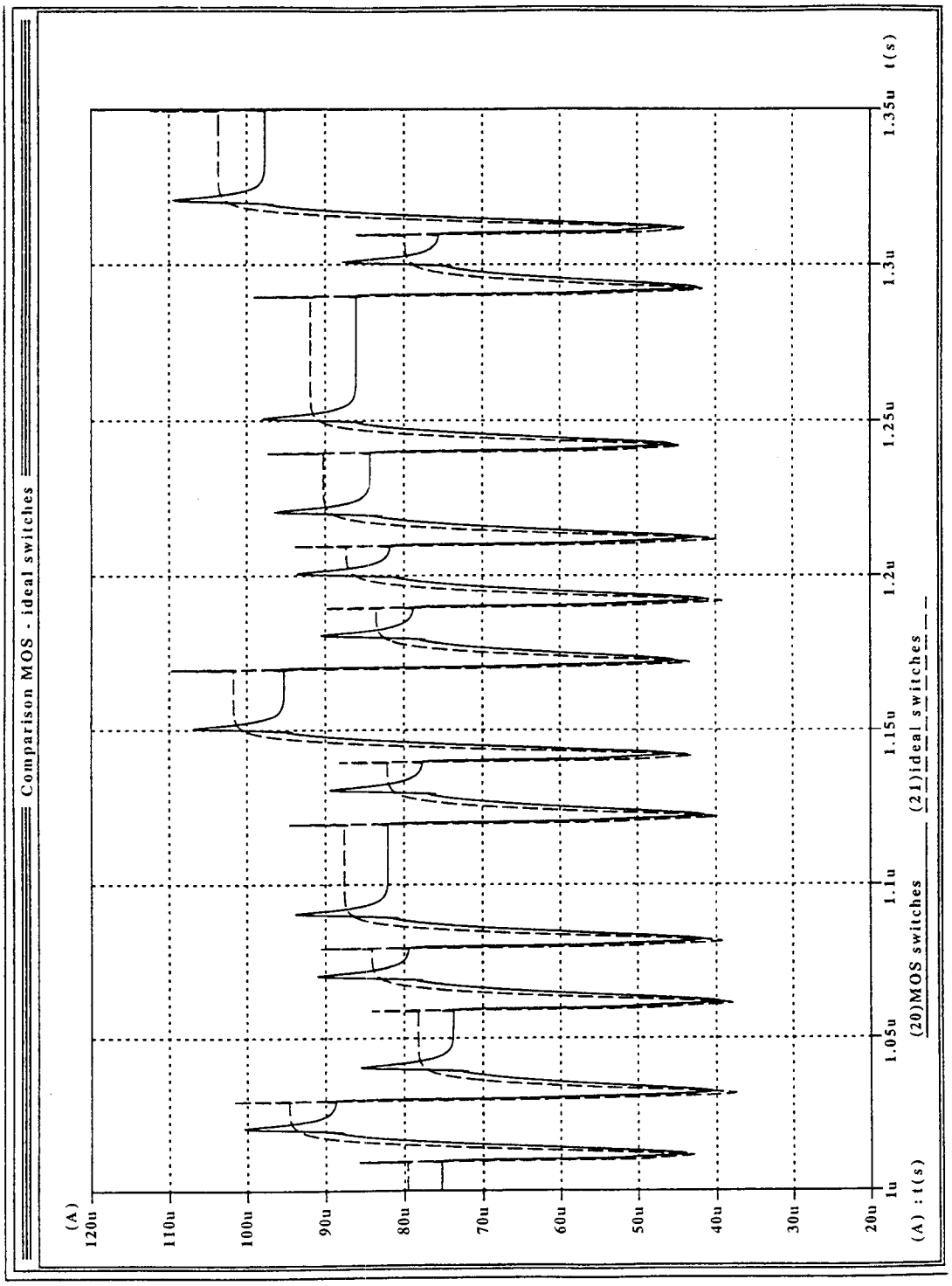


Figure 5.9. Comparison effect of MOS switches - ideal switches for output i_{pm}

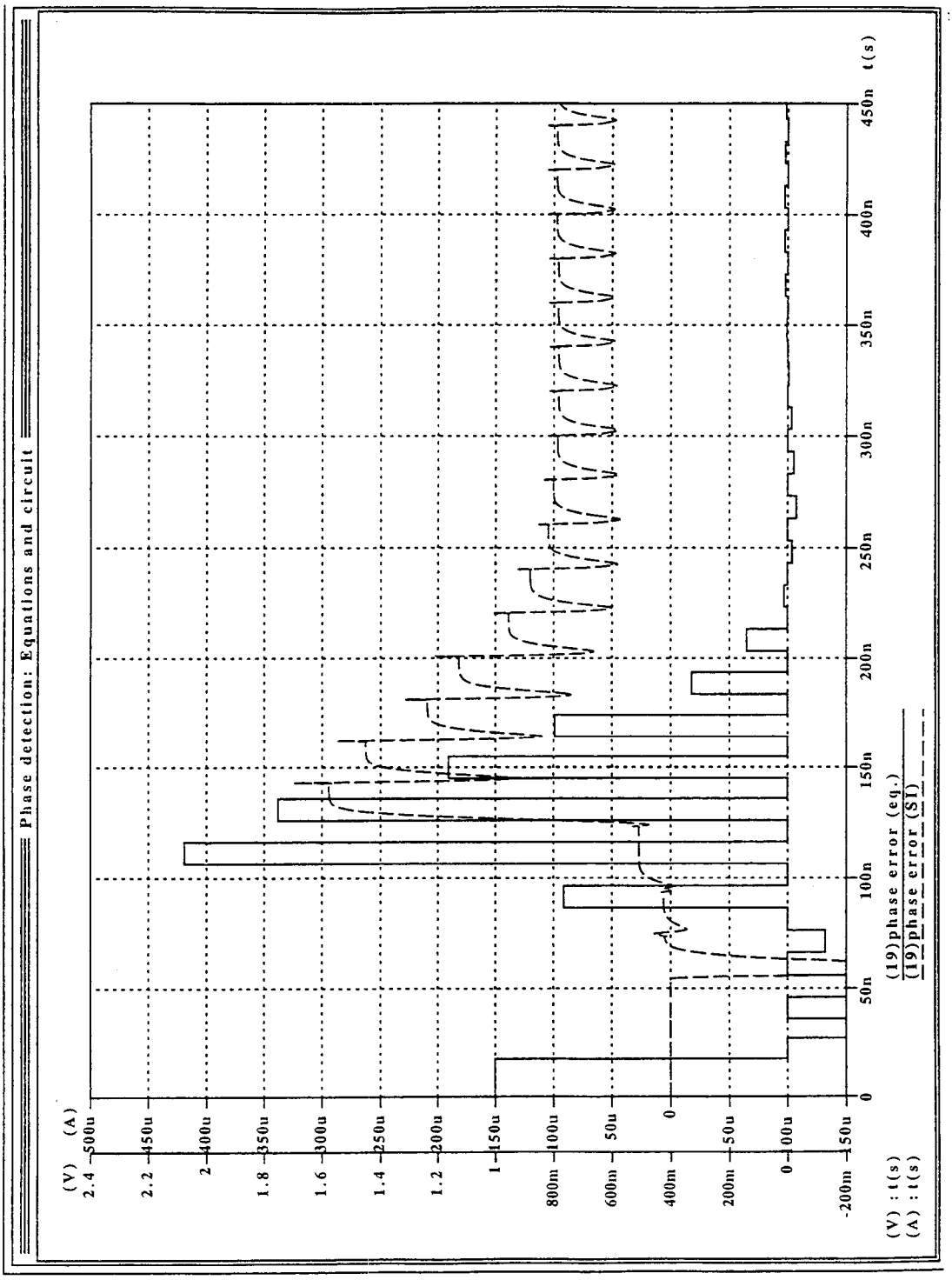


Figure 5.10. Comparison SI circuit and ideal equation in simulation

428uA. The output current range extends from 230uA to 5uA for the gain error with the common mode current representing zero gain error being 102uA . The output current range for the phase error is found to be 260uA to 10uA with a common mode current of 109uA.

6. CONCLUSION AND FUTURE WORK

6.1. CONCLUSION

The analog implementation of MDFE provides advantages such as low power consumption and suitable performance for the high symbol densities of the future. MDFE is based on a run-length constrained code, whose effects on the signals in the forward and backward path were assessed. The coding facilitates the detection of phase and gain offsets.

Simple equations for the phase and gain error were developed using the slicer-input and the detected symbols in derivation from a minimum-mean square error gradient based algorithm. An exhaustive search was performed for the loop filters of the phase locked loop and the automatic gain control. With a phase-lag compensation stage in the phase-locked loop, fast joint transient behavior with zero steady-state error is achieved. Capability of clock acquisition and tracking of random variations as well as suitable noise rejection was shown in simulations. An analytical description of the phase-locked loop and the automatic gain control during acquisition mode is provided and its improvement by phase-lag compensation in the timing recovery loop is demonstrated. The system has been tailored for operation at a user density of 2.5PW50.

An analog hardware implementation in CMOS technology is presented applying switched-current techniques for the phase and gain error. The proposed fully-differential SI circuitry offers the advantages of charge-injection cancellation to first order.

6.2. FUTURE WORK

Future work should integrate the phase and gain error obtained from the detectors into an entire analog phase-locked loop and automatic gain control, respectively. As the storage densities on magnetic hard disks tend to increase, the applied detection scheme needs to be capable of dealing with nonlinear effects in the magnetization caused by closely spaced transitions on the media. Consideration of these effects could be provided by nonlinear adaptive equalization schemes affecting the customized phase and gain detection which will need to be adjusted to the occuring signal waveforms. In a future project, a RAM-DFE implementation of MDFE will be investigated.

BIBLIOGRAPHY

[1] J.G. Kenney, L.R. Carley and R. Wood, "Multi-level Decision Feedback Equalization for Saturaration Recording",*IEEE Transactions on Magnetics*, vol. 19, no.4, pp.2160-2171, July, 1993

[2] J. Cioffi, W.L. Abbott, H.K. Thapar, C.M. Melas, K.D. Fisher, "Adaptive Equalization in Magnetic-Disc-Storage Channels",*IEEE Communications Magazine*, pp.14-28, Feb. 1990

[3] R.D. Cideciyan et al., "A PRML System for Digital Magnetic Recording", *IEEE Journal on Selected Areas in Communications*, vol.10, no.1, pp.38-55, Jan. 1992

[4] D.J. Tyner and J.G. Proakis, "Partial Response Equalizer Performance in Digital Magnetic Recording Channels", *IEEE Transactions on Magnetics*, vol.29, no.6, pp.4194-4208, Nov. 1993

[5] J.J. Moon and L.R. Carley, "Performance Comparison of Analog DFE Architectures for Disk-Drive Applications", *IEEE Transactions on Magnetics*, vol.19, no.4, pp.3155-3172, Nov. 1990

[6] J.G. Kenney and R. Wood, "Multi-level Decision Feedback Equalization: An Efficient Realization of FDTS/DF",*IEEE Transactions on Magnetics*, vol. 31, no.2, pp.1115-1120, March, 1995

[7] A.V. Oppenheim and R.W. Schaefer, *Discrete-time Signal Processing*, Prentice-Hall, 1988

[8] J.G. Kenney, "Multi-level Decision Feedback Equalization with Clock Recovery", *IEEE publ*, cat. 1058-6393/92, pp.945-949, IEEE 1992

[9] P.A. McEwen and J.G. Kenney, "Allpass Forward Equalizer for DFE", *1995 Digests of Intermag '95*, p. CB-08, published 1995 by IEEE, 0-78-3-2605-9/95

[10] J.G. Kenney, "Geometric Representation fo the Tree-search Detector and its Hardware Implications", *Dissertation, Carnegie-Mellon University*, Dec. 1991

[11] A. Gallopoulos, C. Heegard, P.H. Siegel, "The pover spectrum of Run-Length-Limited Codes", *IEEE Transactions on Communications*, vol.37, no.9, pp.906-917, Sept. 1989

[12] Kobayashi, "Coding schemes for digital data", *IEEE Transactions on Communication Technology*, vol.COM-19, no.6, pp.1087-1100, 1971

[13] W.L. Abbott and J.M. Cioffi, "Timing Recovery for adaptive decision Feedback equalization of the Magnetic storage channel", *IEEE publ.*, cat. CH2847-2/90/0000-0929, pp.929-932 1990

[14] O. Shimbo and M.I. Celebiler, "The Probability of Error due to Intersymbol Interference and Gaussian Noise in Digital Communication Systems", *IEEE Transactions on Communication Technology*, COM-19, pp.113-119, 1971

[15] S.U.H. Quereshi, "Timing Recovery for Equalized Partial-Response Systems", *IEEE Transactions on Communications*, pp.1326-1331, Dec. 1976

[16] K.H. Mueller and M.S. Mueller, "Timing Recovery in Digital Synchronous Data Receivers", *IEEE Transactions on Communications*, vol.24, pp.516-531, May 1976

[17] F.M. Gardner, *Phaselock-Techniques*, 2nd Ed., J.Wiley & Sons, 1979

[18] E.A. Lee and D.G. Messerschmitt, *Digital Communication*, Kluwer Academic Publishers, 1988

[19] J. Sonntag et al., "A High-Speed, Low Power PRML Read Channel Device", *IEEE Transactions on Magnetics*, vol.31, no.2, pp.1186-1195, March, 1995

[20] T.T. Lau and J.G. Zhu, "Phase Dependence of Track Edge noise in MR Head written overlapping Tracks", *1995 Digests of Intermag '95*, p. HQ-03, published 1995 by IEEE, 0-78-3-2605-9/95

[21] K. Ogata, *Discrete-Time Control Systems*, Prentice-Hall, 1987

[22] D.P. Lindorff, *Theory of Sampled-Data Control Systems*, J.Wiley & Sons, 1965

[23] B.C. Kuo, *Analysis and Synthesis of sampled-data control systems*, Prentice-Hall,Inc., 1963

[24] A.B. Schrader et al., "The Influence of write current offset on Bit Shift", *1995 Digests of Intermag '95*, p. FB-08, published 1995 by IEEE, 0-78-3-2605-9/95

[25] S.J. Daubert, D. Vallancourt and Y.P. Tsividis, "Current copier cells", *Electronics Letters*, vol.24, no.25, pp.1560-1562, Dec. 1988

[26] J.B. Hughes, N.C. Bird and I.C. Macbeth, "Switched currents - a new technique for analog sampled-data signal processing", *IEEE Publ. , ISCAS '89*, pp.1584-1587

[27] R. Gregorian and G.C. Temes, *Analog MOS integrated circuits for signal processing*, J.Wiley, NY, 1986

[28] A. Nedungadi and T.R. Viswanathan, "Design of Linear CMOS Transconductance Elements", *IEEE Transactions on Circuits and Systems*, vol. 31, no.10, Oct. 1984

[29] D.J. Allstot and R.H. Zele, "Low voltage fully-differential CMOS switched-current filters", *Proc. of the Custom Integrated Circuits Conf.*, IEEE cat.n.93CH3214-4, pp.6.2.1-6.2.4, 1993

[30] G.C. Temes, "Fast CMOS Current Amplifier and Buffer Stage", *Electronics Letters*, vol.23, no.13, pp.696-697, June 1987

[31] D.G. Nairn, "Analytic step response of MOS current mirrors", *IEEE Transactions on circuits and systems*, vol.40, no.2, pp. 133-135, Feb. 1993

[32] U. Ramacher and U. Rueckert, *VLSI Design of Neural Networks*, Kluwer Academic Publishers, 1991

APPENDICES

APPENDIX: LIST OF FIGURES

prev. →	00	01	10	11	v
00	101/v	100/00	001/v	010/00	000/00
01	100/v	100/01	010/v	010/01	000/01
10	101/10	100/10	001/10	010/10	000/10
11	101/11	100/11	001/11	010/11	000/11

Table 0.1. RLL 2/3(1,7) Finite-state-machine

APPENDIX B: MDFE ARCHITECTURE AND SABER SIMULATION

The SABER simulator is well suitable for simulation of mixed analog and digital components and templates can be customized easily. Ideal functions can be programmed based on equations.

APPENDIX C: RLL - CODING, FINITE STATE DESCRIPTION

A finite state description for 2/3(1,7) RLL coding is listed in table *0.1*, taken from [11]. The pair (u_0, u_1) of user bits which shall be coded are in the first row, indicated as "actual data". With the information of the following pair (u_2, u_3) in the left column, we find the 3 coding symbols for (u_0, u_1) and which column shall be used for the coding of (u_2, u_3).By applying reduction techniques, the Run-length-diagram from figure *0.2* can be transformed into the finite- state-transition diagram figure *0.3* where the numbers represent the number of consecutive zeros after a 1 has occured. It can be noticed from figure *0.3* that not all run-lengths appear as edge

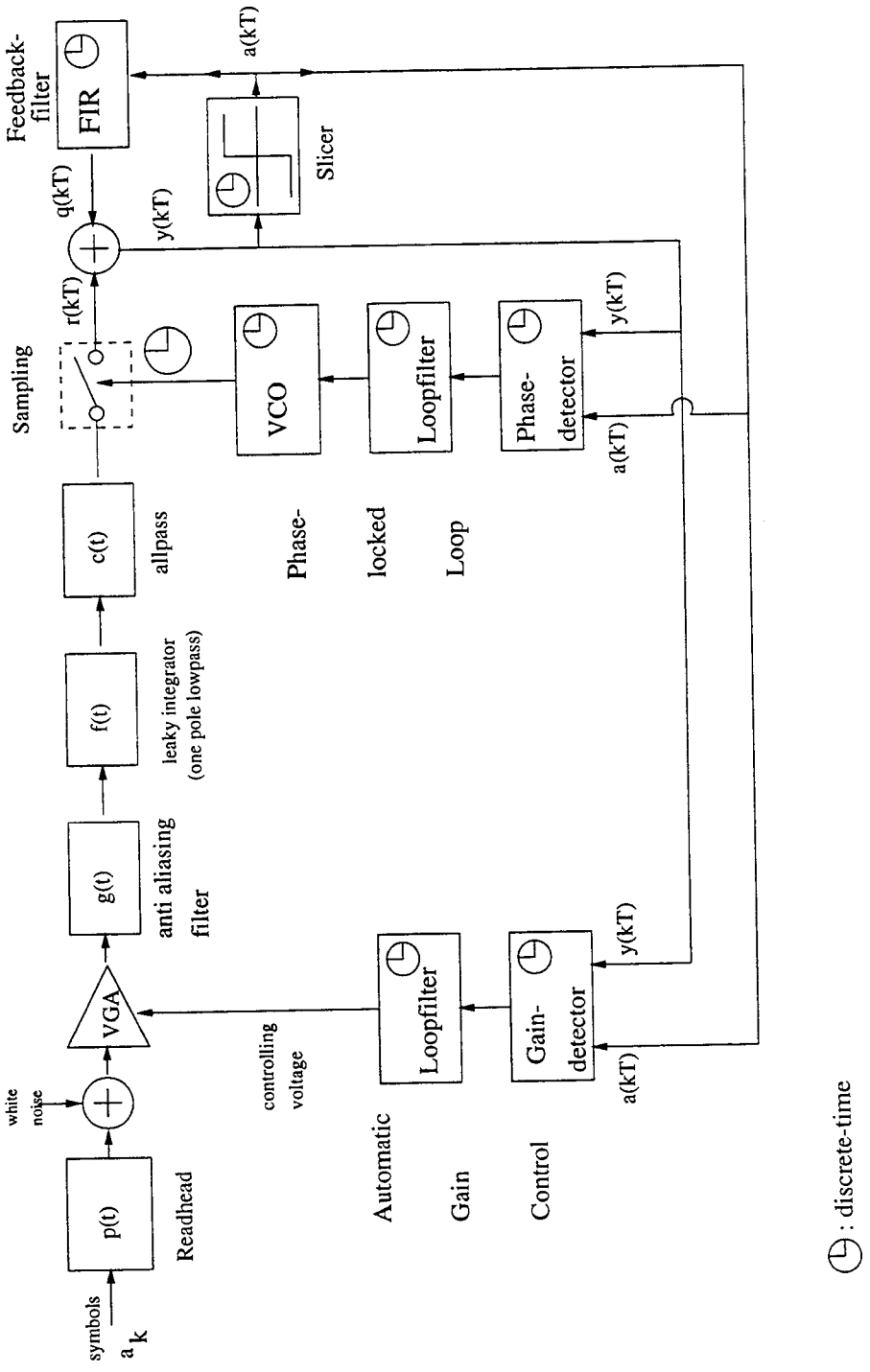


Figure 0.1. Block diagram MDFE architecture

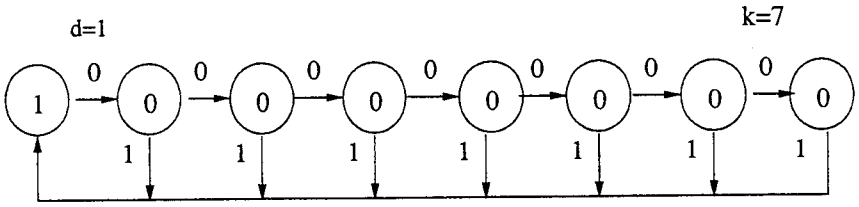


Figure 0.2. Run-length-diagram for (1,7) RLL code

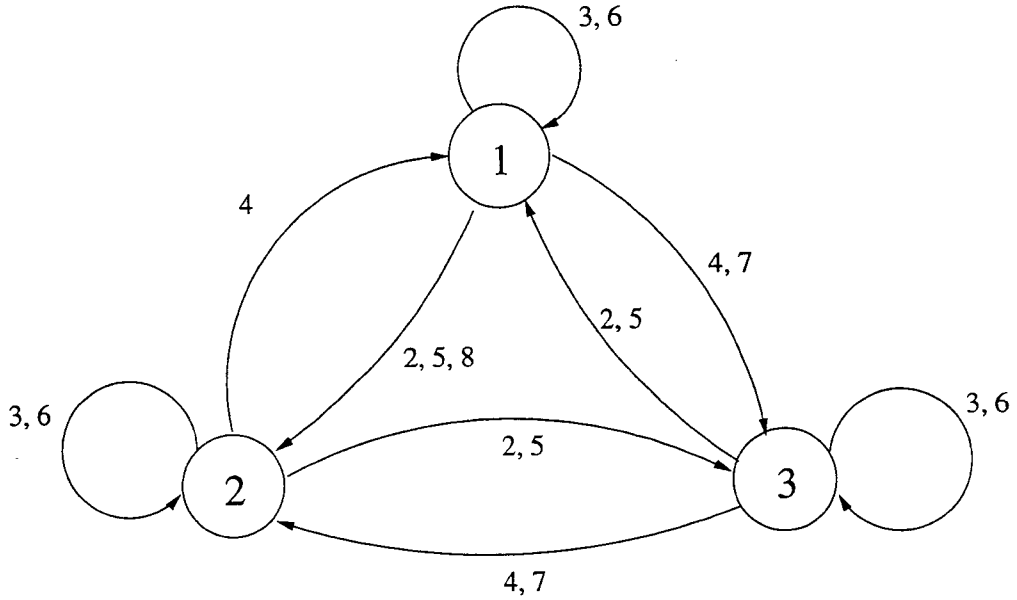


Figure 0.3. Finite-state-transition diagram for 2/3(1,7) RLL code

	a_1	a_2	a_3	a_4	a_5	a_6	a_7	a_8
start in 1	1	1	0.25	-0.25	-0.25	-0.0625	0.0625	0.0625
start in 2	1	1	0.1825	-0.322	-0.322	-0.1167	0.016	0.01
start in 3	1	1	0.2207	-0.2727	-0.2727	-0.065	0.065	0.065
mean	1	1	0.2185	-0.2816	-0.2816	-0.0813	0.048	0.046
SABER	1	1	0.2048	-0.298	-0.2924	-0.1108	0.038	0.0525

Table 0.2. Mean values for symbols a_k given $a_0 = -1$ and transition

emerging from every state, e.g. from state 2 no sequence of 6 or 7 consecutive zeros is possible. By this means, an inherent correlation between symbols is introduced. An evaluation of conditioned probabilities for the following symbols, given a known symbol, requires the probabilities for the edges in *figure 0.3.* These can be retrieved from [11]. In [12] the number of possible sequences $N_{dk}(n)$ for a given length n is found as

$$N_{dk}(n) = (d + k + 1 - n) + \sum_{i=d}^{k} N_{dk}(n - i - 1) \qquad \text{(C1)}$$

which renders 21 different sequences for $n = 8$ for $d = 1; k = 7$. Due to the even symmetry property of autocorrelation, the same sequences and probabilities in a reversed order are obtained. Evaluating those possible symbol sequences, probabilities can be calculated for each symbol in the sequence using the state-transition probabilities given in [11]. Therefrom the expected values of table *0.2* can be derived for each state separately and then summed up and compared to the average values of the SABER simulation. In a similar manner the expected symbol values $E\{a_m \mid a_0 = 1\}$ can be determined, if no information about transitions is available.

Due to the fact that abs(a_0) = 1, the discrete autocorrelation function is identical to the calculated expected values, as the equation holds

$$E\{a_m \mid a_0 = 1\} = E\{a_m \cdot (a_0 = 1)\} = R\{a(mT)\} \tag{C2}$$

for the stationary process $a(kT) = a_k$.

APPENDIX D: MATLAB/SIMULINK SIMULATION OF MDFE

In figure *0.4* the system used for the control-simulation of the joint adjustment of phase and gain is shown. Core of the system is the MATLAB-function *'combierror'* which incorporates the pulse response $w(t)$ as a look-up table for the occuring phaseshifts. 22 symbols of a random symbol sequence $a\{k\}$ are used as input and 22 samples of band-limited white noise with selectable power. Each sample is multiplied by the corresponding gain value. The phase and gain error is computed and processed by the loopfilters in the subsystems phaseupdate and gainupdate, respectively. The observed variables are the phasedifference $phdiff$ to the ideal phase provided by a digital clock and the gain *gain* of the current mainsample a(kT). Phase and gain steps can be put in at arbitrary time by the inputs on the left side.

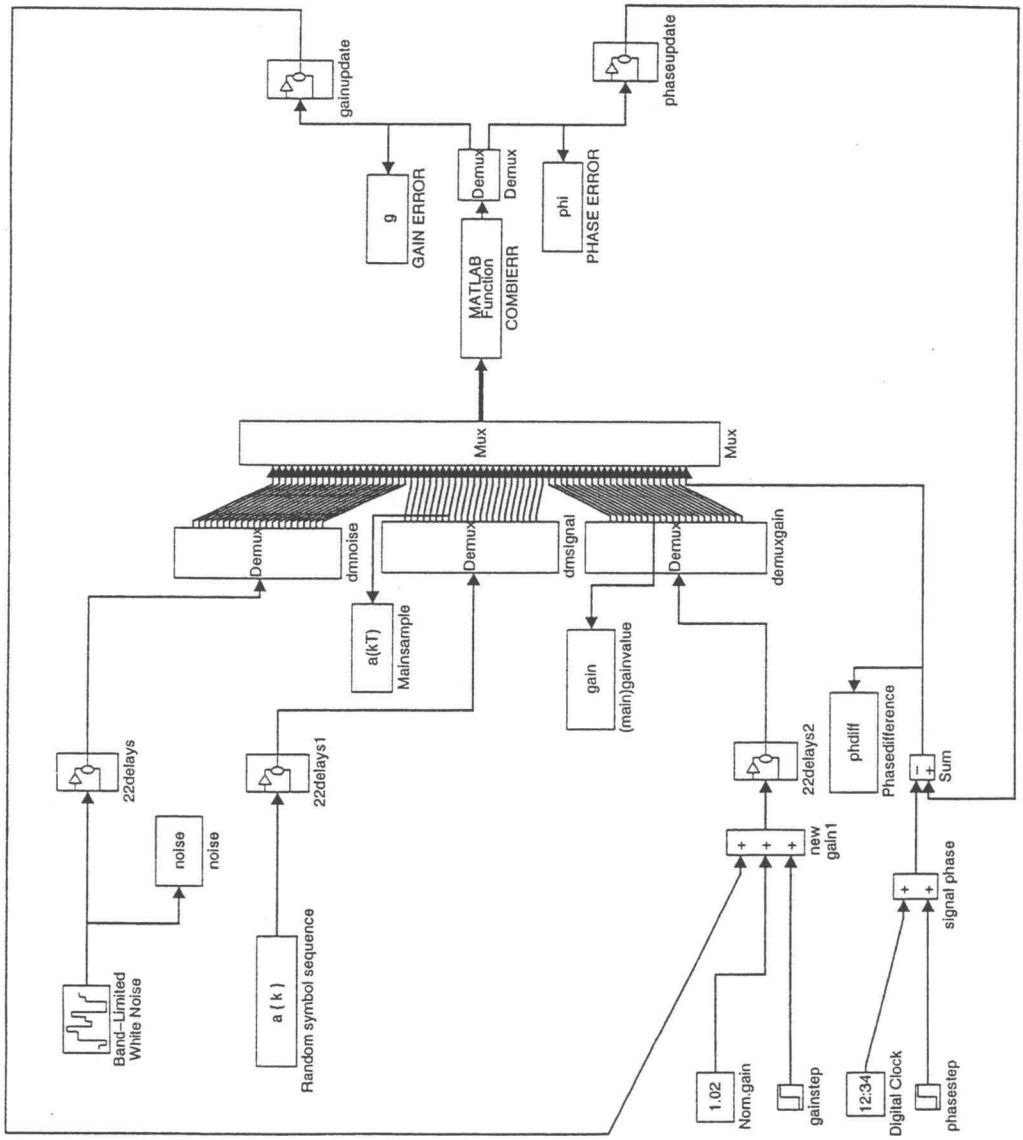


Figure 0.4. MATLAB Loopsimulation *COMBISYS*