### AN ABSTRACT OF THE THESIS OF

<u>Duncan S. Hazenboom</u> for the degree of <u>Master of Science</u> in <u>Electrical and Computer</u> <u>Engineering</u> presented on <u>June 1, 2004</u>.

Title: <u>A Comparison of Substrate Noise Coupling in Lightly and Heavily Doped CMOS</u> <u>Processes for 2.4GHz LNA's</u>

Abstract approved:

Signature redacted for privacy.

Terri S. Fiez

Signature redacted for privacy.

U

Kartikeya Mayaram

Three types of low noise amplifiers operating at 2.4GHz were designed. They are the commonly used single-ended and differential amplifiers as well as a new quasidifferential amplifier. The substrate noise injected into these amplifiers is examined for both heavily and lightly doped CMOS substrates.

For the single-ended amplifier the noise is modeled in SPICE with good correlation between measurements and simulations. Using these models and simulations the major noise coupling mechanisms are identified. In both types of substrates, harmonics of the clock couple into the bond pads and the inductor at the LNA output. Intermodulation products of the clock and the RF carrier are produced by noise coupling directly into the input transistor in the heavily doped substrate or into the gate interconnect in the lightly doped substrate. Methods of noise mitigation are identified and simulated for each substrate.

In the differential amplifier harmonic noise is dominated by unequal coupling into passive circuitry. Intermodulation noise in the differential amplifier arises from coupling of substrate noise into the active devices. Even though the substrate noise is common mode, it is shown that the intermodulation noise is not reduced in a differential amplifier circuit.

The performance of the quasi-differential amplifier is comparable to the differential amplifier in the lightly doped substrate. However, in the heavily doped substrate the intermodulation noise is much larger with the quasi-differential amplifier.

©Copyright by Duncan S. Hazenboom

June 1, 2004

All Rights Reserved

# A Comparison of Substrate Noise Coupling in Lightly and Heavily Doped CMOS

Processes for 2.4GHz LNA's

by

Duncan S. Hazenboom

## A THESIS

Submitted to

Oregon State University

in partial fulfillment of

the requirements for the

degree of

Master of Science

Presented June 1, 2004

Commencement June 2005

#### ACKNOWLEDGEMENTS

My greatest appreciation goes out to my wife Roxanne. Without her support and encouragement over the past few years it would have been very difficult to return to school.

I am grateful to my advisors, Dr. Terri Fiez and Dr. Karti Mayaram for giving me the opportunity to work on a project that combined my interests in RF design with substrate coupling. Their willingness to let me forge ahead combined with advice and direction when I needed it was very much appreciated.

Several of the classes I have taken at OSU have been helpful for completing this thesis. In particular, the class on interconnects taught by Dr. Weishaar and the course on RFIC design by Dr. Mayaram have been most informative.

Thanks to Dr. David McIntyre and Dr. Andreas Weishaar for serving on my defense committee along with my advisors.

I would also like to thank Dr. Chengang Xu for his support using EPIC and some of the students that helped make this project possible. Sirisha Adluri for designing the stepped buffers, Martin Held for completing the top level layout of both integrated circuits, Hui En Pham for assisting with the initial EPIC simulations, and James Ayers for suggesting a method to improve some of the measurements.

This work has been supported financially in part by SRC under contract 2001-TJ-911 and by the DARPA TEAM project under contract F33615-02-1-1179.

# TABLE OF CONTENTS

1	Intr	oductio	Dn	1	
2	Motivation				
3	Circuit Design and Layout				
	3.1	Ste	pped Buffer	5	
	3.2	Sin	ngle-ended LNA	6	
		3.2.1	Design	6	
		3.2.2	Layout	8	
	3.3	Dif	fferential LNA	10	
		3.3.1	Design	10	
		3.3.2	Layout	11	
	3.4	Qu	asi-Differential LNA	13	
		3.4.1	Design	13	
		3.4.2	Layout	14	
	3.5	Inte	egrated Circuit	15	
	3.6	Pac	ckaging and Printed Circuit Board	16	
4	Modeling				
	4.1 Circuit Modeling				
	4.2	Su	bstrate Noise Modeling	18	
		4.2.1	General Substrate Modeling Approach	18	
		4.2.2	Modeling of the Heavily Doped Substrate and the Single-ended LNA	19	
		4.2.3	Modeling of the Lightly Doped Substrate and the Single-ended LNA	20	
5	Ext	berimer	ntal Results	21	
	5.1 Measurement Setup			21	
	5.2 Measured RF Performance of Each LNA			22	
	5.3 Substrate Coupled Noise Measured in the Single-ended LNA		bstrate Coupled Noise Measured in the Single-ended LNA	22	
	5.4 Substrate Coupled Noise Measured in the Differential LNA		bstrate Coupled Noise Measured in the Differential LNA	25	
	5.5 Substrate Coupled Noise Measured in the Ouasi-differential LNA				
6	An	alysis o	of Results	31	
	6.1	An	alysis of the Single-ended LNA	31	
			,		

# TABLE OF CONTENTS (Continued)

## Page

		6.1.1	Measured and Simulated Single-ended LNA Performance	. 32	
	6.1.2 Noise Coupling Comparison for Stepped Buffers 2 and 4.				
		6.1.3	Noise Coupling Mechanisms for the Single-ended LNA	. 37	
		6.1.4	Noise Mitigation for the Single-ended LNA	. 39	
	6.2	Ana	lysis of the Differential LNA	. 40	
		6.2.1	Noise Coupling in the Heavily Doped Substrate	. 41	
		6.2.2	Noise Coupling in the Lightly Doped Substrate	. 43	
	6.3	Ana	lysis of the Quasi-Differential LNA	. 45	
		6.3.1	A Comparison of the Noise Coupling in Lightly and Heavily Doped		
	Substrates			. 46	
		6.3.2	A Comparison of the Noise Coupling in the Differential and Quasi-		
		Differen	ntial Amplifiers	. 46	
7	Co	nclusion	s	. 49	
Bib	Bibliography				
App	Appendicies				
	Appendix A Printed Circuit Board5				
	Appendix B Interconnect and Passive Device Modeling				
Appendix C Resistive Substrate Modeling Approximation				. 65	
	Appendix D Analysis of Substrate Noise in the Differential Amplifier				
	Appendix E Additional Amplifier Measurements				

## LIST OF FIGURES

Page

<u>Figure</u>

1. Substrate noise coupling.       2         2. A comparison of receivers with differential and quasi-differential LNA's.       4         3. Block diagram of the stepped buffer.       5         4. Circuit schematic of the single-ended LNA.       8         5. Die photograph of the single-ended LNA.       9         6. Circuit schematic of the differential LNA.       11         7. Die photograph of the differential LNA.       12         8. Circuit schematic of the quasi-differential LNA.       14         9. Die photograph of the quasi-differential LNA.       15         10. Photograph of the packaged die.       16         11. Cross sections of heavily and lightly doped substrates.       18         12. Cross section and lumped element model for the heavily doped substrate.       20         13. Cross section and lumped element model for lightly doped substrate.       21         14. Measured substrate noise from stepped buffer 4 at the output of the single-ended LNA in heavily and lightly doped substrates.       24         15. Measured substrate noise from stepped buffer 1 at the output of the differential LNA in heavily and lightly doped substrates.       25         16. Measured substrate noise from stepped buffer 2 at the output of the differential LNA in heavily and lightly doped substrates.       27         17. Measured substrate noise from stepped buffer 2 at the output of the differential LNA in heavily and lightly doped substrates.
<ol> <li>A comparison of receivers with differential and quasi-differential LINA's.</li> <li>Block diagram of the stepped buffer.</li> <li>Circuit schematic of the single-ended LNA.</li> <li>Die photograph of the single-ended LNA.</li> <li>Oir photograph of the differential LNA.</li> <li>Die photograph of the differential LNA.</li> <li>Die photograph of the differential LNA.</li> <li>Circuit schematic of the quasi-differential LNA.</li> <li>Circuit schematic of the quasi-differential LNA.</li> <li>Circuit schematic of the quasi-differential LNA.</li> <li>Die photograph of the quasi-differential LNA.</li> <li>Photograph of the quasi-differential LNA.</li> <li>Photograph of the packaged die.</li> <li>Cross sections of heavily and lightly doped substrates.</li> <li>Cross section and lumped element model for the heavily doped substrate.</li> <li>Cross section and lumped element model for lightly doped substrate.</li> <li>Cross section and lumped element model for lightly doped substrate.</li> <li>Measured substrate noise from stepped buffer 2 at the output of the single-ended LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 1 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 2 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 2 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 2 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 4 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 4 at the output of the differential LNA in heavily and lightly doped substrates.</li> &lt;</ol>
<ol> <li>Block diagram of the stepped buffer.</li> <li>Circuit schematic of the single-ended LNA.</li> <li>Die photograph of the single-ended LNA.</li> <li>Die photograph of the differential LNA.</li> <li>Die photograph of the differential LNA.</li> <li>Circuit schematic of the quasi-differential LNA.</li> <li>Circuit schematic of the quasi-differential LNA.</li> <li>Die photograph of the quasi-differential LNA.</li> <li>Photograph of the packaged die.</li> <li>Photograph of the packaged die.</li> <li>Cross sections of heavily and lightly doped substrates.</li> <li>Cross section and lumped element model for the heavily doped substrate.</li> <li>Cross section and lumped element model for lightly doped substrate.</li> <li>Cross section and lumped element model for lightly doped substrate.</li> <li>Measured substrate noise from stepped buffer 4 at the output of the single-ended LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 1 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 2 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 1 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 2 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 4 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 4 at the output of the differential LNA in heavily and lightly doped substrates.</li> </ol>
<ol> <li>Circuit schematic of the single-ended LNA</li></ol>
<ul> <li>5. Die photograph of the single-ended LNA</li></ul>
<ul> <li>6. Circuit schematic of the differential LNA.</li> <li>11</li> <li>7. Die photograph of the differential LNA.</li> <li>8. Circuit schematic of the quasi-differential LNA.</li> <li>9. Die photograph of the quasi-differential LNA.</li> <li>14</li> <li>9. Die photograph of the quasi-differential LNA.</li> <li>15</li> <li>10. Photograph of the packaged die.</li> <li>16</li> <li>11. Cross sections of heavily and lightly doped substrates.</li> <li>18</li> <li>12. Cross section and lumped element model for the heavily doped substrate.</li> <li>20</li> <li>13. Cross section and lumped element model for lightly doped substrate.</li> <li>21</li> <li>14. Measured substrate noise from stepped buffer 4 at the output of the single-ended LNA in heavily and lightly doped substrates.</li> <li>24</li> <li>15. Measured substrate noise from stepped buffer 2 at the output of the single-ended LNA in heavily and lightly doped substrates.</li> <li>25</li> <li>16. Measured substrate noise from stepped buffer 1 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>27</li> <li>17. Measured substrate noise from stepped buffer 2 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>28</li> <li>18. Measured substrate noise from stepped buffer 4 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>28</li> <li>18. Measured substrate noise from stepped buffer 4 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>28</li> </ul>
<ol> <li>Die photograph of the differential LNA.</li> <li>Circuit schematic of the quasi-differential LNA.</li> <li>Die photograph of the quasi-differential LNA.</li> <li>Die photograph of the quasi-differential LNA.</li> <li>Photograph of the packaged die.</li> <li>Photograph of the packaged die.</li> <li>Cross sections of heavily and lightly doped substrates.</li> <li>Cross section and lumped element model for the heavily doped substrate.</li> <li>Cross section and lumped element model for lightly doped substrate.</li> <li>Cross section and lumped element model for lightly doped substrate.</li> <li>Cross section and lumped element model for lightly doped substrate.</li> <li>Measured substrate noise from stepped buffer 4 at the output of the single-ended LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 2 at the output of the single-ended LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 1 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 2 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 2 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 2 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 4 at the output of the differential LNA in heavily and lightly doped substrates.</li> </ol>
<ol> <li>Circuit schematic of the quasi-differential LNA.</li> <li>Die photograph of the quasi-differential LNA.</li> <li>Photograph of the packaged die.</li> <li>Photograph of the packaged die.</li> <li>Cross sections of heavily and lightly doped substrates.</li> <li>Cross section and lumped element model for the heavily doped substrate.</li> <li>Cross section and lumped element model for lightly doped substrate.</li> <li>Cross section and lumped element model for lightly doped substrate.</li> <li>Cross section and lumped element model for lightly doped substrate.</li> <li>Cross section and lumped element model for lightly doped substrate.</li> <li>Measured substrate noise from stepped buffer 4 at the output of the single-ended LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 1 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 2 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 2 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 2 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 2 at the output of the differential LNA in heavily and lightly doped substrates.</li> </ol>
<ol> <li>Die photograph of the quasi-differential LNA</li></ol>
<ol> <li>Photograph of the packaged die</li></ol>
<ol> <li>Cross sections of heavily and lightly doped substrates</li></ol>
<ol> <li>Cross section and lumped element model for the heavily doped substrate.</li> <li>Cross section and lumped element model for lightly doped substrate.</li> <li>Measured substrate noise from stepped buffer 4 at the output of the single-ended LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 2 at the output of the single-ended LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 2 at the output of the single-ended LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 1 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 2 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 2 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 2 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>Measured substrate noise from stepped buffer 4 at the output of the differential LNA in heavily and lightly doped substrates.</li> </ol>
<ol> <li>Cross section and lumped element model for lightly doped substrate</li></ol>
<ul> <li>14. Measured substrate noise from stepped buffer 4 at the output of the single-ended LNA in heavily and lightly doped substrates</li></ul>
<ul> <li>LNA in heavily and lightly doped substrates</li></ul>
<ul> <li>15. Measured substrate noise from stepped buffer 2 at the output of the single-ended LNA in heavily and lightly doped substrates</li></ul>
<ul> <li>LNA in heavily and lightly doped substrates</li></ul>
<ul> <li>16. Measured substrate noise from stepped buffer 1 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>17. Measured substrate noise from stepped buffer 2 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>18. Measured substrate noise from stepped buffer 4 at the output of the differential LNA in heavily and lightly doped substrates.</li> </ul>
<ul> <li>in heavily and lightly doped substrates.</li> <li>17. Measured substrate noise from stepped buffer 2 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>18. Measured substrate noise from stepped buffer 4 at the output of the differential LNA in heavily and lightly doped substrates.</li> </ul>
<ul> <li>17. Measured substrate noise from stepped buffer 2 at the output of the differential LNA in heavily and lightly doped substrates.</li> <li>18. Measured substrate noise from stepped buffer 4 at the output of the differential LNA in heavily and lightly doped substrates.</li> </ul>
<ul> <li>in heavily and lightly doped substrates</li></ul>
18. Measured substrate noise from stepped buffer 4 at the output of the differential LNA
in heavily and lightly doned substrates 20
In heavity and lightly upped substrates $27$
19. Measured substrate noise from stepped buffer 3 at the output of the quasi-differential
LNA in the lightly doped substrate
20. Measured substrate noise from stepped buffer 4 at the output of the quasi-differentia
LNA in heavily and lightly doned substrates 31

# LIST OF FIGURES (Continued)

<u>Figu</u>	<u>re</u> <u>Page</u>
23.	Harmonic and IM noise coupling into the single-ended LNA in the heavily doped
	substrate. (a) Harmonics of the clock. (b) IM products of the clock and the input
	RF signal
24.	Harmonic and IM noise coupling into the single-ended LNA in the lightly doped
	substrate. (a) Harmonics of the clock. (b) IM products of the clock and the input
	RF signal
25.	Noise coupling mechanisms as a percentage of the total noise power
26.	Harmonic and IM noise coupling into the differential LNA in the heavily doped
	substrate. (a) Harmonics of the clock. (b) IM products of the clock and the RF
	input signal 43
27.	Harmonic and IM noise coupling into the differential LNA in the lightly doped
	substrate. (a) Harmonics of the clock. (b) IM products of the clock and the input
	RF signal
28.	Harmonic and IM noise coupling into the differential and quasi-differential LNA's in
	the lightly doped substrate. (a) Harmonics of the clock. (b) IM products of the
	clock and the input RF signal

## Page

# LIST OF TABLES

Ta	ble	Page
1.	Measured performance of the LNA's at 2.4GHz in both substrates.	22
2.	Summary of the single-ended LNA performance	32

# LIST OF APPENDIX FIGURES

# Figure

# Page

A-1.	Schematic of the printed circuit board	56
A-2.	Schematic of the printed circuit board	57
A-3.	Photograph of the test PCB.	58
B-1.	SPICE model for on-chip interconnect.	58
B-2.	SPICE model bond pad.	63
B-3.	SPICE model for spiral inductor.	64
C-1.	Equivalent circuit for a section of homogeneous substrate	65
D-1.	Drain current in an N-channel MOSFET.	67
D-2.	Drain currents in a differential amplifier.	69
E-1.	S-parameters for the single-ended LNA on the lightly doped substrate	72
E-2.	S-parameters for the single-ended LNA on the lightly doped substrate	73
E-3.	S-parameters for the differential LNA on the lightly doped substrate	74
E-4.	S-parameters for the differential LNA on the heavily doped substrate.	.75
E-5.	S-parameters for the quasi-differential LNA on the lightly doped	
	substrate	.77
E-6.	S-parameters for the quasi-differential LNA on the heavily doped	
	substrate.	.78

# LIST OF APPENDIX TABLES

Page

E-1.	Summary of the single-ended LNA performance	71
E-2.	Summary of the differential LNA performance	74
E-3.	Summary of the quasi-differential LNA performance	76

<u>Table</u>

# A COMPARISON OF SUBSTRATE NOISE COUPLING IN LIGHTLY AND HEAVILY DOPED CMOS PROCESSES FOR 2.4GHZ LNA'S

### **1** INTRODUCTION

The convenience and improved productivity offered by wireless systems has lead to their widespread use for both consumer and commercial applications. In order to meet the aggressive cost targets, reduced form factors, and low power consumption for these wireless applications, it is desirable to integrate the wireless transceiver onto a single chip with other analog and digital circuits. Due to continued scaling, MOS transistor  $f_T$ 's are now well above 30GHz [1] making them a popular choice for wireless system on a chip applications where digital logic and radio frequency (RF) circuitry is implemented on the same chip.

One of the most significant challenges with implementing both digital and RF circuitry on a single chip is unwanted interference. Switching noise from the digital logic gates travels through the supply lines and the conductive silicon substrate, as depicted in Figure 1, degrading the performance of sensitive analog circuits such as a low noise amplifier (LNA). Previous research on noise coupling into LNA's focused on either heavily doped substrates [2], [3] or lightly doped substrates [4] but not both. This paper expands on the previous work by comparing the digital noise coupling into three different LNA architectures fabricated on both substrate types. In addition, a modeling approach that accounts for the digital noise coupled into both active and passive devices is presented. This modeling approach is applied to a single-ended LNA allowing the various noise coupling mechanisms to be identified. Based on these models, methods for

mitigating the noise in the single-ended LNA are evaluated. The knowledge gained from detailed modeling of the single-ended LNA is applied to analyzing the noise coupling in two additional amplifier architectures. The first of these amplifiers has a differential input and output while the second is a novel design with a single-ended input and fully differential output.



Figure 1. Substrate noise coupling.

This paper is organized as follows. The motivation for this work is explained in Section 2. The design of the noise generator and each type of amplifier is presented in Section 3. The modeling approach used for the RF analysis of the amplifiers and for the substrate noise coupling analysis is detailed in Section 4. The measured RF and noise coupling performance for each type of amplifier is provided in Section 5. This is followed by analysis and simulations of the noise coupling in Section 6. Concluding remarks are given in Section 7.

#### **2** MOTIVATION

In previous substrate noise coupling research, performance comparisons of the same circuit in heavily and lightly doped substrates has been limited to passive circuits [6]. Active RF circuits present additional challenges making a substrate comparison of practical importance. Since low noise amplifiers are generally considered to be the most sensitive block in a typical RF receiver they are a good choice for characterizing the effect of substrate noise coupling. This work evaluates the impact of substrate noise on three different low noise amplifiers designed for typical specifications of a 2.4GHz wireless application in a 0.25µm CMOS process.

A single-ended cascode architecture with inductive source degeneration was selected since it has been shown to provide superior noise performance compared to other singleended topologies [1], [7] and [14]]. This configuration is a very popular amplifier for CMOS applications.

Differential amplifiers are typically used in situations where non thermal noise sources limit an amplifier's sensitivity. Since the input and output signals are differential common mode noise is cancelled [8], [9]. The rejection of common mode substrate noise, in particular, has been sited by many as a reason for using the differential architecture [10], [11] and [12]. A differential amplifier was added to this work to evaluate its substrate noise rejection performance.

In a typical wireless receiver application the received signal is captured by the antenna and then band pass filtered before entering the LNA. One significant drawback of the differential amplifier is that it requires a balun to convert the single-ended signal from the filter output to a differential signal for the amplifier input, as shown in Figure 2. Baluns implemented on-chip consume valuable die area and can have more than 1dB of loss resulting in a significant degradation of the receiver noise figure. Off-chip baluns have more than 0.3dB loss but are large, especially at 2.4GHz, and expensive. The obvious solution to this problem is to use a single-ended amplifier allowing the balun to be eliminated. However, in applications where common mode noise rejection is required due to substrate or other noise, a single-ended signal is a problem. Another approach is to use a quasi-differential LNA since it has a single-ended input and a differential output. Due to the inherent asymmetry of this amplifier, its ability to reject common mode substrate noise is questionable. For this reason, the quasi-differential amplifier was also included in this evaluation.



Figure 2. A comparison of receivers with differential and quasi-differential LNA's.

### **3** CIRCUIT DESIGN AND LAYOUT

## **3.1** Stepped Buffer

The stepped buffer used to emulate the digital circuit noise is described in [13]. The circuit consists of seven inverter stages where each stage is e (2.718) times larger than the preceding stage as shown in Figure 3. All stages, except for the last, are loaded with an additional inverter.



Figure 3. Block diagram of the stepped buffer.

Four stepped buffers are placed at various locations on the chip to identify the impact of spacing on substrate noise. Due to the limited number of pins available in the package used for testing, all four stepped buffer circuits share common power and ground pins. Each stepped buffer has its own input pin.

### 3.2 Single-ended LNA

### 3.2.1 Design

Figure 4 shows the basic amplifier circuit. M0 is the common source input stage, M1 is the common gate output stage and M2 is used to set the dc bias current. A power dissipation of 8mW was selected for this amplifier since this is typical of 2.4GHz WLAN applications. The LNA was designed using the method established in [14] for a fixed power dissipation.

In general, noise figure is defined as the ratio of the signal-to-noise ratio at the input to the signal-to-noise ratio at the output. The expression for minimum noise figure for the single-ended amplifier is:

$$F_{\min} = 1 + \frac{2.4\gamma}{\alpha} \left( \frac{\omega_o}{\omega_T} \right) \tag{1}$$

where  $\gamma$  is a constant taken as 4/3,  $\alpha$  is a constant related to the power dissipation as defined in [14], and  $\omega_0$  is the center frequency. For short channel devices, the unity gain frequency,  $\omega_T$ , is inversely proportional to the device gate length, L. This means that the lowest noise figure is achieved for the shortest gate lengths. As a result, the minimum gate length of 0.24 $\mu$ m for the process under consideration was selected for both M0 and M1.

The expression for the gate width at which the minimum noise figure is achieved is approximated by:

$$W_{opt} \approx \frac{1}{3\omega_o LC_{ox}R_s}$$
(2)

where the gate oxide capacitance is  $C_{ox}$  and the amplifier source impedance is  $R_s$  chosen as 50 ohms in this case. For a gate length of  $0.24\mu m$ , a width of  $300\mu m$  was selected for M0.

The width of transistor M1 was set to  $200\mu$ m, optimizing the simulated noise figure performance of the circuit. To minimize the noise figure the gates of both M0 and M1 were fingered. The distributed gate resistance for a gate contacted on both sides can be modeled as a lumped resistance [27] given by:

$$R_{gate} = \frac{R_{sq}W}{12N^2L} \tag{3}$$

As shown in this equation, the gate resistance,  $R_{gate}$ , is reduced as the number of fingers, N, is increased.  $R_{sq}$  is the resistance per square of the polysilicon gate. Using this relation as a guideline and SPICE simulations, 50 fingers for M0 and 25 fingers for M1 yielded good noise performance.

For a common source amplifier with inductive source degeneration the input impedance can be approximated as:

$$Z_{in} = s(L_s + L_g) + \frac{1}{sC_{gs}} + \omega_T L_s$$
(4)

where  $C_{gs}$  is the gate to source capacitance of the MOSFET and the inductors are as shown in Figure 4.

Using this relation as a starting point,  $L_s$  is calculated to provide a 50 ohm real input impedance and  $L_g$  is sized to cancel the imaginary portion of the input impedance at the operating frequency of 2.4GHz. The amplifier output is conjugate matched to 50 ohms by appropriately selecting  $L_d$  and  $C_{out}$ .



Figure 4. Circuit schematic of the single-ended LNA.

#### 3.2.2 Layout

The amplifier die photo is shown in Figure 5. The path from the LNA input pin to the gate of M0 is short to minimize resistive metal losses which degrade noise figure performance. The input bond pad was shielded from the substrate to avoid the deleterious affects of substrate resistance on the noise figure. The shielded bond pad consisted of metal layers 5 through 3 all connected together for the input signal, metal 2 was left floating for mechanical isolation, and metal 1 was tied to the on-chip ground plane providing the shield. This is similar to the structure described in [15]. L<sub>g</sub> was implemented using the input bond wire and a high Q inductor on the PCB to optimize the noise figure performance. Placing L<sub>g</sub> off-chip allowed the input match to be tuned compensating for package and bond wire differences between the simulated pre-

fabrication and actual post-fabrication circuit performance. The source degeneration inductor,  $L_s$ , was implemented with two bond wires in parallel to the PCB ground. M0 and M1 were each surrounded with  $0.6\mu$ m wide p+ guard rings. This improves the noise figure by reducing the substrate resistance of the bulk node and provides shielding from substrate noise. The guard rings were tied to a large on-chip ground grid. The ground grid was constructed with all five metal layers and several p+ substrate taps. It is connected to the PCB ground through four bond wires resulting in a low impedance ground path. C<sub>out</sub> and L<sub>d</sub> were both implemented on-chip. A 3.5 turn 3.74 nH square spiral inductor with a Q of 5.6 was selected for L<sub>d</sub> since accurate models were available from the foundry [28].



Figure 5. Die photograph of the single-ended LNA.

### **3.3 Differential LNA**

### 3.3.1 Design

The classical source coupled pair differential amplifier described in [8] and shown in Figure 6 was used. The amplifier consists of two single-ended amplifiers connected as a source-coupled pair as shown in Figure 6. The DC bias current in each half, the transistor sizes and the component values of  $L_s$ ,  $L_g$ ,  $L_d$  and  $C_{out}$  are the same as the single-ended amplifier. By taking advantage of the circuit's symmetry and using half-circuit analysis the approximate input impedance can be expressed as:

$$Z_{in} = 2 \left[ s(L_s + L_g) + \frac{1}{sC_{gs}} + \omega_T L_s \right]$$
(5)

This is simply twice that for the single-ended amplifier, or in this design it is 100 ohms. Baluns were used to convert the differential input and output signals to single-ended signals. Neglecting the loss of the input balun, the noise figure performance of this amplifier is expected to be the same as its single-ended counterpart.



Figure 6. Circuit schematic of the differential LNA.

### 3.3.2 Layout

The amplifier die photo is shown in Figure 7. A symmetrical layout is vital for achieving maximum common mode noise rejection. From Figure 7 it is apparent that two single-ended amplifiers have been placed with one mirroring the other. A short input path and off-chip input matching were used similar to the single-ended amplifier. Both of the LNA input bond pads (IN+, IN-) and the gate biasing (VGG) bond pad were shielded. The source degeneration inductors,  $L_s$ , are three turn, 0.92nH inductors routed on the top metal layer and have a simulated Q of 3.67. The inductors are connected to a common bias point on the axis of symmetry where the biasing transistors M4 and M5 are located. No guard rings were placed around these biasing transistors. The RF transistors,

M0, M1, M2 and M3 were laid out exactly the same way as in the single-ended amplifier. The guard rings for the RF transistors and the substrate taps for the bias transistors are tied to a large on-chip ground grid similar to the one used for the single-ended amplifier. The ground grid is also routed around the source inductors providing them with some shielding. A low impedance path from the on-chip ground to the PCB ground is provided through four package pin connections in parallel. The drain inductors, L<sub>d</sub>, are identical to those used in the single-ended amplifier. Since the LNA is placed in the corner of the die the output trace routing is not perfectly symmetrical. The lengths of both traces were made the same to ensure that the capacitive coupling to the substrate is matched. However, one output trace is closer to stepped buffer 2 than the other. Unfortunately, this was unavoidable.



Figure 7. Die photograph of the differential LNA.

### 3.4 Quasi-Differential LNA

#### 3.4.1 Design

A novel quasi-differential amplifier shown in Figure 8 was developed. It is similar to the differential circuit with a few notable exceptions. Firstly, the virtual ground node of the source coupled pair is replaced with a ground as shown in [16], [17]. Secondly, the input signal is single-ended and fed into only one of the common source input MOSFET's, M0. The drain of M0 is capacitively cross coupled by  $C_x$  to the gate of the other common source MOSFET, M1. Since a common source amplifier has a phase shift of 180° and a common gate amplifier has a 0° phase shift, the positive output is 180° out of phase with respect to the negative output, as desired.

The input impedance of this amplifier is approximately the same as the single-ended amplifier as given by Equation (4). The MOSFET sizes and all component values remain unchanged from the singled ended design. The sizing of the cross-coupling capacitor,  $C_x$ , is critical to ensure that the two outputs are equal in magnitude and opposite in phase. The termination impedance on the gate of M1,  $L_{g1}$ , was also crucial for proper amplitude and phase balance. A high Q off-chip inductor was used for  $L_{g1}$  to avoid degradation of the overall amplifier noise figure and to ensure that the layout at the gates of M1 and M0 is as symmetric as possible.



Figure 8. Circuit schematic of the quasi-differential LNA.

### 3.4.2 Layout

Figure 9 is a die photograph. In order to achieve as much common mode substrate noise rejection as possible the layout was made symmetric. It consists of two halves mirrored about the axes of symmetry similar to the differential circuit. The biasing FET, M4, is located on the axis of symmetry. A mirror image dummy of the cross-coupling capacitor,  $C_x$ , was connected to the drain of M1. A large on-chip ground plane was created, similar to that used on the other amplifiers. The ground plane was made the same area as in the differential LNA and is also connected to the PCB ground through

four package pins. The differential output traces are asymmetric since the amplifier is placed in the corner of the IC. However, the lengths of both output paths were made the same.



Figure 9. Die photograph of the quasi-differential LNA.

## 3.5 Integrated Circuit

Two test chips were fabricated using a 0.25µm, single poly, five metal CMOS process. The layout of each chip is identical but one was fabricated in a heavily doped CMOS substrate and the other in a lightly doped CMOS substrate. The packaged test chip for the lightly doped substrate is shown in Figure 10. The three LNA's are placed in the corners of the die and one or more digital noise sources are located near each amplifier. Note that the chip is large, 4.1x4.1mm, since other test structures that are not part of this evaluation were also fabricated.



Figure 10. Photograph of the packaged die.

# 3.6 Packaging and Printed Circuit Board

Each chip was assembled into a micro lead frame 48 pin plastic package (MLF48). This package was selected since it has very low inductive and capacitive lead parasitics and the die paddle is exposed on the bottom side allowing it to be directly soldered to the printed circuit board (PCB) ground plane. The chips were attached to the die paddle with non-conductive epoxy. Gold bond wires 0.001 inches in diameter were used.

The packaged parts were mounted on identical 0.031 inch thick, 2 layer, FR4 test boards. Isolated power supplies on the PCB provide 2.5V to the stepped buffers and 2.0V to the LNA's. A detailed description of the test board is provided in Appendix A.

#### 4 MODELING

### 4.1 Circuit Modeling

The input signal and power pins for the stepped buffers are located in the upper right corner of the package resulting in long on-chip interconnects of 4 to 7 mm in length. Detailed modeling of these power, ground and input lines was performed for the PCB, package and die. Accurate modeling of the resistive losses as well as the parasitic inductances and capacitances was particularly important since these give rise to supply droop and ground bounce. This noise, in addition to the switching noise from the stepped buffer MOSFET's, propagates through the substrate into the low noise amplifiers.

In order to obtain good correlation between the measured and simulated RF and substrate noise performance for the amplifiers, a detailed SPICE model was essential. Critical interconnects and transmission lines on the PCB were accounted for. A package model was created from three dimensional electromagnetic (EM) simulation results provided by the manufacturer. The self and mutual inductances of the bond wires were modeled by applying the geometric approximations outlined in the EIA/JESD59 bond

wire modeling standard and using FastHenry [18]. Bond wire capacitances were modeled using FastCap [19]. SPICE models for the on-chip interconnects, bond pads, inductors and capacitors were extracted from EM simulations. More detailed information on the models that were used is provided in Appendix B.

### 4.2 Substrate Noise Modeling

### 4.2.1 General Substrate Modeling Approach

There are two general substrate types for CMOS technologies. Figure 11 is a cross section showing the typical resistivity of each substrate layer. The capacitive affects of the substrate are assumed to be small enough at 2.4GHz that they can be ignored. A detailed explanation of this assumption is provided in Appendix C.



Figure 11. Cross sections of heavily and lightly doped substrates.

Noise is injected into the substrate by the inverters in the stepped buffer through substrate taps and capacitive coupling at the PN junctions and interconnects. This noise is transferred through the resistive substrate to the LNA. The noise couples into the LNA through PN junction and interconnect capacitances and by the MOSFET threshold voltage change due to the "body effect" [5].

A substrate model is extracted for calculating the noise coupling [5]. It consists of mutual resistances,  $R_{ij}$ , from each contact to all other contacts and the self resistance,  $R_{ii}$ , from each contact to the die backplane. The contacts were taken as the bulk contacts, MOSFET areas, and interconnect areas. A Green's function based simulator called EPIC was used to obtain the substrate resistances [24]. Capacitances from interconnects to the substrate were calculated from the process area and fringing capacitance data.

#### 4.2.2 Modeling of the Heavily Doped Substrate and the Single-ended LNA

Figure 12 is a simplified cross section of the heavily doped substrate showing some of the critical components in the substrate network. All of the self resistances are connected to the single substrate node. Since the epi layer is fairly resistive, the mutual resistance between contacts separated by more than five times the epi layer thickness is large and can often be ignored [6]. The mutual resistance between closely spaced contacts such as the FETs and their bulks is significant and must be taken into account.  $C_{11}$  is the capacitance from the stepped buffer input clock interconnect to the substrate and  $C_{66}$  represents the capacitance from the output bond pad to the substrate.  $C_e$  represents the capacitance of the epoxy between the chip backplane and the die paddle.



Figure 12. Cross section and lumped element model for the heavily doped substrate.

## 4.2.3 Modeling of the Lightly Doped Substrate and the Single-ended LNA

A simplified substrate network cross section for the lightly doped case is shown in Figure 13. Since the substrate bulk is resistive, use of a single substrate node is no longer valid. Each self resistance is connected to the die-paddle through a capacitor that is proportional to the size of the contact. The mutual resistances are much smaller than in the heavily doped case and are proportional to the separation between two contacts [6]. The output inductor,  $L_d$ , and gate interconnect were found to be important in the lightly doped case. Their oxide capacitances and self resistances are also represented in Figure 13 [20].



Figure 13. Cross section and lumped element model for lightly doped substrate.

## **5 EXPERIMENTAL RESULTS**

#### 5.1 Measurement Setup

The amplifier S-parameter measurements were completed with a Agilent 8720 network analyzer. Substrate noise measurements were made as follows. A Tektronix AWG520 was used to generate the clock signal applied to the input of the stepped buffers. For the single-ended LNA the stepped buffer clock inputs are driven with a 2Vp-p, 50% duty cycle, 39MHz square wave. To reduce the levels of unwanted clock harmonics coupling through the PCB and package, a 2Vp-p, 39MHz sinusoidal signal is used to drive the stepped buffers for the differential and quasi-differential LNA measurements. The LNA input was generated with a -18dBm sinusoidal signal from an Agilent 8665A signal generator and the LNA output spectrum was monitored with an Agilent E4440A spectrum analyzer with the detector set to peak mode.

### 5.2 Measured RF Performance of Each LNA

The measured performance for each of the amplifiers at 2.4GHz in the heavily and lightly doped substrates is summarized in Table 1. Since the measurements include the test PCB losses, the gain is lower than expected for a 0.25µm process for LNA's with on-chip probing.

		Lightly Dop	oed	Heavily Doped		
	Single- ended	Differential	Quasi- differential	Single- ended	Differential	Quasi- differential
S11 (dB)	-14.7	-26.7	-11.4	-15.3	-22.7	-13.6
S12 (dB)	-26.1	-39.3	-47.3	-25.4	-37.6	-50.1
S21 (dB)	8.8	8.7	10.2	8.6	8.3	9.7
S22 (dB)	-17.0	-21.2	-17.3	-17.4	-20.2	-15.5

Table 1. Measured performance of the LNA's at 2.4GHz in both substrates.

## 5.3 Substrate Coupled Noise Measured in the Single-ended LNA

The measured substrate coupled noise from stepped buffer 4 into the single-ended LNA is shown in Figure 14. There are both harmonic and intermodulation (IM) tones at the LNA output [3]. The tones at 2.301, 2.340, 2.379, 2.418, 2.457 and 2.496 GHz are the 59<sup>th</sup>, 60<sup>th</sup>, 61<sup>st</sup>, 62<sup>nd</sup>, 63<sup>rd</sup> and 64<sup>th</sup> harmonics, respectively, of the 39MHz clock. The

tones appearing between these are IM products arising from the 1<sup>st</sup> and 2<sup>nd</sup> harmonics of the clock mixing with the 2.4GHz RF carrier. When the bias to the LNA is removed the IM products disappear but the harmonics remain.

Typically, noise levels in a lightly doped substrate are lower than those in a heavily doped substrate due to the increased resistive isolation of the substrate. In this case the IM products produced by the odd clock harmonics are at least 2dB lower in the lightly doped substrate and the IM products produced by the even clock harmonics are more than 8dB lower in the lightly doped substrate. However, the direct clock harmonics are surprisingly similar in magnitude for both substrates.

To confirm that this data is valid, measurements were made from stepped buffer 2 which is located about seven times farther from the single-ended LNA than stepped buffer 4. These measurements, presented in Figure 15, show that the noise remains similar for the heavily doped case indicating that the coupling is independent of separation. For the lightly doped case, the noise dropped significantly demonstrating that the noise decreases with an increase in separation as expected [6]. One additional check was performed to confirm that coupling mechanisms other than through the substrate do not dominate the measurement results. A clock signal was input to the stepped buffer while the buffer's DC bias was turned off. The spectrum at the LNA output was then measured as described previously. No noise coupling was observed. Note that this is only valid for the lightly doped substrate because some noise coupling from the clock interconnect to the single substrate node is expected in the heavily doped substrate.



Figure 14. Measured substrate noise from stepped buffer 4 at the output of the singleended LNA in heavily and lightly doped substrates.


Figure 15. Measured substrate noise from stepped buffer 2 at the output of the singleended LNA in heavily and lightly doped substrates.

### 5.4 Substrate Coupled Noise Measured in the Differential LNA

The noise coupling into the differential LNA was evaluated by making measurements from stepped buffers 1, 2 and 4. Referring to Figure 7, stepped buffer 1 is located above the amplifier for injecting asymmetric noise. Stepped buffer 2 is placed to the left of the amplifier on its axis of symmetry, hence its noise should be injected equally between both halves of the amplifier circuit. Stepped buffer 4 is located about  $3000\mu$ m away allowing the effects of noise injected symmetrically from large distances to be evaluated. The measured noise from each of these stepped buffers in both types of substrates is presented in Figure 16, Figure 17 and Figure 18. From the results in Figure 16 and in Figure 17 it can be seen that the IM noise is 3 to 12 dB lower in the lightly doped substrate. This is because the guard rings around the active devices are more effective in the lightly doped substrate. However, the harmonic noise is large in both substrates. An explanation of this unexpected result is provided in Section 6.

Figure 18 is a comparison of the noise generated from stepped buffer 4 coupling into the differential amplifier for both the heavily and lightly doped substrates. The harmonics are higher in the heavily doped substrate because the common bulk node readily conducts noise into the amplifier. Compared to the single-ended LNA in a heavily doped substrate, the harmonics are about 10dB lower. This confirms that the differential circuit is providing only about 10dB of rejection explaining why the harmonic noise is not completely eliminated. Even though the noise injection is essentially symmetric, imbalances in the amplifier circuitry limit the differential cancellation. In the lightly doped substrate the noise is attenuated by the large lateral resistances which increase with greater physical separation between the noise generator and amplifier. As a result, the harmonics and IM products are generally below the measurement noise floor in the lightly doped substrate.



Figure 16. Measured substrate noise from stepped buffer 1 at the output of the differential LNA in heavily and lightly doped substrates.



Figure 17. Measured substrate noise from stepped buffer 2 at the output of the differential LNA in heavily and lightly doped substrates.



Figure 18. Measured substrate noise from stepped buffer 4 at the output of the differential LNA in heavily and lightly doped substrates.

## 5.5 Substrate Coupled Noise Measured in the Quasi-differential LNA

The noise coupling from stepped buffers 3 and 4 into the quasi-differential LNA was also measured. The measured results for both substrate types are presented in Figure 19<sup>1</sup> and Figure 20. Referring to Figure 7, stepped buffer 3 is placed just below the amplifier on its axis of symmetry. Stepped buffer 4 is located about  $3000\mu$ m below the amplifier.

<sup>&</sup>lt;sup>1</sup> Stepped buffer 3 on the heavily doped IC could not be used since the clock input was not connected due to a layout problem.

From Figure 19 it can be seen that even though stepped buffer 3 is symmetrically located there is significant harmonic and intermodulation noise. These noise levels are similar to those for the differential LNA.

The performance in the heavily and lightly doped substrates from stepped buffer 4 is compared in Figure 20. The IM noise in the heavily doped substrate is very high compared to the other amplifier architectures. The cross coupling capacitor,  $C_x$ , couples substrate noise into the gate of M1 increasing the IM noise. The harmonics are only 2dB to 10dB lower in the lightly doped substrate. This is likely because ground bounce noise is injected from stepped buffer 3 which is close to the output interconnects of the amplifier. The IM noise is typically 15dB lower in the lightly doped substrate. This indicates that the shielding near the amplifier input circuitry is much more effective in the lightly doped substrate. Also, for separations greater than about 300µm the resistive isolation of the lightly doped substrate is higher [6].



Figure 19. Measured substrate noise from stepped buffer 3 at the output of the quasidifferential LNA in the lightly doped substrate.



Figure 20. Measured substrate noise from stepped buffer 4 at the output of the quasidifferential LNA in heavily and lightly doped substrates.

#### 6 ANALYSIS OF RESULTS

## 6.1 Analysis of the Single-ended LNA

From the measured results presented in Figure 14, it is evident that the harmonic noise is similar in both substrates but the IM noise is lower in the lightly doped substrate. When the amplifier was turned off, the IM noise dropped but the harmonic noise remained virtually unchanged. This indicates that the coupling mechanisms for the IM products are due to mixing with the RF carrier in the active devices whereas the harmonics are dominated by coupling through passive circuitry directly to the amplifier output.

Based on these measurements, a more exact identification of the substrate noise coupling mechanisms is not possible making it necessary to perform more detailed noise simulations. The single-ended cascode LNA structure is common to all three amplifiers. Therefore, by using the single-ended LNA simulations as an example, useful insight can be gained into the substrate noise coupling mechanisms of all three amplifiers.

### 6.1.1 Measured and Simulated Single-ended LNA Performance

The first step in performing simulations on the single-ended LNA is to verify that the modeling of the LNA properly predicts its RF performance. Table 2 compares the measured and simulated performance at 2.4GHz. In general there is good agreement between the simulated and measured results.

	Lightly Doped		Heavily Doped	
	simulated	measured	simulated	measured
S11 (dB)	-14.4	-14.7	-16.6	-15.3
S12 (dB)	-24.4	-26.1	-26.3	-25.4
S21 (dB)	9.1	8.8	8.8	8.6
S22 (dB)	-14.2	-17.0	-15.1	-17.4
NF(dB)	2.5		2.6	
Input P1dB (dBm)	-10.3	-11.2	-10.5	-11.5
Current at 2V (mA)	4.00	4.03	3.97	4.07

Table 2. Summary of the single-ended LNA performance.

The simulated substrate noise for the single-ended LNA was obtained by applying the substrate modeling approach previously described. The substrate network was added to the SPICE netlist for the combined amplifier and stepped buffer circuits. MOSFET junction capacitances are automatically accounted for since they are part of the BSIM3v3 device model. A transient analysis was performed and then a discrete Fourier transform was computed on the amplifier output signal revealing the desired signal and the undesired noise.

Figure 21 and Figure 22 compare the simulated and measured substrate noise spectrums in both the heavily and lightly doped substrates. As can be seen, reasonably good agreement is demonstrated between simulations and measurements for the IM products and the harmonics with both substrates.



Figure 21. Single-ended LNA output power spectrum for the heavily doped substrate.



Figure 22. Single-ended LNA output power spectrum for the lightly doped substrate.

#### 6.1.2 Noise Coupling Comparison for Stepped Buffers 2 and 4

Figure 23 compares the measured noise coupling from stepped buffers 2 and 4 to the single-ended LNA in the heavily doped substrate. The harmonic and IM noise from stepped buffer 2 is typically within a few dB of the noise produced by stepped buffer 4. In the heavily doped substrate this is expected since the noise coupling is independent of the distance between the amplifier and noise source for separations greater than 5 times the epi layer thickness [6]. Noise measurements from stepped buffers 2 and 4 in the lightly doped substrate are compared in Figure 24. The harmonics from stepped buffer 2 are at least 6 dB lower. The IM noise from stepped buffer 2 is also lower but limited by the measurement noise floor. These results indicate that the noise rejection of the lightly

doped substrate is superior to the heavily doped substrate when the amplifier is located far away from the noise source.



Figure 23. Harmonic and IM noise coupling into the single-ended LNA in the heavily doped substrate. (a) Harmonics of the clock. (b) IM products of the clock and the input RF signal.



Figure 24. Harmonic and IM noise coupling into the single-ended LNA in the lightly doped substrate. (a) Harmonics of the clock. (b) IM products of the clock and the input RF signal.

# 6.1.3 Noise Coupling Mechanisms for the Single-ended LNA

Additional simulations were run to identify the salient mechanisms for both the IM and harmonic noise. The results are plotted in Figure 25. With the heavily doped substrate, 90% of the IM noise power is due to coupling into the bulk node of M0 from the single substrate node through the self resistance,  $R_{44}$  in Figure 12. The remaining noise is dominated by coupling through  $R_{55}$  onto the chip ground plane and then into the bulk node of M0. In the lightly doped case, 95% of the IM noise is due to coupling into the trace connecting the LNA input bond pad, gate of M0 and  $R_g$ . This mechanism is represented by the mutual resistance  $R_{24}$  in Figure 13. The rest of the noise is dominated by coupling to the chip ground and then into the bulk node of M0.

Referring again to Figure 25, the coupling mechanisms for the harmonics have also been identified. In the heavily doped substrate, the noise on the single substrate node capacitively couples onto bond pads. The 2V supply bond pads account for 47% of the noise power and an additional 38% is from the LNA output bond pad. Coupling into inductor  $L_d$  accounts for much of the remaining noise. In the lightly doped case, 67% of the harmonic noise power couples into  $L_d$  through mutual resistances such as  $R_{27}$  and  $R_{17}$ and the oxide capacitance  $C_{77}$ . Noise coupling into the bond pads, M0 gate interconnect and other portions of the circuit accounts for the remainder. It is interesting to find that the harmonic noise is not dominated by coupling into MOSFET's M0 and M1. This is because these MOSFET's have an effective substrate contact area almost two orders of magnitude smaller than the bond pads or output inductor and they are shielded with guard rings.



Figure 25. Noise coupling mechanisms as a percentage of the total noise power. (a) Intermodulation noise. (b) Clock harmonic noise.

#### 6.1.4 Noise Mitigation for the Single-ended LNA

From the previous analysis it is evident that in a heavily doped substrate the single substrate node acts as a conduit spreading noise from the buffer to the amplifier. Reducing the noise voltage on the single substrate node should drop both the IM and harmonic noise. Simulations demonstrate that a die perimeter ring that is grounded with four down bonds, reducing the impedance to ground at low frequencies, decreases the IM noise. Attaching the die with conductive epoxy increased C<sub>e</sub>, providing a low impedance path to ground at 2.4GHz. Together, these diminished the noise coupling by at least 14 dB.

In the lightly doped substrate the noise couples into the LNA primarily through lateral resistances. Placing a grounded guard ring around the affected circuitry has been shown to be an effective method for reducing noise in lightly doped substrates [6], [20]. A 15µm wide p+ guard ring was placed completely around the LNA (including the inductor) separating it from the buffer. The guard ring was grounded to the die paddle at each end with down bonds. The simulated noise reduction for both the harmonics and the IM products was about 9dB.

#### 6.2 Analysis of the Differential LNA

Previous research has indicated that with a differential circuit, superior substrate noise isolation is expected in a heavily doped substrate compared to a lightly doped substrate [6]. In a heavily doped substrate, excellent noise rejection is anticipated for noise injected either on or off the circuit's axis of symmetry. This is because the noise currents tend to flow vertically from the common bulk node through R<sub>ii</sub> since R<sub>ij</sub> is typically large and, therefore, not a significant path for the noise. In a lightly doped substrate, there is no common substrate node to distribute noise equally to each half of the differential circuit. The lateral substrate resistances, R<sub>ij</sub>, tend to dominate the coupling and as a result, better rejection is expected for symmetrically injected noise than asymmetrically injected noise.

Many people have used differential amplifiers because of their ability to reject common mode substrate noise. Previous work has shown that intermodulation products in a balanced amplifier arise from low frequency signals on the substrate coupling into the circuit at the current source MOSFET's, M4 and M5 [3]. However, simulations indicate that for the design in this paper, the intermodulation products are dominated by coupling into the RF MOSFET's, M0, M1, M2, and M3 (in the heavily doped substrate). This can be explained by considering the small-signal amplifier input,  $v_i$ , and the substrate noise,  $v_{bs}$ . It can be shown that the small-signal output current of a differential source coupled pair has the two terms given by:

$$i_{o} = g_{m}v_{i} + \frac{g_{mb}v_{bs}v_{i}}{V_{GS} - V_{T}}$$
(6)

The first term is due to the signal applied at the amplifier input. The second term is the product of the input signal and the substrate noise which is responsible for the IM noise at the amplifier output. Note that there is no term dependent only on the substrate noise confirming that common mode substrate noise is not directly amplified by this circuit. However, the common mode substrate noise mixes with the input signal producing intermodulation noise which is not cancelled by the differential circuit. A detailed explanation is provided in Appendix D.

#### 6.2.1 Noise Coupling in the Heavily Doped Substrate

Figure 26 compares the measured noise coupling from stepped buffers 1, 2 and 4 in the heavily doped substrate. Harmonics of the clock are similar in magnitude for the noise from stepped buffers 1 and 2 but several dB lower for the noise injected from stepped buffer 4. Ideally the harmonic noise should be similar for all three cases and is expected to be at a low level since this common mode noise will cancel when the positive and negative amplifier outputs are combined in the output balun. However, this is not the case for several reasons. Firstly, since stepped buffer 2 is very close to the output interconnects and stepped buffer 1 is close to the upper  $L_s$  and  $L_d$ ,  $R_{ij}$  imbalance becomes significant. This  $R_{ij}$  imbalance explains why the harmonic noise is much higher from stepped buffers 1 and 2. Secondly, the common mode rejection of the amplifier is limited by circuit imbalances due to differences in bondwire lengths and PCB mounted matching components. This accounts for the noise measured from stepped buffer 4. When the DC bias to the LNA is removed the harmonic levels drop 3 to 5 dB demonstrating that much of the harmonic noise couples in at the LNA input where  $L_s$  is the most likely offender since the input bond pads are shielded from the substrate. The coupling mechanism at the LNA output is expected to be into inductors  $L_d$  and the output bond pads as it was for the single-ended LNA.

The IM products produced from the clock harmonics are similar in magnitude for all three noise generators. The only exceptions are the IM products due to the first clock harmonic (these are the ones closest to 2.4GHz). By making coupling measurements with a clock applied to input of stepped buffer 1 but the DC bias to the stepped buffer turned off, it was confirmed that the noise coupling is through the PCB and not the substrate for the IM products produced from the fundamental of the clock signal. As previously explained, intermodulation products are produced when substrate noise couples into any of the active devices. Common mode substrate noise mixes with the differential mode amplifier signals resulting in differential mode noise. Since the active devices have guard rings around them R<sub>ii</sub> is the dominant path for the IM noise making it independent of the noise generator location.



Figure 26. Harmonic and IM noise coupling into the differential LNA in the heavily doped substrate. (a) Harmonics of the clock. (b) IM products of the clock and the RF input signal.

#### 6.2.2 Noise Coupling in the Lightly Doped Substrate

The noise produced by stepped buffers 1, 2 and 4 in the lightly doped substrate is compared in Figure 27. Contrary to expectations, the harmonic levels from the asymmetric (stepped buffer 1) and symmetric (stepped buffer 2) noise sources are similar. Unfortunately, stepped buffer 1 is located too close to the output interconnects and as a result injects more noise into the negative amplifier output than the positive output. By measuring the harmonic levels with the DC bias to the LNA turned off additional insight is gained. With stepped buffer 1 the harmonic noise drops by more than 5dB when the amplifier bias is removed indicating that most of the noise is contributed at the amplifier input. The noise is most likely coupling into  $L_s$ . For stepped buffer 2, the harmonic levels drop only about 2dB revealing that most of the noise is injected at the amplifier output. This noise is likely coupling into the output inductors,  $L_d$ , the output interconnects, and the output bond pads, similar to the singled ended LNA. The harmonic noise produced by stepped buffer 4 is typically about 15dB lower. The added distance between the LNA and the noise generator has increased  $R_{ij}$  by about an order of magnitude. In addition, the noise is injected into the amplifier more symmetrically so there is further reduction due to the common mode rejection of the differential circuit.

The IM products produced by the harmonics of the stepped buffer clock signal are generally very low. Excellent IM rejection is achieved since the guard rings around the active devices block most of this noise. For stepped buffers 1 and 2 the IM noise is similar in level. One explanation is that ground bounce noise is injected at the substrate taps for both stepped buffers regardless of which one is being clocked.



Figure 27. Harmonic and IM noise coupling into the differential LNA in the lightly doped substrate. (a) Harmonics of the clock. (b) IM products of the clock and the input RF signal.

### 6.3 Analysis of the Quasi-Differential LNA

The main advantage of the quasi-differential LNA is that it converts a single-ended input signal into a differential output eliminating the need for a balun. This requires that the input circuitry be asymmetric, hence the rejection of common mode noise coupled into the input stage of the amplifier is expected to be poorer than it is for the differential LNA.

# 6.3.1 A Comparison of the Noise Coupling in Lightly and Heavily Doped Substrates

Since the amplifier input circuit is asymmetric, common mode noise at the input is not rejected very well. As a result, the harmonic noise in the heavily doped substrate is dominated by coupling into the amplifier input circuitry. This was confirmed by observing that the harmonics drop several dB when the power is removed from the amplifier in the heavily doped substrate. Harmonics in the lightly doped substrate are only a few dB lower compared to the heavily doped substrate. Both stepped buffers 3 and 4 share power and ground interconnects. When stepped buffer 4 is clocked, ground bounce noise is injected from the substrate taps of stepped buffer 3.

The IM products resulting from the clock harmonics are more than 10dB higher in the heavily doped substrate mostly because this substrate provides less isolation. In the heavily doped substrate, coupling into the input MOSFET bulk nodes is expected to be a dominant mechanism, as it was in the single-ended LNA. In addition, the cross-coupling capacitor  $C_x$  also has substantial capacitive coupling from its lower electrode to the substrate. The IM noise is much weaker in the lightly doped substrate largely due to the added resistive isolation of this substrate. The guard rings around the input MOSFETS and the p+ taps around  $C_x$  also help reduce the IM noise in the lightly doped substrate.

# 6.3.2 A Comparison of the Noise Coupling in the Differential and Quasi-Differential Amplifiers

The measurement results from stepped buffer 3 for the quasi-differential amplifier and stepped buffer 2 for the differential amplifier in the lightly doped substrate are compared

in Figure 28. The harmonics are typically more than 4dB higher in the differential LNA. This is likely due to stepped buffer 1 injecting additional ground bounce noise from its substrate taps into the differential LNA. The harmonics in the quasi-differential LNA are due to layout asymmetries such as the proximity of the negative output to the stepped buffer and mismatching in bond wires and off-chip components. The IM products are similar in magnitude for both amplifiers close to the carrier (up to +/-78MHz) becoming larger farther from the carrier for the quasi-differential amplifier. This indicates that the quasi-differential LNA has excellent IM rejection performance near the center frequency of the design but it degrades for higher order IM products. The capacitive coupling from the substrate into the cross-coupling capacitor increases with increasing frequency accounting for this degradation.



Figure 28. Harmonic and IM noise coupling into the differential and quasi-differential LNA's in the lightly doped substrate. (a) Harmonics of the clock. (b) IM products of the clock and the input RF signal.

#### 7 CONCLUSIONS

Three different architectures of 2.4GHz low noise amplifiers have been fabricated on both heavily and lightly doped CMOS substrates. They include the traditional singleended cascode and fully differential amplifiers as well as a novel quasi-differential amplifier. Noise at the amplifier outputs was measured for each amplifier in both types of substrates from noise sources located near and far away from the amplifier circuits. For noise sources located within a few hundred micrometers of the amplifiers, the harmonic noise was similar in the lightly and heavily doped substrates. However, the IM noise was lower in the lightly doped substrate where the shielding provided by the guard rings around the transistors is more effective. For noise sources located a few thousand micrometers from the amplifiers, the lightly doped substrate provided much better noise rejection of IM and harmonic noise.

Resistive substrate models were employed to simulate the noise injected into the single-ended LNA. Using these models and simulations, the major noise coupling mechanisms were identified. In both types of substrates, harmonics of the clock couple into bond pads and the inductor at the LNA output. Intermodulation products of the clock and the RF carrier are produced by noise coupling directly into the input transistor in the heavily doped substrate, or into the gate interconnect in the lightly doped substrate. Suitable noise mitigation methods were selected and simulated. A combination of conductive epoxy die attach and a die perimeter ring reduced the noise by greater than

14dB in the heavily doped substrate. For the lightly doped substrate, a p+ guard ring resulted in a 9dB noise reduction.

With the differential amplifier, the IM noise was found to be greater in the heavily doped substrate compared to the lightly doped substrate. Analysis revealed that differential amplifiers provide no rejection of common mode noise that mixes with the differential signal in the active devices. For this reason a heavily doped substrate should be avoided in applications where IM noise is of concern.

The quasi-differential amplifier was found to have poorer noise performance than the differential amplifier in the heavily doped substrate. However, in the lightly doped substrate, the noise immunity of the quasi-differential amplifier was comparable to the differential amplifier over bandwidths of about 10% of the center frequency. The elimination of the input balun makes this amplifier attractive for many receiver applications.

Future work is needed to improve substrate modeling tools so that the effects of interconnects, passive components and the die attach material can be accounted for automatically, especially for the analysis of lightly doped substrates. A means of performing substrate network sensitivity analysis would be particularly powerful as it could be used to identify the coupling mechanisms making it easier to select appropriate noise mitigation methods. An effective means of protecting the differential LNA against intermodulation noise needs to be explored. In addition, the quasi-differential LNA concept could be researched further.

#### **BIBLIOGRAPHY**

[1] T. H. Lee, "CMOS RF: no longer an oxymoron," *IEEE RFIC Symposium*, pp. 3-6, June 1999.

[2] D. Leenaerts and P. DeVreede, "Influence of substrate noise on RF performance," *European Solid-State Circuits Conference*, pp. 255-258, Sept. 2000.

[3] M. Xu, D. K. Su, D. K. Shaeffer, T. H. Lee, and B. A. Wooley, "Measuring and modeling the effects of substrate noise on the LNA for a CMOS GPS receiver," *IEEE J. Solid-State Circuits*, vol. 36, pp. 473-485, March 2001.

[4] C. Soens, C. Crunelle, P. Wambacq, G. Vandersteen, S. Donnay, Y. Rolain, M. Kuijk, and A. Barel, "Characterization of substrate noise impact on RF CMOS integrated circuits in lightly doped substrates," *Proceedings of IMTC 2003*, pp. 1303-1308, May 2003.

[5] N. K. Verghese, "Extraction and Simulation Techniques for Substrate Coupled Noise in Mixed-Signal Integrated Circuits," *Ph.D. Dissertation*, Carnegie Mellon University, Aug. 1995.

[6] R. Gharpurey and R. G. Meyer, "Modeling and analysis of substrate coupling in integrated circuits," *IEEE J. Solid-State Circuits*, vol. 31, pp. 344-353, March 1996.

[7] Y. Ge and K. Mayaram, "A comparative analysis of CMOS low noise amplifiers for RF applications," *Proceedings of the IEEE International Symposium on Circuits and Systems*, vol. 4, pp. 349-352, 1998.

[8] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, New York, NY, 2002.

[9] J. J. Zhou and D. J. Allstot, "Monolithic transformers and their application in a differential CMOS RF low-noise amplifier," *IEEE J. Solid-State Circuits*, vol. 33, pp. 2020-2027, Dec. 1998.

[10] D. K. Shaeffer, A. R. Shahani, S. S. Mohan, H. Samavati, H. R. Rategh, M. M. Hershenson, M. Xu, C. Yue, D. J. Eddleman, and T. H. Lee, "A 115-mW, 0.5µm CMOS GPS receiver with wide dynamic-range active filters," *IEEE J. Solid-State Circuits*, vol. 33, pp. 2219-2231, Dec. 1998.

[11] J. C. Huang, R. Weng, C. Hsiao, and K. Lin, "A 2V 2.4GHz fully integrated CMOS LNA with Q-enhancement circuit," *Proceedings of APMC*, vol. 3, pp. 1028-1031, Dec. 2001.

[12] F. Svelto, S. Deantoni, G. Montagna, and R. Castello, "An 8mA, 3.8dB NF, 40dB gain CMOS front-end for GPS applications," *Proceedings of ISLPED*, pp. 279-283, Jul. 2000.

[13] S. Adluri, "Contributions to substrate noise due to supply coupling and pin parasitics," *M.S. Thesis*, Oregon State University, Nov. 2003.

[14] D. K. Shaeffer and T. H. Lee, "A 1.5V, 1.5GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, pp. 745-759, May 1997.

[15] J. T. Colvin, S. S. Bhatia, and K. K. O, "Effects of substrate resistances on LNA performance and a bondpad structure for reducing the effects in a silicon bipolar technology," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1339-1344, Sept. 1999.

[16] X. Yang, T. Wu, and J. McMacken, "Design of LNA at 2.4GHz using 0.25µm technology," *Silicon Monolithic Integrated Circuits in RF Systems Topical Meeting*, pp. 12-14, Sept. 2001.

[17] F. Behbahani, J. C. Leete, Y. Kishigami, A. Roithmeier, K. Hoshino, and A. A. Abidi, "A 2.4-GHz low-IF receiver for wideband WLAN in 0.6-μm CMOS - architecture and front end," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1908-1916, Dec. 2000.

[18] M. Kamon, C. Smithhisler and J. White, "FastHenry user's guide," Massachusetts Institute of Technology, Cambridge, MA, 1996.

[19] K. Nabors, S. Kim, J. White and S. Senturia, "FastCap user's guide," Massachusetts Institute of Technology, Cambridge, MA, 1992.

[20] A. L. L. Pun, T. Yeung, J. Lau, F. J. R. Clement, and D. K. Su, "Substrate noise coupling through planar spiral inductor," *IEEE J. Solid-State Circuits*, vol. 33, pp. 877-884, June 1998.

[21] Anonymous, "Mixed signal circuit techniques," Application Note AN-280, Analog Devices, Norwood, MA.

[22] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analyis and Design of Analog Integrated Circuits*, Fourth edition, John Wiley & Sons, New York, NY, 2001.

[23] W. Sansen, "Distortion in elementary transistor circuits," *IEEE Transactions on Circuits and Systems - II*, vol. 46, pp. 315-325, March 1999.

[24] C. Xu, K. Mayaram, and T. Fiez, "EPIC user's manual," School of EECS, Corvallis, OR, 2003.

[25] F. Martorell, D. Mateo, and X. Aragones, "Modeling and evaluation of substrate noise induced by interconnects," *IEEE Proceedings of Design, Automation and Test in Europe Conference and Exhibition 2003*, pp. 524-529, March 2003.

[26] C. Xu, T. Fiez, and K. Mayaram, "High frequency lumped element models for substrate noise coupling," *IEEE International Workshop on Behavioral Modeling and Simulation*, pp. 47-50, Oct. 2003.

[27] B. Razavi, R. Yan, and K. F. Lee, "Impact of distributed gate resistance on the performance of MOS devices," *IEEE Transactions on Circuits and Systems - I*, vol. 41, pp. 750-754, Nov. 1994.

[28] M. T. Yang and Y. J. Wang, "TSMC 0.25um mixed signal 1P5M+ salicide 2.5V/3.3V RF SPICE models," Document T-025-MM-SP-005, Taiwan Semiconductor Manufacturing Co., Taiwan, July 2001.

# **APPENDICIES**

# **Appendix A Printed Circuit Board**

This appendix includes the complete PCB schematic with component values. In addition a photograph of the PCB along with general notes that explain the PCB and components is provided.



Figure A-1. Schematic of the printed circuit board.



Figure A-2. Schematic of the printed circuit board.



Figure A-3. Photograph of the test PCB.

## **PCB Design Notes**

- Off-chip matching was placed as close to the IC package as possible to reduce PCB parasitics.
- 2. Baluns were needed to convert the differential signals to single-ended signals that could be connected to test instrumentation. Commercially available baluns (the large rectangular components in the PCB photo) were used to minimize insertion loss and save space. Unfortunately only a single-ended 50 ohm to differential 50 ohm (single-ended 25 ohm) type was available. The balanced output was matched to 100 ohm (50 ohm single-ended) with a 1.65nH/1.2pF "L" match.
- The 1.65nH inductors are air core for high Q hence low resistive losses and minimal NF degradation.

- 4. The RF transmission lines are all 50 ohm microstrip with solder mask relief in some places to add additional matching components if needed.
- 5. Each LNA has 50 ohm input and output connections. SMA connectors were selected since they have good performance at 2.4GHz, are readily available, and easy to interface to test instrumentation.
- 6. The power supply inputs can be connected directly or through low noise regulators which add more isolation between the digital and analog circuits.
- 7. A ground plane was added on the top side of the PCB with several vias to the bottom side ground to reduce unwanted coupling between signal traces (improve isolation). The vias also ensure a true ground plane helping to eliminate unwanted resonances in the ground plane.
- 8. A star ground approach [21] is used where the on-chip grounding for the stepped buffers and each LNA is separate. These grounds are then connected to a common point on the PCB directly beneath the IC to prevent ground currents from flowing in the substrate. The stepped buffer and LNA ground planes are separated on the PCB, except for the common connection point beneath the package. This avoids unwanted ground loops where return currents sharing a common path can induce noise from the buffer circuit into the LNA circuit.
- 9. Power supply decoupling and bypass capcitors were placed as close to the IC pins as possible. Note that several bypass capcitors were placed in parallel on the 2V bias line for the single-ended LNA. This reduced the parasitic inductance of the supply path which increased the gain of the LNA.

10. A single input is provided for the stepped buffers, this input signal is then routed to the desired buffer by the switches shown to the left of the stepped buffer input connector.
#### Appendix B Interconnect and Passive Device Modeling

#### Interconnect and passive device modeling on the PCB

All simulations were done with Spectre RF. The 50 ohm transmission lines on the PCB were modeled as lossy transmission lines in Spectre. In areas where the differential transmission lines were close together a 4 port S-parameter file was extracted using Momentum. This file was then linked into Spectre. The baluns were modeled using the 3 port S-parameter data supplied by the manufacturer. When SPICE models were available for the passive R, L and C components they were used. If they were not available then ideal components were assumed.

## Modeling of the package and bond wires

The package, including bond wires, dominates the off-chip parasitics hence accurate modeling was important for obtaining good simulation results. Capacitance and inductance matricies for the package were available from the package manufacturer. This data was converted into a SPICE model for Spectre. Initial (pre IC layout) bond wire modeling consisted of the self inductance of each bond wire and the mutual inductance to the two adjacent bond wires. The self resistances and mutual capacitances were ignored. These inductance values (in nH) were calculated using the approximate equations from [8] shown below. In these equations,  $\ell$  is the bond wire length in meters and *r* is the bond wire radius, taken to be  $25 \times 10^{-6}$ m for this project, M is the mutual inductance, and D is the separation between the two bond wires in meters.

$$L \cong 2x10^{-7} \ell \left[ \ln \left( \frac{2\ell}{r} \right) - 0.75 \right]$$
(B-1)

$$M = \frac{\mu_o \ell}{2\pi} \left[ \ln \frac{(2\ell)}{D} - 1 + \frac{D}{\ell} \right]$$
(B-2)

These equations were suitable for initial circuit simulations but were not accurate enough for final post-layout analysis. In particular, the mutual inductance term was found to have large errors (>50%) since the spacing between the actual bond wires is non uniform. Post-layout modeling for the bond wires was done by estimating the bond wire lengths from a photograph taken of one of the packaged devices before the encapsulant was applied. This information was then used in conjunction with the geometric approximations outlined in the EIA/JESD59 bond wire modeling standard to develop a three dimensional physical representation of the bond wires. The self resistances and self and mutual inductances were then extracted using FastHenry [18]. Bond wire self and mutual capacitances were modeled using FastCap [19].

#### Modeling of on-chip interconnects and passive components

SPICE models for the on-chip interconnects were created by obtaining the interconnect resistance and capacitance data from the TSMC 0.25µm process documentation. The interconnect inductances and substrate spreading resistances were extracted from simulations using Momentum. The interconnect model shown below was selected. For long interconnects, longer than 1/10 of a wavelength, multiple sections

were cascaded together.  $L_s$  and  $R_s$  are the series inductance and resistance of the trace,  $C_{ox}$  is the capacitance through the SiO<sub>2</sub> layer to the substrate and  $R_{sub}$  is the substrate spreading resistance.



Figure B-1. SPICE model for on-chip interconnect.

SPICE models for both the shielded and unshielded bond pads were extracted from Momentum.  $C_{ox}$  is the oxide capacitance to the substrate and  $R_{sub}$  is the substrate spreading resistance. For the shielded bond pads  $R_{sub}$  was essentially 0 ohms and the ground is connected to the shield.



Figure B-2. SPICE model for bond pad.

The model for the 3.5 turn spiral inductor used for the output matching on the amplifiers was provided by TSMC. However, this model was for thick top metal. Since

a standard top metal was used for these chips the value of  $R_s$  in the model was appropriately increased. A TSMC model was not available for the 3 turn source inductor in the differential amplifier. This model was developed by simulating the S-parameters in Momentum. The model parameters were then optimized until the S-parameters from the lumped-element model matched the S-parameters from Momentum.



Figure B-3. SPICE model for spiral inductor.

The models shown here are for the heavily doped substrate where the ground in these figures is the single substrate node. This ground is then connected to the ground on the PCB through the capacitance of the epoxy bonding the chip to the die paddle as described in Section 4.2.2. The lateral resistances  $R_{ij}$  in the substrate model are attached to the node between  $C_{ox}$  and  $R_{sub}$ . With the lightly doped substrate, an additional capacitance is placed between  $R_{sub}$  and the ground which represents the capacitance of the die attach epoxy. The ground, in this case, becomes the PCB ground as described in Section 4.2.3.

## Appendix C Resistive Substrate Modeling Approximation

The question of whether or not a resistive substrate model is valid to apply for this work is looked at in two ways. Firstly, recent research [26] indicates that the resistive model is valid up to about 1GHz. The simulations in this research are based on a maximum substrate resistivity of  $20\Omega$ cm. Since the substrate used in this experiment has about half the resistivity it is reasonable to extend the valid range for resistive model up to about 2GHz. Using this approach, the resistive model assumption is borderline, but should not result in significant error.

The second view is based on the assumption that the substrate is homogeneous and is both resistive and capacitive [5], [20]. Therefore the admittance of a cubic shaped section of substrate can be modeled as a parallel RC network as shown in Figure C-1.



Figure C-1. Equivalent circuit for a section of homogeneous substrate.

From Equation (C-1) it is apparent that the substrate admittance is simply 1/R for low frequencies and increases for high frequencies.

$$Y = \frac{1}{R} + j\omega C = \frac{1 + j\omega RC}{R}$$
(C-1)

The relaxation time or substrate time constant is defined as the inverse of the 3dB frequency and is given by:

$$\tau = \frac{1}{\omega_{_{3dB}}} = \rho \varepsilon_o \varepsilon_r \tag{C-2}$$

where  $\rho$  is the volume resistivity of the substrate,  $\varepsilon_0$  is the permittivity of free space and  $\varepsilon_r$  is the relative dielectric constant of the substrate taken as 11.9 [5]. The largest relaxation time is in the lightly doped substrate and is 10.54 ps. This corresponds to a 3dB frequency of 15.1GHz. Since 2.4GHz is about 1/6 of the 3dB frequency for the substrate the assumption of a resistive model is reasonable.

#### Appendix D Analysis of Substrate Noise in the Differential Amplifier

The approximate drain current for a MOSFET in saturation is given by the common second-order expression below [22]. Where k' is a constant equal to the product of the charge carrier mobility and gate oxide capacitance. W and L are the transistor width and length,  $V_{GS}$  is the applied gate to source voltage and  $V_T$  is the gate threshold voltage.

$$I_D = \frac{k'W}{2L}(V_{GS} - V_T)^2$$



Figure D-1. Drain current in an N-channel MOSFET.

Adding the AC components to the DC terms in the above equation one obtains,

$$I_{D} + i_{d} = \frac{k'}{2} \frac{W}{L} (V_{GS} + v_{gs} - V_{T} - v_{t})^{2}$$

where the  $v_t$  term accounts for the AC noise injected into the bulk node. This expression can be rearranged to solve for  $i_d$  by using an expanded version of the method outlined in [23]. First I<sub>D</sub> is subtracted from both sides of the equation and then both sides are divided by I<sub>D</sub>.

$$\frac{i_d}{I_D} = \frac{1}{I_D} \frac{k'W}{2L} (V_{GS} + v_{gs} - V_T - v_t)^2 - 1$$

The quiescent portion of the gate to source overdrive voltage term can now be factored out and then the result is simplified.

$$\frac{i_d}{I_D} = \frac{1}{I_D} \frac{k'}{2} \frac{W}{L} (V_{GS} - V_T)^2 \left( 1 + \frac{v_{gs} - v_t}{V_{GS} - V_T} \right)^2 - 1$$

$$\frac{i_d}{I_D} = \left( 1 + \frac{v_{gs} - v_t}{V_{GS} - V_T} \right)^2 - 1$$

$$i_d = \frac{2I_D v_{gs}}{V_{GS} - V_T} - \frac{2I_D v_t}{V_{GS} - V_T} - \frac{2I_D v_{gs} v_t}{(V_{GS} - V_T)^2} + \frac{I_D v_{gs}^2}{(V_{GS} - V_T)^2} + \frac{I_D v_t^2}{(V_{GS} - V_T)^2}$$
(D-1)

The threshold voltage  $V_T$  is given as:

$$V_T = V_{TO} + \gamma \left( \sqrt{V_{SB} + \phi} - \sqrt{\phi} \right)$$

where  $V_{TO}$  is the threshold voltage when  $V_{SB}$  is zero.  $\varphi$  is a constant related to the Fermi level and  $\gamma$  is another device parameter as detailed in [22]. By taking the derivative with respect to time, the time varying or small-signal portion of the threshold voltage is found.

$$v_t = \frac{\mathcal{W}_{sb}}{2\sqrt{V_{SB} + \phi}} = -\chi v_{bs} \tag{D-2}$$

The symbol  $\chi$  is used to simplify the expression.

The small signal transconductances from the gate and bulk to the drain are given as below [22].

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{2I_D}{V_{GS} - V_T} \tag{D-3}$$

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = g_m \chi \tag{D-4}$$

Substituting (D-2), (D-3), and (D-4) into (D-1) and then simplifying results in an expression for the small signal drain current as a function of the small signal gate to source and source to bulk voltages.

$$i_{d} = g_{m}v_{gs} + g_{mb}v_{bs} + \frac{g_{mb}v_{bs}v_{gs}}{V_{GS} - V_{T}} + \frac{g_{m}v_{gs}^{2}}{2(V_{GS} - V_{T})} + \frac{g_{mb}\mathcal{X}v_{bs}^{2}}{2(V_{GS} - V_{T})}$$
(D-5)

The first term on the right hand side is the familiar expression for the fundamental AC portion of the output current. The second term is the output current due to a small-signal on the bulk (substrate noise) which gives rise to the harmonic noise. The third term is the product of the small-signal inputs at the substrate and the gate resulting in intermodulation noise. The last two terms can be ignored since their frequency components are not near the operating frequency of the amplifier.

A representation of a differential amplifier is given in Figure D-2. In this amplifier, the total output current is the difference in the output currents from each side of the amplifier.

 $i_{o} = i_{o}^{+} - i_{o}^{-}$ 



Figure D-2. Drain currents in a differential amplifier.

By substituting in the first three terms of (D-5) and then simplifying, the expression for the small-signal output current is obtained.

$$i_{o} = g_{m} \frac{v_{i}}{2} + g_{mb} v_{bs} + \frac{g_{mb} v_{bs} \frac{v_{i}}{2}}{V_{GS} - V_{T}} - \left( -g_{m} \frac{v_{i}}{2} + g_{mb} v_{bs} - \frac{g_{mb} v_{bs} \frac{v_{i}}{2}}{V_{GS} - V_{T}} \right)$$
(D-6)

$$i_{o} = g_{m}v_{i} + \frac{g_{mb}v_{bs}v_{i}}{V_{GS} - V_{T}}$$
(D-7)

The small-signal output current has two terms. The first is due to the input signal applied to the amplifier. The second term is the product of the input signal and the substrate noise. This shows that intermodulation noise is not cancelled by the differential circuit. Note that the output term consisting of only the substrate noise is not present hence the harmonic noise is cancelled.

#### **Appendix E** Additional Amplifier Measurements

## Single-ended LNA

The performance for the single-ended LNA at 2.4GHz is summarized in Table E-1. Since the measurements include the test PCB losses, the gain is lower than expected in this process for a LNA with on-chip probing. In addition, the bypass capacitor from the 2V supply to ground was placed off-chip adding bond wire inductance which also reduced the gain. The measured versus simulated S-parameters are plotted in Figures E-1 and E-2. Generally there is good agreement except for the resonant dip shown in S22 which is related to parasitics on the PCB.

	Lightly Doped		Heavily Doped	
	simulated	measured	simulated	measured
S11 (dB)	-14.4	-14.7	-16.6	-15.3
S12 (dB)	-24.4	-26.1	-26.3	-25.4
S21 (dB)	9.1	8.8	8.8	8.6
S22 (dB)	-14.2	-17.0	-15.1	-17.4
NF(dB)	2.5		2.6	
Input P1dB (dBm)	-10.3	-11.2	-10.5	-11.5
Current at 2V (mA)	4.00	4.03	3.97	4.07

Table E-1. Summary of the single-ended LNA performance.



Figure E-1. S-parameters for the single-ended LNA on the lightly doped substrate.



Figure E-2. S-parameters for the single-ended LNA on the heavily doped substrate.

### **Differential LNA**

The differential amplifier performance at 2.4GHz is summarized in Table E-2. In theory the noise figure should be similar to the single-ended amplifier. However, the losses in the input balun add at least 0.35dB to the noise figure. Similarly, the losses in both the input and output baluns reduce the gain compared to the single-ended case. Figures E-3 and E-4 compare the simulated and measured S-parameters for the lightly and heavily doped substrate versions of the amplifiers.

	Lightly Doped		Heavily Doped	
	simulated	measured	simulated	measured
S11 (dB)	-23.1	-26.7	-19.5	-22.7
S12 (dB)	-39.2	-39.3	-40.2	-37.6
S21 (dB)	9.0	8.7	8.8	8.3
S22 (dB)	-35	-21.2	-19.7	-20.2
NF(dB)	3.0	_	3.1	_
Input P1dB (dBm)	-8.3	-8.8	-8.0	-9.0
Current at 2V (mA)	8.14	8.24	8.12	8.30

Table E-2. Summary of the differential LNA performance.



Figure E-3. S-parameters for the differential LNA on the lightly doped substrate.



Figure E-4. S-parameters for the differential LNA on the heavily doped substrate.

# **Quasi-differential LNA**

The quasi-differential amplifier performance at 2.4GHz is summarized in Table E-3. The measured input return loss (S11) was several dB worse than the simulated S11. This is probably due to inductive coupling between the gate inductors,  $L_{g1}$  and  $L_{g2}$ . The measured isolation is 5 to 9 dB better than simulated. The noise figure is better than the differential amplifier since the insertion loss of the input balun has been eliminated from the circuit. However, some of this improvement is lost since the path from the input to the positive output passes through three FET's, instead of only two, reducing the overall amplifier noise figure. The gain is over 1dB higher than for the other amplifier architectures. This is because the source degeneration inductance is a little lower and the input power split is less than the 3dB found in the differential amplifier. Figures E-5 and E-6 compare the measured and simulated S-parameter magnitudes for the lightly and heavily doped substrate versions of the amplifier. The additional resonance in S22 is suspected to be from PCB parasitics.

	Lightly Doped		Heavily Doped	
	simulated	measured	simulated	measured
S11 (dB)	-14.1	-11.4	-18.1	-13.6
S12 (dB)	-42.1	-47.3	-41.0	-50.1
S21 (dB)	10.5	10.2	10.0	9.7
S22 (dB)	-18.5	-17.3	-19.0	-15.5
NF(dB)	2.8		3.0	
Input P1dB (dBm)	-9.3	-8.8	-8.5	-9.2
Current at 2V (mA)	8.10	7.98	8.02	8.06

Table E-3. Summary of the quasi-differential LNA performance.



Figure E-5. S-parameters for the quasi-differential LNA on the lightly doped substrate.



Figure E-6. S-parameters for the quasi-differential LNA on the heavily doped substrate.