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Title A CIRCUIT THAT RESPONDS TO A WIDE RANGE OF INPUT SIGNALS TO PROVIDE RELIABLE AUTOMATIC TRIGGERING

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The design and operation of a completely automatic trigger circuit is presented. This circuit differs from conventional trigger circuits in that manual control adjustments are not necessary. It will automatically provide stable triggering over a wide range of trigger signal amplitudes, repetition rates and waveshapes. The circuit consists of three semiconductor bistable circuits and decision logic so that triggering will occur for only those trigger signals that will not introduce time jitter in the output signal.

A CIRCUIT THAT RESPONDS TO A WIDE RANGE OF INPUT SIGNALS TO PROVIDE RELIABLE AUTOMATIC TRIGGERING

by

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INTRODUCTION

It is necessary in a number of electronic instruments to start or trigger an event or chain of events in time synchronism with a trigger signal. For example, it is required that the horizontal sweep in an oscilloscope be triggered at the proper time with respect to an incoming signal so that the time variation of that signal may be viewed. In a pulse generator, an output pulse may be initiated by the trigger signal. If the incoming or trigger signal is repetitive in the above cases, it is desirable for the display or output pulse to be kept in the same time relationship with each trigger signal.

Each trigger signal provides horizontal display information in an oscilloscope. The waveform displayed on the cathode-ray tube will appear in substantially the same place for each successive trace if the trace is triggered in constant time relationship for each trigger signal. If this time relationship varies, the waveform will have horizontal movement between traces. This movement is commonly termed jitter.

This thesis is a discussion of a trigger circuit that provides reliable, automatic triggering from trigger signals having a wide range of amplitudes, repetition rates and waveshapes. Automatic triggering is provided for positive trigger signals having peak amplitudes of 100 mV to 1 V. The frequency range is DC to 100 MHz.

This circuit was designed for a programmable oscilloscope that must reliably accept trigger signals from many different sources. This trigger circuit eliminates the need for manually operated control adjustments found in conventional trigger circuits. These control adjustments are used to avoid trigger jitter and mistrigger problems. The basic automatic trigger circuit consists of suitable circuitry and decision logic so that only those trigger signals will be accepted that will not introduce jitter or cause mistriggering in the output signal.

FUNCTION OF TYPICAL TRIGGER CIRCUITS

General operation of a trigger circuit as used in an oscilloscope will be explained using the block diagram of Figure 1. Consider an operation where a signal source is providing both a signal to be displayed and a time-related trigger signal. An output is generated by the trigger circuit for each accepted trigger signal to initiate the horizontal-sweep circuit. The vertical-signal processing and the horizontal-sweep circuits develop voltage levels representing signal amplitude and time respectively. These voltage levels deflect the electron beam in a cathode ray tube to display the signal waveform.

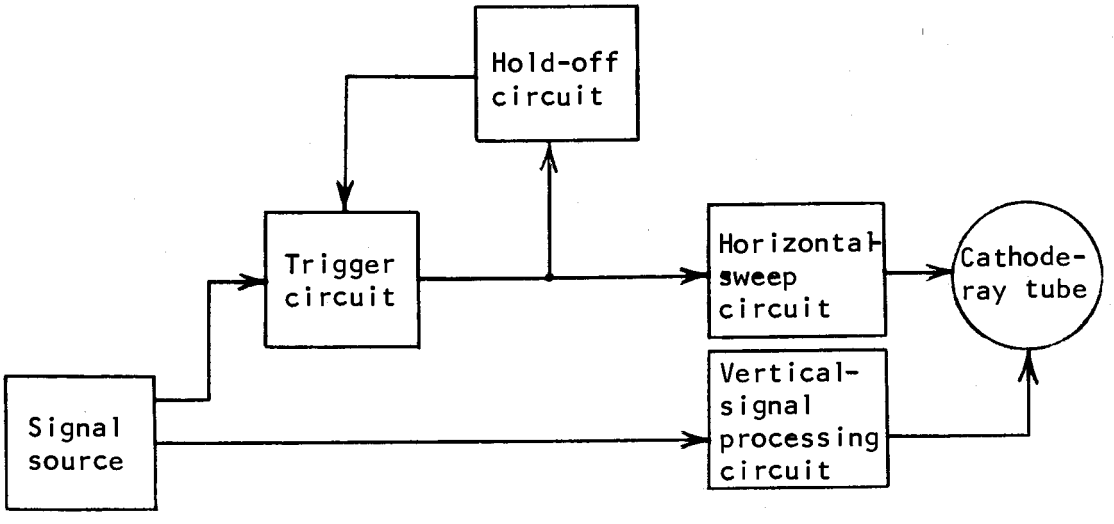


Figure 1. Block diagram of trigger circuit used in an oscilloscope.

The output of the trigger circuit is also connected to a hold-off circuit. The hold-off circuit inhibits the trigger circuit for a predetermined time after a trigger output signal occurs. This predetermined time interval is referred to as the hold-off interval and

must be long enough to allow the horizontal-sweep and vertical-signal processing circuits to complete their operation. The period of the trigger signal is often several orders of magnitude less than the sum of the hold-off and trigger reset intervals as shown in Figure 2. Many trigger signals occur during the hold-off interval, but no output signals will be generated by the trigger circuit. At the end of the hold-off interval, the trigger circuit is reset and can produce an output for the next trigger signal input. The reset interval is the time between the end of one hold-off interval and the start of the next. The duration of the reset interval is determined by the period of the trigger signal.

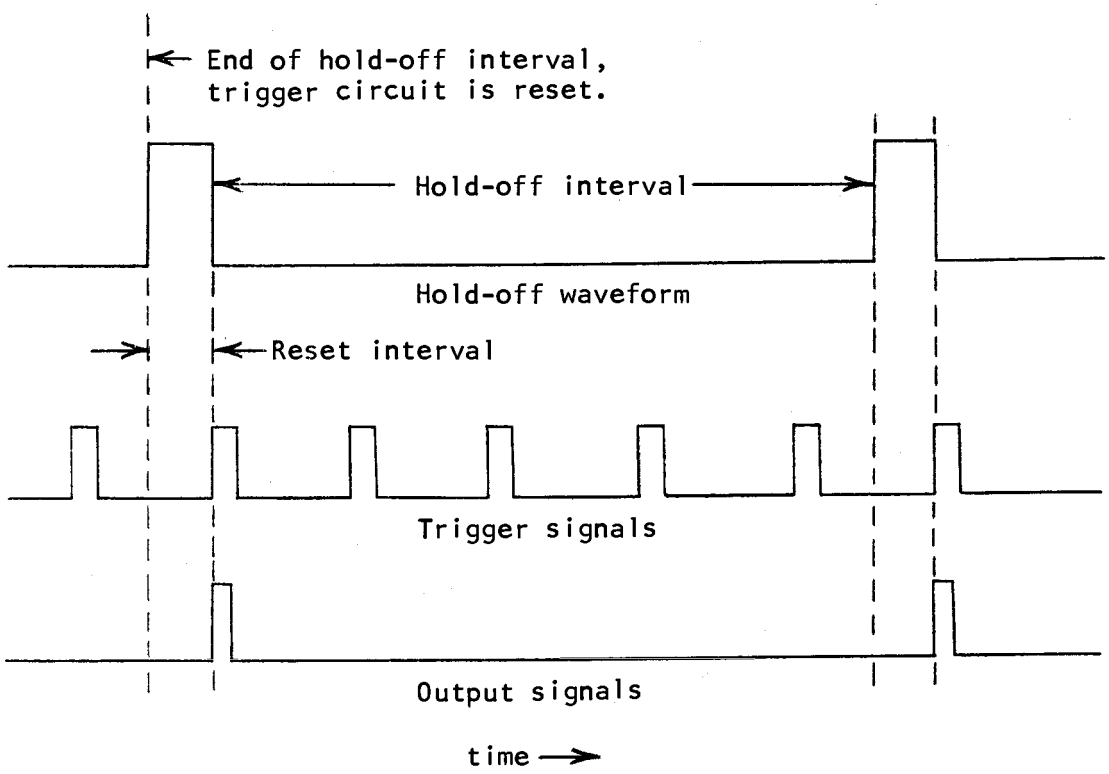


Figure 2. Trigger and hold-off circuit waveforms.

THE PROBLEM WITH CONVENTIONAL TRIGGER CIRCUITS

Conventional trigger circuits can generate output signals having jitter when the trigger circuit has just been reset. Jitter can occur when the sum of the hold-off and reset intervals (see Figure 2) is an integral multiple of the period of the trigger signal. The process of accepting only every n^{th} trigger signal is known as counting down. The time relationship between the output of the trigger circuit and the trigger signal can vary depending upon whether the n^{th} trigger signal occurs just before, coincident with, or just after the trigger circuit is reset. Time jitter has been reduced in practice by providing short-duration trigger signals or by generating short-duration pulses in a standardizing circuit within the trigger circuit. By making a standardized signal whose amplitude is fixed and whose pulse duration is shorter than observable jitter, the output will maintain time relationship whenever the trigger circuit is reset.

Figure 3 shows three time relationships with short-duration trigger signals occurring just before, coincident with and just after the trigger circuit is reset at time t_1. The trigger signal has occurred before the trigger circuit was reset in the figure 3a, and the trigger circuit will therefore not respond until the next trigger signal. The output signal has the correct time relation to the next trigger signal as shown by the dashed lines from the trigger signal to the leading edge of the output signal. Figures 3b and 3c also show acceptable time coincident trigger output signals.

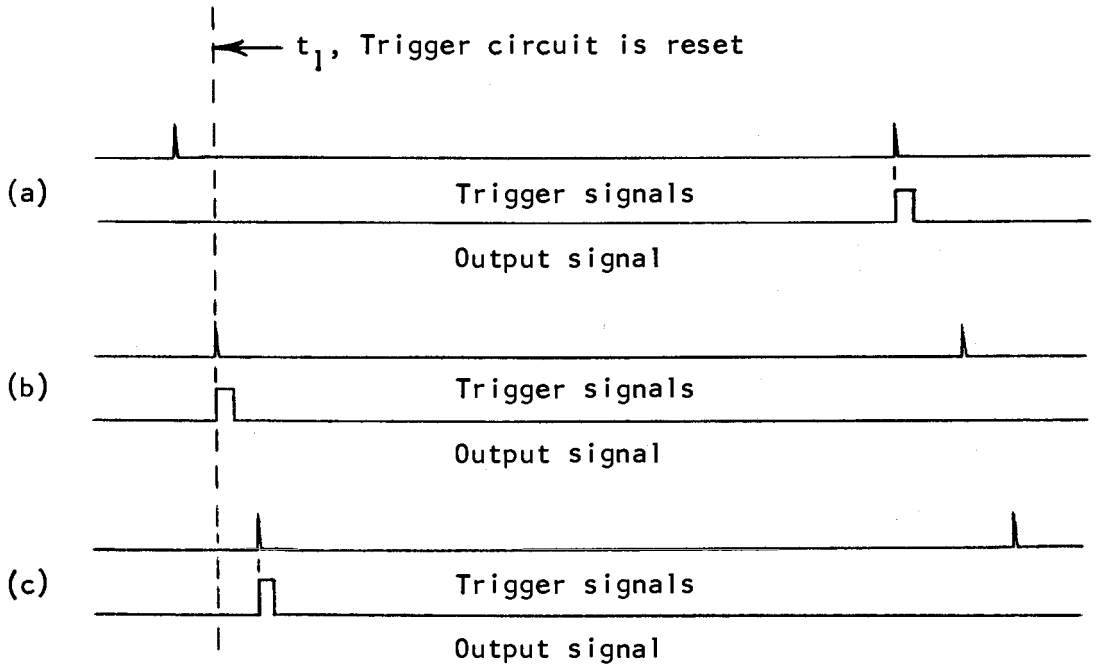


Figure 3. Short-duration trigger signals.

A common method of achieving a standardized drive pulse for a trigger circuit is through the use of a Schmitt trigger (1). The Schmitt trigger will change to its high-voltage state at a predetermined input voltage level independent of the waveshape of the input signal. Once this level is reached, the switching time of the Schmitt trigger is practically independent of the input signal. The output of the Schmitt trigger is differentiated and the time constant of this derivative is made equal to the switching time of the Schmitt trigger. Thus, short-duration pulses can be generated if the switching time of the Schmitt trigger is short.

When the pulse duration of the standardized pulse is no longer negligible with respect to observable jitter, control adjustments can be applied to avoid triggering problems. Three trigger situations

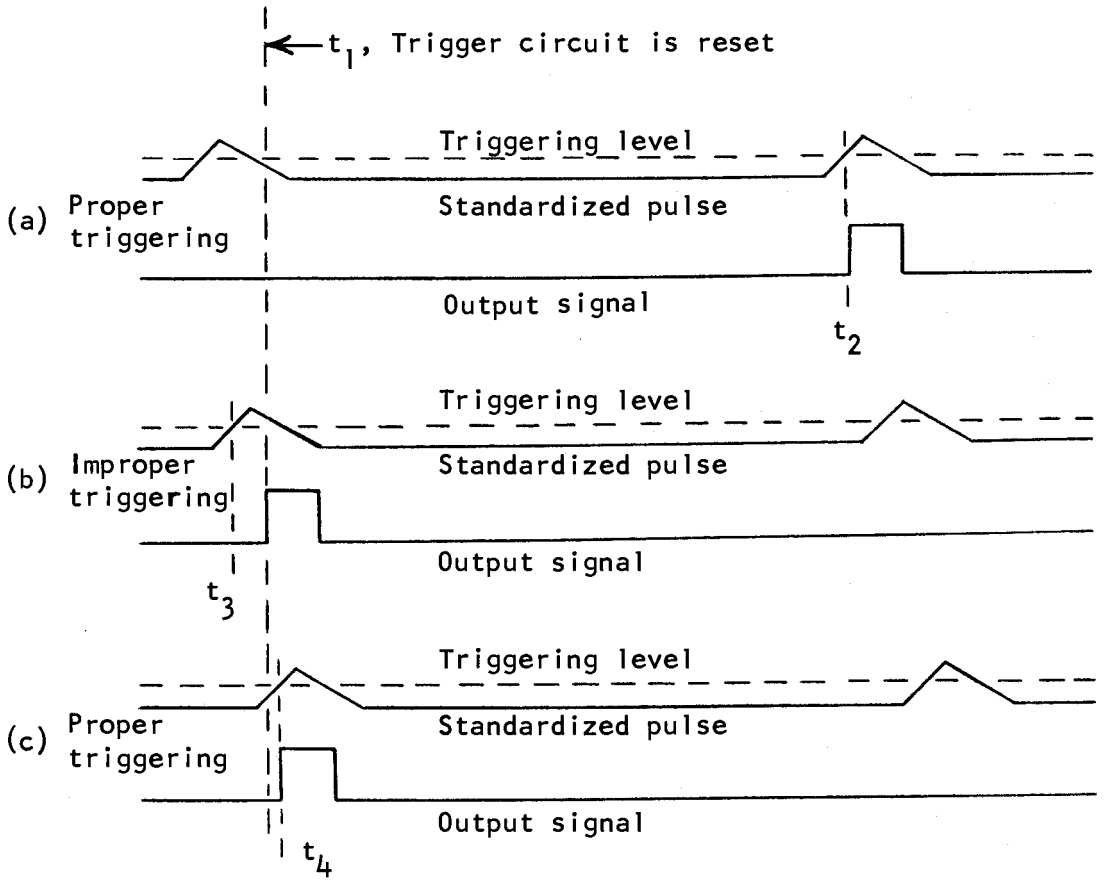


Figure 4. Example of proper and improper triggering.

are shown in figure 4 to show the relationship of the standardized-pulse leading edge to the output signal. The triggering level is shown as 50% of the amplitude for these pulses. In figure 4a, the trigger signal has dropped below the triggering level before reset time t_1 and the trigger circuit will not respond until the next standardized pulse occurs. Then proper trigger recognition takes place at time t_2. In figure 4c, proper triggering is apparent at time t_4. In figure 4b, the standardized pulse that is present at reset time t_1 exceeds the triggering level. An output signal is generated at reset time t_1, but should have been generated at time t_3. Proper trigger-

ing for figure 4b can be obtained by adjusting the duration of the hold-off interval so it does not end in time coincidence with the standardized pulse. This procedure has a disadvantage in that whenever the trigger-signal period is changed, an adjustment is usually necessary. This procedure also works, but with more difficulty when the trigger signal has not been standardized.

When output signals are generated as represented by figure 4b, jitter will result. Figure 5 is an illustration of a voltage step that would be displayed on an oscilloscope where trigger signals are alternately or randomly accepted as in figures 4a, 4b, and 4c. Triggering situations represented by figures 4a and 4c for correct triggering introduce no jitter and produce the overlapping traces of waveform 2. Waveform 1 represents traces having jitter and is caused by trigger-signal acceptance as in figure 4b. The width of the jitter is determined by the pulse duration of the standardized pulse. Waveform 1 can occur anywhere between the dashed-line waveform and the correctly triggered waveform 2.

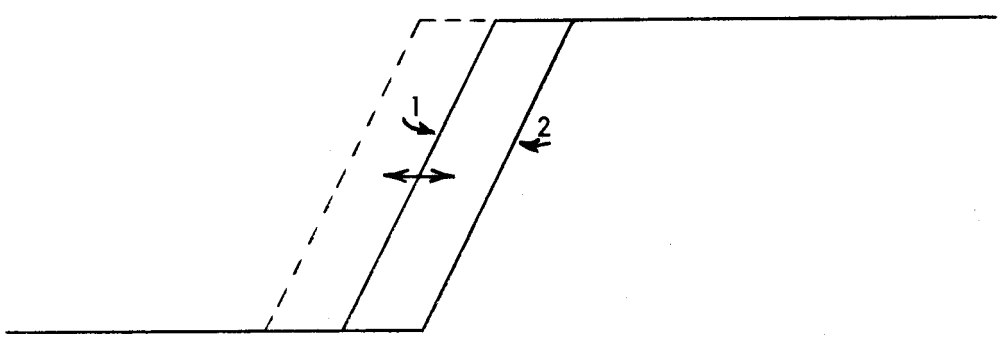


Figure 5. Illustration of a voltage step showing jitter.

DESCRIPTION AND OPERATION OF THE AUTOMATIC TRIGGER CIRCUIT

The automatic trigger circuit eliminates the problems associated with countdown as found in conventional trigger circuits. This is accomplished by the procedure in which the circuit is reset for receiving trigger signals at the end of the hold-off interval. The purpose of the main circuit elements of the trigger circuit will be explained with reference to the block diagram of figure 6.

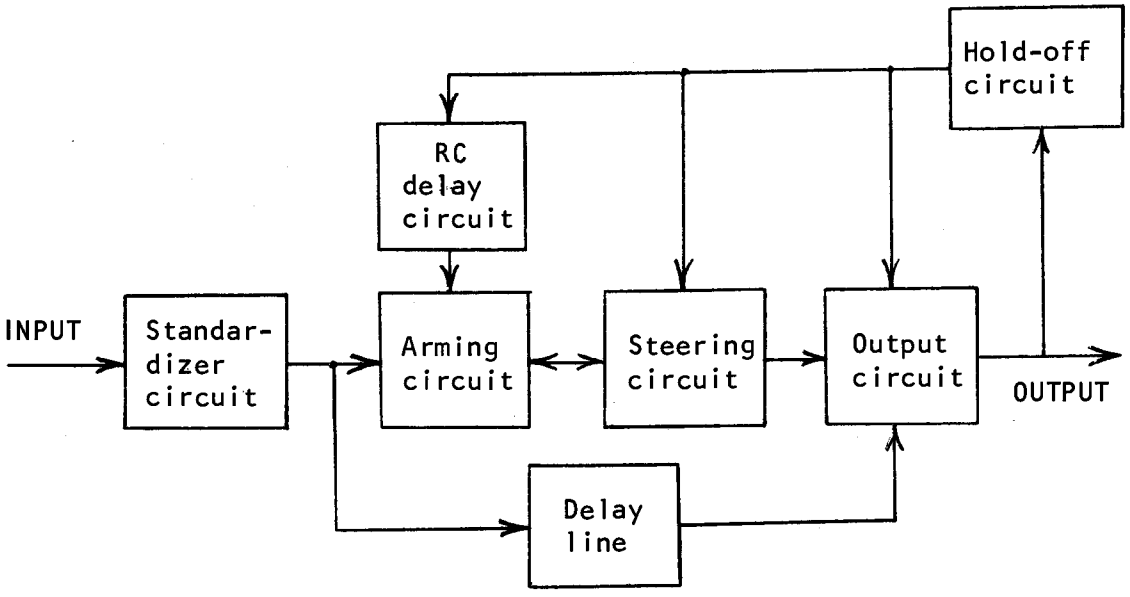


Figure 6. Block diagram of the automatic trigger circuit.

The standardizer, arming, and output circuits are bistable circuits; that is, two voltage-stable states exist. A current which exceeds a given amplitude will cause the bistable circuits to switch from an initial low-voltage state to a high-voltage state. The current must be reduced by an order of magnitude for these circuits to return to their low-voltage states. The standardizer circuit produces

a pulse of short duration and fixed amplitude for each trigger signal. Successive pulses maintain constant time relationship to each trigger signal.

Either the arming or the output circuit is referred to as armed if its current level is such that it can be triggered to its high-voltage state by a pulse from the standardizer circuit. Providing current that brings a circuit to the armed level is called arming. The hold-off circuit supplies current to the steering circuit which in turn provides current to either the arming or the output circuit depending upon the voltage states of the arming and output circuits. If the arming circuit is in its low-voltage state or if both the arming and output circuit are in their high-voltage states, the arming circuit will receive the current from the steering circuit. If the arming circuit is in its high-voltage state and the output circuit in its low-voltage state, the output circuit will receive the current from the steering circuit. Once either circuit is in its high-voltage state the lack of current from the steering circuit is not sufficient to cause either circuit to revert to its low-voltage state.

The arming circuit receives current from the steering circuit and the RC delay circuit. The RC delay circuit delays the current from the hold-off circuit to the arming circuit. This delay in arming of the arming circuit is necessary so that the current from the hold-off to the output circuit can have sufficient time to become stabilized before the arming circuit is armed. The delay line is provided to delay the application of the standardized pulse to the

output circuit. This delay allows for stabilization of the current that is steered to the output circuit after the arming circuit is triggered to its high-voltage state. The change to the high-voltage state in the output circuit is the output signal from the trigger circuit.

The complete operation of the trigger circuit will be explained with reference to the waveforms of figure 7. These waveforms are similar to figure 2 and are expanded to show arming and triggering operations of the trigger circuit. It is not important for the following discussion whether or not the trigger circuit is counting down. The time scales are relative and should be considered only on a generalized basis. Once the general operation of the automatic trigger circuit has been presented, the detailed operation for worst-case conditions where the countdown ratio is changing can be presented.

Consider the waveforms of figure 7 for a trigger circuit in operation where previous trigger signals have been processed each in a similar manner. When the trigger circuit is reset at time t_1, the hold-off circuit provides arming current for the trigger circuit. Figure 7a shows the output voltage of the hold-off circuit and figure 7b shows the trigger signal. The standardized pulse is shown in figure 7c with a dashed line showing time t_2. The standardized pulse as delayed by the delay line is shown in figure 7d with a dashed line showing time t_3. The difference between times t_3 and t_2 is the time delay of the delay line.

Current from the steering and RC delay circuits add to form the

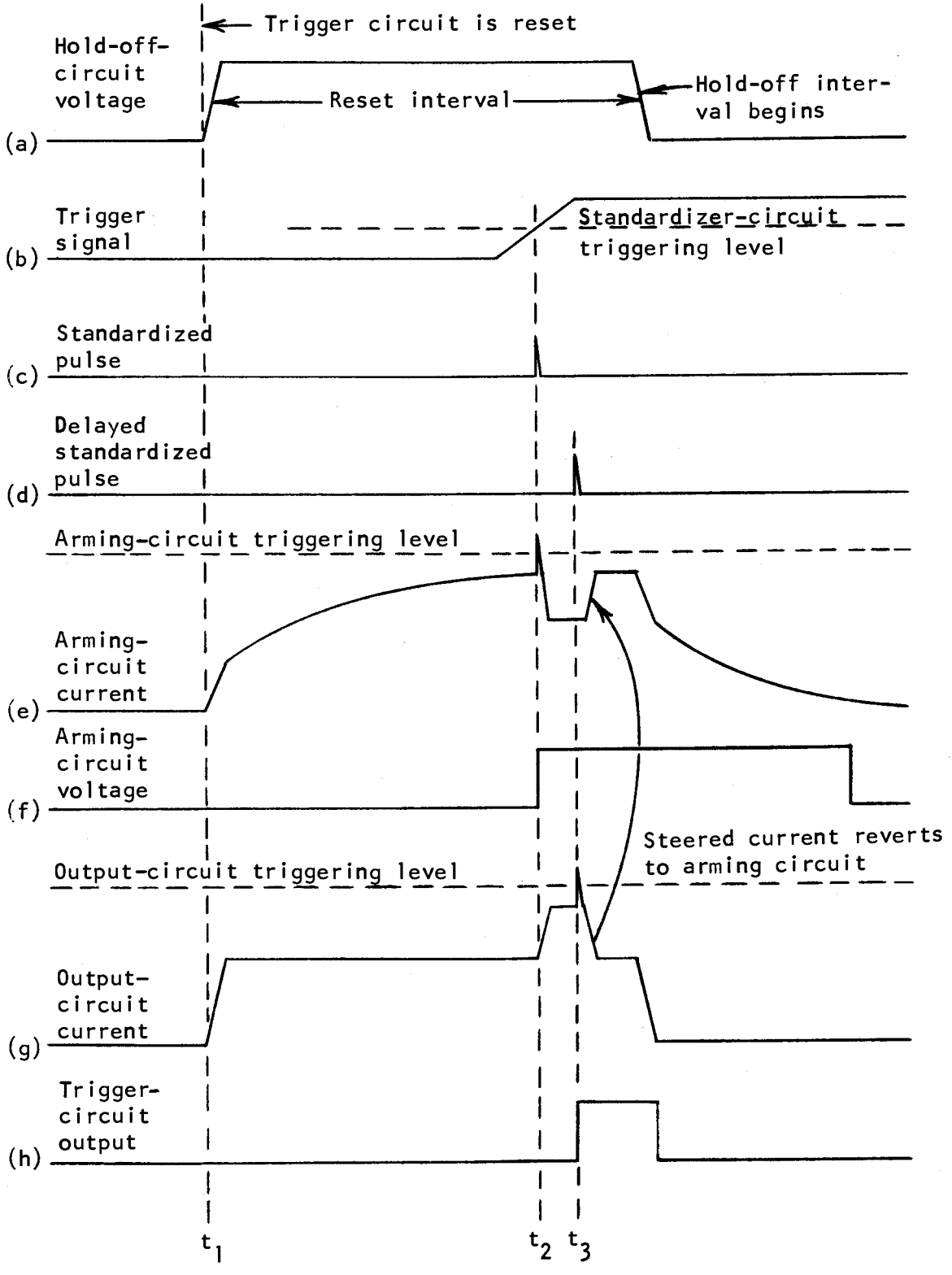


Figure 7. Automatic-trigger-circuit waveforms.

arming-circuit current shown by figure 7e. This current rises initially to a value determined by the current supplied by the steering circuit and then increases as the RC delay circuit supplies additional current. This additional current approaches a final value exponentially at a rate determined by the RC delay circuit elements. The final value is less than the triggering level of the arming circuit. The standardized pulse, when summed with the steering and RC delay circuit currents, will cause the arming circuit to be triggered to its high-voltage state if this total current exceeds the triggering level at the time the standardized pulse occurs.

Figure 7f shows the voltage increase of the arming circuit once it has been triggered to its high-voltage state at time t_2. The steering circuit must then supply current to the output circuit as shown in figure 7g. This waveform shows that a substantial amount of current was provided to the output circuit at time t_1 and that the current transfer of the steering circuit has taken place at time t_2. The current in the output circuit is now sufficient so that the output circuit is armed and will be triggered to its high-voltage state when the delayed standardized pulse occurs at time t_3.

The output voltage of the trigger circuit is shown by figure 7h. This output voltage activates the hold-off circuit, but because of finite circuit delays, the hold-off circuit does not respond immediately. Until the hold-off interval starts, both the arming and output circuits are in their high-voltage states. The current provided by the steering circuit will revert from the output circuit to the

arming circuit at time t_3 as seen in figure 7e and 7g. When the hold-off interval starts, the current level in the output circuit falls to zero and the output circuit reverts to its low-voltage state. The current to the arming circuit from the RC delay circuit decreases slowly as seen in figure 7e. When the current is sufficiently reduced, the arming circuit reverts to its low-voltage state. See figure 7f. At the end of the hold-off interval (not shown), the trigger circuit is again reset and the process is repeated.

Jitter introduction is possible in conventional trigger circuits when the trigger signal occurs close to the reset time. This was explained on pages 6 through 8. A worst-case condition for jitter introduction is when the countdown ratio n is changing. A typical situation that can occur is shown in figure 8. Trigger signal acceptance

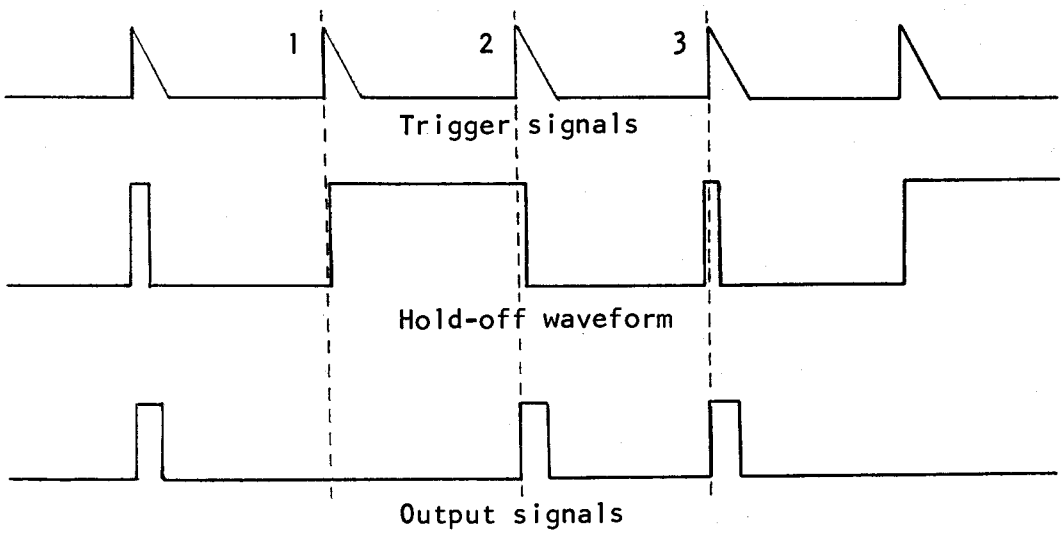


Figure 8. Worst case for jitter introduction.

is such that both long and short times for arming the trigger circuit are available. This can be seen in figures 4a and 4c respectively. The automatic trigger circuit has an output circuit that always triggers at the same point on the leading edge of the delayed standardized pulse. Since the leading edge of that pulse is in constant time relationship to the trigger signal, jitter is not introduced. This will be explained in the following discussion.

Figure 9 shows detailed signal processing for three consecutive trigger signals identified in figure 8 as 1, 2, and 3. Trigger signal 3 is shown in dashed lines in figure 9. Note that figure 9 is similar to figure 7 except for additional details. No attempt has been made to consider the fact that the current from the steering circuit to the output circuit reverts back to the arming circuit as shown in figures 7e and 7g. This does not affect the operation of the trigger circuit and is not an important point for this discussion.

From figure 9e it can be seen that the current to the arming circuit rises initially to approximately 30% of the triggering level at time t_1. Then it approaches a 90% level at an exponential rate. The current to the output circuit as shown in figure 9g rises to 60% of the triggering level and is stable at that level. Trigger signal 1 occurs slightly too early for the standardized signal to trigger the arming circuit. This is shown in figure 9e. The delayed standardized pulse is identified by 1' and is shown in figures 9d and 9g. It is not sufficient to raise the output-circuit current to the level necessary for triggering. Therefore, no trigger-circuit

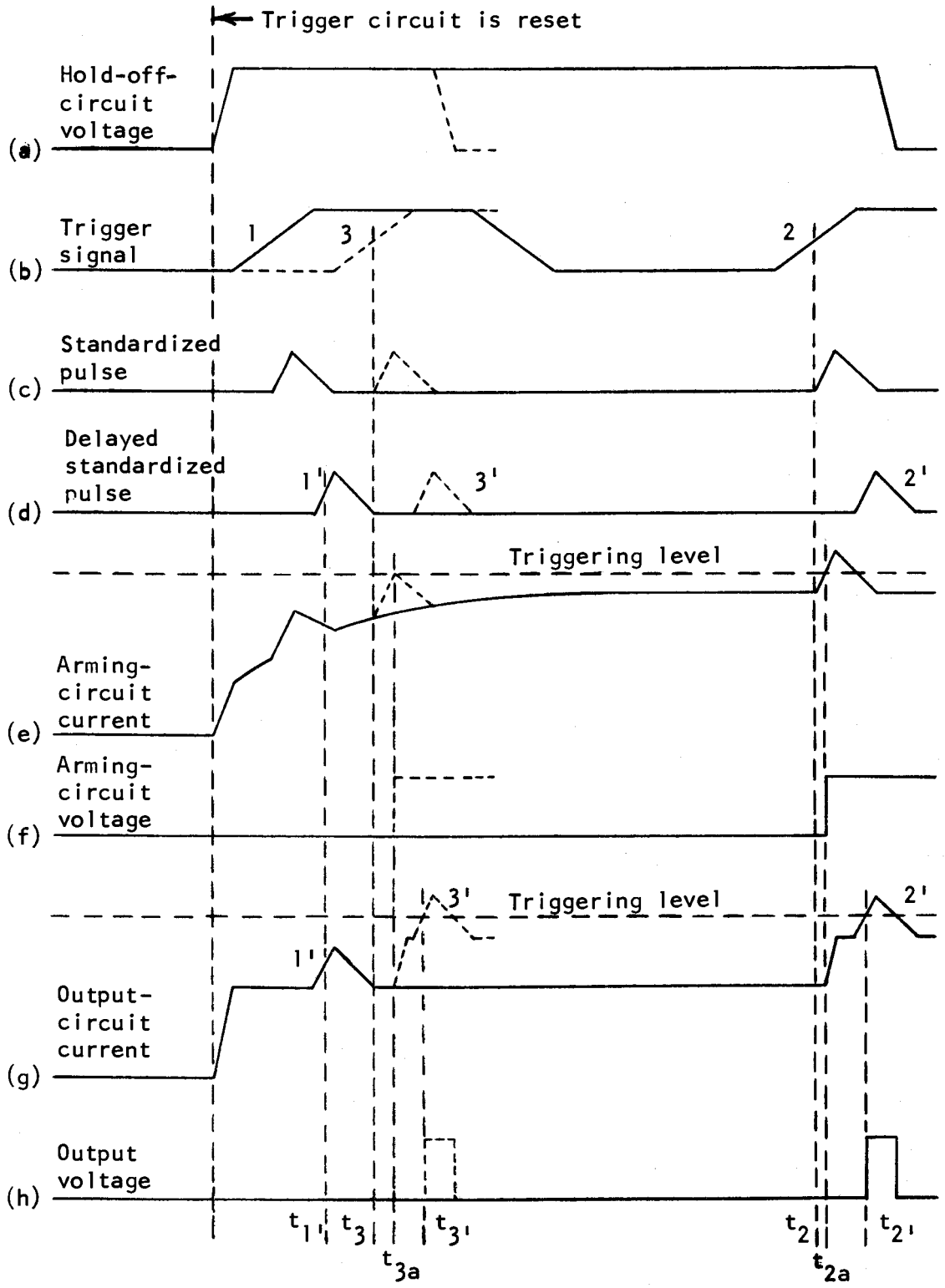


Figure 9. Worst case for trigger-signal processing.

output occurs in figure 9h corresponding to time $t_{1'}$.

Trigger signal 2 will produce an output. Figure 9e shows that the arming circuit is armed to the fullest extent since trigger signal 1 was skipped. The standardized pulse corresponding to time t_{2a} triggers it to a high-voltage state. See figure 9f. This high-voltage state of the arming circuit completes the arming of the output circuit. This arming is shown as an increase in current corresponding to time t_{2a} in figure 9g. The output circuit will be triggered by the delayed standardized pulse at time $t_{2'}$.

For trigger signal 3, shown in dashed lines, the arming circuit is triggered at the earliest time possible. See figure 9e. The full amplitude is required from the standardized pulse. Since the standardized signal has a finite risetime, the arming circuit is triggered later with reference to the trigger signal for trigger signal 3 than for trigger signal 2. This is shown by

$$t_{2a} - t_2 < t_{3a} - t_3.$$

However, the current from the steering circuit to the output circuit reaches a stable level before the delayed standardized pulse occurs. See figure 9g. Thus, the same signal amplitude is required for either the delayed standardized pulse 2' or the delayed standardized pulse 3' to reach the triggering level. Therefore, the output will maintain constant time relationship for either trigger signal 2 or trigger signal 3. This is shown by time intervals

$$t_{2'} - t_2 = t_{3'} - t_3.$$

Because of finite risetimes of practical devices, the interval

denoted by $t_{2'} - t_2$ or $t_{3'} - t_3$ is slightly longer than the time delay of the delay line.

The previous discussion has assumed that the duration of the standardized pulse would be shorter than the time delay of the delay line. This allows arming of the output circuit to take place and to stabilize before the standardized pulse arrives via the delay line. As the standardized pulse duration is increased, less time is available for the arming current to stabilize. This can increase the probability for the introduction of jitter. If the standardized pulse duration is longer than the time of the delay line as shown in figure 10c, a trigger output can be produced that is not coincident with the leading edge of the delayed standardized pulse.

Figure 10b shows a trigger signal that occurs at time t_2 that is nearly coincident with the reset time t_1. The standardized and delayed pulses are longer in duration than the time delay of the delay line. In figure 10e, the arming-circuit current increases as in figure 7e and 9e, but with the standardized pulse added to it. When the current reaches the triggering level, the arming circuit is triggered to its high-voltage state and arms the output circuit. Since the delayed standardized-pulse arrives at the output circuit at time t_3 and is still present, the output circuit is triggered at time t_4. The current from the steering circuit immediately reverts to the arming circuit as shown in figures 10e and 10g. The output pulse should have occurred at time t_3, but has occurred at an arbitrarily later time t_4.

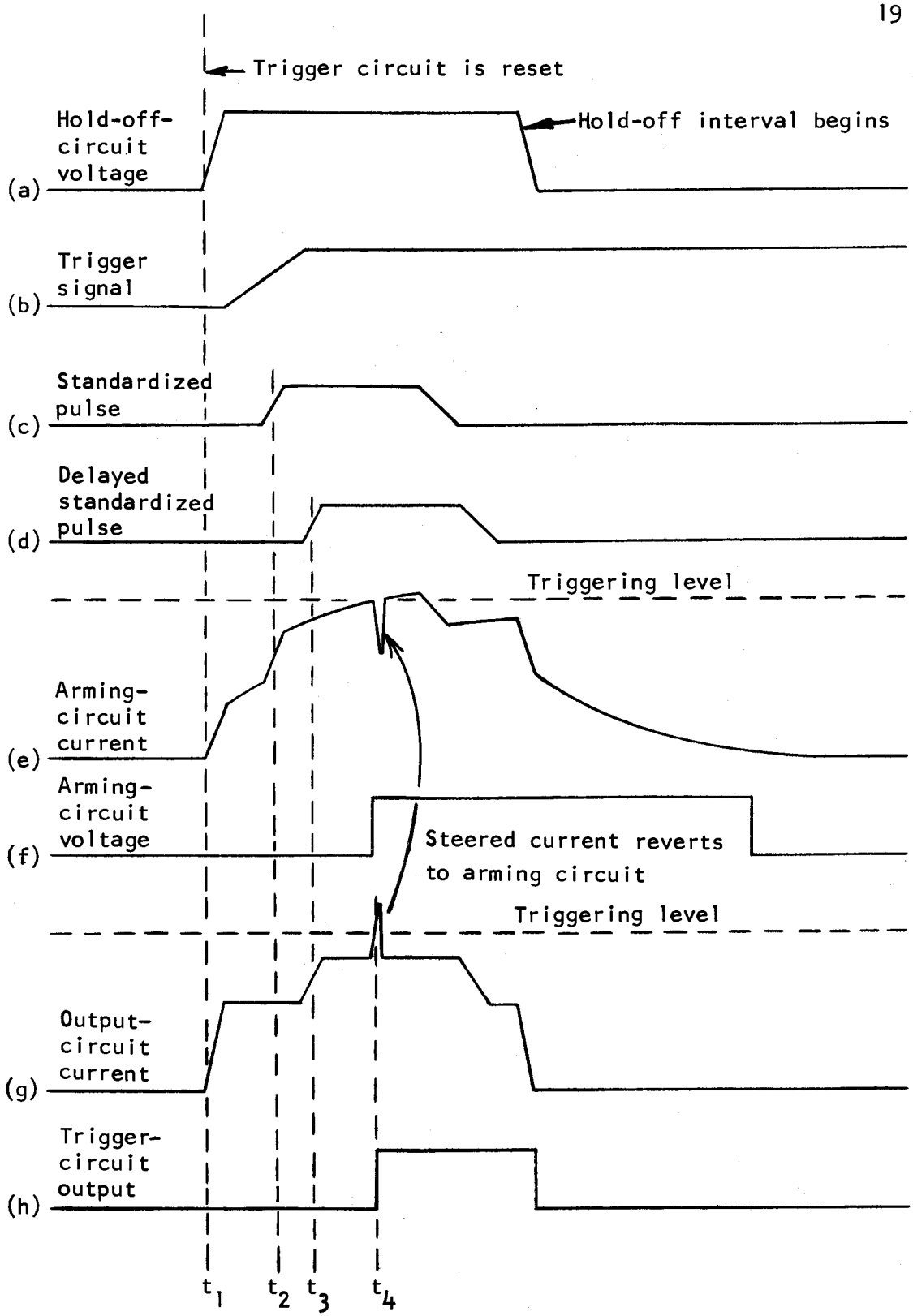


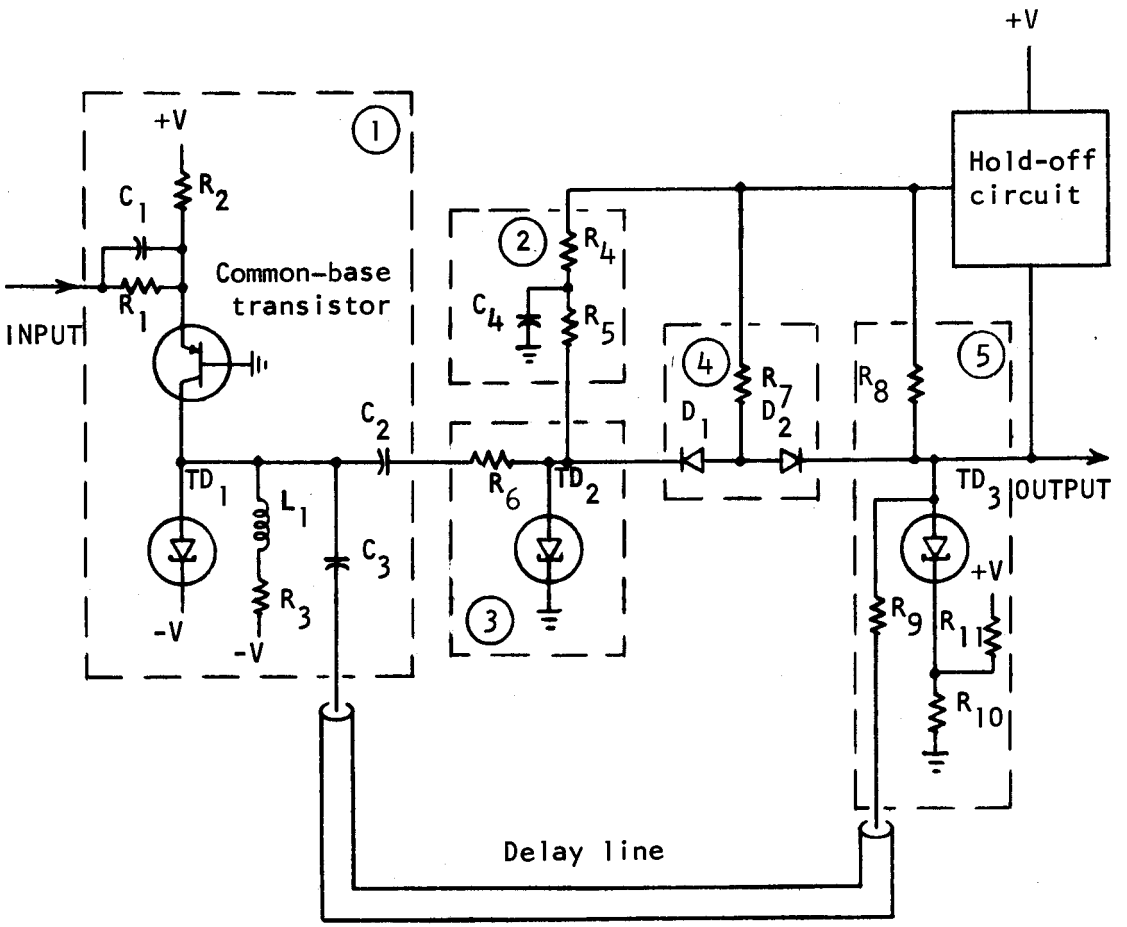
Figure 10. Effect of standardized-pulse duration.

DETAILED CIRCUIT DESCRIPTION

The schematic diagram of figure 11 shows the complete network for the automatic trigger circuit. In figure 11, a network for biasing the base of the grounded-base transistor and a tunnel diode (TD) temperature compensating circuit are not shown. This simplifies the diagram so that the more important circuit features may be seen more clearly. Dashed lines enclose networks that make up the various circuits within the trigger circuit.

The standardizer circuit consists of an isolation transistor connected to TD_1. The biasing level of TD_1, and its load determine the Schmitt trigger characteristics of the standardizer circuit. R_1 and C_1 connected to the emitter of the common base transistor form a 50Ω load for the trigger signal. R_2 provides a constant current for TD_1. In addition, the grounded-base stage reduces the voltage appearing at the trigger signal input when TD_1 changes states. This reduces interaction from the trigger circuit to the trigger signal source. C_2 and C_3 differentiate the output from TD_1 and also prevent direct-current coupling between circuits. R_3 and L_1 form a complementary network with C_1 and C_2 so that TD_1 works into a resistive load.

The RC delay circuit consists of R_4, R_5, and C_4. This combination has a 1μs time constant and provides bias current to TD_2 in the arming circuit. Current is coupled from the standardizer circuit to TD_2 via C_2 and R_6. C_2 and R_6 have a 1 ns time constant. Current is



Network

1. Standardizer circuit
2. RC delay circuit
3. Arming circuit
4. Steering circuit
5. Output

Figure 11. Schematic diagram of the automatic trigger circuit.

also coupled from the standardizer circuit, via C_3 to the 5 nanosecond delay line and R_9. R_9 is a termination for the delay line. The differentiated pulse coupled to TD_3 also has a 1 nanosecond time constant.

R_8 provides arming current to the output circuit. R_{10} and R_{11} bias TD_3 positive by 200 mV. Current in the steering circuit through R_7 is conducted through either D_1 or D_2 depending upon the voltage levels at TD_2 and TD_3. When TD_2 and TD_3 are in their low states, D_1 will conduct since its cathode will be 200 mV lower than the cathode of D_2. When TD_2 changes to its high state with a characteristic 400-500 mV increase in voltage, D_2 must conduct since its cathode is at a lower potential. When D_2 conducts and D_1 is off, the current from the steering circuit arms the output circuit. The output circuit will then have sufficient current to be triggered by the delayed standardized pulse.

D_1 and D_2 are low capacitance diodes so that capacitive coupling of the voltage transition of TD_2 to TD_3 is minimized. Current sufficient to trigger TD_3 would be transferred through D_1 and D_2 if their capacitance was too high. D_1 and D_2 must also be low storage devices so that current transfer from TD_2 to TD_3 can take place and stabilize in approximately 1 nanosecond. This allows a safety margin for the standardized pulse which is delayed by the 5 nanosecond delay line to insure full arming of the output circuit.

Circuit details of the hold-off circuit are not necessary since many common circuits are available. The output voltage of the hold-

off circuit is +V during the reset interval and 0 V during the hold-off interval.

SUMMARY

The trigger circuit will provide output signals that have less than 30 picoseconds of jitter in relation to the trigger signal for a minimum trigger signal level of 100 mV peak into 50 ohms. The frequency range is DC to 100 MHz. This thesis has discussed the automatic trigger circuit specifically because of its significance. However, minor circuit switching can be employed to provide nonautomatic, low-level signal recognition as well as higher frequency synchronizing. Manual polarity switching can also be provided for all modes of operation.

A logical extension of this automatic trigger circuit is a trigger circuit that accepts every other trigger signal. This would also provide automatic triggering and could be accomplished by driving both the arming and output circuits with the same standardized pulse so that the delay line can be eliminated. This is not desirable for oscilloscope use, however, since the resultant trigger circuit output will always have a period twice that of the trigger signal. When the trigger-signal period is longer than the hold-off interval, the display on the cathode-ray tube has less intensity than the trigger circuit with the delay line.

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