TRANSISTOR DC AMPLIFIER DESIGN THEORY

by

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ABBREVIATED LIST OF SYMBOLS

h_{ie} Common-emitter input impedance with the output short-circuited. Also referred to as h_{11e}.

h_{re} Common-emitter backward voltage transfer ratio with the input open. Also referred to as h_{12e}.

h_{fe} Common-emitter forward current transfer ratio with the output short-circuited. Also referred to as h_{21e}.

h_{oe} Common-emitter output admittance with the input open. Also referred to as h_{22e}.

α_n Ratio of collector current to emitter current, normal connection.

α_i Ratio of collector current to emitter current, inverted connection (collector and emitter terminals interchanged).

f_α Frequency at which alpha becomes 0.707 of its low-frequency value, common-base configuration.

I_{co} Collector saturation current with the emitter open.

I_{eo} Emitter saturation current with the collector open.

I_e Emitter current.

I_b Base current.

I_c Collector current.

V_{eb} Emitter-to-base voltage.

V_{ce} Collector-to-emitter voltage.

V_{cb} Collector-to-base voltage.

K Boltzmann's constant, 1.37×10^{-19} erg/degree.

T Absolute temperature, $^\circ$K.

q Magnitude of charge on an electron, 1.6×10^{-19} coulomb.

δ Algebraically equal to KT/q, or 0.026 volts at 300°K.

Δ Difference operator.

$\multimap$ An amplifier, usually understood to be a dc amplifier unless otherwise indicated.

E_s Signal voltage source.

u   micro, 10^{-6}.

m   milli, 10^{-3}.

k   kilo, 10^{3}.

TRANSISTOR DC AMPLIFIER DESIGN THEORY

INTRODUCTION

This paper was prepared to present a practical and realizable solution to the problems of transistor dc amplification. Thus it consists not only of theoretical dc amplifier requirements, problems, and possible solutions for both dc and modulated dc systems, but also the design considerations and experimental results leading to the construction of an acceptable dc amplifier.

Inherent to the subject of general dc amplification is the problem of thermal drift associated with direct-coupled circuitry. In addition, the transistor functions according to well-defined thermal laws thus making temperature considerations even more critical in this application. Offsetting this disadvantage, however, is the tremendous ruggedness, reliability, and low power consumption of the transistor. At the present state of the art, the transistor has been proven to be as reliable as the best vacuum tubes, able to withstand shocks of several thousand g's capable of operating on milliwatts of power at temperatures up to 150°C, and available at about the same cost as a vacuum tube.

From the preceding description it is seen that the transistor is very desirable for many applications. In particular this report emphasizes the application of the dc amplifier to an operational voltage amplifier;

however, most of the information is equally relevant to general dc amplifier applications. Pertinent to all applications are considerations of stability, bandwidth, impedance levels, amplification noise, transistor inter- changeability, and cost. These are some of the more general problems treated in this report.

A rather specific analysis is given to the chopper- type dc voltage amplifier which was experimentally inves- tigated in detail. This amplifier consisted of a series arrangement of a transistor chopper, ac amplifier, demod- ulator, and dc amplifier.

DERIVATION OF DC AMPLIFIER REQUIREMENTS

Before an intelligent choice of a dc amplification system can be made, the requirements of such a system must be specified. Thus this phase of the report will attempt to develop the theoretical requirements of an operational amplifier* along with the practical considerations involved in such a project.

Operational Amplifier Analysis

The operational amplifier is commonly understood to be the basic building block of analog computers. In the intended application to an analog computer, a natural choice exists as to the mode of operation, voltage or current. The network configurations and idealized responses for each mode are indicated below (15, p. 410-13).

Figure 1. An Operational Voltage Amplifier

$$\frac{e_o}{e_{in}} = \frac{-Z_2}{Z_1}$$

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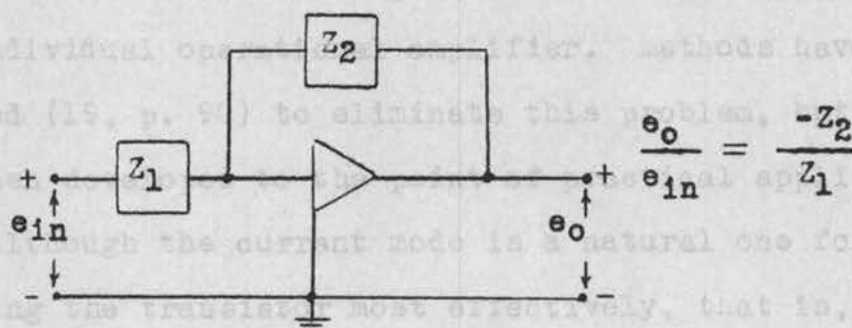
* An operational amplifier can be defined as a dc amplifier used with various feedback networks in analog computations.

Figure 2. An Operational Current Amplifier

$$\frac{i_o}{i_{in}} = -\frac{Z_1}{Z_2}$$
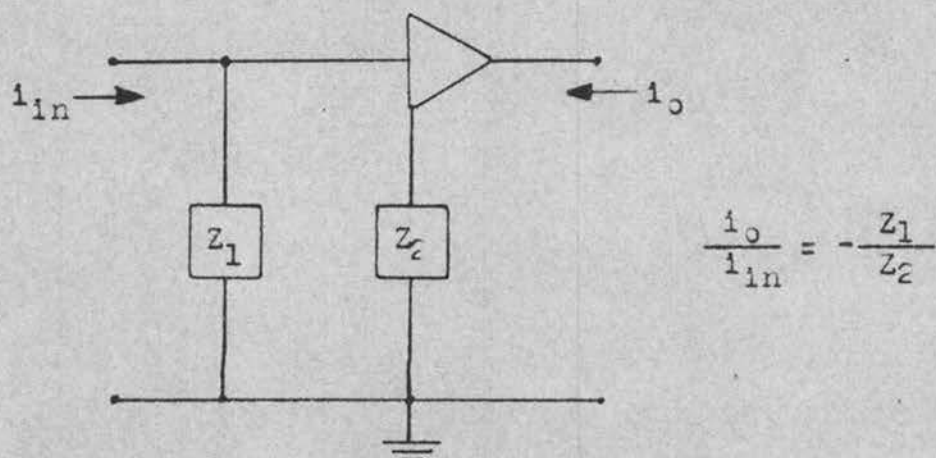
The choice of the operational mode is now seen to be imposed by the proposed application. Since an analog computer requires at least ten operational amplifiers to handle a sufficiently large collection of problems, it is imperative that each amplifier be capable of operating from common power supplies. This condition eliminates the operational current amplifier from further consideration since the feedback impedance, Z_2, isolates each amplifier thus necessitating isolated power supplies for each individual operational amplifier. Methods have been proposed (19, p. 90) to eliminate this problem, but none have been developed to the point of practical applications. Thus, although the current mode is a natural one for utilizing the transistor most effectively, that is, the transistor is a current operated device, has low input impedance, and a high output impedance, the prohibitively

large bulk and cost of such an analog computer eliminates this choice.

At this point our problem is now confined to the operational voltage amplifier, figure 1. Since all such amplifiers have a common ground, they may utilize common power supplies and are thus readily adaptable to large analog computer operations.

Ideally, a voltage operated device such as an operational amplifier* has infinite input impedance and zero output impedance. If in addition, the dc amplifier has infinite voltage amplification, an identity is established such that the response of the network shown in figure 1 becomes $\frac{e_o}{e_{in}} = \frac{-Z_2}{Z_1}$. This equation is the basis for all analog computer operations. Thus the utility of the operational amplifier lies in the accuracy with which this relationship may be obtained and the flexibility of operations which may be performed by choosing different impedances for Z_1 and Z_2.

Since a transistor dc amplifier will by necessity have a finite input impedance, finite voltage amplification, and a non-zero output impedance, it is desirable to know what error is produced by virtue of these non-ideal conditions. The complete expression for the response of

* Throughout the rest of the report, the term "operational amplifier" will be understood to mean a voltage operated dc amplifier used with various feedback networks in analog computations.

the network shown in figure 1 can be shown (Appendix II) to be:

$$(1) \quad \frac{e_o}{e_{in}} = -\frac{Z_2}{Z_1} \left[1 + \frac{1}{A} \left(1 + \frac{R_o}{r} + \frac{Z_2}{r} + \frac{R_o}{Z_1} + \frac{Z_2}{Z_1} + \frac{R_o}{Z_2} \right) \right]$$

Where: R_o = output impedance of dc amplifier

   r = input impedance of dc amplifier

   A = voltage amplification of dc amplifier

The error term is easily recognized as:

$$(2) \quad error = 6 = \frac{1}{A} \left(1 + \frac{R_o}{r} + \frac{Z_2}{r} + \frac{R_o}{Z_1} + \frac{Z_2}{Z_1} + \frac{R_o}{Z_2} \right)$$

The limiting values of Z_1 and Z_2 for a given magnitude of error are easily found from this expression. For the specific case of A = 25,000, R_o = 1,000 ohms, and r = 2,000 ohms the limiting values are plotted in figure 44. This figure illustrates the error of the operational amplifier which results from a given choice of Z_1 and Z_2 and an amplifier with the above mentioned specifications.

Certain conclusions are obvious from this analysis. First, it illustrates that an analog computer based on a dc amplifier with A = 25,000, R_o = 1,000 ohms, and r = 2,000 ohms is not as limited by the choice of Z_1 and Z_2 as is commonly supposed, a maximum dc gain of 200 being possible with an error of only 1%. This indicates

that a transistorized operational amplifier, although restricted, has many applications.

The complete operational amplifier network responses for an integrator and differentiator operation with the non-ideal dc amplifier are developed in Appendix III and IV, respectively.

Equation 1 also implies many more requirements other than amplification, Z_1, Z_2, input impedance and output impedance. These are:

1. The output drift due to temperature and aging are negligible.

2. The amplification A, is large at all frequencies for which the computation accuracy is to be good.

3. The amplifier including the feedback loop Z_1 and Z_2 is stable.

4. The effects of noise and non-linearity are negligible.

These requirements then impose conditions of thermal drift, aging, amplification, bandwidth, stability, phase-shift, noise, and non-linearity upon the operational amplifier.

Practical Consideration

An inherent implication in any practical project is that it be economically feasible. This provides another requirement which will have to be considered since, practically speaking, it is always desirable to obtain the most

acceptable performance for the least cost.

Included indirectly in the cost requirement is the added condition that component tolerance be as large as possible. Thus it is desired to eliminate as many matched or hand-picked components as possible.

Another factor to be considered in a satisfactory dc amplifier design is the effects of interchanging transistors. It is desirable to be able to replace transistors of the same type with as little adjustment as possible and still obtain satisfactory results.

A further consideration is the stability of a series of cascaded operational amplifier networks with an overall feedback loop. In this configuration, which is commonly encountered, the phase-shift is additive thus imposing more stringent requirements on the phase-shift per amplifier.

Another requirement is apparent from an investigation of multiple network operations. Namely, that to prevent saturation in succeeding amplifiers each amplifier must be designed so that for the zero input condition, there is also a zero output. This condition is commonly known as an automatic zero-set, AZS arrangement.

Summary of Compromise Specifications

With all the previously mentioned considerations

in mind, a set of specifications may now be drawn up. It will be noted that the following specifications are quite lenient --the operational amplifier as a whole falling in about the five per-cent error category. Of course, it is desirable to refine the specifications so that the overall error would be less than one per-cent; however, these requirements provide a measure of usefullness as well as a suitable starting point which is practical.

A limitation which has not been mentioned previously is that for the presently available transistors, the maximum output voltage swing is about $\pm$ 15 volts. This figure appears below.

From the above conditions the following specifications may be derived for the proposed dc amplifier which is to be used in an operational amplifier network.

1. Voltage amplification to be equal to or greater than 20,000.

2. Input impedance to be equal to or greater than 2,000 ohms.

3. Output impedance to be equal to or less than 1,000 ohms.

4. Maximum output voltage swing to be $\pm$ 15 volts.

5. Thermal drift at the output to be equal to or less than 0.25 volt in the temperature range of $70^{\circ}F \pm 15^{\circ}F$.

6. Long term output drift to be less than 0.10 volt per hour.

7. Bandwidth to be dc to 1,000 cps, or greater.

8. Phase-shift at output to be less than 10° deviation from the net 180° phase-shift.

9. Noise at output to be less than 0.10 volt peak-to-peak.

10. Non-linear distortion to be less than 2%.

11. Transistors and components to be interchangeable with minimum of custom adjustments or hand-picking.

12. Cost to be minimum for acceptable performance.

DISCUSSION OF TRANSISTOR OPERATIONAL CHARACTERISTICS

With the desired specifications in mind, the transistor characteristics may now be examined to isolate and analyze the particular aspects which will be important in this application. Consequently, this section of the report is included to provide the background information which is necessary before the significance of particular transistor dc amplification systems can be appreciated.

Physical Characteristics

First to be considered are those characteristics in which the transistor exceeds its vacuum tube counterpart. These qualities are reliability, ruggedness, power dissipation, size, and weight. It is for these reasons that the transistor has been so rapidly developed and applied.

The reliability of transistors is usually considered from the standpoint of short-term and long-term effects. Short-term effects are those contributed by temperature and shock. Electrically the effects of temperature are well known, an increase in the saturation current of reverse-biased junctions being the primary effects of a rise in temperature. Thus it produces no failures in well designed circuits.

As far as mechanical ruggedness is concerned, it has experimentally been found that a shock of 500 g's will

damage less than 1% of the transistors tested. Even at
8,000 g's, a 60% to 75% survival rate was obtained.
Vibration and acceleration characteristics are equally
impressive, thus making the mechanical ruggedness of the
transistor greater than that of many passive circuit
elements (20, p. 95-97).

Long term effects generally include the changes
produced by continuous operation, namely, aging effects
and failure rates. Generally, it has been found that
aging produces the same effects as noted from an increase
in temperature. These effects are a reduction in the
value of current gain and an increase in the collector
saturation current, I_{co}. Most of the total change occurs
in the first few hundred hours; silicon transistors
usually showing considerably less change than germanium
transistors. These changes are primarily due to changes
in the transistor surface conditions (2, p. 376-86).

According to a recent Bell System study, (2, p. 388-
91) grown-junction transistors in their P-carrier system
exhibited a failure rate of 0.67% per 1,000 hours. In
less complex circuitry where transistor requirements were
not so stringent, failure rates ranged from 10^{-4} % to
o.20% per 1,000 hours. As a basis for comparison, tube
failure rates in IBM computer service were found to range
from 0.17% to 2.0% per 1,000 hours. In the more

conservatively designed Bell systems the tube failure rate ranges from 0.019% to 0.29% per 1,000 hours. Also it is to be noted that in a submarine cable system, long considered the ultimate in reliability, the required failure rate was just under 0.03% per 1,000 hours. Thus the analysis of transistor failures in field equipment shows failure rates that are comparable with well-designed, conservatively used vacuum tubes. Also, since these results were obtained from transistors of 1956 or earlier vintage, it is probable that presently developed transistors have a higher reliability than these figures indicate.

The other more obvious characteristics which make the transistor a necessity for many applications are its extremely small size, weight and power dissipation.

The above mentioned characteristics are the primary reasons for adapting the transistor to a dc amplifier system.

Inherent Limitations

Since a transistor exhibits different characteristics in each of its three configurations --common-emitter, common-base, and common-collector, a specific configuration must be specified with any discussion of its particular characteristics. The only configuration which is capable of an iterative voltage gain, however, is the

common-emitter stage (24, p. 73-88); thus this stage is the only one which deserves much consideration as a voltage amplifier. The common-base and common-collector stages, may be very useful as input and output stages where either a small or large, input or output resistance is desired. For these reasons the remainder of this discussion will be primarily directed at the characteristics of the common-emitter configuration.

A fundamental property of any junction transistor is the dependence of the collector saturation current, I_{co}, upon the temperature of the device. Since I_{co} varies exponentially with temperature, doubling about every $10^{o}C$, it is very temperature sensitive and considerable care must be exercised to account for its variation. However, the effects of I_{co} are well defined (24, p. 52-54), and consequently there is no mystery involved in designing a suitable temperature stable amplifier. The full significance of this limitation will not be developed until a later section.

Other factors which contribute to the thermal dependence of the transistors are the linear decay of V_{be} (≈ 2 $\frac{mv}{^{o}C}$) a slow exponential rise in h_{oe}, and a small increase in h_{fe} at lower temperatures and a decrease at the higher temperatures (13, p. 25-30). These changes are, however, of secondary importance and are not usually considered

directly. In high temperature applications these factors
may become appreciable.

Another transistor characteristic which is of para-
mount importance is the relationship between the magnitude
and phase of the common-emitter current amplification, h_{fe},
and frequency. A valid expression or experimental result
of this relationship is most difficult to obtain since h_{fe}
is dependent to a great extent on the external circuit and
on the extrinsic parameters, besides the intrinsic tran-
sistor. For our purposes, however, it is sufficient to
note that feedback loops around two common-emitter stages
are nearly always stable, while feedback loops around
three stages are generally unstable. Also it should be
noted that the upper cutoff frequency in the common-
emitter configuration is usually slightly less than the
quotient of the alpha cutoff frequency in the common-base
configuration and the low frequency h_{fe}.

Like all other electronic devices the transistor
exhibits definite noise properties. Generally the noise
encountered in transistors is considered to include three
different types; the thermal noise of an ohmic conductor,
shot noise, and excess or semiconductor noise. The first
two types are white noise while the last type is charac-
terized by a $\frac{1}{f}$ behavior and is usually found below 1,000
cps. Thus in dc applications it is quite likely that the

semiconductor noise would be most troublesome.

Outside of choosing a low noise-figure transistor to begin with, there are certain general procedures which tend to minimize the noise tendency. Driving the transistor from a source impedance of about 1,000 ohms seems to reduce the noise (23, p. 14-20) as does reducing the collector-to-emitter voltage and emitter current. Thus the operating point on the critical input stages should be made as low as possible.

Another condition to be considered is the nonlinearity of h_{fe}. Generally h_{fe}, the small-signal parameter, decreases with increasing collector current. Thus for large-signal amplification the output will be appreciably distorted. The amount of distortion can be anticipated from a visual display of the characteristic curves of the transistor in question. To reduce this nonlinear tendency it is feasible to use as large a load impedance as possible, and if further improvement is desired, to apply negative feedback around individual or multiple stages.

Other important parameters to be considered in a satisfactory design are the maximum collector power dissipation, and the maximum collector-to-emitter voltage. Needless to say, the ratings of the transistor should never be exceeded. These parameters are usually

determined by the type of transistor and its construction.

If interchangeability is a requirement to be considered then some thought must be given to the deviations which are likely to be found in transistors of the same type. Generally the manufacturer will state a maximum, minimum, or average h_{fe}, or a combination of the above. Other parameters are quite likely to vary as much as 100% from average. Thus the design must be able to accomodate very large deviations with a minimum of custom adjustments. Usually one must specify a minimum and maximum h_{fe} to insure that the transistor will be biased in a linear region. The other parameters are generally not so critical.

Bias Stabilization

The temperature dependence of I_{co} has been previously mentioned as an inherent limitation of the transistor. In this section we shall discuss the stabilization, with regard to I_{co}, of the single-stage common-emitter biasing network and its effect on the dc voltage amplification of the stage.

It is easily found that besides providing a suitable biasing arrangement for the transistor, the biasing network determines the sensitivity of the external circuit to temperature. Thus a well-designed biasing network is mandatory. Several suitable biasing schemes exist (24 p. 68-71), however, we shall examine just one of them

which is very general and useful. Other biasing schemes
would yield the same general conclusions.

Figure 3. A Common-Emitter Single Battery Biasing Circuit
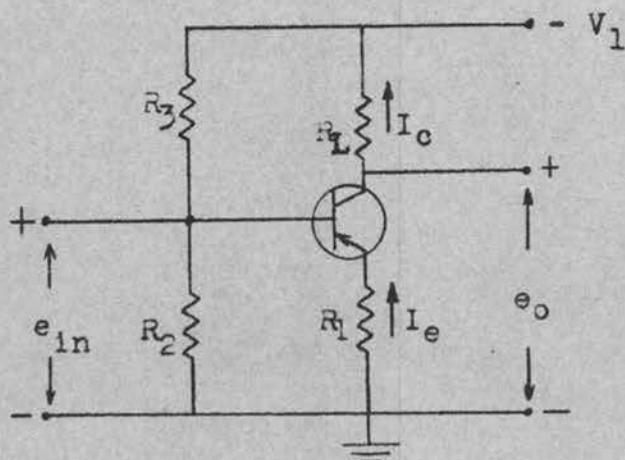
Certain stability factors may be derived for this
circuit on the basis of the variation of I_{co} and its effect
on the external circuit. According to Shea's analysis
(24, p. 54-71), the current stability factor is defined
as the quotient of the change in emitter current and the
change in I_{co}, or algebraically:

(3) $\quad S_I = \dfrac{\Delta I_e}{\Delta I_{co}} = \dfrac{G_1}{G_2 + G_3}$, for average conditions, $(G_n = \dfrac{1}{R_n})$

Likewise, the voltage stability factor is defined as
the quotient of the change in collector-to-base voltage
and the change in I_{co}.

(4) $\quad S_v = \dfrac{\Delta V_{cb}}{\Delta I_{co}} = S_I R_1 + (1 + S_I) R_L$, for average conditions.

To meet the small thermal drift requirements, therefore, ideally S_V and S_I should equal zero. To approach this result, equation 3 states that R_1 should be large and R_2 and R_3 should be small. The voltage stability equation states that the above mentioned conditions should be met plus the condition that R_L should be small.

One other result is needed to fully appreciate the significance of the above statements. This result is the expression for the input impedance of the transistor.

(5) $\qquad R_{in} = h_{ie} + h_{fe} R_1$, for average conditions.

From these equations the full significance of the gain versus bias stability conflict may be understood. By increasing R_1 and decreasing R_2 and R_3, thereby increasing the thermal stability, the input impedance of the transistor is raised geometrically while the input impedance of the complete stage is decreased. Thus if this stage is driven by a current source, most of the signal current will be lost through R_2 and R_3 and very little current will enter the transistor. If the stage is driven by a voltage source, the shunting effect of R_2 and R_3 will not be so noticeable; however, the high input impedance of the transistor will definitely limit the current which can enter the transistor. In either case,

the signal current which can enter the transistor is comparitively small. It naturally follows then that the voltage amplification of the stage will be very small since the transistor is a current operated device. Furthermore, the condition that R_L shall be small for good thermal stability limits the possible voltage amplification even more. For these reasons it is very difficult to achieve appreciable dc voltage amplification per stage with suitable temperature stability.

From the definitions of the voltage and current stability factors, it is apparent that the stability is directly dependent upon ΔI_{co}. Thus if ΔI_{co} could be decreased for the same change in temperature, the gain versus stability conflict would be alleviated somewhat. This is the reason for the introduction of the silicon transistor. The I_{co} for both germanium and silicon increase at about the same rate with temperature, however, at room temperature an average silicon transistor has an I_{co} of the order of 10^{-8} amps while an average germanium transistor has an I_{co} of the order of 10^{-6} amps. Thus silicon transistors are much better suited to high temperatures applications and dc amplification. It seems that nature always works against the engineer, for accompanying the beneficial temperature characteristics of

silicon is a cost of about ten times that of germanium.
So, a conflict still exists.

ANALYSIS OF DC AMPLIFIER SYSTEMS

To obtain the optimum system for a given application, all applicable systems must be evaluated. It is for this reason that a brief analysis must be given to all the systems which could possibly satisfy the previously set forth requirements. From this analysis, then, a system can be chosen which will best satisfy the requirements for the application.

Generally a dc amplifier system will be either a direct-coupled configuration or a modulated dc system. These are the classifications which will be discussed in this section.

Direct Coupled Configuration

The characteristics of the individual transistor common-emitter stage have already been examined in the previous section. From this discussion a rather obvious possibility is apparent, that of a cascade of several common-emitter stages. A conventional arrangement of such a circuit is illustrated below.

Figure 4. A Direct-Coupled Single-Sided DC Amplifier
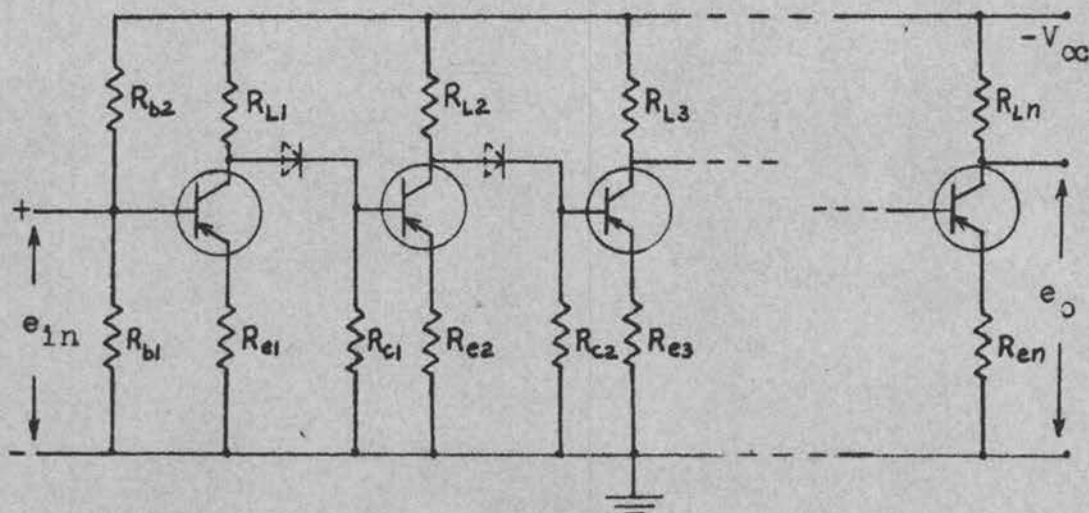
Since this type of circuit is merely a series of common-
emitter stages, all the limitations of the single stage
still apply individually. However, it should be noted
that if all stages are identical, each iterative stage
has perfect I_{co} stability, and the temperature character-
istics of the complete circuit become approximately those
of only the first stages. Even with considerable differ-
ence between stages, as long as the transistors are all
of the same polarity --either PNP or NPN, some cancel-
lation of temperature characteristics from stage to stage
will be effected. On the other hand, if the transistors
alternate polarity; that is, PNP-NPN-PNP --etc., the
temperature characteristics from stage to stage combine
additively so that the complete circuit would have very
poor thermal stability characteristics.

Thus in a real application where it is certainly not
desirable to have all stages identical from the standpoint
of their quiescent operating points, a certain amount of
cancellation of temperature characteristics may be effected
from stage to stage by using similar polarity transistors.
However, a compromise is still in order between the voltage
amplification per stage and thermal stability considera-
tions. This compromise means accepting a low amplification
per stage, which indicates a large number of stages, in an
attempt to preserve some thermal stability.

This compromise, however, with its large number of
stages introduces other problems, namely the voltage accumu-
ulation from stage to stage. If a large collector supply
voltage is used it further aggravates the gain versus
bias stability conflict because of the necessity for lar-
ger resistors in the front stages of the circuit. A
smaller collector voltage supply may be used if breakdown
diodes are used between stages to compensate for the
voltage accumulation. If the diodes are used, as indicated
in figure 4, the resistors R_{c1}, R_{c2}, $\cdots R_{cn}$, are usually
necessary to provide sufficient current to fully saturate
or break down the diode. Otherwise these resistors may
not be necessary. Their insertion provides an additional
shunt path thus lowering the amplification.

The breakdown diode in saturation exhibits an

intrinsic incremental resistance of:

$$(6) \quad R_{\text{lnc}} = \frac{\delta}{I} \qquad \text{where} \qquad \delta = \frac{KT}{q}$$

$$\delta = 0.026 \text{ volts at } 300^\circ K$$

$$I = \text{Current through the diode}$$

Additionally, the breakdown diode has a positive temperature coefficient of from 0.001 to 8.0% which must be considered.

The voltage accumulation presents an additional problem in that an output device must be constructed to satisfy the automatic-zero-set requirement.

It is easily recognized that the voltage accumulation problem is eliminated if the transistors are of alternate polarity; however, as previously indicated this combination would exhibit very poor thermal characteristics.

Several non-linear compensating techniques have been developed so that an amplifier may exhibit appreciable gain per stage and yet have satisfactory thermal stability. Among these techniques are the utilization of the positive voltage temperature coefficient of reverse biased diodes, the negative voltage temperature coefficient of forward biased diodes, the negative resistance coefficient of both forward and reverse biased diodes, other temperature sensitive resistors, and extra transistors of the same type

used as compensating current generators (24, p. 20-23).
All these techniques, however, are dependent upon the
matching of the temperature characteristics of the compen-
sated and compensating devices. This requires special
hand-picked and matched components which are hard to
obtain, costly, and definitely undesirable from the stand-
point of interchangeability.

From this brief analysis, the single-sided cascaded
dc amplifier is seen to have definite shortcomings. To
achieve appreciable amplification per stage either the
temperature stability must be sacrificed, the increased
cost of silicon transistors must be absorbed, or the
increased cost and complexity of matched compensating
devices must be tolerated. Additionally, the voltage
accumulation necessitates an output device to provide
an AZS arrangement.

A typical figure for the drift of such a dc amplifier
is 100 millivolts referred to the input (8, p. 249) for
a temperature change of 20°C to 50°C.

Another direct coupled configuration which has con-
siderable merit as a dc amplifier is the differential
amplifier (12, p. 157-60). The differential amplifier
is a form of double-sided or double-ended circuit which
amplifies the difference between its inputs. A
conventional arrangement is shown below:

Figure 5. A Differential DC Amplifier
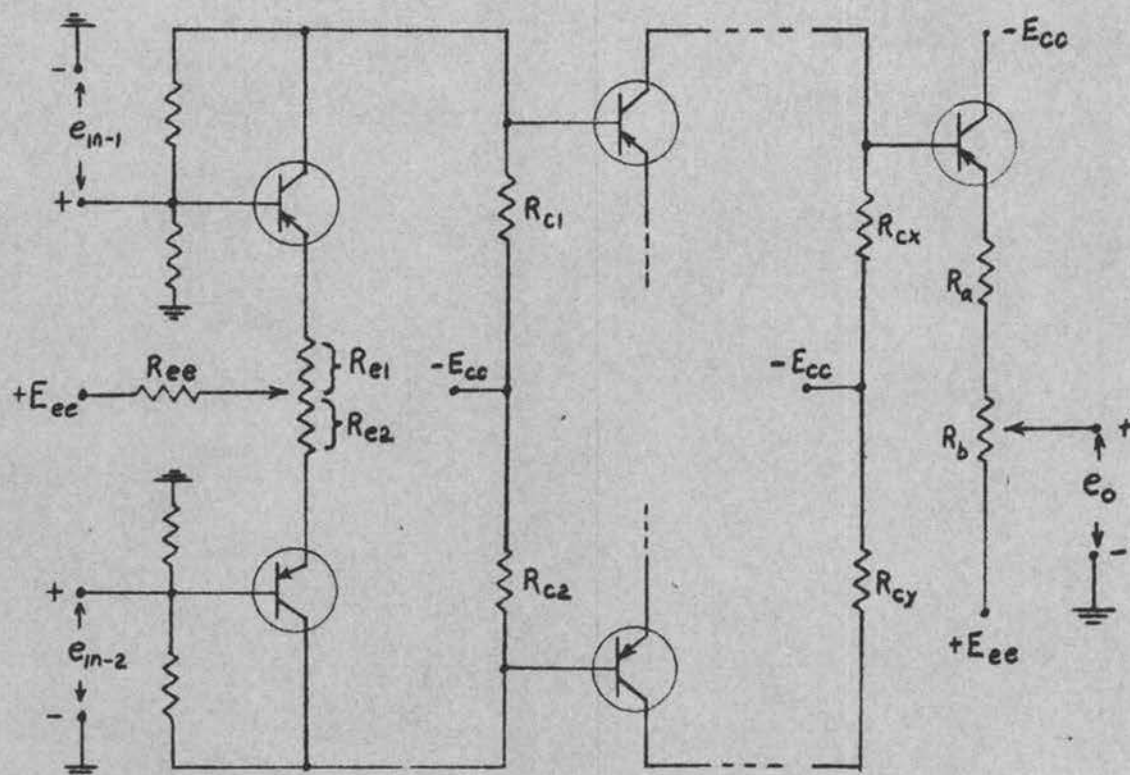
The principle advantages attributed to this type of
circuit (18, p. 194-98) over the single-sided circuit are
that the temperature induced variations tend to oppose
each other, and that the emitter resistor R_{ee} can be made
as large as necessary, thus making the sum of emitter
currents as stable as desired, without adversely affect-
ing the gain per stage. Other desirable characteristics
are that the gain and input impedance are twice that of
its single-sided counterpart. The differential amplifier
also has a voltage accumulation from stage to stage which

requires the same consideration as discussed for the single-sided amplifier. An AZS arrangement is also shown in the figure.

The primary problem with this circuit is matching each pair of transistors with respect to temperature induced I_{co} variations, emitter current, h_{fe}, and base-to-emitter voltage variations with temperature. The degree of matching naturally determines the extent of idealization which may be expected from the amplifier.

A typical figure for the thermal drift of such a dc amplifier in the temperature range of $20^{o}C$ to $50^{o}C$ is about 2 millivolts referred to the input (8, p. 249).

Another matter of some practical concern in applying this circuit to an operational amplifier is that a device must be provided to eliminate the dc bias at the input.

From this brief discussion, it is seen that the differential amplifier is much to be preferred over the single-sided amplifier; however, it is still not very desirable for this application because of its necessity for matched transistors.

At this point it is generally concluded that the application of direct-coupled dc amplifier configurations is definitely limited, primarily because of the gain versus bias stability conflict. At best the situation is alleviated somewhat by matched transistors and components,

complex circuitry, and custom adjustments; all being
prohibitive from the standpoint of cost, time and inter-
changeability. The next section deals with a method which
practically eliminates the previously noted conflict.

Modulated DC Systems

According to IRE standards, modulate means to vary
some characteristic of one wave in accordance with another
wave. In this discussion a modulated dc system refers to
a system which utilizes the advantages gained by changing
the dc signal to an ac signal in some aspect of its opera-
tion, the advantage being that it is much easier to
amplify ac signals with acceptable thermal stability than
dc signals. This advantage is attributable to the use of
reactive bypass and coupling components.

An illustration of possible systems configurations
is shown on the following pages. It will be noted that
a discrimination is made between dc chopper amplifiers
and dc chopper stabilized amplifiers. A chopper amplifier
is one in which the chopper and its associated circuitry
are the sole mode of amplification; whereas a chopper
stabilized amplifier is one in which the chopper amplifier
is used in conjunction with another mode of amplification.

Figure 6-A illustrates a rather novel, although conven-
tional, approach to eliminating thermal drift. In this sys-
tem the output of the conventional dc amplifier is divided
by its amplification factor and compared to the input. The

(A)

(B)

(C)
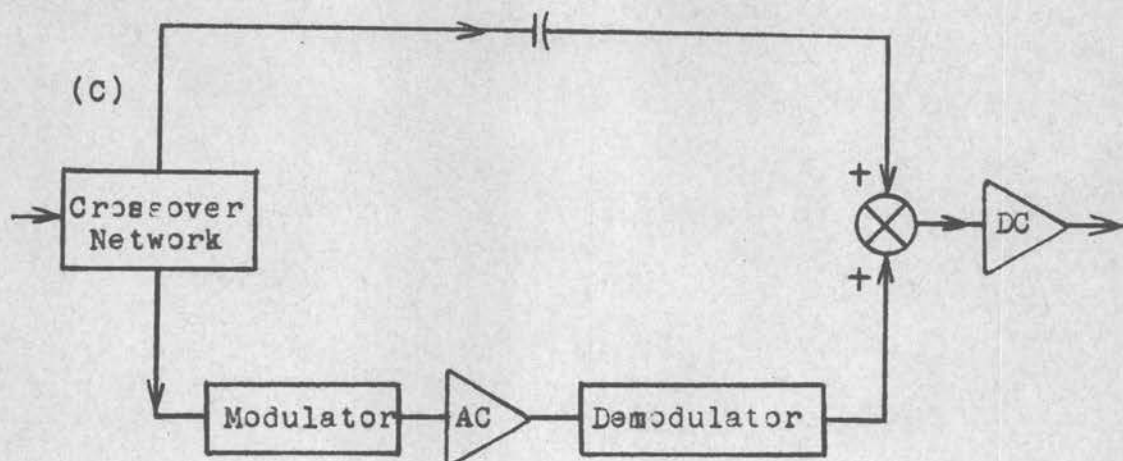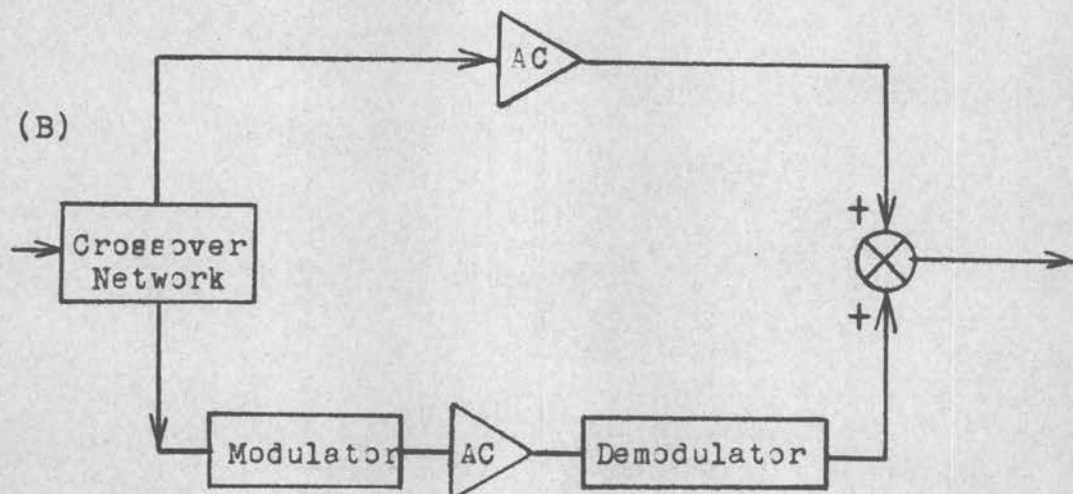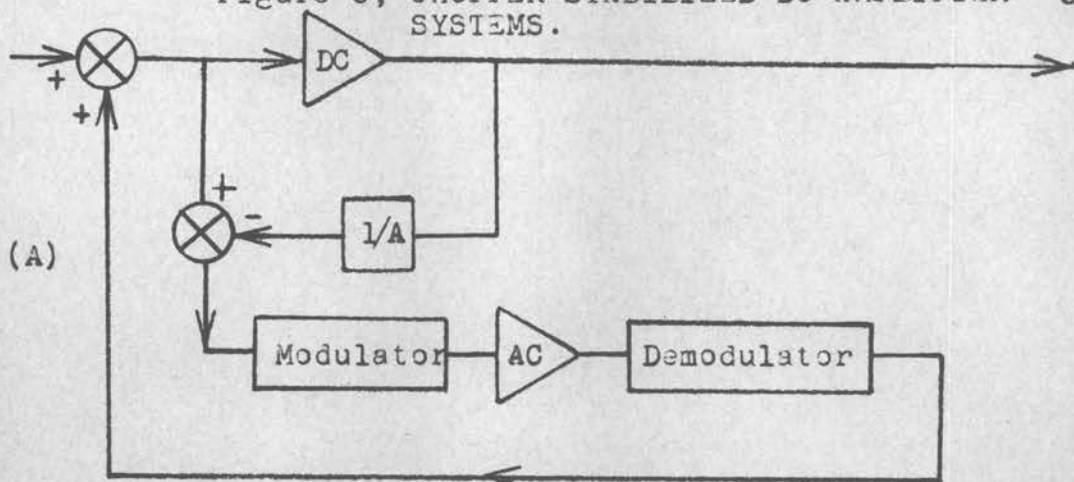
Figure 7, DC Chopper Amplifier Configurations

(A)
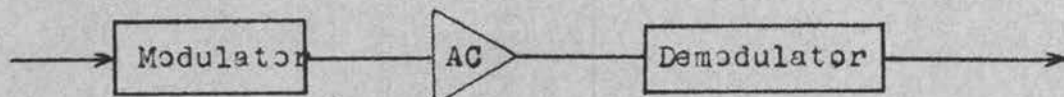
(B)
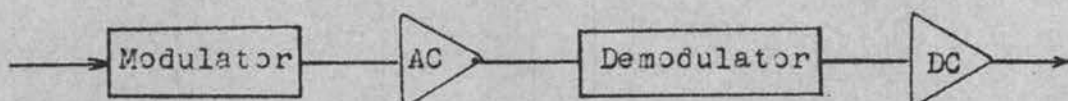
difference then activates the chopper-amplifier which
produces an input to counteract this difference. Thus
the drift of the main dc amplifier is reduced by the amp-
lifieation of the chopper amplifier. The basic disadvan-
tage of this system is that it appears to be too complex
and refined for this application. Undoubtedly, it could
meet the desired requirements. However, a simpler tech-
nique is more desirable.

The system shown in figure 6-B provides a different
amplifier for the ac and de signal components. Although

this system could provide high gain with a minimum of drift and an extremely large bandwidth, it again suffers because of its complexity.

The system of figure 6-C is merely a simplification of figure 6-B. Instead of providing a separate ac amplifier the high frequency signals are fed directly into the high-level output dc amplifier. Because of this simplification the bandwidth is considerably reduced over that of figure 6-B. The stabilization of this system could logically provide a practical problem, and the system again appears to be too complex for this application.

Of all the modulated dc systems, the chopper amplifier shown in figure 7-A is seen to be the ultimate in simplicity. However, since the demodulator is usually simply a low-pass RC filter, the system could be unstable with certain types of feedback encountered in operational amplifier operations (5, p. 10). The system of figure 7-B remedies this situation by isolating the demodulator from the output by a high-level dc amplifier. Thus if the modulating techniques will allow a sufficient bandwidth and the ac and dc amplifiers provide a sufficient voltage amplification, this system appears to be the most desirable.

From this analysis the system shown in figure 7-B was chosen as the one to be experimentally evaluated.

Consequently, most of the rest of this report is an investigation of this system.

Optimum System Analysis (Figure 7-B)

Theoretically the modulation technique could utilize the phase, frequency, or amplitude of the carrier signal. However, the simplest technique is merely that of chopping the input signal. The chopped signal is then amplified in the ac amplifier, the amplified dc input level is recovered in the demodulator, and the output high-level dc amplifier further amplifies the signal and isolates the output from the demodulator.

By virtue of its simplicity the chopper is a natural choice of the modulation technique. However, here a choice exists as to full-wave or half-wave chopping. With full-wave chopping there is no inherent phase-shift; however, it requires a double-sided chopper, ac amplifier, and demodulator. This indicates twice as many components as those required for a half-wave chopping system. The half-wave chopping system, though, introduces an effective time lag, or phase shift, when the chopped signal is demodulated, equal to half the period between samples. Algebraically:

(7) $\phi = \dfrac{f_s}{f_c} 180^\circ$, where f_s = signal frequency

$\qquad\qquad\qquad\qquad\qquad\quad f_c$ = chopping frequency

$\qquad\qquad\qquad\qquad\qquad\quad \phi$ = phase-shift

Thus to restrict the phase-shift to 10^0 or less with a
maximum frequency of 1,000 cps, the chopping frequency
must be at least 18,000 cps. This is perfectly feasible
with a transistor chopper.

Additionally, since the chopping technique is merely
a form of sampling, the sampling theorems and principles
(3, p. 37-41) do apply. The basic information which is to
be obtained from this analysis, however, is that the samp-
led wave must be sampled at a rate at least twice that of
the highest significant signal frequency to obtain all of
the original information which is contained in the sampled
wave. Practically, the sampling rate must be considerably
faster than that predicted theoretically. Also, the theo-
retical considerations show that the demodulator should
consist of a low pass filter with a cutoff frequency of
one-half the chopping frequency. Under these idealized
conditions no information in the sampled wave will be lost.

A practical analysis indicates that other frequency
sensitive networks, usually low-pass RC filters, must be
used to preserve stability. By necessity these shaping
networks must be placed in the dc sections of the ampli-
fier; that is, at the input, after the demodulator, and
after or within the dc amplifier (7, p. 10-13).

To minimize the thermal drift it is also seen that
the dc amplifier gain should be as low as possible. This

necessitates a high gain ac amplifier.

CIRCUIT DESIGN ANALYSIS OF THE OPTIMUM SYSTEM

With the desired system and specifications now in mind, the individual components may be developed. An attempt is made to make each component a complete discussion within itself. This development will follow the natural sequential order; that is, chopper, ac amplifier, demodulator, and dc amplifier.

Preliminary Design Layout

Before entering into the development of each component, it is advantageous to have a more specific idea of the overall system which is being designed. Consequently, the system block diagram is shown below in order that one may better understand the development to follow. This block or flow diagram is derived in part from the previous discussion and the remainder from the development which follows:

Figure 8. A Specific Chopper-Amplifier Block Diagram
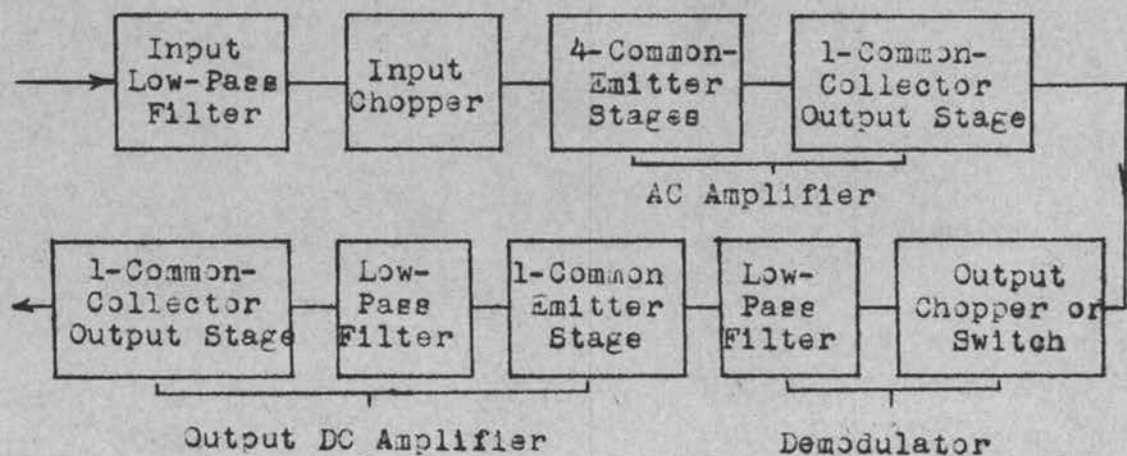
At this point certain conclusions can be drawn from
the preliminary layout (17, p. 34-39). First, it is noted
that the input filter must have an input resistance of
2,000 ohms to meet the previously set forth requirements.
Next, it is apparent that the input chopper must have a
very small bias error, or in other words, for a zero in-
put signal it must have a very near zero output since the
rest of the circuit cannot tell the difference between a
bias error produced by the chopper or an external signal.
Thus the chopper must be a very high quality chopper and
capable of switching very rapidly. It is obvious that the
sensitivity of the chopper determines the sensitivity of
the system. Consequently, the sucess of the system, to
a large extent, is determined by the performance of the
chopper.

To be discussed in more detail later in the report,
are the common-collector output stages on the end of the
ac amplifier and dc amplifier. These stages, it will be
noted, produce no phase-shift and a low output resistance.

Overall there is seen to be a 180° phase-shift which
is necessary in order that the feedback loop and amplifier
be stable. Also, the low-pass filters help maintain
stability since they are inserted to attenuate the higher
frequencies where the total phase-shift may approach 0°
and oscillations would otherwise occur.

The single-stage dc amplifier must obviously be quite stable with temperature if the system is to be stable with temperature variations. However, if most of the amplification can be obtained in the ac amplifier, the dc amplifier need not produce very much gain.

At this point it should also be mentioned that a good choice of power supply voltages is best made if one starts at the output which must be at 0 dc level and work back toward the front. Naturally, the transistors and other circuitry must be well in mind before this choice is made.

Chopper Design Consideration

A search for a suitable chopper or switch to convert dc to ac will yield many different methods. Among these are the mechanical chopper, vacuum and gas tube switching circuits, diode switching circuits, cryatron, transistor switches utilizing the Hall effect, and the conventional transistor switching circuits. At this point we shall confine our attention to the latter method --conventional transistor switching circuits. This choice is dictated by the requirements of availability, simplicity, high quality, and high switching frequency.

The basic principle of conventional transistor switching circuits is suggested by the well-defined dependence of the emitter current, and hence the collector

current, upon the emitter-to-base voltage. Algebraically, the relationship can be shown (18, p. 344) to be:

$$(8) \quad I_e = I_{eo} \left(e^{\frac{V_{eb}}{\delta}} - 1 \right) - \alpha_i I_c$$

$$\delta = \frac{KT}{q}$$

$$(9) \quad I_c = I_{co} \left(e^{\frac{V_{eb}}{\delta}} - 1 \right) - \alpha_n I_e \ , \quad \text{where:} \quad \alpha_i = \text{Inverted alpha}$$

$$\alpha_n = \text{Normal alpha}$$

It will be noted that these equations as well as the following discussion apply to polarities associated with a PNP transistor. The same information applies to NPN transistors with polarities reversed.

These equations show that if the emitter junction is made positive with respect to the base, a large emitter current of exponential order will flow. (Since I_c is normally negative, the two components of I_e combine additively.) On the other hand, if the emitter is made negative with respect to the base, a very small emitter current will flow. Thus the state of the switch is determined by the polarity of the emitter-to-base voltage.

Extremely different switching characteristics are obtained in each of the different switching configurations. Thus an analysis of each configuration is in order. These configurations are illustrated on the following page.

Figure 9. The Basic Switch Configurations

(A) Common-Base
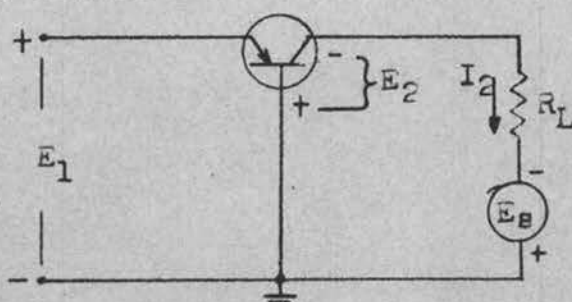
(B) Common-Collector
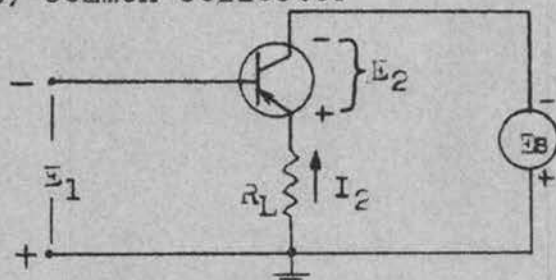
Ideal Characteristics

Saturated (ON) $E_2 = 0$

$$I_2 = \frac{E_s}{R_L}$$

Cutoff (OFF) $I_2 = 0$

$$E_2 = E_s$$

(C) Common-Emitter
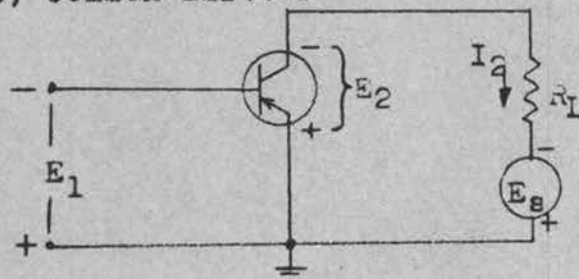
In the preceding figures it is understood that E_1 is the voltage which determines the state of the switch, and that E_s is the voltage which is being switched into the load resistance, R_L. E_2 and I_2 are the quantities which are dependent upon the transistor and determine the quality of the switch.

Under the assumption that these switches are switched

from the saturation region to the cut-off region, the characteristics of each configuration may be obtained (18, p. 339-352). Basically, the common base configuration is undesirable because the saturation voltage, E_2, is negative and by no means negligible, being in the order of a tenth of a volt. The common collector switch exhibits a small saturation voltage, but the cut-off current, I_2, is negative, which is also undesirable. The common-emitter switch is the best behaved configuration as both the cut-off current, I_2, and saturation voltage, E_2, are very small and always positive. Thus the common-emitter configuration offers the most ideal characteristics.

Now that the basic configuration has been determined, a more detailed analysis of its operating characteristics should be made in order to find the causes, effects, and solutions of the non-ideal characteristics.

Of primary importance is the magnitude of the saturation voltage and cut-off current. These parameters can easily be recognized from the common-emitter characteristic curves. An idealized and exaggerated set of these curves is illustrated on the following page to emphasize the point.

Figure 10. Idealized PNP Common-Emitter Characteristic
Curves
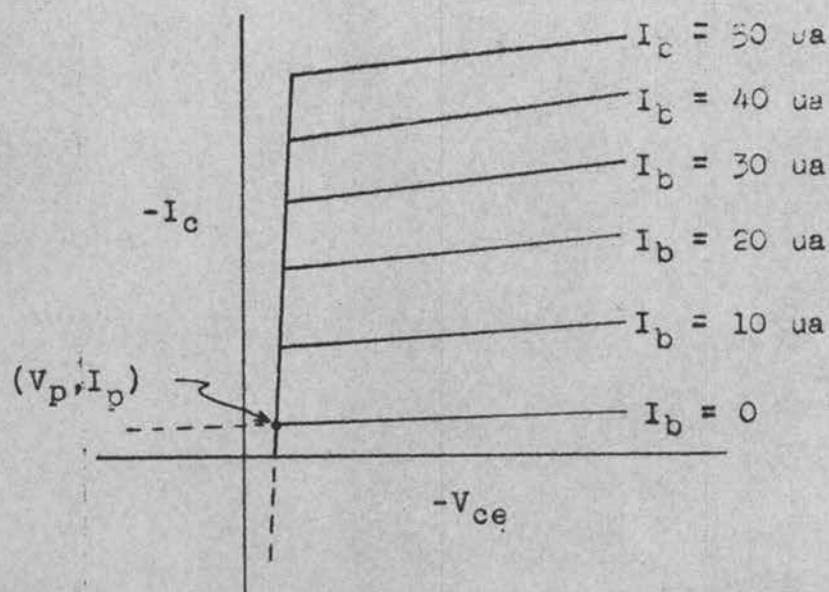
During the saturation the voltage V_p exists between
the collector and emitter thus yielding the saturation
voltage, and during cutoff, a cutoff current I_p flows
through the collector leg thus yielding the cutoff current.
The above discussion then suggests that the transistor
switch can be thought of as an ideal switch shunted by
a current source with finite impedance during cutoff, or
in series with a voltage source with internal resistance
during saturation.

In terms of the transistor parameters, the non-ideal
saturation voltage and cutoff current can be expressed
as (16, p. 16-21):

(10) $I_p^n = \dfrac{(1 - \alpha_i)}{(1 - \alpha_n \alpha_i)} I_{co}$

$$(11) \qquad V_p^n = \frac{KT}{q^o} \ln \frac{1}{\alpha_i}$$

For ordinary germanium transistors, these parameters usually are in the order of several microamps and several millivolts.

Now if the transistor is inverted; viz, the collector and emitter terminals interchanged, the above parameters are reduced by approximately one order of magnitude (16, p. 16-21).

$$(12) \quad I_p^i = \frac{(1 - \alpha_n) \, I_{eo}}{1 - \alpha_n \alpha_i}$$

$$(13) \quad V_p^i = \frac{KT}{q} \ln \frac{1}{\alpha_n} \qquad \text{Where } I_{eo} \; \alpha_n \quad I_{co} \alpha_i$$

This inversion is possible since both the collector and emitter terminals are of the same polarity, N-type or P-type. Thus either one may act as the emitter or collector. However, in the normal configuration the collector is made larger than the emitter so as to have a high collector efficiency. Thus when these functions are reversed the collector efficiency is considerably reduced. For this reason, generally the α_i ranges from 0.3 to 0.9 and α_n ranges from 0.9 to 1.0. Accompanying the reduced collector efficiency is also a decrease

in the maximum allowable power dissipation.

A closer examination of the single stage common-emitter switch will also show that it is incapable of turning off appreciable negative signals.

After understanding the characteristics of the single-stage common-emitter switch, we are now ready to procede with the next logical step in a refinement of the transistor switch, namely, the differential type, or series-pair switch.

Figure 11. The Series-Pair Switch

(a)Inverted Connection   (b)Normal Connection
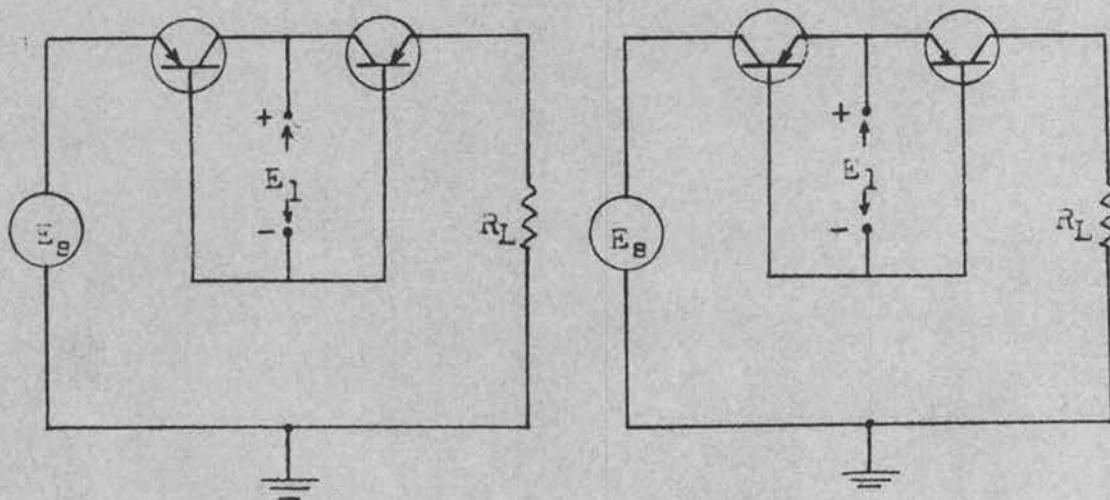
A rather obvious advantage of this switch is that at every interval of time, the saturation voltage or cutoff current, depending upon the state of the switch,

of the two transistors combine differentially. This
greatly improves the quality of the switching character-
istics.

In analyzing this and other more complex transistor
switches a useful rule to keep in mind is as follows:
The transistor may conduct in either direction if either
junction is forward biased, and the transistor will be
cutoff only if both junctions are reverse biased. From
this information it is seen that with E_1 positive as
indicated, both transistors are turned on; and with E_1
negative, one transistor always is turned off regardless
of the signal polarity, E_s. Thus this switch may be
used to switch signals of either polarity up to the
breakdown voltage of the transistors.

As far as current limitations are concerned, it is
advisable to restrict the current through the switch in
the inverted connection to about 2/3 of the maximum rated
current. This restriction is primarily due to the smal-
ler inverted alpha. In the normal connection, the full
rated I_c may be recognized.

Generally speaking, the normal configuration is pre-
ferable in high level applications, while the inverted
configuration provides better low level performance. Also,
the series switch, meaning that the switch is a series
with the load, is usually preferable in low impedance

(less than a thousand ohms) circuits; while the shunt
switch, meaning that the switch is in parallel with the
load, is used more advantageously in the high impedance
circuit (11, p. 28-35).

At this point then, we are ready to choose a con-
figuration to be used as the input chopper in the pro-
posed dc chopper amplifier. Since this application
requires a high quality low-level switch to be used in
a fairly high impedance circuit, the natural choice is
the shunt, inverted connection, series-pair configuration.

Figure 12. The Shunt Series-Pair Switch, Inverted Con-
nection
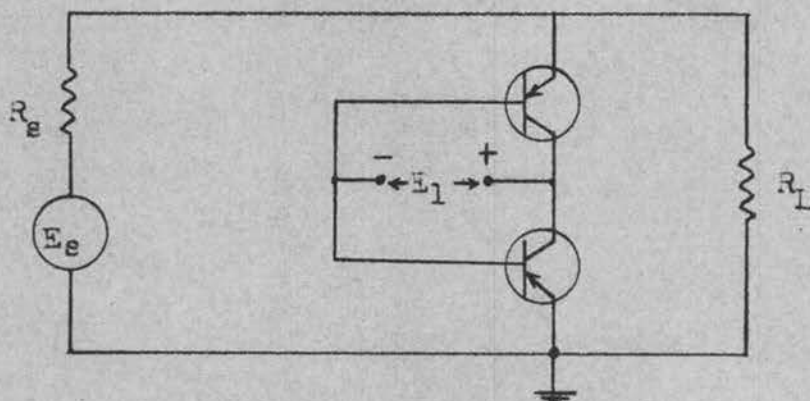
With this configuration in mind, we are now in a
position to study the more specific characteristics of
the switch in actual operation.

As to the choice of transistors, theoretical con-
siderations indicate that a high α_n, low α_i, and low
I_{co} are desirable. Also to be considered are the

collector saturation resistance, Rcs, and transient switch-
ing characteristics.

Of the available transistors, the Philco 2N346 surface
barrier transistor seemed to be best suited to this appli-
cation. Only germanium transistors were considered,
although silicon transistors are more desirable from the
standpoint of their lower I_{co}. Also it was found that
grown junction transistors are definitely unsuitable for
low-level applications because of their large ohmic
resistance which makes the collector saturation resis-
tance very large, several hundred ohms.

The 2N346 was found to have an α_n of about 0.975,
α_i of about 0.8 and, an I_{co} of about 1 to 2 ua. Also,
its alpha cutoff frequency of 75 Mc was found to be indic-
ative of excellent high speed switching characteristics.

Of basic importance in the "on" or conducting state
are the collector saturation resistance and collector
saturation voltage. The emitter-to-collector saturation
resistance, R_{cs}, for a transistor in the inverted connec-
tion has been shown (5, p. 5) to be:

$$(14) \quad R_{cs} = \frac{kT}{q} \frac{1}{I_b} (1 - \alpha_n \alpha_i) \alpha_i + R_x \quad \text{where: } I_b = \text{Base current}$$
$$R_x = \text{Ohmic resistance}$$

For the specific case of the 2N346, this equation becomes:

(15) $R_{cs} = 7.15 \times \dfrac{10^{-3}}{I_b} + 10$, ohms

(The ohmic resistance of 10 ohms is estimated)

And at $I_b = 400$ ua, $R_{cs} = 28$ ohms*.

As a verification of this theoretical result, the experimental values of R_{cs} were obtained. The experimental value is easily obtained from a visual display of the characteristic curves. A typical set of common-emitter, inverted connection, characteristic curves with saturated resistances indicated are shown on the following page.

It is easily proven that the experimental and theoretical values compare favorably indicating the validity of the equation. The experimental results also show that fairly small saturation resistances can be obtained by driving the transistor with sufficient base current.

The collector saturation voltage is a slightly more complex function since it depends on both the effective load resistance and base current. This relationship is illustrated in figure 14. From this set of curves it is seen that if the effective load resistance as seen by

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* Power transistors have much lower R_{cs} values but are not suited for low-level or high-frequency switching.

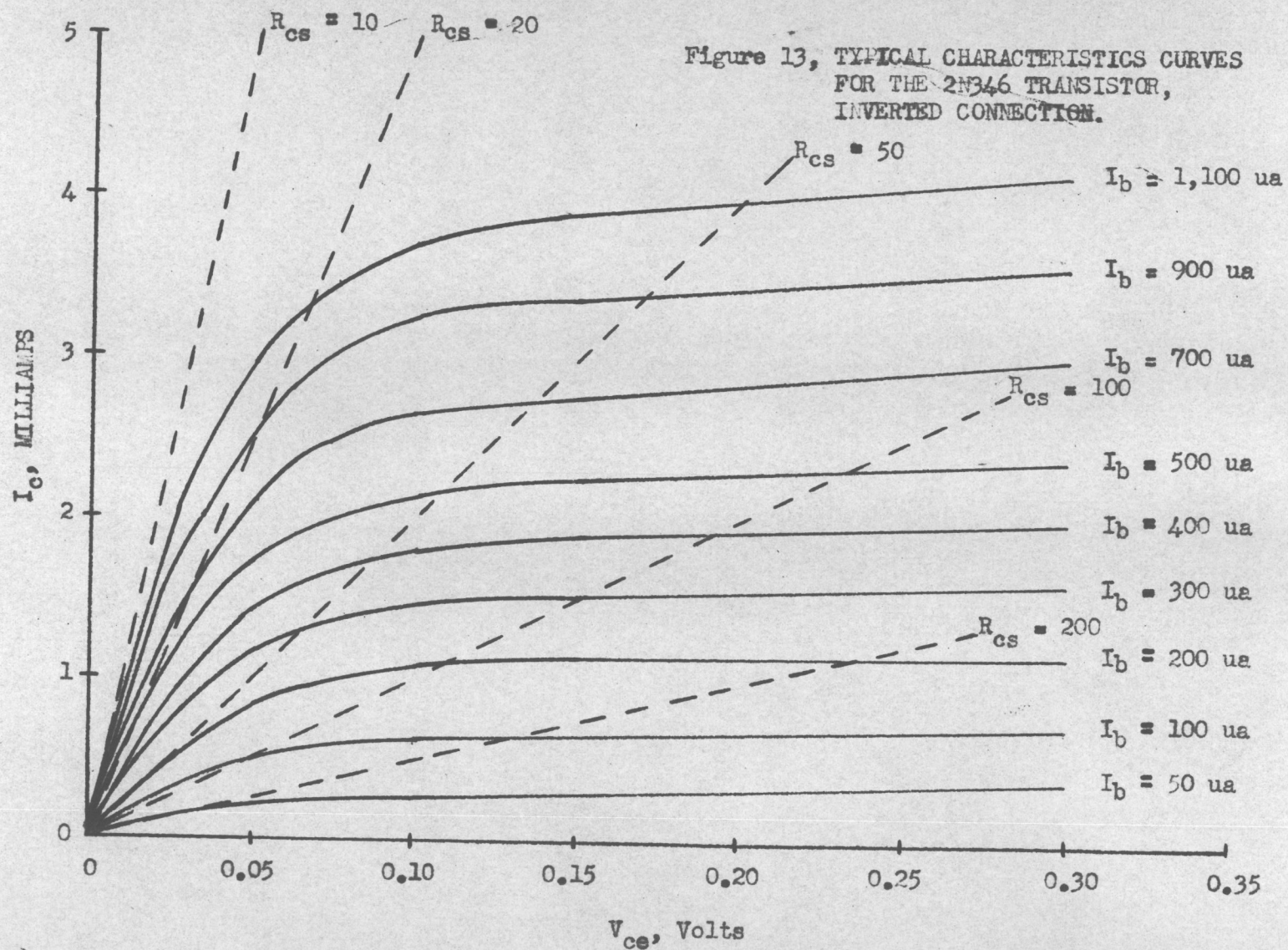Figure 13, TYPICAL CHARACTERISTICS CURVES FOR THE 2N346 TRANSISTOR, INVERTED CONNECTION.

Figure 14, COLLECTOR-TO-EMITTER SATURATION VOLTAGE AND BASE
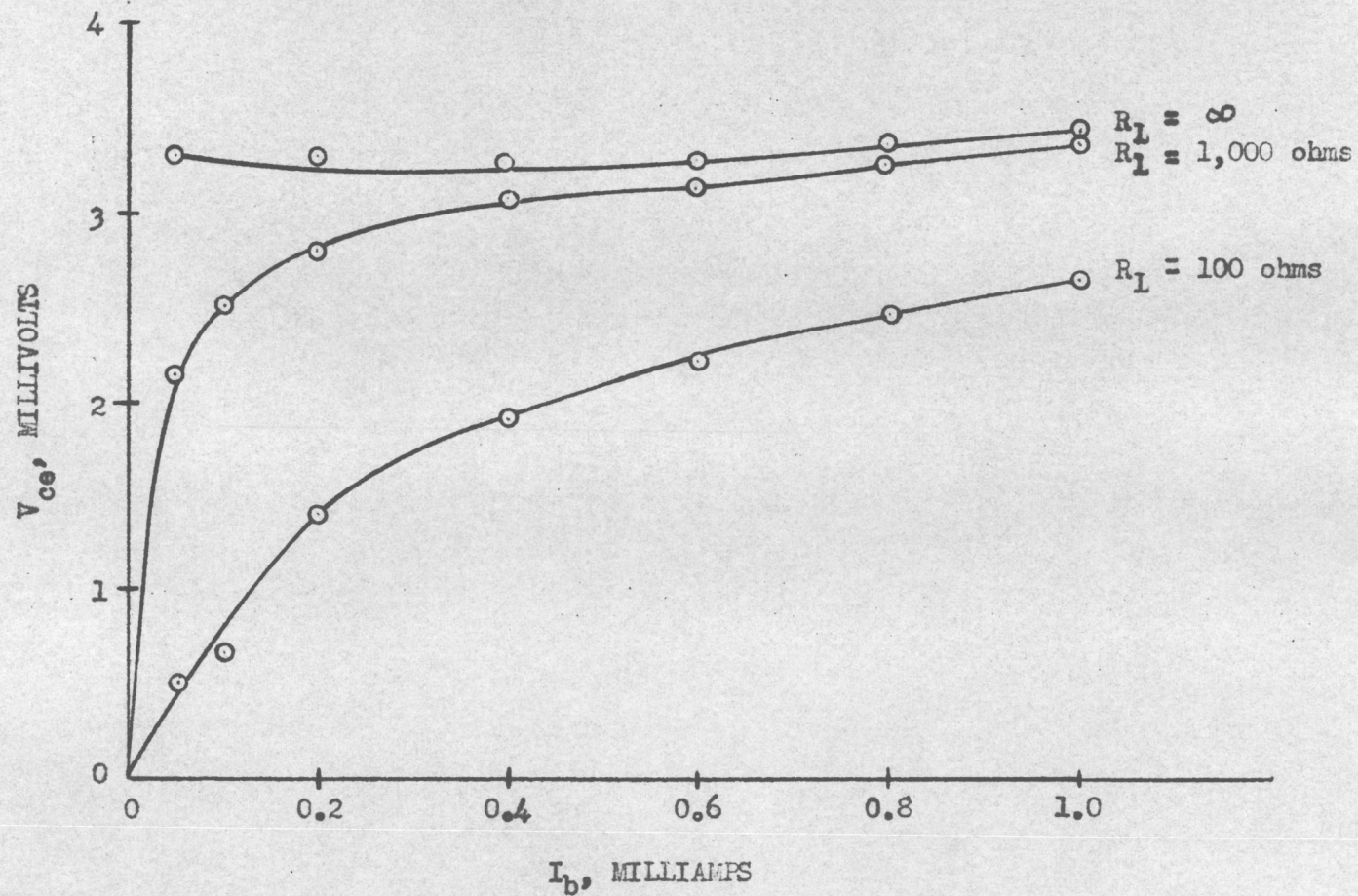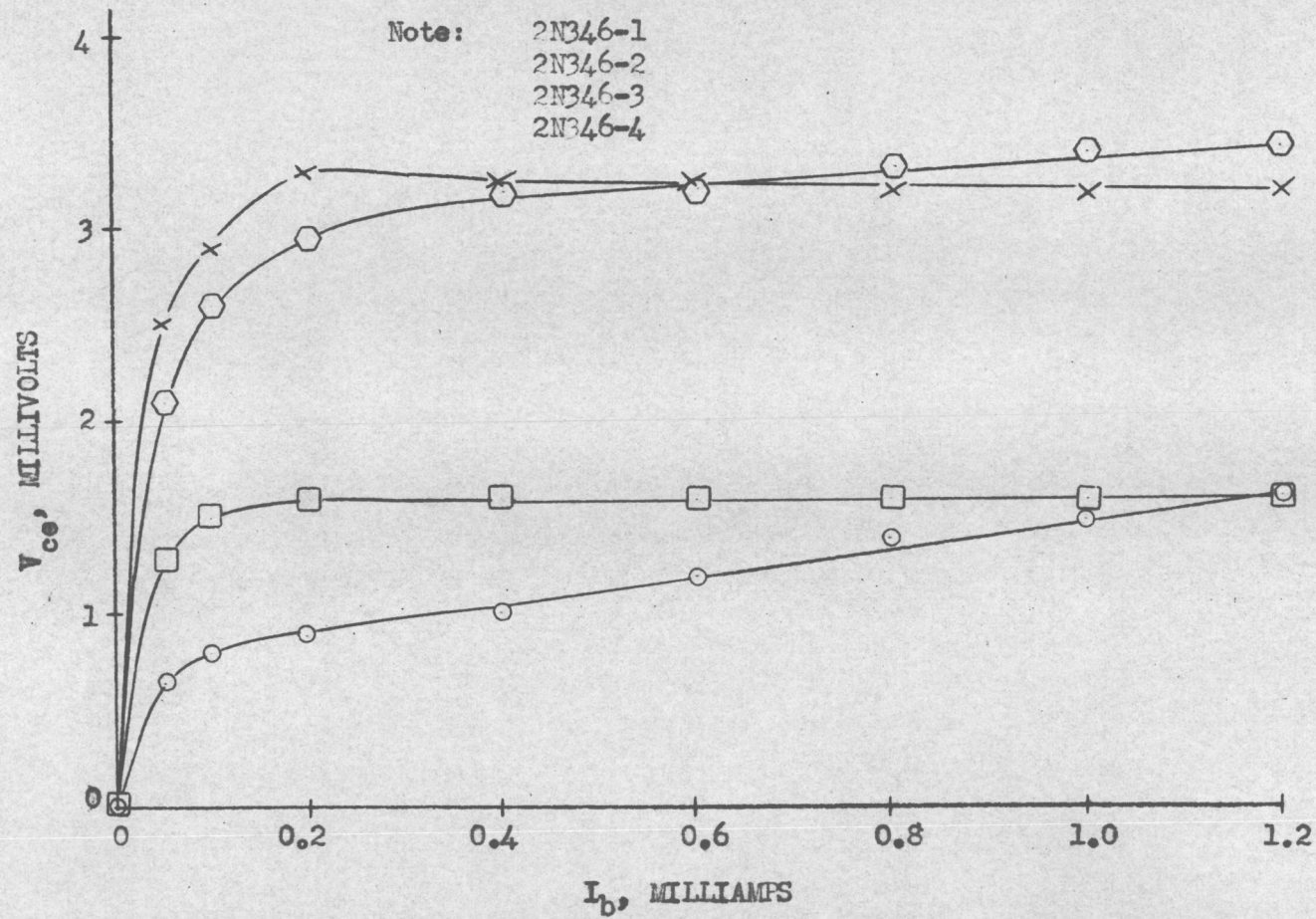CURRENT FOR THE 2N346 TRANSISTOR, INVERTED CONNECTION.

50

Figure 15, COLLECTOR-TO-EMITTER SATURATION VOLTAGE AND BASE
CURRENT FOR THE 2N346 TRANSISTOR, INVERTED CONNECTION.
(Characteristics of four random transistors)

Note: 2N346-1
         2N346-2
         2N346-3
         2N346-4

the switch is in the vicinity of 1,000 ohms or greater,
the saturation voltage is fairly constant. This is indica-
tive of the source resistance, R_{cs}, which already has been
discussed.

The dependence of the collector saturation voltage
upon base current is not very well defined as shown in
figure 15. Common to all of these curves, however, is a
knee in the vicinity where the acting emitter-base junction
becomes saturated. It should also be noted that at zero
base-current the collector-to-emitter voltage is not
actually zero as indicated by the test instruments. In-
stead it has a magnitude determined by the relative doping
of the P and N regions. This potential, however, cannot
be read by a current-drawing device.

The real importance of figure 15, however, lies in
the illustration of the difference in the direction of
change and rate of change of the saturation voltage with
base current. Because none of the transistors tested
showed the same rate of change of V_{ce} with I_b, it is rela-
tively easy to get an exact match at some particular value
of base current, although not at all values. Thus at some
specific value of base current two transistors are easily
picked which have the same collector saturation voltage.
Consequently, when these transistors are inserted in the
circuit of figure 12, and driven with the specified amount

of base current, the overall bias error during saturation
is zero. This is a very significant result as will be
later seen.

The cutoff characteristics of the 2N346 in this low-
level application were found to be very good. Despite a
predicted value of the cutoff current source, equation 12,
of 0.14 ua, the actual magnitude was so small it was
difficult to measure --being in the order of a few hun-
dredths of a microamp. Also it was noted that the tran-
sistors were quite uniform in this respect which indicates
a very good match in the differential type of circuit.
Consequently, the cutoff characteristics could very well
be considered ideal, for this application.

It was found that the optimum cutoff voltage, E_1,
was not at all critical--a value anywhere from 0.1 to 1.2
volts being satisfactory. However, for other types of
transistors this value may be critical and generally
speaking the cutoff voltage should not exceed a few tenths
of a volt. It is conventional practice to use diodes as
the voltage limiting device for this state.

With the cutoff characteristics being very near
ideal, it is now very easy to choose a pair of transistors
which are also balanced with respect to their individual
saturation voltages. First, a circuit is constructed as
shown in figure 12, without the external signal source,

and using a square-wave generator as the switching voltage, E_1, source. Now by monitoring the output waveform with a high sensitivity, $1 \frac{mv}{cm}$, oscilloscope one can insert a pair of transistors, adjust the base current drive from zero through maximum, and note if a balance is obtained. If the balance is obtained the output wave form will appear as shown in figure 19. If not, there will always be an offset in the saturation state, as shown in figure 20. Thus it is not necessary to obtain any point by point plots, as shown in figure 15, to obtain a pair of matched transistors.

As far as the switching source, indicated as E_1, is concerned, either a voltage or current source may be used. However, as has been shown, it is the base current which drives the transistor into saturation, the on state, and the collector-to-emitter voltage which cuts off the transistor. Furthermore, the switching source must be isolated from ground to obtain the best results. For this purpose a pulse transformer was found to be very good.

In the actual chopper constructed for the dc amplifier, a square-wave voltage generator in conjunction with a pulse-transformer was used as the switching source, E_1. Under these conditions it is necessary to know what base current is produced by virtue of a given voltage. This information is easily obtained and illustrated in figure 16.

Figure 16, BASE CURRENT AND COLLECTOR-TO-BASE VOLTAGE
FOR THE 2N346 TRANSISTOR, INVERTED CONNECTION.
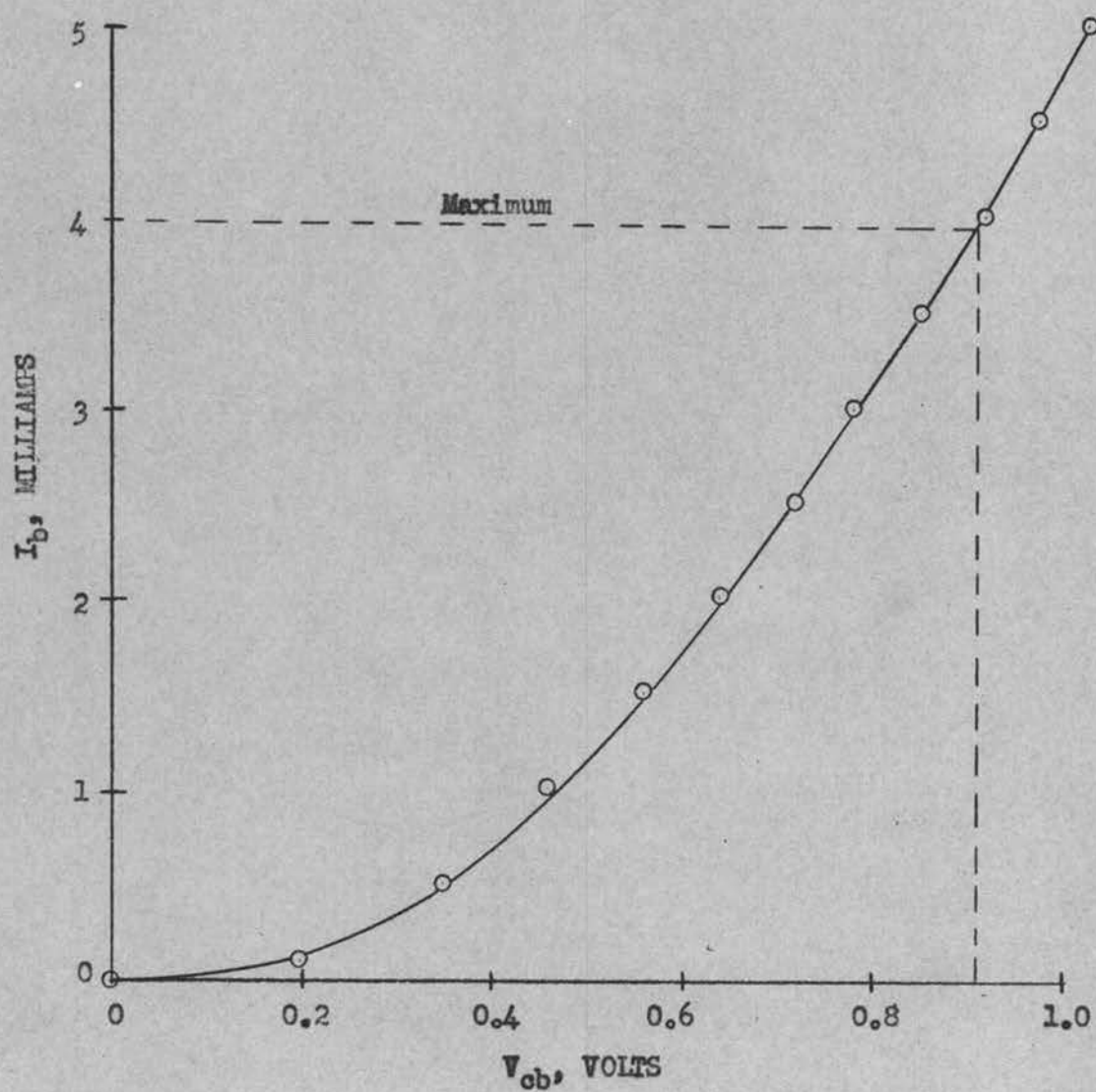
From this curve, then, a given base current can be imposed
by virtue of the applied voltage. The primary reason for
obtaining this curve, however, is to find the maximum
voltage which can be applied without exceeding the current
limitations of the transistor. Since the current is an
exponential function of the applied voltage, it is very
easy to apply slightly too much voltage, greatly exceed
the current rating, and destroy the transistor. This point
deserves considerable emphasis.

The transient response of this switch can be seen
from an analysis of figures 19 and 20. It is fairly
obvious that the primary transient occurs as the switch
changes states. This is a result of the instantaneous
change of the direction of the current in the base region.
The resultant spike or transient is of about 25 to 50
millivolts magnitude and has a duration of about 0.4 micro-
second. Aside from this transient the switch is very well
behaved. No trouble is encountered with delay time or
hole-storage time because of the very thin base region
of the surface barrier transistor and the very small mag-
nitude of signals, less than one millivolt potential and
about a microamp of current, being switched. Along with
this discussion it should be mentioned that given equal
quality transistors, the NPN transistor will generally
exhibit faster transients than the PNP transistor because

of the higher mobility of electrons as compared to holes.

Based upon this discussion an input chopper was con-
structed as shown in figure 41, for the proposed dc
amplifier. The switch itself exhibited a detectable change
in output for less than 10 microvolts input and produced
no appreciable bias error in either state, conducting or
non-conducting.

AC Amplifier Design Considerations

The design of the ac amplifier is for the most part
a straightforward application of the transistor. Since
it was desired to be able to utilize chopping frequencies
of from 10 kc to 100 kc, it was necessary that the ac
amplifier have a bandwidth of from 10 kc to about 1 Mc.
The other primary requirement of the ac amplifier was
that it have a voltage amplification of about 20,000 or
more in the passband with a minimum of noise, distortion,
and temperature variations.

The gain versus bias stability conflict which was
described previously does not apply to an ac amplifier
because of the possible use of reactive bypass elements.
In this connection, it should be noted that the emitter
leg bypass capacitors should present a 99% bypass in the
applicable frequency range to the resistor which they are
to bypass. If the conventional 90% bypass elements are

used, it is very likely that undesired degeneration and phase-shift will occur.

The coupling and composition of the ac section was determined primarily by thermal considerations. It has already been shown that the direct-coupled configuration of the same type, PNP or NPN, has the best thermal stability of any other combination. Consequently this scheme was used.

Of the available transistors the 2N247 and 2N248, both PNP, seemed well adapted to this application since they have a moderate h_{fe} of about 40 to 80 and a common base alpha cutoff frequency of 30 and 50 Mc, respectively. The noise figures of the transistors were not available, however, they were judged to be acceptable. Also, the linearity of h_{fe} was considered acceptable from a brief analysis of their characteristic curves.

To obtain the number of stages which are required one must first make an approximation of the voltage amplification which can be effected per stage. Generally speaking, with some current feedback, an amplification of 20 is easily obtained per stage. With this figure as a base, then, four stages would yield a voltage amplification of 160,000. Thus about 20 db of additional feedback could be applied and still maintain an amplification of 20,000. This would generally be considered enough feedback to make

the amplifier quite stable. Consequently four stages were
judged to be adequate.

The quiescent operating points and biasing networks
were chosen and constructed by conventional procedures
(18, p. 82-101). Of the four stages it was found easiest
to accomplish a current gain with the first three stages,
and to use the fourth stage as a voltage amplifier.

Two different types of feedback were used as indicated
on the circuit diagram, figure 41. First, current feed-
back in the form of an unbypassed emitter resistor of from
50 to 200 ohms was used to obtain some degeneration and
stabilization. Additionally this type of feedback offers
possibilities of extending the frequency response at the
higher frequencies by providing a partial capacitive by-
pass to lower the input impedance of the stage and hence
boost the high frequency amplification.

The second type of feedback is a type of dual voltage
feedback, in that a voltage is fed back which is propor-
tional to the output current. This type of feedback was
applied from the emitter of one stage to the base of the
preceding stage. This type of feedback has the normal
advantages attributed to loops which enclose two stages
rather than a single stage, and also the fact that the
feedback is taken from a low-impedance point and applied
to a high-impedance point. Thus it does not load down

the stages enclosed in the loop.

Another point to be noted is that because of the high voltage amplification involved and the use of non-ideal power supplies, decoupling was found to be necessary to prevent random oscillations.

Although in a direct-coupled circuit, each stage is somewhat dependent upon the preceeding stage, transistor interchangeability is not adversely affected. To change transistors, generally only a readjustment of the emitter resistor is required to compensate for the variation in transistor parameters which is encountered.

Utilizing the methods outlined above an acceptable ac amplifier was constructed with an amplification of about 22,000 and a bandwidth of 950 kc. For more results see the chapter entitled "Experimental Results".

Demodulator Design Analysis

At this point in the design, the original dc information has theoretically been chopped and amplified. Now it is desired to recover the amplified information, a process referred to as demodulation.

It should be noted, that by necessity the input circiut must contain a series capacitor between the input chopper and the ac amplifier to isolate the chopper from the dc level at the input to the ac amplifier. Since this

capacitor cannot pass a dc voltage, it distributes the
chopped signal about the dc level at the input to the ac
amplifier. Thus to recover the chopped and amplified
information, only a half of each cycle must be utilized.
This is easily accomplished by using a series switch to
connect the output of the ac amplifier to a low-pass
filter during a half of each chopping cycle.

Since the ac amplifier produces no appreciable phase-
shift the positive portion of the chopped wave at the
output of the ac amplifier would be in phase with a posi-
tive input signal, and the negative portion 180° out of
phase with the original signal. Either portion may be
recovered depending upon the phase of the recovered
signal which is desired. In this specific case the posi-
tive in-phase portion was required.

The resultant demodulator then takes the form shown
below.

Figure 17. An Equivalent Demodulator Circuit Diagram

Where:

R_S = Output im-
pedance of ac
amplifier

R_L = Input im-
pedance of dc
amplifier
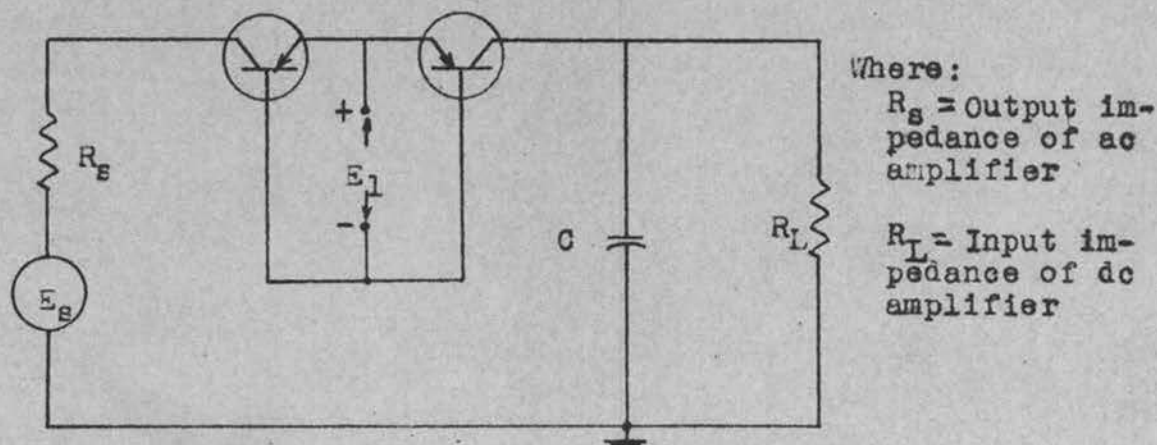
For a theoretical minimum noise, the capacitor should charge very fast and discharge very slowly or $R_s \rightarrow 0$, and $R_L \rightarrow \infty$. Since the common-emitter stage has an output impedance of several thousand ohms, it was decided to use a common-collector output stage on the ac amplifier to feed the demodulator from a low impedance source, about 1,000 ohms. However, it was later found that a source impedance of several thousand ohms was more desirable since the modulated wave contains several undesirable transients. Thus, by making the charging time-constant longer, the demodulated output of the capacitor could not follow the very brief transients and the noise was considerably reduced. Therefore, the common collector ac output stage is not necessary.

The switch itself is similar to the input chopper discussed previously except that the normal series connection is used. This is a better configuration for the high-level application involved here. Also, the 2N588 transistor was chosen over the 2N346 for this application because of its better high-level characteristics.

The parameters of the equivalent circuit, figure 17, which were obtained in the actual demodulator were approximately $R_s = 6,000$ ohms, $R_L = 20,000$ ohms, and $C = 0.02$ uf. Thus the charging time-constant was about 0.12 milliseconds and the discharge time-constant about 0.40 milliseconds,

assuming idealized switching conditions. These parameters were found to be about optimum for a chopping frequency of 80 kc, or a chopping period of 12.5 microseconds.

Output DC Amplifier Design Requirements

After constructing and testing the input circuit, input chopper, ac amplifier and demodulator, it was found that the overall amplification from the input to the output of the demodulator was about 5,000. Thus an amplification of at least 4 is required to boost the total amplification to 20,000 or more.

As previously discussed, it was also required that the input impedance to the high-level dc amplifier be in the order of ten or twenty thousand ohms.

To achieve this minimum gain of 4 along with an input impedance of about 20,000 ohms, and acceptable thermal stability, it was decided that silicon transistors would be necessary. This conclusion is apparent after setting up a few theoretical circuits which satisfy the amplification and input impedance requirements, and then calculating the stability factors for the various circuits, allowing a $15^{\circ}F$ temperature variation. With germanium transistors it was found that the quiescent collector voltage could easily change a volt or more, while with silicon transistors the change was in the order of

hundredths of a volt.

The NPN type of transistor, in contrast to the PNP transistors used in the ac amplifier, was chosen in order to use the quiescent dc level of -14 volts at the output of the demodulator to the best advantage. In addition to the type, it is easily seen that a moderate h_{fe} is desired along with an alpha cutoff frequency of several hundred kilocycles.

One more condition must be imposed before a satisfactory transistor can be chosen. This condition is that the transistor must have a maximum collector-to-emitter voltage in the order of 40 volts or more if a $\pm$ 15 volt output swing is to be permitted. This is true because the common-emitter amplification stage must produce a plus or minus 17 or 18 volts which is attenuated to 15 volts by the common-collector output stage and the AZS arrangement.

From these conditions, then, the 2N334 transistor was chosen. Specifically, it is a silicon type NPN transistor with an h_{fe} of about 40 and an alpha cutoff frequency of 8 Mc. In addition it has a maximum collector-to-emitter voltage of 45 volts.

The output dc amplifier circuit itself is a straight-forward conventional type of circuit, which presents no unusual situations. However, the common-collector output stage requires considerably juggling of power supplies

and breakdown diodes until the proper combination of
voltages is arrived at whereby the quiescent output level
will be zero volts dc.

It is naturally understood that the common-collector
output stage besides providing an AZS arrangement was asked
to provide a low output impedance of about 1,500 ohms.
This value can be calculated from circuit equations (16,
p. 11-23) or obtained experimentally. The output impedance
could easily be lowered to 1,000 ohms or less with a proper
choice of power supplies.

Additionally, the low-pass RC filters or shaping
networks were found necessary to limit the bandwidth and
consequently reduce the output noise.

EXPERIMENTAL RESULTS

In the manner described previously, a dc chopper amplifier was constructed as indicated on the circuit diagram, figure 41. The completed circuit and test setup appeared as shown below.

Figure 18. Experimental Test Setup
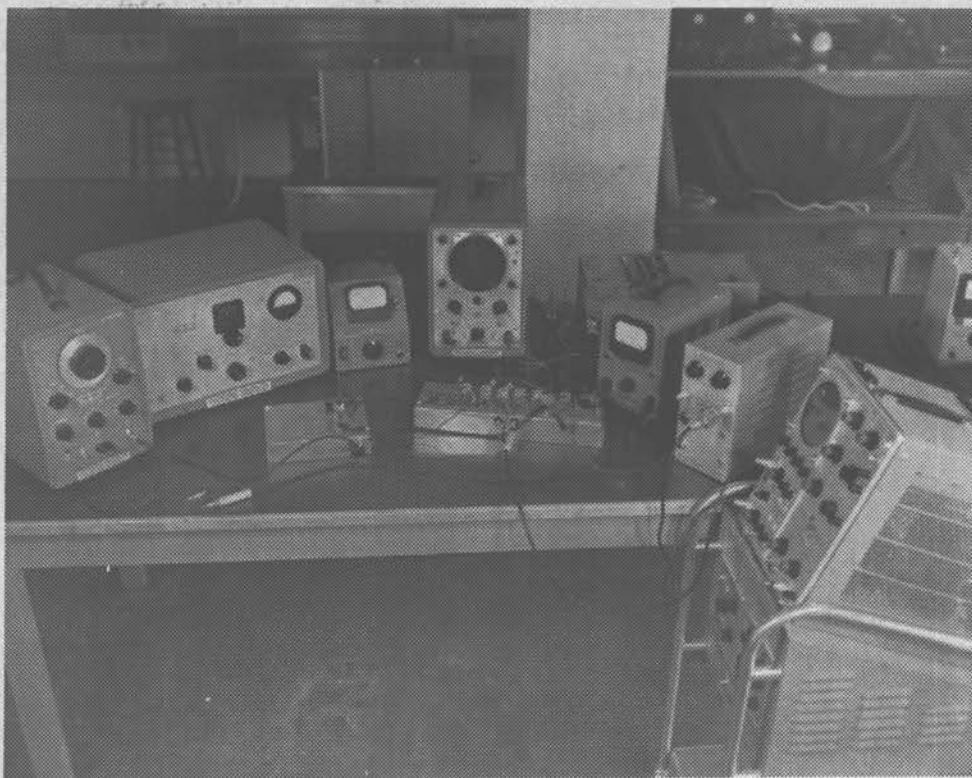
DC Amplifier Results

Before evaluating the specific results of the total dc amplifier, considerable insight into the operation of the amplifier can be gained by examining the oscillographs recorded at various points in the circuit under various

test conditions. All oscillographs were recorded with an effective oscilloscope bandwidth of about 10 Mc and a chopping frequency of 80 kc unless otherwise noted. Also, the scale factors listed are per major division as shown on the oscillographs.

The operating characteristics of the input chopper were difficult to obtain pictorially because of the very small voltages involved, less than one millivolt. However, the output of the input chopper with a zero input signal appeared as indicated below.

Figure 19.   Output Voltage of the Input Chopper With A Zero
Input Signal

(A)

Horiz: 2 usec/div
Vert: 2.5 mv/div

(B)

Horiz: 2 usec/div
Vert: 25 mv/div
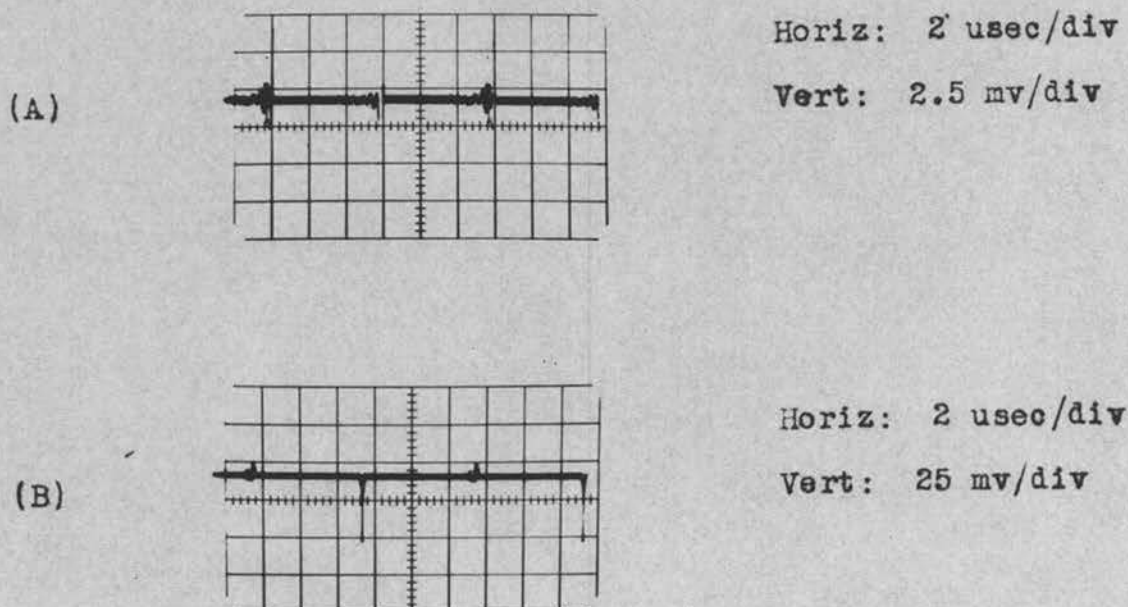
(C)
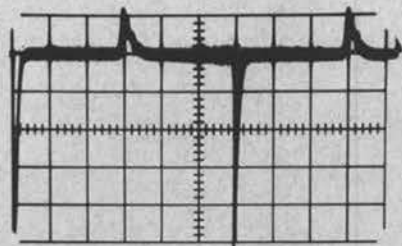
Horiz: 2 usec/div
(Bandwidth of 1.3 Mc)

Vert: 2 mv/div

The most important characteristic to be noted from these oscillographs are the form and magnitude of the transients which occur while the chopper is changing states. It should also be noted that there is no appreciable bias error produced in either state. Figure 19-C illustrates the waveform approximately as seen by the ac amplifier since the ac amplifier has a bandwidth of 950 kc and the oscillograph was recorded with an effective oscilloscope bandwidth of 1.13 Mc.

The output of the input chopper with an applied external signal is indicated below.

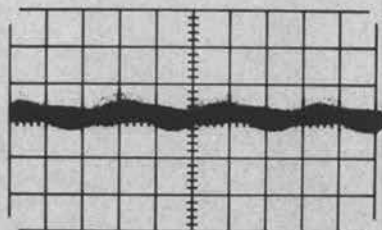Figure 20. Output Voltage of the Input Chopper With A -1 Millivolt DC Input Signal
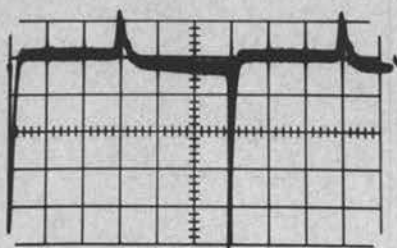
Horiz: 2 usec/div
(Bandwidth of 1.3 Mc)

Vert: 2 mv/div

Figure 21. Output Voltage of the Input Chopper With An
AC Input Signal

Horiz: 2 msec/div

Vert: 2.5 mv/div

The previously shown two oscillographs were recorded
on the output side of the capacitor connecting the chopper
to the ac amplifier, thus they represent the input to the
ac amplifier. The indicated response to a dc signal is
quite obvious, in contrast to the response to the ac sig-
nal. Figure 21 should contain two traces which have an
outline similar to the familiar amplitude-modulated wave.
Thus the outlines of the two traces should be 180° out of
phase with each other. However, the signal level had to
be increased beyond that required for normal operation to
obtain a visible trace, and they appear somewhat distorted.

The following figure illustrates the response of the
ac amplifier to the chopped waveform with a zero input
signal.

Figure 22. Input and Output Voltage Waveforms of the AC
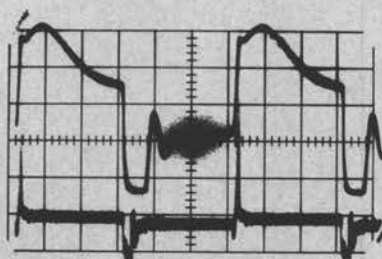Amplifier With Zero Input Signal

Upper trace:
    Horiz: 2 usec/div
    Vert: 2.5 mv/div

Lower trace:
    Horiz: 2 usec/div
    Vert: 5 v/div

This oscillograph vividly illustrates the hold stor-
age time accumulated by the ac amplifier in response to
the large transients caused by the input chopper. This
is a basic limit to the speed of chopping which can be
used effectively. The portion of the trace immediately
to the right of the negative transient is that produced
by the chopper being in the conducting or non-transmitting
state, and the portion immediately to the right of the
positive transient is produced while the chopper is in
the non-conducting, or transmitting state.

The response of the ac amplifier to an applied dc
input signal is seen in the following figure.

Figure 23. Input and Output Voltage Waveforms of the AC
           Amplifier With an Applied Input Signal of -0.8
           Millivolts

Upper trace:
   Horiz: 2 usec/div
   Vert: 5 v/div
Lower trace:
   Horiz: 2 usec/div
   Vert: 2.5 mv/div

This figure illustrates the change in the waveform
at the output of the AC amplifier caused by an input signal
of -0.8 millivolt. The lower trace was recorded at the
input to the ac amplifier, and the upper trace at the out-
put of the ac amplifier.

Figure 24. Output Voltage Waveform of the AC Amplifier
           With an AC External Signal
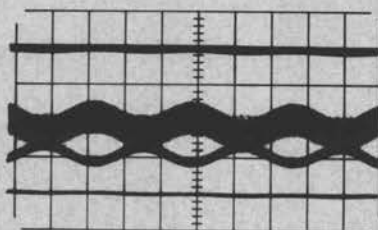
Horiz: 2 msec/div
Vert: .5 v/div

This figure illustrates the waveform produced at the
output of the ac amplifier by virtue of applying an ac
signal at the input to the dc amplifier. It will be noted

that the two outlines of the ac signal are 180° out of
phase as they should be.

The next figure illustrates the ability of the output
demodulator switch to control large signals. The illustra-
tion was obtained by replacing the input to the switch by
a simple dc source and removing the demodulator capacitor.
Thus the switch should ideally connect the dc source to
the resistive load and disconnect it according to the
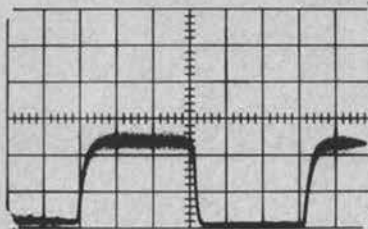polarity of the switching voltage.

Figure 25. Response of the Demodulator Switch to Large
Signals

(A) Applied source of 15 volts
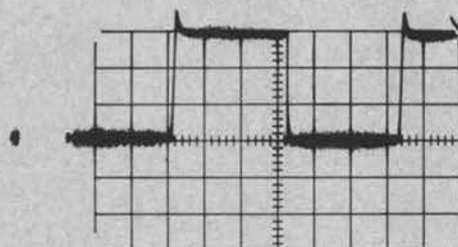
Horiz: 2 usec/div
Vert: 5 v/div

(B) Applied source of -15 volts
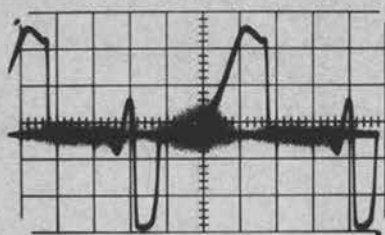
Horiz: 2 usec/div
Vert: 5 v/div

It is seen from this figure that the switch can control positive signals as large as 15 volts very well, however, as is typical of this switch it does not quite completely turn off a negative signal of 15 volts. It was observed, though, to control a negative 10 volts very well. Since the maximum signal to be encountered in application is 5 volts, it was concluded that this series type of switch can control these signal magnitudes very well.

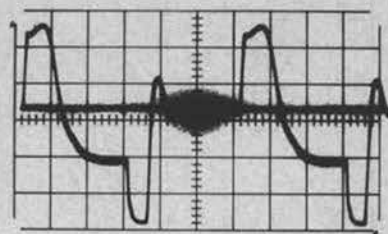The following illustrations depict the response of the demodulator to an applied dc signal.

Figure 26.　Input and Output Voltage Waveforms of the Demodulator in Response to a Given DC Signal
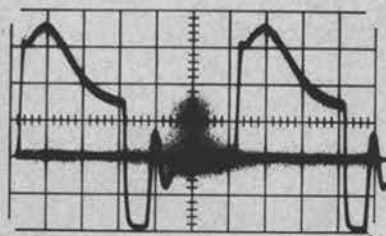
(A)　Zero Input Signal

Both traces:
Horiz: 2 usec/div
Vert: 5 v/div

(B) +0.8 Millivolt DC Input Signal

Both traces:
Horiz: 2 usec/div
Vert: 5 v/div

(C)   -0.8 Millivolt DC Input Signal

Both traces:
    Horiz: 2 usec/div
    Vert: 5 v/div

In these oscillographs, both traces were recorded
with the same dc orientation, although the dc orientation
is not the same for all three oscillographs. The straight
line or trace was recorded at the output of the demodu-
lator, while the other waveform was taken from the input
to the demodulator, or the output of the ac amplifier
common-collector output stage. These figures then show
which part of the waveform the demodulator output follows.

Figure 27.   Input and Output Voltage Waveforms of the
               Demodulator in Response to an AC Signal Input

(A)
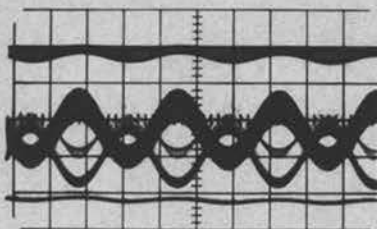
Horiz: 2 msec/div
Vert: 5 v/div

(B)

Horiz: 2 msec/div
Vert: 5 v/div

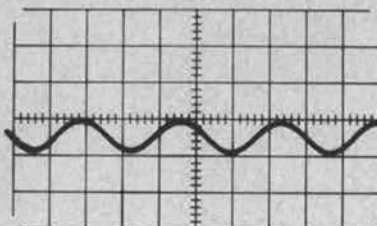The above two oscillographs were taken with corresponding phase and dc reference. The upper illustration shows the input to the demodulator, and the lower illustration shows the output of the demodulator. From these oscillographs one may easily see that the upper more fuzzy component of figure 27-A is the one which is recovered by the demodulator. The lower one could be recovered by merely changing the polarity of the switching voltage on the demodulator switch, however, it would be 180° out of phase with the original signal, as previously explained.

Figure 28. Output Voltage Waveform of Total DC Amplifier
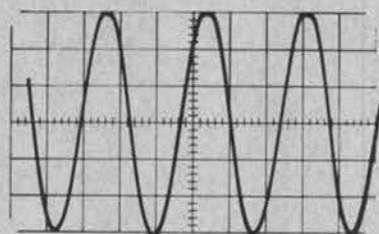
Horiz: 2 msec/div
Vert: 5 v/div

The above figure illustrates the sinusoidal waveform at the output of the dc amplifier with a full 30 volt swing from peak-to-peak.

The noise at the output of the dc amplifier with a zero input is depicted on the following page.

Figure 29.   Noise at Output of DC Amplifier
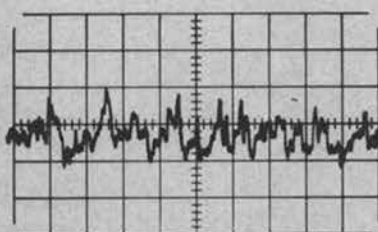
Horiz: 2 msec/div
Vert: 0.25 v/div

It can be noticed that the noise is primarily com-
posed of low frequency components, and has a maximum peak-
to-peak magnitude of about 0.6 volts.

The switching voltage waveform used throughout the
tests appeared as indicated below.

Figure 30.   Switching Voltage Waveform
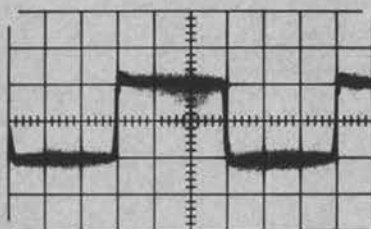
Horiz: 2 usec/div
Vert: 0.25 v/div

A very pertinent characteristic of the overall dc
amplifier is the effect of variations in the chopping
frequency. This effect is shown in figure 31.   (Figures
31 through 41 are contained in Appendix I.)

This figure illustrates that the amplification of

the overall dc amplifier is quite indifferent to changes
in the chopping frequency over a fairly large range of
frequencies. The overall amplification is within 2 db of
maximum with a chopping frequency anywhere from 20 kc to
80 kc, with the 3 db down points at 12 kc and 140 kc.
The fall-off at low frequencies is caused partly by the
fall-off of the ac amplifier at low frequencies and partly
by the inability of the pulse transformers, which supply
the switching voltage to the switches, to pass good square
waves. At low frequencies their output becomes the deriva-
tive of the input square wave. The high frequency fall-
off is caused primarily by the fall-off of the ac amplifier
and the effects of the transients produced by the input
chopper which become more critical as the chopping period
is reduced. Both the input chopper and the demodulator
switch were found to switch very effectively as high as
three or four hundred kilocycles. However, with an ac
amplifier response as indicated in figure 32, the ability
to pass a good representation of a square wave is limited
to about 100 kc. It is generally understood that at least
five harmonics are required to produce an approximation
of the square wave. This would mean the first, third,
fifth, seventh, and ninth harmonic of the fundamental,
since the square wave is composed of an infinite number
of odd harmonics.

The ac amplifier also causes a time lag from input
to output of about 0.3 usec, or a phase lag of about
9° at 80 kc. This characteristic is probably beneficial
as it indicates that the demodulator switch changes states
slightly before the corresponding part of the chopped
signal has been passed. Thus the demodulator retains the
potential of the top of the chopped wave rather than a
magnitude determined by the transients or round off of the
chopped signal.

The frequency response of the overall dc amplifier
is shown in figure 33. The amplification is flat from
dc to 400 cps with a 3 db down point at 1,100 cps which
is just slightly beyond the requirement of 1,000 cps.
The phase-shift from input to output is 117° at the 3 db
down point.

The frequency response of the overall dc amplifier
is primarily determined by the demodulator and output
dc amplifier, the remainder being due to the input filter
and half-wave chopping technique. This conclusion is
easily seen by comparing figure 33 to figure 34 which
shows the frequency response for the output demodulator
and output dc amplifier. The rather abrupt fall-off in
amplification and the consequent rise in phase shift are
caused by the demodulating capacitor, and the other low-
pass RC filter placed in the output dc amplifier. These

filters were necessary, first, to maintain stability, and second, to reduce the noise of the overall dc amplifier. Since noise is approximately proportional to bandwidth, doubling the bandwidth approximately doubles the noise at the output. Stability could be obtained with a much larger bandwidth, as large as ten or twenty kc, however, the presence of considerable noise required that the bandwidth be reduced to a minimum. This then is the reason for the restricted bandwidth.

The noise at the output of the overall open-loop dc amplifier was found to be about 0.6 volt peak-to-peak, or about 0.3 volts as indicated on an rms voltmeter with a frequency range of 20 cps to 2 mc. Of this total, about 5 millivolts peak-to-peak were contributed by the output dc amplifier alone, and about 0.3 volts peak-to-peak by the ac amplifier alone. The comparatively large noise voltage of the overall dc amplifier, however, was found to be produced by the chopped waveform, entering the ac amplifier, being modulated by the noise of the first couple of ac amplification stages, the noise modulated signal being further amplified in the remainder of the ac amplifier, demodulated in the demodulator, and further amplified by the output dc amplifier. Consequently, to reduce the noise voltage without further limiting the bandwidth, a very low noise ac amplifier must be

constructed. Thus very low noise figure transistors,
especially at low frequencies, are indicated.

In this discussion it should also be noted that con-
siderable emphasis must be placed on obtaining power
supplies which exhibit very low noise voltages while
under load. If the power supplies indicate a noise volt-
age much in excess of 0.5 millivolts peak-to-peak, the
noise figures of the individual components and overall
dc amplifier increase very rapidly.

An added feature was also built into the output dc
amplifier in that by removing the 10,000 ohms series
resistance between the demodulator and output dc amplifier,
the amplification of the overall amplifier could be raised
from 26,500 to 44,000. This would represent a significant
improvement in the dc amplifier although the noise and
drift increase proportionally. However, because of the
great difficulty involved in obtaining valid open-loop
test results at the higher value of gain, the amplifier
was left at its lower value for the tests indicated in
this discussion.

It will be noted from the previous experimental
results, that this system is also wasteful of the amplifi-
cation built into the different components. With an ac
amplification of 22,000 and output dc amplification of
4.3, a total amplification of about 94,000 is possible.

However, out of this possible amplification of 94,000 only 26,500 is realized, the remainder being absorbed by the input circuit to the ac amplifier. In comparison, a very small amount of amplification is lost in the demodulation process. In addition, if the input impedance is increased, the total overall dc amplification is further reduced since the overall dc amplification is approximately inversely proportional to the input impedance.

During the operation of this test circuit it was noted that the long term drift, several hours, at a given room temperature was negligible in comparison to the noise, probably being less than 0.1 volt peak-to-peak.

The non-linear distortion of the overall open-loop dc amplifier was found to be 3.8%. This value represents a minimum value, as the exact settings of the chopping frequency and magnitude were optimized. The distortion is definitely dependent upon the magnitude and frequency of the chopping source, and the magnitude of the switching signal supplied to the demodulator switch; although not in a well defined manner. Consequently there values must be individually adjusted for best results. The non-linear distortion of the ac amplifier and output dc amplifier contribute only a very small part of the total observed non-linear distortion.

The thermal drift of the open-loop overall dc amplifier is indicated in figure 35. It is shown that

the overall dc amplifier has a drift of about 0.25 volt
in the temperature range of from 55°F to 85°F, which is
the normal operating temperature of laboratory equipment.
However, at temperatures much higher than 85°F the thermal
drift increases very rapidly. This sudden rise and then
fall is caused by the unbalanced temperature tracking
qualities of the germanium transistors used in the input
chopper. Thus, if one desires a small thermal drift at
high temperatures, silicon transistors or temperature
matched germanium transistors are indicated.

The contributions to the overall thermal drift by
the ac amplifier and output dc amplifier are illustrated
in figure 36. The rather non-uniform drift of the ac
amplifier is caused by the different temperature tracking
abilities of the different stages, diodes, and resistors.
The thermal drift of the output dc amplifier is rather
uniform although much higher than would be expected. This
would lead to the conclusions that either the silicon
transistors had higher I_{co} values than indicated, there
were some unusually temperature sensitive resistors in
the circuit, or the diodes had large temperature coeffi-
cients. It should be noted that the output dc amplifier,
particularly, is of an experimental nature. Thus it could
be "cleaned up" in a well thought out design and thus made
more stable with temperature.

From the preceding discussion, it is seen that the circuit as shown in figure 41 has the following major specifications.

1. Voltage amplification of 26,500.

2. Input impedance equal to 2,000 ohms.

3. Output impedance equal to 1,500 ohms.

4. Maximum output voltage swing of 15 volts.

5. Thermal drift equal to 0.25 volt in the temperature range of 55°F to 85°F.

6. Long term output drift less than 0.1 volt.

7. Bandwidth of dc to 1,100 cps.

8. Phase-shift at 1,000 cps equal to 117°, with reference to the input.

9. Noise at output equal to 0.6 volt peak-to-peak.

10. Non-linear distortion equal to 3.8%

11. The circuit requires matching input chopper transistors which is easily accomplished. Other transistors are interchangeable with only a readjustment of emitter resistor usually necessary. Individual adjustment of chopping frequency and switching signal magnitudes is necessary for optimum results.

As a word of caution, it should be mentioned that the dc chopper amplifier as shown in figure 41 is strictly an experimental circuit and consequently its physical circuitry could be improved.

Operational Amplifier Results

Since the dc amplifier was designed toward an application to the operational amplifier, its basic characteristics as an operational amplifier network are of interest. (The network, as shown in figure 1, becomes merely an operational dc amplifier if Z_1 and Z_2 are resistors, the ratio of R_2 to R_1 being termed the dc gain of the network. If Z_1 is a resistance, while Z_2 is a capacitor, the network becomes an integrating operational amplifier; and if the resistor and capacitor are interchanged, the network becomes a differentiating operational amplifier.)

The predictability of the operational dc amplifier was found to correspond very well with the theoretical values indicated in figure 44. With Z_1 and Z_2 in the order of 10 ohms to 10 Kohms generally very predictable operations could be performed, the error being in the order of 1%. However, with more incongruous values the error could easily be increased to 100% or more. An exact analysis of the predictability was difficult to obtain because of the required accuracy in components and measuring instruments.

The frequency response of the operational dc amplifier network is indicated in figures 37 and 38. From figure 37 it is noted that the bandwidth is nearly the same regardless of the value of dc gain, thus a trade of

bandwidth for gain is not effected. This characteristic was obtained because the fall-off of amplification with frequency of the overall dc amplifier was not the ideal 6 db per octave, and probably also because the resistors in the operational amplifier network were interacting with frequency sensitive elements within the dc amplifier itself. Consequently, at a dc gain of unity the bandwidth was only about 4,000 cps, at a dc gain of 48 the bandwidth was about 1,700 cps, and at the open-loop dc gain of 25,000 the bandwidth was still 1,100 cps.

The phase-shift response of the operational dc amplifier network at different values of dc gain is illustrated in figure 38. This figure shows that the phase-shift is relatively independent of values of dc gain below 50. This would be expected from the amplification response previously noted.

Also of particular interest is the amount of non-linear distortion which the particular operational amplifier network exhibits. This relationship is shown as a function of dc gain in figure 39. The non-linear distortion in the open-loop configuration was about 3.8% which decreased to less than 0.1% at unity dc gain. In the open-loop configuration, the switching frequency and magnitudes had to be individually adjusted to obtain the optimum results; however, when loaded down with feedback until

the dc gain was in the vicinity of 100 or less, the operational amplifier was quite insensitive to the switching frequency and magnitude.

The noise encountered in the operational dc amplifier was about 0.1 to 0.2 volt peak-to-peak for values of dc gain below 100.

The response of the integrating type of operational amplifier network is depicted in figure 40. With an RC time-constant of 0.005 seconds, the quality of integration would only be expected to be good above 200 cps, as shown. It is seen that the amplification of the network varies inversely as the frequency, and that the phase-shift, with reference to the input, is 90° for all useable frequencies. The phase-shift is not merely the phase-shift relationship of the open-loop dc amplifier plus an additional lag of 90° as might be expected, because the integration relationship is obtained as long as the amplification is high, with no regard to its phase-shift, as long as it is stable.

From a brief investigation of the integrating operational amplifier, it was generally concluded that the network behaved in a predictable manner within its limitations as indicated in Appendix III.

The differentiator type of operational amplifier network is not of very much practical use since its output

is primarily noise. This was easily verified. Consequently no specific data was taken on the differentiator type of network.

A complete analysis of the characteristics of the dc chopper amplifier used in operational amplifier networks is beyond the scope of this report.

CONCLUSIONS

General Discussion

Of the two possible modes of operation, current or
voltage, the operational voltage amplifier network is much
better suited to large scale analog computer operations
because of the possible use of common power supplies for
the operational amplifiers. The specifications for a
dc amplifier, to be used in such a network, may deviate
considerably from ideal, and still not destroy the use-
fulness of the amplifier. In particular, the input
impedance, output impedance, and phase-shift may vary
appreciably from the ideal, and as long as the amplifi-
cation is high, accurate and predictable operations may
be effected.

In selecting a transistor dc amplifier circuit for
such an application, considerations of voltage amplifi-
cation and temperature stability are of paramount impor-
tance. In general the direct-coupled type of dc circuitry
is unsatisfactory because of the conflict between bias
stability and amplification. However, the differential
type of circuit is much to be preferred to the single-
sided configuration. The conflict between bias stability
and amplification in direct-coupled circuits can only be
resolved appreciably by using matched or custom tailored

temperature sensitive elements. Thus one usually resorts to a dc chopper-stabilized or dc chopper-amplifier.

Of the chopper-stabilized amplifier or chopper-amplifier, the chopper-amplifier outwardly offers the simplest solution. However, the success of this system is primarily determined by the quality of the chopper. The chopper must also be a high frequency device in order to obtain a suitable bandwidth. Herein, a method has been developed whereby transistors can be easily picked which are matched at a specific value of base current and temperature, and thus exhibit ideal characteristics in a differential type of switch. Thus a very high quality switch can be constructed. This switch utilizes two transistors in the inverted connection, series pair configuration.

The principle disadvantage encountered with this type of chopper, however, is that the transistors are not necessarily balanced at all temperatures, thus considerable mismatch may occur at higher temperatures; and that an appreciable transient of about one-half microsecond duration is produced as the switch changes states. These imperfections are further magnified by the ac amplifier, and as a result the chopper-amplifier designed around this input chopper may have very poor temperature characteristics.

A chopper-type dc amplifier was constructed, as

illustrated in figure 41, which consisted of a series
arrangement of input chopper, ac amplifier, demodulator,
output dc amplifier, and their associated circuitry. The
input chopper was constructed as indicated above, and the
overall dc amplifier exhibited a thermal drift of 0.25
volts in a temperature range of from 55°F to 85°F, and an
output noise of 0.6 volt peak-to-peak with a bandwidth of
from dc to 1,200 cps. Other principle specifications were
an input impedance of 2,000 ohms, an output impedance of
1,500 ohms, a maximum output voltage swing of $\pm$ 15 volts,
and a voltage amplification of 26,500. A much larger
bandwidth could be utilized, however, the noise increases
approximately proportional to the bandwidth. The rela-
tively large noise voltage of 0.6 volts peak-to-peak was
caused by the noise of the ac amplifier modulating the
chopped signal.

Within its limitations the amplifier was found to
operate satisfactorily as an operational amplifier in
the integrator and dc amplifier operational networks. The
dc chopper amplifier as shown in figure 41, however, is
an experimental circuit and consequently its physical
circuitry could be improved. Its principle value lies
in providing the general characteristics of this type of
circuit --it is not an end result in itself.

Possibilities for Future Work

Future work in the field of transistor dc amplifiers could well be directed at improving the characteristics of the dc chopper amplifier which was investigated in this report. The principle disadvantages of this circuit were found to be its excessive thermal drift, noise, and low input impedance.

The use of silicon transistors in the input chopper would definitely improve the temperature characteristics of the circuit and possibly improve the chopping operation. Another possibility of improving the modulation technique lies in eliminating the switching transients. This would allow a much greater chopping frequency.

A delightful possibility of improving the overall dc amplifier is that of using a current-step-up transformer in the input circuit between the chopper and ac amplifier. This could possibily improve the switching characteristics, input impedance, and overall amplification.

An extremely low noise, high gain, ac amplifier is also required to reduce the noise of the overall system.

To further perfect the amplifier, it is quite probable that a phase-lead network could be utilized to correct for some of the undesired phase-shift.

From this investigation, it is definitely seen that the chopper-stabilized amplifier, figure 6-A, deserves

considerable investigation as it may prove to be a better system than the one herein investigated.

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APPENDIX I

ILLUSTRATIONS OF TEST RESULTS
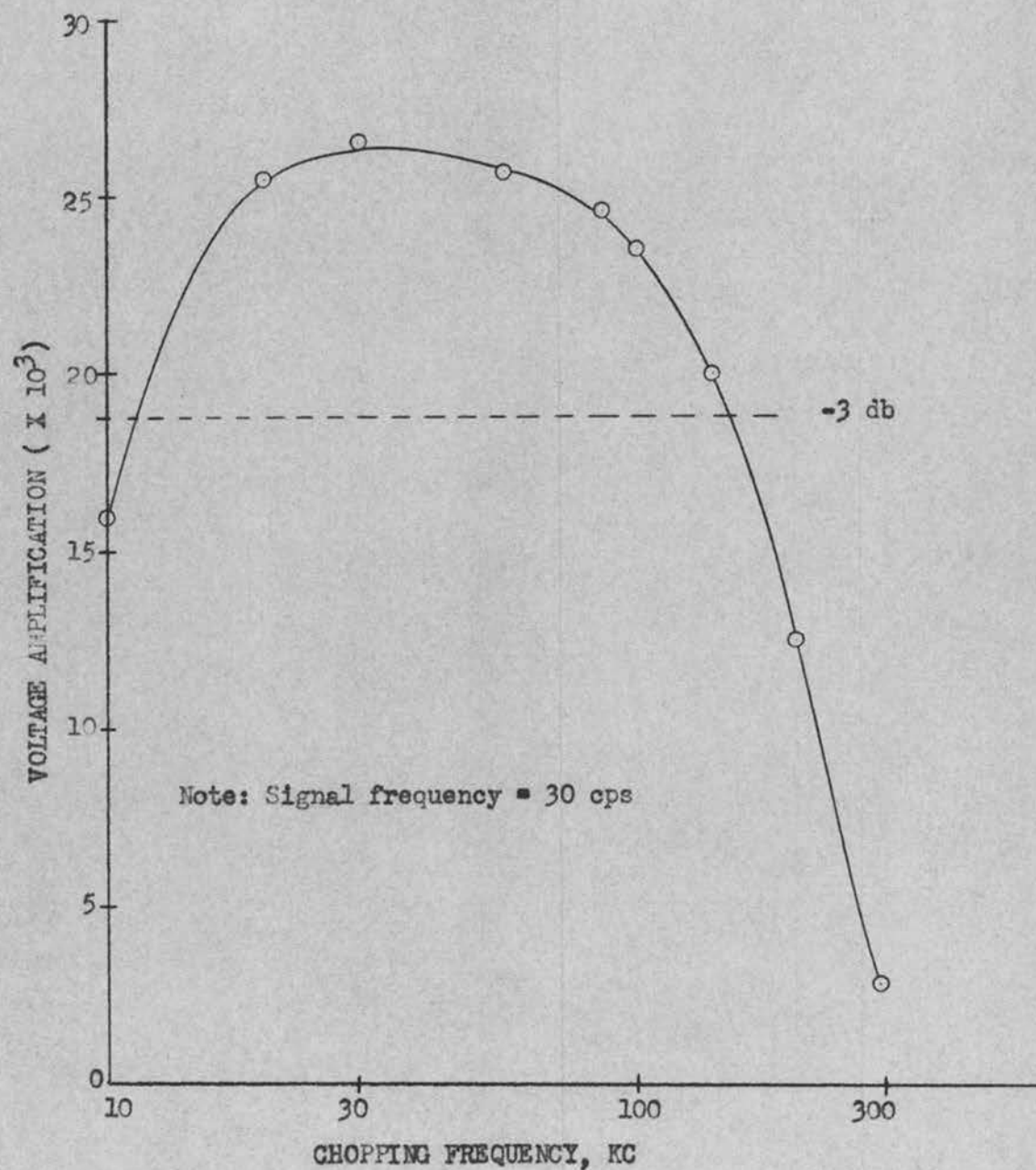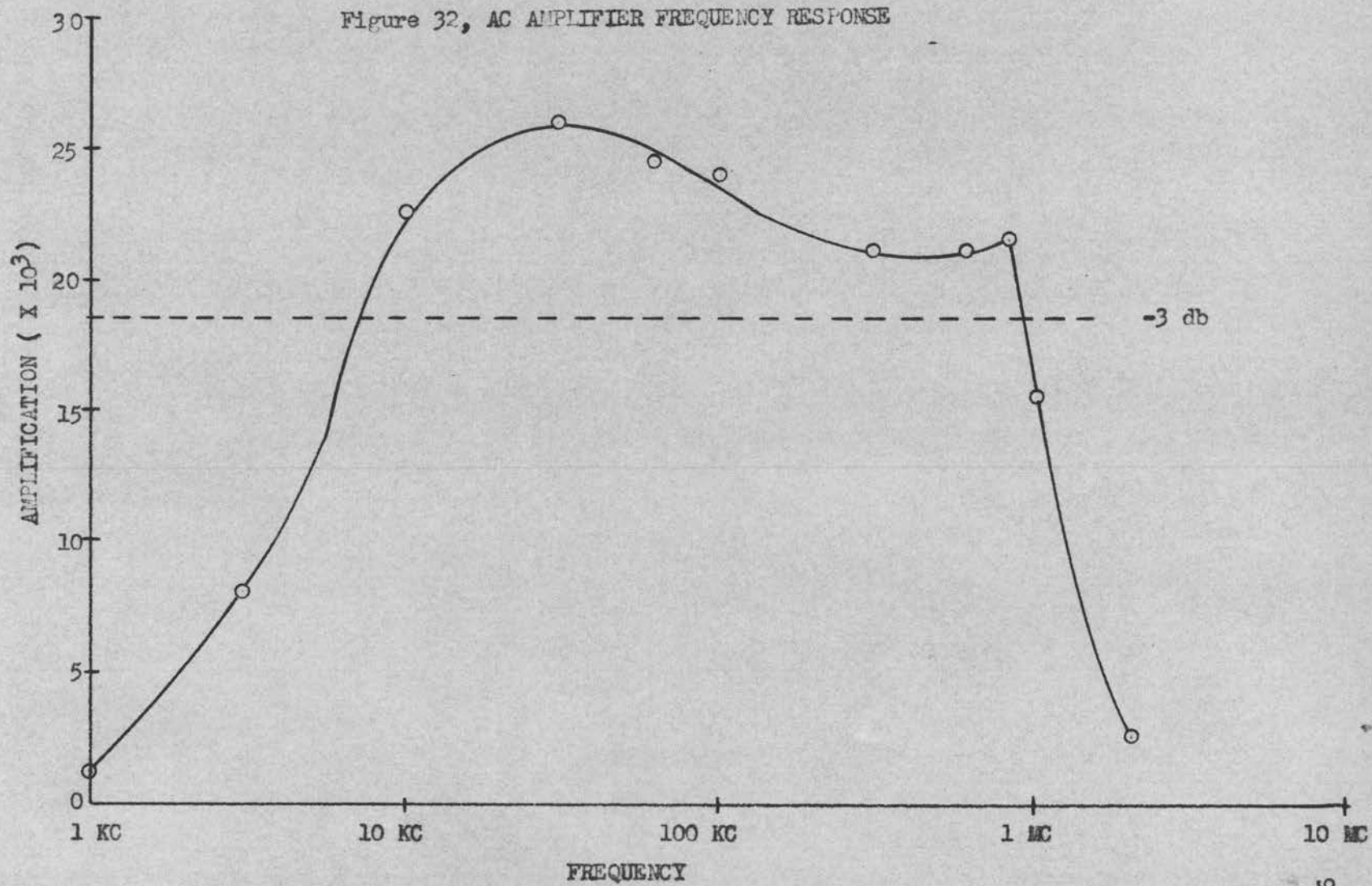
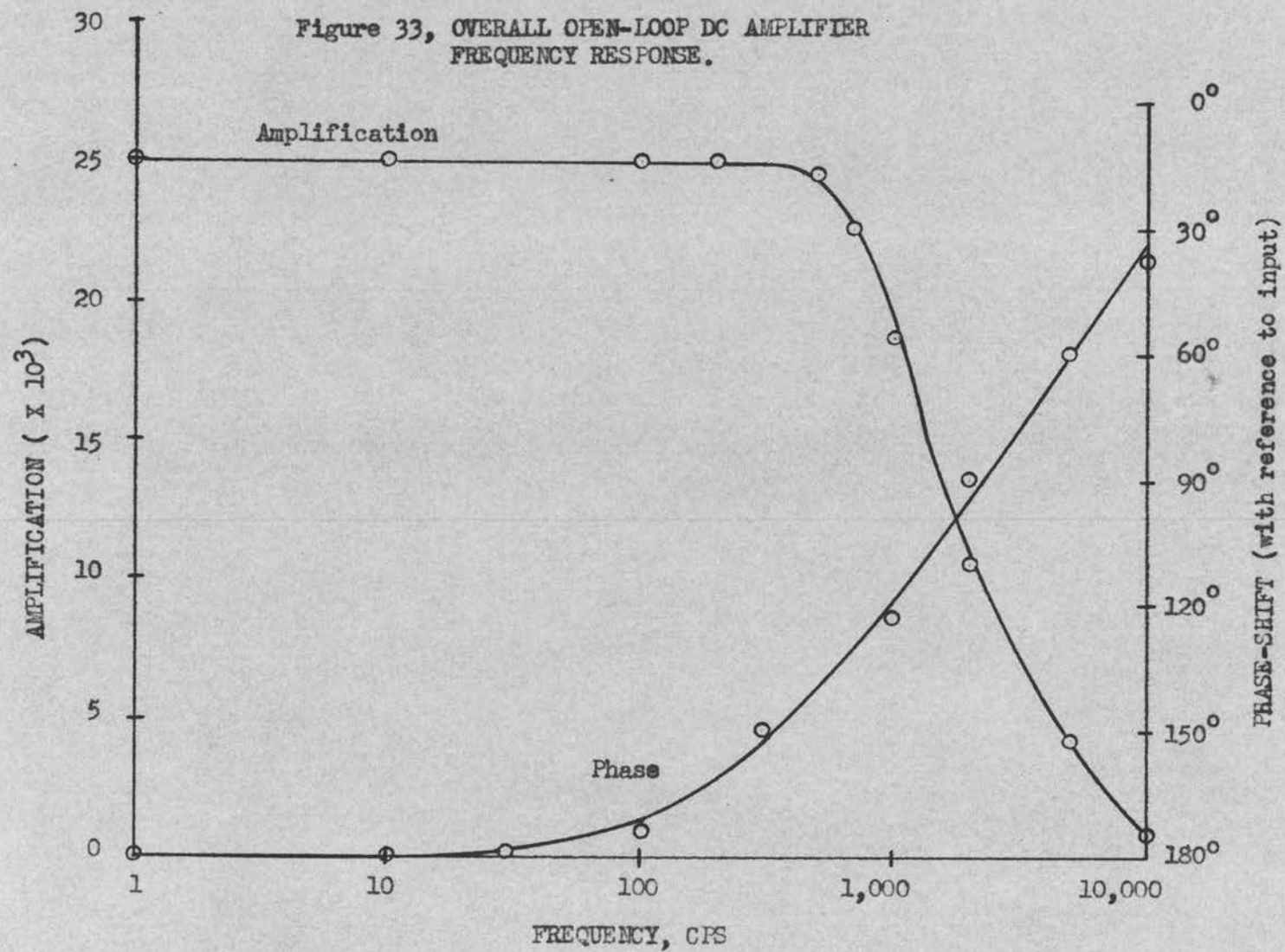Figure 31, OVERALL DC AMPLIFICATION AND CHOPPING FREQUENCY.

Figure 32, AC AMPLIFIER FREQUENCY RESPONSE

Figure 33, OVERALL OPEN-LOOP DC AMPLIFIER FREQUENCY RESPONSE.

Figure 34, DEMODULATOR AND OUTPUT DC AMPLIFIER
FREQUENCY RESPONSE.
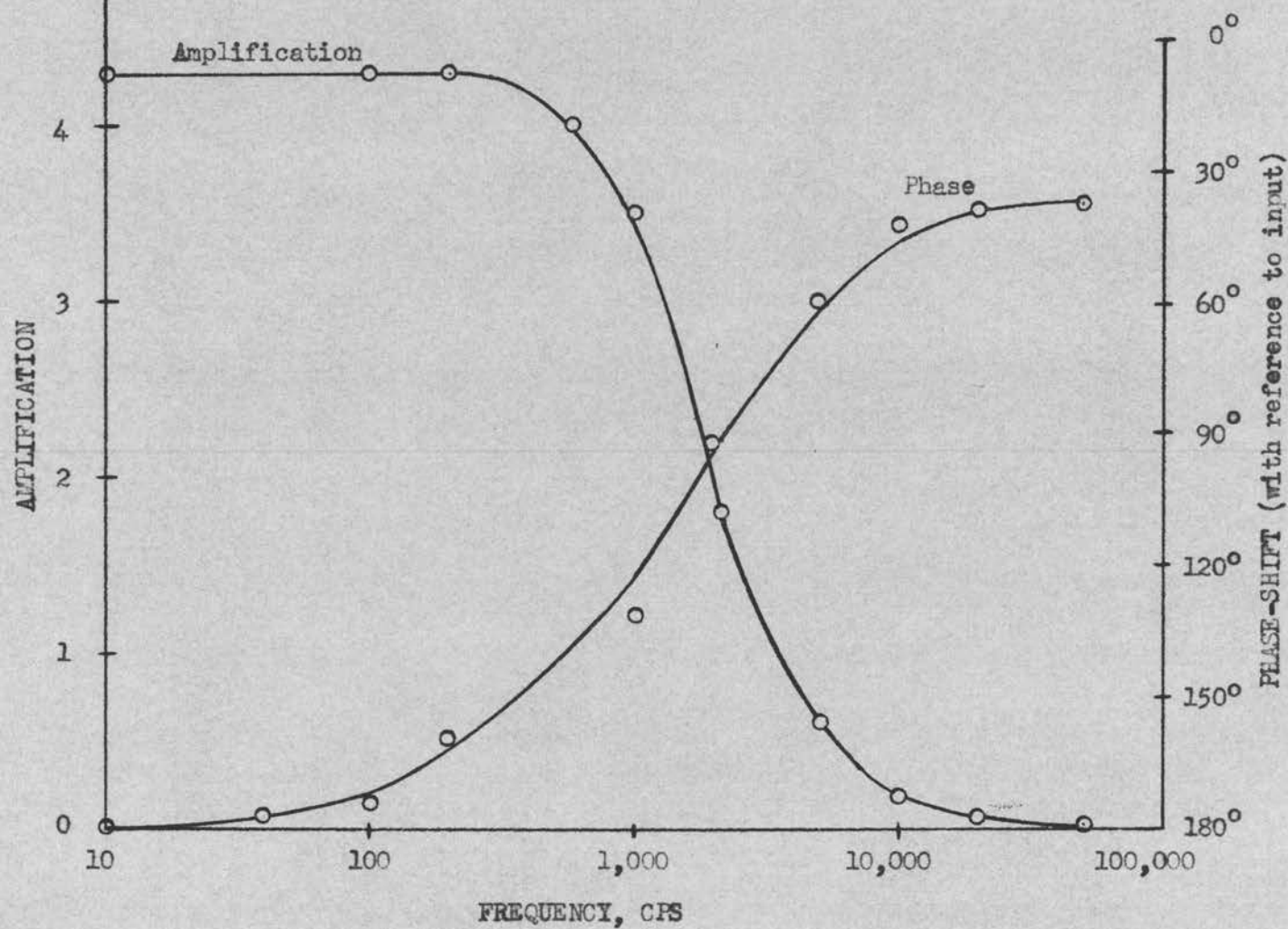
Figure 35, THERMAL DRIFT OF OVERALL OPEN-LOOP
DC AMPLIFIER.
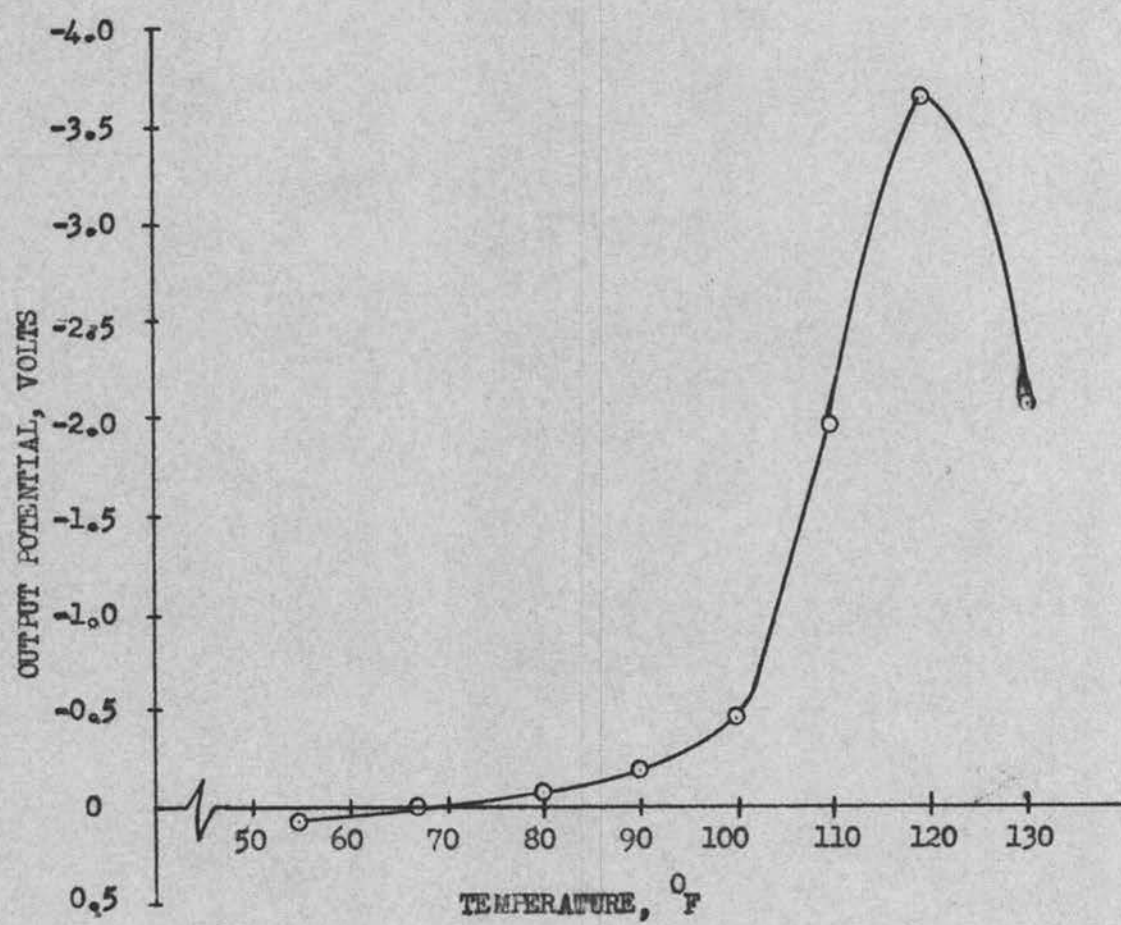
Figure 36, THERMAL DRIFT OF AC AMPLIFIER AND OUTPUT DC AMPLIFIER.
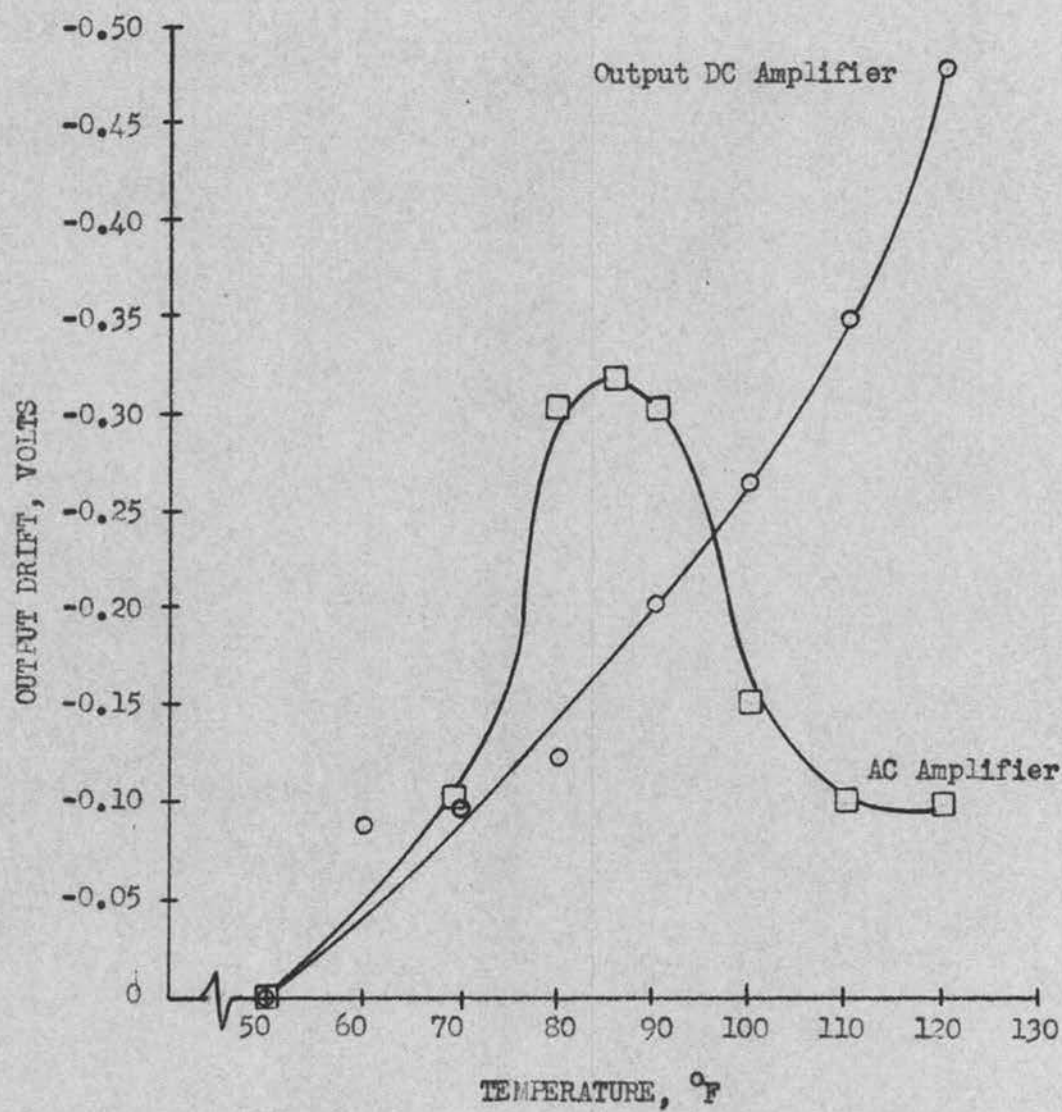
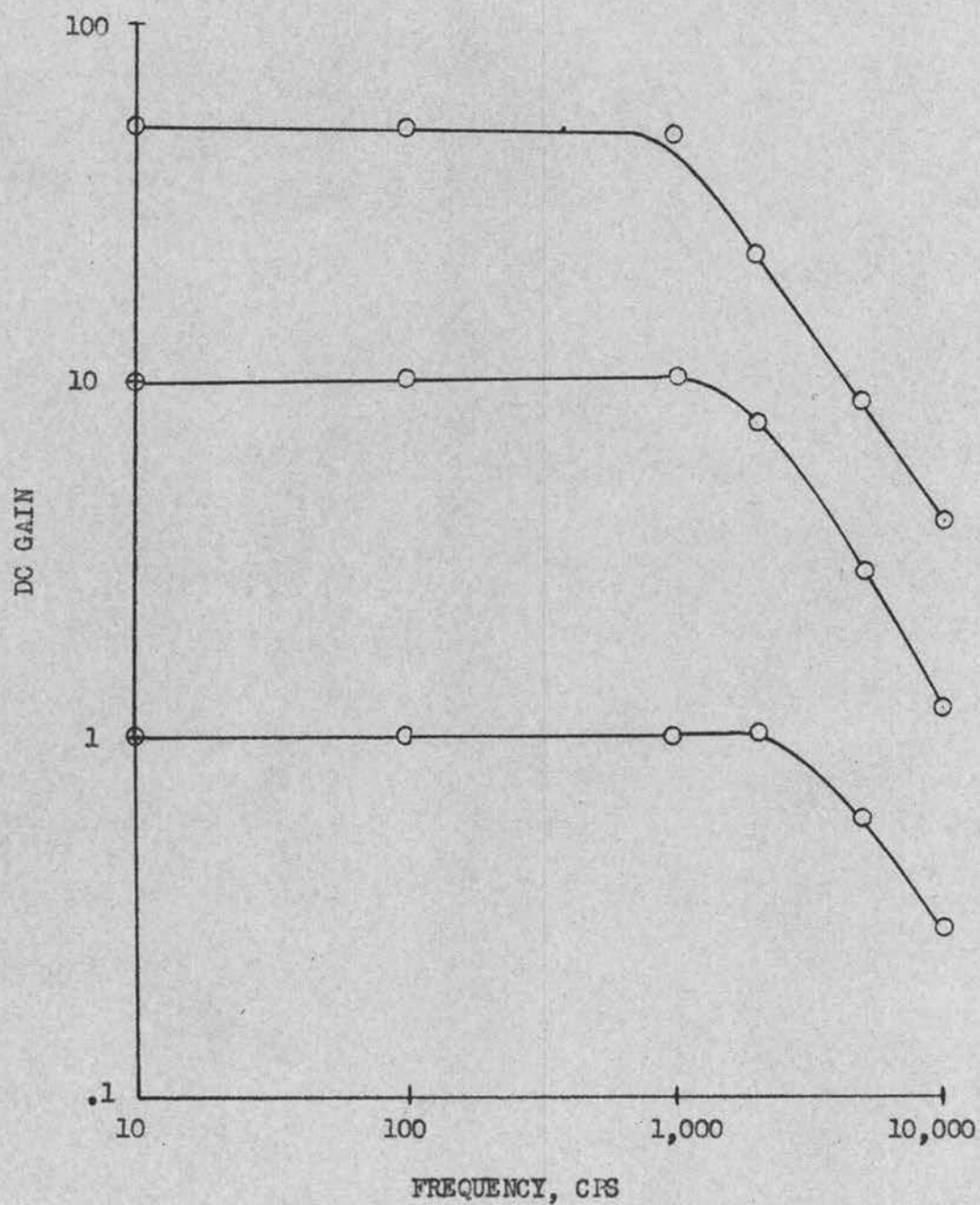Figure 37, FREQUENCY RESPONSE OF OPERATIONAL AMPLIFIER AT DIFFERENT VALUES OF DC GAIN.

Figure 38, PHASE-SHIFT AND FREQUENCY FOR THE
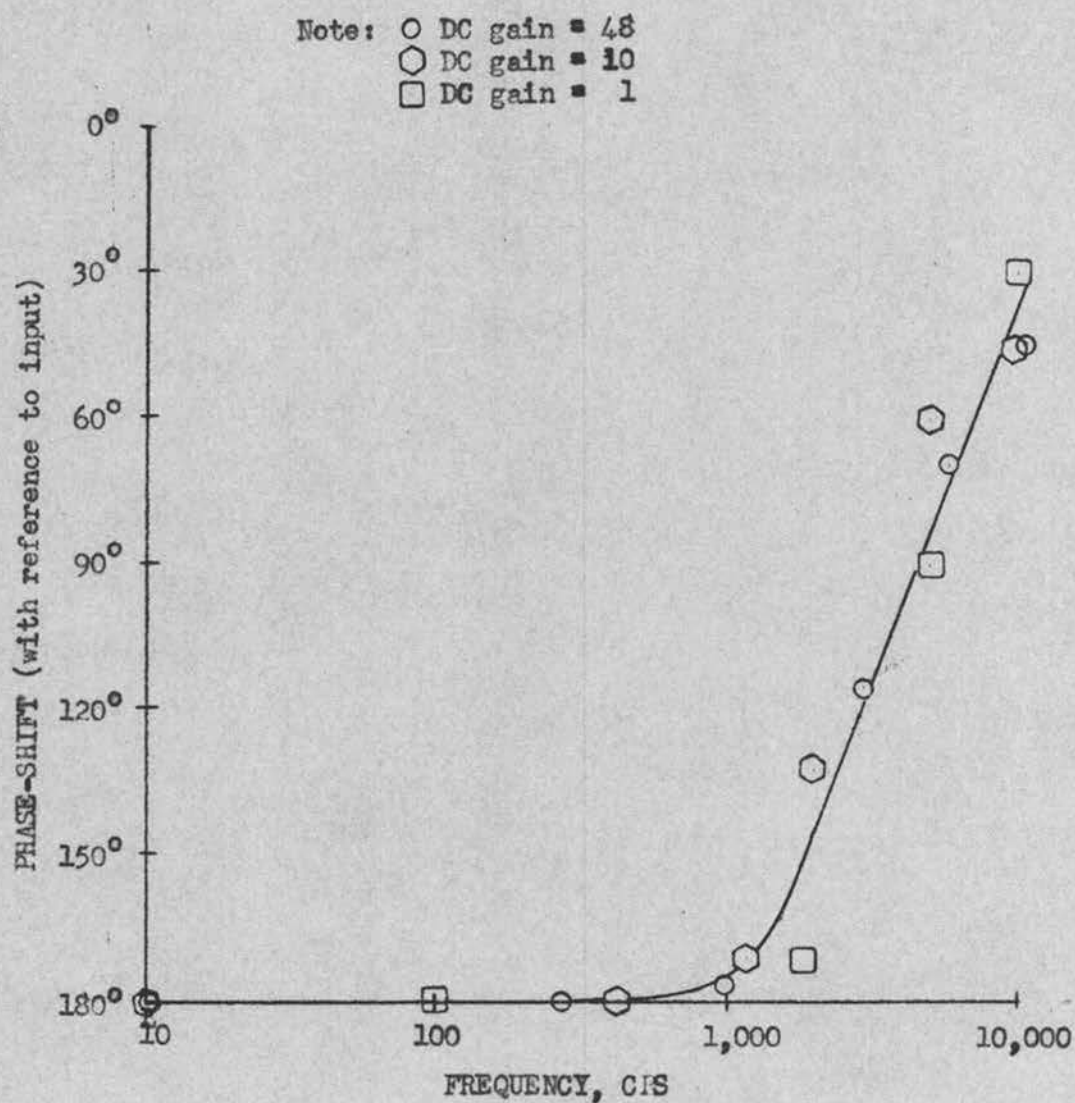OPERATIONAL AMPLIFIER AT DIFFERENT
VALUES OF DC GAIN.

Note: O DC gain = 48
⬡ DC gain = 10
☐ DC gain = 1

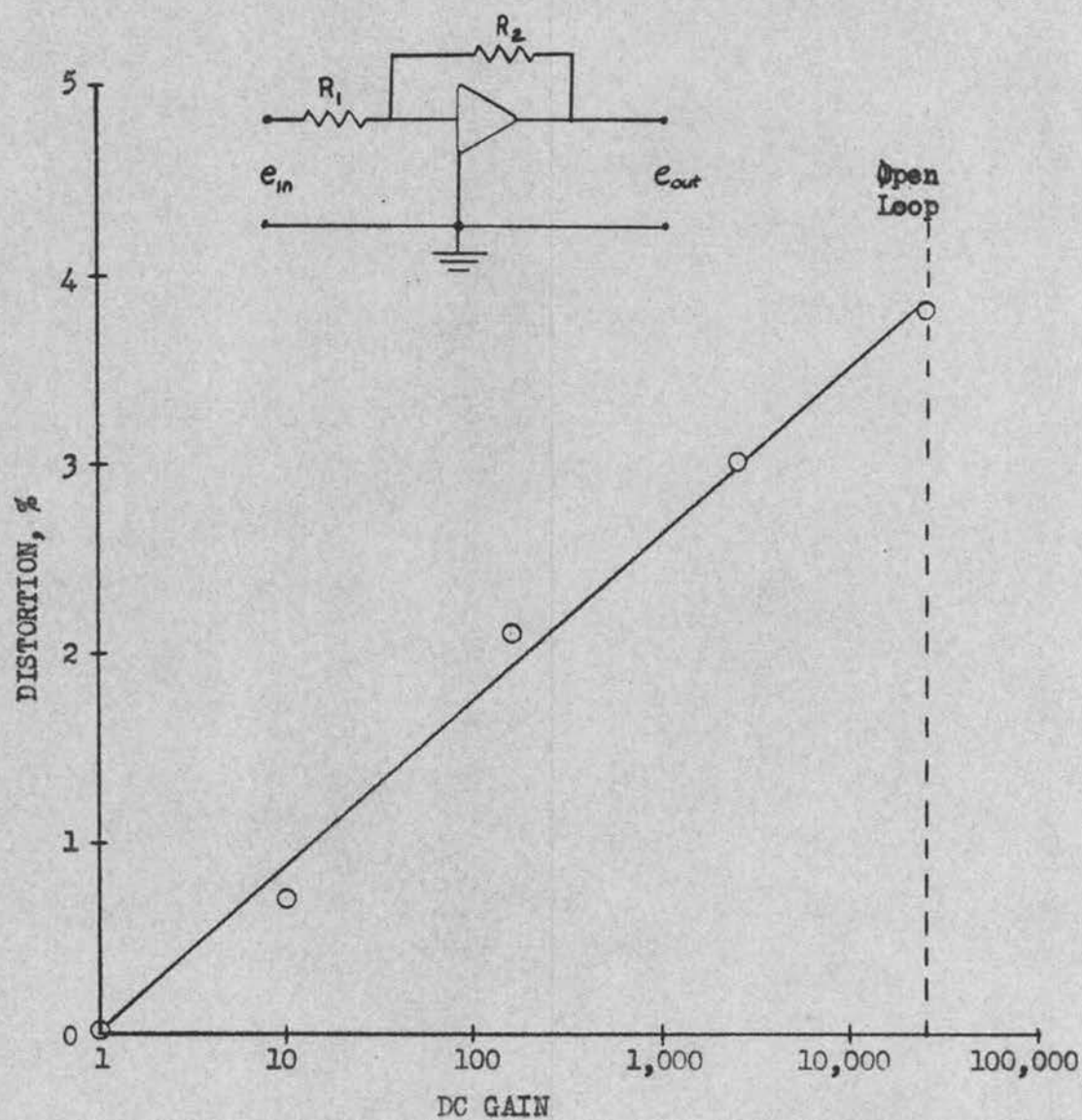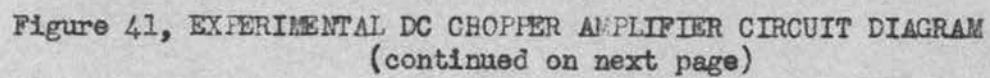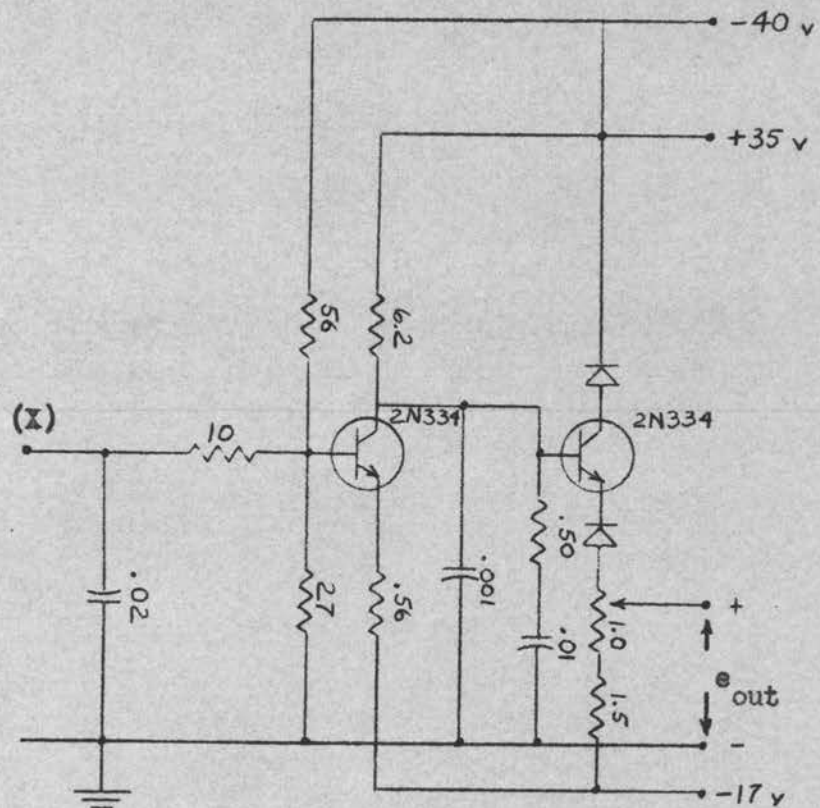Figure 39, NON-LINEAR DISTORTION AND DC GAIN OF THE OPERATIONAL AMPLIFIER.

Figure 40, FREQUENCY RESPONSE OF OPERATIONAL
AMPLIFIER INTEGRATOR NETWORK.

Note: R = 1.0 K Ω
C = 0.5 uf

Figure 41, EXPERIMENTAL DC CHOPPER AMPLIFIER CIRCUIT DIAGRAM
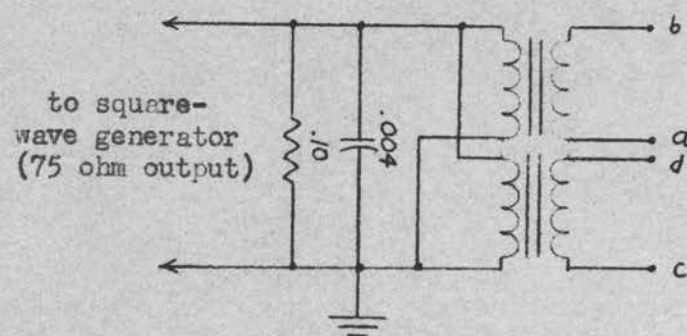(continued on next page)
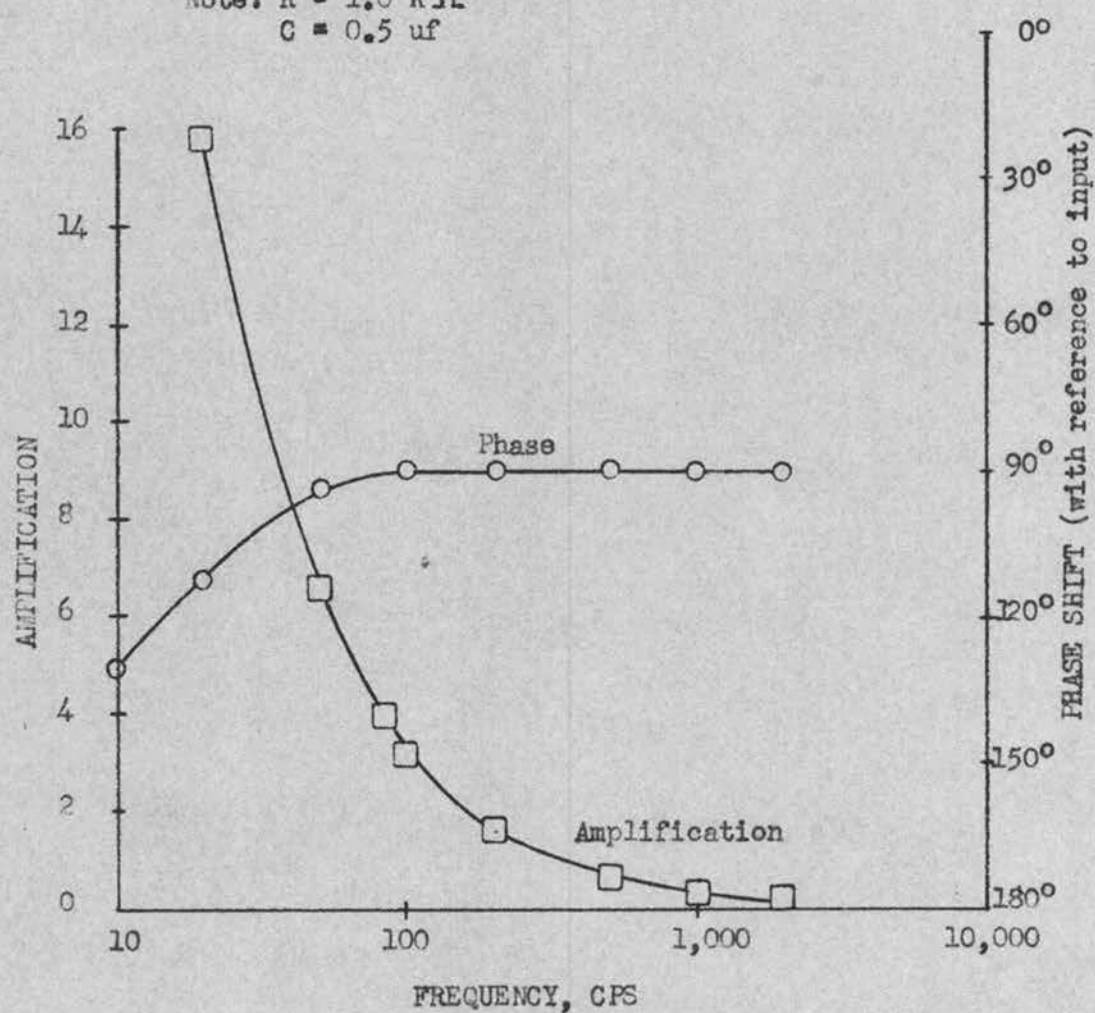
Note: Indicated Units ..
   All resistors in kilo-ohms
   All capacitors in micro-farads
   All inductors in milli-henries

107-A

APPENDIX II

DEVIATION AND ILLUSTRATION OF THE ERROR
CHARACTERISTICS OF A NON-IDEAL
OPERATIONAL NETWORK

DEVIATION AND ILLUSTRATION OF THE ERROR CHARACTERISTICS OF
A NON-IDEAL OPERATIONAL NETWORK

The non-ideal dc amplifier can be represented in
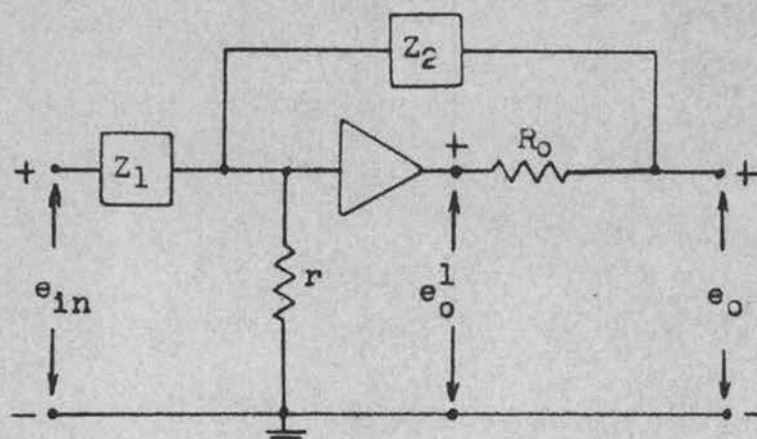terms of the ideal amplifier as shown below.

Figure 42. Equivalent Circuit of the Non-Ideal Amplifier
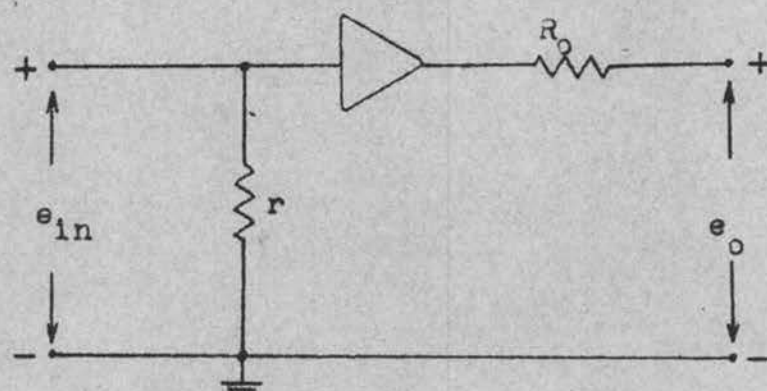
where: r = input impedance
R_O = output impedance

Thus the general operational amplifier network for
a non-ideal operational amplifier is represented as shown
below.

Figure 43. A Non-Ideal Operational Amplifier Network

Now, if we assume a zero source impedance and infinite
load impedance, and equate the sum of currents into the
second summing point to zero, we obtain:

(1) $\left(\dfrac{e_o^1}{A} - e_o^1 \right) \dfrac{1}{R_o + Z_2} + \dfrac{e_o^1}{A} \dfrac{1}{r} + \left(\dfrac{e_o^1}{A} - e_{in} \right) \dfrac{1}{Z_1} = 0$

A rearrangement yields,

(2) $\dfrac{e_o^1}{e_{in}} = \dfrac{1}{\dfrac{Z_1}{R_o + Z_2} + \dfrac{1}{A} \left(\dfrac{Z_1}{r} + \dfrac{Z_1}{R_o + Z_2} + 1 \right)}$

Utilizing the first summing point, we obtain:

(3) $\left(e_o - e_o^1 \right) \dfrac{1}{R_o} + \left(e_o - \dfrac{e_o^1}{A} \right) \dfrac{1}{Z_2} = 0$

(4) $\dfrac{e_o}{e_o^1} = \dfrac{Z_2 + \dfrac{R_o}{A}}{R_o + Z_2}$

Multiplying expressions (2) and (4) yields,

$\dfrac{e_o}{e_{in}} = \dfrac{Z_2 + \dfrac{R_o}{A}}{-Z_1 + \dfrac{1}{A} \left(Z_1 + \dfrac{Z_1 R_o}{r} + \dfrac{Z_1 Z_2}{r} + Z_2 + R_o \right)}$

Now if $\dfrac{R_o}{A Z_2} \ll 1$

(5) $\dfrac{e_o}{e_{in}}$

$$= \dfrac{Z_2}{-Z_1 + \dfrac{1}{A}(Z_1 + \dfrac{Z_1 R_o}{r} + \dfrac{Z_1 Z_2}{r} + Z_2 + R_o + \dfrac{R_o Z_1}{Z_2}) - \dfrac{1}{A^2}(\dfrac{R_o Z_1}{Z_2} + \dfrac{Z_1 R_o^2}{r Z_2} + \dfrac{z_1 r_o}{r_2} + R_o + \dfrac{R_o^2}{Z_2})}$$

And neglecting the term in $\dfrac{1}{A^2}$,

(6) $\dfrac{e_o}{e_{in}} = \dfrac{Z_2}{-Z_1 + \dfrac{1}{A}(Z_1 + \dfrac{Z_1 R_o}{r} + \dfrac{Z_1 Z_2}{r} + R_o + Z_2 + \dfrac{R_o Z_1}{Z_2})}$

Now if $\dfrac{1}{A Z_1}(Z_1 + \dfrac{Z_1 R_o}{r} + \dfrac{Z_1 Z_2}{r} + R_o + Z_2 + \dfrac{R_o Z_1}{Z_2}) << 1$

(7) $\dfrac{e_o}{e_{in}} = -\dfrac{Z_2}{Z_1}\left[1 + \dfrac{1}{A}(1 + \dfrac{R_o}{r} + \dfrac{Z_2}{r} + \dfrac{R_o}{Z_1} + \dfrac{Z_2}{Z_1} + \dfrac{R_o}{Z_2})\right]$

The error term is easily recognized as

(8) error $= \boldsymbol{6} = \dfrac{1}{A}(1 + \dfrac{R_o}{r} + \dfrac{Z_2}{r} + \dfrac{R_o}{Z_1} + \dfrac{Z_2}{Z_1} + \dfrac{R_o}{Z_2})$

Solving for Z_1 we obtain

(9) $Z_1 = \dfrac{-Z_2 r (Z_2 + R_o)}{Z_2^2 + Z_2(R + r - A\boldsymbol{6}r) + Rr}$

Now if we desire the error limiting values of Z_2 and Z_1, they can be found from the equation:

$$(10) \qquad Z_1 = \frac{-Z_2 \, r \, (\, Z_2 + R_o \,)}{Z_2^2 + Z_2 \, (\, R_o + r - A \, \epsilon \, r \,) + Rr}$$

For the specific case of:
$$A = 25,000$$
$$r = 2,000$$
$$R_o = 1,000$$

$\epsilon =$ 10%		$\epsilon =$ 0.1%		$\epsilon =$ 0.1%	
Z_2, Ω	Z_1, Ω	Z_2, Ω	Z_1, Ω	Z_2, Ω	Z_1, Ω
0.4	-	4	-	40	-
1	1	10	6.67	100	70
1 K	0.8	1 K	8.0	1 K	85
10 K	4.4	10 K	45.0	10 K	550
100 K	40.8	100 K	500	50 K	-
1 M	500	500 K	-		
5 M	-				

$$\epsilon = \text{error}$$

This plot is approximated on the following page.

Figure 44, ERROR LIMITING VALUES OF Z_1 AND Z_2 FOR THE NON-IDEAL OPERATIONAL AMPLIFIER.

Note: $A = 25,000$
$r = 2,000$ ohms
$R_0 = 1,000$ ohms
$\delta = error$

$\delta = 0.1\%$ $\delta = 1\%$ $\delta = 10\%$

Z_1, OHMS

Z_2, OHMS
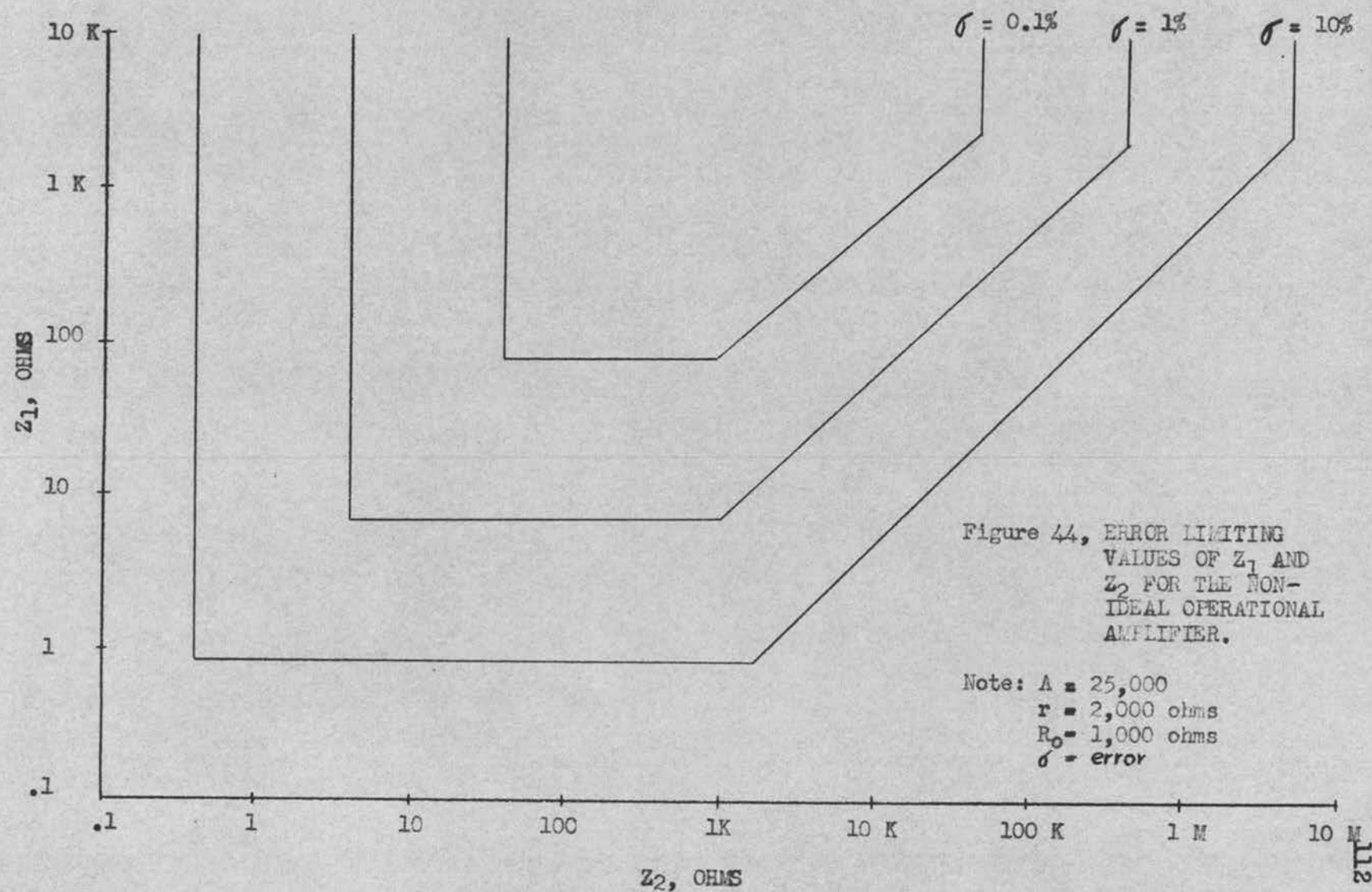
APPENDIX III

DERIVATION OF INTEGRATING OPERATIONAL AMPLIFIER NETWORK ERROR RELATIONSHIP
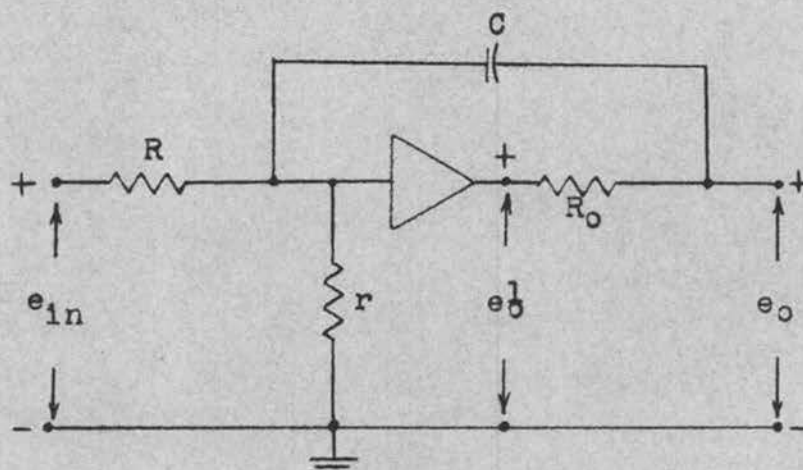
DERIVATION OF INTEGRATING OPERATIONAL AMPLIFIER NETWORK ERROR RELATIONSHIP

Proceding as in Appendix II,

Figure 45. A Non-Ideal Operational Amplifier, Integrator Network

Assumptions: 1. Zero source impedance
2. Infinite load impedance

In terms of the Laplace operator S, the current summation around the second node yields,

$$(1) \quad \left(\frac{e_o^1}{A} - e_o^1 \right) \frac{1}{R_o + \frac{1}{cs}} + \left(\frac{e_o^1}{A} - e_{in} \right) \frac{1}{R} + \frac{e_o^1}{A} \frac{1}{r} = 0$$

Rearrangement yields,

$$(2) \quad \frac{e_o^1}{e_{in}} = \cfrac{1}{\cfrac{-RCS}{R_o CS + 1} + \cfrac{1}{A} \left(\cfrac{RCS}{R_o CS + 1} + \cfrac{R}{r} + 1 \right)}$$

Summing the currents about the first node yields

(3) $\quad (e_o - e_o^1) \dfrac{1}{R_o} + (e_o - \dfrac{e_o^1}{A})\ C\,S = 0$

(4) $\quad \dfrac{e_o}{e_o^1} = \dfrac{1 + \dfrac{1}{A}(\,R_o\,C\,S\,)}{R_o\,C\,S + 1}$

Combining the expressions (2) and (4) gives

(5) $\quad \dfrac{e_o}{e_{in}} = \dfrac{1 + \dfrac{1}{A}(\,R_o\,CS\,)}{-RCS + \dfrac{1}{A}\left[\,RCS + R_o CS + SC\,\dfrac{R\,R_o}{r} + \dfrac{R}{r} + 1\right]}$

If $\dfrac{1}{A}(\,R_o CS\,) \ll 1$, and we neglect terms involving $\dfrac{1}{A^2}$,

(6) $\dfrac{e_o}{e_{in}} = \dfrac{1}{-RCS + \dfrac{1}{A}\left[(RCS)(R_o CS) + RCS + R_o CS + \dfrac{RR_o}{r}CS + \dfrac{R}{r} + 1\right]}$

and, again if $\dfrac{1}{ARCS}\left[(RCS)(R_o CS) + RCS + R_o CS + \dfrac{RR_o}{r}CS + \dfrac{R}{r} + 1\right] \ll 1$

(7) $\dfrac{e_o}{e_{in}} = -\dfrac{1}{RCS}\left[1 + \dfrac{1}{A}(R_o CS + 1 + \dfrac{2\,R_o}{R} + \dfrac{1}{rCS} + \dfrac{1}{RCS})\right]$

$\qquad = -\dfrac{1}{RCS}\left[1 + \dfrac{1}{A}(\dfrac{1}{RCS} + \dfrac{1}{rCS} + R_o CS + \dfrac{2R_o}{R} + 1)\right]$

APPENDIX IV

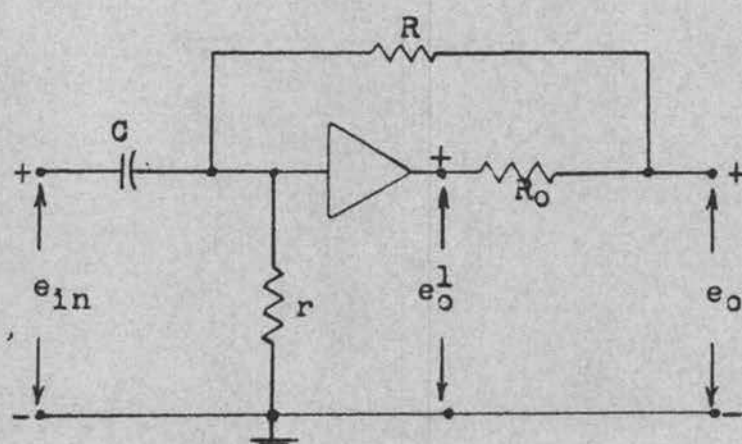### DEVIATION OF DIFFERENTIATING OPERATIONAL
AMPLIFIER NETWORK ERROR
RELATIONSHIP

DEVIATION OF DIFFERENTIATING OPERATIONAL AMPLIFIER NETWORK ERROR RELATIONSHIP

Proceding as in Appendix I,

Figure 46. A Non-Ideal Operational Amplifier Differentiating Network

Assumptions: 1. Zero source impedance
2. Infinite load impedance

In terms of the Laplace operator S, the current summation around the second node yields,

$$(1) \quad \left(\frac{e_o^1}{A} - e_o^1 \right) \frac{1}{R + R_o} + \frac{e_o^1}{A} \left(\frac{1}{r} \right) + \left(\frac{e_o^1}{A} - e_{in} \right) CS = 0$$

$$(2) \quad \frac{e_o^1}{e_{in}} = \frac{C\,S}{-\frac{1}{R + R_o} + \frac{1}{A} \left(\frac{1}{r} + \frac{1}{R + R_o} \right)}$$

The summation of currents about the first node yields,

$$(3) \quad (e_o - e_o^1) \, \frac{1}{R_o} + (e_o - \frac{e_o^1}{A}) \, \frac{1}{R} = 0$$

$$(4) \quad \frac{e_o}{e_o^1} = \frac{R - \frac{R_o}{A}}{R + R_o}$$

Combining expression (2) and (4), yields

$$(5) \quad \frac{e_o}{e_{in}} = \frac{(R - \frac{R_o}{A}) \, C \, S}{-1 + \frac{1}{A} \left[1 + \frac{R}{r} + \frac{R_o}{r} \right]}$$

Now if $\frac{1}{A} (1 + \frac{R}{r} + \frac{R_o}{r}) \ll 1$,

$$(6) \quad \frac{e_o}{e_{in}} = - \left[RCS - \frac{R_o}{A} CS \right] \left[1 + \frac{1}{A} (1 + \frac{R}{r} + \frac{R_o}{r}) \right]$$

Combining terms and neglecting the term involving $\frac{1}{A^2}$,

$$(7) \quad \frac{e_o}{e_{in}} = - RCS \left[1 + \frac{1}{A} (R_o CS + \frac{R}{r} + \frac{R_o}{r} + 1) \right]$$