AN ABSTRACT OF THE THESIS OF

Triet T. Le for the degree of Doctor of Philosophy in

Electrical and Computer Engineering presented on February 19, 2008.

Title: Efficient Power Conversion Interface Circuits for Energy Harvesting
Applications

Abstract approved:

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Harvesting energy from the environment for powering micro-power devices
have been increasing in popularity. These types of devices can be used in embed-
ded applications or in sensor networks where battery replacement is impractical.
In this dissertation, different methods of energy harvesting from the environment
are explored as alternative sources of energy for devices. Some of the most pop-
ular energy extraction used in electronic devices today are radio frequency (RF)
and thermal/vibrational energy extraction. This dissertation presents novel power
techniques that enable some of the most efficient power conversion circuits pub-
lished to date.

New power conversion circuits to interface to a piezoelectric micro-power
generator that produces electrical energy from temperature differences have been
fabricated and tested. Circuit designs and measurement results are presented for
a half-wave synchronous rectifier with voltage doubler, a full-wave synchronous
rectifier and a passive full-wave rectifier circuit. The active rectifier based on

synchronous rectification, fabricated in a 0.25-μm CMOS process, is 86% efficient with 22-μW peak output power when connected to the piezoelectric micro-power generator. This gives the highest efficiency to date for active rectification circuits at the micro-power level. The passive rectifier circuit is 66% efficient with 16-μW peak output power and requires no quiescent current to operate.

RF-powered devices are typically inductively coupled and extract their energy from the near field while operating within a few inches of the radiating source. Longer operating distances, exceeding 10 meters, are desired for a broader set of applications including distributed sensor networks. This dissertation describes an efficient method for far field power extraction from RF energy to enable long-distance passively powered sensor networks.

Passive rectifier circuits are designed in the TSMC 0.25μm mixed-signal CMOS process and antennas for the system are printed on a 4-layer FR4 board. A high-Q resonator is used with a matching network to passively amplify the input voltage to the rectifier. At the circuit level, floating gate transistors are used as rectifying diodes to reduce the diode threshold loss in voltage rectification and therefore increase the rectifier efficiency. A 36-stage rectifier fabricated in a 0.25-μm CMOS process attains an efficiency of over 60% in the far field with a received power sensitivity of 5.5μW (-22.6 dBm), corresponding to an operating distance of 44 meters. The effective threshold voltage of the floating-gate diode is reduced to 36 mV. This is the highest performance for far-field RF energy conversion reported to date.

In ultra-low energy system, such as sensor networks, it is essential that power management circuitry are designed to dissipate very low quiescent power. RF energy and power management circuits are designed in a 0.18μm CMOS process. Voltage regulators are designed to operate at high input voltage and low

power in a standard CMOS process. The voltage regulators can withstand input voltages up to 12 volts and dissipates from 90 nW to 1.4 μW of power. A floating-gate programming circuit is designed with a self-wakeup timer that turns itself on about once a month. The floating-gate programming circuits dissipates about 30 nW in sleep mode and 8 μW in active mode.

Efficient Power Conversion Interface Circuits for Energy Harvesting Applications

by

Triet T. Le

A THESIS

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Doctor of Philosophy

Presented February 19, 2008
Commencement June 2008

Doctor of Philosophy thesis of <u>Triet T. Le</u> presented on <u>February 19, 2008</u>

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ACKNOWLEDGMENT

and figures that I included in this thesis. Thanks **Hector** and **Farhad** for keeping me in good physical shape and for not letting me take it easy in the gym. To all of my other lab mates in KEC 3040, thanks for all the help you have given, everything you did for me are gratefully appreciated.

I would like to thank all of my friends from my earlier years of graduate school. Thanks all for being my companions throughout my first two years. Together, we survived through all the course work and exams.

In addition, I would like to thank everyone at Living Water Baptist Church for their support in providing me comfort throughout the difficult times in my life.

I would also like to thank everyone in my family for their support throughout my years in college. I thank my aunt and uncle, **Dao Le** and **Hoa Nguyen** as well as my parents, **Hanh** and **Cam Le** for providing me a home on weekends and breaks. I thank them for the sacrifice they made raising me from childbirth to adulthood. I thank all my brothers and sisters for their financial as well as emotional support in my 10-or-so years of college.

A special thanks go to **Hue Le**, my wife for her love and support. For believing in me, caring for me, and for keeping me healthy. Without her I would not be as healthy or motivated as I am today.

And most of all, I thank **GOD**, my Lord and Savior for his guidance in every aspect of my life. I believe "I can do everything through him who gives me strength."

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1. INTRODUCTION

1.1. Motivation

In recent years, there has been an increasing need for power conversion circuits for power and energy harvesting applications. Energy harvesting methods such as RF powered systems [1, 2], solar powered systems [3, 4], wind powered systems, motional energy harvesting systems [5, 6], thermoelectric powered systems [7, 8], and piezoelectric conversion systems [9, 32] can be used to harvest energy from a controlled or ambient environment, to power devices directly or store the energy in capacitors or batteries for later use. These harvesting methods support a wide range of applications and can also be used to increase the lifetime of pre-existing devices. The advantages of energy harvesting applications are that they reduce or eliminate the dependency of devices on batteries and power sources while prolonging their lifetimes or the time between charging of wireless devices. Energy harvesting approaches are mostly used in micro-power applications such as sensor nodes in a distributed sensor network, biomedical implants and radio frequency identification (RFID) [11]. These systems are often very small in size and require little power to operate.

This dissertation covers energy harvesting power interface circuits, used to directly power devices and also charge storage devices such as batteries and capacitors. A general block diagram of a power harvesting system is shown in Figure 1.1.

For a general energy harvesting system, there must be a transducer that harvests energy and converts it into electrical power [12]. The transducer can be
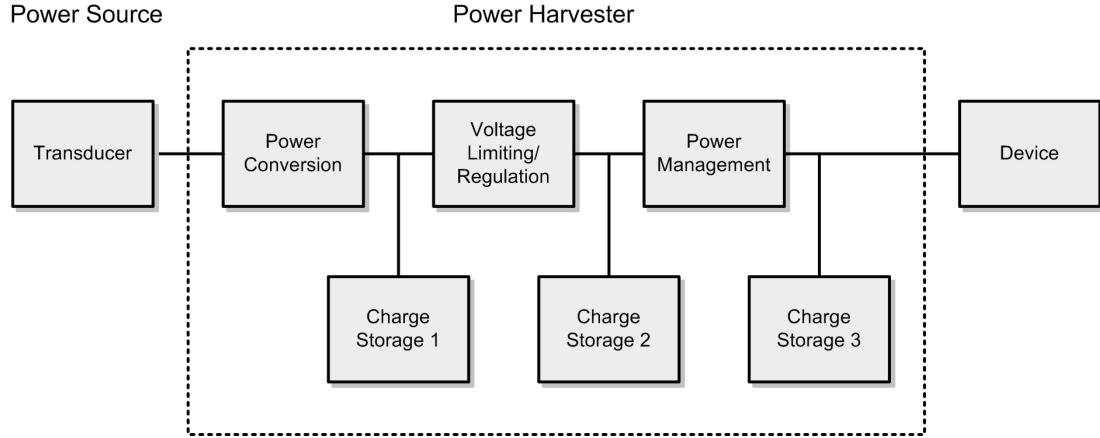
FIGURE 1.1. General block diagram of an energy harvesting system.

an antenna, a piezoelectric device, a solar cell, a fuel cell, a wind turbine, and many other forms. The electrical power available at the output of the transducer can be in the form of direct (DC) or alternating current (AC) and can vary depending on the mode of energy harvesting. A power conversion interface circuit is required to convert the energy to a usable form for storage or it may pass to a voltage regulation circuit.

The power conversion circuit may be in the form of a rectfier or a DC-DC voltage converter. For certain power conversion interface circuits, impedance matching or maximum power tracking is required to ensure maximum power transfer between the power source and power harvester. Charge Storage 1 is the charge storage device to hold the charge harvested through the power conversion interface circuit. The charge storage device in this case can be a capacitor, a battery or any other charge storage element.

Depending on the application and voltage available at the power conversion circuit, a buck or boost converter is used to regulate the voltage from the output of the power conversion circuit to a stable DC voltage. In some cases, voltage limiting is done instead of a voltage regulator. Charge Storage 2 stores the charge that is delivered by the output of the voltage regulator or voltage limiter. The power management circuit controls the conduction path between the device and energy harvester. Charge storage 3 is used to stabilize the voltage at the device during operation.

1.2. Comparison of Energy Harvesting Methods

The following section presents a summary of different energy harvesting methods comparing the range of harvestable energy under various environmental conditions. Radio frequency, piezoelectric, solar, thermoelectric, vibrational, electrostatic and acoustic energy harvesting methods are studied and compared.

1.2.1. Radio Frequency Energy Harvesting

Other than direct wiring, the most common method of distributing power to embedded electronics is through the use of radio frequency (RF) radiation [1, 5]. RF power harvesting is most often used in RFID or passive RF tags to replace the bar code as a new form of data collection. Passive RFID tags are typically used in a very short range of less than 3 meters. RF powered devices are also used in applications such as structure monitoring where the RF powered devices are embedded into a structure making battery replacement impossible without destroying the structure. Some applications employing RF powered devices re-

quire deployment of these devices in very large numbers thus, making individual node battery replacement impractical [13–15]. In RF energy harvesting, the RF harvester can harvest energy from propagating RF waves which can be ambient RF waves generated by nearby electronic components such as cellular phones, or generated from a dedicated RF power source.

For RF power harvesting, the power that can be transmitted by an RF power source is limited by FCC regulations [16]. The power that can be harvested at the harvester is a strong function of the distance of the harvester from the power source. In free space, the path loss of the RF signal is given by Friis' equation [17] as

$$L_P = \left(\frac{4\pi R}{\lambda} \right)^2 \tag{1.1}$$

where R is the distance between the power source and power harvester, and λ is the wavelength of the RF signal transmitted from the power source. Figure 1.2 shows the freespace pathloss of RF signal transmission in ultra-high frequencies (UHF). The pathloss for RF signal transmission exceeds 50 dB at a frequency of 900 MHz and 60 dB for 2.4 GHz at a distance of 10 meters. Figure 1.3 shows the maximum power that can be received according to FCC regulations as a function of distance from a single RF power source [16]. For a freespace distance of 40 meters, the maximum theoretical power available power for conversion is 7.0 μW and 1.0 μW for frequencies of 900 MHz and 2.4 GHz, respectively.

In different environments, the pathloss of the radiated signal behaves differently than it would behave in freespace. With multipath fading and destructive signal collisions, the propagational signal loss from the power source to the harvester increases. Using a simplified pathloss model for a typical office building or a 1-story warehouse [18, 19], the pathloss and received power at the energy har-
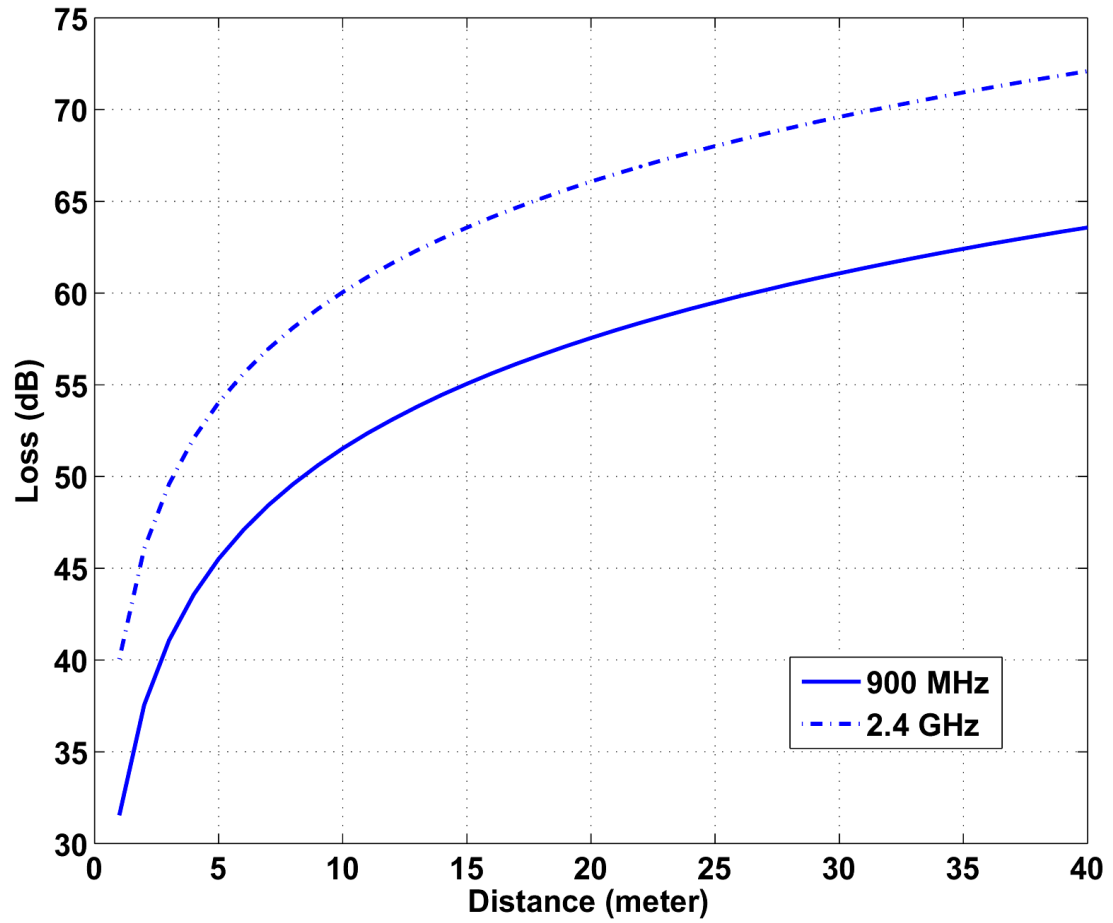
FIGURE 1.2. Path loss of RF signal transmission at UHF.
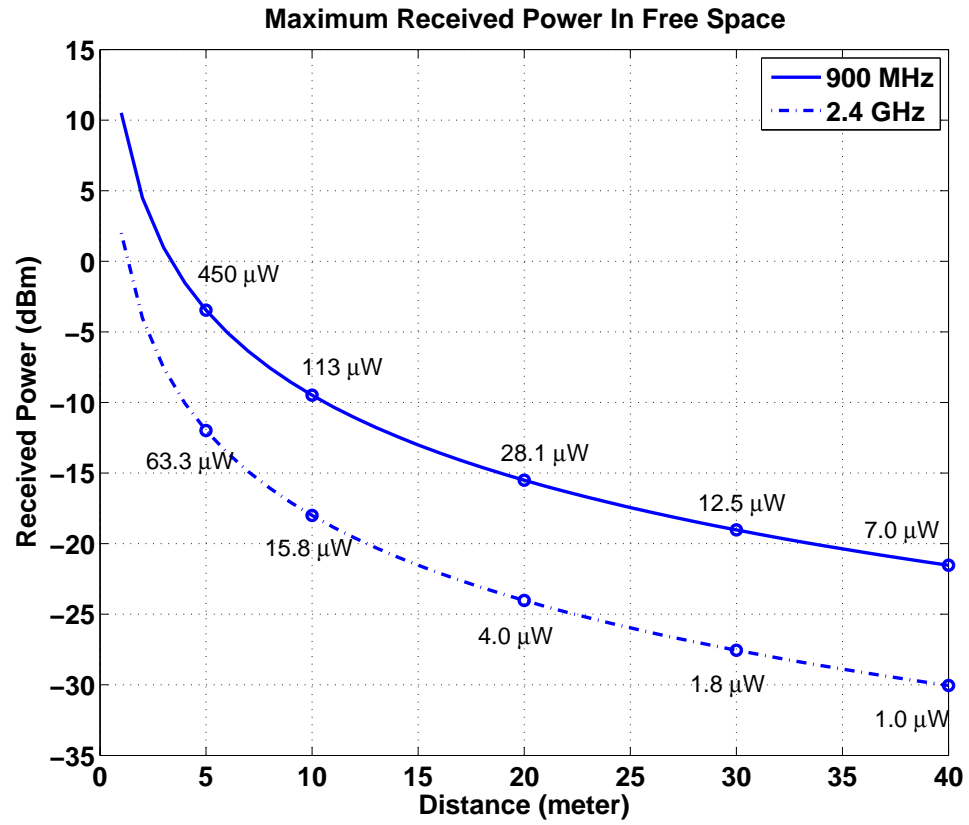
FIGURE 1.3. Maximum allowable receive power versus distance according to FCC regulations for RF energy harvesters from a single RF power source.

vester can be calculated. Figure 1.4 shows the path loss of an RF signal at UHF with the path loss model derived from [19]. The path loss for a 900 MHz signal reaches approximately 60 dB for a distance of 10 meters while exceeding 70 dB for a 2.4 GHz signal at the same distance. Figure 1.5 shows the maximum received power allowed by FCC regulations [16] from a single RF power source at UHF with the pathloss model of an office environment [18, 19]. The received power of 10 μW is achievable at 8 meters in an office environment for a transmitted signal at 900 MHz and 3 meters for a transmitted signal at 2.4 GHz. With this high propagational loss, RF power harvesting is best designed for a short range system or a system with highly efficient power conversion and storage.

1.2.2. Piezoelectric Energy Harvesting

One of the most widely used power harvesting techniques for micro-power operation uses piezoelectric materials to convert mechanical energy from any type of vibration and heat to electrical energy. Also, when an electrical voltage is applied across the piezoelectric materials, the inverse happens and electrical power is converted into mechanical vibration. Due to these bi-directional effects, piezoelectric materials are widely used for making sensors and actuators. Piezoelectric materials are also used to generate electrical power to operate electrical devices from the striking of heels of shoes by walking or running [20, 21].

The piezoelectric effect is one of several ways to convert vibrational energy to electrical power [5]. Piezoelectric power harvesting capitalizes on certain crystal or ceramic materials to generate an electrical potential in response to an applied mechanical stress [22]. One of the most commonly used piezoelectric materials is Lead Zirconate Titanate, more commonly known as PZT. To excite the piezo-
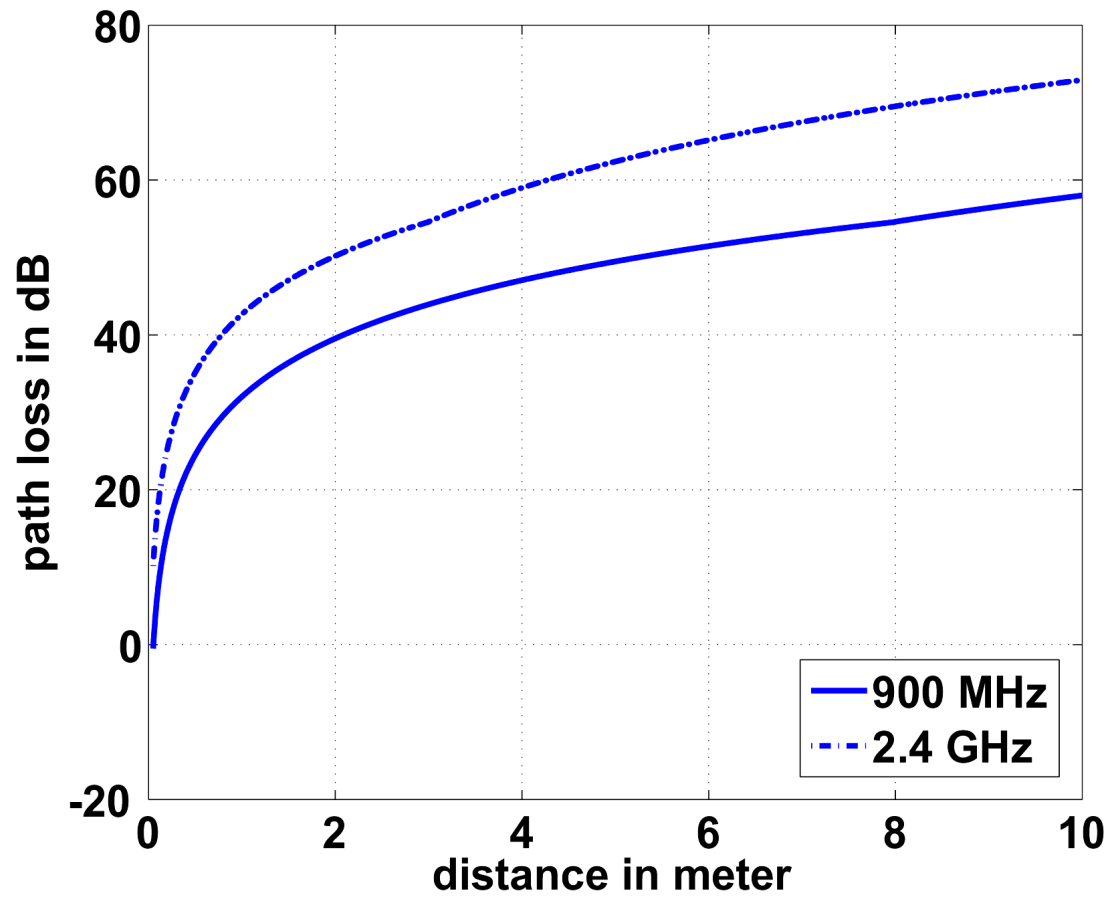
FIGURE 1.4. Path loss of RF signal transmission in UHF with pathloss model derived from [18, 19].
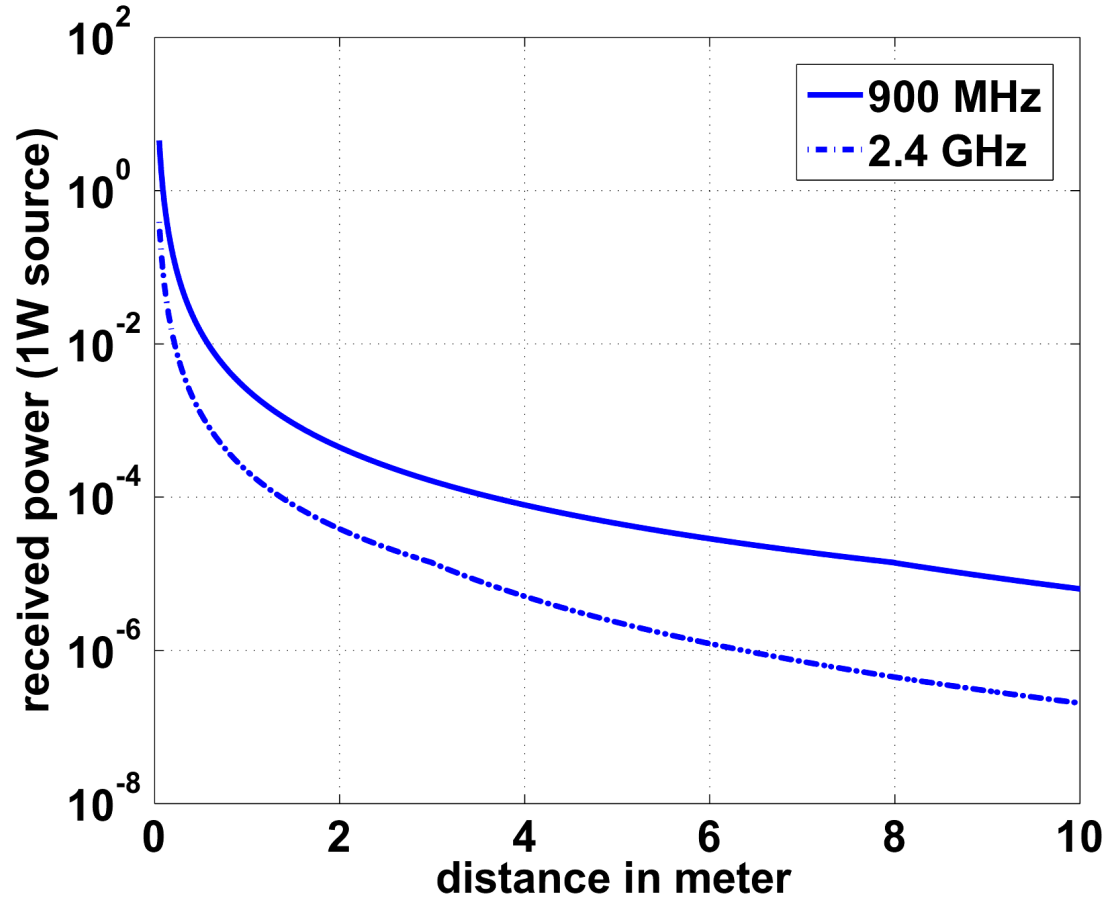
FIGURE 1.5. Maximum allowed receive power versus distance according to FCC regulations for RF power harvesters from a single RF power source, with pathloss model derived from [18, 19].

electric membrane, an alternating pressure can be applied or a proof mass can be placed on the end of the cantilever to enhance vibration on the piezeelectric material. Figure 1.6 shows the mechanical setup of a piezoelectric generator with a cantilever and proof mass. The power generated from this system is proportional to the proof mass, to the square of acceleration, and inversely proportional to the resonant and excitation frequency [23].
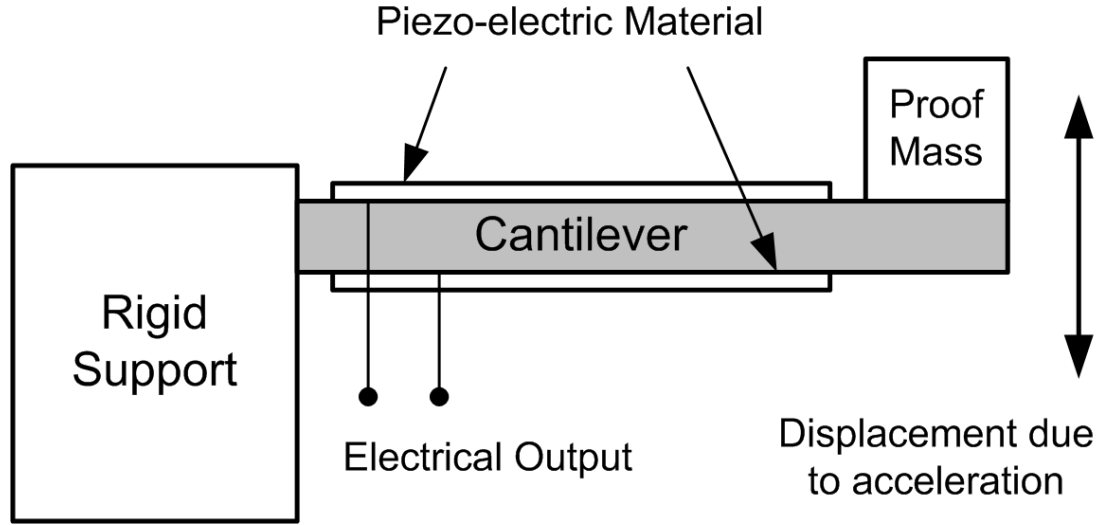
FIGURE 1.6. Diagram of piezoelectric power generator [24].

Figure 1.7 shows the power density from vibrational energy at different frequencies and amplitudes of input vibration. A power density of 10 mW/cm³ is possible at an acceleration of 10 m/s² and an excitation frequency of 50 Hz. At a lower excitation frequency and higher acceleration, the power density can be improved significantly. However, in an ambient environment both the amplitude and frequency of vibration is very low, hence typical power that can be extracted from the ambient environment is about 40 μW.
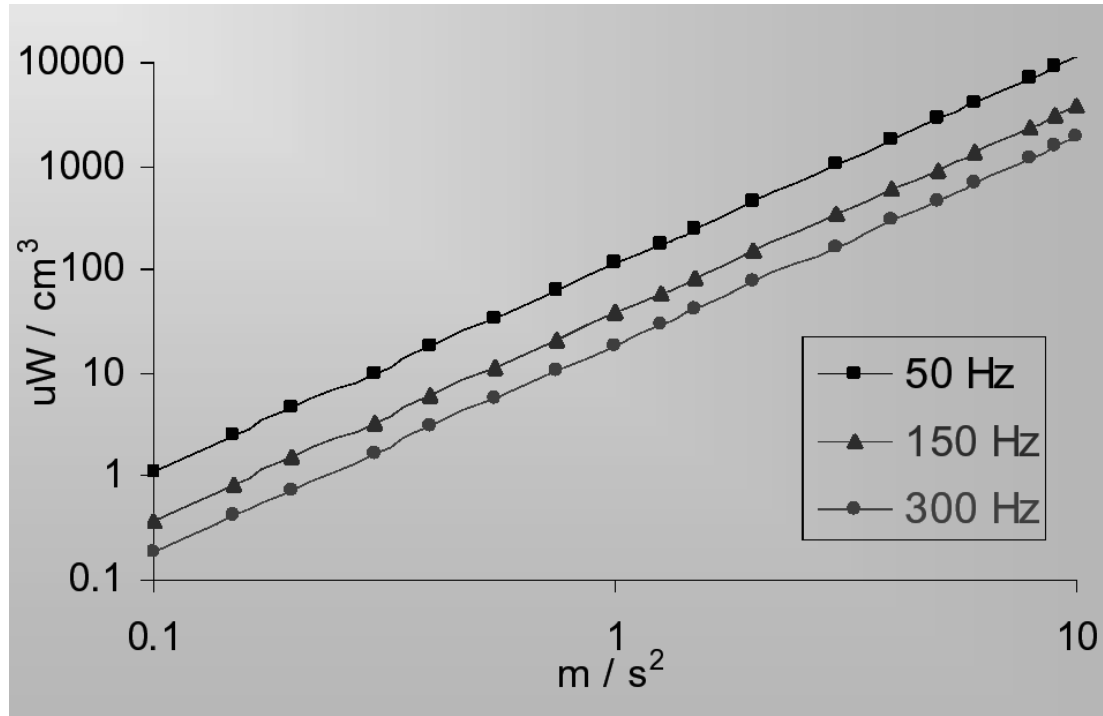
FIGURE 1.7. Power density of piezoelectric power generator at different frequency and amplitude of input vibration [24].

1.2.3. Solar Energy Harvesting

Solar energy harvesting is another method to extract power from the environment to power devices. Solar energy is available when there is direct light. Solar powered devices are used in applications where battery replacement is impractical. Solar power harvesters convert sun light to electrical power via the photovoltaic effect or by heating of fluid to create steam that can be converted to electrical power. Defined as full sun light, the solar power density at the equator at noon on the equinox is 1000 W/m^2 or equivalently 100 mW/cm^2 [25]. In the United States, the average solar power density throughout the year is approximately 25 mW/cm^2. Typical single junction solar cells have an efficiency of 14-19% in production [26] and 30-34% in research. Multi-junction solar cells have achieved an efficiency of over 42% but are relatively more expensive to mass produce [27].

Experimental results shows that the I-V characteristics as well as the maximum power point of solar cells are a function of light intensity and temperature. Figure 1.8 shows the simulated I-V characteristics of a typical 1-W solar cell for different lighting conditions and standard test temperature (25°C). The dimension of the solar cell is about 3 x 3 inches, which translates to a solar cell efficiency of about 17%. From the I-V curves, the short circuit current of the solar cell varies directly with light intensity while the open circuit voltage does not vary greatly with light intensity. In Figure 1.9, the output power curves for the same 1-W solar cell with the maximum power points are shown. From the plot, the maximum power point current varies significantly with light intensity while the maximum power point voltage varies only slightly.
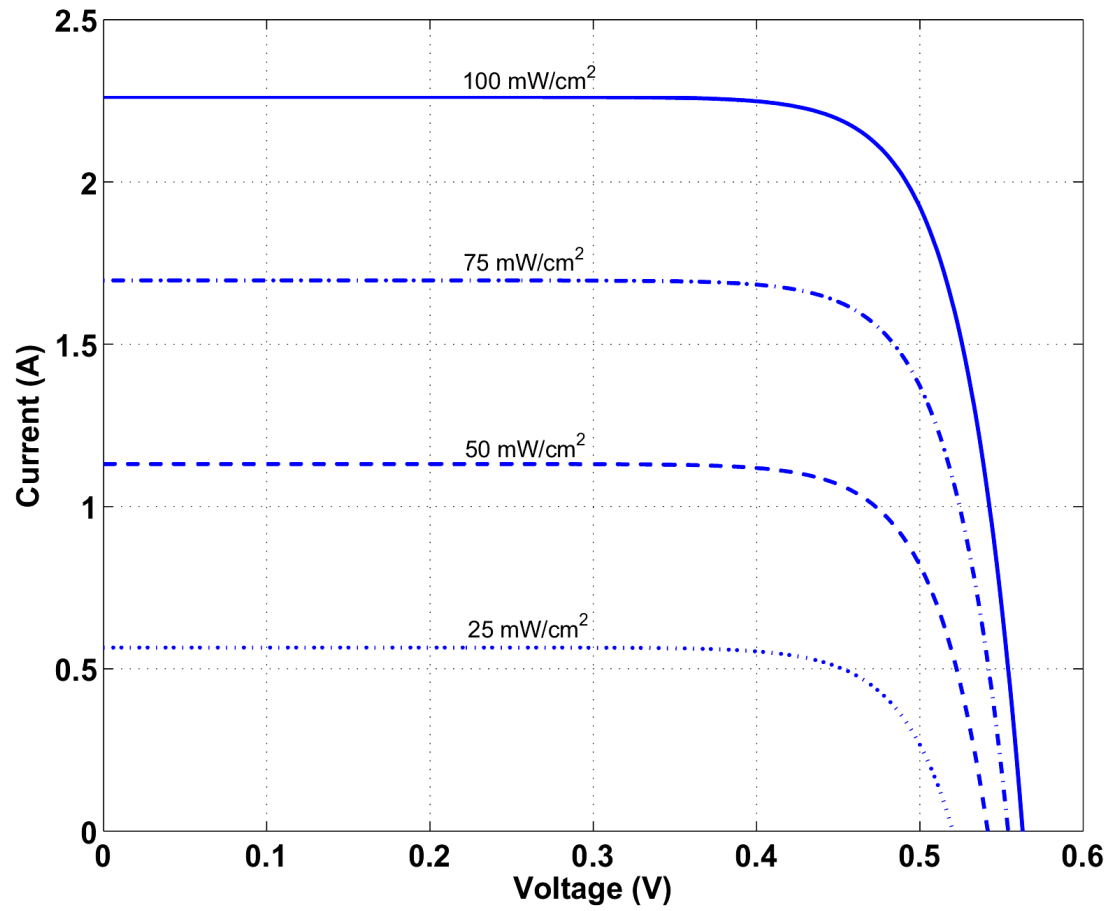
FIGURE 1.8. I-V characteristics of a typical 1-W solar cell for different lighting conditions (at 25°C).
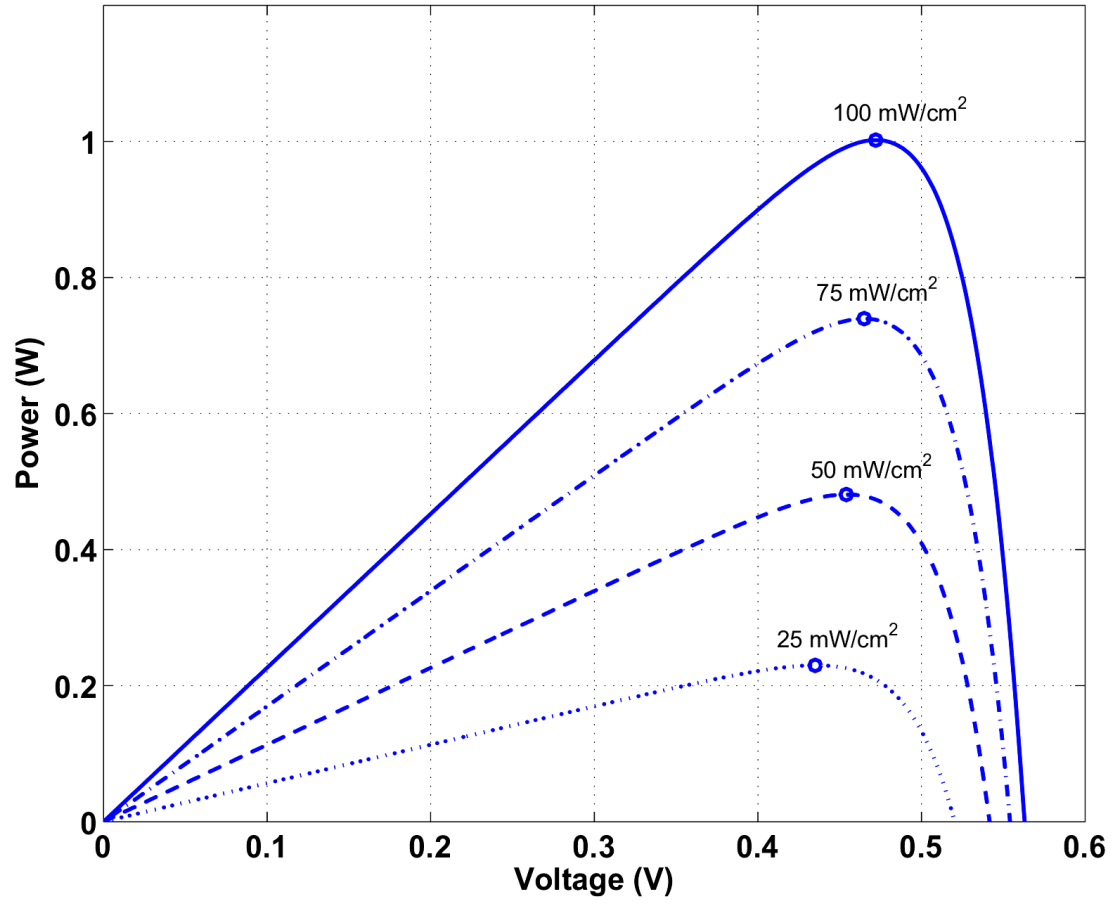
FIGURE 1.9. Output power of a typical 1-W solar cell for different lighting conditions (at 25°C).

Figure 1.10 shows the I-V characteristics of a typical 1-W solar cell at different temperatures for standard lighting conditions ($100\,\mathrm{mW/cm^2}$). From the I-V curves, the short circuit current of the solar cell varies only slightly while the open circuit voltage varies greatly. Figure 1.11 shows the output power curves for the same 1-W solar cell with the maximum power point marked. From the plot, both the maximum power point current and voltage vary directly with temperature. From these plots, it can be observed that the short circuit current and maximum power point current of the solar cell is strongly affected by light intensity, while the open circuit voltage and maximum power point voltage is more dependent o the temperature. With these variations in voltage and current from temperature and lighting conditions, the solar power conversion system requires a maximum power tracking circuit to ensure maximum power transfer between the solar cell and the load.

1.2.4. Thermo Electric Energy Harvesting

Energy can be extracted from the thermal temperature difference between two junctions to generate a small amount of electricity [28]. The thermoelectric effect uses the thermal gradient between two dissimilar metal conductors to produce an electrical voltage from diffusion current caused by the heat flow across the dissimilar conductors. The thermoelectric effect is reversable so when an electrical voltage is applied at the conductors, a temperature gradient is created across it. The term thermoelectric effect comprises of the Seebeck effect, the Peltier effect and the Thompson effect of thermoelectricity. Products that utilize thermoelectric energy harvesting includes twist watches that run from the temperature gradient generated between the human body and the ambient environment.
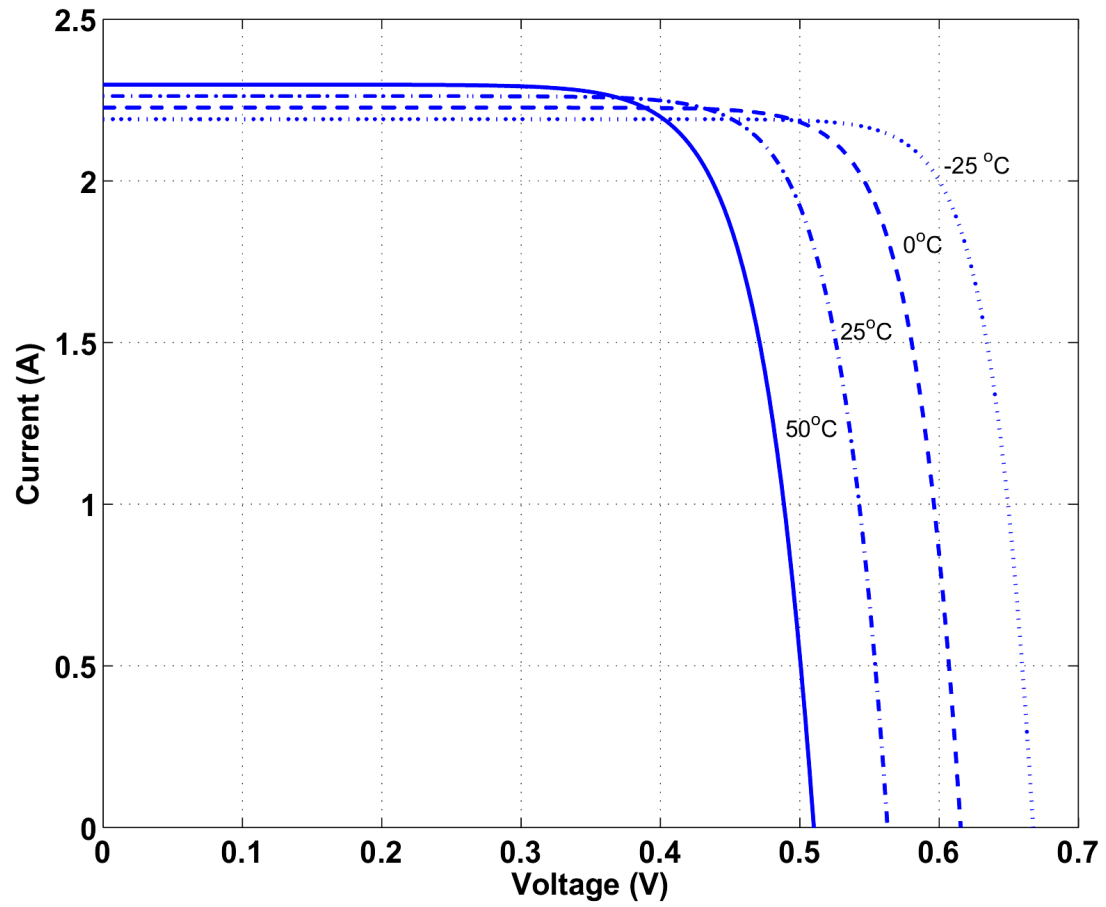
FIGURE 1.10. I-V characteristics of a typical 1-W solar cell at different temperatures (at 100 mW/cm^2).
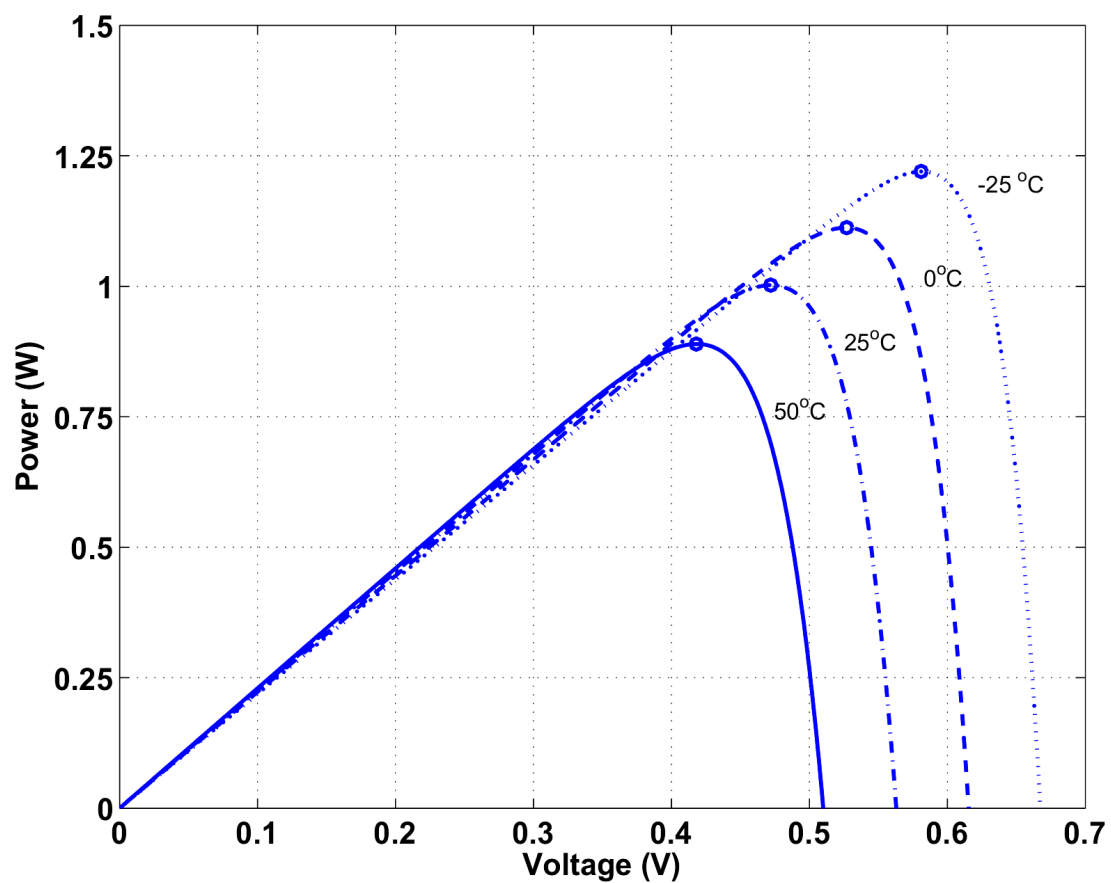
FIGURE 1.11. Output power of a typical 1-W solar cell at different temperatures (at 100 mW/cm²).

Micro-thermoelectric generator have demonstrated the capability of generating a power density of 15 μW/cm^3 from a thermal gradient of 10 °C [28]. In recent years, the thin-film thermoelectric technology has improved to enhance the power density of thermoelectric generators. By employing nanoscale thermoelectric materials using superlattices and self-assembled quantum dots, the power density of thermoelectric generators can be increased to over 100 μW/cm^3 with an thermal gradient of 1°C [29] once this technology is fully developed. These thermoelectric generators are designed to generate power in the 100 mW range from the heat produced by microprocessors or other integrated circuits that dissipate from 10-20 W of power.

1.2.5. Vibrational Energy Harvesting

Other than the piezoelectric effect, other methods to extract power from vibration includes the electrostatic effect (capacitive) or electromagnetic effect (inductive) of vibrational energy conversion. Vibrational energy conversion can be powered from sources such as the human body or powered from machinery. For capacitive vibrational energy harvesting, the capacitance of a varactor are is by the vibration to convert mechanical energy into electrical energy. In inductive vibrational energy harvesting, a coil vibrates through a magnetic field to yield an electrical current.

Typical motional power that can be extracted from human caused vibration is in the microwatt range for very cubic centimeter (cc) while typical harvestable power excited by machinery can be in the hundreds of microwatts for every cubic centimeter. Vibrational energy harvesting is used for applications such as wrist watches and heel strikes for shoes in military applications.

1.2.6. Electrostatic Energy Harvesting

In the case for electrostatic energy harvesting, an electrostatic generator or machine is required to produce the static electric effect. Similar to static electricity, the electrostatic generator produces a high voltage and low current by means of inducing friction.

In electrostatic generators, electrical charge can be accumulated by using electrostatic induction or friction. An electrostatic generator can consist of two conductors that generate charge of opposite sign or of moving gears that generate a steady stream of static electricity. Electrostatic machines are often seen in science classrooms to safely demonstrate the effect of electrostatic electricity. The voltage generated from static electricity can reach up to 1,000,000 volts with modern electrostatic generators, however, its current is very low. Another disadvantage of electrostatic power generators is the size of the generator as they are generally much larger than any types of transducer for other modes of energy harvesting.

1.2.7. Acoustic Energy Harvesting

Energy can also be extracted from sound waves as is the case for acoustic energy harvesting. In acoustic energy harvesting, an acoustic transducer or resonator is used to convert acoustic energy to electrical energy. In general, acoustic power can only be harvested in very noisy environments. A study has been conducted using incident sounds as a source of excitation for piezoelectric materials to power an ultra-low power processing circuit and it was found that the system can only operate at very high noise, i.e., 114 dB [30]. In the ambient environment, energy from acoustic noise is very low, hence energy harvesting from sound wave

is very inefficient. From theorectical results, acoustic energy harvesting can only yield 0.96 μW/cm^3, much lower than other methods of energy harvesting.

1.2.8. Summary of Energy Harvesting Methods

From the summary of different energy harvesting methods, it is clear that energy harvesting by radio frequency and piezoelectric effects are two of the most attractive approaches for low power applications. Table 1.1 shows the power density and energy density of different modes of energy harvesting. The power density for each energy harvesting method is shown for various environmental conditions. The energy density of these methods is also calculated assuming a 10 year lifetime for devices that employ these energy harvesting methods.

The power harvested from the sun has the highest power density in the most ideal situation but drops off as a linear function of light intensity. It can be observed that on a cloudy day or in an office environment, the energy from light is significantly lower compared to other means of energy extraction. Energy harvesting from vibrational, electrostatic and acoustic methods also lacks the power density compared to other methods.

1.3. Dissertation Outline

In this dissertation, efficient power conversion interface circuits for piezoelectric and RF power harvesting systems are presented. One of the challenges in designing a power generator is the design and construction of an efficient rectifier circuit to harvest the energy from the PZT membrane. In Chapter 2, a model for a particular piezoelectric membrane is shown and novel power conversion circuits to interface to a piezoelectric micro-power generator have been fabricated

	Power Density (μW/cm^3)	Energy Density (kJ/cm^3) 10 Year life	Source of Information
RF (900 MHz)	450 @ 5m	142.0	
	113 @ 10m	71.0	
	28 @ 20m	35.5	
	7 @ 40m	17.7	Le, *et al.,* 2006 [14]
RF (2.4 GHz)	63.3 @ 5m	20.0	
	15.8 @ 10m	10.0	
	4.0 @ 20m	5.0	
	1.0 @ 40m	2.5	Le, *et al.,* 2006 [14]
Solar (Outdoors)	15,000 - peak sun	4,730 - peak sun	Commonly
	150 - cloudy day	47.3 - cloudy day	Available
Solar (Indoors)	6 - office desk	1.9 - office desk	Roundy 2003 [5]
Vibrations	200	63.1	Roundy, *et al.,* 2002 [5]
Acoutics	0.003 @ 75 dB	0.0009 @ 75 dB	
	0.96 @ 100 dB	0.30 @ 100 dB	Theory
Thermo-electric			Venkasubramanian,
	100	31.5	*et al.,* 2007 [29]
Shoe Inserts			Stamer 1996 [20]
	330	104	Shenck 2001 [21]

TABLE 1.1. Comparison of energy harvesting methods [5].

and tested. Circuit designs and measurement results are presented for a half-wave synchronous rectifier with a voltage doubler, a full-wave synchronous rectifier and a passive full-wave rectifier circuit connected to the piezoelectric micro-power generator.

In Chapter 3, an RF-DC power conversion system for far-field RF energy extraction is presented. In a far field RF energy harvesting system, RF energy must be extracted from the air at very low power density since the propagation energy drops off rapidly as distance from the source is increased. One of the challenges of designing such a system is the very low available RF power to the receiver in the far-field, and the available voltage for rectification in the RF to DC conversion system falls below the threshold of standard CMOS transistors. Non-conventional rectifier circuits must be designed with threshold reduction techniques to improve the performance of the power conversion system.

The system is designed to efficiently convert far-field RF energy to DC voltages at very low received power and voltages. Passive rectifier circuits are designed in a 0.25μm CMOS technology using floating gate transistors as rectifying diodes. Optimized for far field, the high operating voltage range for the rectifier achieved at low load currents make it ideal for use in passively powered sensor networks.

Chapter 4 presents novel voltage regulators and floating-gate programming circuits designed to enhance the power efficiency of RF energy harvesting systems. Operated in weak-inversion, the voltage regulator circuits are designed to operate at sub-microwatt power. The floating-gate programming circuit is designed to replenish charge to the floating-gate of the rectifier circuit for RF power conversion. The programming of the floating-gate is done periodically to prevent charge from leaking off from the floating-gate and also to optimize the performance of

the floating gate rectifier over time. Measured results and characterization of the voltage regulators and floating-gate programming circuits are shown.

Chapter 5 concludes the dissertation and identifies key research problems for further investigation.

2. PIEZOELECTRIC MICRO-POWER GENERATION INTERFACE CIRCUITS

2.1. Abstract

New power conversion circuits to interface to a piezoelectric micro-power generator have been fabricated and tested. Circuit designs and measurement results are presented for a half-wave synchronous rectifier with voltage doubler, a full-wave synchronous rectifier and a passive full-wave rectifier circuit connected to the piezoelectric micro-power generator. The measured power efficiency of the synchronous rectifier and voltage doubler circuit fabricated in a 0.35-μm CMOS process is 88% and the output power exceeds 2.5-μW with a 100-kΩ, 100-nF load. The two full-wave rectifiers (passive and synchronous) were fabricated in a 0.25-μm CMOS process. The measured peak power efficiency for the passive full-wave rectifier circuit is 66% with a 220-kΩ load and supplies a peak output power of 16-μW with a 68-kΩ load. Although the active full-wave synchronous rectifier requires quiescent current for operation, it has a higher peak efficiency of 86% with a 82-kΩ load, and also exhibits a higher peak power of 22-μW with a 68-kΩ load which is 37% higher than the passive full-wave rectifier.

2.2. Introduction

With the need for portable and lightweight electronic devices on the rise, highly efficient power generation approaches are a necessity. Novel approaches to obtaining power conversion are being explored including the piezoelectric micro power generator [31], high-voltage solar cell arrays [3] and thermal energy conversion [7]. One that is particularly promising uses a piezoelectric material to convert

mechanical energy from heat or vibration into electrical energy. Conversely, applying an electric voltage to this material produces a mechanical strain. Because of these bi-directional effects, piezoelectric materials are widely used for making sensors and actuators.

The use of a thin piezoelectric film/plate for a micro power supply, as shown schematically in Fig. 2.1, is a new and exciting application [31]. In this application, the piezoelectric laminate is mechanically forced to vibrate and thus, it works as a generator to transform the mechanical energy into electrical energy. The piezoelectric material used for this power generation circuit is lead-zirconate-titanate (PZT). The PZT membrane is placed on a silicon substrate between two electrodes. The electrodes are used as conductors to carry the electrical charge from the PZT membrane to the power conversion circuit. The power conversion interface circuit takes the charge across the piezoelectric device and converts this electrical charge into a DC voltage, which can be used to drive a current load. Fig. 2.2 shows the picture of the fabricated PZT with dimension of 2.45 mm x 2.45 mm. The PZT membrane is fabricated on a separate silicon substrate from the power generation interface circuits.

One of the challenges in a power generator of this type is the design and construction of an efficient power conversion circuit to harvest the energy from the PZT membrane. Unlike conventional power supplies and batteries, which typically have very low internal impedance, the piezoelectric generators internal impedance is relatively high. This high internal impedance restricts the amount of output current that can be driven by the PZT source to the micro-amp range. Another unique characteristic of this power source is the relatively low output voltage of the piezoelectric device. This low output voltage makes it challenging
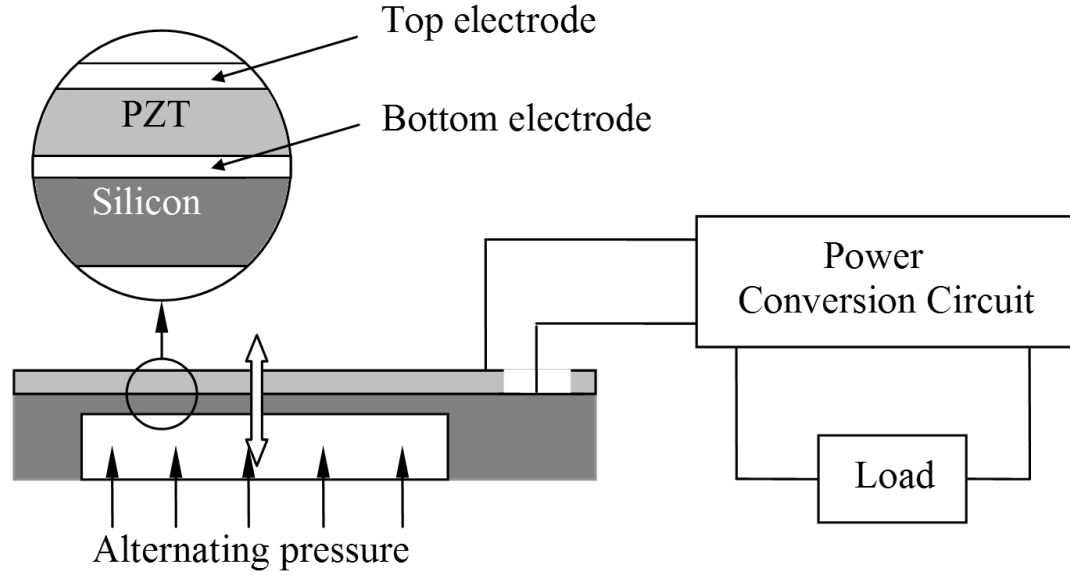
FIGURE 2.1. Schematic of power generation using a piezoelectric laminate.

to develop rectifier circuits that are efficient since many half wave or full wave diode rectifiers require nonzero turn-on voltages to operate.

The above issues are addressed in this paper by presenting several rectifier circuits that are suitable for power conversion with a piezoelectric source. In Section 2.3, typical measured PZT device characteristics are described along with a model that is used for simulation of the power conversion circuits. Section 2.4 presents half-wave rectifier circuits and compares passive and active circuit approaches. Section 2.5 describes the implementation of two full-wave rectifiers that enhance the performance over the half-wave rectifiers. The measured results and comparison of these two implementations are also presented. Section 2.6 concludes the paper.

FIGURE 2.2. Picture of the fabricated PZT.

2.3. Piezoelectric Device Characteristics and Modeling

In order to design a power generation interface circuits, a circuit model of the piezoelectric membrane is needed to simulate the interface circuit. When pulses of pressure are applied to a piezoelectric membrane, the amount of charge across the piezoelectric device as well as the output swing varies in amplitude and depends on the membrane characteristics. A typical measurement of the open circuit output voltage is shown in Fig. 2.3 [32, 33]. In this case, the output voltage ranges from -0.85 V to 1.7 V. When experiencing the most change in pressure, the PZT membrane will undergo positive deflections, causing the voltage across the membrane to go to the maximum positive potential. When the change in pressure is zero, the PZT membrane will be at the most negative potential. The smaller increase in the waveform in the negative range is caused by the deflection of the membrane in this direction.

Measurements of the membrane as a function of frequency reveal that the resonant frequency of a 2.45 mm membrane is approximately 340 Hz as shown in Figure 2.4. The peak-to-peak voltage is greatest when the membrane is excited at the resonant frequency. The actual resonant frequency depends on the dimensions of the PZT material.

Through measurement results, an equivalent circuit model is developed for the 2.45 mm square PZT membrane as shown in Figure 2.5. Two sinusoidal voltage sources are used to model the voltages at resonance and the second harmonic frequency. The voltage source V_1 represents the fundamental frequency and V_2 represents the second harmonic frequency of the excitation. Although the electrical model for the piezoelectric device can be extended to a higher order (i.e. adding more sinusoidal voltage sources for higher order harmonics), a second or-
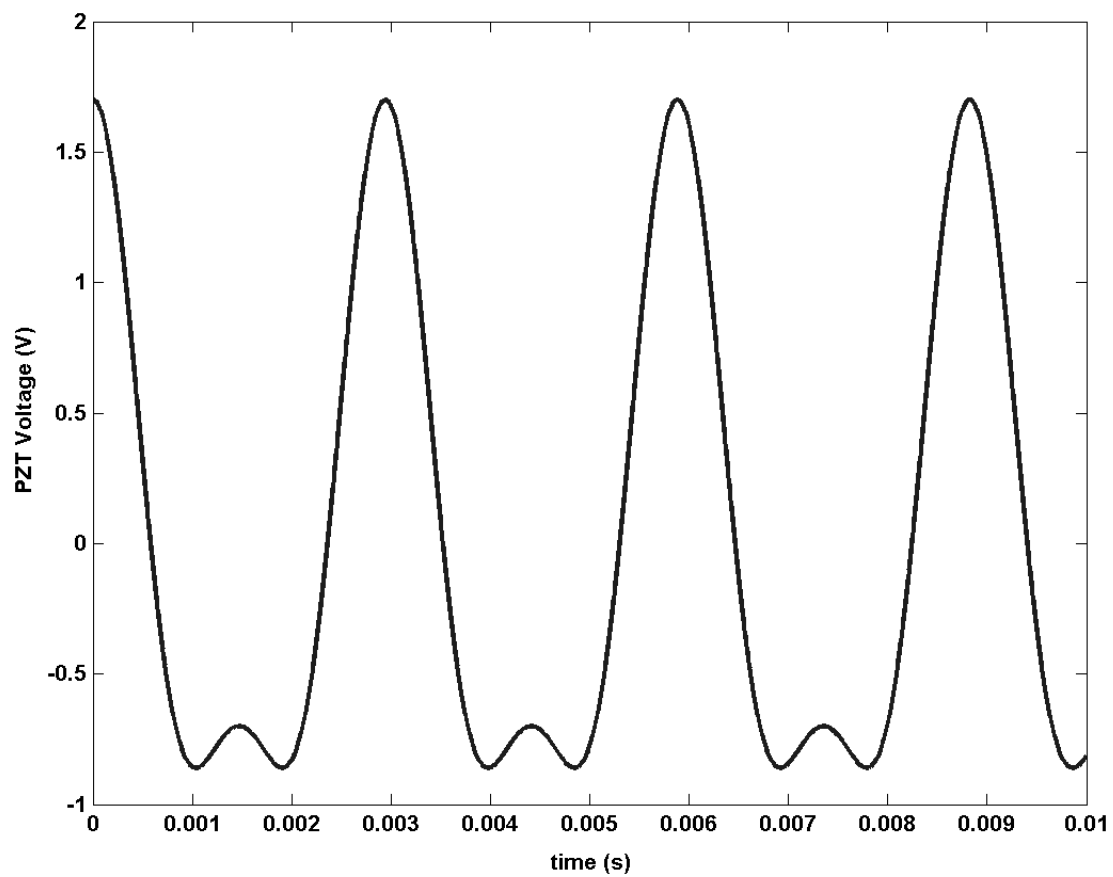
FIGURE 2.3. Measured open circuit output voltage of the 2.45 mm x 2.45 mm piezoelectric membrane.
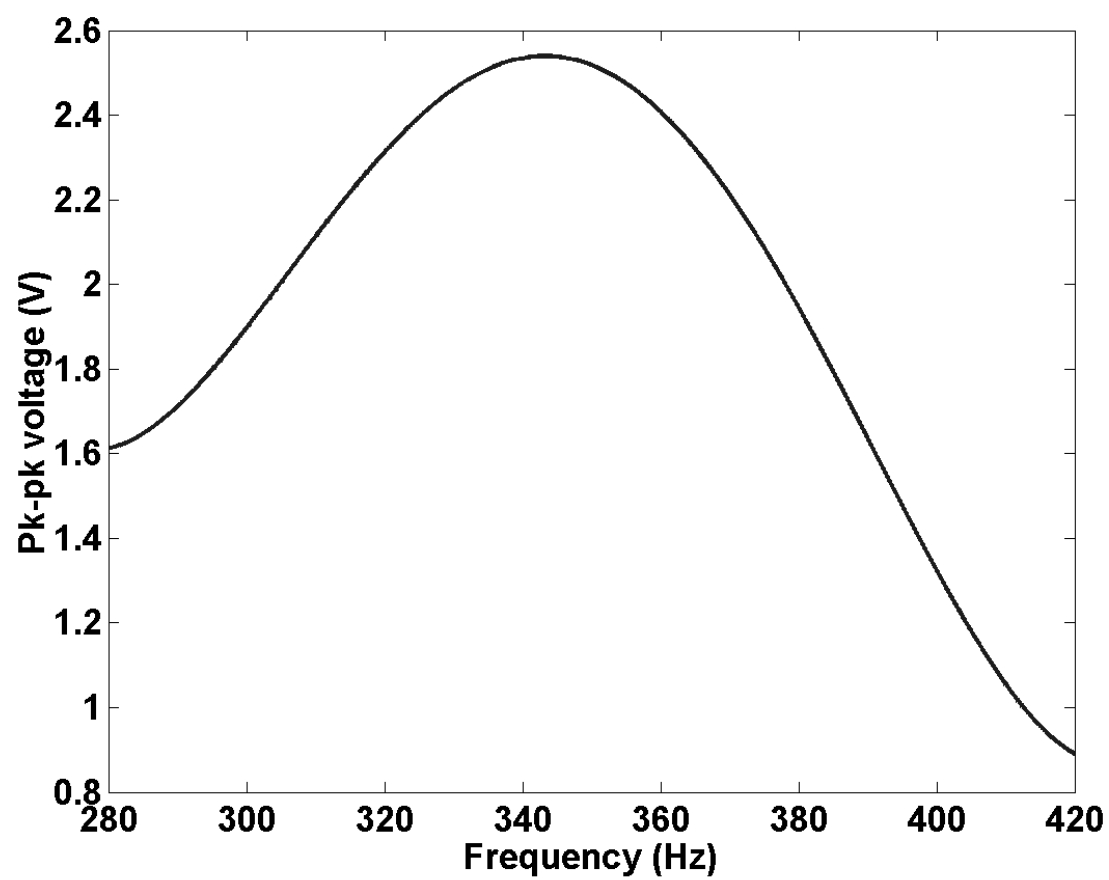
FIGURE 2.4. Measured peak-to-peak output as a function of input frequency.

der model is used because it is simple and provides a good approximation for the output voltage.

The internal impedance of this particular piezoelectric device is modeled as a 200-kΩ resistor connected in parallel with a 30-nF capacitor. At DC, the internal impedance is 200 kΩ and at the resonant frequency, the internal impedance is dominated by the reactive component from the internal capacitance. It is important to note that unlike most power sources, which have low output impedance, the piezoelectric power source is relatively high output impedance. This introduces unique challenges in designing efficient regulation and conversion circuitry.

By curve fitting the peak-to-peak voltage as a function of the input frequency, a fourth-order polynomial was found to most accurately model the changes in the output voltage at different excitation frequencies. Using the coefficients in Fig. 2.5, a particular frequency is chosen for the transient simulation using

$$V(t, f) = V_1(f) * cos(2\pi f t) + V_2(f) * cos(4\pi f t).$$

The response matches particularly well for excitation frequencies in the range of 280-430 Hz which are of highest interest in our application. By fixing the frequency of excitation on the PZT membrane and using this equivalent circuit model, it is possible to simulate and design power conversion circuits for subsequent fabrication.

2.4. Half-Wave Rectifier Interface Circuits

2.4.1. Passive Half-Wave Diode Rectifiers

To implement a half-wave diode rectifier in a conventional integrated circuit process, the diodes are constructed from diode-connected transistors. The diode-
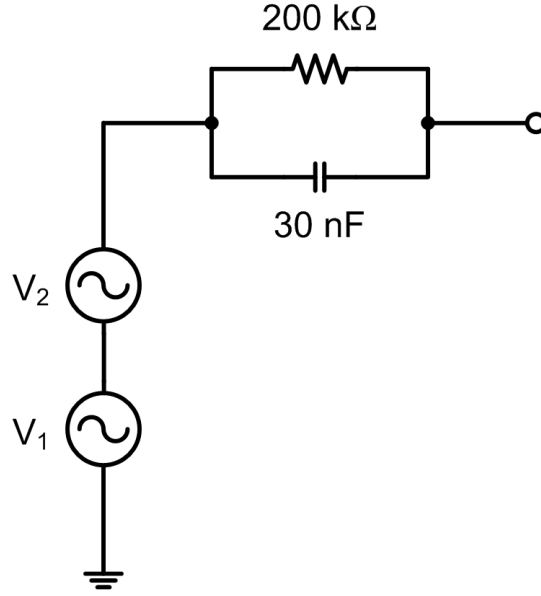
$$V_1(f) = a_1*f^4 + a_2*f^3 + a_3*f^2 + a_4*f + a_5$$

$$V_2(f) = b_1*f^4 + b_2*f^3 + b_3*f^2 + b_4*f + b_5$$

$a_1 = 2.0409 \times 10^{-8}$ $b_1 = 2.0188 \times 10^{-8}$

$a_2 = -2.8432 \times 10^{-5}$ $b_2 = -2.8541 \times 10^{-5}$

$a_3 = 1.4629 \times 10^{-2}$ $b_3 = 1.4952 \times 10^{-2}$

$a_4 = -3.2949$ $b_4 = -3.4392$

$a_5 = 2.7515 \times 10^{2}$ $b_5 = 2.9331 \times 10^{2}$

FIGURE 2.5. Equivalent circuit of the piezoelectric membrane which models the output voltage waveform as a function of excitation frequency (f) as well as the characteristic output impedance [9].

tied NMOS transistor circuit of Fig. 2.6 rectifies the voltage when the input voltage exceeds the threshold voltage of the transistor. With a typical NMOS transistor threshold voltage of 0.5 V, there is a significant reduction in the output voltage of the rectifier and the overall power efficiency. The body effect increases the threshold voltage of the NMOS transistor further, and thus the circuit is improved when a diode-tied PMOS transistor (with the body tied to the source) is connected in parallel with the NMOS transistor, Fig. 2.7.

$$\frac{20\ \mu m}{0.35\ \mu m}$$
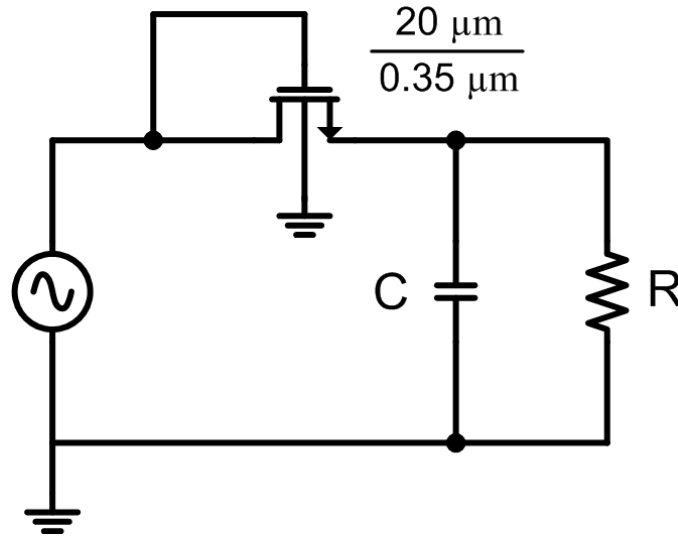
FIGURE 2.6. Half-wave rectifier with diode-tied NMOS.

To compare these circuits, simulations were performed using the TSMC 0.35μm CMOS process models. Figure 2.8 shows the simulated output power versus output current curve for the rectifier structures of Fig. 2.6 and 2.7 using the PZT equivalent circuit. From the output power curves, both half-wave rectifiers are capable of delivering a peak power of less than 2 μW.
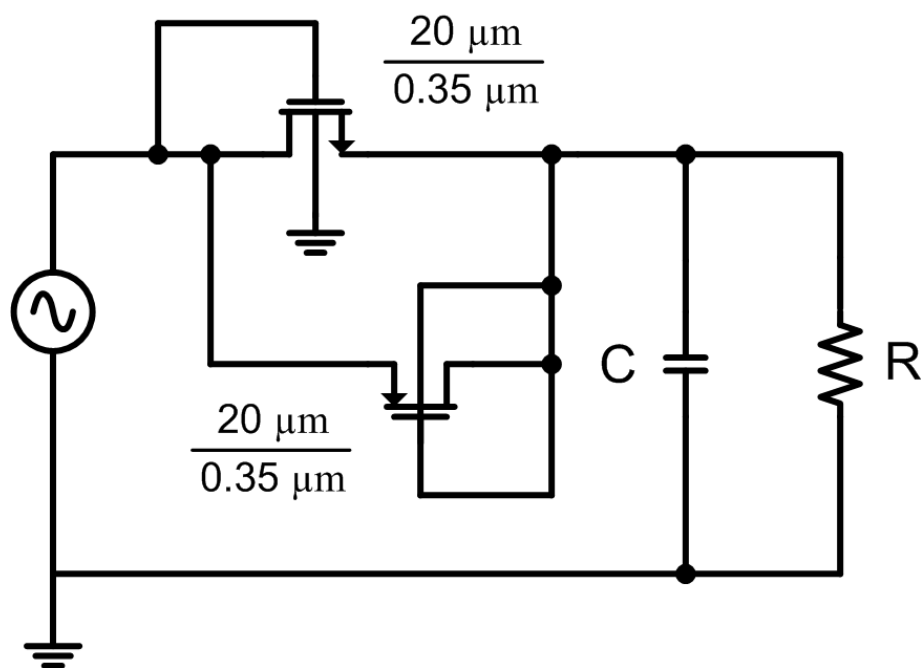
FIGURE 2.7. Half-wave rectifier with NMOS and PMOS diodes.
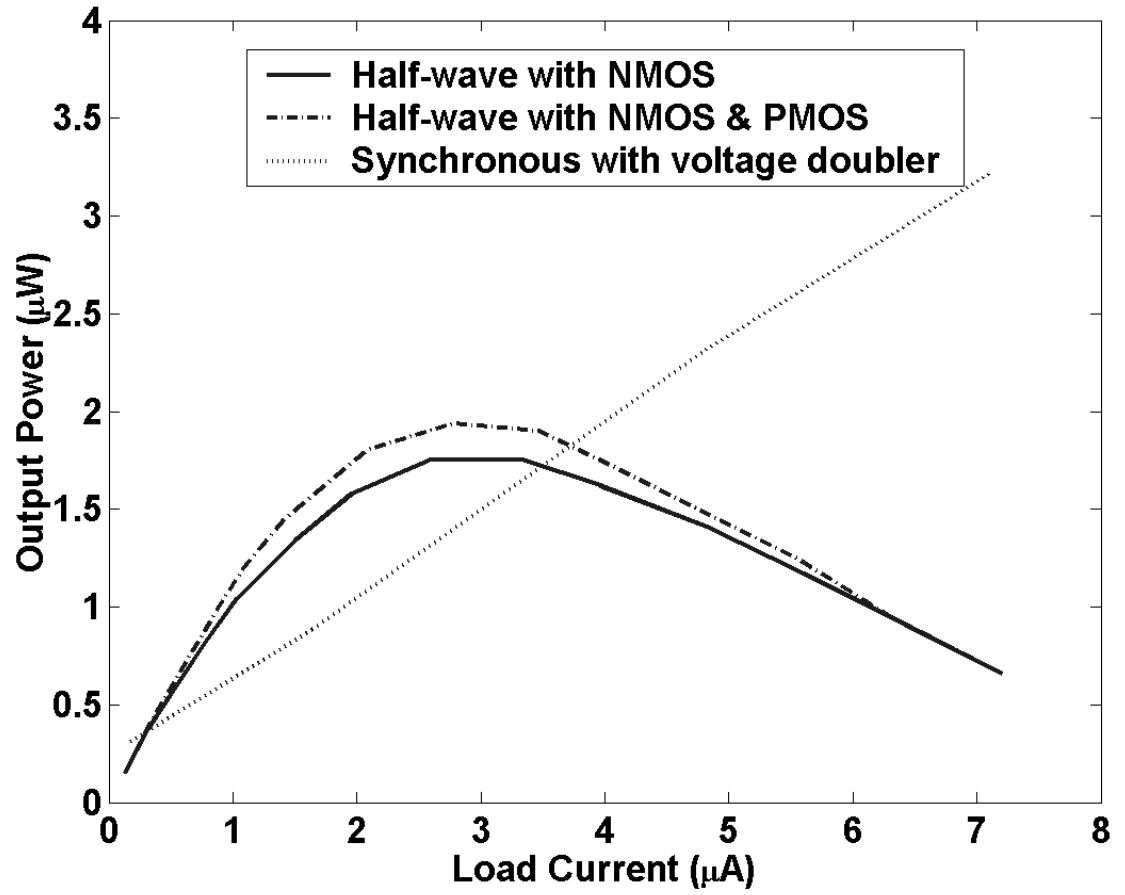
FIGURE 2.8. Simulated power delivery of half-wave rectifier circuits in a 0.35-μm CMOS process with the PZT input as shown in Fig. 2.3.

2.4.2. Synchronous Half-Wave Rectification

One way to overcome the limitation of the voltage drop is to use a synchronous rectifier circuit (Fig. 2.9). The PZT membrane model is used to simulate the synchronous rectification circuit with the voltage source and impedance block representing the equivalent circuit of the PZT device. The synchronous rectification circuit significantly reduces the equivalent diode voltage drop. However, because active circuits are used to reduce the diode drop, additional static power is required to operate the circuit. If this power is excessive, it can outweigh the benefits of the reduction in diode voltage drop.

In the synchronous rectifier circuit, a MOS transistor is used as a switch to control the conduction in the forward path. When the input to the synchronous rectifier is higher than its output voltage, the comparator output goes to the positive supply rail and turns on the switch to allow the charging of the output load. Conversely, when the input voltage of the synchronous rectifier is lower than the output voltage, the comparator output goes low, the switch is turned off and the forward conduction path is disconnected. The output voltage is very low from this circuit so an additional voltage doubling circuit is added as shown in Fig. 2.10. The voltage doubler is used to double the maximum voltage available from the PZT device.

A PMOS transistor is used as the switch for synchronous rectification because it allows a higher gate voltage drive and reduces the on-resistance of the switch. This allows more current to flow through the forward path and increases the rate at which the output capacitor is charged to its peak value. The size of the PMOS switch and the power supply voltage of the comparator in the synchronous rectifier also control the magnitude of the current and the charging rate through
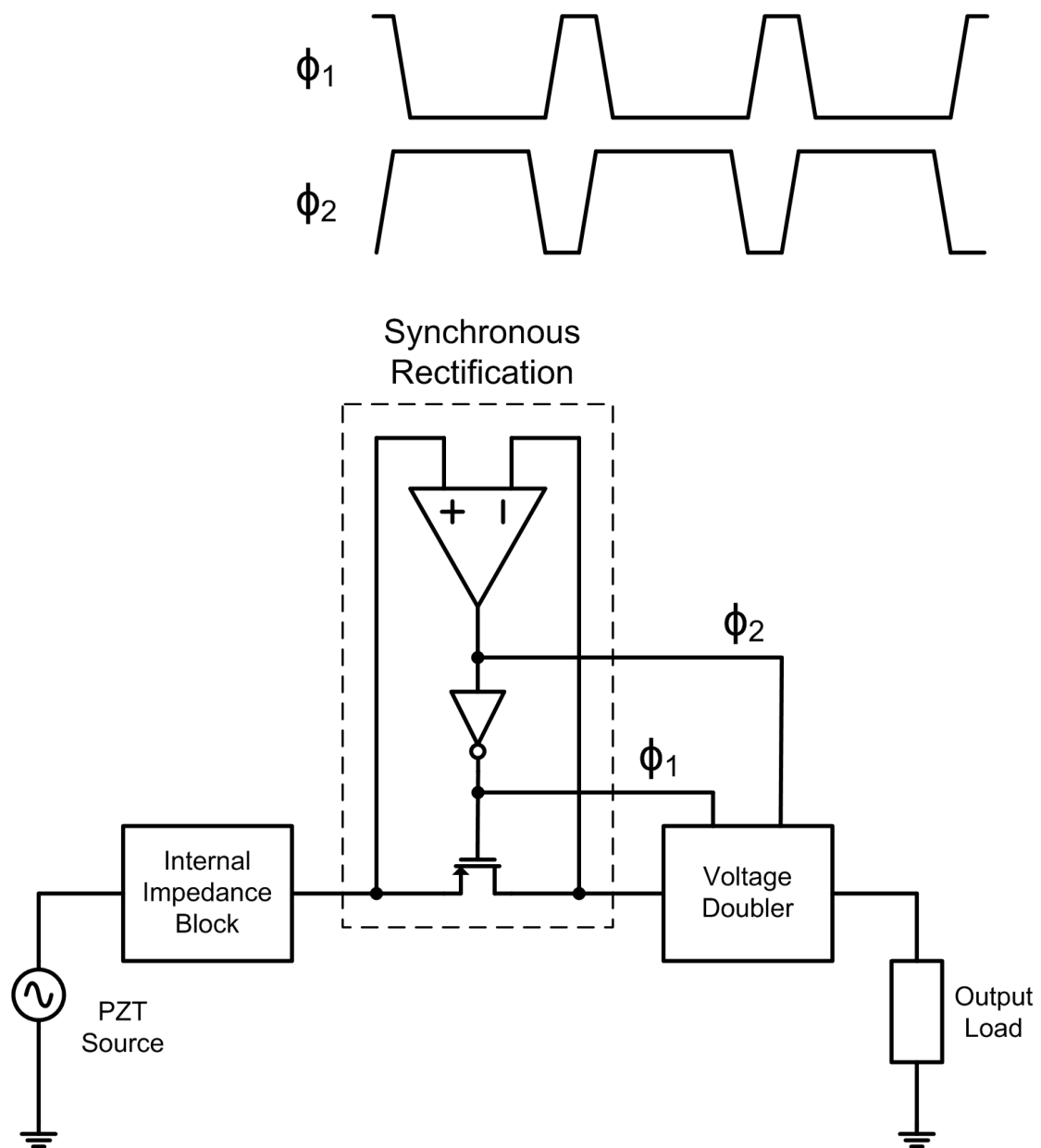
FIGURE 2.9. Modified synchronous rectifier to generate two-phase clocking for the voltage doubler
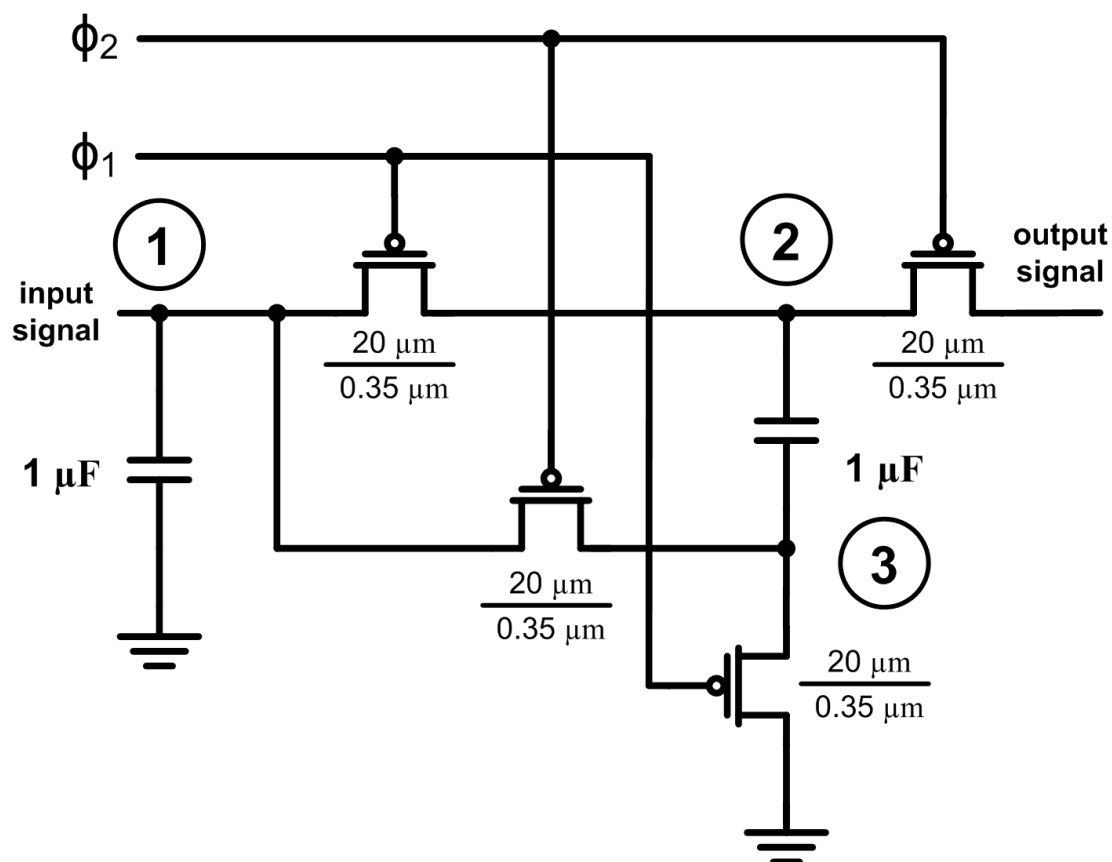
FIGURE 2.10. Transistor-level schematic of the voltage doubler.

the synchronous rectifier. Increasing the supply voltage of the comparator reduces the on-resistance of the switch and increases the charging rate but it also increases the power consumption for the comparator. The synchronous rectifier circuit is designed to operate with a supply voltage of 3.3 V. Increasing the size of the PMOS switch increases the charging rate but when the size of the switch gets too large, the gate capacitance seen by the output of the comparator increases thus reducing the slew rate of the comparator.

A switched capacitor voltage doubler customized to this application is shown in Figure 2.10 [34]. The two clock phases ϕ_1 and ϕ_2 are generated from the output of the comparator in the synchronous rectifier. In the voltage doubler, the 1 μF capacitor connected to node 1 holds the charge in the forward path. When the synchronous rectifier transistor is turned on, ϕ_1 is low and the two PMOS transistors connected to it are turned on. This charges the internal 1-μF capacitor connected between nodes 2 and 3. When ϕ_2 is low, the two capacitors are stacked to double the voltage at the output.

The design of the comparator is the most critical part in designing an efficient synchronous rectification circuit. The amount of power consumed by the comparator circuit is considered power loss in the synchronous rectification circuit because power must be drawn from other sources to power up the comparator. With the high internal impedance of the PZT device, the amount of power that can be delivered to the load is in the microwatts range. In order to create an efficient power conversion circuit, the comparator must operate with nanowatts of power.

For synchronous rectification of the voltage coming from the PZT membrane, the performance requirements for the comparator are relatively modest. A unity-gain bandwidth in the kiloHertz range and an open loop gain of approxi-

mately 40 dB is sufficient. To meet these requirements while achieving very low power, the comparator was designed in the subthreshold region [35, 39, 40]. The operating current is 50 nA and the supply voltage is 3.3 V resulting in a power dissipation of 165 nW.

Folded-cascode and telescopic opamp configurations were considered for this comparator. One of the advantages of the folded-cascode configuration is the high gain achieved from the two stages, however, the tradeoff is that it dissipates twice as much power as the telescopic configuration shown in Fig. 2.11. The telescopic configuration is chosen in this case because it burns less static power and more simple to design to fit to the desired specifications. To achieve the 40-dB gain with 50 nA of operating current, the input transistors are sized at 600 μm/0.6 μm to achieve a g_m of about 1.4-μA/V. The active load of the comparator is cascoded to help achieve the correct output common mode voltage as well as to limit the amount of current available when the output of the comparator goes high.

The EKV transistor model was used to design the comparator [35–37] in the subthreshold region. Simulation results of the power conversion circuit efficiency versus output load, is shown in Fig. 2.12, where power conversion efficiency defined as the ratio between the average output power and average input power when the output voltage is charged up to a steady state. The comparator in the measurement was powered by an external power source. For the calculation of power conversion efficiency, the input power is the combination of the average power dissipated by the PZT membrane model and the power dissipated by the comparator. The PZT membrane model was used as the input power source to the power conversion circuit. For output currents greater than 4 μA, the efficiency is more than 90%. To compare this rectifier with the passive half-wave rectifier, the
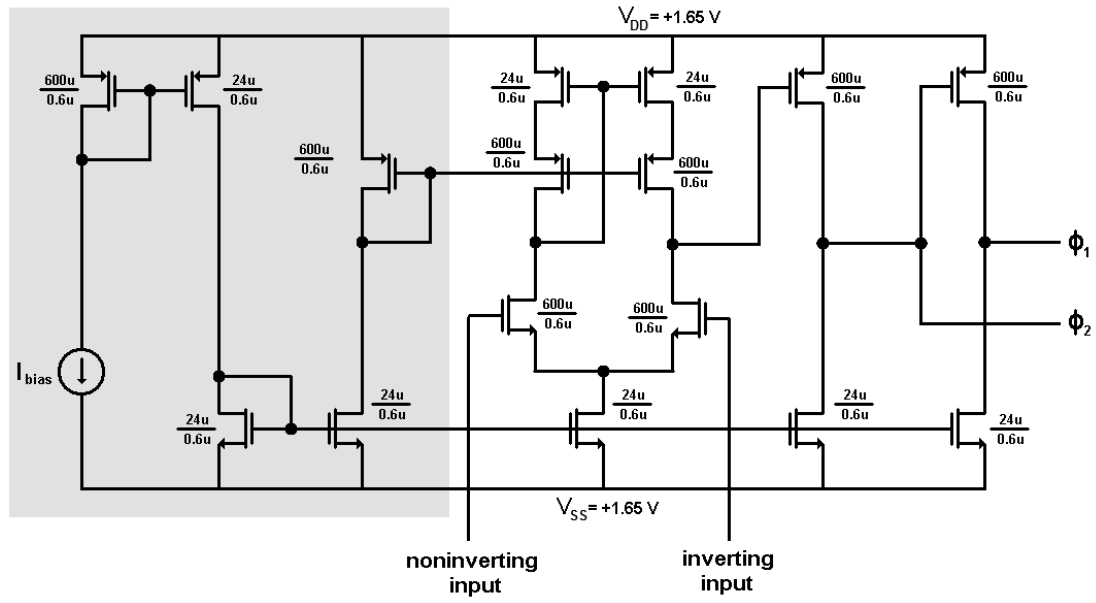
FIGURE 2.11. Schematic of the comparator designed and fabricated in the TSMC 0.35-μm CMOS process.

power delivery versus load current is shown in Fig. 2.8. For 6-μA load current, the output power is nearly 3 μW which is double that of the passive rectifier.
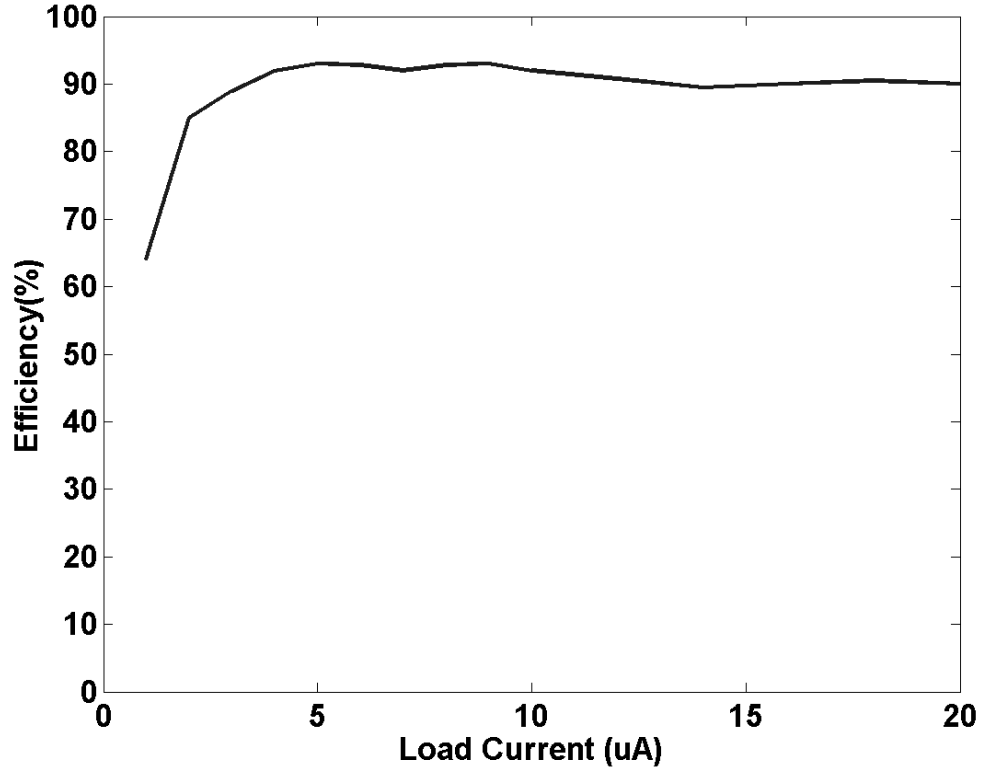
FIGURE 2.12. Simulated efficiency versus output load for the synchronous rectifier designed in the 0.35-μm CMOS process.

The die photograph for the synchronous rectifier and voltage doubler is shown in Fig. 2.13. The total die area is 160 μm x 100 μm fabricated in the TSMC 0.35-μm CMOS process. All routing and interconnections are as short as possible to reduce junction leakage. When the bias current of the comparator is in the lower nanoamp range, junction leakage can no longer be negligible and may

reduce the performance of the comparator. Also, the comparator is shielded with a guard ring to reduce the noise current from the substrate.
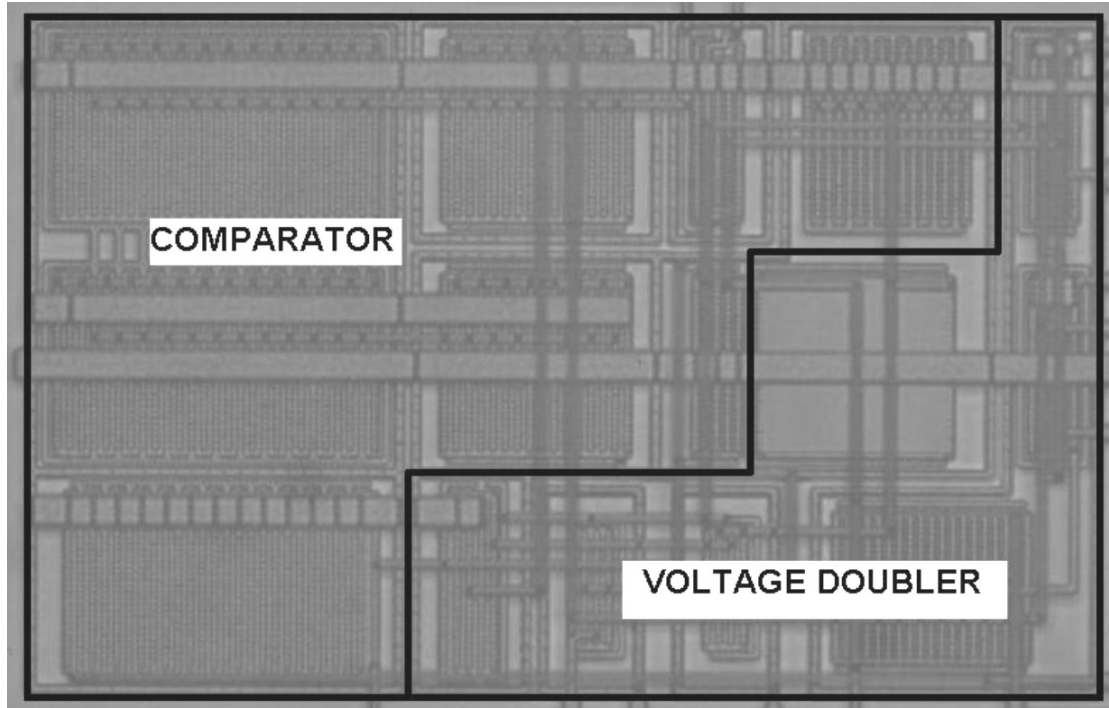
FIGURE 2.13. Die photograph of the synchronous rectifier and voltage doubler designed and fabricated in the TSMC 0.35-μm CMOS process.

The chip was characterized by connecting the power conversion circuit to the actual piezoelectric membrane. The piezoelectric membrane was excited using a periodic mechanical air pressure device driven by a high voltage AC source. The air pressure is focused on the piezoelectric membrane and periodically alternates at the resonant frequency. Table 2.1 summarizes the simulation versus the measurements of the power conversion circuit.

The measured results are in good agreement with the simulations. The DC output voltage is in the range of 0.6 V for a peak input of approximately 0.6 V. The

	R_{load}	P_{input} (μW)	V_{out} (V)	P_{out} (μW)	Efficiency ($\%$)
Simulated	10 MΩ	0.410	0.559	0.312	67.9 %
Measured	**10 MΩ**	**0.457**	**0.576**	**0.332**	**65.5** %
Simulated	330 kΩ	1.002	0.541	0.880	84.3 %
Measured	**330 kΩ**	**1.053**	**0.548**	**0.910**	**82.5** %
Simulated	100 kΩ	2.472	0.480	2.311	91.7 %
Measured	**100 kΩ**	**2.766**	**0.498**	**2.498**	**88.4** %

TABLE 2.1. Measured and simulated results for the half-wave synchronous rectifier and voltage doubler connected to the output of the PZT device.

ripple on the output ranges from 0.1 to 0.2 V. The ripple is primarily dependent on the gain of the comparator, the value of the holding capacitor, and the clock frequency. The output power ranges from 0.3 to 2.5-μW with an efficiency of 65% to 88%, respectively.

2.5. Full-Wave Rectifier Circuits

Improvements in the output power can be made using full-wave rectification and adapting it to achieve the highest possible output power from the piezoelectric device.

2.5.1. Passive Full-Wave Rectifier Interface Circuit

The conventional full-wave diode rectifier circuit is shown in Fig. 2.14. With this structure, the output suffers from a loss of voltage equivalent to two diode voltage drops. To overcome this limitation, the reduced diode turn-on voltage structure shown in Fig. 2.15 in the dotted box is used in place of the conventional diode. The modified passive power conversion circuit operates fundamentally the same as the conventional full-wave rectifier. The top portion of the circuit provides the conduction path between the input and the output nodes to charge up the holding capacitor. While the bottom portion of the circuit provides the conduction path between the input and ground to clamp the input voltage to ground once the input goes negative.
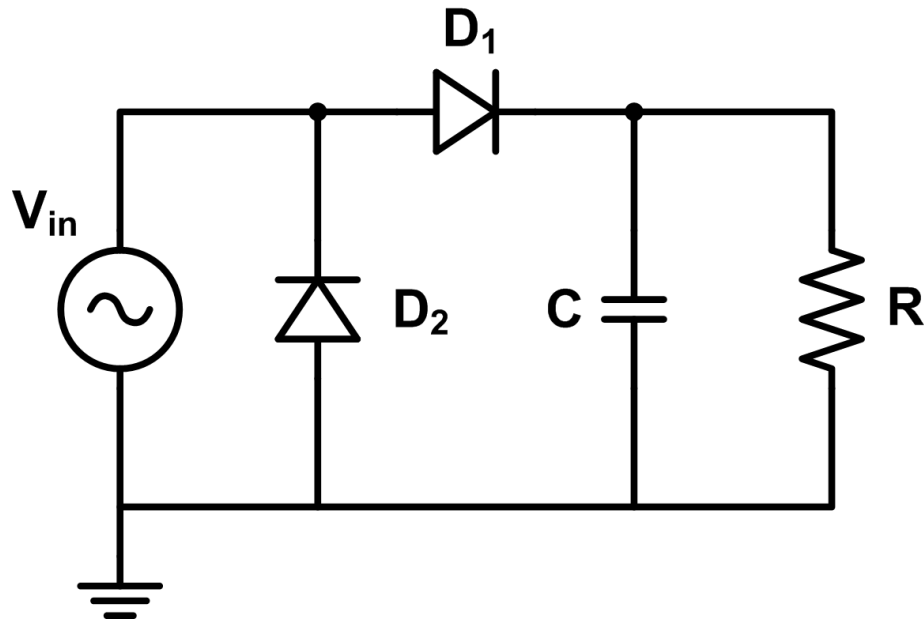
FIGURE 2.14. Passive full-wave rectifier.
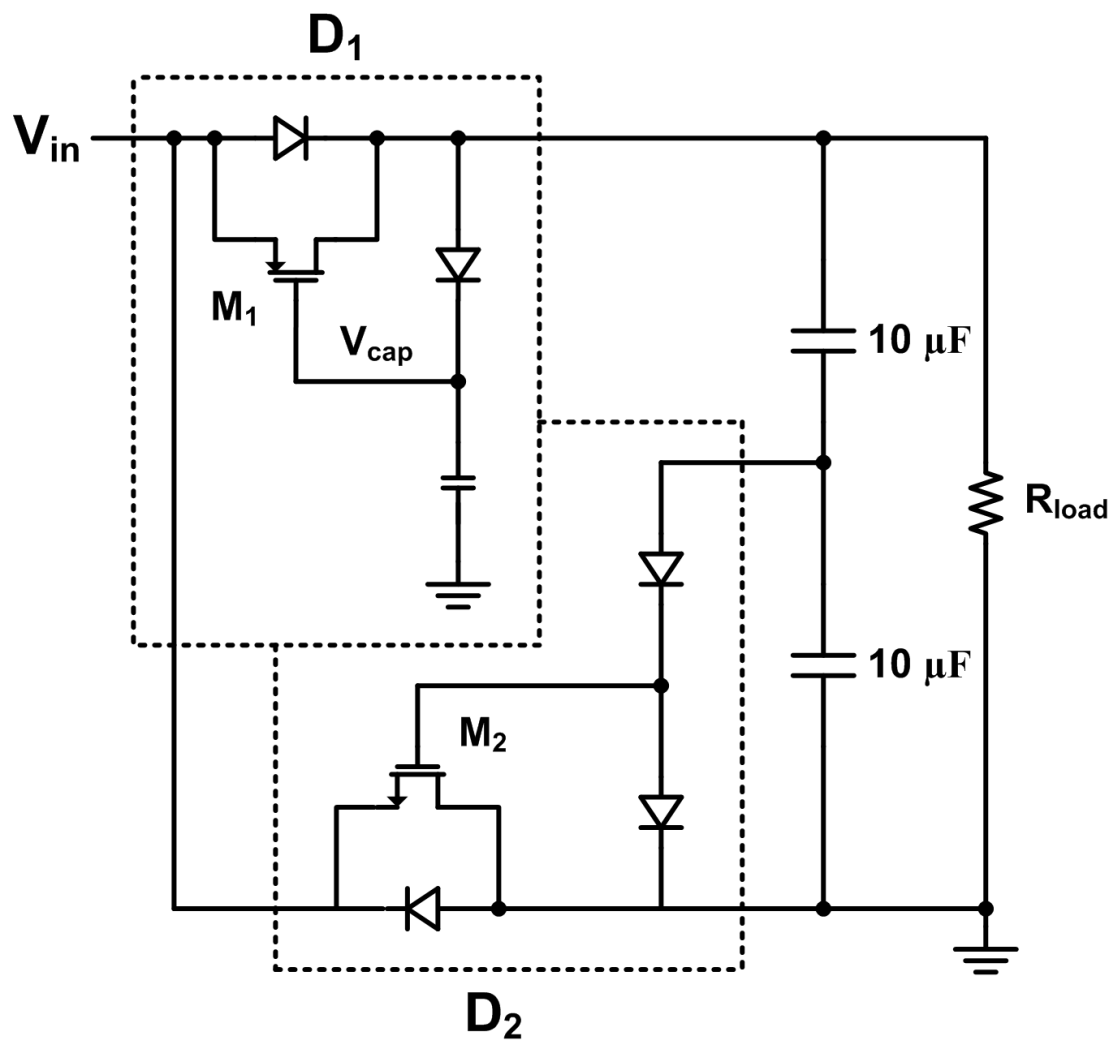
FIGURE 2.15. Reduced diode turn on voltage passive power conversion circuit.

The reduced V_T diode circuit, as shown in the dotted regions of Fig. 2.15, is designed to reduce the threshold voltage of a diode, to improve the efficiency, increase the output power and the output voltage. When the input voltage (V_{in}) in Fig. 2.14 and 2.15 is higher than the output (V_{out}) by at least the diode voltage drop, current flows through the diode tied transistor D_1 and charges the output capacitor until the output voltage reaches:

$$V_{out} = V_{in} - V_{TN} \tag{2.1}$$

where V_{TN} is the threshold voltage of diode tied transistor D_1. As the output node is charged up, the voltage across the capacitor, V_{cap}, also charges up toward the voltage:

$$V_{cap} = V_{out} - V_{TN} \tag{2.2}$$

Substituting 2.1 into 2.2 we get

$$V_{cap} = V_{in} - 2V_{TN} \tag{2.3}$$

through the diode-tied transistor D_2. The voltage held on the capacitor is two threshold voltages below the input voltage. Since the V_{SG} of the PMOS transistor is $2V_{TN} > |V_{TP}|$, the PMOS transistor will start to conduct and charge the output node. The PMOS transistor is cutoff when the gate-source voltage reaches the threshold voltage of the PMOS transistor, V_{TP}, i.e,

$$V_{in} - V_{cap} = |V_{TP}| \tag{2.4}$$

Substituting V_{cap} from 2.3 into 2.4 we obtain:

$$V_{SG} = V_{in} - V_{cap} = V_{in} - (V_{out} - V_{TN}) = |V_{TP}| \tag{2.5}$$

$$|V_{TP}| = V_{in} - V_{out} + V_{TN} \tag{2.6}$$

$$V_{out} = V_{in} - (|V_{TP}| - V_{TN}) \tag{2.7}$$

From the above relationship, the effective V_T of the circuit in 2.15 is $|V_{TP}| - V_{TN}$

The full-wave passive rectifier circuit was designed and fabricated in the TSMC 0.25-μm CMOS process. The die microphotograph is shown in Fig. 2.16 where all capacitors are off-chip due to the large sizes required (in the microfarad range). The circuit is designed so that the ratio of the two 10-μF holding capacitors can be changed to achieve maximum power transfer at a particular load current. Maximum power transfer is achieved by keeping the voltage drop of the bottom holding capacitor to roughly two diode voltage drops.
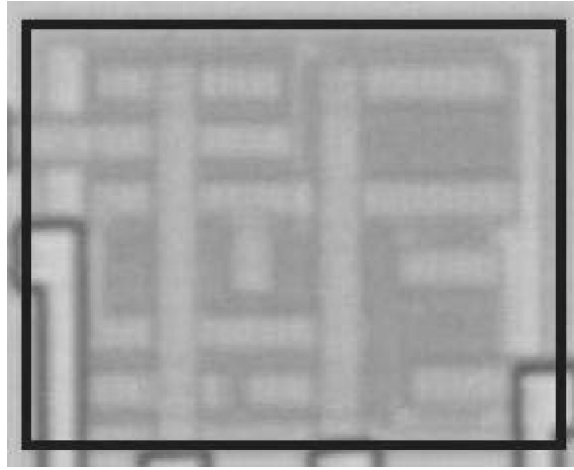
FIGURE 2.16. Die photograph of the passive full-wave rectifier circuit with reduced VT circuitry fabricated in a 0.25-μm CMOS process.

Fig. 2.17 through 2.19 shows the efficiency, output power, and output voltage versus load current plot for the low-V_T passive full-wave rectifier. The efficiency of the passive rectifier peaks between 5 and 10-μA at about 65%. It is

capable of delivering 16-μW to the load and can deliver up to 2.2V under no-load conditions.
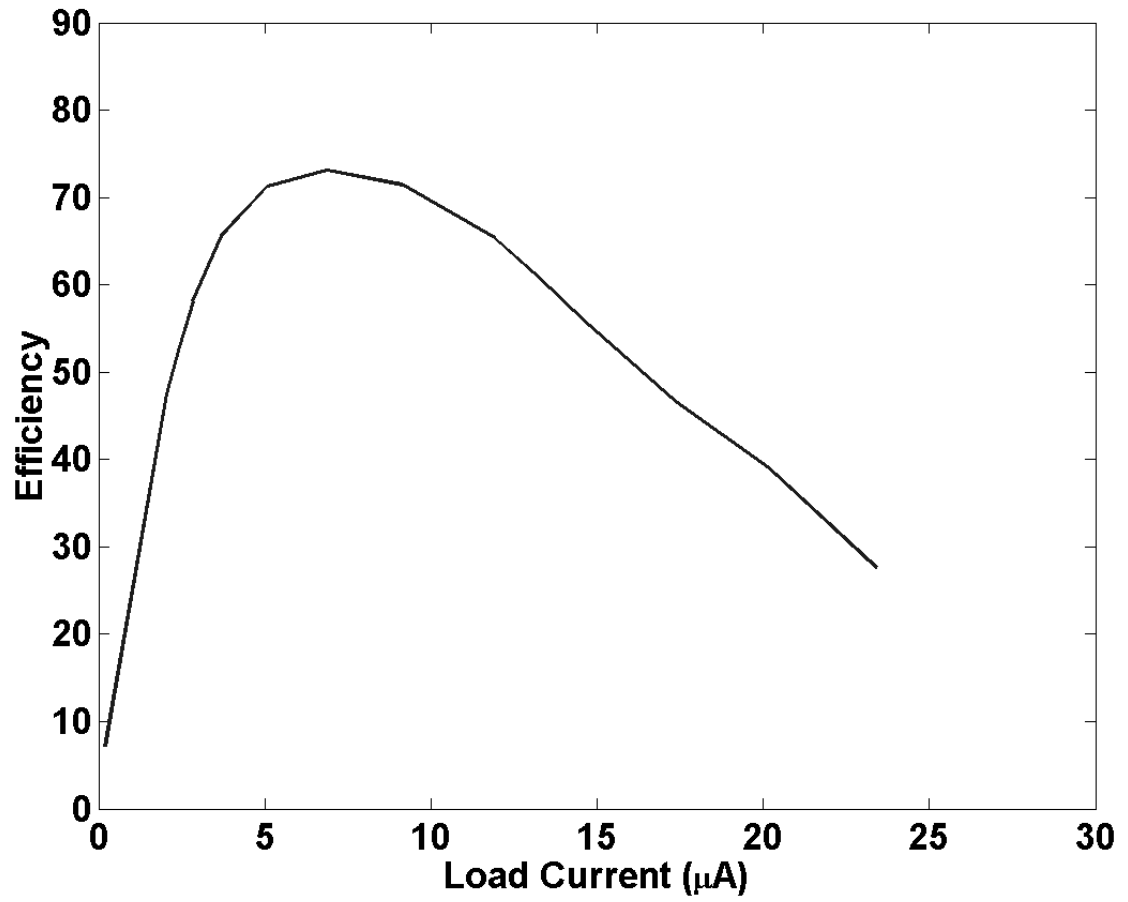
FIGURE 2.17. Power conversion efficiency versus load current of the full-wave passive rectifier circuit with reduced-VT.
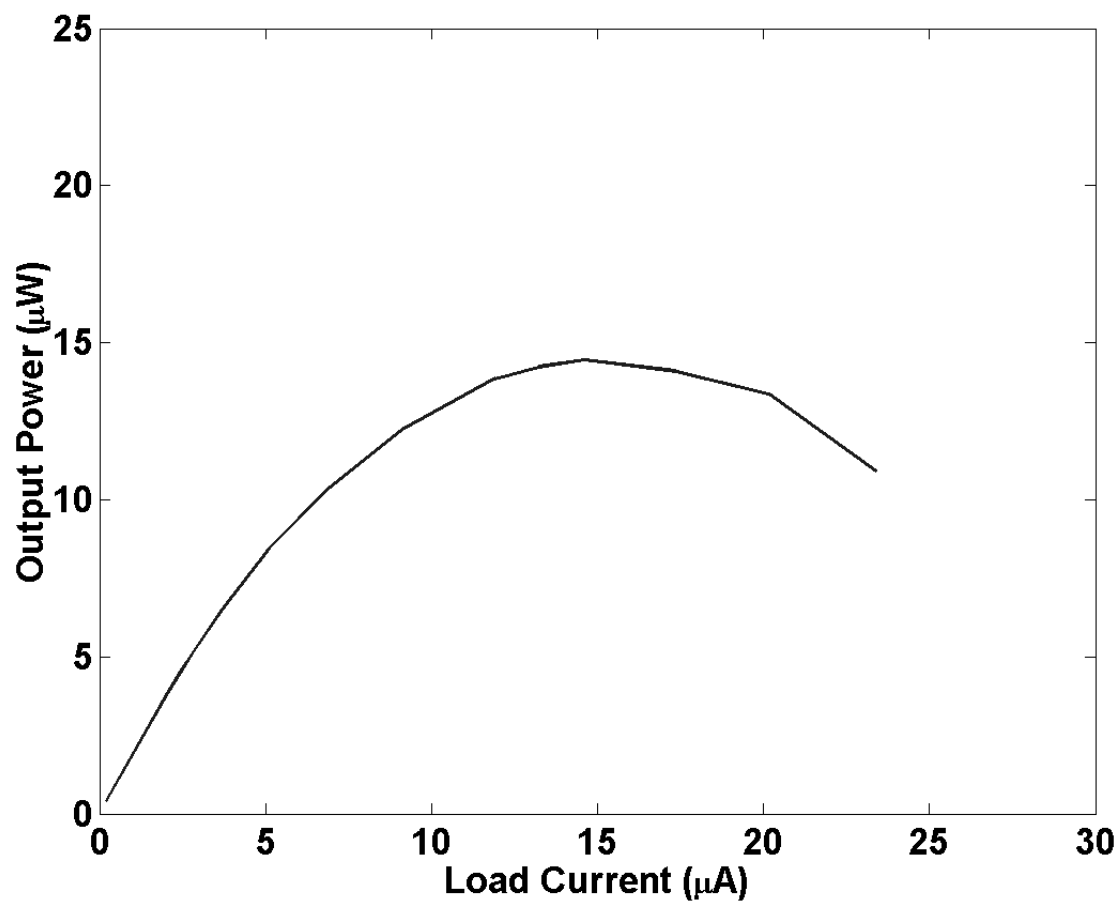
FIGURE 2.18. Output power versus load current of the full-wave passive rectifier circuit with reduced-VT.
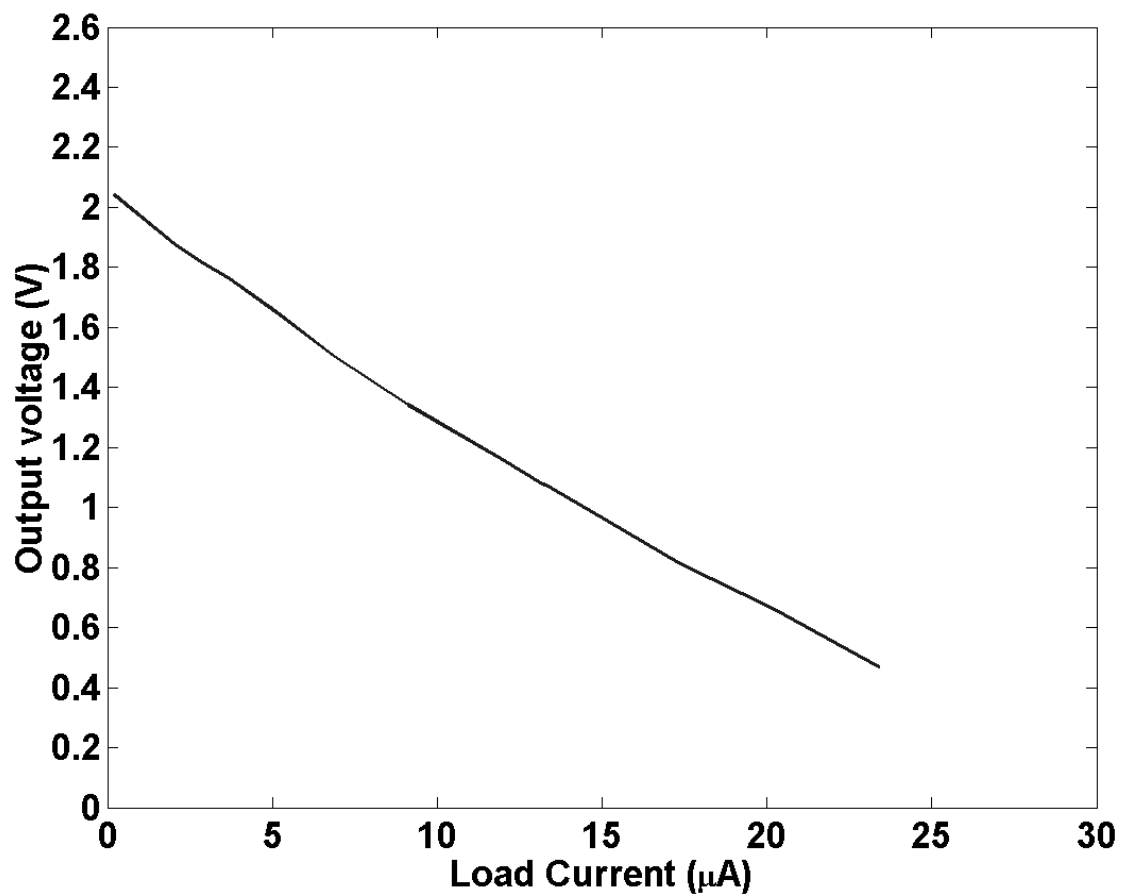
FIGURE 2.19. Output voltage versus load current of the full-wave passive rectifier circuit with reduced-V_T.

2.5.2. Synchronous Full-Wave Rectifier Interface Circuit

An alternative to the passive full-wave rectifier is the synchronous full-wave rectifier shown in Fig. 2.20 [38]. The two conduction paths are controlled by synchronous rectifiers. When the input voltage to the rectifier is higher than the output voltage, comparator C_1 switches high, thus turning on switch M_1 to provide a forward conduction path between the input and the output nodes. When the input voltage goes negative, comparator C_2 is switched high and switch M_1 is turned on, providing a conduction path between the input and ground. This causes the input voltage to be clamped to ground.
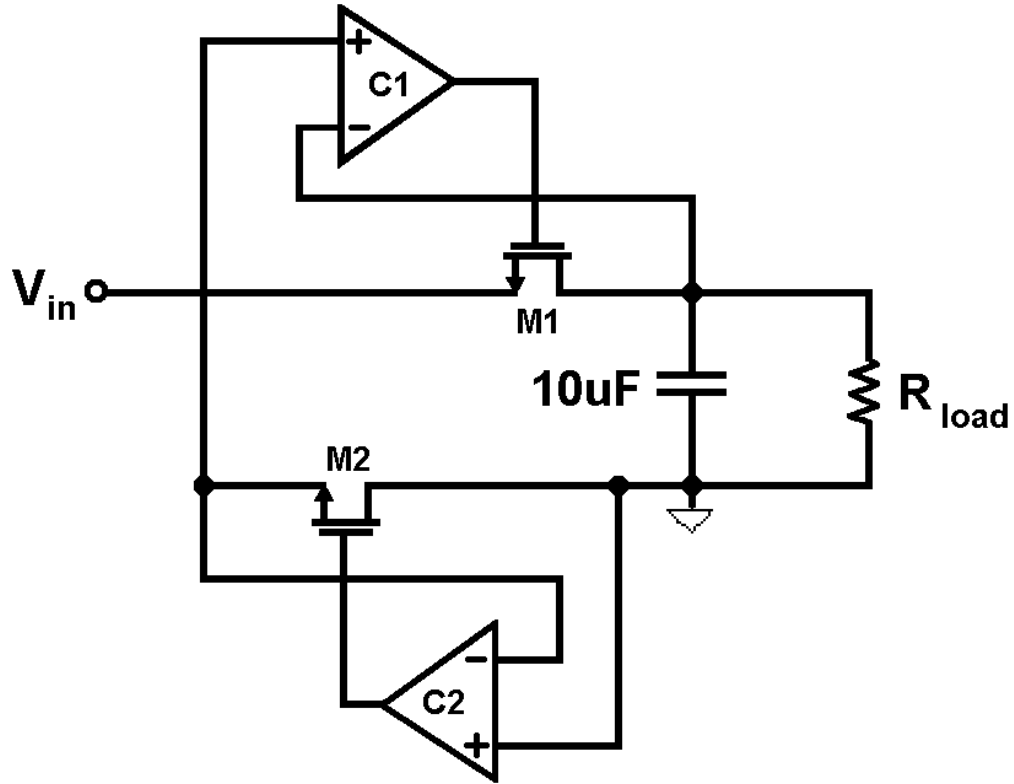
FIGURE 2.20. Synchronous full-wave rectifier.

When a PZT membrane is connected between the input of the rectifier and ground, the internal impedance of the PZT membrane is dominated by the capacitance at the resonant frequency, and the device acts like a capacitor. When the input voltage is clamped to ground, the PZT membrane holds the voltage difference between the PZT output voltage and ground. When the PZT output voltage is at the lowest voltage potential, the amount of charge held across the PZT membrane is equivalent to the peak negative voltage. Once the voltage from the piezoelectric device rises again, the charge stored across the device will add to the PZT output voltage and cause the input voltage to increase until it reaches the peak-to-peak voltage of the piezoelectric membrane output.

The comparators used in the active full-wave rectifier are designed to operate in the subthreshold region. Each of the comparators require a separate power supply of 2.5 V, with the V_{DD} and V_{SS} of each comparator set at different voltage level. The unity gain bandwidth of these comparators range from 4 kHz to 200 kHz depending on how much power the comparator consumes. The DC gain of the comparator is in the range of 40-60 dB. A PMOS transistor is used as the switch controlled by comparator C_1 and an NMOS transistor is used as the switch controlled by comparator C_2 to maximize the gate voltage drive.

The die photograph of the full-wave synchronous rectifier circuit is shown in Figure 2.21. The active area of the layout is 150 μm x 100 μm. The layout is symmetrical to reduce device mismatches and all routing is minimized to reduce junction leakages.

Measurement results for the synchronous rectifier circuit are shown in Fig. 2.22 through 2.25. Figure 2.22 shows the power conversion efficiency curves of the full-wave synchronous rectifier as a function of the load current. The conversion efficiency changes with a change in the slew rate of the comparator due to the
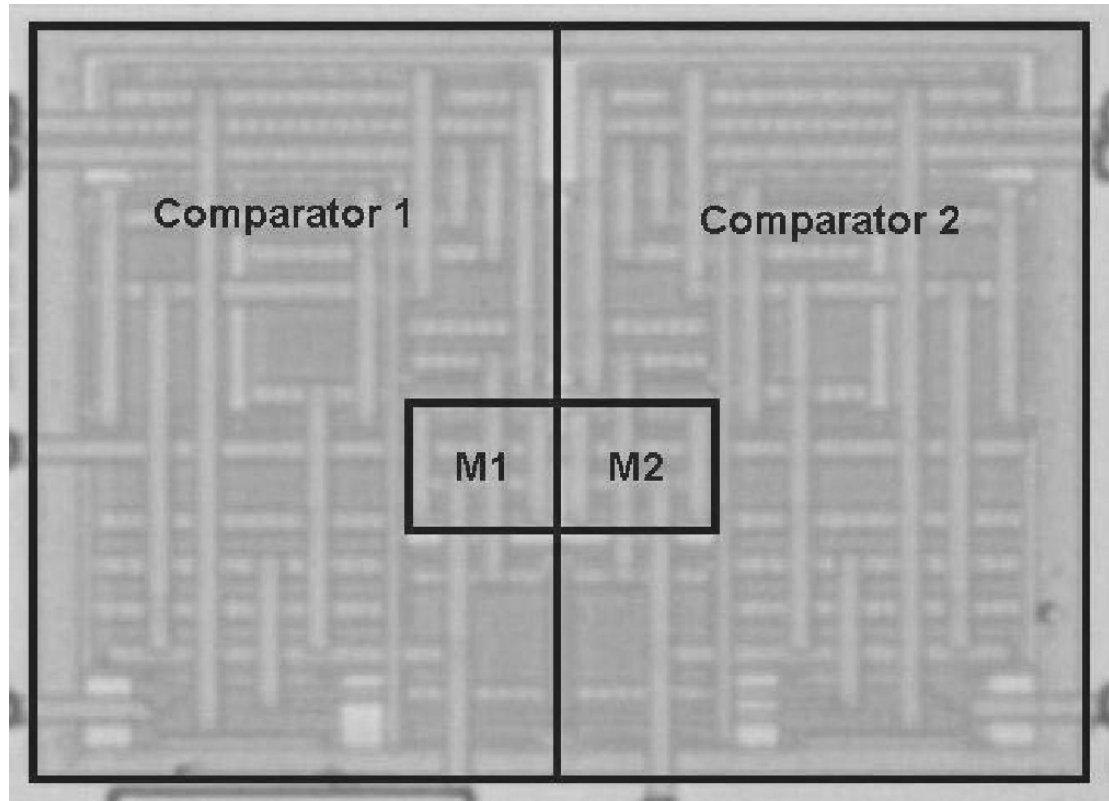
FIGURE 2.21. Die photograph of the full-wave synchronous rectifier circuit fabricated in a 0.25μm CMOS process.

change in the bias currents. For low power dissipation (0.58 μW), the slew rate is low and the switching speed of the synchronous rectifier is lower. The power conversion efficiency is approximately 70%. For high power dissipation in the comparator (2.73 μW), the slew rate is higher and losses due to the switching are reduced. However, the comparator power dissipation also contributes to the power loss thus reducing the overall efficiency of the rectifier.
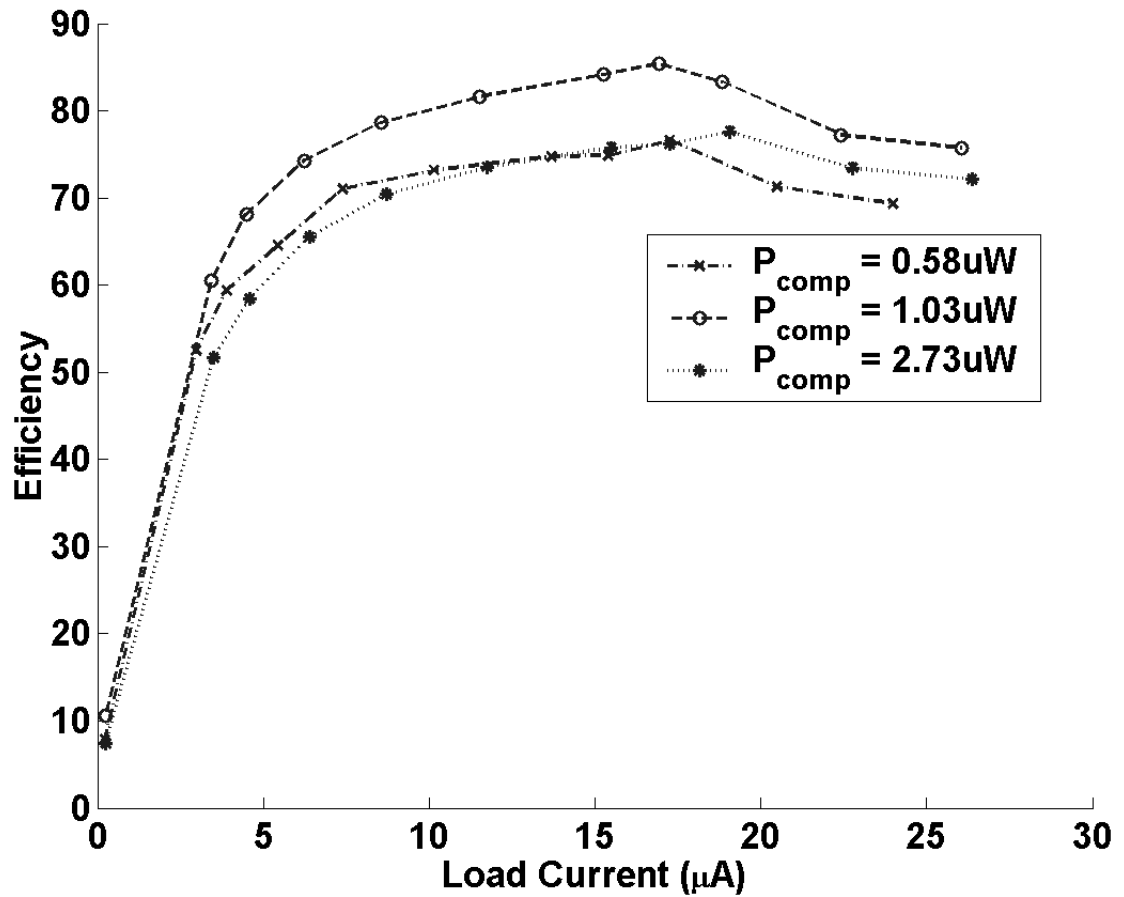
FIGURE 2.22. Measured power conversion efficiency for the synchronous rectifier.
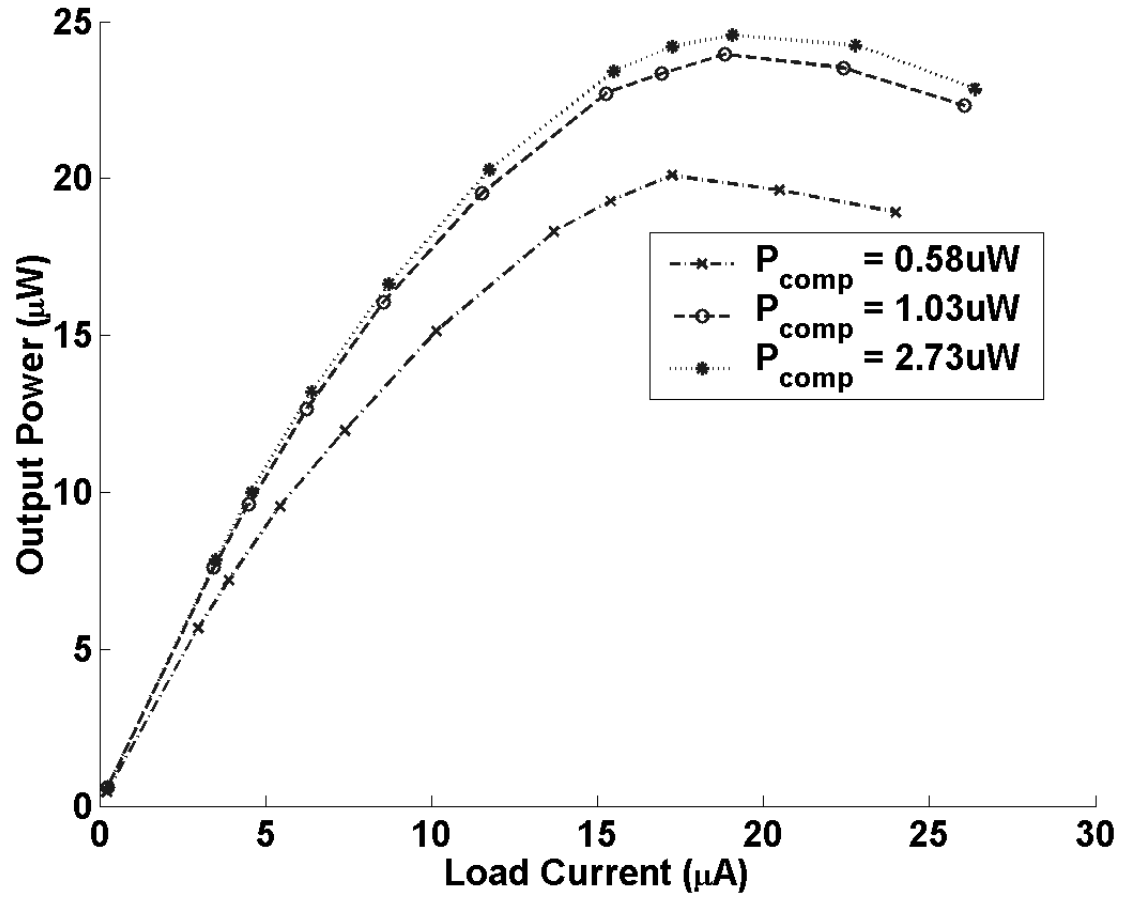
FIGURE 2.23. Measured output power for the synchronous rectifier.

Fig. 2.23 and 2.24 show the output power and effective output power curves of the full-wave synchronous rectifier. The output power curve is the amount of power dissipated at the load while the effective output power is the output power minus the power dissipated by all the comparators. In the case of high power dissipation in the comparator (2.73 μW), the amount of output power is the highest of the three curves, which reaches to almost 25 μW. However, the effective output power for this case is not the best of the three cases since the power dissipated in the comparators is quite high. The best effective output power curve is the case where the comparator power dissipation is 1.03 μW. The peak effective output power for the full-wave synchronous rectifier is around 22 μW. Fig. 2.25 shows the output voltage curves for the three cases. The case of low power dissipation has the worst performance and peaks at 2.15 V with no load. The other two cases are quite close and they have a peak output voltage of roughly 2.45 V with no load.

Of all the power conversion circuits introduced, the best performance is achieved using the active circuit based on the full-wave synchronous rectification architecture. It gives higher efficiency (85%), higher output voltage (2.45 V at open load) and is able to deliver more power to the load (22 μW). The full-wave passive rectifier performs well despite the relatively high diode threshold voltage (about 0.5 V) in the TSMC 0.25-μm CMOS process. If a process with low diode threshold voltage is used, the performance of the full-wave passive rectifier can be drastically improved and could overcome the performance of the full-wave synchronous rectifier.
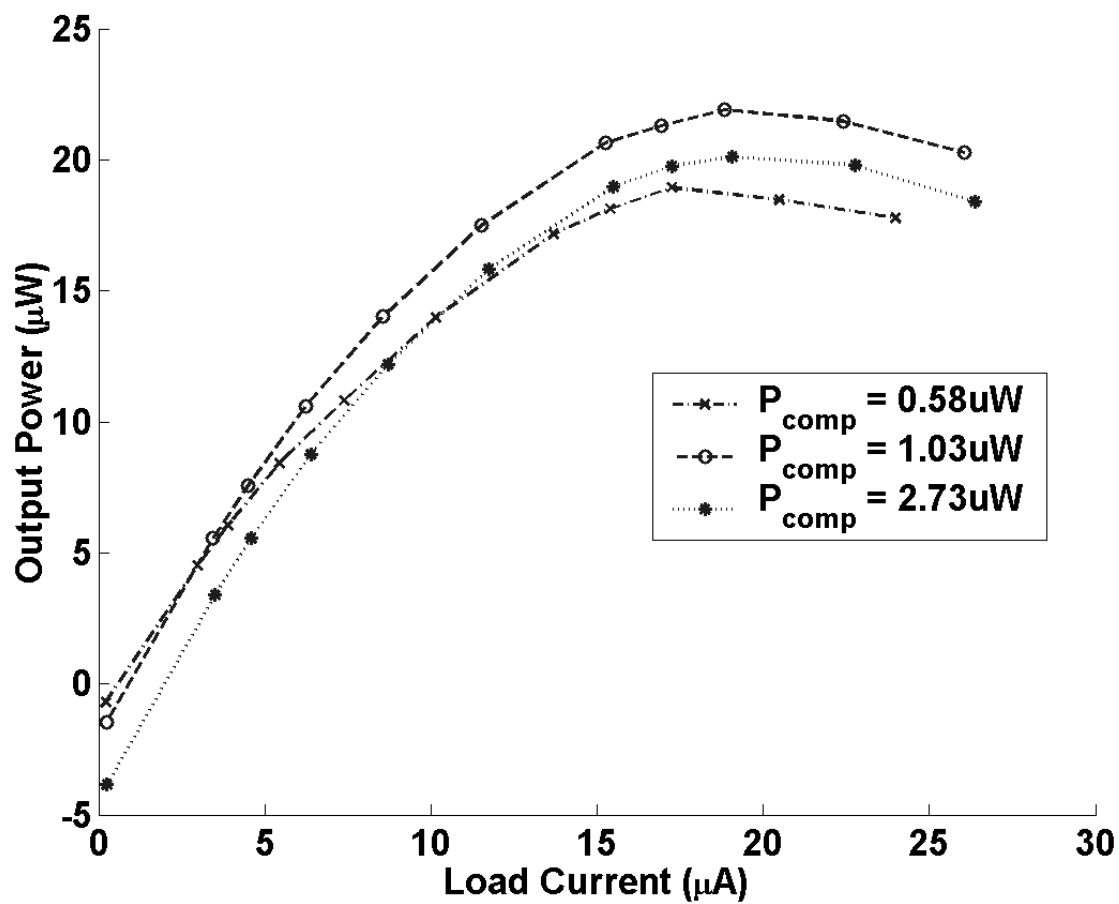
FIGURE 2.24. Measured effective output power for the synchronous rectifier.
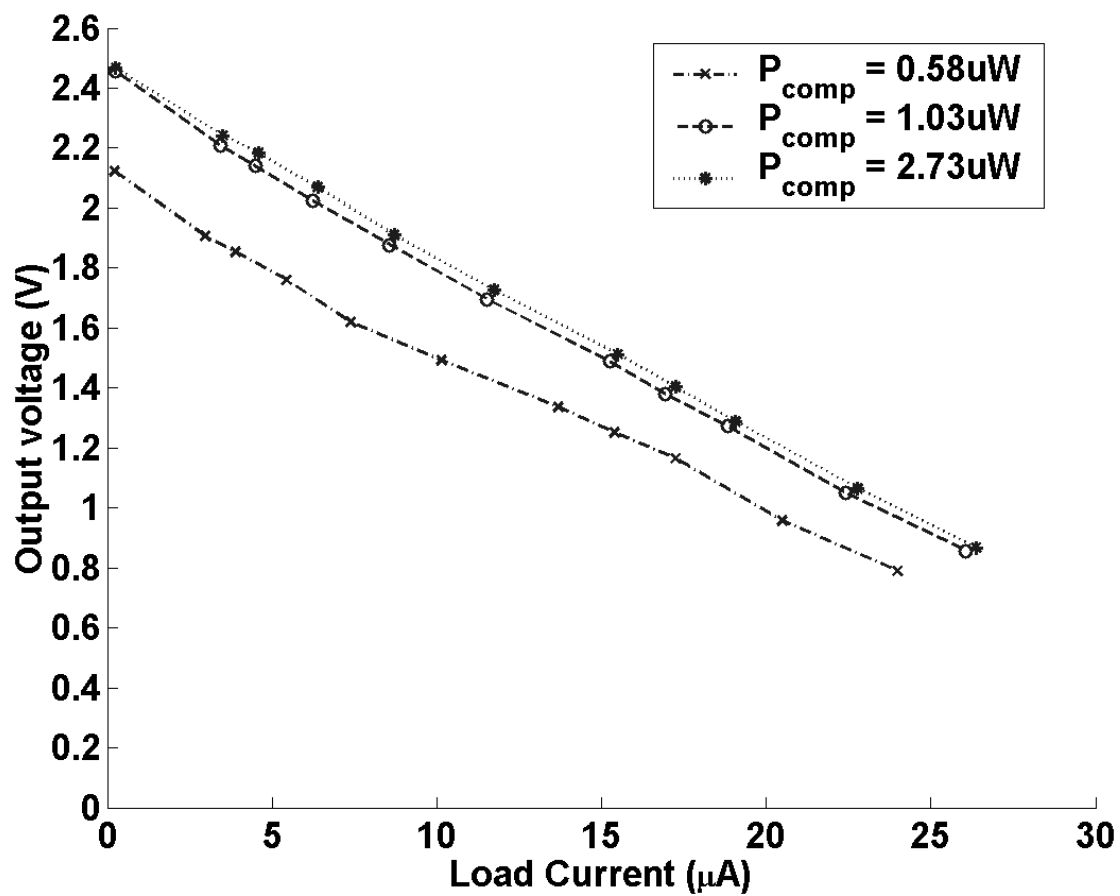
FIGURE 2.25. Measured output voltages for the synchronous rectifier.

2.6. Conclusion

New power conversion circuits to interface to a piezoelectric power generator are presented. Their simulation and measurement results are shown. Due to the low output voltage nature of the PZT material, conventional diode rectifiers do not provide efficient power conversion. The high internal impedance of the material also confines maximum power conversion to the microamp range.

3. EFFICIENT FAR-FIELD RADIO FREQUENCY ENERGY HARVESTING FOR PASSIVELY POWERED SENSOR NETWORKS

3.1. Abstract

An RF-DC power conversion system is designed to efficiently convert far-field RF energy to DC voltages at very low received power and voltages. Passive rectifier circuits are designed in a 0.25μm CMOS technology using floating gate transistors as rectifying diodes. The 36-stage rectifier can rectify input voltages as low as 50mV with a voltage gain of 6.4 and operates with received power as low as 5.5μW (-22.6 dBm). Optimized for far field, the circuit operates at a distance of 44m from a 4W equivalent isotropically radiated power (EIRP) source. The high voltage range achieved at low load current make it ideal for use in passively powered sensor networks.

3.2. Introduction

Passively powered devices are becoming increasingly important for a wide range of sensing applications. Also known as remotely powered devices, passively powered devices do not require any internal power source while extracting their power from propagating radio waves, sunlight, mechanical vibration [31, 41], thermal gradients [7], convection flows or other forms of harvestable energy. One of the most popular power extraction methods for passively powered devices is to harvest power from propagating radio frequency (RF) signals [1].

RF powered devices are often used in applications such as structural monitoring where the RF powered devices are embedded into a structure making

battery replacement impossible without destroying the structure. Some applications employing RF powered devices require deployment of these devices in very large numbers thus, making individual node battery replacement impractical.

RF powered devices are often part of telemetry systems to remotely measure and report data back to a central processing unit [42–45]. Devices powered by propagating RF waves are most often used in passive radio frequency identification (RFID) or passive RF tags to replace the bar code as a new form of data collection [1, 2]. Passive RFID tags are typically used in the range of 1-3 meters. Many modern biomedical implants are passively powered with radio waves to prolong the lifetime of the implanted device, and to reduce the chances of infection and chemical instability from the use of batteries [46, 47]. Bionic implants generally operate within close proximity of the base station (typically 1-50 cm) and must be robustly designed since there is little tolerance for error in implanted devices. RF powered devices are also used in ultra-low power sensor networks in remote areas to eliminate the use of batteries in the sensor system and to keep the sensor network free of maintenance [13, 14]. The applications for these sensor networks normally require an operating distance of 3 to 100 meters and they usually have a backup battery in case the power provided by the RF radiation is insufficient. Other applications for RF powered devices include access control, equipment monitoring and even personal identification.

In all of these applications, there must be a power conversion circuit that can extract enough DC power from the incident electromagnetic waves for the passive device to operate. Previously reported far field RF powered devices generally operate from distances of less than 10 meter from the RF source due to the high power loss from RF wave propagation at UHF frequencies [48]. Others previous work achieved sufficient power but provides low output voltage with higher load

current making it inadequate for use in passively powered wireless sensor networks [49]. A highly efficient passive power conversion circuit is needed for long distance passive sensing in distributed sensor networks.

In a far field RF energy harvesting system, RF energy must be extracted from the air at very low power density since the propagation energy drops off rapidly as distance from the source is increased [50]. In free space, the power density drop off at the rate of $\frac{1}{d^2}$, where d is the distance from the radiating source. The available power to the receiver decreases by 6dB for every doubling of distance from the transmitter. With multi-path fading, the power density drops off at a much faster rate than $\frac{1}{d^2}$, it is therefore critical that the power conversion circuit operate at very low receive power to achieve longer operating distance. Rectification circuits for such systems must be optimized to improve on the minimum power-threshold it takes for the system to operate. To overcome this power-threshold, the system requires significantly more efficient circuit and system level design [51].

One of the major challenges to achieving this goal is the relatively high voltage requirement of rectifying circuits currently employed [52, 53, 38]. When the available RF power to the receiver is under 100μW, the available voltage for rectification in the RF to DC conversion system falls below 0.3 V, much too low to overcome the threshold voltage (V_{th}) of conventional rectifier circuits. Alternative solutions must be found to circumvent or diminish the "dead-zone" in voltage rectification and otherwise reduce the effective threshold voltage in standard CMOS rectifier designs.

This dissertation describes highly sensitive and efficient rectifier circuit techniques as well as system level design issues for RF to DC power conversion. Fully passive rectifier circuits are designed in a 0.25μm CMOS technology opti-

mized to operate at very low received power. A receive antenna is designed in a 4-layer FR4 board to maximize power transfer in the system. Section 3.3 provides the system overview of the far-field RF power conversion system and describes the importance of each of the major blocks and design issues in the system. Section 3.4 presents the circuit level design of the far-field RF-DC power conversion system where the different rectifier designs are shown. Section 3.5 provides the design and measurement details for the receive antenna. Section 3.6 describes the overall test setup and experimental results for the full system and compares the results to recently published designs.

3.3. System Overview

When RF powered devices harvest their power from RF wave radiation, a radiating source or base station is required to transmit a high intensity RF signal wirelessly through the air. Fig. 3.1 shows how the system operates as a network where multiple sensors receive their energy from the same power source. The high intensity RF signal is then picked up by a receiving antenna on the sensor and the RF signal is converted to a DC voltage as shown in Fig. 3.2. The DC voltage is stored on a holding capacitor and supplies power to the integrated circuits.

The RF to DC power conversion system is designed to operate in UHF frequencies in the ISM band of 902-928 MHz. In this frequency range, RF power is transmitted more efficiently for longer distances and experiences lower propagational losses than higher frequency bands (i.e., 2.4 GHz). The system is optimized to operate at distances above 10 meters, with load current below 1 μA, and with the capacity to store charge for long periods of time. Given that the power density drops off at the rate of $\frac{1}{d^2}$ in free space, the propagational RF signal loss through
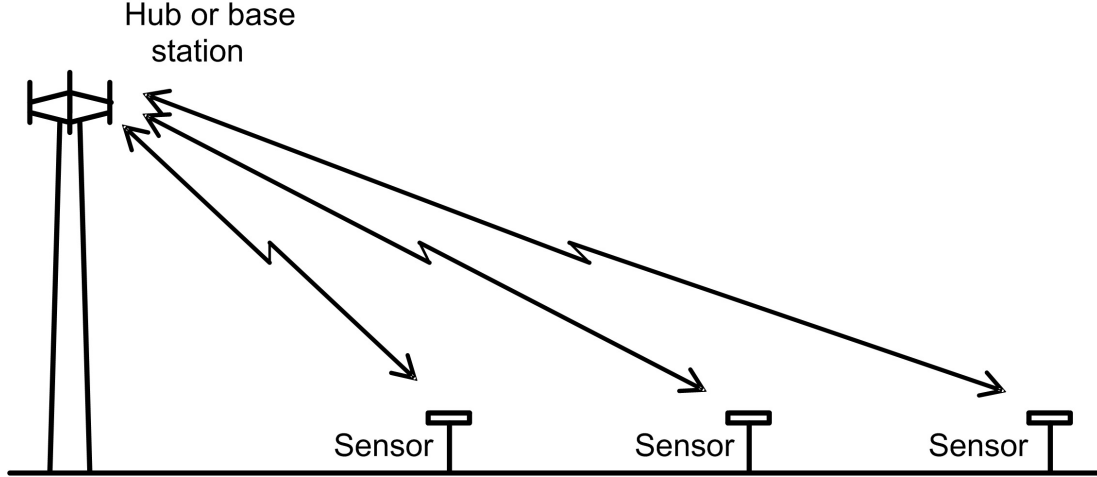
FIGURE 3.1. Illustration of communication links between base station (hub) and sensors in a passively powered sensor network.

the air at 915 MHz can be calculated to be 51.6 dB with the Friis equation for freespace loss [17]. The maximum transmit power allowed by the FCC in the 902-928 MHz band is 36 dBm equivalent isotropically radiated power (EIRP) (30 dBm maximum transmit power with 6 dB antenna gain) [16], thus the received power for distances greater than 10 meters is below 27 μW, this translates to less than 75 mV in a 50 Ω matched system. The power conversion circuit must be highly sensitive for long range operation, thus the threshold voltage of the system must be greatly reduced to improve power conversion efficiency at distances greater than 10 meters. It is also essential to come up with design techniques at the system level that can increase the voltage available for rectification to further increase the power conversion efficiency.
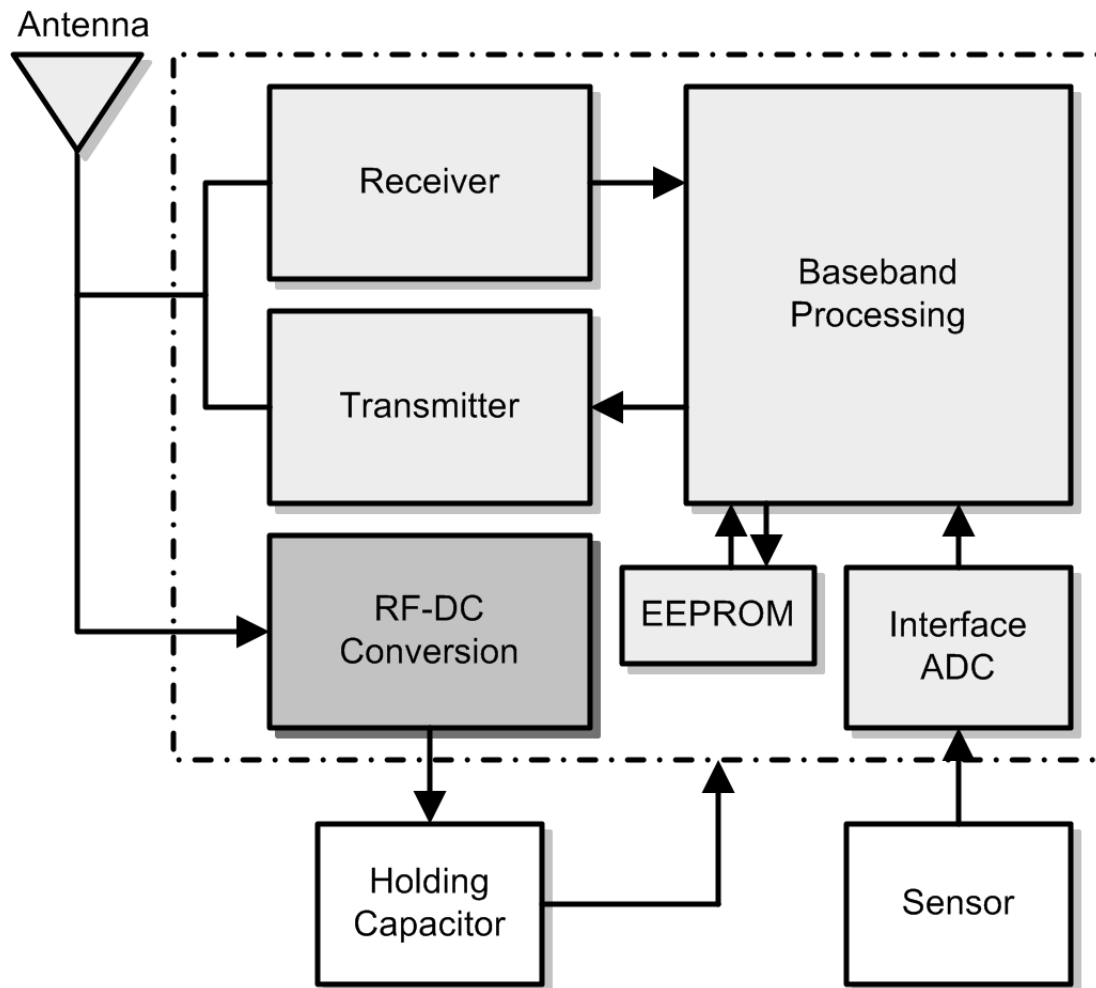
FIGURE 3.2. Block diagram illustrating the RF-DC power conversion system in a passively powered sensor.

An RF-DC power conversion system is designed to passively amplify the voltage available for rectification by forming a high-Q resonator. The main intent of the system is to maximize the voltage coming into the RF-DC power conversion system so that it can provide a stable DC output voltage at ultra-low receive power. The system, shown in Fig. 3.3, consists of an antenna to pick up the power radiated by the RF waves, an impedance matching network to ensure maximum power transfer in the system, and a rectifier circuit to convert the RF signal to a DC voltage. The passive amplification of voltage is done by matching the impedances between the receive antenna and the rectifier circuit. Due to the high-Q nature of the voltage rectification circuit, to be shown later in Section 3.4, the impedance matching creates a high-Q resonator between the receive antenna and the rectifier circuit. The details of each block shown in Fig. 3.3 as well as system level design issues are subsequently discussed to define specifications and limitations of the power conversion system.
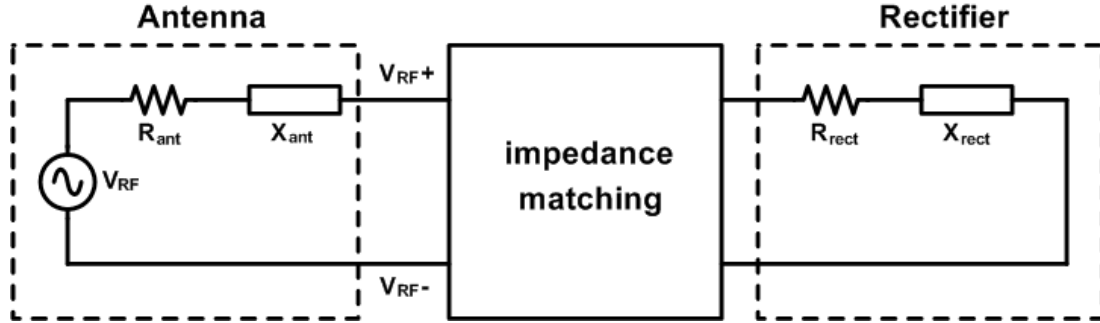
FIGURE 3.3. Passive RF-DC conversion circuit showing the equivalent circuit representation for the antenna and rectifier.

3.3.1. High-Q Resonator

The key method to improve the efficiency of the RF-DC power conversion at the system level is to maximize the input voltage to the rectifier. This is done by forming a resonator with high quality factor, Q, between the impedances of the receive antenna and the rectifier circuit. By doing this, it passively amplifies the incoming RF signal. To ensure the maximum possible power is transferred to the rectifier circuit, the receive antenna impedance is matched to the input impedance of the rectifier circuit [54]. Due to the fact that systems with high-Q resonate with greater amplitude at the resonant frequency than systems with low-Q, the high-Q resonator acts as a passive voltage-amplifier to increase the peak voltage coming into the input of the rectifier without dissipating additional power. The passive voltage gain from the high-Q resonator is directly proportional to its Q. With an increase in the amplitude of the voltage coming to the input of the rectifier, the output voltage of the rectifier also increases and, therefore, increases the overall power conversion efficiency of the system. One drawback of the high-Q resonator is it can reduce the operating bandwidth of the RF-DC power conversion system since

$$Q = \omega * \frac{Energy Stored}{Average Power Dissipated} \tag{3.1}$$

or

$$Q = \frac{f_c}{\triangle f} \tag{3.2}$$

where ω is the resonant frequency in radians/second, f_c is the center frequency of operation, and $\triangle f$ is the 3-dB bandwidth of the system [54]. For the far-field RF-DC power conversion system operating in the band 902-928 MHz, the maximum Q that can be attained without sacrificing bandwidth is 35. This

limitation on the system Q does not cause much concern since on-chip compo-
nents rarely have unloaded-Q of more than 10, and the parasitic resistance from
these components damp out the resonator to prevent the Q of the system from
limiting the bandwidth. In the case of a series connected matched LC resonator,
the reactive components are complex conjugates of each other and the resistive
components are matched. The loaded-Q of the resonator is therefore

$$Q = \frac{1}{2}\frac{\omega L}{R} = \frac{X_L}{2R} \tag{3.3}$$

or

$$Q = \frac{1}{2}\frac{1}{\omega RC} = \frac{X_C}{2R} \tag{3.4}$$

where X_L and X_C are the reactive components, and R is the resistive com-
ponent of the LC resonator. The loaded-Q of the resonator is half the unloaded-Q
of the rectifier and antenna since the resistance in the series connected matched
resonator is doubled. To achieve a high system Q, it is therefore desirable to in-
crease the reactive components of the rectifier and antenna while reducing resistive
components.

3.3.2. Impedance Matching

A matching network between the receive antenna and rectifier is necessary
to fine tune the impedance match between the antenna and the rectifier to further
reduce transmission loss and increase the voltage gain [55, 56]. Coarse impedance
matching is done through circuit and antenna design but fine impedance matching
must also be done on the PCB for more accurate matching. Fig. 3.4 shows the
simulated effect of impedance mismatch for a typical high Q resonator. The max-
imum voltage gain that can be attained is equal to the loaded Q of the resonator,

or half that of the unloaded rectifier Q. With impedance mismatch greater than 7%, the passive voltage gain from the resonator is reduced to below 3 regardless of the resonator Q. With impedance mismatch greater than 15%, the high-Q matching network provides no voltage gain and even yields a voltage attenuation that becomes greater with increasing Q. The impedance mismatch between the antenna and rectifier must be minimized to obtain a high voltage gain.
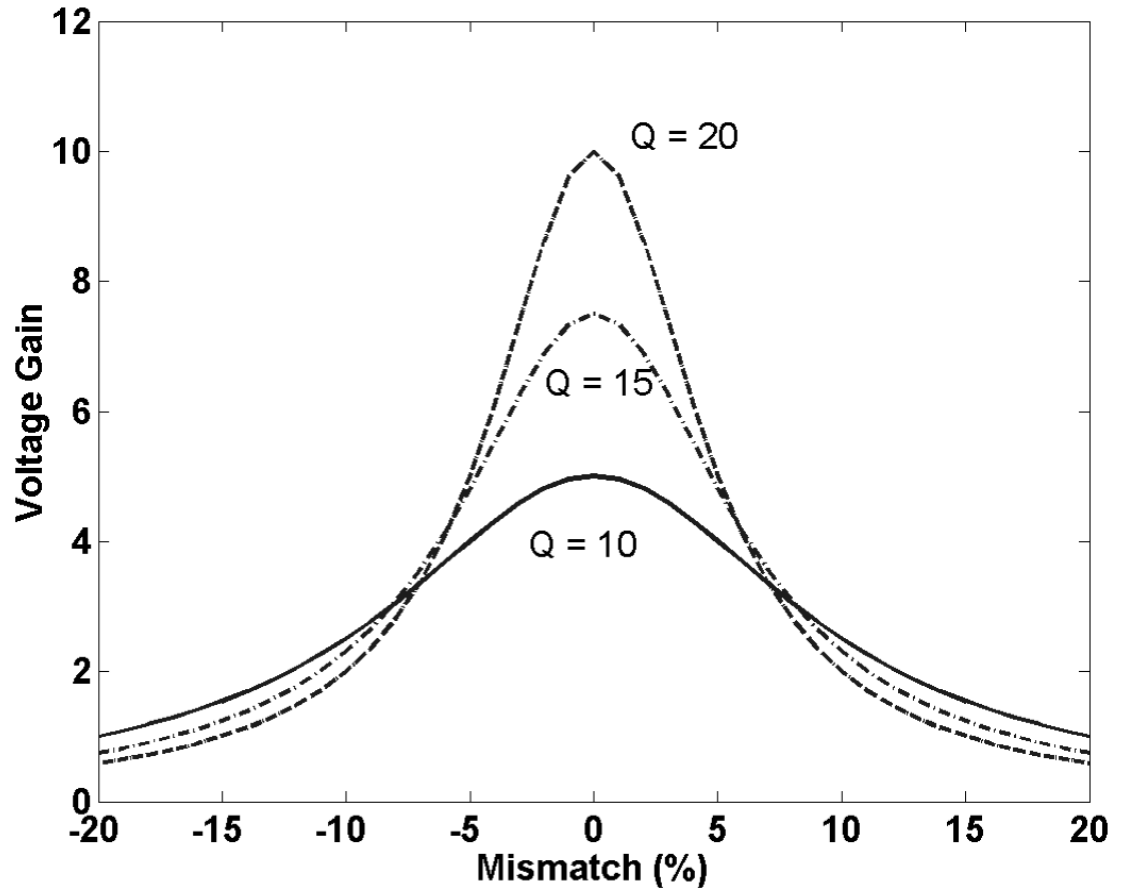
FIGURE 3.4. Effect of impedance mismatch in high Q resonators.

3.3.3. Rectifier Circuit

From the top level block diagram, the rectifier circuit is modeled by an impedance with a real part R_{rect} and a reactive part X_{rect} (Fig. 3.3). From the system point of view, the rectifier circuit must be designed to reduce threshold voltage loss (V_{th}) as much as possible to improve the efficiency of the RF-DC power conversion system. The rectifier circuit must also be designed so that the output voltage can be scaled by cascading multiple rectifier stages in series. Improving the Q of the rectifier input impedance is essential to increasing the power conversion efficiency of the overall system. The rectifier input impedance Q should also be kept as high as possible and parasitic components in the rectifier must be kept as low as possible to maintain a high overall system Q and thus power conversion efficiency.

The number of cascaded rectifier stages in the RF-DC conversion system also has a significant effect on the rectifier input impedance. In a conventional voltage rectification circuit design in CMOS technology, the rectifier impedance as seen from the input is capacitive and resistive due to the gate capacitance and the channel resistance (r_{ds}) of the MOS transistor [57]. In general, cascading multiple rectifier stages in series causes capacitive components to increase linearly with the number of stages while providing parallel paths causes the resistive component to decrease. With a large number of stages, the resistive component from the rectifier is so low that it is dominated by other sources of parasitic resistance (i.e. drain and source connection resistors) and hence, the Q of the system is reduced due to a linear increase in parasitic capacitance.

If there are too few rectifier stages in cascade, the output voltage of the rectifier may not be high enough to operate the sensor node. As the number of

rectifier stages increases, the DC output voltage increases until the number of rectifier stages reaches an optimal point. Adding more stages beyond the optimal point reduces the system Q and causes a reduction in the DC output voltage. Thus, it is critical for the number of rectifier stages to be selected through extensive circuit simulation so that the output DC voltage is maximized while maintaining a high system Q to achieve maximum power conversion efficiency.

3.3.4. Parasitic Components

A major design issue at the board level is reduction of the unwanted parasitic components that affect system performance. Since the system is to be designed with a high-Q resonator, any additional parasitic components between the antenna and rectifier will greatly diminish the performance of the power conversion system. It is therefore critical to specify an accurate parasitic model for simulating the effect of all parasitic components that affect power conversion efficiency. In the design of the RF-DC power conversion system, the traces connected to inputs of the rectifier are most sensitive to parasitics since a high-Q resonance is required at these inputs. Fig. 3.5 shows the equivalent circuit model for the parasitic components that affect the power conversion efficiency of the rectifier circuit. The impedance values are extracted from circuit simulation and typical values of bondwire, package and impedance trace models.

These parasitic components cannot be avoided altogether, but the value of each parasitic component can be reduced through careful layout and package selection. The bond pad can be designed to be minimum size and only consisting of the top two metal layers to reduce bond pad capacitance to the substrate. The package for the integrated circuit is selected so that pin parasitics are minimized
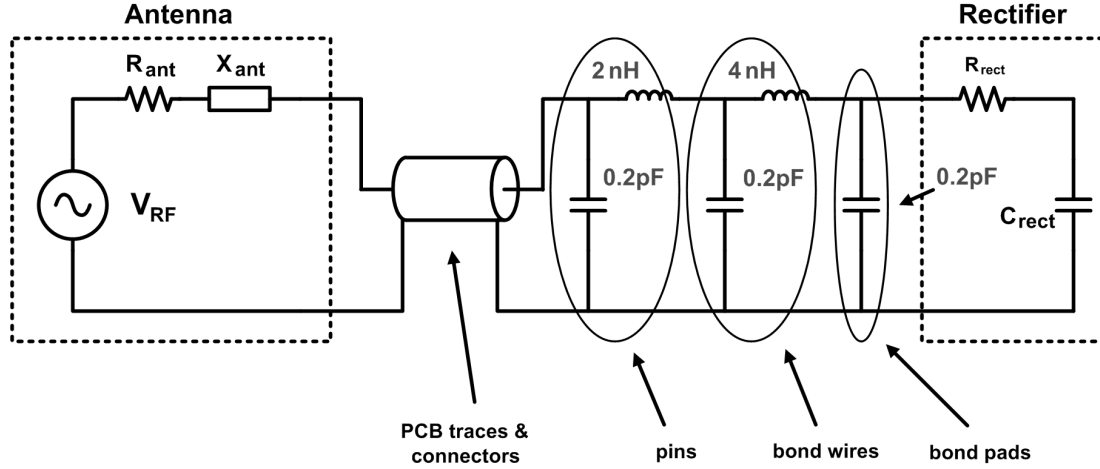
FIGURE 3.5. Parasitic components that affect performance of the RF-DC power conversion circuit.

and critical input pins are placed in locations where the length of bond wires is minimized. PCB traces are made as short as possible and they are impedance controlled to reduce the parasitic capacitance and inductance.

3.3.5. Receive Antenna

The antenna design is critical in the RF-DC power conversion system since it must extract the power radiated by the RF waves. The antenna performs best when it is impedance matched to the rectifier circuit at the operating frequency to reduce transmission loss from PCB traces. Also, the antenna must be small in area and must have a bandwidth large enough to cover the frequency band from 902-928 MHz. More details of the specific design employed here is given in Section 3.5.

3.4. Rectifier Design

A study of different rectifier designs is done and the voltage doubler rectifier configuration is chosen [58]. Figure 3.6 and 3.7 shows the conventional voltage doubling rectification circuit and the proposed floating-gate rectification circuit. For the floating-gate rectification circuit, floating-gate devices are used to create a gate-source bias to reduce the threshold voltage loss of the MOS transistor.
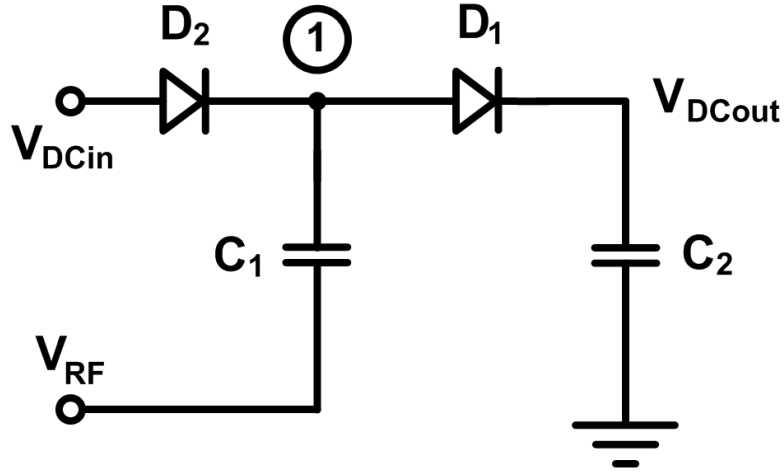
FIGURE 3.6. Conventional voltage doubler rectifier.

3.4.1. Conventional Voltage Doubler Rectifier

The voltage doubler rectifier structure is considered for the design of the RF-DC power conversion system because it rectifies the full-wave peak-to-peak voltage of the incoming RF signal and it can be arranged in cascade to increase the output voltage. The voltage doubler rectifier in Fig. 3.6 consists of a peak rectifier formed by D_1 and C_2 and a voltage clamp formed by D_2 and C_1 [38].
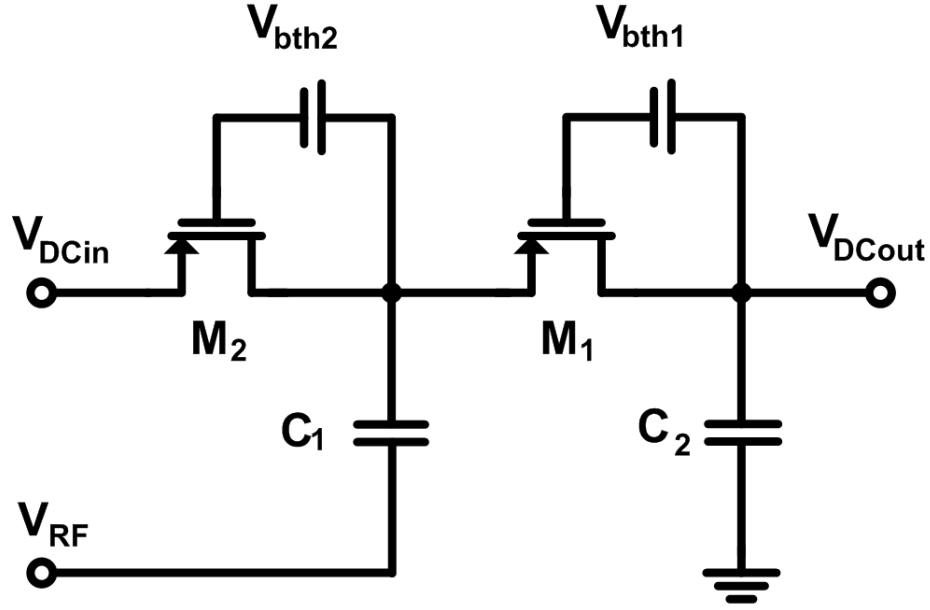
FIGURE 3.7. PMOS floating-gate rectifier.

The voltage clamp and the peak rectifier are arranged in cascade configuration to provide a passive level shift in voltage before rectification.

In the negative phase of the input, current flows through diode D_2 while D_1 is cutoff. The voltage across diode D_2 stays constant around its threshold voltage and the voltage at node 1 is charged to -V_{th2}. At the negative peak, the voltage across capacitor C_1 is $V_{amp} - V_{th2}$ (where V_{amp} is the amplitude of the input signal.) In the positive phase of the input, current flows through diode D_1 while D_2 is in cutoff. The voltage across capacitor C_1 remains the same as the previous phase because it has no way to discharge. At the positive peak, the voltage across D_2 is $2V_{amp}$ V_{th2}. Since D_1 is conducting current to charge C_2, the voltage at the output is a threshold voltage below that across D_2, i.e., the voltage at the output V_{out} is $2V_{amp} - V_{th2} - V_{th1}$.

3.4.2. Floating-Gate Voltage Doubler Rectifier

The floating gate devices may be designed to passively reduce the threshold voltage of the rectifier circuit. In a floating gate device, when charge is injected into the floating gate of the transistor, it remains in the gate oxide because of the high impedance provided by the oxide layer. There are previous methods designed to compensate for the threshold voltage drop in voltage rectification circuits [61, 63]. The threshold reduction method shown in [61] requires the input voltage to be sufficiently large to start up the circuit. This method also requires a bias resistor R_b which generally has resistance in the megaohm range (i.e. large physical size). Although the static power dissipated from this resistor is minimal, it causes a bias voltage much less than the desired threshold voltage. The voltage drop across a diode tied transistor under 10 nA bias is much different than one drawing 10 μA of current, this voltage difference is typically 100 mV for every decade of current difference, yielding effective threshold of few hundred millivolts. The threshold reduction technique in [62] suffers from the same constraint, as it uses diode-tied transistors biased at 2 nA to generate bias voltages for diode-tied transistors drawing current in the microamp range. This method would also require extra circuitry to generate a voltage bias and differential clock which requires a secondary battery. Zero-threshold transistors may also be used for voltage rectification but they only have zero threshold for a small current range. The floating-gate rectifier technique allows the threshold of the rectifier circuits to be programmed and can be optimized to operate over a wide range of output current. For the floating-gate rectifier circuit, the overall rectifier architecture is the same as the voltage doubler rectifier circuit. The diodes D_1 and D_2 are

replaced by diode-tied floating gate transistors. The gate oxide is a very good insulator which keeps the charge from leaking off in the floating gate [59].

To design a floating gate device in a standard CMOS process, a MOS capacitor is placed in series with the gate of the diode-tied transistor as shown in Fig. 3.8. The gate of the diode-tied transistor and the gate of the MOS capacitor are connected together to form a high impedance node to trap charges in the floating gate. The charge in the floating gate is therefore fixed which results in a fixed voltage bias across the MOS capacitor. The charges that are trapped inside the floating gate device act as a gate-source bias to passively reduce the effective threshold voltage of the transistor.
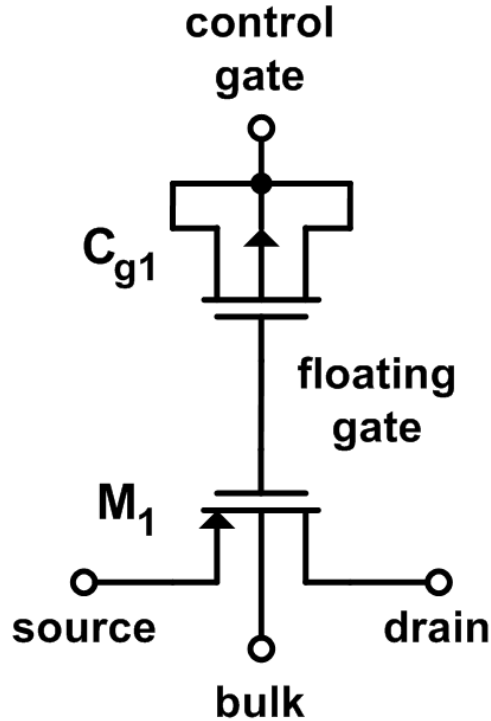
FIGURE 3.8. PMOS implementation of a floating gate transistor.

The floating-gate devices need to be initially programmed to reduce the threshold voltage of he rectifier, thus enhancing the power conversion efficiency. The charge on the floating gate can be injected via Fowler-Nordheim (F-N) tunneling when the rectifier is not operating, or it can be charged by injecting a relatively large sinusoidal signal to the input of the rectifier at any time. The Fowler-Nordheim tunneling technique charges the floating gate to the desired voltage much faster, but the amount of charge is harder to control and also, additional circuitry is needed to inject or remove charge from the floating gate. Similar to programming a non-volatile Flash EEPROM, the programming node is driven by a high voltage pulse to force a sharp bend in the energy band diagram of the floating-gate device. This enables charge to enter the insulated floating-gate by means other than the mechanism of F-N tunneling. The applied programming sinusoidal input voltage has amplitude larger than the threshold voltage of the transistor used for rectification. Charge is injected into the floating gate via the parasitic capacitance between the gate-source and gate-drain junction of the transistor and by hot electron effects. The large sinusoidal signal is externally generated and applied directly to the input of the rectifier until the output reaches an optimal point. If the floating-gate node is over charged, a negatively biased sinusoidal wave may bring it back to the optimal point. The sinusoidal signal can be applied in pulses with peak voltages between 5-6 V with 2.5-3.0 V DC bias or by a continuous train of signals at lower voltages and bias, depending on the duration of the pulse train.

The programming pulse does not need to be sinusoidal, but as the pulse is applied to the input node (which is high-Q), the pulse will be transformed to more of a sinusoidal signal. By applying a sinusoidal signal, the amplitude of the applied pulse can be better controlled. In this work, all floating-gate programming node

are capacitively coupled and can be programmed simultaneously from the same programming pin, with all other circuitry grounded, via F-N tunneling technique, and by the application of the sinusoidal signal at the input nodes when the rectifier is operating. The floating-gate rectifier is programmed with iterations of 20 pulses with 5 ms trigger, 5 V amplitude and 2.5 V DC offset and repeat until the output voltage is at the maximum point for a wide range of current. If the floating-gate is over charged, 10 deprogramming pulses with 5 ms trigger time, -6 V and -3.0 V DC offset are injected to the programming node to recover charge on the floating-gates.

With the floating-gate device, the threshold voltages of the diode-tied transistors M_1 and M_2 are reduced by creating a gate-source bias. The gates of transistors M_1 and M_2 in Fig. 3.7 are high impedance nodes so any charge trapped in the floating gates can be retained for a long time. Retaining charge in floating-gate devices is critical to the useful lifetime for the power conversion circuit under discussion. With the 70 angstrom oxide thickness in the 0.25-μm CMOS process, the device retains charge in the floating gate in excess of 10 years for normal operation at room temperature [64]. However, the performance of the rectifier circuit may reduce slightly as charge is leaked from the floating gate. During fabrication, the residual charge trapped in the floating gate may also affect the threshold voltage of the rectifier circuit, hence the floating gate must be programmed to account for these residual charges. Removal of residual charge may be done initially with the F-N tunneling method, which is a high voltage pulse applied to a separate control gate of the floating-gate device.

The transistor level schematic of the 36-stage floating-gate rectifier is shown in Fig. 3.9. V_{RF} represents the input signal extracted from the RF wave, V_{DCin} is the input DC voltage coming from the previous rectifier stage and V_{DCout} is

the output DC voltage of the rectifier. The 36-stage design uses diode-tied PMOS transistors as rectifying devices and a MOS capacitor (MOSCAP) is used to create the gate-source bias for each individual diode-tied transistor in the rectifier. The MOSCAPs (C_{g1} and C_{g2}) are designed to operate for the most part in the depletion region and their capacitance is a function of the applied voltage. To create the gate-source bias, a large sinusoidal signal is applied at the input of the rectifier and charge is injected over time through the parasitic capacitance of the diode-tied transistors. When the gate-source bias reaches a potential close to V_{th}, the capacitance reaches a flat point and remains constant. The amount of charge stored in the floating gate reaches equilibrium and the MOSCAP operates in the inversion region, the source-gate bias voltage is, therefore, approximately the threshold voltage of the diode-tied transistors (M_1 and M_2).

FIGURE 3.9. Transistor level schematic of PMOS floating-gate rectifier.

3.4.3. Multistage Rectifier Circuit

The individual stages of the floating-gate voltage doubler rectifier circuit can be arranged in cascade to increase the output voltage of the rectifier [52, 65, 66]. Fig. 3.10 shows N stages of a voltage doubler rectifier in cascade. When the rectifier stages are cascaded, each rectifier stage acts as a passive voltage level shifter in addition to the voltage shift in voltage clamp and peak rectification. The number of rectifier stages used in the design is important since too few rectifier stages yields insufficient output voltage and too many rectifier stages damps out the effect of the high-Q resonator.

One of the important tradeoffs in the design of the voltage doubler rectifier is the size of the transistor versus parasitic capacitance [67, 68]. The smaller the transistor size, the less parasitic capacitance it has, however, rectification efficiency is lowered by the smaller transistor size since smaller transistor can deliver less current to the load. The transistor sizes can be reduced to a few times the minimum width to reduce parasitic capacitance as seen from the input of the rectifier, however, the reduction in channel width may cause a decrease in the performance of the rectifier due to the increase in the channel resistance of the diode-tied transistors. Two different designs are implemented to compare the tradeoffs between a reduction in the parasitics and the rectifier performance.

3.4.4. Rectifier Designs and Optimization

Two designs in a 0.25 μm CMOS process are evaluated to illustrate the tradeoffs in the design. The first design uses a relatively large device size of 12μm$/0.24\mu$m (NMOS) and the second uses 2μm$/0.24\mu$m PMOS devices. The larger device-size, NMOS floating-gate rectifier is first designed to test the func-
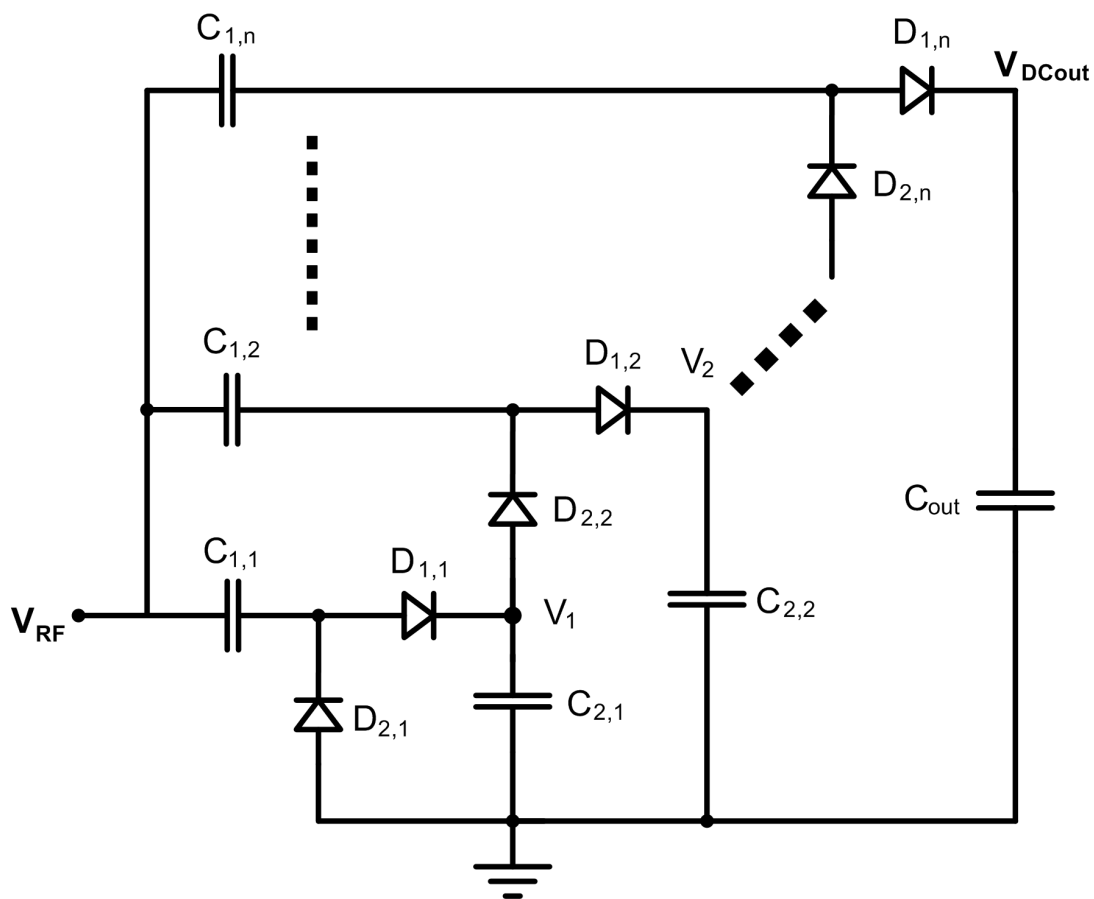
FIGURE 3.10. Voltage doubler rectifier with N-stages in cascade.

tionality of the floating-gate rectifier circuits while the smaller device-size, PMOS rectifier is a follow-up design to improve the performance of the RF power conversion circuit for longer distance operation. The PMOS rectifier is designed with smaller device sizes to decrease the parasitic capacitance for each stage and consequently to increase the number of rectifier stages. This leads to a higher output voltage and longer operating range. Also, the PMOS transistor is chosen over an NMOS transistor to reduce the variation of threshold voltages between the different rectifier stages due to body effect. Fig. 3.11 shows the maximum voltage gain that can be achieved in the rectifier with different numbers of floating-gate rectifier stages arranged in cascade. As the number of rectifier stages increase, the resonator Q between the antenna and rectifier impedance is reduced. In fact, the resonator Q is inversely proportional to the number of rectifier stages.

The output voltage of the rectifier for both designs with an input voltage with 300 mV amplitude is shown in Fig. 3.12. The output voltage initially increases as more rectifier stages are added until an optimal point then it reduces as the resonator Q is decreased. The impact of the number of rectifier stages on the input impedance is shown in Fig. 3.13. As the number of rectifier stages increases, the capacitive component in the rectifier input impedance increases thus reducing the reactive component of the rectifier input impedance. The reactive component of the rectifier input impedance is found to be inversely proportional to the number of rectifier stages. With the decrease in the reactive component, the maximum voltage gain that can be achieved at the input is also decreased at the same rate since the resistive component in the input impedance stays fairly constant.

The optimized number of cascaded rectifier stages for the 12 μm (NMOS) and 2 μm (PMOS) designs is 16 and 36 stages, respectively. The simulated input

impedance for the two designs is 6.6 - j85 Ω and 6.6 - j84 Ω, almost identical to each other.
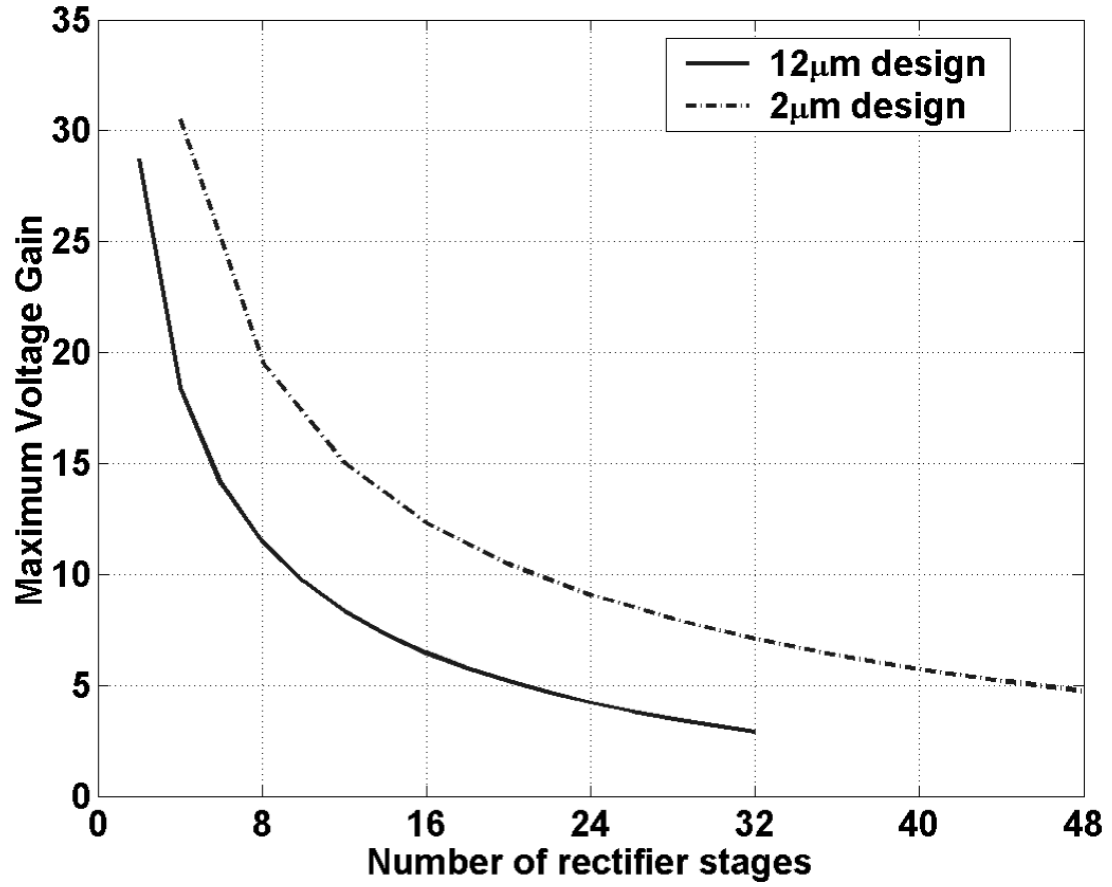
FIGURE 3.11. Effect of number of rectifier stages on maximum voltage gain.

To establish the tradeoff between the transistor sizes used for rectification versus the number of rectifier stages, a model is extracted by curve fitting of the output voltage data for the two different designs. Figure 3.14 shows a 3 dimensional surface plot for the rectifier output voltage as a function of the number of rectifier stages and the transistor width. It can be observed that a width of
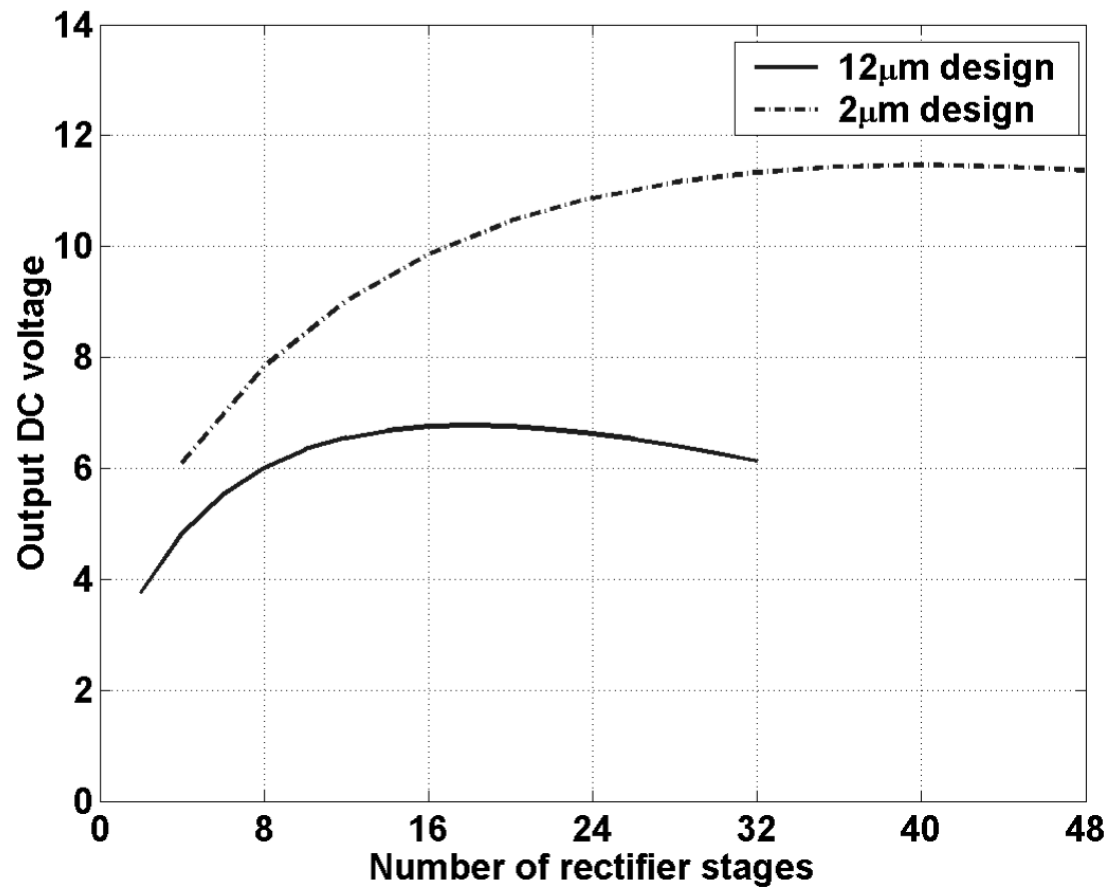
FIGURE 3.12. Effect of number of rectifier stages on output DC voltage.
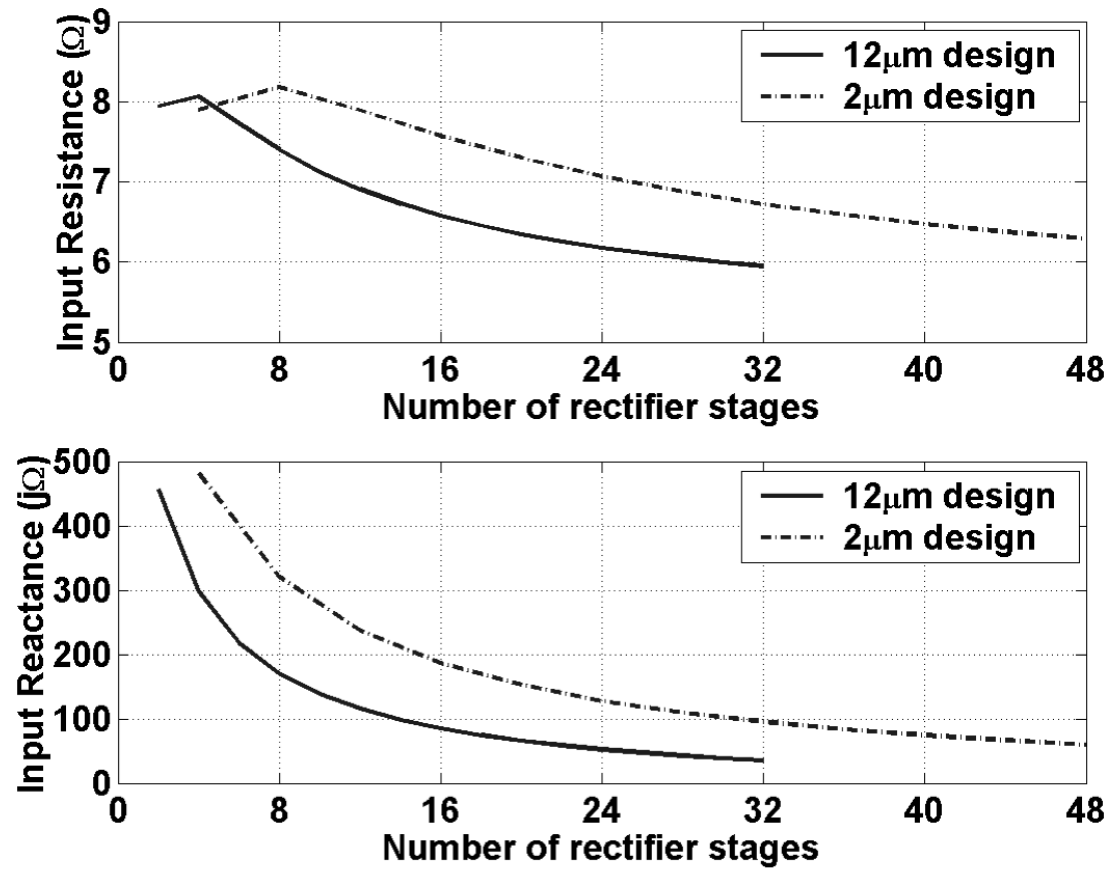
FIGURE 3.13. Effect of number of rectifier stages on input impedance of rectifier.

2 μm is the best design choice for the highest output voltage when the number of rectifier stages is below 40. Any increase in device size from 2 μm results in a reduction in the output voltage. Reducing the device size below 2 μm could lead to a slight improvement in the output voltage. However, the number of rectifier stages required is significantly increased which results in a larger die size. Figure 3.15 shows the constant output voltage contour plot as function of the transistor width and the number of rectifier stages. The 36 stage design with a 2μm device size is very close to the highest voltage contour, thus, this design is optimal for the output voltage.
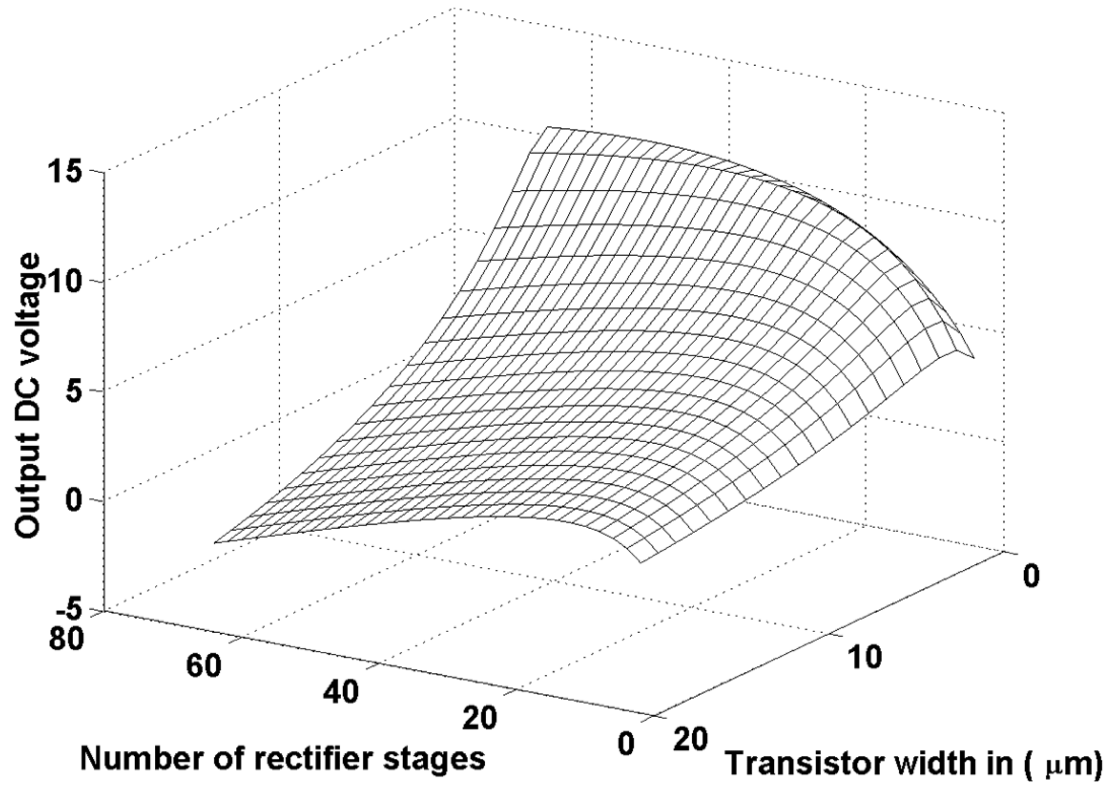
FIGURE 3.14. Output voltage curves as function of the number of rectifier stages and the transistor width.
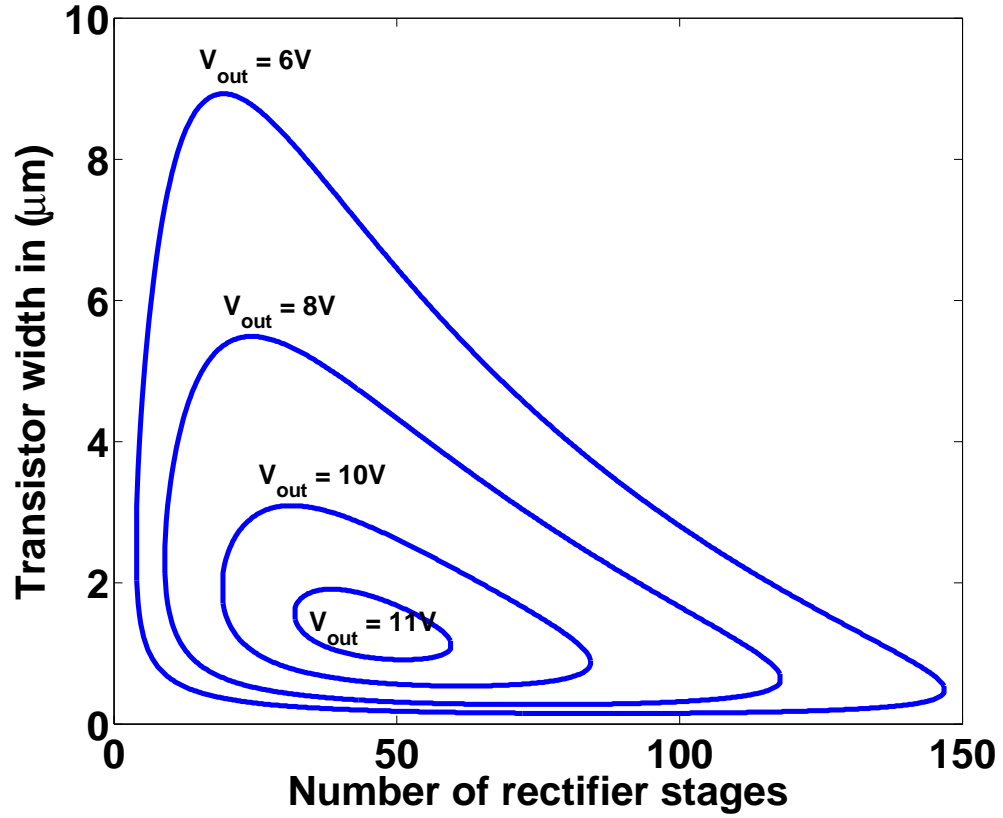
FIGURE 3.15. Contour plot of constant output voltage.

3.5. Antenna Design

The antenna for the RF-DC conversion circuit is designed with meander lines on a printed circuit board to reduce the area of the antenna and to provide the desired antenna input impedance to the impedance matching network. Figure 3.16 shows the antenna design with two outer loops on each side connected to an inner loop in the center. The antenna ports are in the middle of the design and connect to the antenna through the inner loop to transform the impedance

as seen from the outer loops of the antenna. To achieve resonance at the desired frequency, the antenna is designed to have its impedance match with the input impedance of the floating-gate rectifier circuit. The outer loop of the antenna is designed to tune the antenna to the correct operating frequency and the perimeter of the loop is 35 centimeters, roughly equal to one wavelength at 916 MHz. The perimeter of the inner loop varies depending on the value of the input impedance of the rectifier. The line of symmetry between the two sides of the antenna splits the antenna into two identical parts and this line of symmetry acts as a virtual ground to create the fully differential signal at the antenna ports. The dimension of the drawn area of the antenna is 15 cm x 2 cm (6 x 0.8 inches).

The antenna design is tuned for maximum received power at 916 MHz and the antenna is designed on the top layer of a 4-layer FR4 board with carefully controlled impedance to ensure the impedance of PCB traces does not vary from the intended values. The traces in the antenna are exposed so that they can be tapped to fine tune the operating frequency. The impedance matching network can be placed anywhere along the antenna to fine tune the matching between the antenna and the rectifier circuit. The antenna is designed with a bandwidth of about 40 MHz to maintain a high antenna Q. Due to the fact that the antenna must be impedance matched to the rectifier, the loop design provides little antenna gain in the antenna throughout the frequency bandwidth it operates.

Figure 3.17 shows the simulated and measured input impedance of the antenna around the operating frequency band. The antenna is designed and simulated in Momentum 3-dimensional planar electromagnetic simulator that is part of the Advanced Design System (ADS) design flow. The measured resistive component shows less than 1Ω variation from the simulated value and the reactive component also correlates well with the simulated results. The measured input
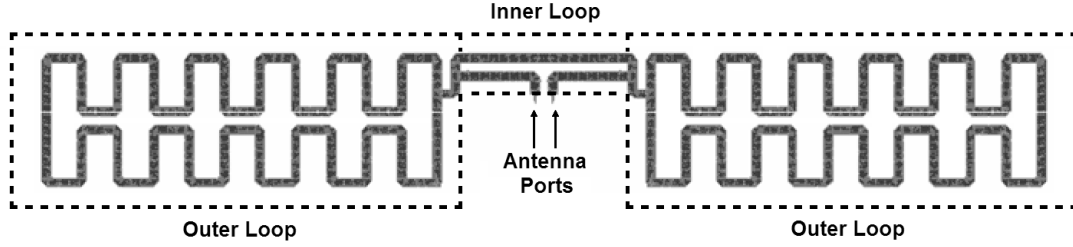
FIGURE 3.16. Antenna design for RF-DC converter.

impedance components of the receive antenna for the 36-stage rectifier design are shown in Figure 3.18. The measurement of both the antenna and rectifier input impedeance is done on an S-parameter network analyzer calibrated with a 50Ω broadband load. The reactance component for the rectifier is capacitive while the reactance for the antenna is inductive. From the measurement data, the measured resistive components of the antenna and rectifier match well throughout the intended bandwidth for both designs. The reactive component of the 36-stage design matches at 910 MHz.

Figure 3.19 and 3.20 shows the plot of the return loss (S_{11}) and voltage gain, respectively, for the 36-stage design. The antenna is designed to match well enough so that less than 1% of the transmitted signal is reflected back to the antenna (i.e. S_{11} below -20 dB) in the frequency band of operation 902-928 MHz. The design achieves voltage gain above 5 in a 30 MHz bandwidth, however the peak voltage gain is shifted down by approximately 10 MHz from the intended 915 MHz center frequency. In the design of the antenna, only the impedance matching between the antenna and the rectifier input is considered. If further optimization
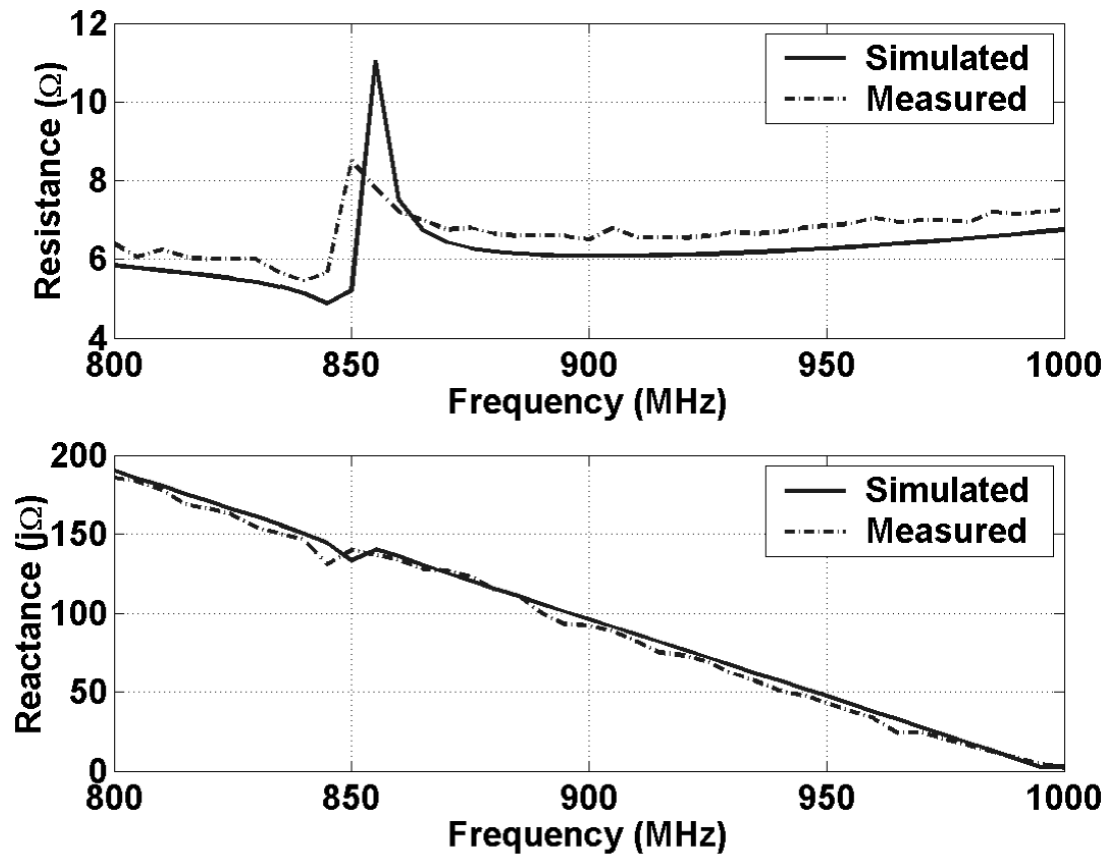
FIGURE 3.17. Simulated and measured components of the antenna input impedance.
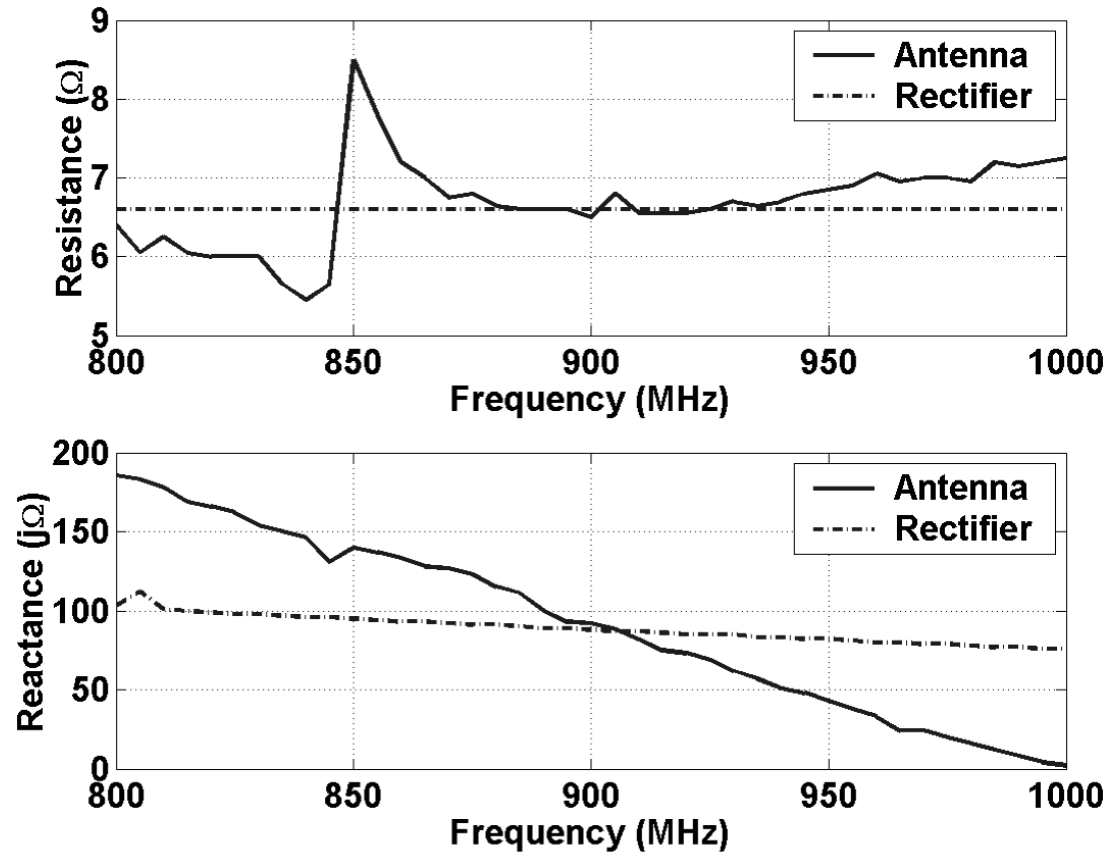
FIGURE 3.18. Measured input impedance of antenna and rectifier circuit.

is done to enhance the antenna gain and efficiency, the performance of the power conversion system can be increased.
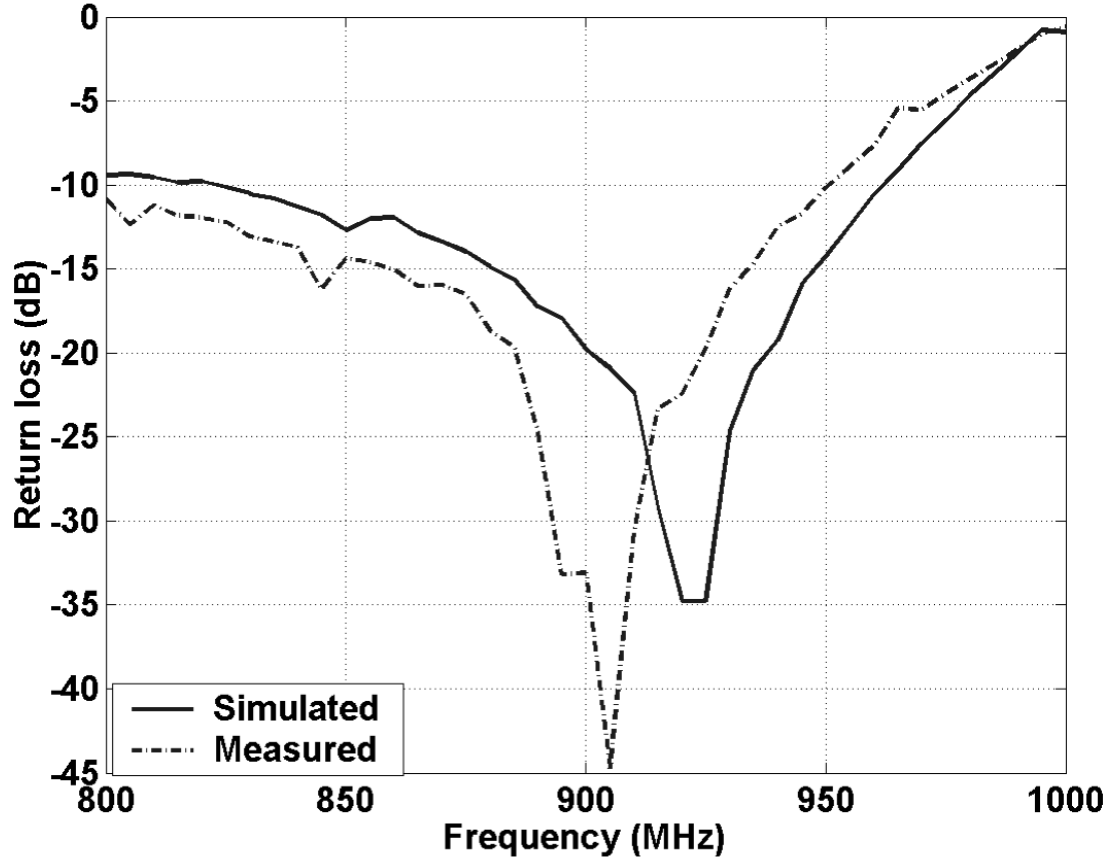
FIGURE 3.19. Measured return loss for 36-stage rectifier design.

3.6. Experimental Results

3.6.1. RF-DC Rectifier Circuit Performance

Rectifier designs with 16 NMOS stages and 36 PMOS stages were fabricated in a 0.25μm 5 metal single-poly CMOS process as shown in Fig. 3.21 and
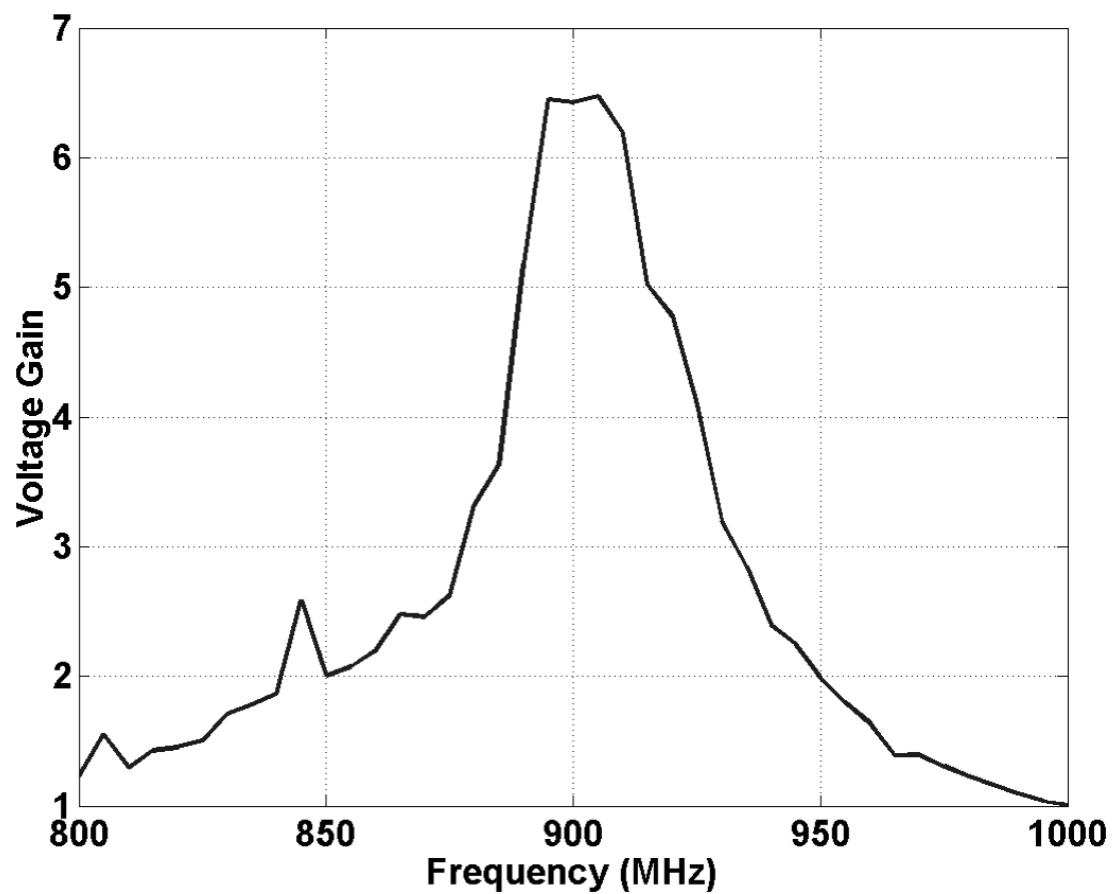
FIGURE 3.20. Voltage gain for 36-stage rectifier design.

3.22, respectively. The active die areas are 350μm x 600μm and 400μm x 1000μm, respectively. The majority of the active area is consumed by the MOSCAPs for floating gate devices and the holding capacitors. The 16-stage and 36-stage rectifier layouts are arranged in two rows of 8 stages each and six rows of 6 stages each, respectively. Both dies have a pair of 1-stage rectifiers included so that the functionality of the NMOS and PMOS diode-tied floating-gate devices can be individually characterized. Each rectifier is packaged in a 0.5mm pin pitch QFN-32 package to reduce bond wire parasitics and trace lengths on the PCB.
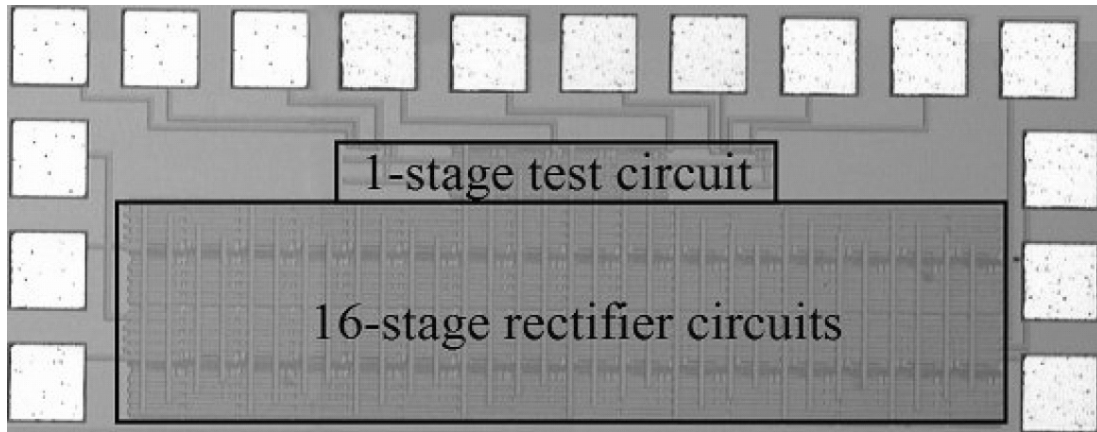
FIGURE 3.21. Die photograph of 16-stage rectifier circuit fabricated in a 0.25μm CMOS process.

In order to test the rectifier circuit, a small amplitude 1 MHz sinusoidal signal is applied directly to the input. The low frequency signal is used to minimize parasitic effects introduced by the board as well as voltage losses in the PCB traces. The purpose of this experiment is to quickly obtain the desired output voltage characteristics of the floating-gate rectifier using a controlled input signal so the floating-node can be more easily programmed to reduce the threshold voltage of the rectifying transistors. At 900MHz, the rectifying transistor output voltage is
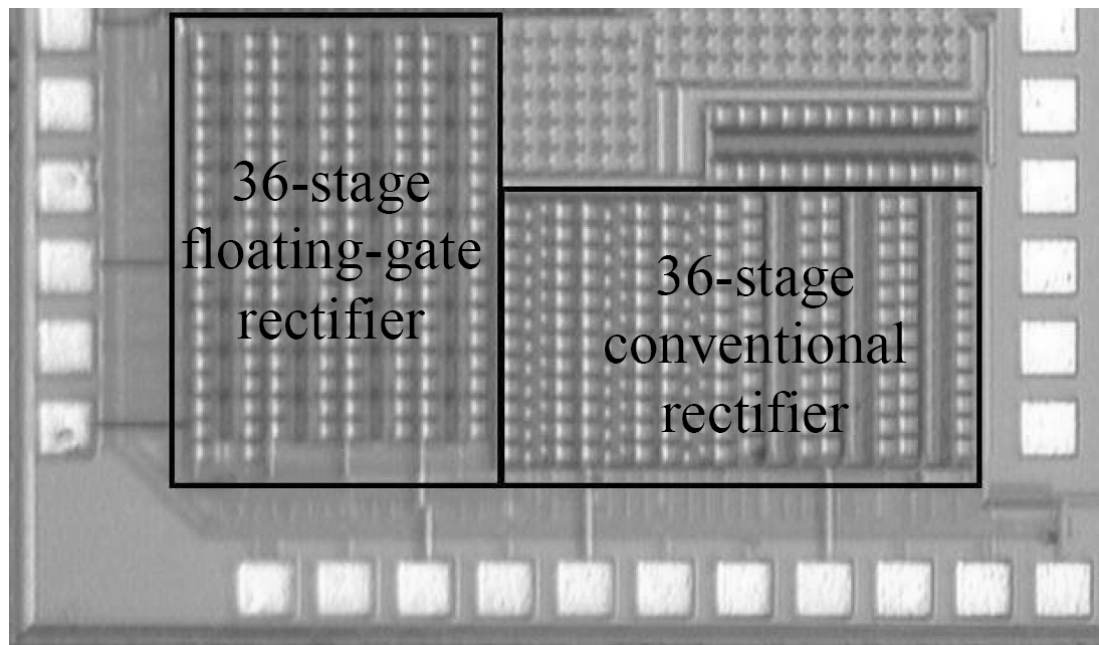
FIGURE 3.22. Die photograph of 36-stage rectifier circuit fabricated in a 0.25μm CMOS process.

reduced by approximately 1 mV/stage due to the delay in the diode response. The threshold voltage of the PMOS and NMOS transistors are approximately 550 mV and 450 mV, respectively, before the injection of charge. After charging the floating gate, the effective threshold voltage for both is between 30-50 mV. This can be seen in Figure 3.23 as a sharp increase in the output voltage is observed in this voltage range. Fig. 3.23 shows the measured output DC voltage unloaded and with a 5 MΩ load for both rectifier designs as a function of the input sinusoidal amplitude. From a straight line extrapolation of the output voltage curves, the threshold voltage for the 16-stage rectifier is 33 mV compared to 30 mV for the 36-stage rectifier. Since the difference in threshold voltages is very small between the two rectifier designs, the improvement in the output voltage of the 36-stage rectifier is primarily due to the higher number of cascaded rectifier stages used in the design.

The performance of the rectifier circuit can be specified by the sensitivity of the rectifier or the minimum input power required for voltage rectification. The average input power can be expressed as:

$$P = \frac{(\frac{V_{rms}}{Q})^2}{R} = \frac{(\frac{V_{amp}}{Q})^2}{2R} \tag{3.5}$$

where Q is the passive voltage gain from the antenna to the input of the rectifier, Vrms is the input rms voltage to the rectifier, Vamp is the rectifier input amplitude and R is the input impedance of the rectifier circuit. The voltage gain of the 16-stage and 36-stage rectifiers, measured from the return loss of the matching between the rectifier and antenna, is 4.8 and 6.4, respectively. Assuming a rectifier input impedance of 7 Ω, the equivalent input power is derived and shown in Figure 3.24. In the case of the 16-stage rectifier, 2V is achieved for 80 mV input, which is equivalent to a power of 20.95 μW (-16.8 dBm). Using the Friis formula
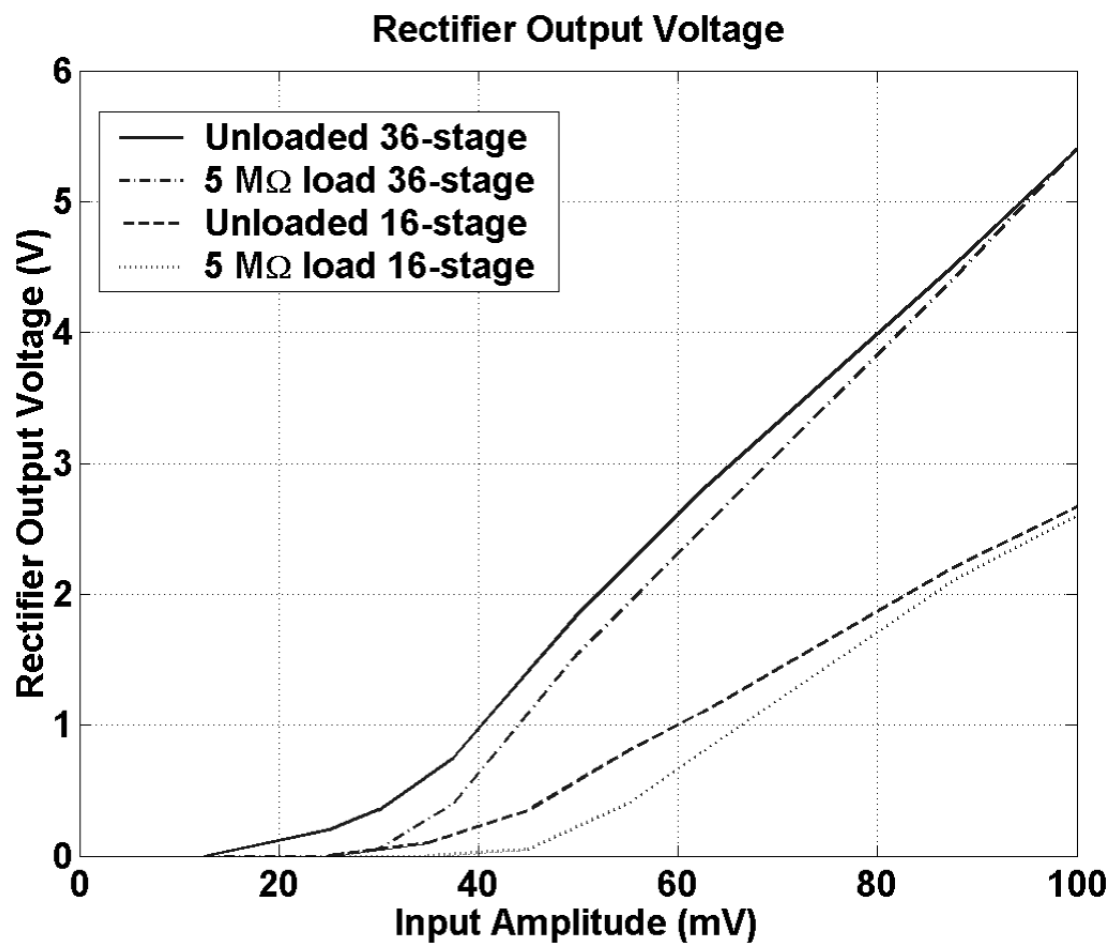
FIGURE 3.23. Measured output DC voltage as a function of the sinusoidal input voltage amplitude.

for free-space wave propagation, this corresponds to an operating distance of 23 meters (Fig. 3.25) assuming a 4W radiating source [16]. This is the maximum theoretical distance that can be achieved with this design while keeping radiated power and antenna gain under the FCC emission limit. For the 36-stage rectifier circuit design, the rectifier performs better with low voltages due to the increased number of voltage doubler rectifier stages and the higher passive voltage gain. The 36-stage rectifier circuit achieves 2V for an input voltage amplitude as low as 50mV. Using (3.5), these values are equivalent to 4.7 μW of power (-23.3 dBm) at 2.0 V output. In free-space, this corresponds to 49 meters in distance.

Table 3.1 shows the transient rise-time of both floating-gate rectifier designs. The transient rise-time is defined as the time it takes for the rectifier output to charge to 90% of the maximum voltage with a 10 μF capacitive load. For the 16-stage floating-gate rectifier, the effective threshold voltage is approximately 36mV. The transient response time of this rectifier is very slow when the input voltage is close to the threshold voltage but increases very rapidly as the over-drive voltage (V_{GS} - V_{TH}) increases, as a result, increasing the driving current. The charging time of the capacitor decreases by a factor of about 3 for every 20 mV increase in input amplitude. For the 36-stage floating-gate rectifier, the effective threshold voltage is approximately 30 mV and the transient charging has the same behavior as the 16-stage rectifier. The transient rise-time of the 36-stage rectifier also decrease by a factor of about 3 for every 20 mV increase in input amplitude as the input amplitude is greater than the threshold voltage.

Defining the voltage efficiency as the percentage of the theoretical voltage achieved [60], the theoretical output for the voltage doubler architecture is the number of cascaded rectifier stages times the peak-to-peak voltage into the rectifier. In the case of the 16-stage rectifier, the theoretical output voltage is 16 times
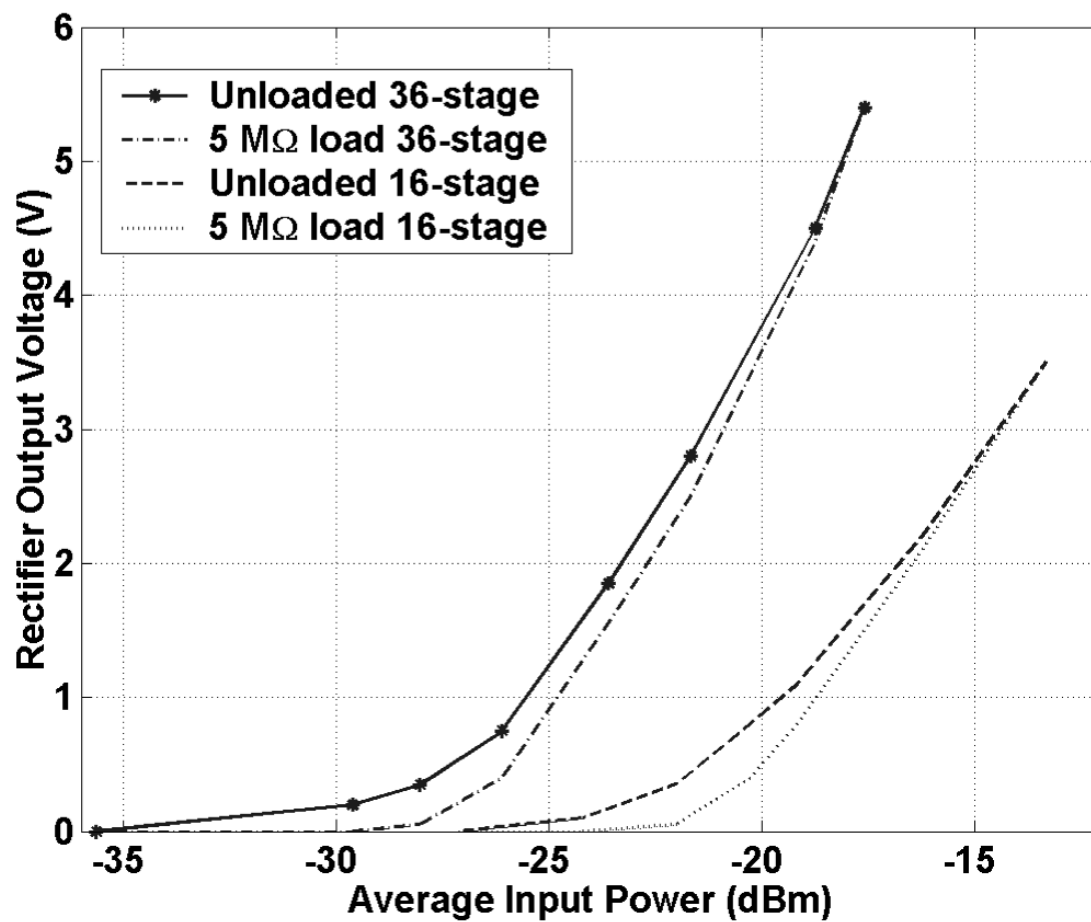
FIGURE 3.24. Measured output DC voltage as function of average input power.
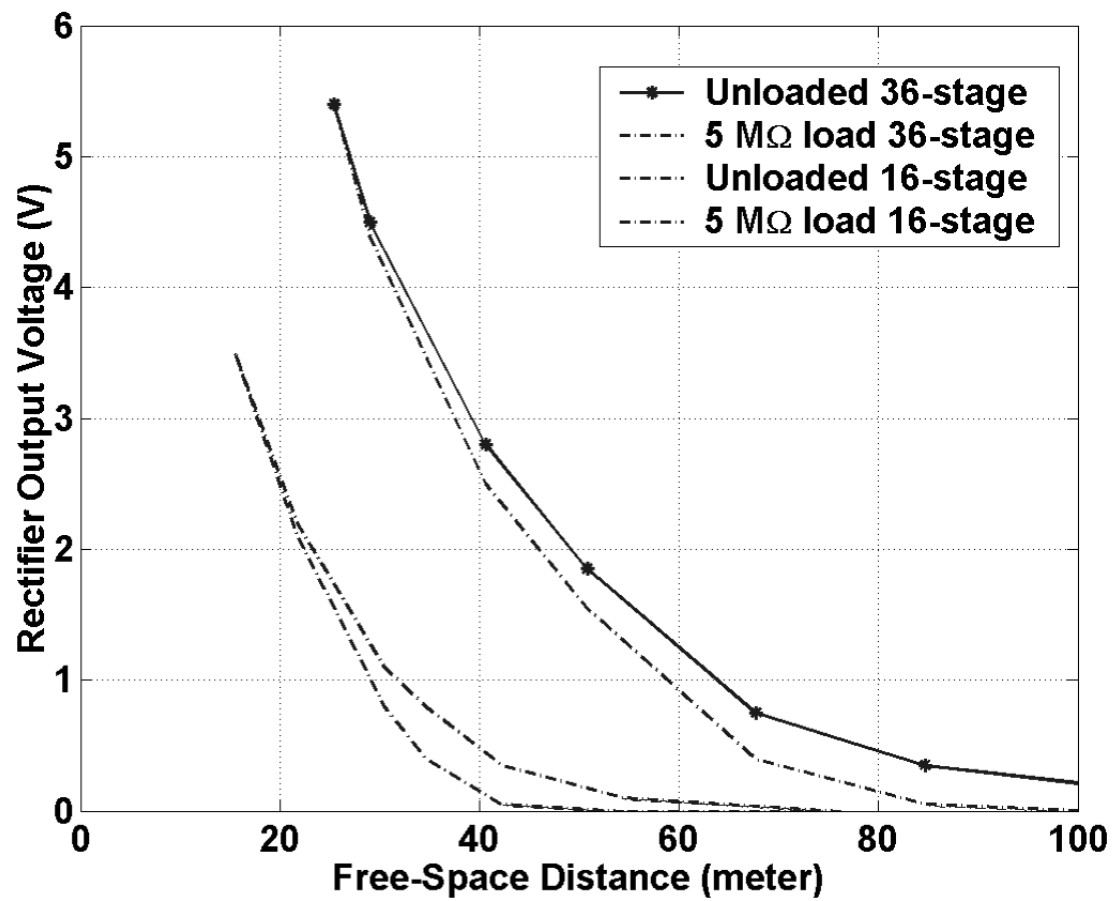
FIGURE 3.25. Measured output DC voltage as function of distance.

Input	16-stage rectifier		36-stage rectfier	
Amplitude	Unloaded	5 MΩ load	Unloaded	5 MΩ load
100mV	1.06 s	1.03 s	2.34 s	2.31 s
80mV	1.84 s	1.81 s	6.34 s	6.01 s
60mV	4.60 s	4.42 s	19.32 s	16.54 s
40mV	96.0 s	90.0 s	49.66 s	34.69 s

TABLE 3.1. Transient response time of floating-gate rectifiers.

the input peak-to-peak voltage. For input voltages above 100 mV, the rectifier efficiency is over 80% as shown in Fig. 3.26 and, hence, it is more efficient at higher input voltages. The voltage efficiency for the 36-stage design is higher as compared to the 16-stage rectifier design for low voltages.

3.6.2. RF-DC Power Conversion System Performance

To test the overall performance of the RF-DC rectifier in actual applications, a custom printed circuit board was designed that includes the antenna with exposed metal traces for impedance and frequency tuning as shown in Figure 3.27. The chip is directly soldered to the board and physically abuts to the antenna to minimize any stray inductance. The output DC voltage is observed via the SMA connector with an oscilloscope or a digital multimeter (DMM).

The performance of the RF-DC power conversion system can be measured wirelessly with propagating electromagnetic wave radiated through an antenna.
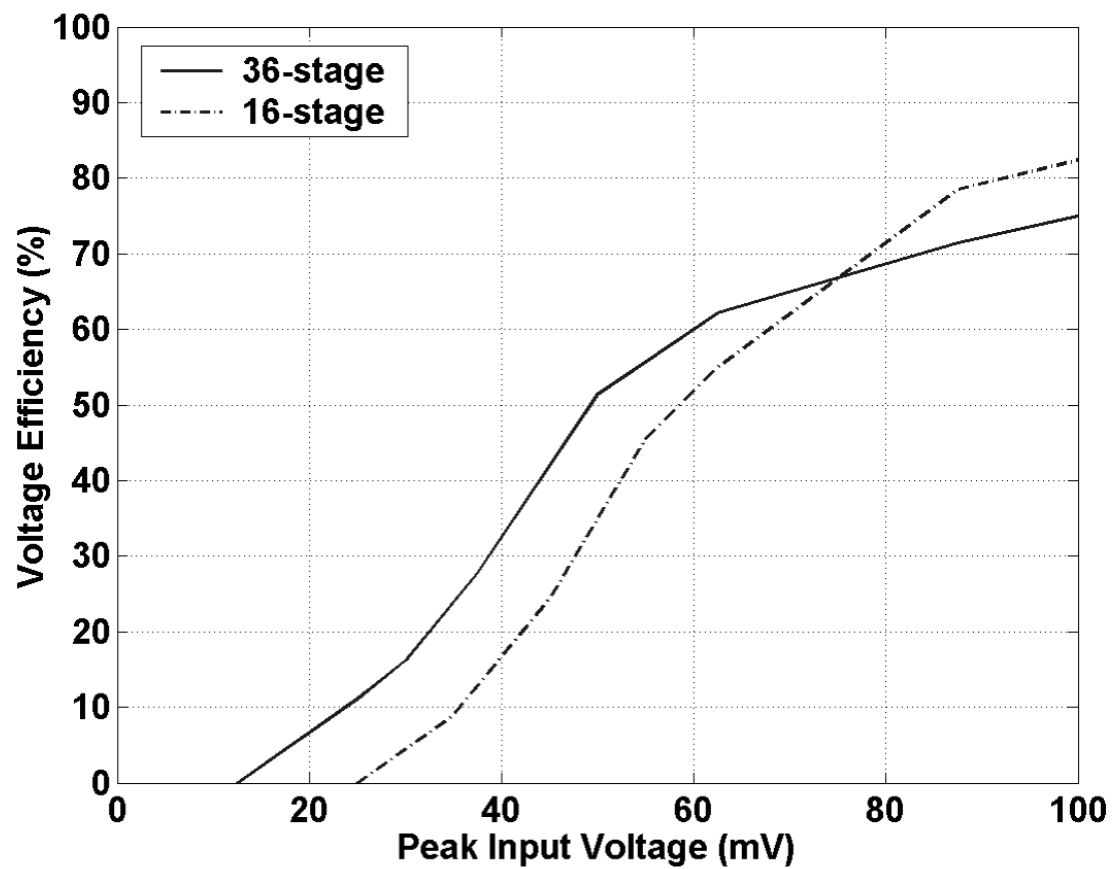
FIGURE 3.26. Measured output DC voltage as function of measured voltage efficiency.
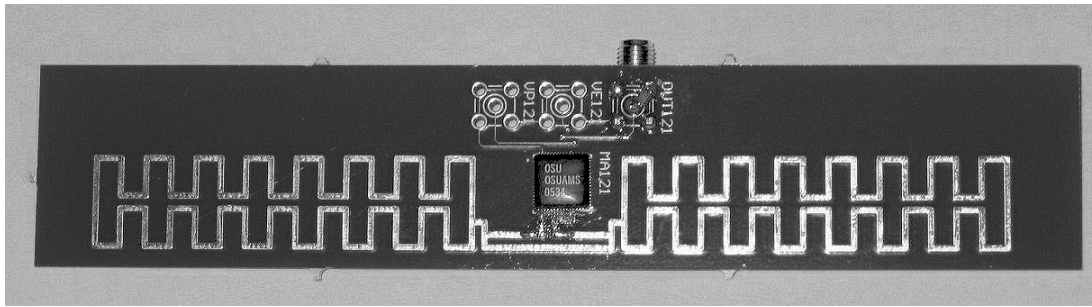
 FIGURE 3.27. PCB to test performance of the RF-DC power converter at the system level.

The output of an HP/Agilent 8665A signal generator is amplified by a Mini Circuits LZY-2 power amplifier to generate signals with 6 W of power in the frequency range of 902-928 MHz. The signal at the output of the power amplifier is then fed to a commercially available diopole antenna through several series connected SMA cables. The losses in the cable combined with the return loss between the power amplifier combined with the gain in the transmit antenna are measured to be around 1.7 dB. Thus, the maximum radiated power is about 36 dBm (4 Watts EIRP).

Only the 36-stage rectifier design is wirelessly measured since it has superior performance in terms of received power sensitivity. Before measuring the overall performance, it is necessary to tune the frequency of the resonator circuit. The resonant frequency can be tuned to the 902-928 MHz range by placing a shorted stub tuning on the bare metal trace at the end of the antenna on the PCB. The tuning of the resonant frequency does affect the output voltage of the RF-DC conversion circuit, since the shorted stub tuning slightly modifies the physical shape of the antenna. The decrease in the output voltage is greater when

the original resonant frequency is further from the desired (i.e., longer length stub tuning) band and the decrease is smaller for a resonant frequency closer to the desired band. Although the frequency tuning does affect the output voltage, this change in output voltage is much smaller compared to the change in output voltage caused by impedance mismatch. For the 36-stage rectifier design, the resonant frequency is originally 860 MHz so the size of the loop is reduced only slightly to increase the resonant frequency to 906 MHz. For the wireless measurement of the RF-DC power conversion circuit, the center frequency is set at 906 MHz for the 36-stage rectifier design.

Figure 3.28 and 3.29 shows the measured output voltage of the 36-stage rectifier as a function of distance and input power for various resistive loads. The 36-stage conversion circuit is capable of outputing DC signal levels of 2 V at distances up to 15 meters with a 36dBm radiating source when it is not loaded as shown in Fig. 3.28. The measured output DC voltage decreases exponentially as distance increases and also decreases as the load resistance is decreased. With a $0.33M\Omega$ load, the conversion circuit operates within 7 meters from the radiating source while providing 1 volt DC. From observation, the operating distance of the rectifier reduces quickly as the load current is increased while at closer distances, the dependence on load current is much less. Fig. 3.29 shows the output voltage curves of the 36-stage design as function of received power calculated from the Friis equation for free-space propagation loss. The slope of the output voltage curves are relatively constant over the full range since the output voltage is inversely proportional to the log of the operating distance. The 36-stage design operates well when the received power is higher than -22 dBm. Measurement of the far-field RF power harvesting system is done in a shielded lab, where the pathloss is enhanced by multipath and standing wave patterns. The same measurement is

also performed in an open area with lower transmitted power and the distance of the measurement is increased by up to 1.4 times.

Figure 3.30 shows the measured output power as a function of distance. The top curve represents the theoretical received power in free-space as calculated by the Friis formula for free-space propagation loss given a 36 dBm radiating source. With a 0.33 MΩ resistive load, the current requirement at the load is higher so more current is drawn from the output of the rectifier to drive the load hence the curve shows a steeper slope. The slope of the roll off is directly proportional to the load current at the output of the rectifier. With a 1.32 MΩ load, 1 μW at 10 meters is possible and up to 12.3 meters with the 5.6 MΩ load. Figure 3.31 shows the output power as function of received power. From this plot, the point where the power curve starts to roll off from the straight (open circuit) line can be seen more clearly. For the 36-stage rectifier design, the output power starts to roll off at about -8 dBm for the 0.33 MΩ load, -13 dBm for the 1.32 MΩ load, and -18 dBm for the 5.6 MΩ load.

The measured power conversion efficiency versus distance curves are shown in Figures 3.32 and 3.33. The power conversion efficiency curve for each individual load is shown as well as the maximum efficiency that can be achieved at a particular distance. For a perfectly matched resonator network, the power available for rectification is half of the received power in the antenna since only half of the power is dissipated in the rectifier. The power conversion efficiency of the RF-DC power conversion system is defined as the ratio between the DC output power and available power for rectification (half of the received power) from the antenna. The maximum efficiency measured is 60% with the 0.33 MΩ load. The power conversion efficiency peaks at around -8 dBm received power due to the fact that the output voltage reaches a maximum point of approximately 9 V,

which is due to the reverse breakdown voltage of the p-n junctions. This peak can be moved or optimized, for example, by changing number of rectifier stages and transistor sizes. For lower load currents, the power conversion efficiency is most optimized at lower received power or longer distances from the RF source. On the other hand, at higher load currents, the power conversion efficiency is most optimized at higher received power or shorter distances. The design of the 36-stage rectifier shows highest efficiency at 3 meters with a 0.33 MΩ load, and the power conversion efficiency curves rolls off as the inverse of distance from the RF source. The peak efficiency with the 5.6MΩ and 1.32 MΩ load is 29% at about 9 meters and 35% at about 5 meters, respectively.

Figure 3.34 shows the maximum energy that can be extracted from the RF signal in one hour at various distances from the radiating source. From the logarithmic plot of extracted energy against distance, the extracted energy curve is approximately a straight line. The maximum extractable energy in an hour is 0.8 J at 1 meter, 40 mJ at 5 meters, 7 mJ at 10 meters and about 1 mJ at 15 meters from the source. With one hour charge time, the RF-DC power conversion circuit acquires and replenishes enough energy to operate a circuit that dissipates 1 mW for one second or 100 mW for 10 ms at distances up to 15 meters. For an increase of every meter in distance, the amount of energy that can be extracted from the RF signal is reduced by a factor of 2.6. This establishes the trade off between power dissipation and operating distance of the integrated circuit powered by the RF-DC power conversion circuit.

Figure 3.35 compares the voltage performance of the 36-stage power conversion circuit with recently published work [61–63]. The work in [62, 63] uses an active switched capacitor circuit with a clock generator and an external power
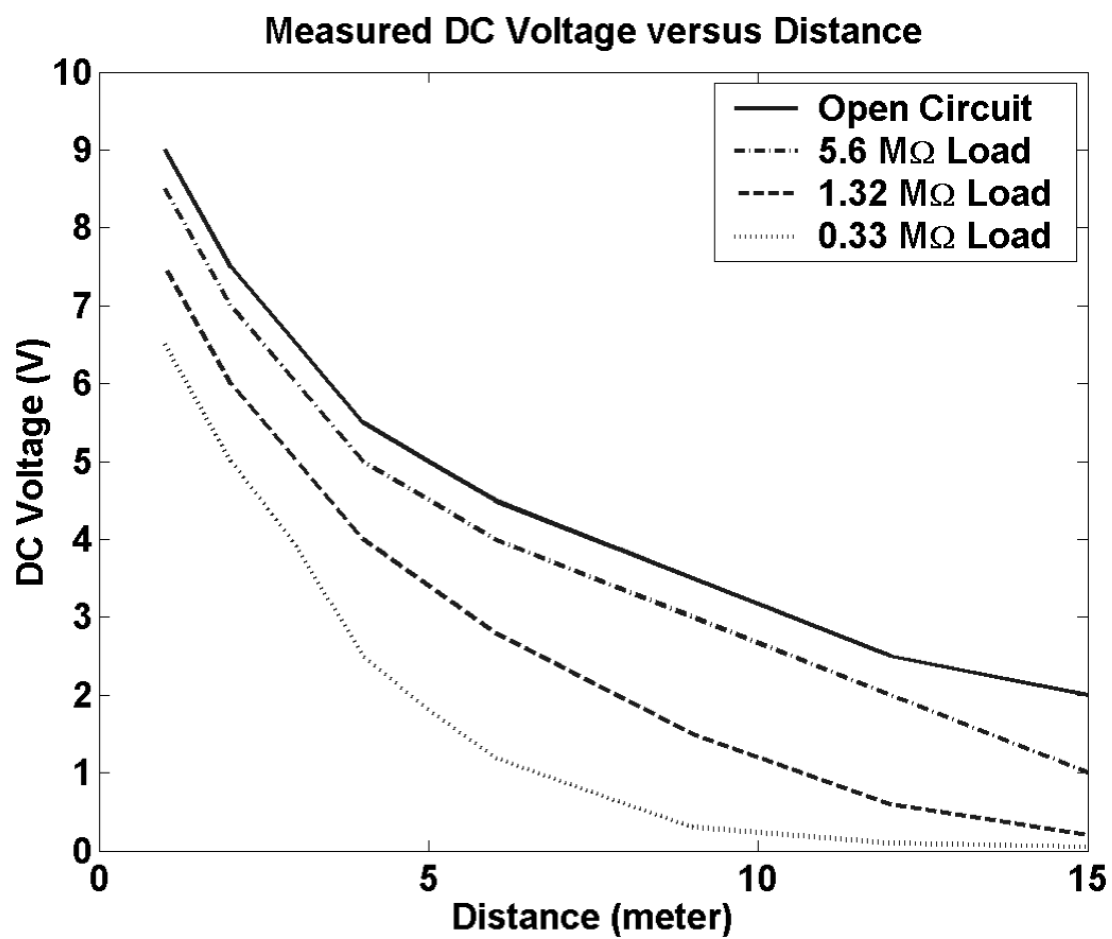
FIGURE 3.28. Measured DC output voltage as function of distance and load for the 36-stage rectifier.
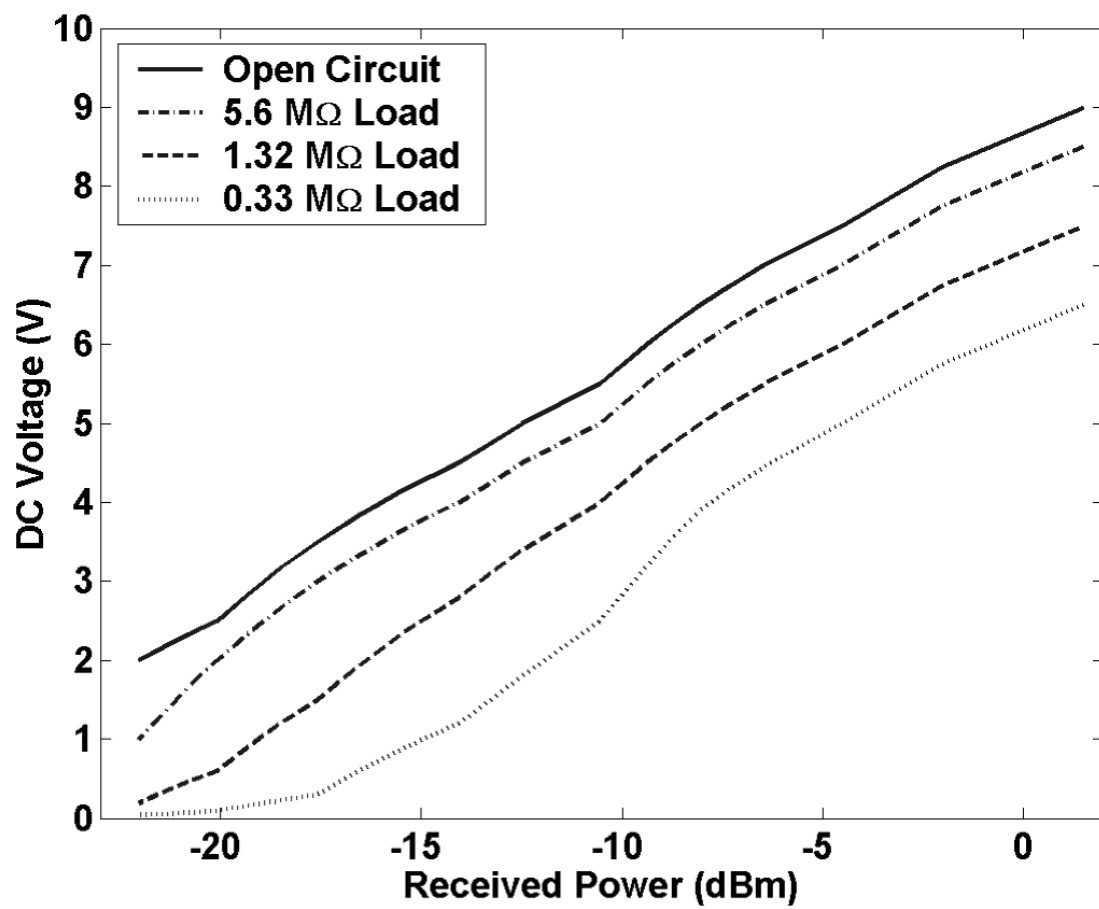
FIGURE 3.29. Measured DC output voltage as function of received power and load for the 36-stage rectifier.
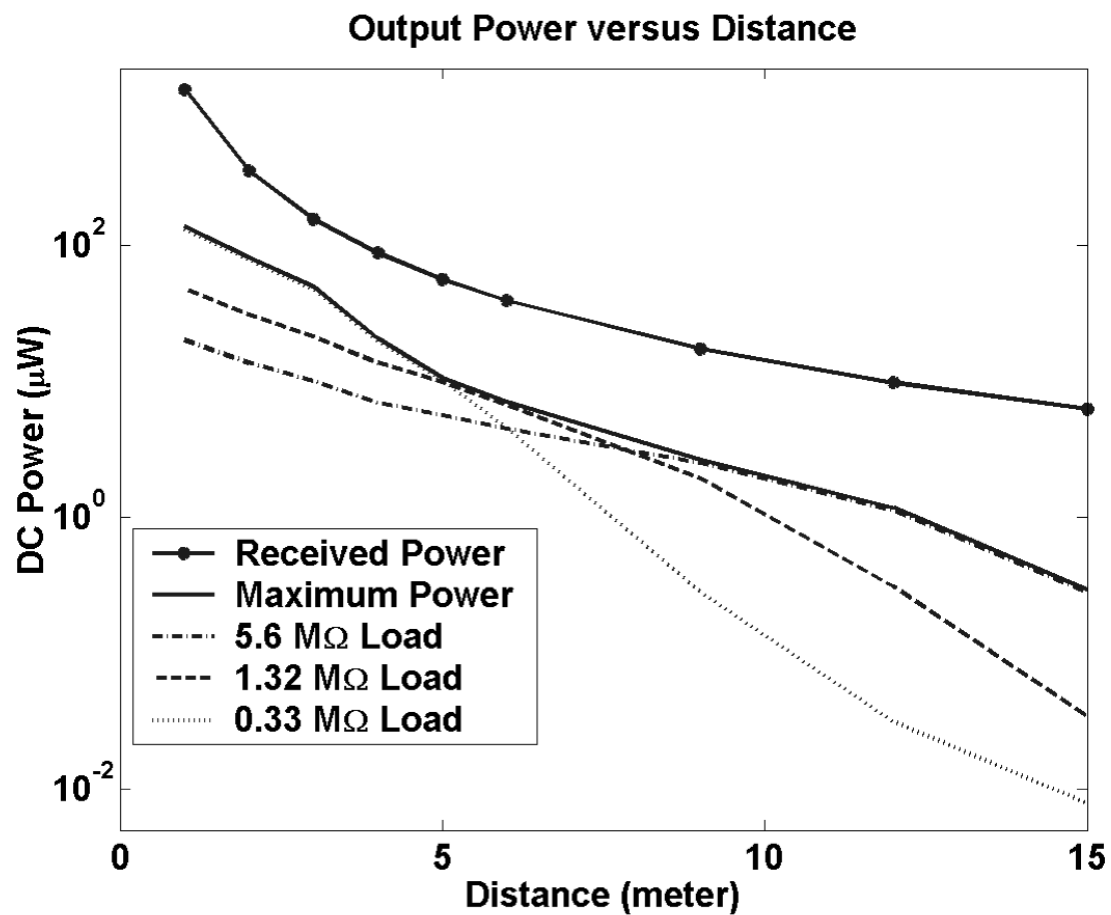
FIGURE 3.30. Measured output power performance as function of distance and load for the 36-stage rectifier.
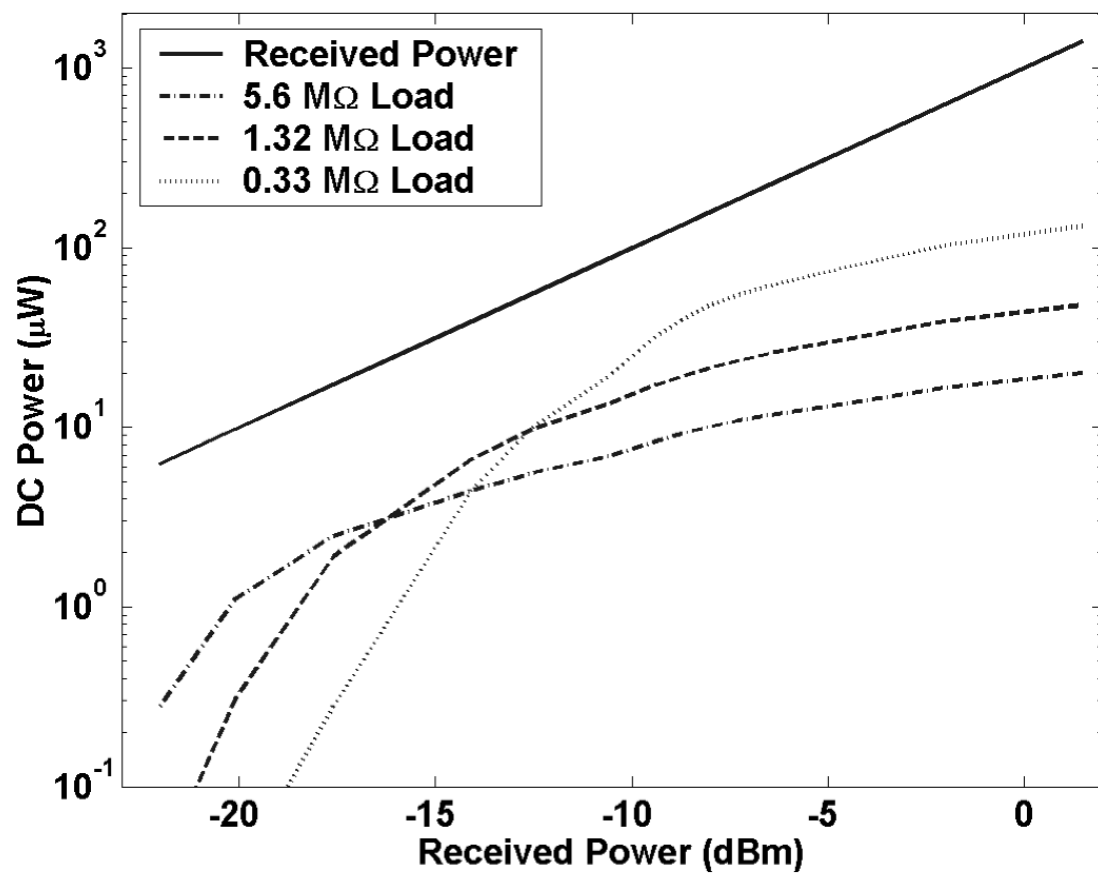
FIGURE 3.31. Measured output power as function of received power for the 36-stage rectifier.
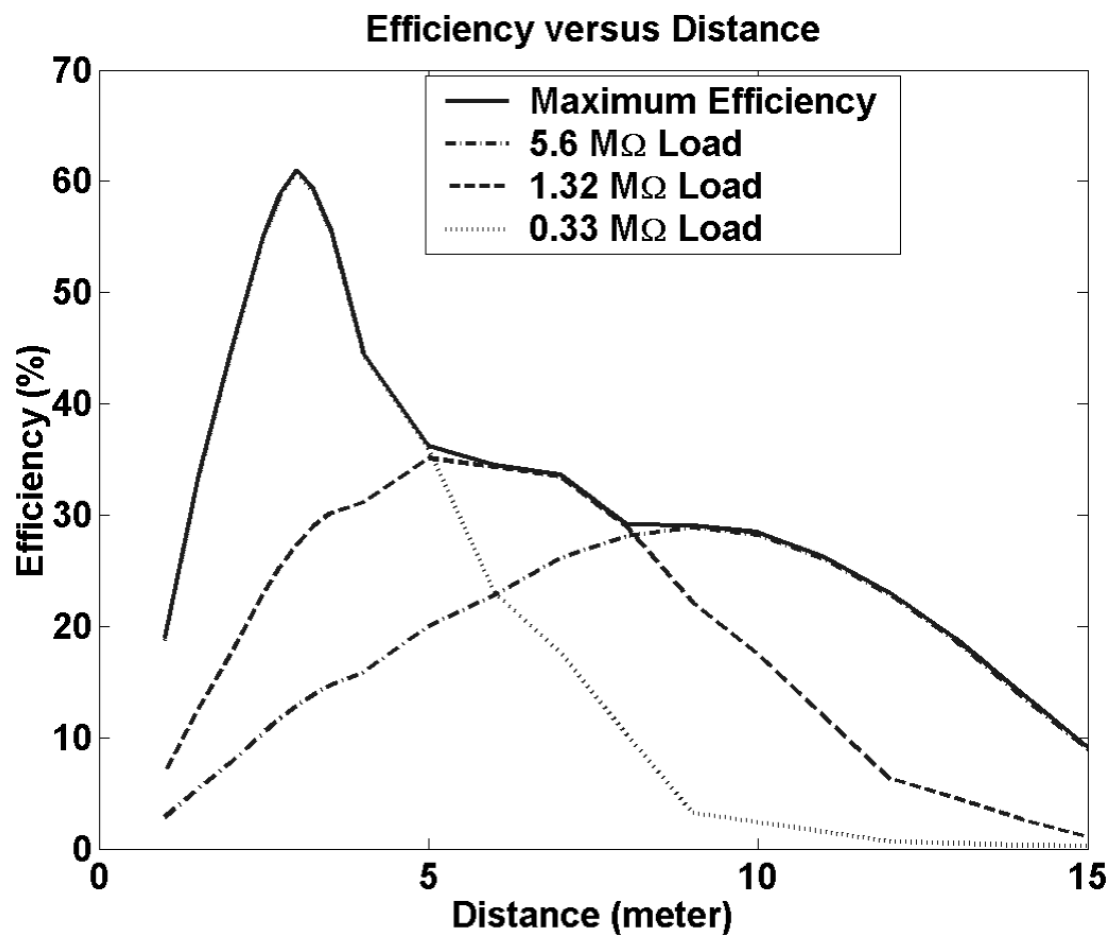
FIGURE 3.32. Measured power conversion efficiency curves as function of distance and load for the 36-stage rectifier.
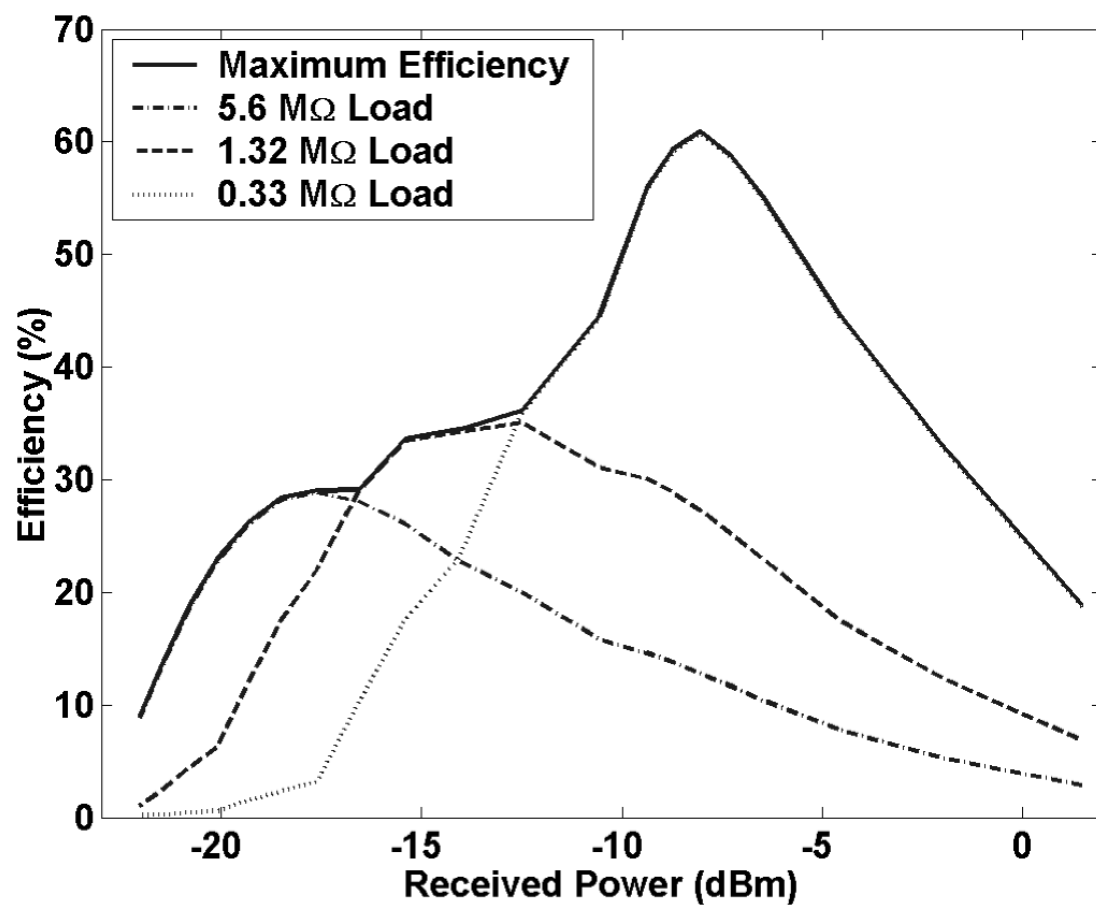
FIGURE 3.33. Measured power conversion efficiency curves as function of received power for the 36-stage rectifier.
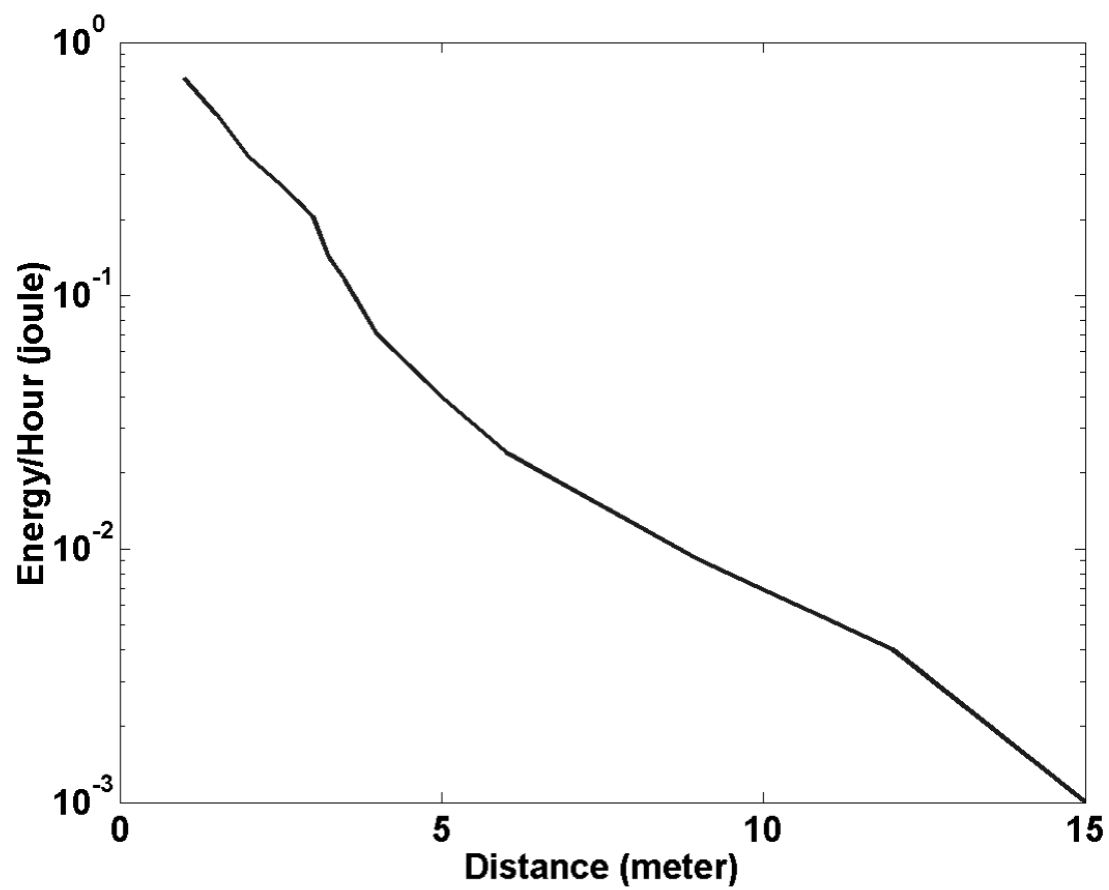
FIGURE 3.34. Measured energy extracted per hour as function of distance for the 36-stage rectifier.

supply to actively bias the gate-source voltage of the diode-tied transistor in the rectifier circuit. The work in [61] uses a passive method to bias the gate-source voltage of the diode-tied transistor, however, the passive circuit does require static power to maintain the gate-source bias. This gate-source bias needs a large turn-on sinusoidal signal to start-up and takes a long time for the bias to charge up when a signal level below threshold voltage is applied. Once the power source is turned off, the gate-source bias will be discharged from the static current. The work in [62, 63] requires the generation of a bias voltage V_{th} which uses a reference current in the nanoamp range, although the static power dissipated from the resistor is minimal, it causes a bias voltage much less than the desired threshold voltage. In other words, the voltage drop across a diode-tied transistor under 2 nA bias is much different than one drawing 2 μA of current. This voltage difference is typically 100 mV for every decade of current difference. Also, this method would require extra circuitry to generate a voltage bias and a differential clock and it would also require a secondary battery. The results obtained from [61] and [62, 63] are measured from an applied sinusoidal input and the distance performance is calculated using the Friis equation for free-space. Distance performance in this work is the actual measured distance from the radiation source. Because [61] and [62, 63] both have voltage regulation, only the voltage at the far distance is compared. The rectifier design in [62, 63] is 1 stage, and in [61] is 6 stages, hence the output voltage is much lower than the 36-stage design under a 5.6 MΩ load, however, the output current with the 5.6 MΩ load is lower compared to [61] and [62, 63]. With the 0.33 MΩ load, the current is increased but the output voltage is only comparable to the other two designs.

Figure 3.36 shows the output power curves for the same three designs. The output power of this work greatly exceeds other designs and, for received power

below -20dBm, it gives output power level 5 times the output power of the closest design. The comparison of the power conversion efficiency is shown in Figure 3.37. This design is 30% more efficient throughout the full range with a peak efficiency of 60%. Table I summarizes this work as compared to previously published work.
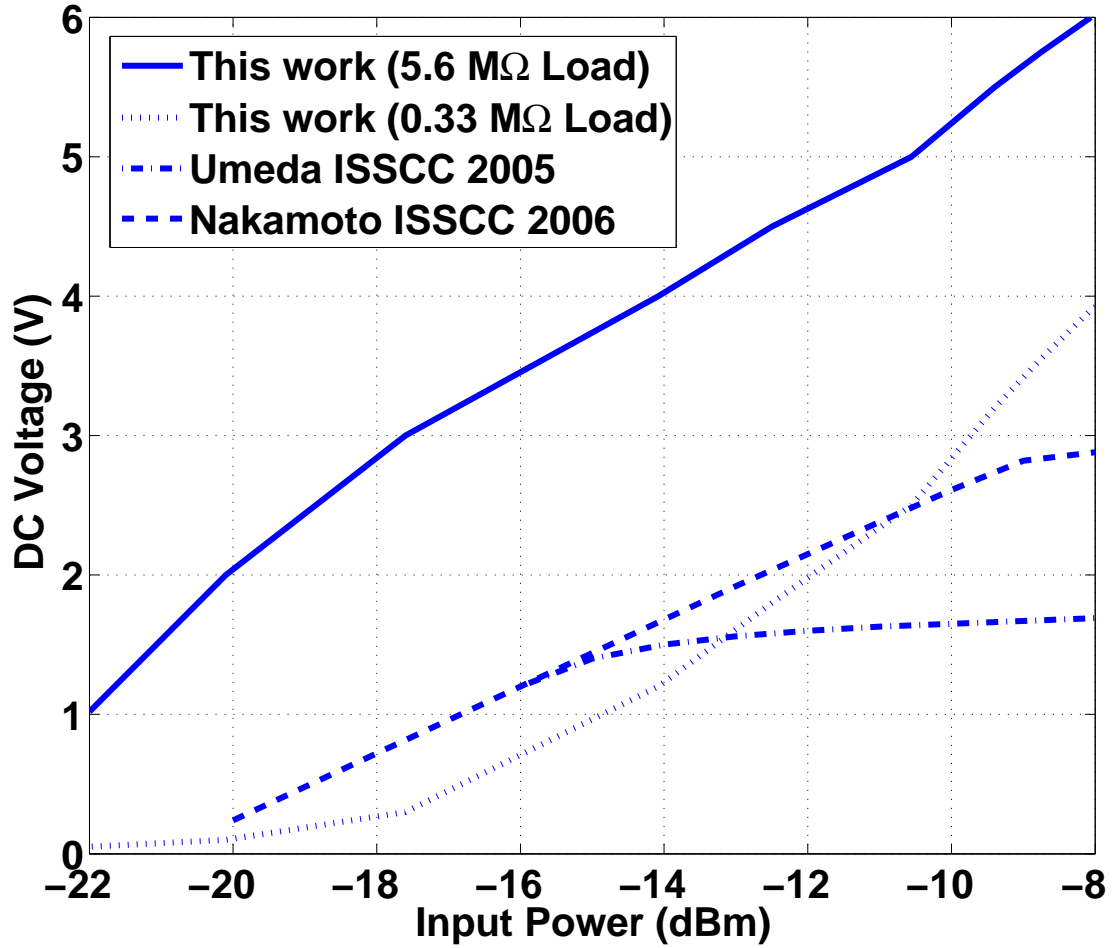
FIGURE 3.35. Output DC voltage as function of the input power.
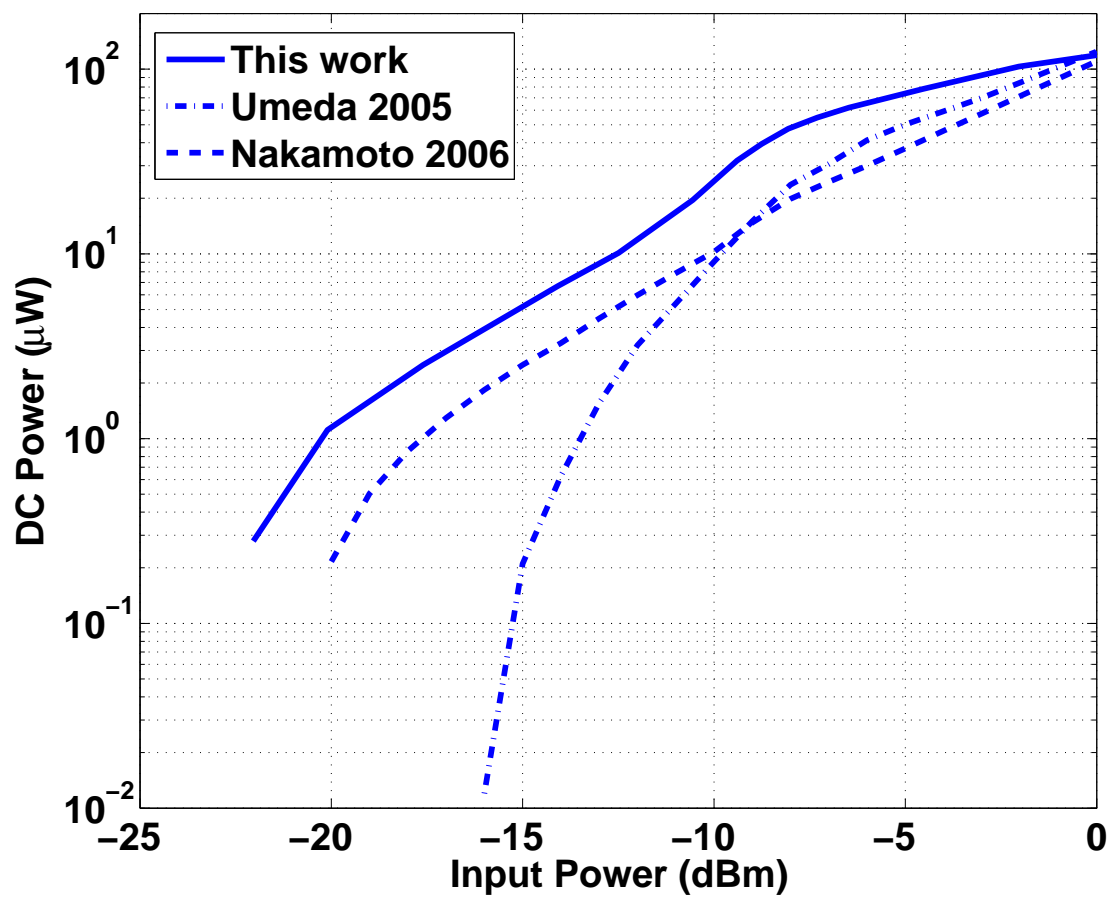
FIGURE 3.36. Output DC power as function of the sinusoidal input.
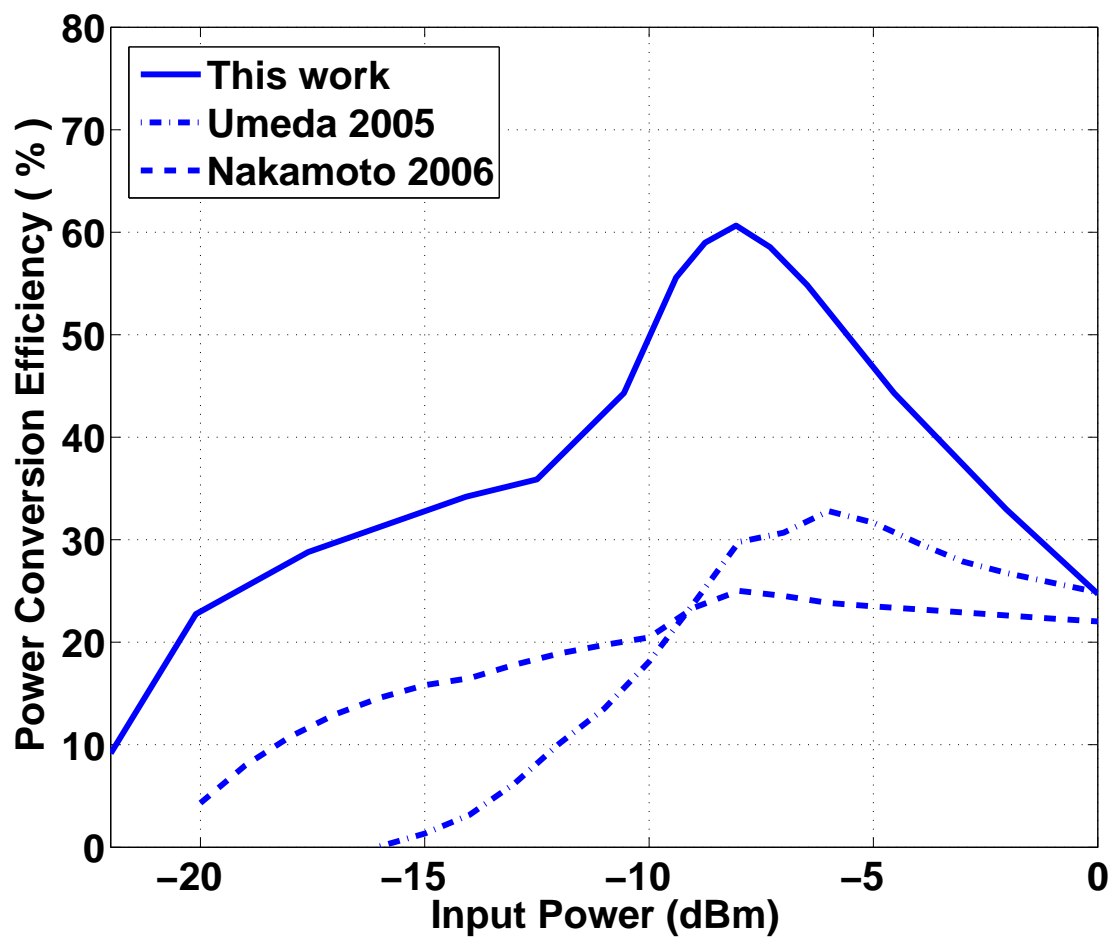
FIGURE 3.37. Power conversion efficiency as function of the sinusoidal input.

Design	This work	Umeda	Nakamoto	Karthaus	Kocer
		[62, 63]	[61]	[51]	[60]
Technology	**0.25 μm**	0.30 μm	0.35 μm	0.5 μm	0.25 μm
Maximum Efficiency	**60%**	33%	24%	28%	11%
Minimum RF Power	**5.5 μW** **-22.6 dBm**	40 μW -14 dBm	100 μW -10 dBm	16.7 μW -17.8 dBm	60 μW -12.3 dBm
Distance (Free space)	**42 meters @ 4 W**	17 meters @ 4 W	11 meters @ 4 W	26 meters @ 4 W	13 meters @ 4 W
Distance (Measured)	**15 meters @ 4 W**	2 meters @ 4 W	4.3 meters @ 4 W	4.5 meters @ 1 W	1.7 meters @ 60 mW

TABLE 3.2. Performance summary.

3.7. Conclusion

A passively powered RF-DC conversion circuit operating at 906 MHz is presented. A novel rectifier circuit is designed and demonstrated to work with signals as low as 50mV and has a maximum measured efficiency of 60%. This allows an increase in the operable distance between the circuit and the radiation source. The system operates with received power as low as -22.6 dBm (5.5μW), corresponding to 42 meters distance in free-space with a 4W radiation source. A measured distance of 15 meters is achieved with 1 volt DC and a 0.3μA load current.

4. EFFICIENT FAR-FIELD RF POWER CONVERSION INTERFACE AND POWER MANAGEMENT CIRCUITS

4.1. Abstract

An RF-DC power conversion system is designed to efficiently convert far field RF energy to DC voltages at very low received power and voltages. Passive floating-gate rectifier circuits are designed in 0.18μm CMOS technology to nearly eliminate the rectifier threshold voltage threshold. An effective threshold voltage of less than 40 mV is achieved. Low-power floating-gate programming circuits are designed to periodically replenish charge to the floating-gates. Ultra-low power voltage regulator circuits are designed to efficiently regulate the DC voltage from RF-DC rectification. The voltage regulator operates at nanowatts of power and can withstand input voltages up to 12 volts.

4.2. Introduction

The vast reduction in size and power consumption of CMOS circuitry has led to an increase in the use of portable devices, and most of these devices require the use of a battery. Energy harvesting methods are being explored to reduce the use of batteries and increase the time between charging of portable devices. One of the most popular energy extraction methods for portable devices is to harvest power from propagating radio frequency (RF) signals [1]. For energy harvesting applications, efficient power conversion circuits are required to maximize the amount of power that can be harvested [9, 61, 62].

In ultra-low power systems, such as in sensor networks, it is essential that circuit blocks are designed to dissipate very low quiescent power. Power man-

agement for such systems must be efficient as very little power is available for storage and operation. A passive rectifier circuit is designed to efficiently convert RF energy to DC power using floating gate transistors as rectifying diodes. Novel voltage regulators and floating-gate programming circuits are designed to enhance power efficiency of RF energy harvesting systems.

4.3. Energy Harvesting System Overview

Figure 4.1 shows the general block diagram of a RF energy harvesting system [14]. For this system, RF power is radiated via the hub or base station transmitter and the power harvester converts this RF energy in to a DC voltage.
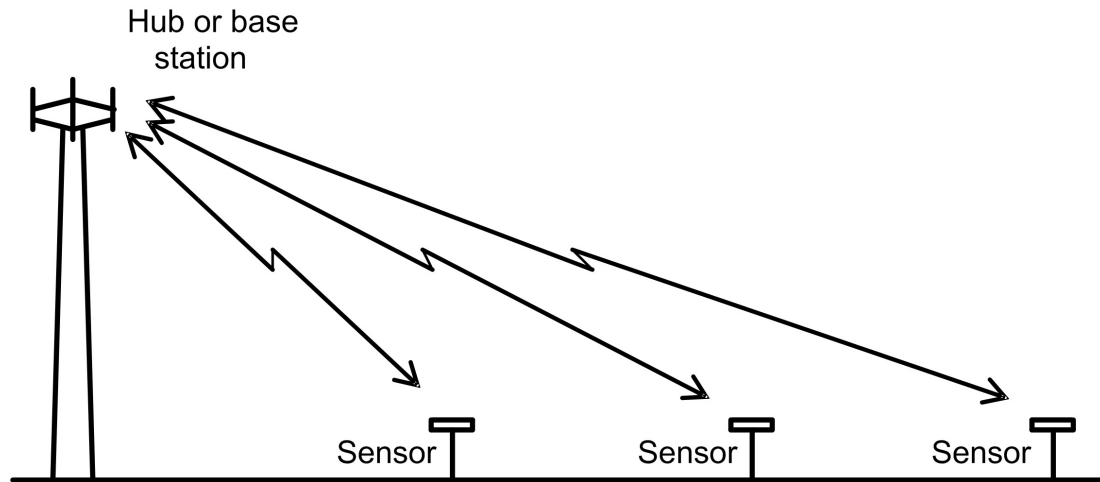
FIGURE 4.1. Illustration of communication links between base station (hub) and sensors in a passively powered sensor network.

Figure 4.1 shows the block diagram of the RF power conversion system with power management circuitry. The RF power is radiated via the transmitter

through the transmit antenna and is harvested by the receive antenna. The RF signal harvested by the antenna is then fed into the high-Q impedance matching network to maximize power transfer while passively providing a voltage gain [69, 55, 56, 68]. After going through the impedance matching network, the RF signal is then rectified to convert it into a DC voltage. A floating-gate rectifier is used to rectify the sinusoidal RF signal to a DC voltage. The floating-gate rectifier is designed with an on-chip floating-gate programming controller that also has an option for off-chip floating-gate programming. The output of the rectifier is loaded by an electronic double layer capacitor to hold the charge harvested by the energy harvester. As the strength of the RF signal can be varied throughout a wide range depending on the distance from the radiated source, voltage regulation is needed at the output of the rectifier to ensure a safe and reliable voltage is delivered to the device. A secondary holding capacitor is used at the output of the voltage regulator to reduce droop in the regulated voltage when the power consumption of the device exceeds the power extracted from the RF environment.

A wake-up circuit is designed as part of the floating-gate programming circuitry to keep track of the time between the programming of the floating-gate and to enable and disable the floating-gate control circuits. The floating-gate programming requires a significant amount of digital circuitry, hence, a separate voltage regulator is designed with a lower regulated voltage to operate digital circuits in subthreshold.

4.3.1. System Flow Diagram with Floating-gate Programming

The flow diagram of the energy harvesting system is shown in Figure 4.3. The floating-gate rectifier is required to be off-line when the floating-gate is pro-
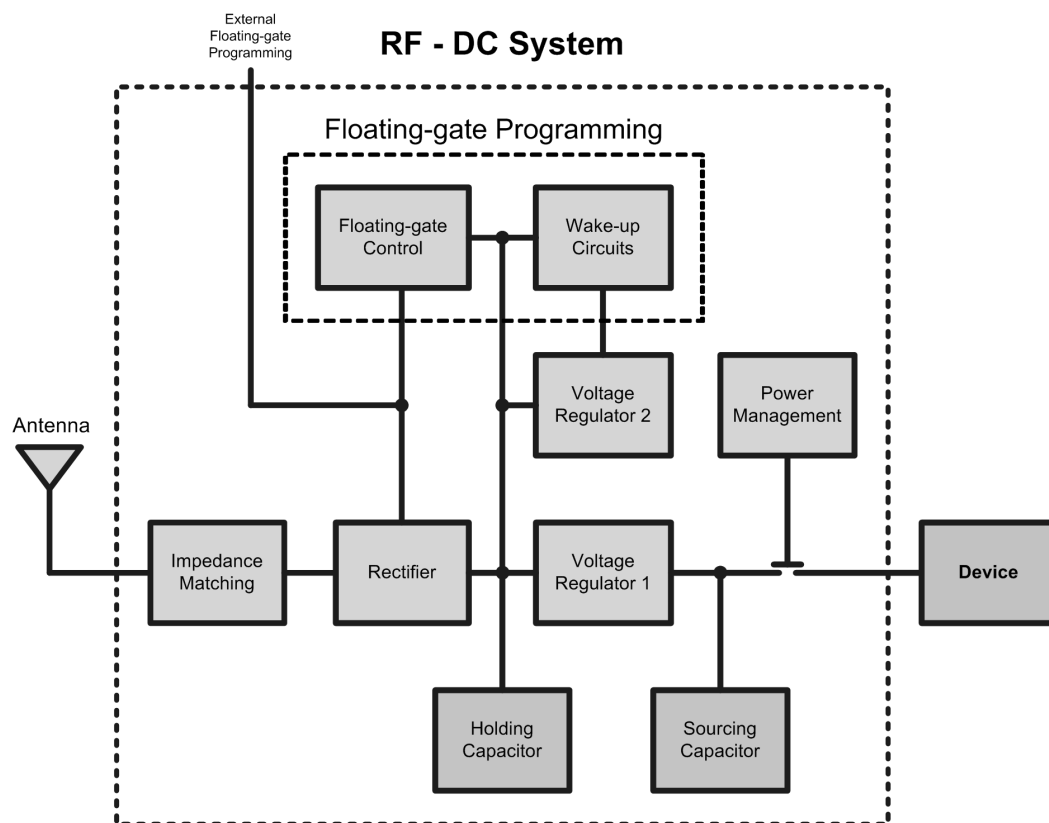
FIGURE 4.2. Block diagram of RF energy harvesting system with floating-gate programming.

grammed. A wake-up timer is designed to enable the floating-gate programming circuits approximately once a month to replenish the charge on the floating gate. When the output of the wake-up timer is high (or enabled), the output of the rectifier circuit is disconnected from the holding capacitor and is connected to other capacitors to hold the analog states of the floating-gate programming. After the floating-gate programming is done, the output of the rectifier circuit is reconnected to the holding capacitor and the energy harvesting system resumes its normal operating mode.
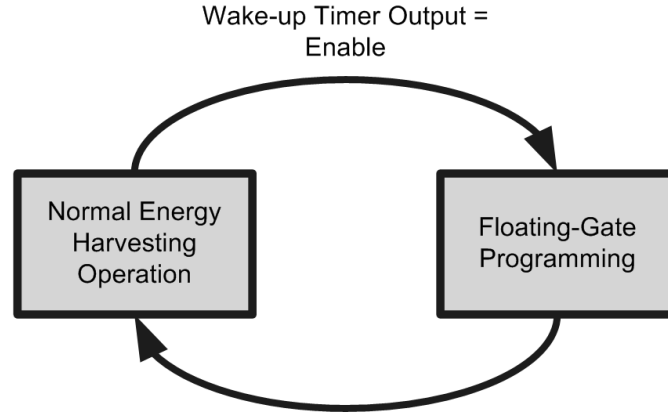
FIGURE 4.3. Flow diagram of the energy harvesting system with floating-gate programming.

4.3.2. Link Budget

The link budget of a reference energy harvesting system is shown in Table 4.1. This reference system has a radiated power of 1-W (30 dBm) with 6-dB of gain for the transmit antenna, which is the highest allowed by FCC regulations [16]. The received antenna gain for the reference system is a dipole antenna with

Distance (meters)	Path loss (dB)	Received Power (dB)	Rectifer Efficiency	Delivered Power (dBm)	Delivered Power (μW)
3.0	41.06	- 9.60	54 %	- 12.25	59.6
4.0	43.56	- 12.1	36 %	- 16.51	22.3
5.0	45.50	- 14.0	33 %	- 18.83	13.1
6.0	47.09	- 15.6	31 %	- 20.69	8.54
7.0	48.43	- 16.9	29 %	- 22.32	5.87
8.0	49.59	- 18.1	28 %	- 23.63	4.34
9.0	50.61	- 19.1	27 %	- 24.81	3.31
10.0	51.53	- 20.0	24 %	- 26.24	2.38
12.0	53.11	- 21.6	17 %	- 29.32	1.17
15.0	55.05	- 23.6	6 %	- 35.78	0.264

TABLE 4.1. Link budget of energy harvesting system with floating-gate rectifier.

2 dB of antenna gain. Table 4.1 shows the received and delivered power from the energy harvesting system as a function of distance in free space [17]. The rectifier efficiency corresponds to the power conversion efficiency of the floating-gate rectifier at different received power [14]. For distances up to 12 meters from the power source, the power that can be delivered to the holding capacitor can be as high as 1.2 μW.

4.4. Rectifier Design

From the system point of view, the rectifier circuit must be designed to reduce threshold voltage loss (V_{TH}) as much as possible to improve the efficiency of the RF-DC power conversion system. The rectifier circuit must also be designed so that the output voltage can be scaled by cascading multiple rectifier stages in series. Also, parasitic components in the rectifier must be kept as low as possible to improve power conversion efficiency.

4.4.1. Conventional and Floating-gate Voltage Doubler Rectifier

The floating-gate rectifier circuit is designed with the voltage doubler rectifier architecture [9]. Figures 4.4 and 4.5 shows the conventional voltage doubler rectifier and the novel floating-gate voltage doubler rectifier, respectively.
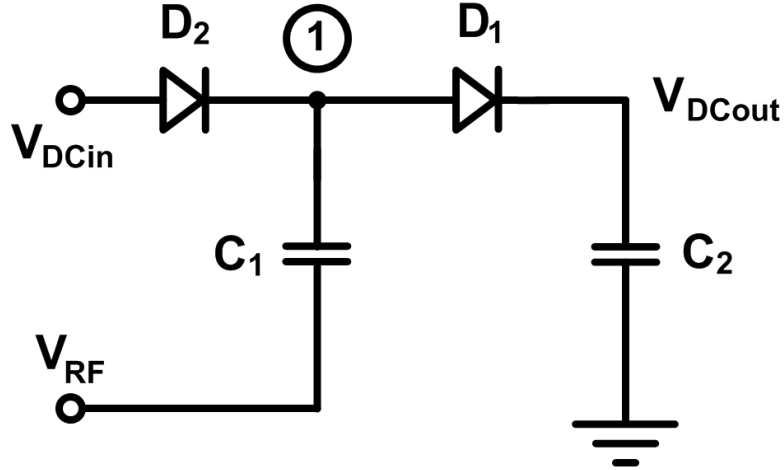
FIGURE 4.4. Conventional voltage doubler rectifier.

To design a floating gate device in a standard CMOS process, a MOS capacitor is placed in series with the gate of the diode-tied transistor as shown in
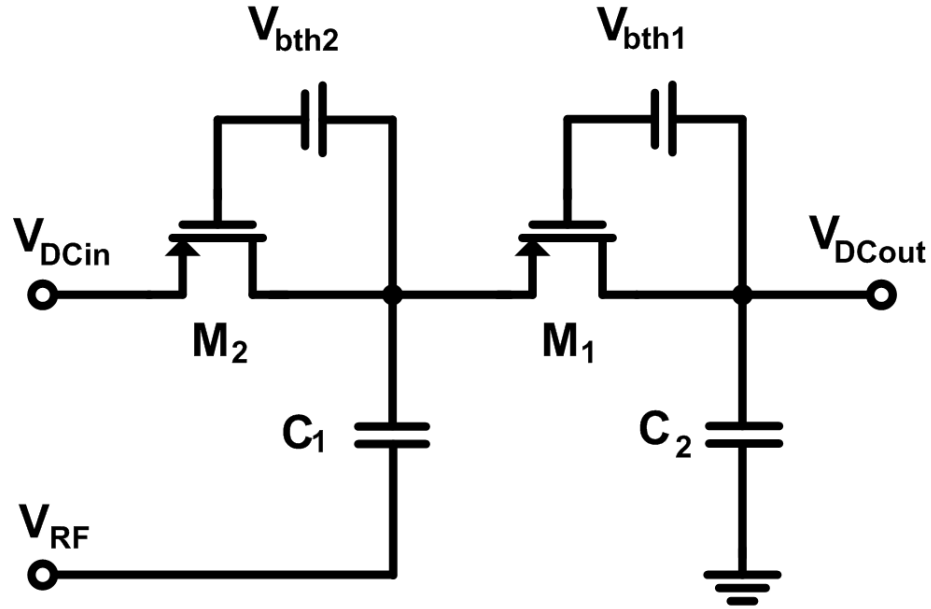
FIGURE 4.5. PMOS floating-gate voltage doubler rectifier.

Figure 4.6. This standard structure form the low threshold diode for rectification, the transistor level schematic of the floating-gate rectifier is shown in Figure 4.7.

4.4.2. Multistage Rectifier Circuit

The individual stages of the floating-gate voltage doubler rectifier circuit can be arranged in cascade to increase the output voltage of the rectifier [65, 66]. Figure 4.8 shows N stages of a voltage doubler rectifier in cascade.

4.5. Floating-Gate Programming Circuits

Floating-gate programming circuits are designed to replenish charge to the floating-gate of the floating-gate rectifier circuit. The programming of the floating-
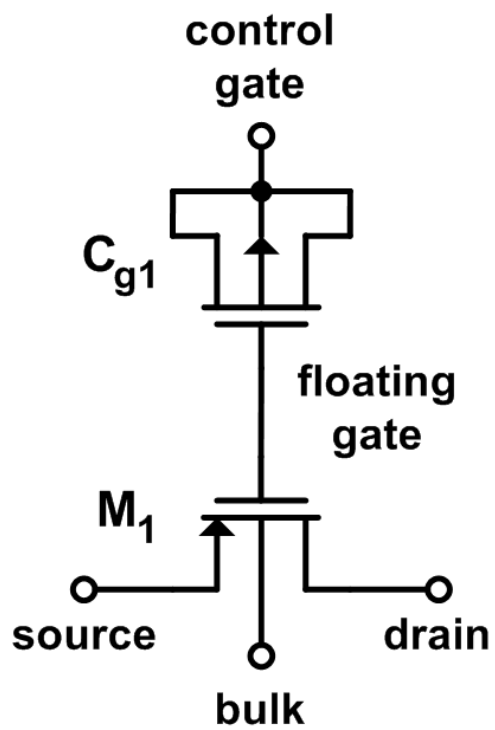
FIGURE 4.6. PMOS implementation of a floating gate transistor.
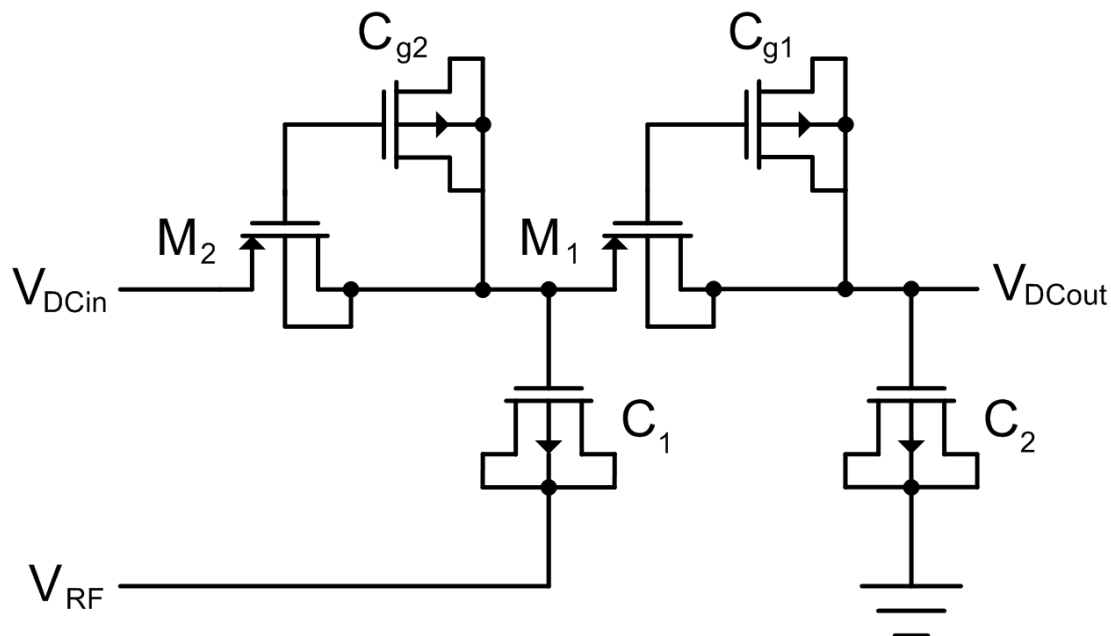
FIGURE 4.7. Transistor level schematic of PMOS floating-gate rectifier.

gate is done periodically to prevent charge from leaking off from the floating-gate and also to optimize the performance of the floating gate rectifier over time. The block diagram of the floating-gate programming circuit is shown in Figure 4.9

The floating-gate programming circuit uses a ring oscillator circuit to generate a pulse that enables the floating-gate programming circuit after some time interval has elapsed. This time interval can be set by altering the combinational logic to change the floating-gate programming interval. The enable circuit can also be designed to trigger once the efficiency of the rectifier drops by a certain amount or when the output voltage drops by a certain percentage. For this work, the design is done so that the floating-gate programming circuit is enabled approximately once every month and the enable pulse remains high until all the floating-
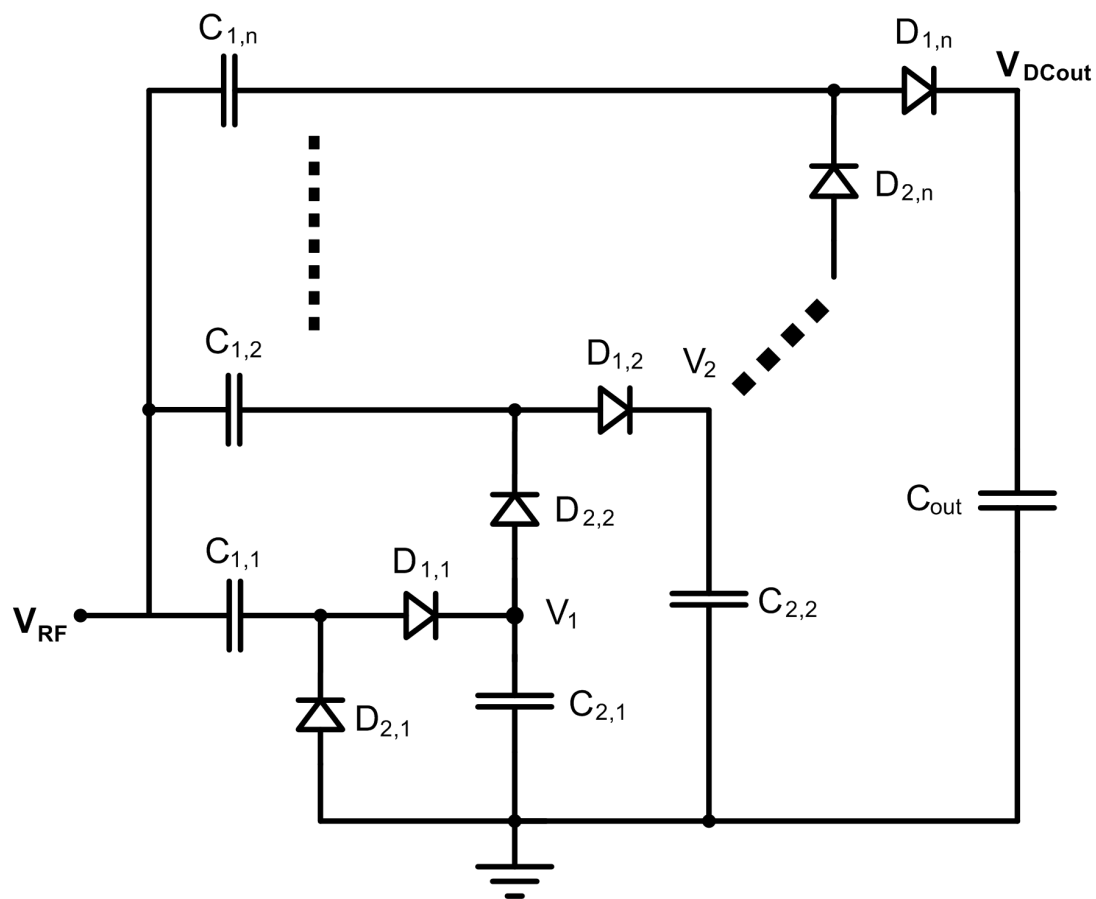
FIGURE 4.8. Voltage doubler rectifier with N-stages in cascade.
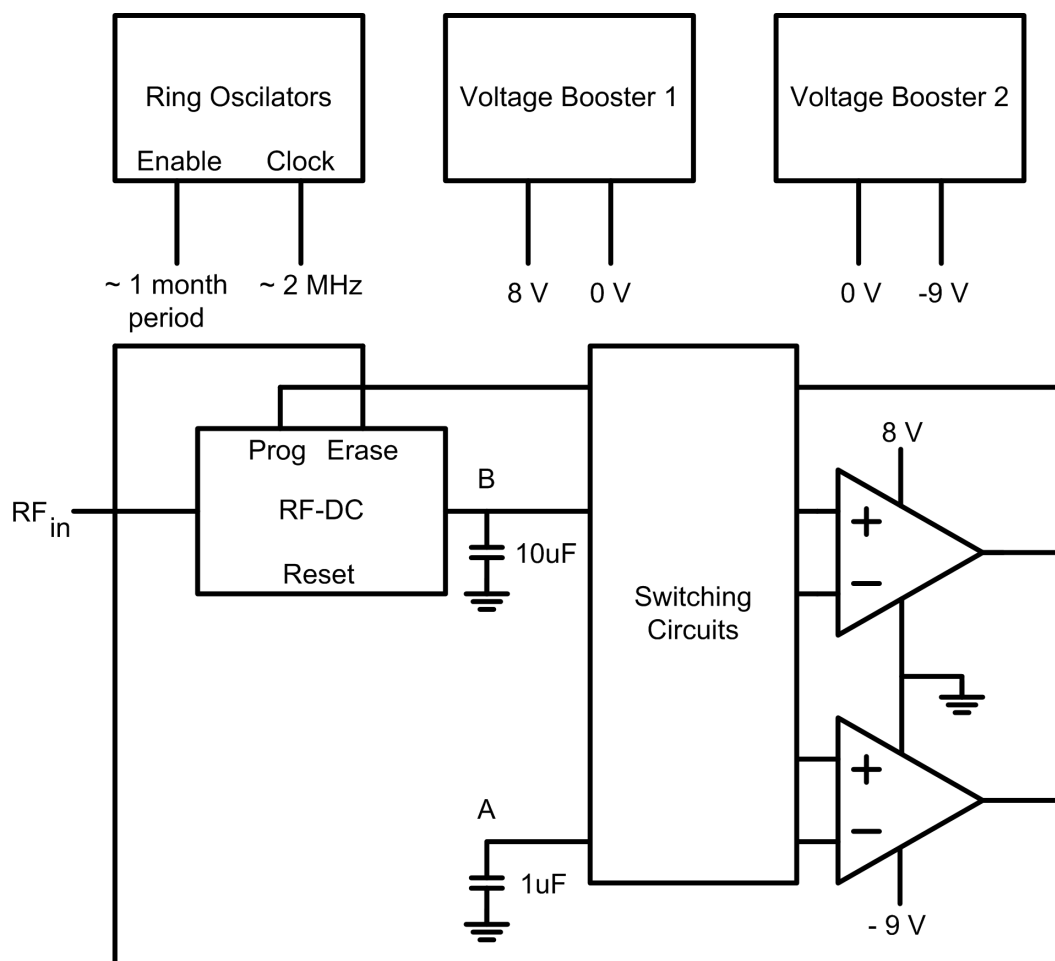
FIGURE 4.9. Block diagram of the floating-gate programming circuit.

gate programming procedures are completed. Figure 4.10 shows the schematic of an NMOS floating-gate device and how it is programmed. The gate of the floating-gate transistor is connected to the control gate via a capacitor, and a separate capacitor is used to tunnel charge to the floating-gate to program the device. The cross sectional view of an NMOS floating-gate with its programming nodes is shown in figure 4.11. In a standard CMOS process, the tunneling capacitor can be designed with two MOS capacitors, one for charge injection and one for charge removal from the floating-gate. In normal operation, the floating-gate device is controlled by the control-gate which is the drain, source and bulk terminal of a PMOS capacitor.
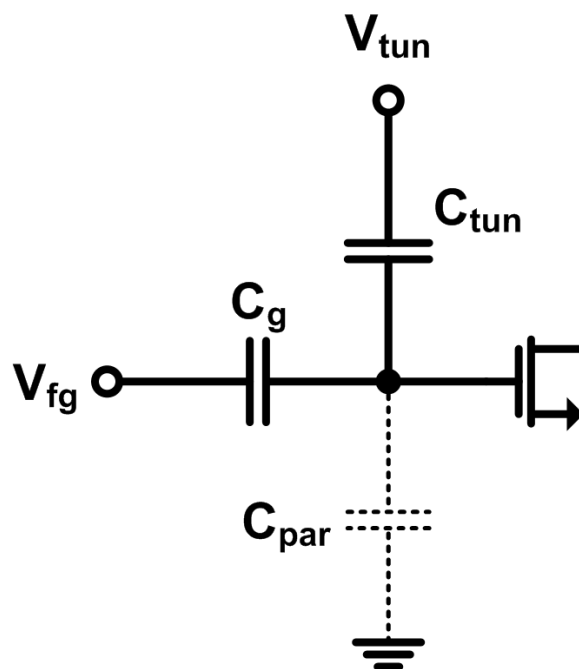
FIGURE 4.10. Structure for programming and deprogramming of floating-gate devices.

FIGURE 4.11. Cross sectional view of an NMOS floating-gate device with programming and deprogramming nodes.

The general idea of putting charge on the floating gate is to overdrive the control gate to cause severe band bending so that charge can be introduced to the floating-gate via Fowler-Nordheim (F-N) tunneling [59]. Two voltage boosters are required to generate a high negative and positive voltage to overdrive and program the floating gates [52]. Two opamps are also required to drive the switching circuit and program or erase charge from the floating gate. The switching circuit is designed on board to increase the flexibility of the floating-gate programming sequence. Two external capacitors are also required for storing the analog state of the rectifier.

4.5.1. Floating-Gate Programming Procedures

The general idea for charging the floating gate is to find the maximum output voltage possible to keep the rectifier at the most optimized efficiency at all times. To do this, the floating-gate programming circuits will initially be in program or erase mode, if the programming or erasing action is causing the voltage

to decrease, the action of the floating-gate programming will then be reversed on the next cycle so that the output voltage is increased to an optimum point. An analog switching circuit is required to ensure proper functioning of the gate charging circuit.

Figure 4.12 shows the five distinct phases of the floating-gate programming. The procedure is to first initialize and then go through the cycle of storing, evaluation and programming phase loop until the amount of charge on the floating-gate is optimized or close to the optimize value. When no further programming is needed, the procedure will go to the completion phase where most of the circuitry for floating-gate programming is powered down.

4.5.1.1. Initialization Phase

In the initialization phase, the rectifier is injected with a controlled input sinusoidal signal and the output storage capacitor is charged. The initialization process can either be triggered by an external control signal or by the on-chip ring oscillator circuit.

4.5.1.2. Storing Phase

In the storing phase, the holding capacitor is charged with the rectifier output voltage to store the analog state of the rectifier. The storage capacity of the holding capacitor must be set to be large enough so charge leakage over one floating-gate programming cycle is minimal and small enough to reduce the time required to program all of the floating-gates.
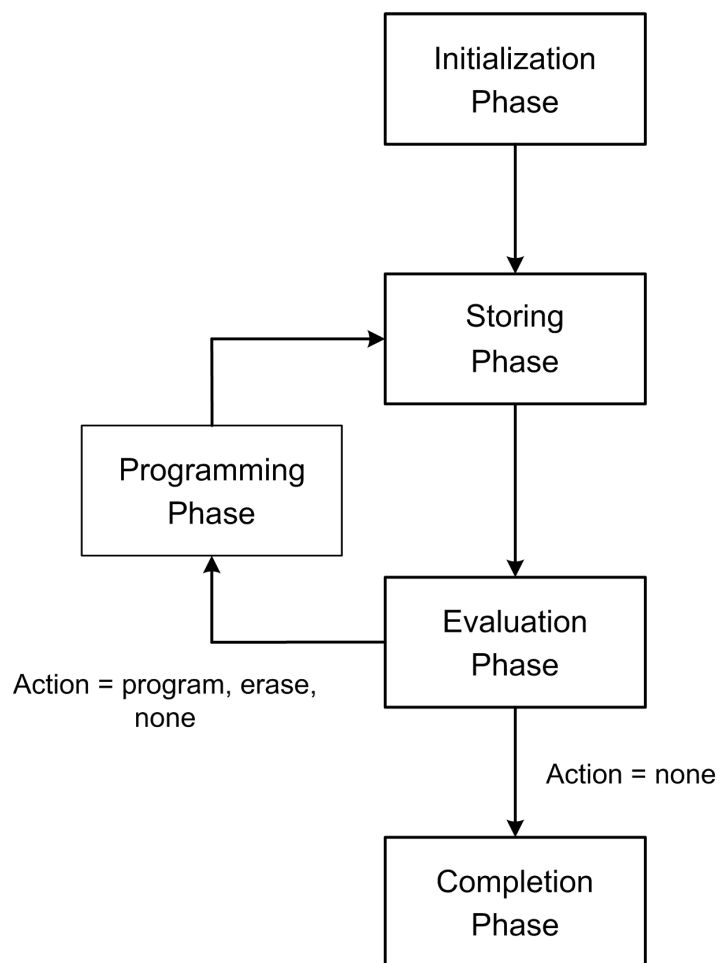
FIGURE 4.12. Procedure for floating-gate programming.

4.5.1.3. Evaluation Phase

In the evaluation phase, the analog states stored on the holding capacitors are compared to evaluate the programming action of the programming state. In the evaluation state, decisions are made on the action of the programming state depending on the analog states and the action taken in the last programming phase and also depending on the architecture of the floating-gate rectifier used. The programming action can be program (charge injection), erase (charge removal), or no action. The amount of time required for the evaluation phase may vary depending, for example, on the amount it takes to compare two analog states.

4.5.1.4. Programming Phase

In the programming phase, the gate voltages of the floating-gate rectifier are programmed to precisely control the amount of charge on the floating gate. The rectifier can be programmed by injecting charge to or removing charge from the floating gate depending on the decision from the evaluation phase. In the programming phase, all nodes that are not programmable are either grounded or left floating, however, it is preferable that they are grounded. All stages of the rectifier are programmed in the programming phase. The amount of time required for the programming phase can be varied depending on the pulse width of the programming signal and the amount of time it takes to generate one programming pulse.

4.5.1.5. Completion Phase

In the completion phase, most of the circuit blocks for floating-gate programming are disabled to conserve power once the floating-gate is appropriately programmed.

4.5.2. Ring Oscillator Circuits

Figure 4.13 12 shows the low frequency ring oscillator used to generate the enable pulse for the gate charging circuit. The ring oscillator is current starved to reduce power while causing the oscillator to oscillate at a very low frequency. A reference current is designed to generate the tail currents for the current starved oscillator. Each branch of the reference current as well as the tail current for the oscillator circuit draws 15 nA of current. The resulting oscillation frequency with a three-stage current-staved ring oscillator is in the hundreds of kilo Hertz. To reduce the frequency further, each oscillator stage is loaded by MOS capacitors (M_9-M_{14}) of approximately 20 pF each. Once each of the ring oscillator stages is equally loaded, the frequency of oscillation is reduced to below one kHz. The output of the ring oscillator is then buffered for a higher current drive and is then sent through the frequency divider circuit to further reduce the oscillation frequency.

Figure 4.14 shows the high frequency ring oscillator circuit. The ring oscillator consists of three stages that are equally loaded by two inverter stages. The output is buffered to increase the current drive of the ring oscillator. Figure 4.15 shows the schematic for the frequency divider circuit. The frequency is divided using 31 D-type flip-flops connected in series. The frequency divider circuits acts as a 31-bit ripple counter that counts up by 1 at the frequency of the slow ring
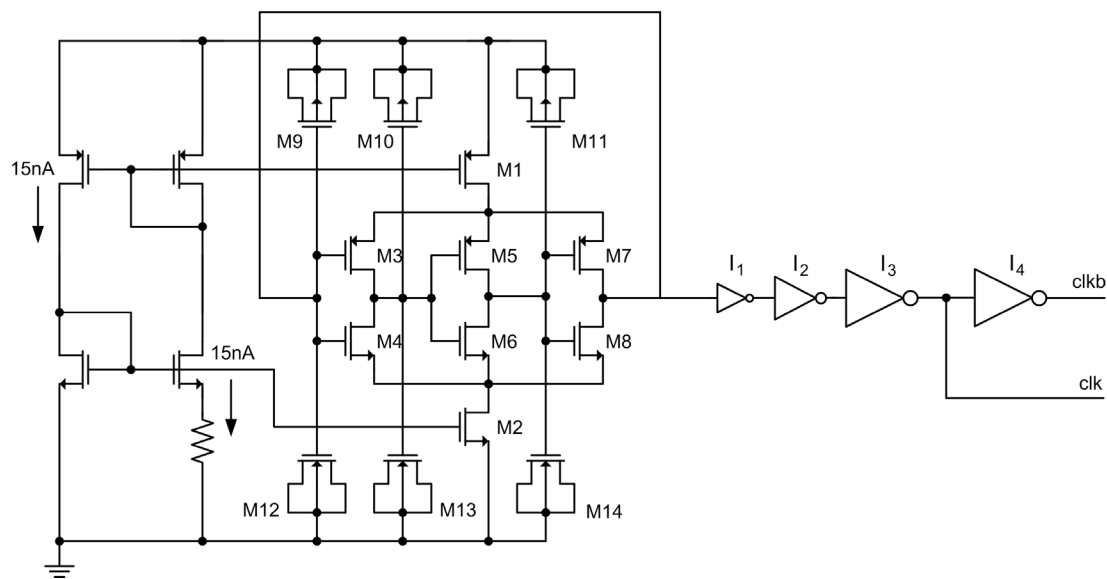
FIGURE 4.13. Low frequency ring oscillator.

oscillator circuit. This resulting frequency has a time period of approximately 1 month until the 31-bit ripple counter reset itself to an all-low stage. Through some combinational logic, the enable pulse is generated about once every month and lasts approximately 1/4 to 1/2 of a second, which is sufficient to replenish charge to the floating gate.

4.5.3. Voltage Boosters

Charge pump circuits used to generate the 8 V and -9 V boosted voltage. Figure 4.16 shows the Dickson charge pump used to generate the positive boosted voltage. With the opamp current as load to the voltage booster, a 2 MHz two phase clock is required to drive the output to the desired 8 V. To generate the
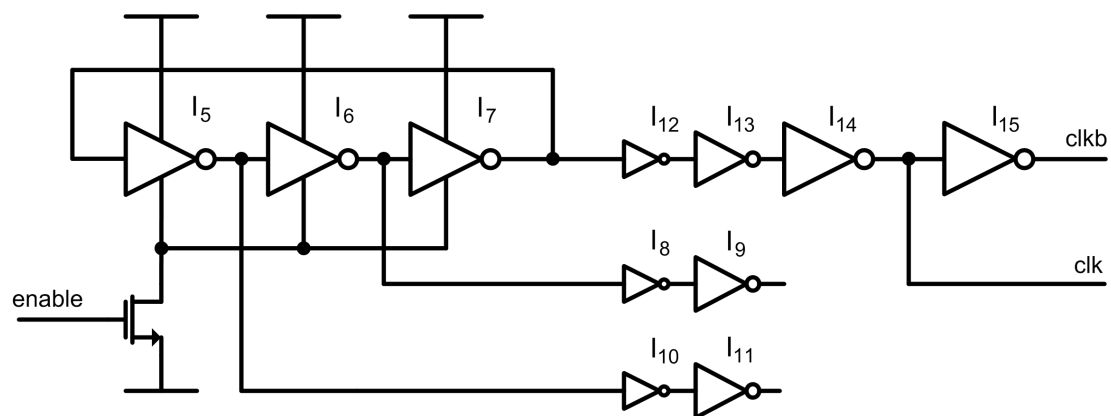
FIGURE 4.14. High frequency ring oscillator.
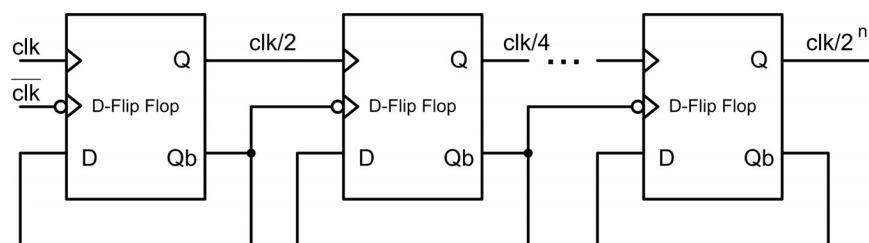
FIGURE 4.15. Frequency divider circuit.

negative boosted voltage, PMOS transistors are used and the diodes are connected in the reverse direction to generate the -9 V boosted voltage.
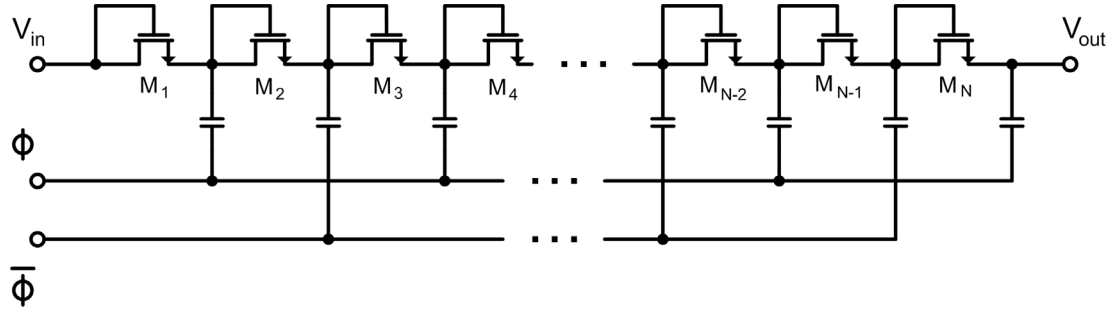
FIGURE 4.16. Dickson charge pump voltage booster circuit for positive voltage generation.

4.5.4. Low Voltage Regulator

To reduce the power dissipation of the floating-gate programming circuits by a few orders of magnitude, a second voltage regulator is designed to generate a voltage supply of 0.625V for the digital circuitry. The floating-gate programming circuit would consume power in the hundreds of milliwatts for up to 1 second operating with a 1.25V supply. The same programming circuit while running at a 0.625V supply would dissipate less than 10μW of average power.

4.6. Voltage Regulator Designs

Two linear voltage regulators are designed to efficiently down convert the output of the floating-gate rectifier circuit to an operable DC supply voltage. A 1.25V DC supply is generated to operate different devices while a 0.6V-0.7V supply

is generated to operate the digital circuitry in the floating-gate programming circuit. Since the output of the floating-gate rectifier circuit can range from 1-10 V DC, the voltage regulators must be robustly designed to handle high voltages without breaking down. The voltage regulator must also be designed with a very low quiescent current to maintain high efficiency in the RF energy harvesting system.

Figure 4.17 shows the basic schematic of the linear series voltage regulator [70]. The linear series voltage regulator consists of a voltage reference circuit, a resistor divider of R_1 and R_2, an opamp, pass transistor M_1 and sourcing capacitor C_1. A low-power on-chip voltage reference is needed on-chip to set a fixed output voltage for the voltage regulator throughout the power supply range from 1.2 V to 10 V and temperature range from -20°C to 60°C. A low-power opamp must be designed to operate in the nano-ampere current range. The output voltage is set by the resistive divider of R_1, R_2 and the reference voltage by the relation $V_{out} = V_{ref} * (1 + \frac{R_1}{R_2})$. During regulation, the opamp compares between the feedback voltage at the resistive divider and the reference voltage to control the current through the pass transistor. When the output voltage of the voltage regulator is lower than the desired regulated voltage, the opamp output voltage decreases and the current through the PMOS transistor M_1 is increased, causing V_{OUT} to increase. When V_{OUT} is greater than the desired regulated voltage, the opamp output voltage increases until the current through the pass transistor becomes lower than the load current of the regulator. The pass transistor can be turned off completely if the regulator is not driving a load. The sourcing capacitor C_1 is used to stabilize the regulator so that the regulator output voltage changes slow enough for the opamp output to respond. This is critical as the opamp must be designed in subthreshold with current in the nano-ampere range.
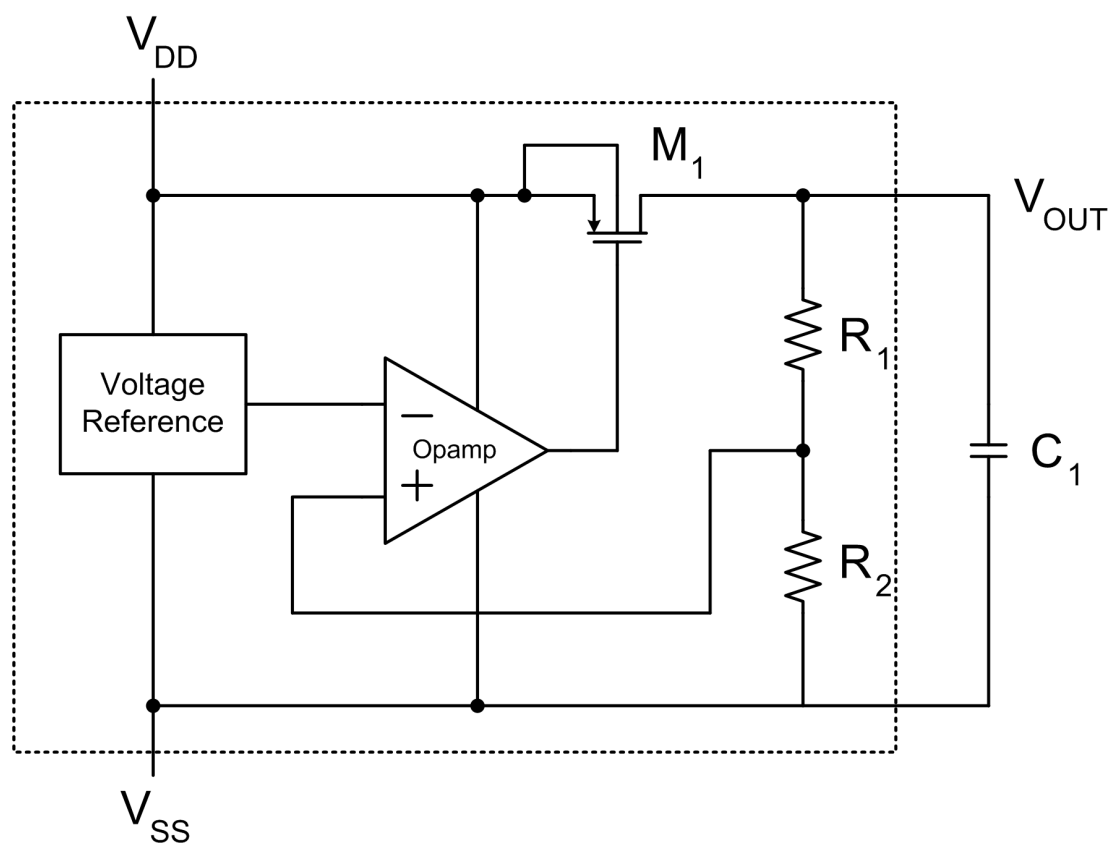
FIGURE 4.17. Linear voltage regulator.

The transistor level schematic of the two ultra-low power voltage regulators are shown in Figures 4.18 and 4.18 [70]. The general structure of both voltage regulators is the same with the exception of the different regulated voltages. The 1.25V regulator requires a resistive divider to generate the desired regulated voltage while the 0.625V regulator has its regulated voltage at the same level as the reference voltage, hence, does not require a resistive divider. The biasing circuitry for both voltage regulators can be shared to reduce static power dissipation. Both voltage regulators are designed to take input from the electric double layer capacitor (i.e. the Panasonic gold capacitor), which is known for its low leakage current modeled by a 10 MΩ resistor. The short circuit current for this capacitor is limited and thus is modeled with a kΩ resistor in series with the capacitor. The voltage regulators can also be driven directly by the rectifier if the power from the rectifier exceeds the power consumed by the device and regulator.

The bungee bias circuitry adaptively biases other circuit blocks to increase the oxide breakdown voltage of the regulators. A proportional to absolute temperature (PTAT) current reference is generated and an on-chip reference voltage is needed to generate a reference voltage used to generate the regulated voltages of 1.25V and 0.625V. The reference voltage is then fed into an opamp connected in a feed-back configuration to amplify the difference between the reference voltage and $\frac{R_2}{R_1+R_2}$ of the regulated voltage. A small capacitor is loaded on the reference voltage node to reduce effects from switching noise of the opamp and power supply noise from a change in the output voltage of the floating-gate rectifier. The output of the opamp drives pass transistors that control the current that flows through the load to maintain a constant output voltage. The design of each circuit block will be discussed in subsequent sections.
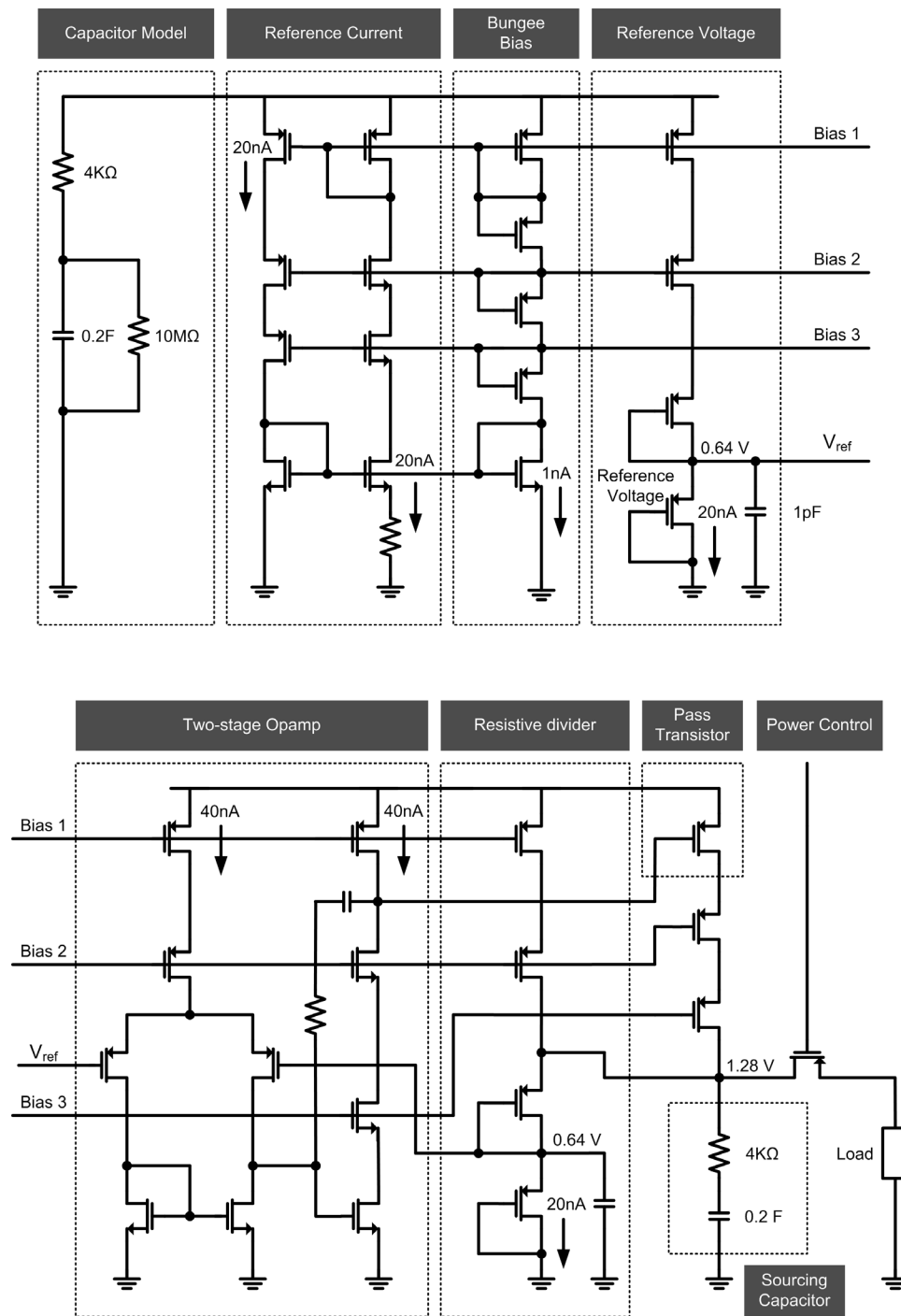
FIGURE 4.18. Transistor level schematic of 1.25 V voltage regulator with adaptive "bungee" biasing circuitry and electric double layer capacitor model for input and output loading.
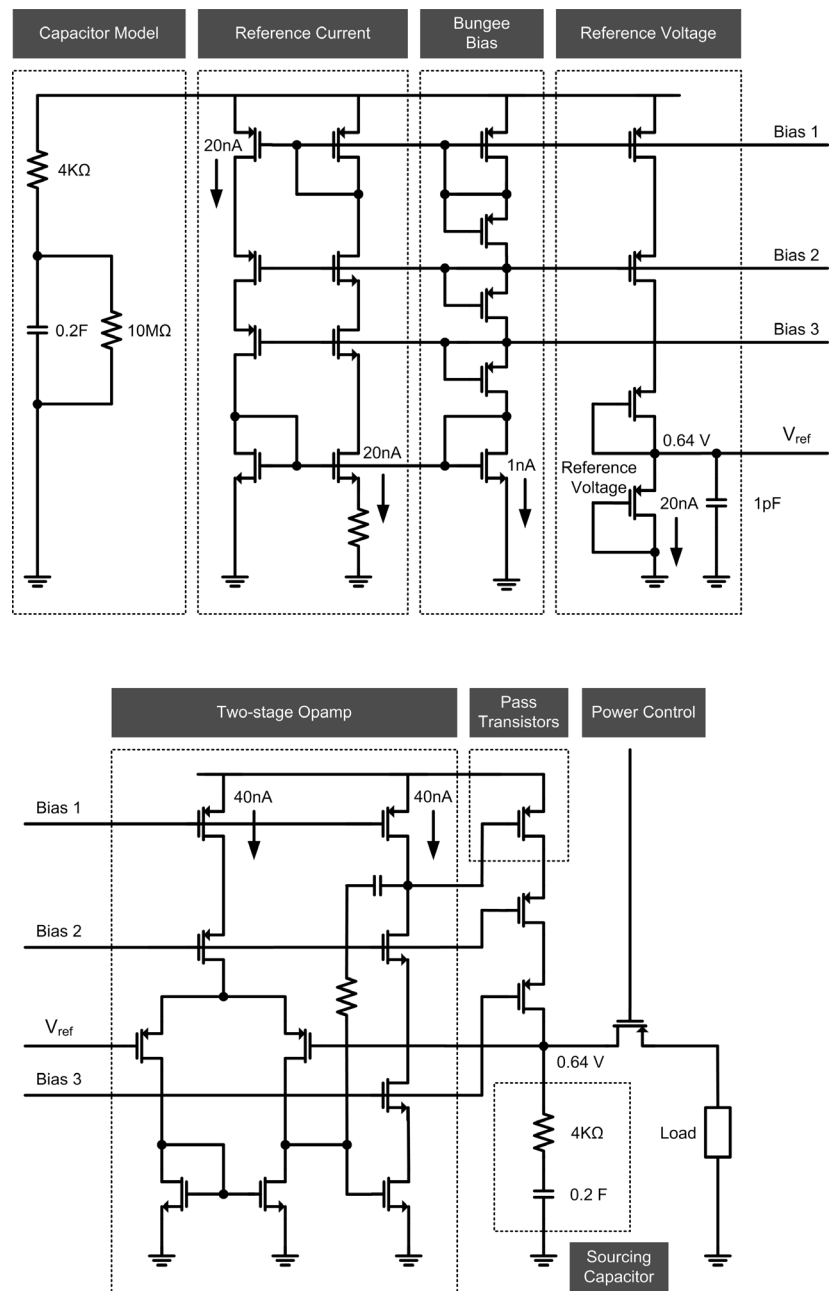
FIGURE 4.19. Transistor level schematic of 0.625V voltage regulator with adaptive "bungee" biasing circuitry and electric double layer capacitor model for input and output loading.

4.6.1. Adaptive Biasing Circuits

The voltage regulator is uniquely designed to achieve high breakdown voltage in a standard triple well CMOS process. No high voltage device or process modifications are needed in order to achieve a breakdown voltage of more than 10 V. N bias voltages can be generated from the cascoding of N-1 devices. The cascoded devices act as resistive dividers to divide the voltage between bias 1 and bias N. The devices can be linear (i.e., resistor) or non-linear (i.e. diodes or transistors). The design of the adaptive bias circuit may be optimized for low power dissipation by reducing the current that flows through the adaptive bungee bias circuitry. The voltage regulator schematic is designed with 3 series connected transistors in leakage mode to greatly reduce the quiescent current to less than a few nano-amperes.

The high breakdown voltage in the regulator is attained by the bungee bias circuit which uses leakage mode devices as resistive dividers to bias the reference current and other circuit blocks. The bungee bias circuit uses a double cascoded stack to prevent the gate-source and gate-drain voltage of any transistor from reaching the oxide break down voltage of 3.6 V (in 0.18-μm Jazz SBC process). Adding more cascoded devices increases the operable voltage of the regulator, however, the minimum supply voltage required for the voltage regulator is increased, and thus the dropout voltage is also increased. From simulation results, the minimum operable voltage is approximately 1.2 V at 27°C, and increases slightly at a lower temperature range.

4.6.2. Current Reference

A PTAT reference current is needed to design a reference voltage as well as generate a bias current for the opamp circuit. The PTAT reference current uses the simple supply independent current structure in a cascode configuration with cascoded transistors with adaptive bungee biasing for breakdown enhancement. The schematic of the reference current circuit is shown in Figure 4.18, and it consists of one resistor to set the reference current. A small PTAT voltage reference is established at the source of transistor M_1 which is converted to a PTAT current through resistor R_1. A low resistivity poly resistor is used to set the reference current of the voltage regulator as it has a lower and more linear temperature coefficient compared to the other types of resistors in the Jazz 0.18-μm process.

Biased in weak inversion, the reference voltage is $V_R = n\frac{kT}{q}ln(\frac{N_1}{N_2})$ when the source and bulk are connected together, where n is the slope factor, $\frac{N_1}{N_2}$ is the $\frac{W}{L}$ ratio of transistors M_1 and M_2, k is the Boltzman's constant, T is the temperature in degrees Kelvin, q is the electrical charge of an electron, where by $\frac{kT}{q}$ is 25.8mV at 27°C. When the source is tied to ground, $V_R = \frac{kT}{q}ln(\frac{N_1}{N_2})$ so the reference current $I_{REF} = \frac{V_{REF}}{R_1} = \frac{kT}{qR_1}ln(\frac{N_1}{N_2})$. With a $\frac{N_1}{N_2}$ ratio of $\frac{5}{3}$, and a resistor of 815 kΩ, the reference current at 27°C is 16.2 nA and the reference voltage is 13.2 mV. Figure 4.20 shows the reference current as a function of temperature and supply voltage.

The cascoded configuration of the bungee bias circuit enhances the current reference circuit in terms of linearity and supply rejection. This is essential since the current reference must be biased in weak inversion to reduce the quiescent power dissipation [71]. In subthreshold, where current is in the nanoamp range, the drain current of a MOS transistor increases exponentially with gate voltage

and current mismatch is increased with different drain-source voltages. The reduced drain-source voltage from cascoding reduces the dependence of the reference current on the supply voltage. Figure 4.20 shows the linearity of the PTAT reference current through the resistor in the current reference circuit. The plot shows good linearity with the bungee bias circuit throughout the desired temperature range from -20°C to 60°C. The PTAT current becomes less linear at input voltages of 1.2 V with temperatures less than 0°C. At voltages lower than 1.2 V, the majority of the voltage drop is in the drain-source junction of the cascoded device, effectively causing the current in the current mirror to slightly decrease. At lower temperatures, the threshold voltage of all the transistors increases, causing the reference current to decrease.

4.6.3. Reference Voltage

The reference current is mirrored to create a PTAT current in order to generate the reference voltage. The reference current is proportional to absolute temperature (PTAT) and the threshold voltage of a PMOS transistor is complimentary to absolute temperature (CTAT). Therefore, the PMOS transistor can be sized so that the temperature coefficient of the PTAT current and CTAT threshold cancel out giving a constant voltage throughout the temperature range of -20°C to 60°C. Typically, the threshold voltage of the high V_{TH} transistor is approximately 600 mV, by stacking and with appropriate sizing of the transistors; the desired 1.25V reference can be generated.
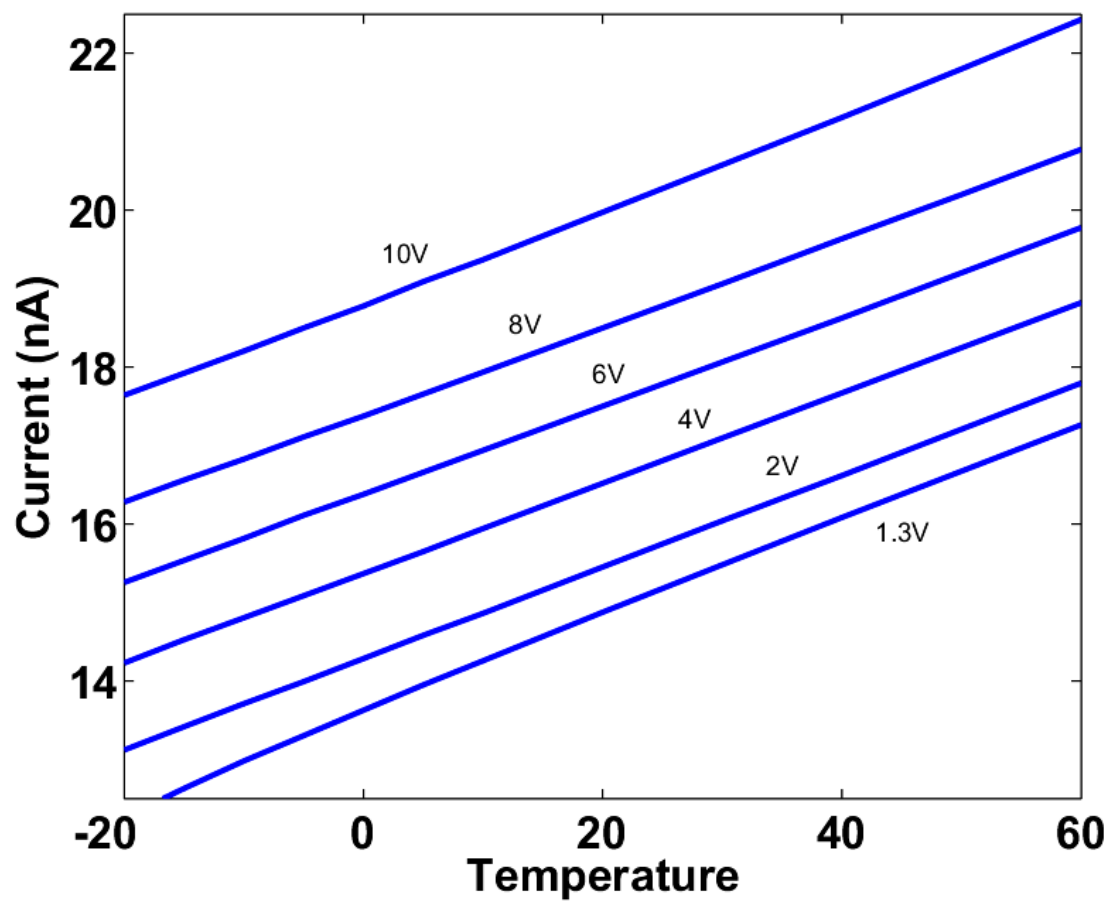
FIGURE 4.20. Linearity of PTAT current reference with bungee bias.

4.6.4. Opamp Design

The opamp used in the voltage regulator is a simple 2-stage opamp with cascoded output stage. The unique feature of this opamp is the ability to operate throughout a wide temperature and supply voltage range without suffering from oxide break down. The opamp uses regular CMOS transistors without any modifications to the process. The high breakdown feature is attained by the bungee bias circuit which biases the tail current for the differential pair in the 1st stage and the cascoded transistors in the 2nd stage of the opamp.

The opamp is designed to operate in the subthreshold current to reduce the quiescent power dissipation. The first stage and second stage are both biased with approximately 40 nA of current at 27°C. With a 1.2 V supply, the opamp can obtain a DC gain of 58 dB, unity gain bandwidth (UGBW) of 275 kHz and 48° phase margin when it is not loaded. The bandwidth is set by the Miller compensation capacitor C_1 as the capacitive load due to the pass transistor is much smaller compared to the compensation capacitor. The bandwidth compensation is done to keep the opamp stable at all frequencies below the unity gain bandwidth. The opamp draws a total current of 75 nA at 1.2 V, which is equivalent to 90 nW of dissipated power. With a 10 V supply, the opamp has a DC gain of 98 dB which is 40 dB higher than at 1.2 V supply. This is due to the higher g_m that the input transistors attain with a much higher V_{DS} when biased in subthreshold. The unity gain bandwidth at 10 V supply is 535 kHz and the phase margin is 60° when it is not loaded. With a 10 V supply, the opamp draws a current of 140 nA, which is equivalent to 1.4 μW of dissipated power.

4.6.5. Pass Transistors Switches

The pass transistor circuit controls the current that is delivered to the output capacitor and the load. The pass transistor circuit with series connected switches reduces the voltage drop across each transistor and prevents them from break down and failing. The pass transistors are biased via the adaptive "bungee bias circuit. The opamp output is connected to the top transistor of the series connected switch, which controls the current that flows through the pass transistors. The two transistors on the bottom control the voltage drop across each transistor equally.

4.6.6. Regulator Performance

The simulated transient response of both voltage regulators under different supply voltages is shown in Figure 4.21 and 4.22. A small output capacitance of 10 μF is used to speed up the simulation time. The tradeoff with a lower loading capacitance is a small variation in the regulated output voltage to remain stable. At higher supply voltages of 6 V and 10 V, the sourcing capacitor charges very quickly as the pass transistors are driven more strongly with a higher overdrive voltage (V_{GS} - V_{TH}). Also, at higher voltages the current available to charge the capacitor is higher in a relative sense. At lower supply voltages, the sourcing capacitor charges more slowly because the pass transistor voltage overdrive is low so the pass transistor switches are driven very weakly, thus less current can be sourced to the sourcing capacitor. It takes up to 60 ms to fully charge the sourcing capacitor with a 1.25 V power supply to the regulated voltage for the 1.25V regulator and less than 1 ms with a 10 V supply.
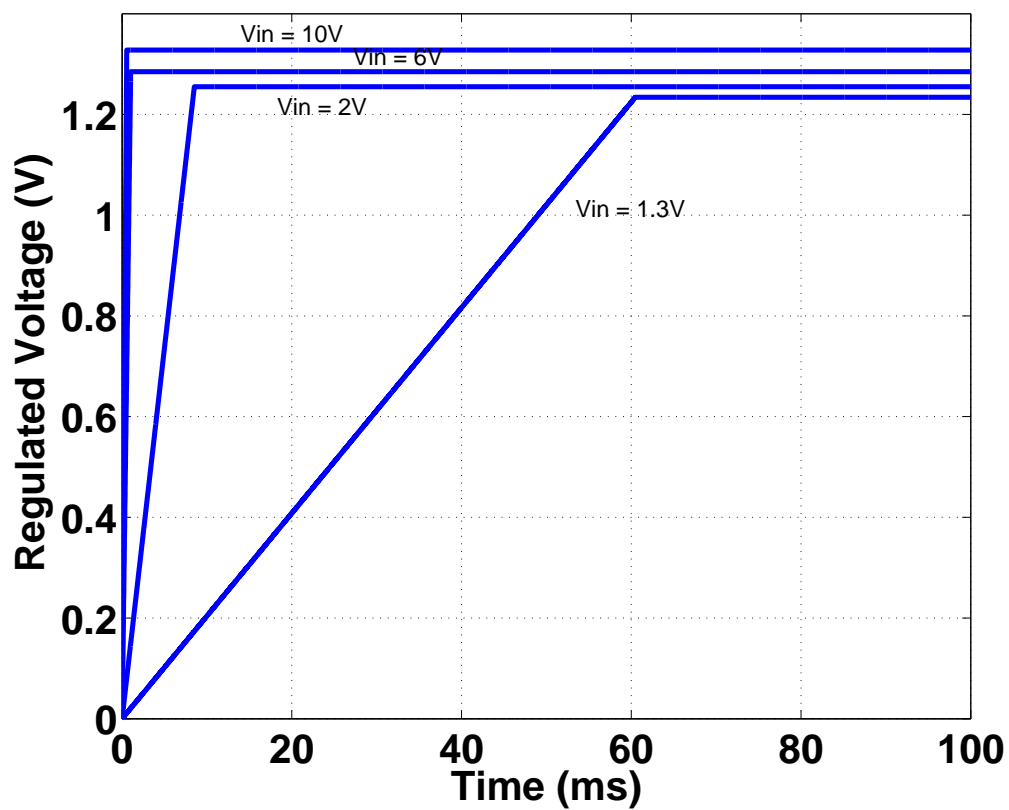
FIGURE 4.21. Transient response of the 1.25 V voltage regulator.
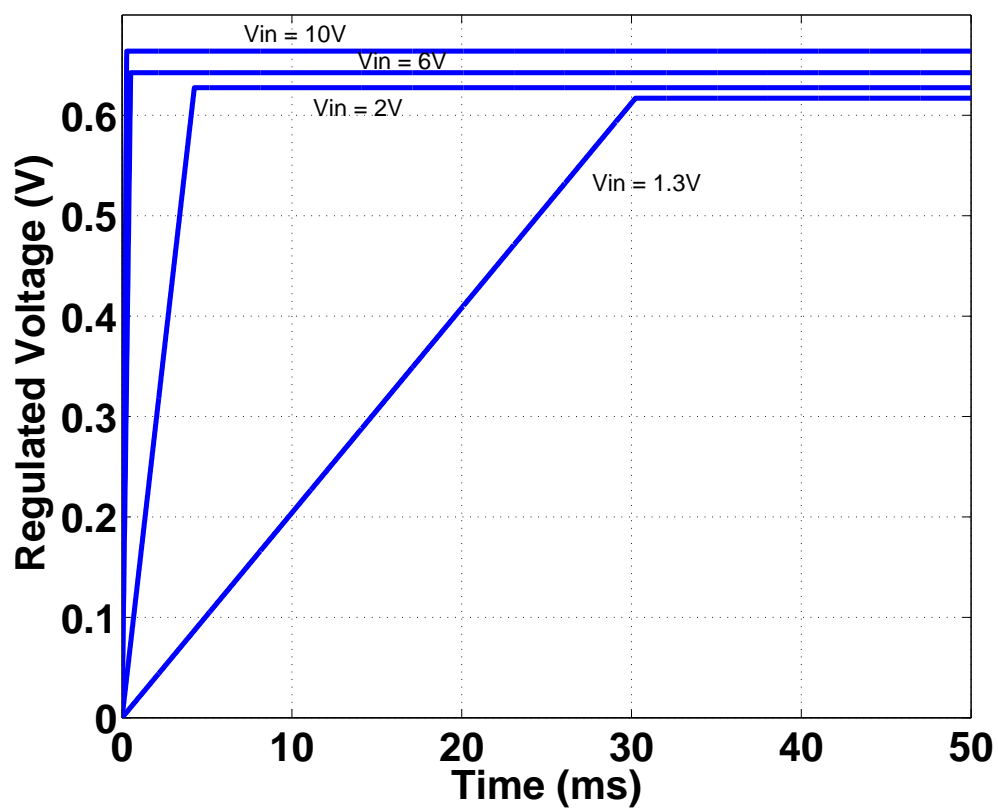
FIGURE 4.22. Transient response of the 0.625 V voltage regulator.

4.7. Measurement Results

The RF power conversion interface circuit which consists of a floating gate rectifier, floating-gate programming circuits and voltage regulators are designed and fabricated in a 0.18μm single-poly CMOS process. The die photograph of the power conversion interface circuit is shown in Figure 4.23. The active layout area of the floating-gate voltage doubler rectifier is 0.165 mm^2 (550 μm x 300 μm). The area for the voltage regulators are 0.062 mm^2 (225 μm x 275 μm), and the total area for the floating-gate programming circuit is 0.162 mm^2. The chip is packaged in a 32-pin QFN package with 0.5 mm pin pitch to reduce bond wire parasitics and trace lengths on the PCB.

4.7.1. Test Setup

In order to fully test the RF power conversion interface circuit, a test PCB is designed to test the functionality as well as the performance of each of the circuit blocks. Figures 4.24 and 4.25 shows the front and back-view of the test PCB, respectively. The chip is placed in the center of the board. Each of the chips has 2 similar copies of the RF power interface circuit that takes input from two antennas. The PCB allows the option of using a chip antenna or an SMA-type antenna. The output has the option of going to an off-chip voltage regulator for additional voltage regulation or connecting to a USB port to power certain portable devices.
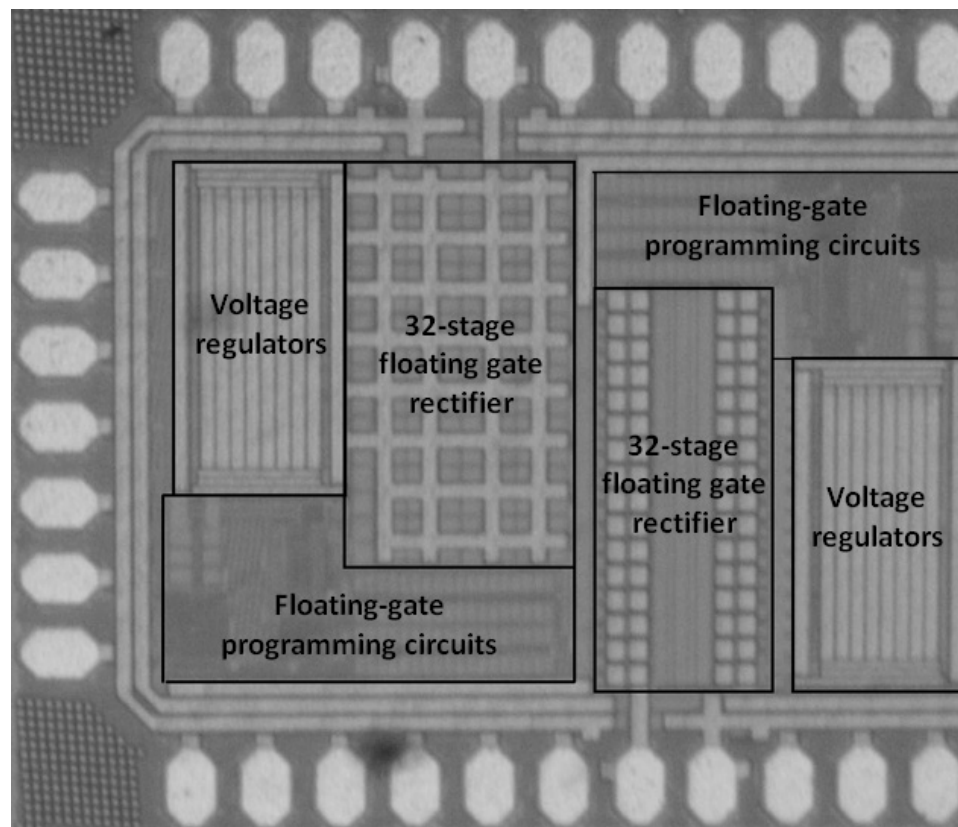
FIGURE 4.23. Die photograph of the RF power conversion interface circuits.
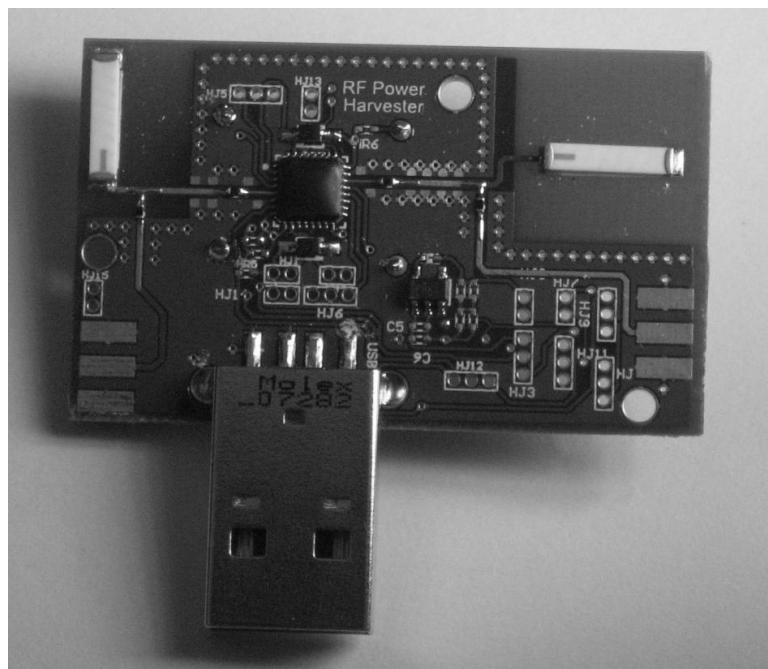
FIGURE 4.24. Photograph of the front-view test printed circuit board (PCB).
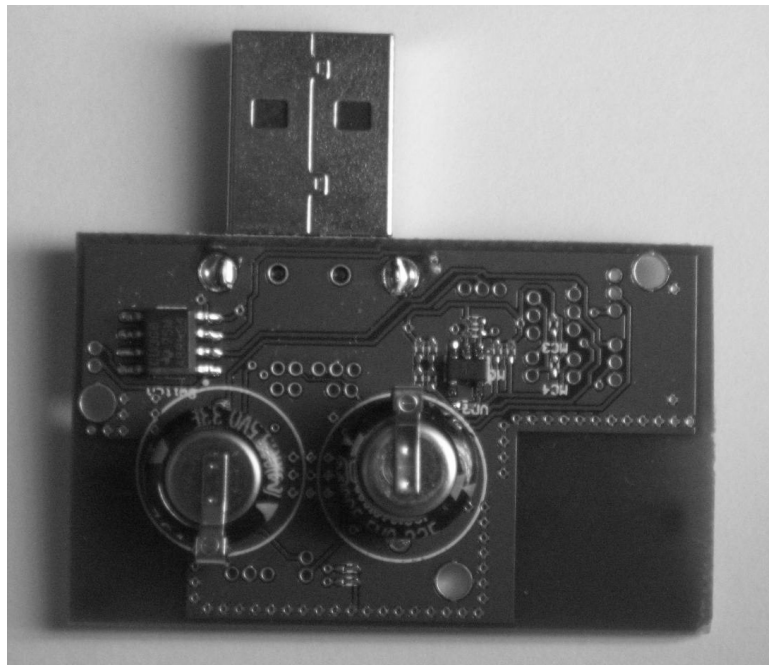
FIGURE 4.25. Photograph of the front-view test printed circuit board (PCB).

4.7.2. Floating-gate Rectifier Measured Results

Figure 4.26 shows the performance of the floating-gate rectifier circuit at various input signal amplitudes. An output voltage of up to 12 V can be achieved at the output with an input amplitude of 250 mV. From a straight line extrapolation of the output curve, the effective threshold of the floating-gate rectifier can be found to be between 35-50 mV after floating-gate programming.
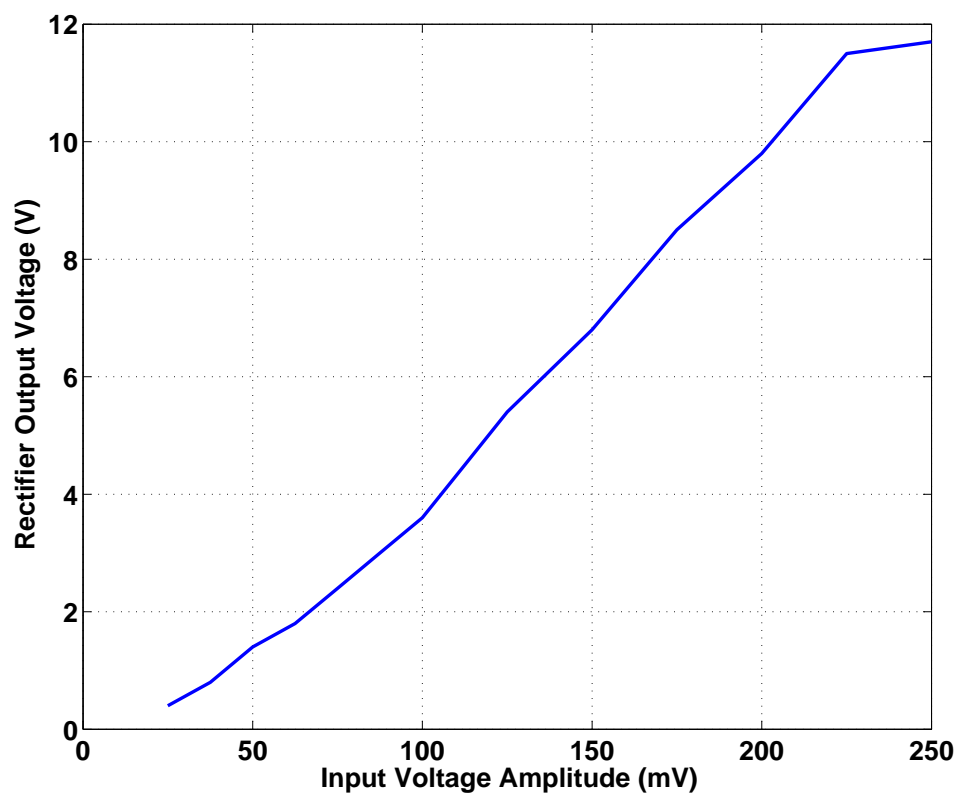
FIGURE 4.26. Measured output voltage performance of the unloaded floating–gate rectifier as a function of input voltage.

4.7.3. Floating-gate Programming Measured Results

Figure 4.27 shows the oscillation frequency of the low frequency ring oscillator circuit at various supply voltages. With the 0.625 V supply, the oscillation frequency of the ring oscillator is approximately 700 Hz. Once the output stage of the ring oscillator is fed into a 31-bit ripple counter, it takes approximately 36-days for the states in the ripple counter to repeat. Through some combinational logic, the mean time between programming intervals is 36 days. Figure 4.28 shows the time between floating-gate programming intervals as a function of supply voltage.

Figure 4.29 shows the output voltage curve for the voltage booster at various supply voltages. With the Dicksons charge pump, a boosted supply of up to 10 V can be generated from a 1 V supply. This 10 V supply is adequate to be used in the programming and deprogramming of the floating-gate rectifier circuit.

4.7.4. Voltage Regulator Measured Results

The measured regulated voltage output is shown in Figure 4.30. The output is fairly constant over the full input range from 1.3V to 10V. The variation in the regulated voltage is 30 mV (2.3 %) with quiescent current measured below 150nA. Through experimental observation, the voltage regulator with bungee bias circuitry operates at over 12 V without suffering from oxide breakdown. Application of higher voltages is not possible since the reverse breakdown voltage of the process is approximately 12 V.

Figure 4.32 shows the PSRR at DC for various input voltages. The PSRR is highest in the middle range of voltage where it is greater than 40 dB for voltage from 1.4 to 10.8 V.
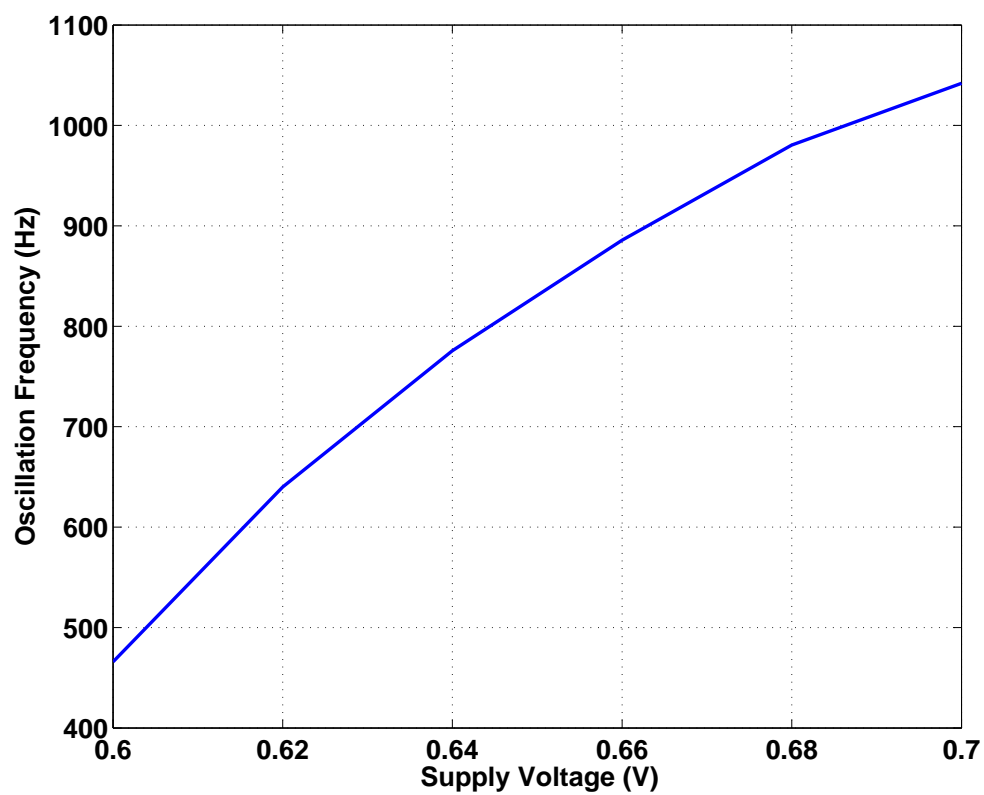
FIGURE 4.27. Measured oscillation frequency as a function of regulated supply voltage.
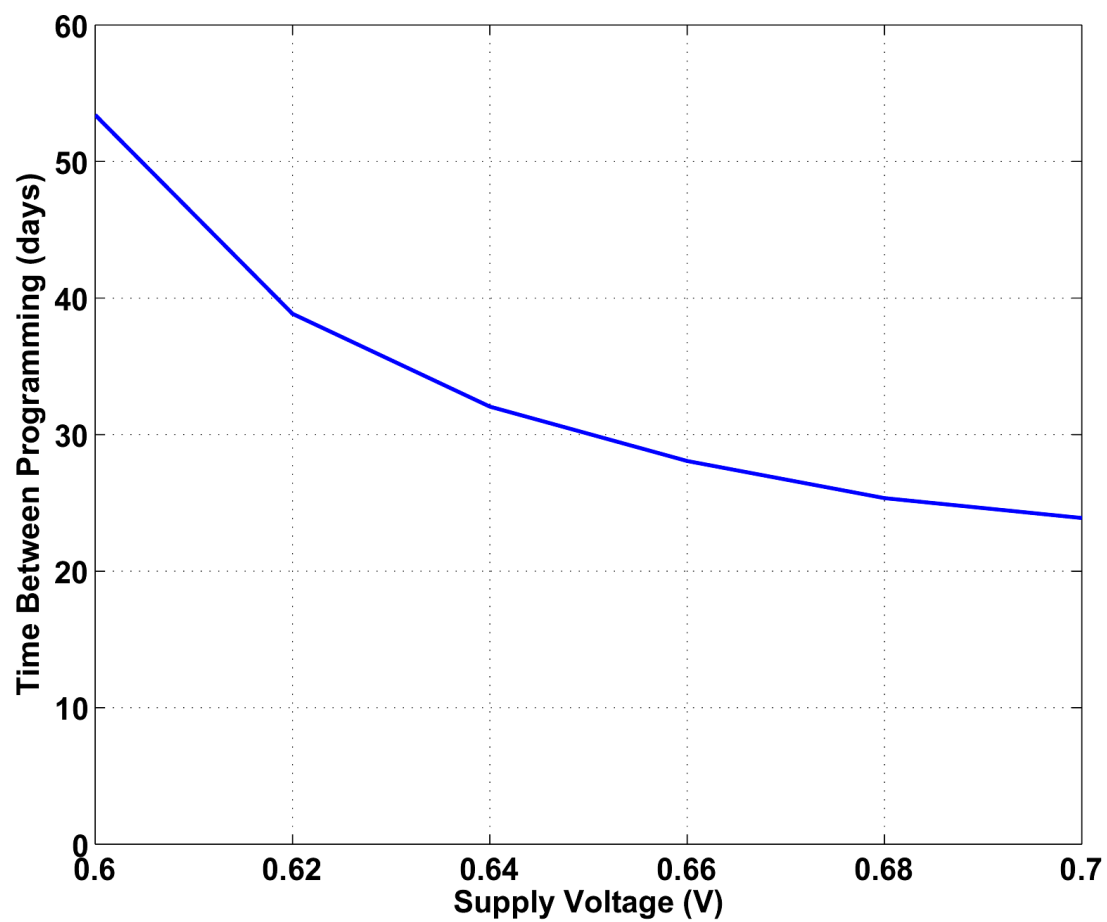
FIGURE 4.28. Time between floating-gate programming intervals.
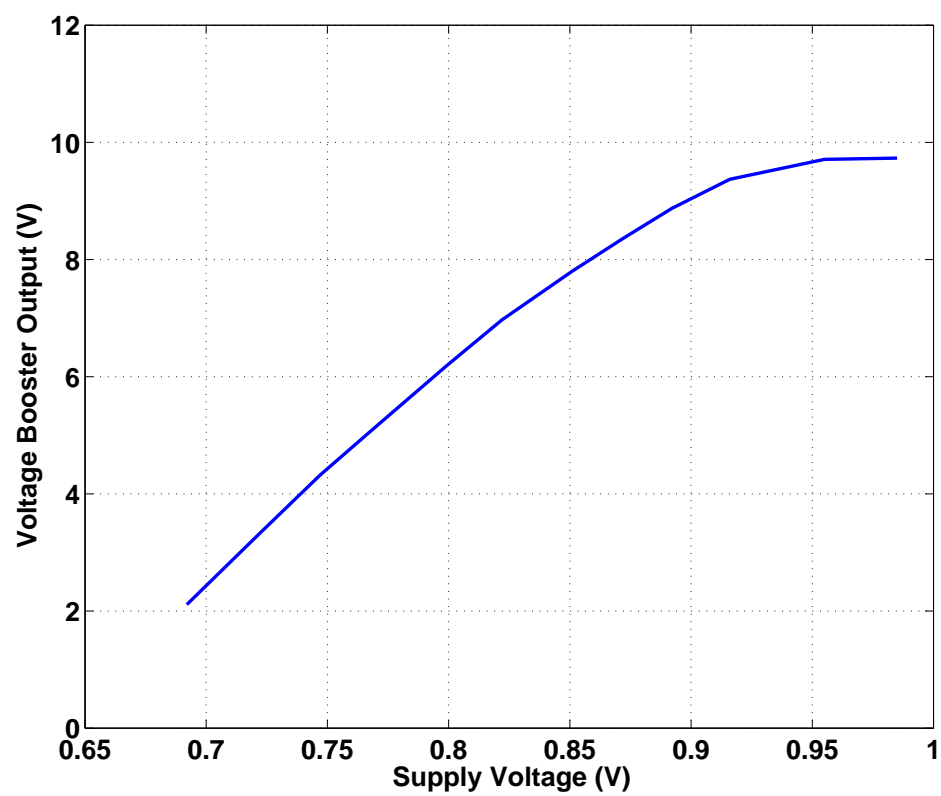
FIGURE 4.29. Measured boosted output voltage as a function of supply voltage.
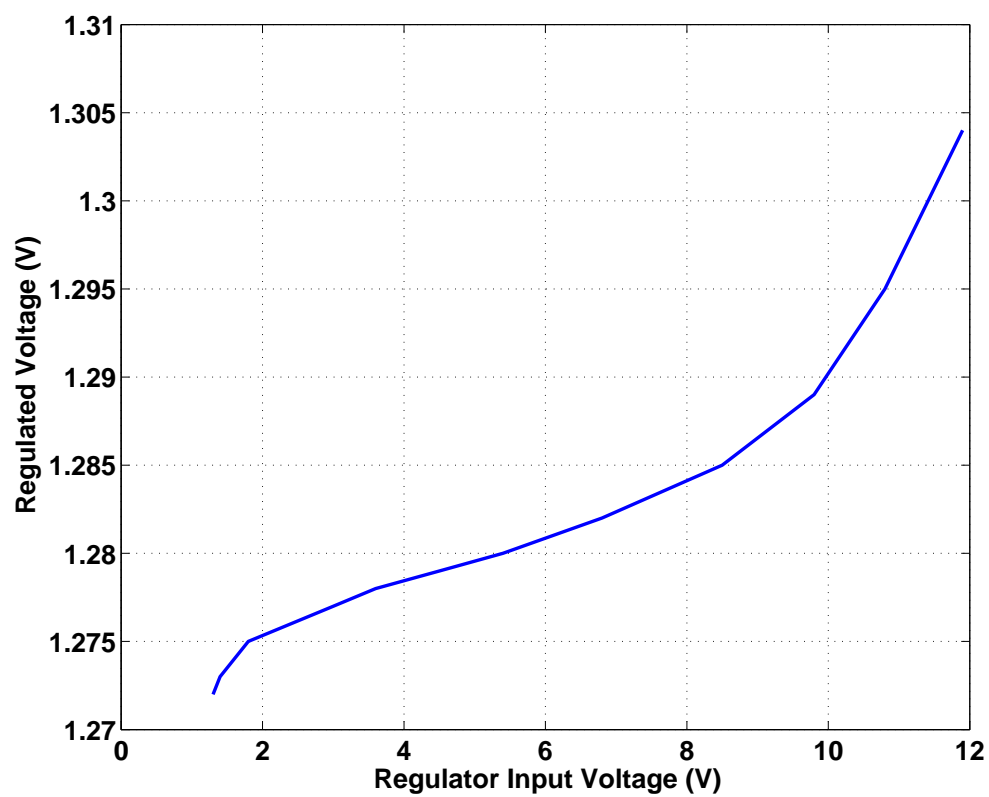
FIGURE 4.30. Measured regulated voltage as a function of the power supply voltage for the 1.25 V voltage regulator.
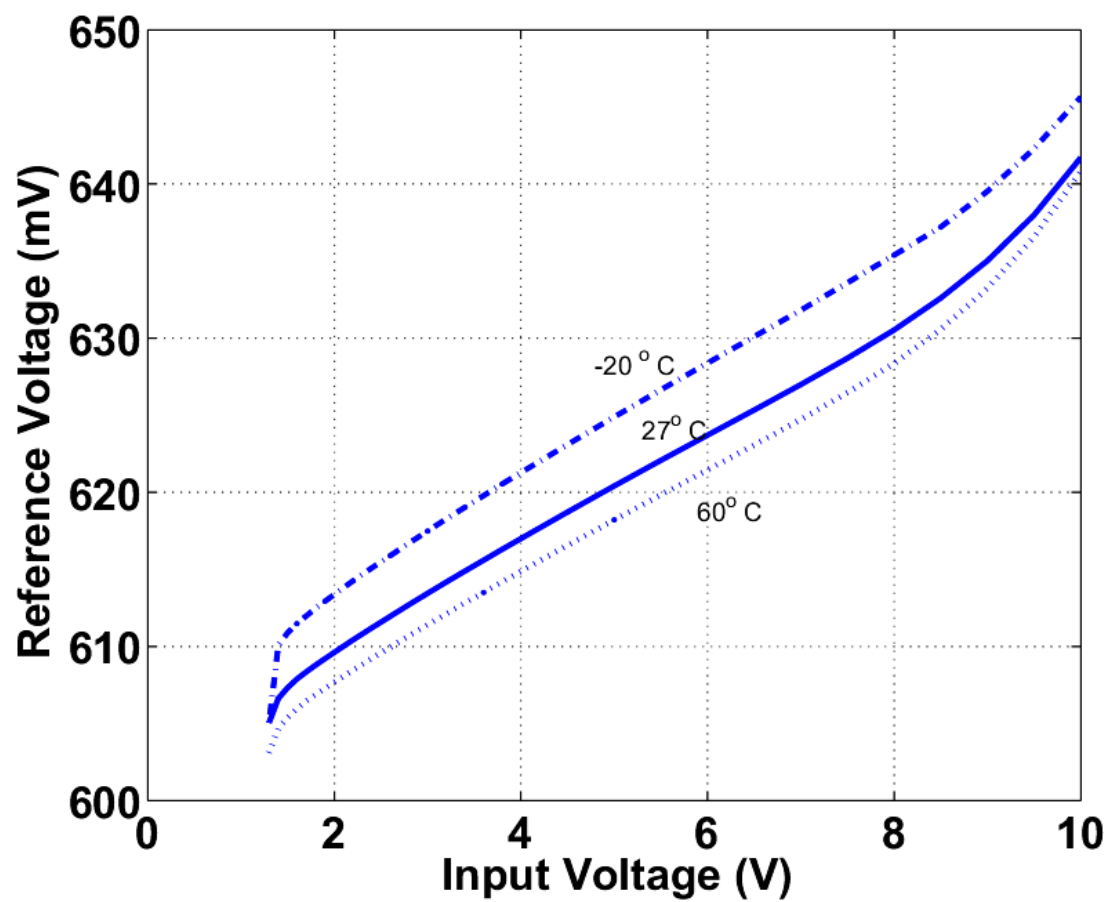
FIGURE 4.31. Measured regulated voltage as a function of the power supply voltage for the 0.625 V voltage regulator.
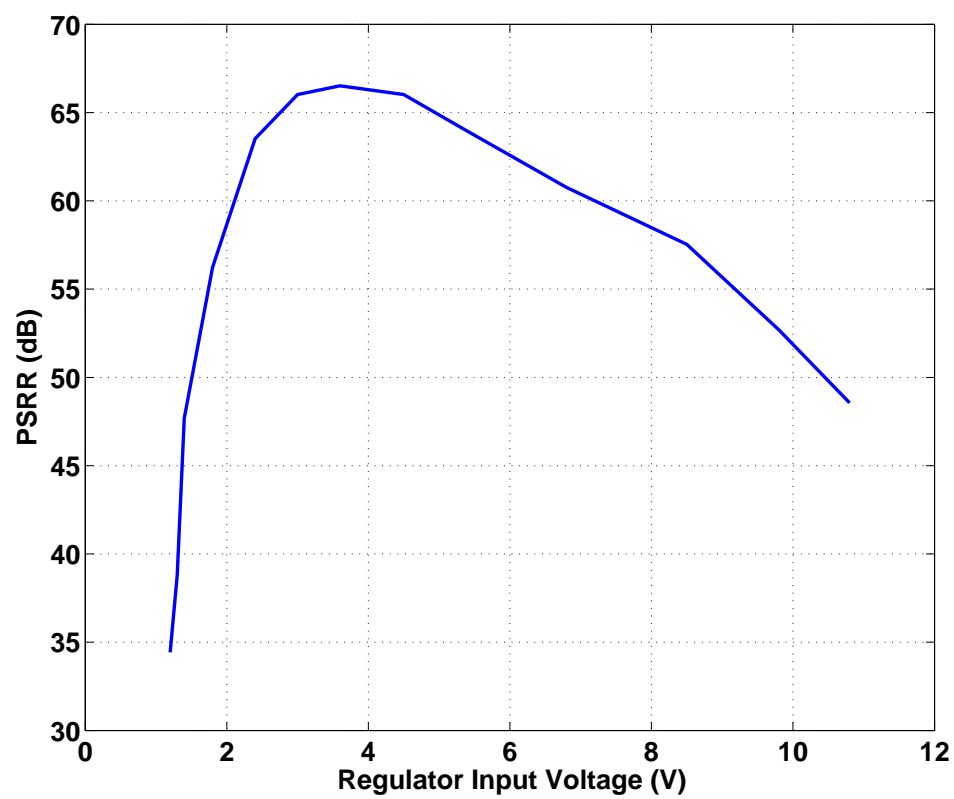
FIGURE 4.32. Measured (DC) power supply rejection ratio (PSRR) of the 0.625 V regulator.

4.7.5. Power Harvester Performance

The performance of the RF power conversion circuitry with a wireless input is shown in Figures 4.33 to 4.35. A high intensity RF signal is transmitted through a dipole antenna at 900 MHz and the RF signal is received by a similar antenna at the power harvester. The voltage at the output of the voltage regulator is measured. Figure 4.33 shows the output voltage as a function of peak input power with 50 kΩ, 300 kΩ and 10 MΩ loads. A stable power supply above 1.0 V can be generated continuously at peak input power as low as -22 dBm for a 1 MΩ load. The power conversion efficiency of the power harvester is shown in Figure 4.34. Optimized for far-field operation, the power harvester has peak efficiency of 51% at -15 dBm input power, corresponding to approximately 10 meters operating distance [4]. Figure 4.35 shows the peak output power performance of the power harvester at various input power. A power draw of 1-μW is possible at an input power as low as -22 dBm, or 10-μW at an input power of -14 dBm.

4.8. Conclusion

An energy harvesting system is shown with voltage regulation circuits and floating-gate programming. Measured results and characterization of the voltage regulators, floating-gate programming circuits, and the RF power harvester are presented. The voltage regulators are shown to operate at voltages exceeding 10 V without suffering from oxide breakdown while dissipating sub-microamp currents. The floating-gate programming circuit is measured with power dissipation in the microwatt range. A low frequency ring oscillator is measured to operate at about 800 Hz while dissipating less than 30 nW of average power. This low frequency oscillator drives a ripple counter that enables the floating-gate programming circuit
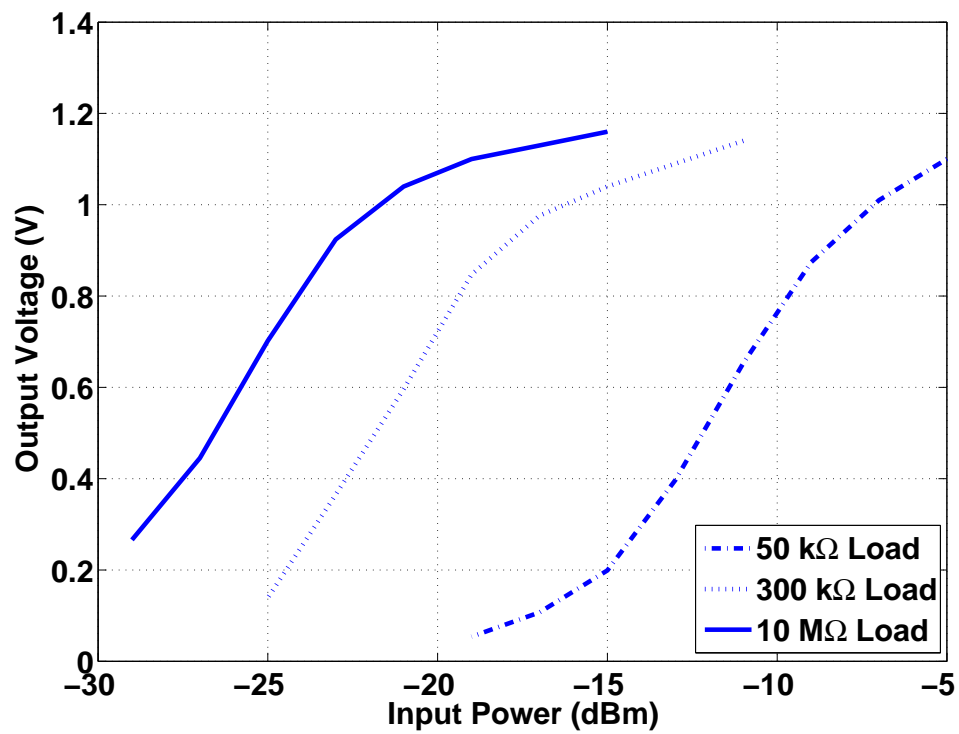
FIGURE 4.33. Measured output voltage performance of RF power harvester.
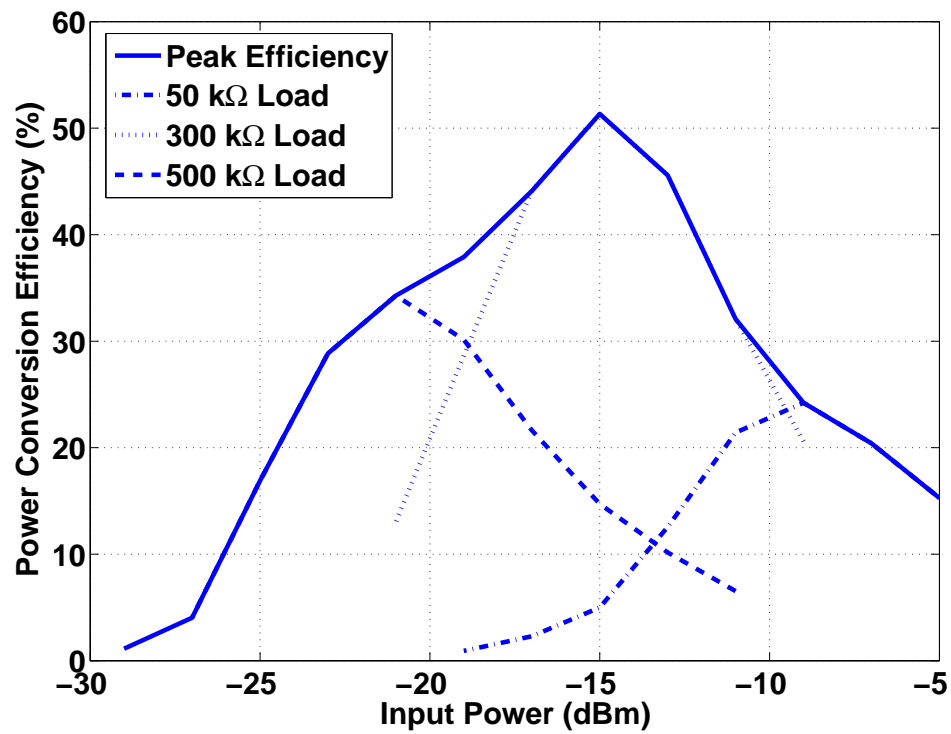
FIGURE 4.34. Measured power conversion efficiency of RF power harvester.
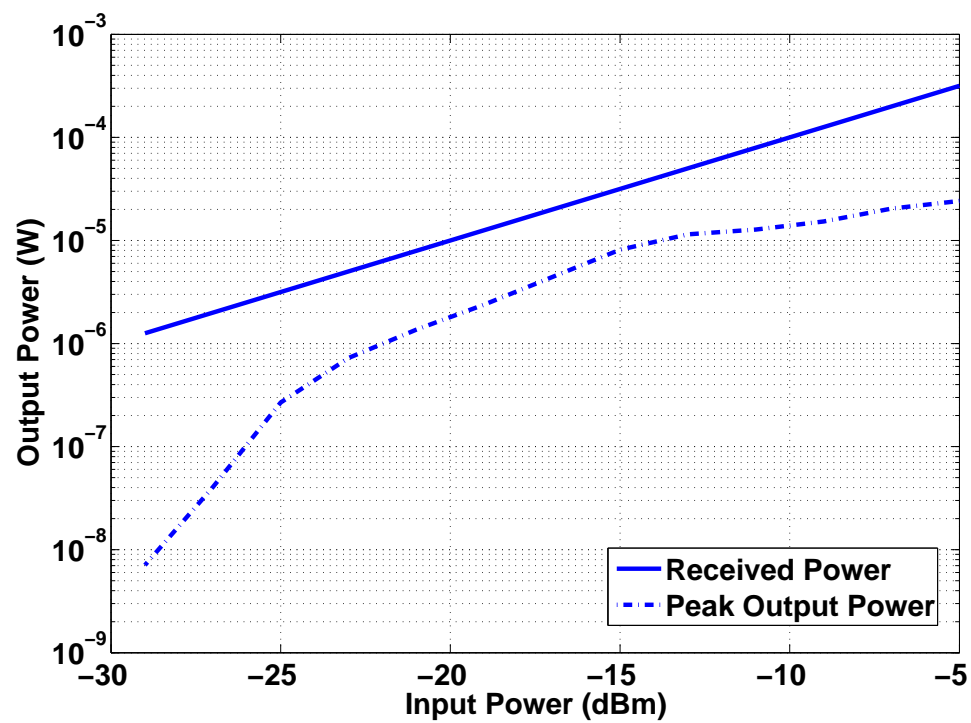
FIGURE 4.35. Measured output power performance of RF power harvester.

approximately once a month. The RF power harvester has measured efficiency of more than 50% and output power of more than 10-W at 10 meters distance.

The floating-gate programming circuit replenishes charge from the floating-gate rectifier to enhance the usable lifetime of the floating-gate rectifier. The replenished charged keeps the floating-gate rectifier at the most optimized efficiency, thus, increasing its effective distance and harvested energy over time. The increase in the harvested energy from floating-gate programming is more significant than the energy spent in the floating-gate programming process. This increase in harvested energy varies with distance and time between charging of the floating-gate. Up to 10% improvement in harvested power can be achieved in the most optimal case.

5. CONCLUSION

5.1. Conclusion

For this work, a summary of different energy harvesting methods in terms of energy density is performed. It is observed that the RF and piezoelectric energy harvesting methods give the best power density under standard environmental conditions. These methods allow the circuitry they power to be self-sustaining in different environments. Low RF power is available in large cities as well as close to TV and cell phone towers and low level vibrations normally occur in many commercial buildings as well as in cars, ships, trains, and aircrafts. Novel power conversion interface circuits are designed to provide further improvements in power conversion efficiency of these power harvesting methods.

An electrical model of a 2.45 mm x 2.45 mm piezoelectric membrane is developed to generate a voltage signal as a function of time and excitation frequency. A study of different rectifier structures is done to compare between their advantages and disadvantages. Different rectifier architectures with half-wave and full-wave rectification as well as passive and active circuits are studied and analyzed. These passive and active rectifier circuits show great improvement compared to conventional diode rectifiers. The passive rectifier circuit can generate 16 μW of power while achieving a peak power conversion efficiency of 65%. It achieves 20-30% improvement over traditional Schottky diode-based rectifier circuits, which is what it is designing to replace. The piezoelectric power interface circuit is capable of producing 22 μW of power while achieving a peak power conversion efficiency of 85% with the active rectifier based-on synchronous rectification. It is still one of the most efficient active rectifiers based on synchronous rectification for micro-power applications.

A far-field RF power conversion circuit is demonstrated at operating frequencies in the UHF range 902-928 MHz. The 36-stage rectifier design that is presented shows incredible improvement compared to previous published works as well as conventional rectifier circuits. The novel rectifier circuits are designed and demonstrated to work with signals as low as 50mV and have a maximum measured efficiency of 60%. This increase in power conversion efficiency allows an increase in the operable distance between the circuit and the radiation source. The system operates with a received power threshold as low as -22.6 dBm (5.5μW), corresponding to 44 meters distance in free-space with a 4W radiation source. A measured distance of 15 meters is achieved with 1 volt DC and a 0.3μA load current in a shielded environment. The power harvester has the best reported power conversion efficiency as well as operating distance to this day. The power harvester can be extended to be used in other methods of energy harvesting to provide slow charging of devices.

Power management circuits are necessity to limit the voltage and control the current that can be charged to power storage devices and devices. Voltage regulator circuits are designed to limit the voltage from the RF power conversion circuit and floating-gate programming circuits are designed to replenish the charge on the floating-gate devices. Measured results and characterization of the voltage regulators and floating-gate programming circuits are presented. The voltage regulators are shown to operate at voltages exceeding 10 V without suffering from oxide breakdown while dissipating less than 150 nA of currents. A low frequency oscillator is designed as part of the wake-up circuitry for the floating-gate programming circuits. The oscillator frequency is measured at 800 Hz while dissipating less than 30 nW of power. The duration between floating-gate programming du-

ration is controlled by a 31-bit ripple counter that is enabled approximately once every month.

The floating-gate programming circuit replenishes charge from the floating-gate rectifier to enhance the usable lifetime of the floating-gate rectifier. The replenished charge keeps the floating-gate rectifier at the most optimized efficiency, thus, increasing its effective distance and harvested energy over time. Up to 10% improvement in harvested energy can be achieved with the floating-gate programming circuit.

5.2. Future Work

With novel power conversion interface circuits designed to efficiently convert piezoelectric and RF energy to DC power, additional work must be done to further improve the performance of these circuitry. For the piezoelectric device, voltage regulation or DC-DC conversion may be done to stabilize the output voltage of the power conversion interface circuits and improve power conversion efficiency of the system. A maximum power point tracking (MPPT) may also be designed to adjust the load of the piezoelectric interface circuit to operate at the maximum power transfer point.

For the RF power conversion interface circuit, further work can be done on the floating-gate rectifier circuit to further reduce the power dissipation of the floating-gate programming circuit and connect these circuit blocks as a feedback system as on a single integrated chip. Also, more experiments can be performed on the floating-gate programming circuits to further characterize each of the circuit blocks so they can be integrated into a single integrated system.

BIBLIOGRAPHY

[1] K. Finkenzeller, RFID Handbook: Fundamentals and Applications in Contactless Smart Cards and Identification, John Wiley, Chicester, Sussex, Second edition, 2003.

[2] A.-L. Annala, I. Oy, and U. Friedrich, Passive long distance multiple access UHF RFID system (RFID), Palomar Project, European Commission, Public Report, Project Number IST1999-10339, Nov. 2002.

[3] J. B. Lee, Z. Chen, M. G. Allen, A. Rohatgi, and R. Ayra, "A high voltage solar cell arrays as an electrostatic MEMS power supply," in *Proc. IEEE Workshop on Micro Electro Mechanical Systems*, Jan. 1994, pp. 331-336.

[4] J. B. Lee, Z. Chen, M. G. Allen, A. Rohatgi, and R. Arya, "A miniaturized high voltage solar cell array as an electrostatic MEMS power supply," *IEEE/ASME Journal of Microelectromechanical Systems*, vol. 4, no. 3, pp. 102 108, Sep. 1995

[5] S. J. Roundy, "Energy Scavenging for Wireless Sensor Nodes with a Focus on Vibration to Electricity Conversion, PhD Thesis, The University of California, Berkeley, Department of Mechanical Engineering, 2003.

[6] N. Penglin, P. Chapman, "Design and Performance of Linear Biomechanical Energy Conversion Devices," *37th IEEE Power Electronics Specialists Conference*, pp. 1-6, June 2006.

[7] S. M. Gim, "Proposal on the conversion of room temperature thermal energy into useful form," in *Procs IEEE Power Engineering Society Summer Meeting*, pp. 1352-1356, July 2001.

[8] V. Leonov, T. Torfs, P. Fiorini, C. Van Hoof "Thermoelectric Converters of Human Warmth for Self-Powered Wireless Sensor Nodes," *IEEE Sensors Journal*, Vol. 7, pp. 650-657, May 2007.

[9] T. Le, J. Han, A. von Jouanne, K. Mayaram, and T.S. Fiez, "Piezoelectric power generation interface circuits," in *Proc. of IEEE Custom Integrated Circuit Conf. (CICC)*, Sep. 2003, pp. 489-492.

[10] M. Renaud, T. Sterken, A. Schmitz, P. Fiorini, C. Van Hoof, R. Puers, "Piezoelectric Harvesters and MEMS Technology: Fabrication, Modeling and Measurements," *International Solid-State Sensors, Actuators and Microsystems Conference*, pp. 891-894, June 2007.

[11] K. Fotopoulou, B. W. Flynn, "Wireless Powering of Implanted Sensors using RF Inductive Coupling," *5th IEEE Conference on Sensors*, pp. 765-768, Oct. 2006

[12] Triet Le, Karti Mayaram, and Terri S. Fiez, "Radio Frequency Power Harvester," United States Provisional Patent, DBI0529223, Sept. 2007.

[13] J. U. M. Araiza, Wireless transmission of power for sensors in context aware systems, Masters Thesis, Massachusetts Institute of Technology, Department of Electrical Engineering and Computer Science, June 2002.

[14] T. Le, K. Mayaram, T. S. Fiez, Efficient far-field radio frequency power conversion system for passively powered sensor networks, *IEEE Custom Integrated Circuits Conference (CICC)*, pp. 293-296, Sept. 2006.

[15] M. Sudou, H. Takao, K. Sawada, M. Ishida, "A Novel RF Induced DC Power Supply System for Integrated Ubiquitous Micro Sensor Devices," *International Solid-State Sensors, Actuators and Microsystems Conference*, Page(s):907 - 910, June 2007

[16] FCC Codes of Regulation, Part 15 [Online]. Available: http://www.access.gpo.gov/nara/cfr/waisidx_03/47cfr15_03.htm

[17] H. T. Friis, "A note on a simple transmission formula," *Proceedings of the Institute of Radio Engineers and Waves and Electron*, vol. 34, pp. 254-256, May 1946.

[18] K.-S. Leong, M. L. Ng, and P. H. Cole, "The Reader Collision Problem in RFID Systems" *IEEE Proceedings of International Symposium on Microwave, Antenna, Propagation and EMG Technologies for Wireless Communications*, vol. 1, pp. 658-661, August 2005.

[19] T. S. Rappaport, Wireless Communications. Principles and Practice, Prentice Hall, Second Edition, 2002.

[20] T. Stamer, "Human-powered Wearable Computing," *IBM Systems Journal*, vol. 35, pp. 618-629, 1996.

[21] N. S. Shenck, J. A. Paradiso, "Energy Scavenging with Shoe-Mounted Piezo-electrics," *IEEE Micro*, vol. 20, pp. 30-41, 2001.

[22] G. H. Gautschi, Piezoelectric Sensorics Force, Strain, Pressure, Acceleration, and Acoustic Emission Sensors 6th ed., Springer Verlag, 2002.

[23] C. B. Williams, C. Shearwood, M. A. Harradine, P. H. Mellor, T. S. Birch, R. B. Yates "Development of an electromagnetic micro-generator," *IEEE Proceedings-Circuits, Devices and Systems*, vol. 148, No. 6, pp. 337-342, Dec. 2001.

[24] S. Roundy, P. K. Wright, and J. Rabaey, "A study of low level vibrations as a power source for wireless sensor nodes," *Computer Communications*, vol. 26, no. 11, pp. 1131-1144.

[25] A. Luque, S. Hegedus, Handbook of Photovoltaic Science and Engineering. John Wiley and Sons, 2003.

[26] O. Schultz, R. Preu, S. W. Glunz, and A. Mette "Silicon Solar Cells with Screen-Printed Front Side Metalization Exceeding 19% Efficiency," *22nd European Photovoltaic Solar Energy Conference and Exhibition*, Sept. 2007.

[27] University of Delaware. "University Of Delaware-led Team Sets Solar Cell Record." *ScienceDaily* (30 July 2007). 1 February 2008 http://www.sciencedaily.com /releases/2007/07/070726210931.htm.

[28] M. Stordeur, I. Stark, "Low Power Thermoelectric Generator - self sufficient energy supply for micro systems," *16th International Conference on Thermoelectrics*, pp. 575-577, Dec. 1997.

[29] R. Venkatasubramanian, C. Watkins, D. Stokes, J. Posthill, C. Caylor, "Energy Harvesting for Electronics with Thermoelectric Devices using Nanoscale Materials," *IEEE International Electron Devices Meeting*, pp. 367-370, Dec. 2007.

[30] R. Amirtharajah, and A. Chandrakasan "Self-Powered Signal Processing Using Vibration Based Power Generation," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 687-695, May 1998.

[31] C. D. Richard, D. F. Bahr, C-G Xu, R. F. Richards, "MEMS power: The P^3 system," presented at the 36th Intersociety Energy Conversion Engineering Conf. (IECE2001) Savannah, GA, 2001.

[32] K. Bruce, Fabrication and characterization of a piezoelectric membrane generator," M.S. Thesis, Washington State Univ., Pullman, WA, 2001.

[33] F. Lu, H. P. Lee, and S. P. Linn, "Modeling and analysis of micro piezoelectric power generators for micro-electromechanical systems," *Electronic Journals, Smart Materials and Structures*, vol. 13, pp. 57-63, February 2004.

[34] D. Johns and K. Martin, Analog Integrated Circuit Design, New York: Wiley, 1997.

[35] E. A. Vittoz, "Micropower Techniques," in Design of VLSI Circuits for Telecommunication and Signal Processing, J. E. Franka and Y. P. Tsividis, Eds. Englewood Cliffs, NJ: Prentice Hall, 1994.

[36] E. A. Vittoz, "Dynamic Analog Techniques" in Design of VLSI Circuits for Telecommunication and Signal Processing, J. E. Franka and Y. P. Tsividis, Eds. Englewood Cliffs, NJ: Prentice Hall, 1994.

[37] EKV model [Online]. Available: http://legwww.epfl.ch/EKV/

[38] A. S. Sedra, K. C. Smith, Microelectronic Circuits, 4th ed. Oxford Univ. Press, 1998.

[39] E. A. Vittoz, "Low-power design: ways to approach the limits," in *Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers,* Feb. 1994, pp. 14-18.

[40] E. A. Vittoz, "Low-power low-voltage limitations and prospects in analog design," in Analog Circuit Design, R.S. van de Plaasche, W.M.C. Sansen, and J.H. Huijsing, Eds. Boston, MA: Kluwer Academic, 1994.

[41] S. Meninger. A low power controller for a MEMS based energy converter, Masters Thesis, Massachusetts Institute of Technology, Department of Electrical Engineering and Computer Science, June 1999.

[42] S. Chatzandroulis, D. Tsoukalas, P.A. Neukomm, "A miniature pressure system with a capacitive sensor and a passive telemetry link for use in implantable applications," *IEEE Journal of Microelectromechanical Systems*, vol. 9, pp. 18-23, March 2000.

[43] D. Dudenbostel, K.L. Krieger, C. Candler, R. Laur, "A new passive CMOS telemetry chip to receive power and transmit data for a wide range of sensor applications," *International Conference on Solid State Sensors and Actuators*, vol. 2, June 1997, pp. 16-19.

[44] K. J. Cho, H. H. Asada, "A recursive frequency tracking method for passive telemetry sensors," *Proceedings of the 2003 American Control Conference*, vol. 6, June 2003, pp. 4943-4948.

[45] F. Kocer, P. Walsh, and M. Flynn, "Wireless power telemetry in 0.25μm CMOS." *IEEE Radio Frequency Integrated Circuits Conference* (RFIC 2004), June 2004, pp. 339-342.

[46] Q. Huang, and M. Oberle, "A 0.5mW passive telemetry IC for biomedical applications," *IEEE Journal of Solid State Circuits*, vol. 33, issue 7, pp. 937-946, July 1998.

[47] T. Lehmann, Y. Moghe, "On-chip active power rectifiers for biomedical applications," *IEEE International Symposium on Circuits and Systems*, vol. 1, May 2005, pp. 732-735.

[48] S. Mandal, Far field RF power extraction circuits and systems, Masters Thesis, Massachusetts Institute of Technology, Department of Electrical Engineering and Computer Science, June 2004.

[49] S. Mandal and R. Sarpeshkar, "Low-Power CMOS rectifier design for RFID applications," *IEEE Transactions on Circuit and Systems I* (TCAS-I), vol. 54, pp. 1177-1188, June 2007.

[50] M. Hata, "Empirical formula for propagation loss in land mobile radio services," *IEEE Transaction on Vehicular Technology*, vol. VT-29, no. 3, pp. 317-325, Aug. 1980.

[51] U. Karthaus, and M. Fischer, "Fully integrated passive UHF RFID transponder IC with 16.7W minimum RF input power," *IEEE Journal of Solid State Circuits*, vol. 38, pp. 1602-1608, October 2003.

[52] J. F. Dickson, "On-chip high-voltage generation in NMOS integrated circuits using an improved voltage multiplier technique," *IEEE Journal of Solid State Circuits*, vol. 11, pp. 374-378, June 1976.

[53] J.-T. Wu, and K.-L. Chang, "MOS charge pumps for low-voltage operation," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 592-597, April 1998.

[54] T. H. Lee, The Design of CMOS Radio Frequency Integrated Circuits. Cambridge University Press, Cambridge, UK, 2nd Edition, 2004.

[55] I. J. Bahl, "High-Q and low-loss matching network elements for RF and microwave circuits," *IEEE Microwave Magazine*, vol. 1, pp. 64-73, Sept. 2000.

[56] P. Cole, M. L. Ng, K. S. Leong, "Some notes on antenna matching and measurement for small RFID tags," http://autoidlab.adelaide.edu.au.

[57] B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, 2001.

[58] T. Le, J. Han, A. Von Jouanne, K. Mayaram, and T.S. Fiez, "Piezoelectric power generation interface circuits," *IEEE Custom Integrated Circuits Conference (CICC)*, Sept. 2003, pp. 489-492.

[59] J. Killen, Utilizing standard CMOS process floating gate devices for analog design, Masters Thesis, Mississippi State University, Department of Electrical and Computer Engineering, August 2001.

[60] F. Kocer, P. Walsh, and M. Flynn, "An RF powered, wireless temperature sensor in quarter micron CMOS," *IEEE International Symposium on Circuits and Systems (ISCAS)*. Volume: 4, May 2004, pp. 23-26.

[61] H. Nakamoto et al. "A passive UHF RFID tag LSI with 36.6% efficiency CMOS-only rectifier and current-mode demodulator in 0.35m FeRAM technology," *International Solid State Circuits Conference*, February 2006, pp. 310-311.

[62] T. Umeda, et al. "A 950MHz rectifier circuit for sensor networks with 10m-distance," *IEEE International Solid State Circuits Conference (ISSCC)*, February 2005, pp. 256-257.

[63] T. Umeda, H. Yoshida, S. Sekine, Y. Fujita, T. Suzuki, S. Otaka, "A 950MHz rectifier circuit for sensor networks with 10m-distance," *Journal of Solid State Circuits*, vol. 41, pp. 35-41, Jan. 2006.

[64] B. Wang; C-H Wang; Y. Ma, C. Diorio, T. Humes, "Study of stress-induced leakage current and charge loss of nonvolatile memory cell with 70Angstrom tunnel oxide using floating-gate integrator technique," *IEEE International Integrated Reliability Workshop 2004*, pp. 28-31, Oct. 2004.

[65] J. Yi, W.-H. Ki,, C.-Y. Tsui,"Analysis and design strategy of UHF micropower CMOS rectifiers for microsensor and RFID applications," *IEEE Transactions on Circuits and Systems-I*, vol. 54, pp. 153-166, Jan. 2007.

[66] G. De Vita and G. Iannaccone, "Design Criteria for the RF Section of UHF and Microwave Passive RFID Transponders," *IEEE Transactions on Microw. Theory Tech.*, vol. 53, no. 9, pp. 2978-2990, Sept. 2005.

[67] J-P Curty, N. Joehl, C. Dehollain, and M. Declercq, "Remotely Powered Addressable UHF RFID Integrated System," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 1602-1608, Nov. 2005.

[68] R. Barnett, S. Lazar and J. Liu, "Design of Multistage Rectifiers with Low-Cost Impedance Matching for Passive RFID Tags," in *IEEE RFIC Symp. Dig.*, Jun. 2006, pp. 291-294.

[69] T. Le, K. Mayaram, and T. S. Fiez,"Efficient far-field radio frequency power conversion system for passively powered sensor networks." *in Proceedings of the IEEE 2006 Custom Integrated Circuits Conference*, Sept. 2006, pp. 293-296.

[70] National Semiconductor, "Linear and switching voltage regulator fundamentals," http://www.national.com/appinfo/power/files/f4.pdf

[71] E. Vittoz, J. Fellrath, "CMOS analog integrated circuits based on weak inversion operations," *IEEE Journal of Solid-State Circuits*, Vol. 12, Issue 3, June 1977.

APPENDICES

APPENDIX A. Voltage Regulator Simulation Results

A.1. Adaptive Bungee Bias

Figure A-1 shows the simulation results of current through the bungee bias circuit at various supply voltages in the -20°C to 60°C temperature range. The bungee bias circuit dissipates less than 1 nA of current at 27°C with a 2.0 V supply voltage as it operates from leakage mode devices. This current increases to as much as 10 nA as the supply voltage is increased to 10 V and temperature is increased to 60°C.

The challenge in designing the adaptive bungee bias circuit is to keep threshold (V_{TH}) mismatch in the cutoff mode transistors to a minimum. Figures A-2 and A-3 shows the bias voltages on the bungee bias circuit without mismatch and with 10mV mismatch, respectively. With no V_{TH} mismatch, the bias voltages stay fairly constant over the whole operating temperature range. In cutoff mode, a V_{TH} mismatch greater than 10 mV can drastically change the channel resistance and thus changes the biasing points of all circuit blocks. The worst case scenario is plotted in Figure A-3 to show the mismatch dependence of the bungee bias circuit. When there is a large V_{TH} mismatch in one of the devices in the cutoff mode, the current through the bungee bias circuit decreases causing an imbalance in the resistive divider. The majority of the voltage drop will be across the top and bottom cutoff mode transistors causing node Bias 4 and Bias 1 to vary widely with temperature. Since these Bias nodes control the bias current in the voltage regulator, a large mismatch in threshold voltage can lead to large variations in the reference current and reference voltage as the temperature changes. The leakage mode devices must be designed to be very large (i.e., 250 μm/0.18 μm) with common centroid layout techniques to reduce V_{TH} mismatch.
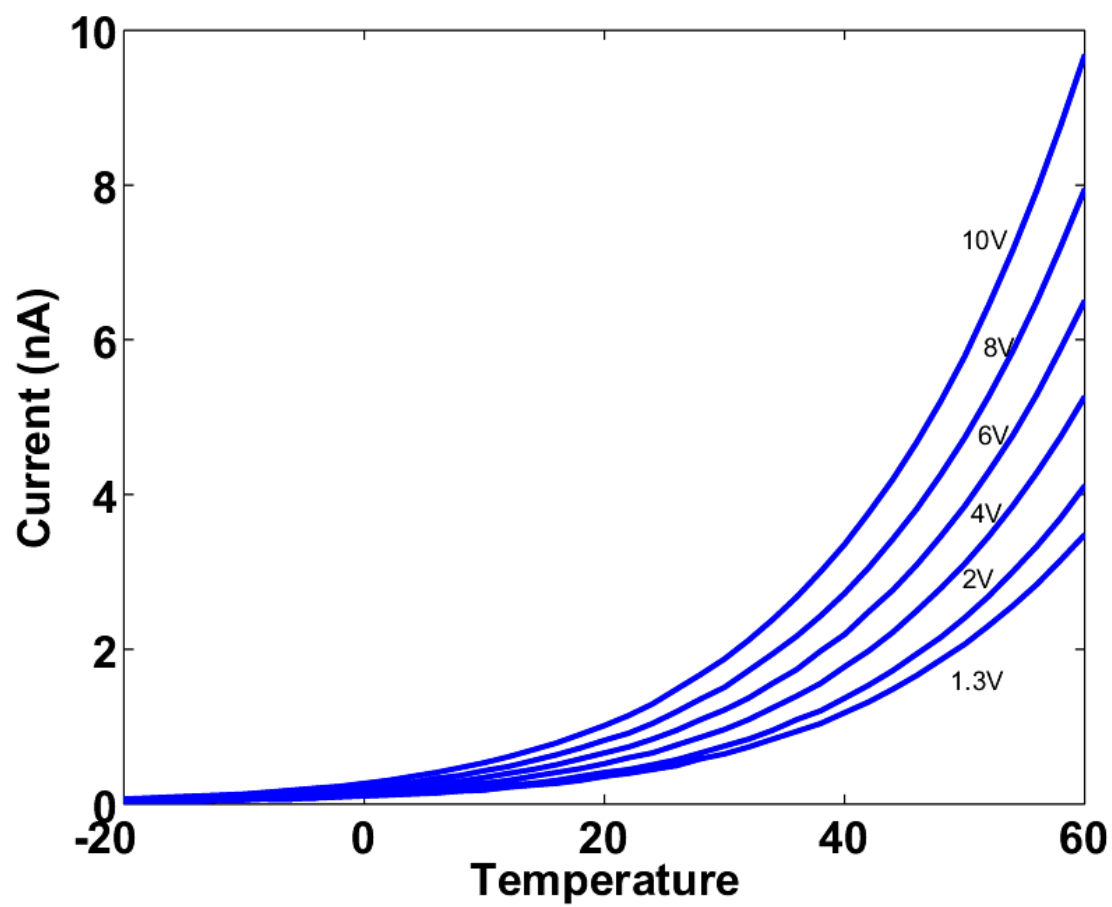
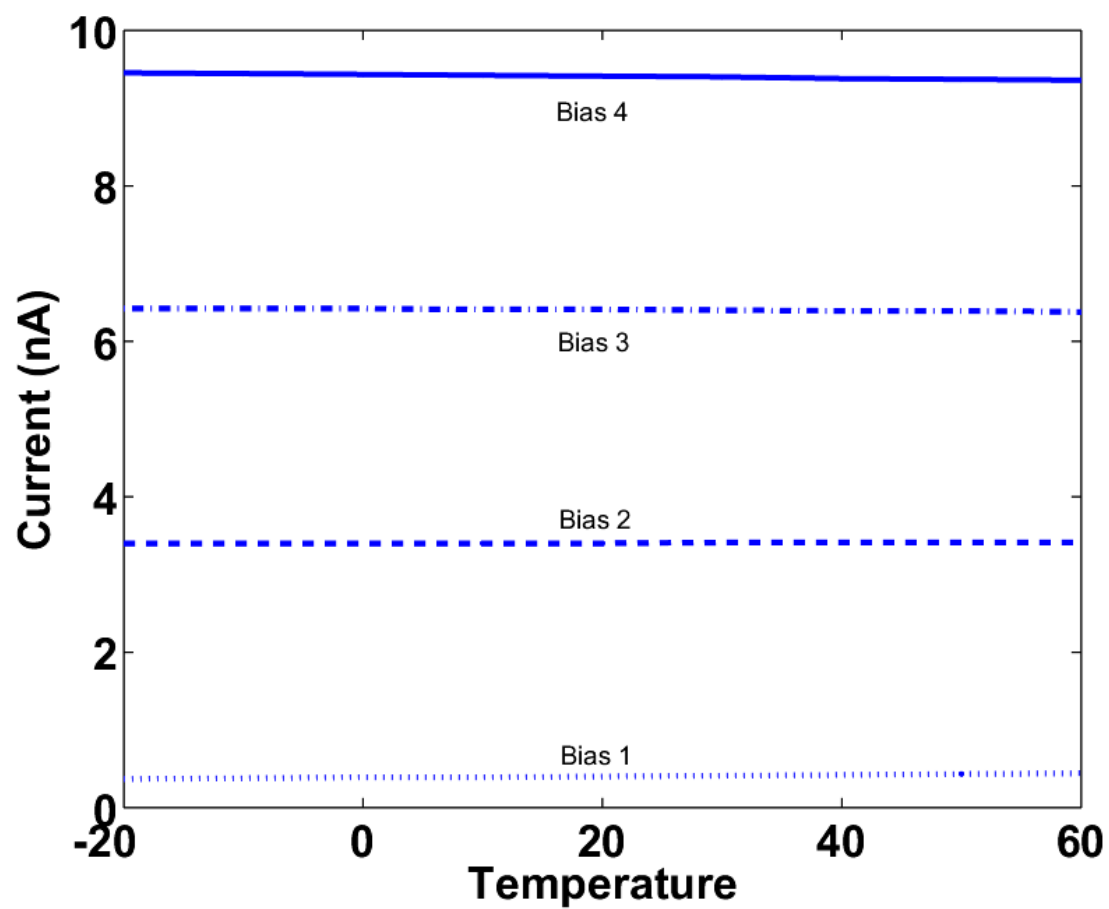FIGURE A-1. Current through adaptive bungee biasing circuit at various supply voltages and temperature.

FIGURE A-2. Bungee bias voltages without V_{TH} mismatch effect.
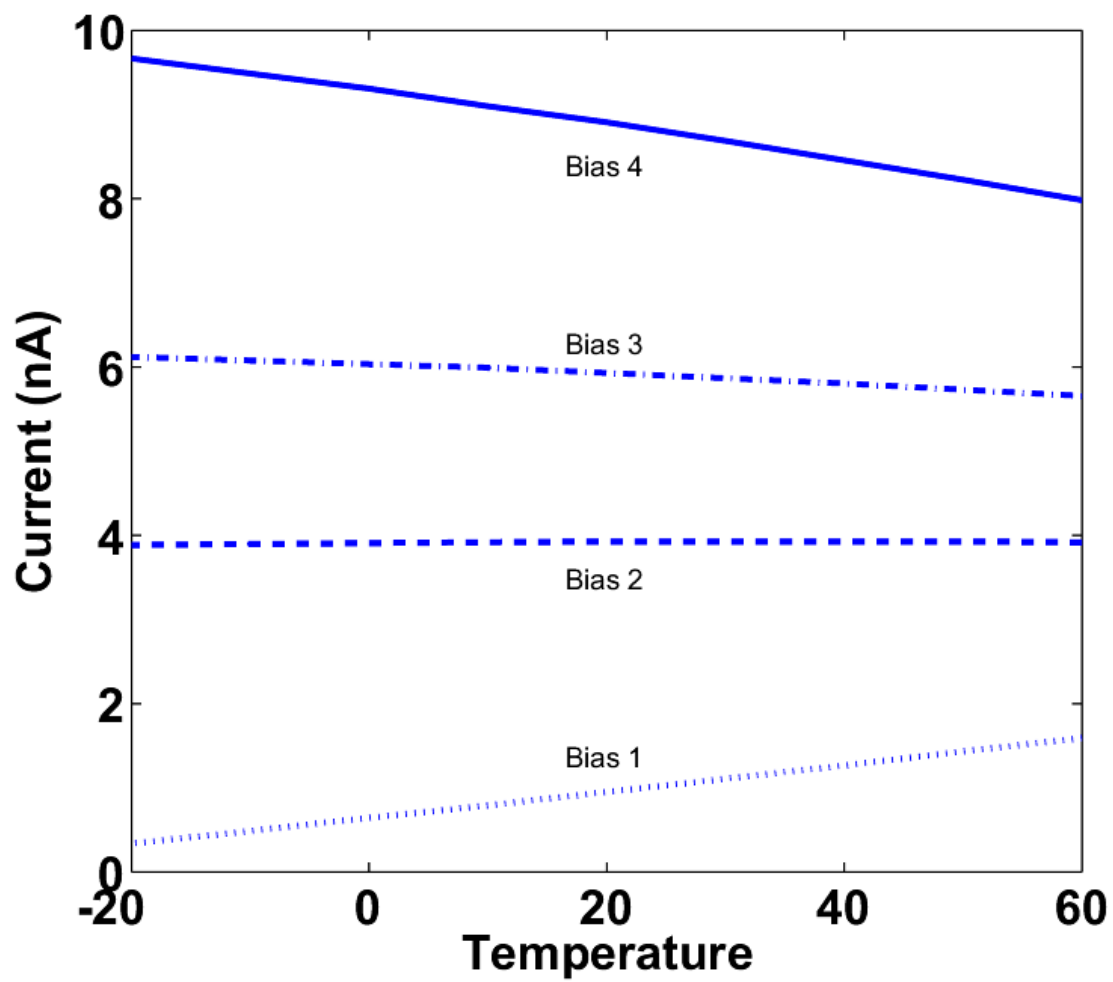
FIGURE A-3. Bungee bias voltages with V_{TH} mismatch of 10mV.

A.2. Current Reference

Figure A-4 shows the linearity of the PTAT reference current through the resistor in the current reference circuit. The plot shows good linearity with the bungee bias circuit throughout the desired temperature range from -20°C to 60°C. The PTAT current becomes less linear at input voltages of 1.2 V with temperatures less than 0°C. At voltages lower than 1.2 V, the majority of the voltage drop is in the drain-source junction of the cascoded device, effectively causing the current in the current mirror to slightly decrease. At lower temperatures, the threshold voltage of all the transistors increases, causing the reference current to decrease.

Figure A-5 shows the current ratio of the supply independent current source throughout the temperature range of -20°C to 60°C with the bungee bias. The cascoded configuration of the bungee bias circuit aids in reducing the current mismatch in all the current mirrors since the drain-source voltage is kept to similar voltages by stacking transistors. For supply voltages of 8 V or below, the result shows less than 1% mismatch in current. As the supply voltage of the PTAT current reference is increased, the drain-source voltage of the current mirror is increased and hence increases the current mismatch. It is critical to keep the current ratio as close as possible to unity to reduce current mismatch in the current mirror since a mismatch in the reference current can cause the temperature coefficients in the voltage regulator to change drastically. This in turn causes a gain error in the voltage reference as a function of temperature and increases the variation in the regulated output voltage.
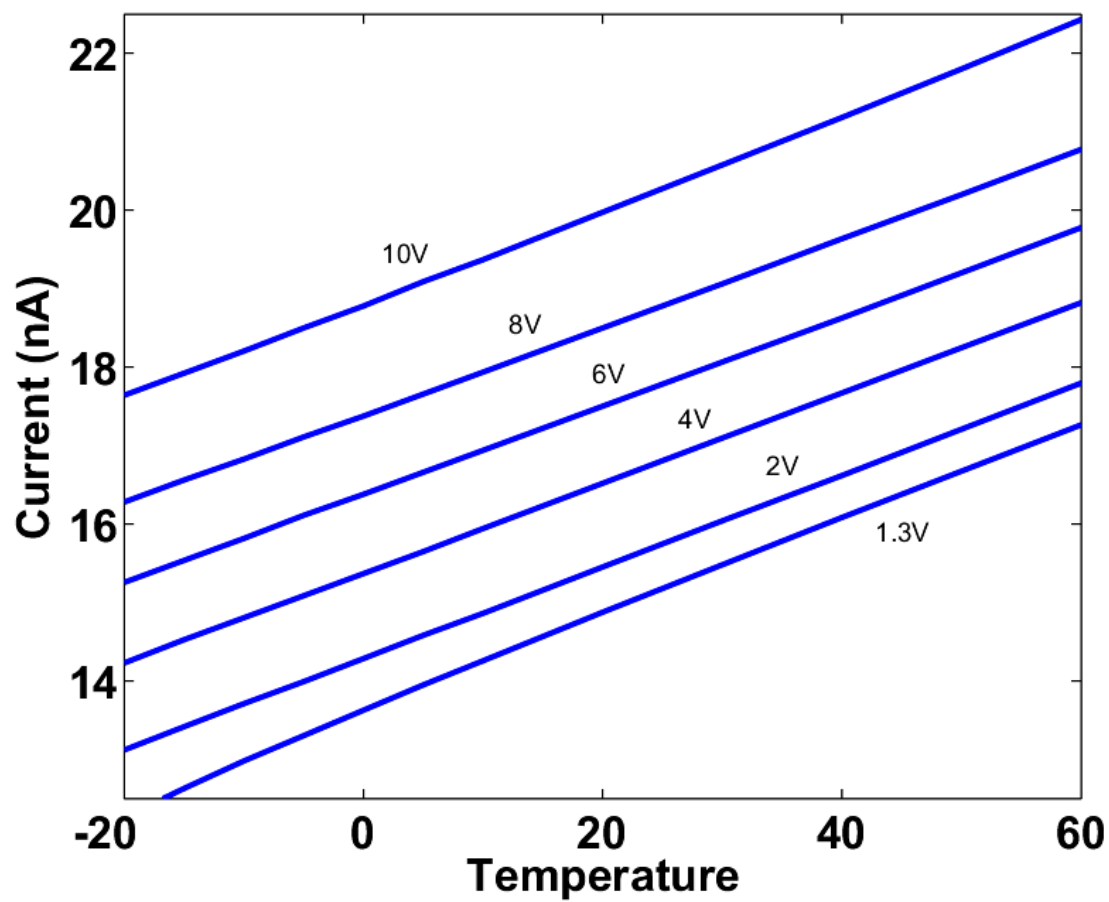
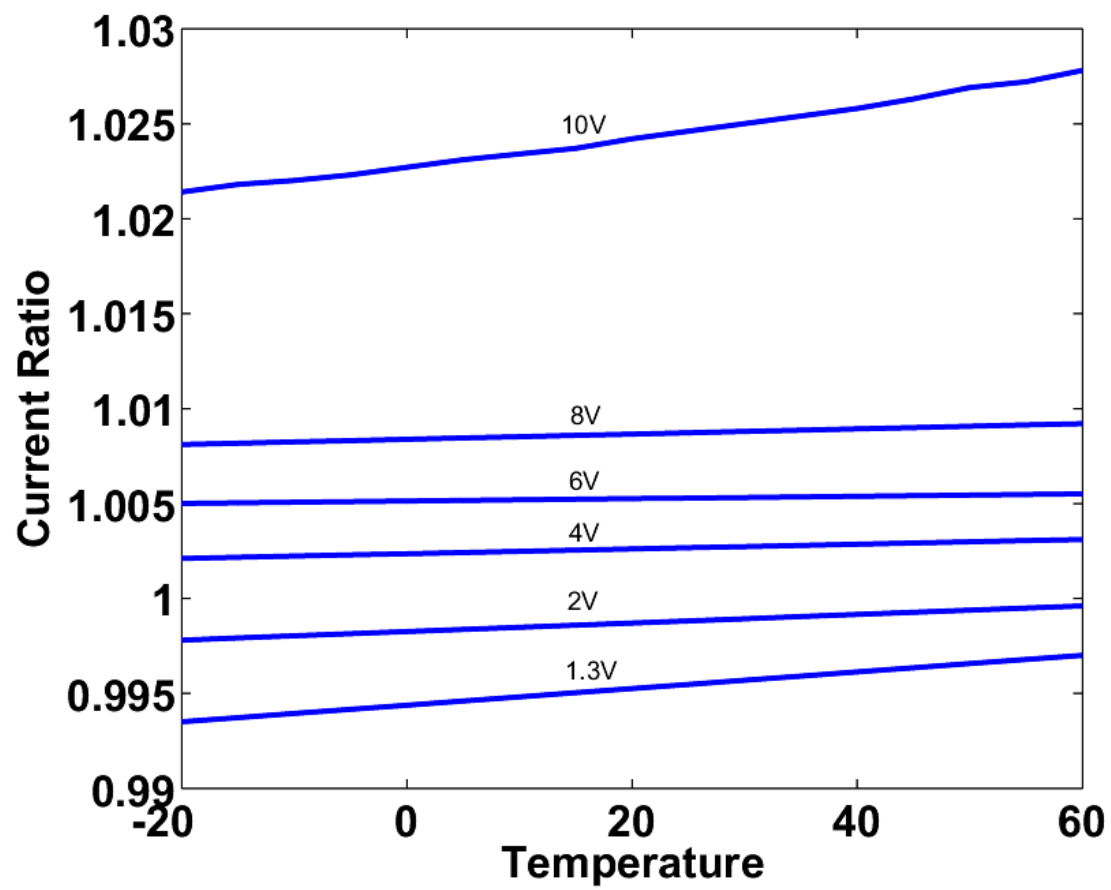FIGURE A-4. Linearity of PTAT current reference with bungee bias.

FIGURE A-5. Current ratio of the current mirror.

A.3. Voltage Reference

Figure A-6 shows the dependence of the reference voltage on temperature under various supply voltages. From simulation results, the reference voltage could vary from 1.206 V to 1.29 V depending on the supply voltage and temperature of the voltage regulator. For an input voltage of 1.3 V, the reference voltage is approximately 1.212 V while the variation throughout the -20°C to 60°C temperature range is only about 10 mV. At an input voltage of 10 V, the reference voltage also varies by about 10 mV from 1.277 to 1.289 V. From Figure A-6, it can be observed that the reference voltage is more strongly dependent on the input supply voltage than the temperature.

Figure A-7 shows the reference voltage curve as a function of supply voltage for the two voltage regulators at -20°C, 27°C, and 60°C. The reference voltages stay fairly flat for supply voltages between 1.25 V and 10 V for both regulators. The increase in the reference voltage becomes non-linear for supply voltages above 8 V as the drain-source voltage of some transistors in the bungee bias circuit becomes high enough to induce current mismatch in the current reference circuit. The nominal regulated voltage for the 1.25 V regulator at 27°C and 2 V input is 1.22 V and 0.61 V for the 0.625 V regulator for the same conditions.

The power supply rejection ratio (PSRR) of the reference voltage is shown in Figure A-9 as a function of frequency with a 2V input. The PSRR is greater than 40 dB for frequencies below 10 kHZ. Figure A-9 show the PSRR at DC for various input voltages. The PSRR is highest in the middle range of voltage where it is greater than 40 dB for voltage from 1.4 to 10.8 V.
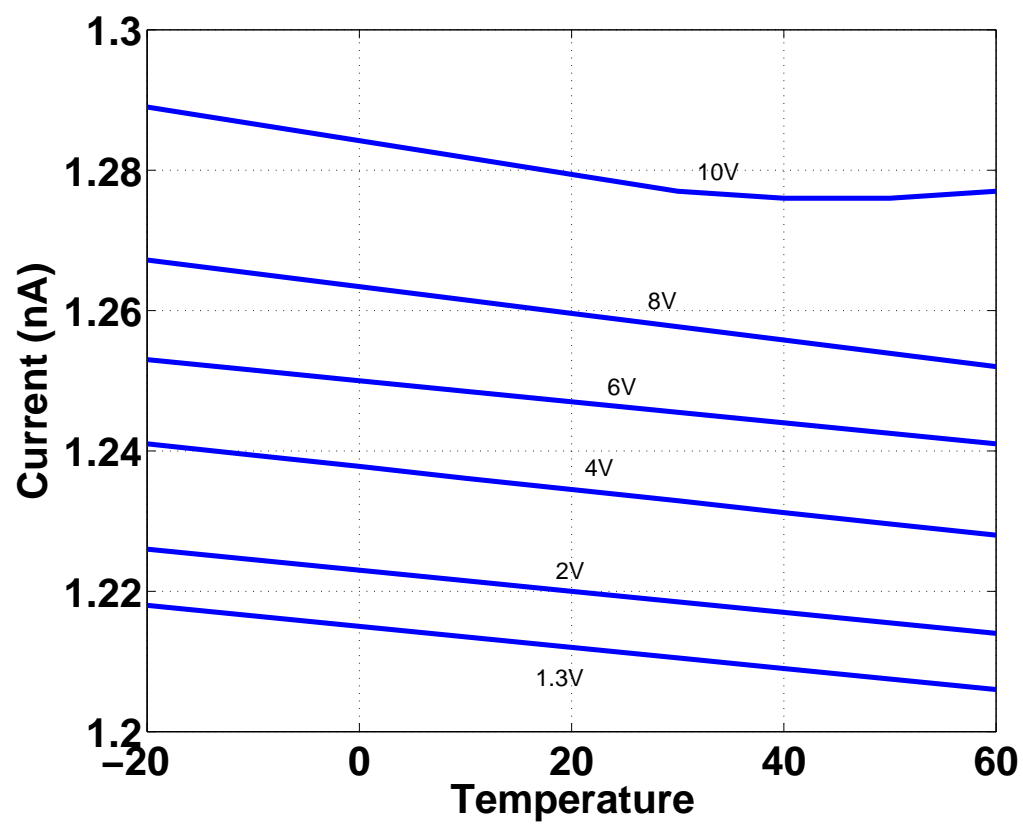
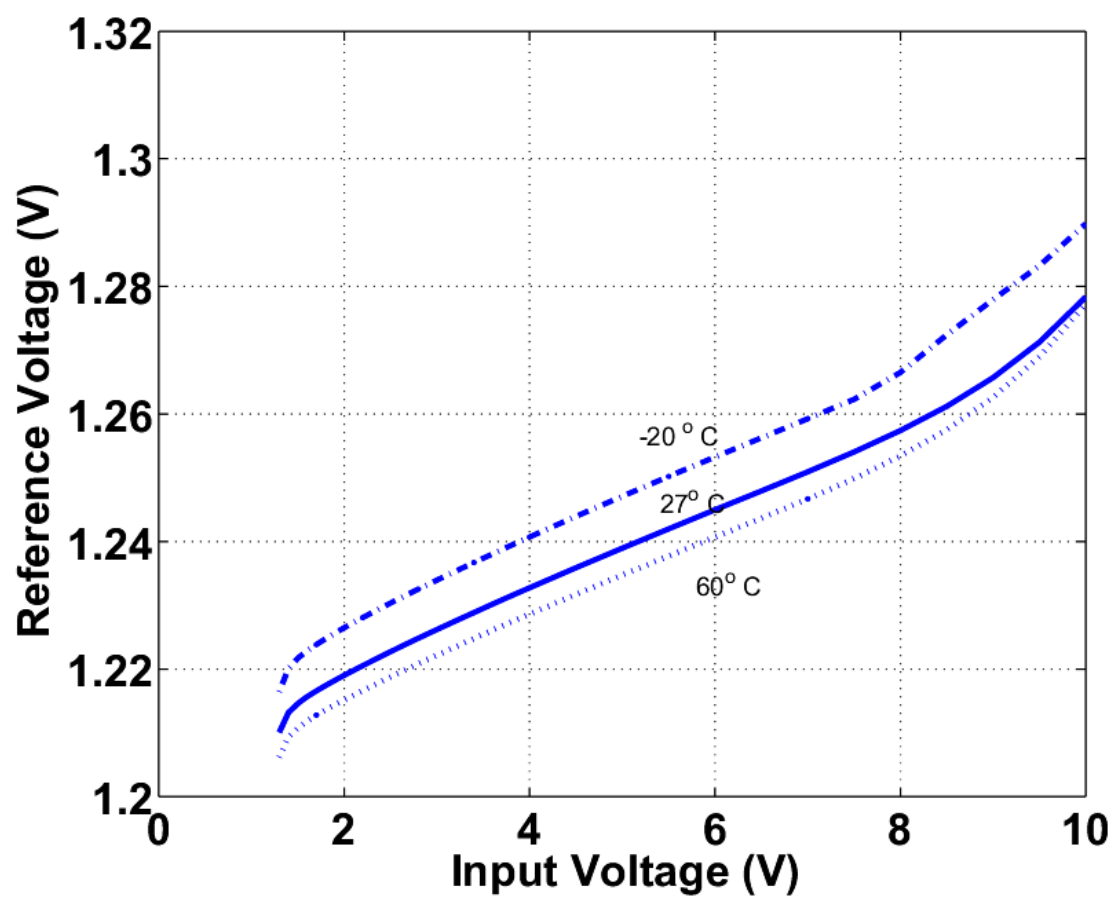FIGURE A-6. Reference voltage as function of temperature.

FIGURE A-7. Reference voltage as a function of the power supply voltage.
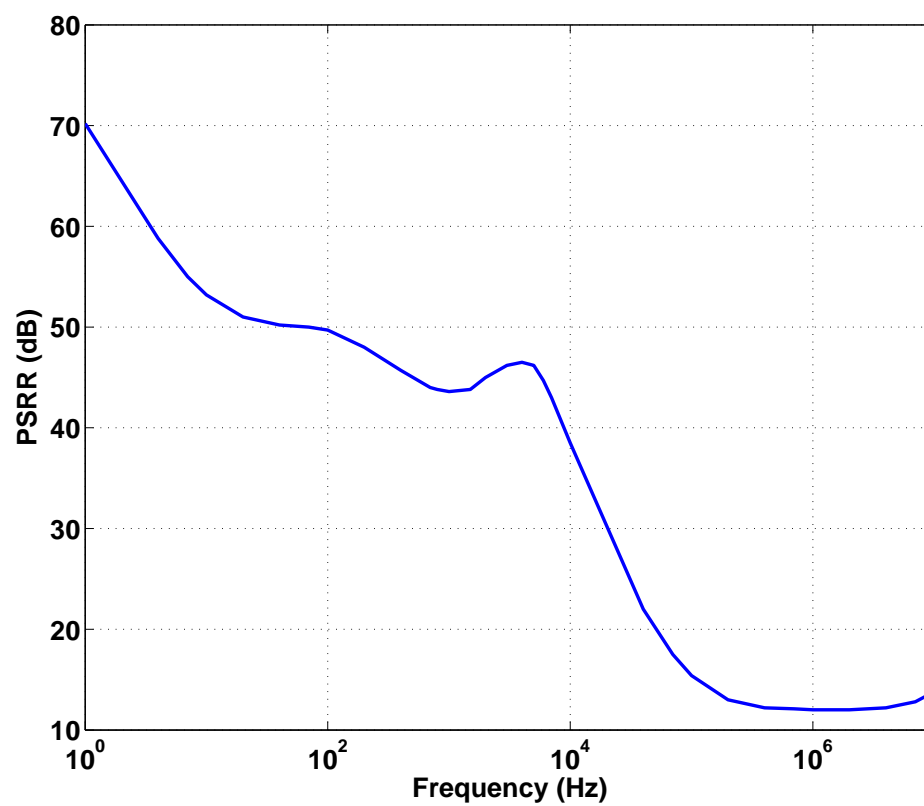
FIGURE A-8. Power supply rejection ratio (PSRR) of the voltage reference circuit as a function of frequency.
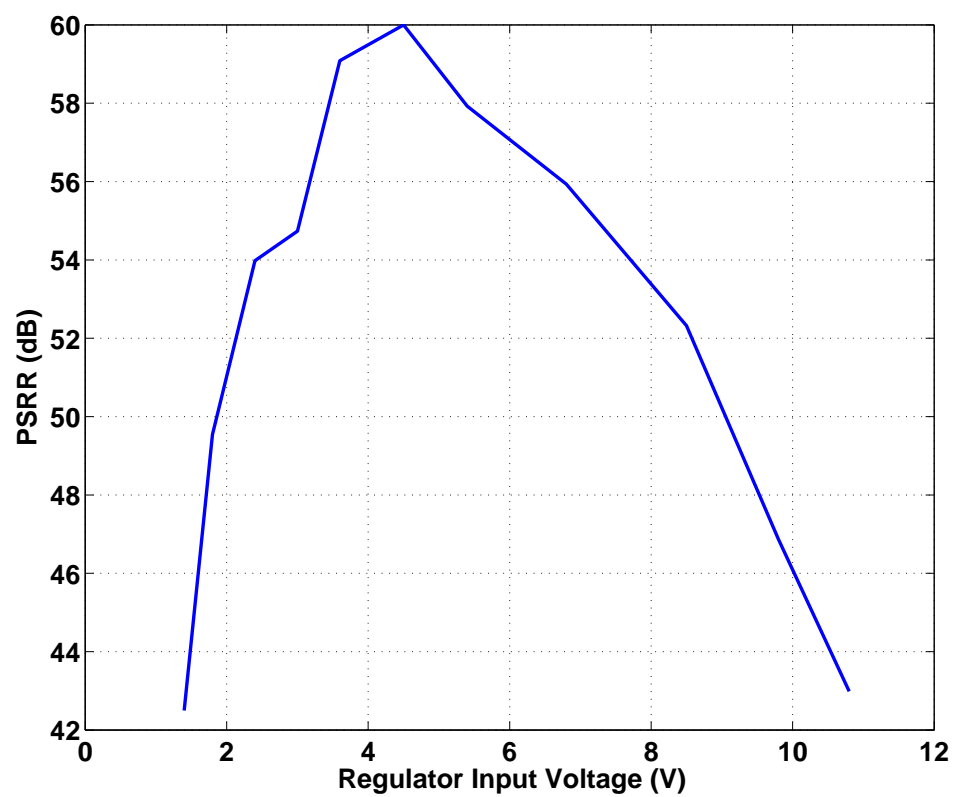
FIGURE A-9. Power supply rejection ratio (PSRR) of the voltage reference circuit as a function of input voltage.

A.4. Opamp Performance

The opamp is designed to operate in subthreshold current to reduce the quiescent power dissipation. The first stage and second stage are both biased with approximately 40 nA of current at 27°C. Simulation results of the opamp are shown in Figures A-10 to A-13 with supply voltages of 1.2 V and 10 V. With a 1.2 V supply, the opamp can obtain a DC gain of 58 dB, unity gain bandwidth (UGBW) of 275 kHz and 48° phase margin when it is not loaded. The bandwidth is set by the Miller compensation capacitor C_1 as the capacitive load due to the pass transistor is much smaller compared to the compensation capacitor. The bandwidth compensation is done to keep the opamp stable at all frequencies below the unity gain bandwidth. The opamp draws a total current of 75 nA at 1.2 V, which is equivalent to 90 nW of dissipated power. With a 10 V supply, the opamp has a DC gain of 98 dB which is 40 dB higher than at 1.2 V supply. This is due to the higher g_m that the input transistors attain with a much higher V_{DS} when biased in subthreshold. The unity gain bandwidth at 10 V supply is 535 kHz and phase margin is 60° when it is not loaded. With a 10 V supply, the opamp draws a current of 140 nA, which is equivalent to 1.4 μW of dissipated power.

A.5. Regulator Performance

The simulated transient response of both voltage regulators under different supply voltages is shown in Figure A-14 and A-15. A small output capacitance of 10 μF is used to speed up the simulation time. The tradeoff with a lower loading capacitance is a small variation in the regulated output voltage to remain stable. At higher supply voltages of 6 V and 10 V, the sourcing capacitor charges very quickly as the pass transistors are driven more strongly with a higher overdrive
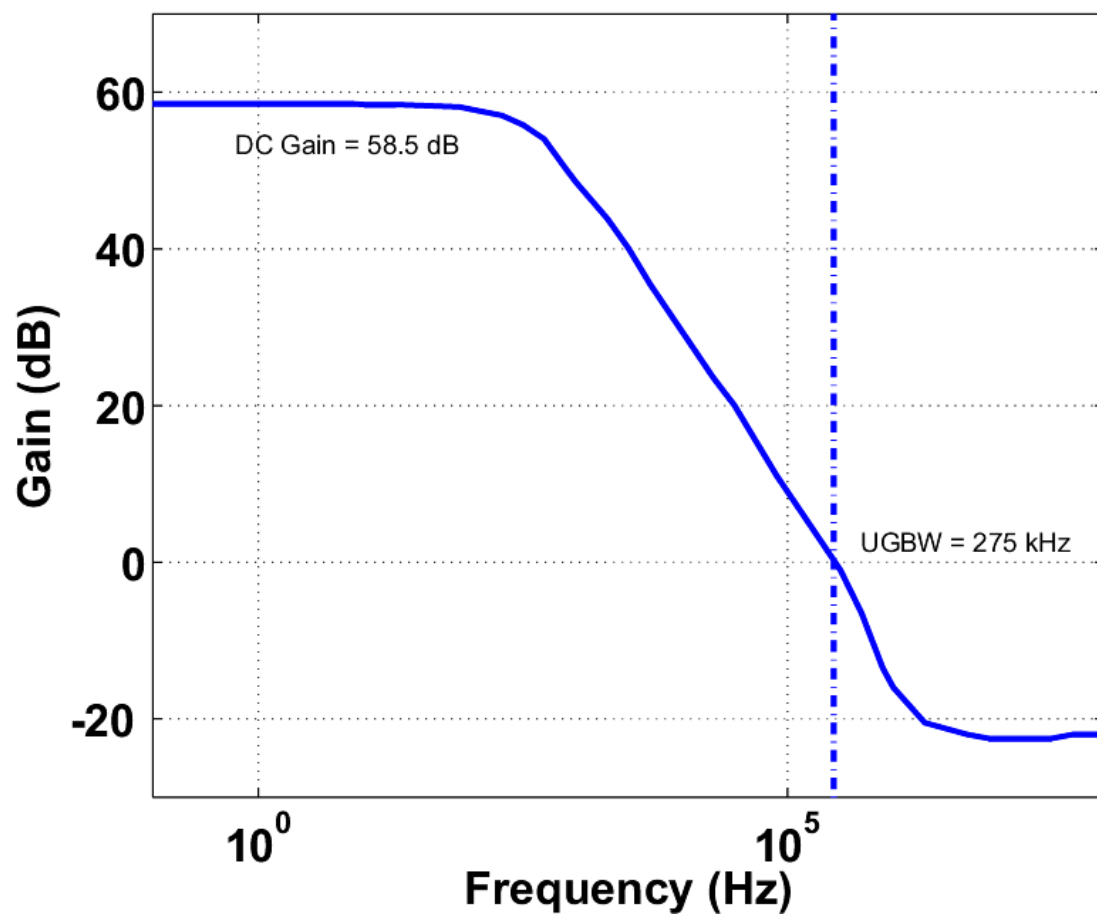
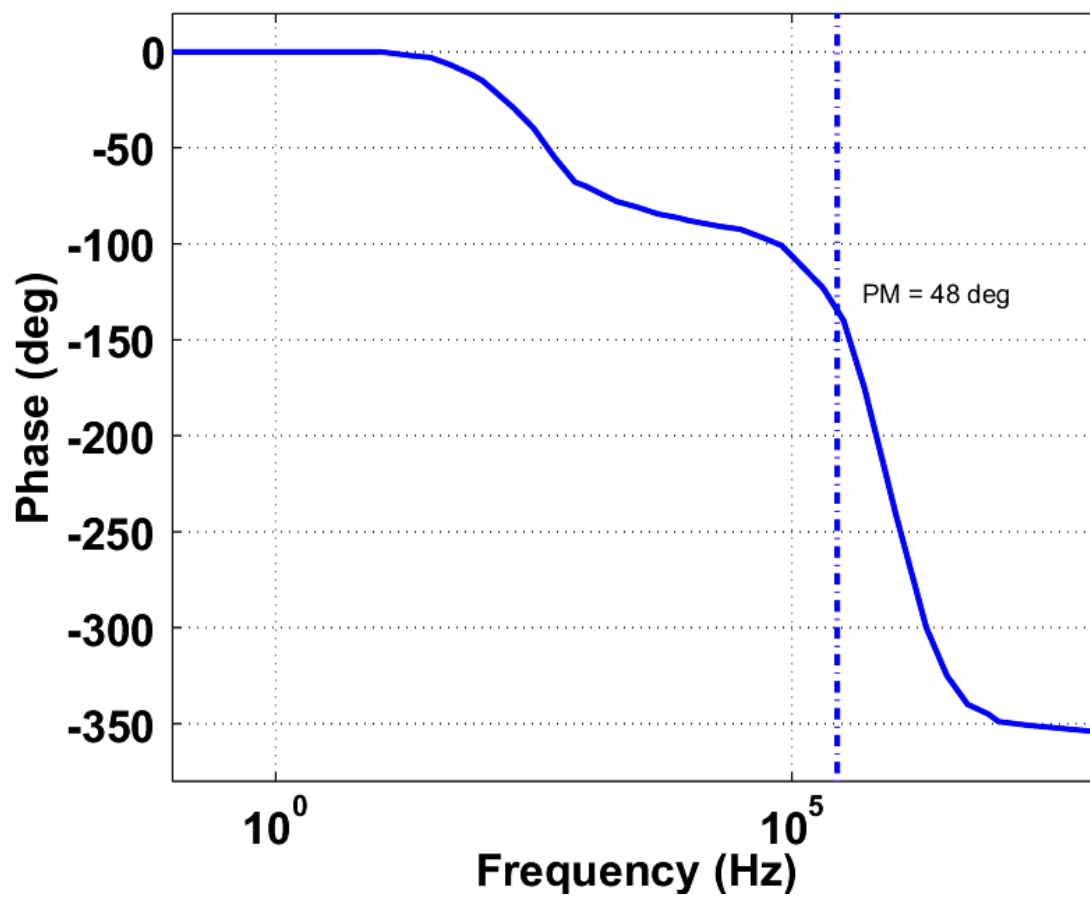FIGURE A-10. Plot of opamp gain operating at 1.2 V.
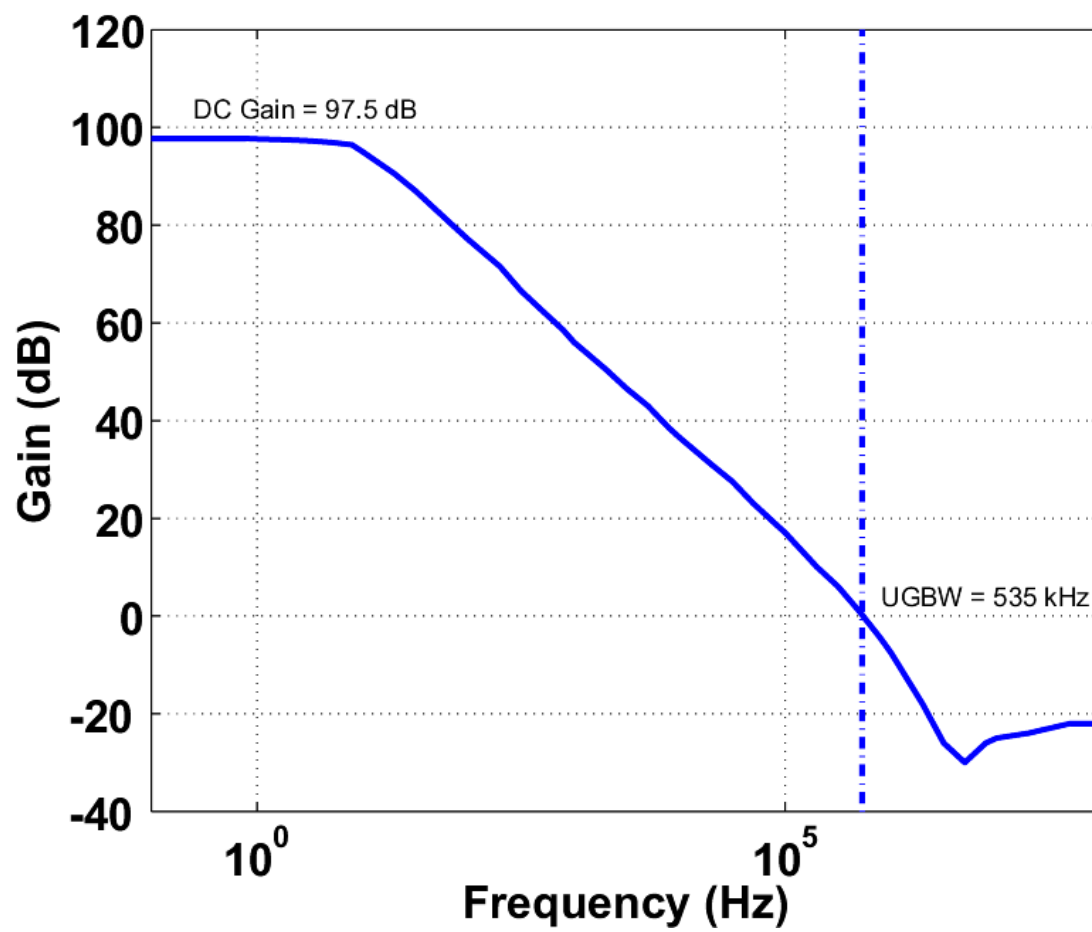
FIGURE A-11. Plot of opamp phase operating at 1.2 V.

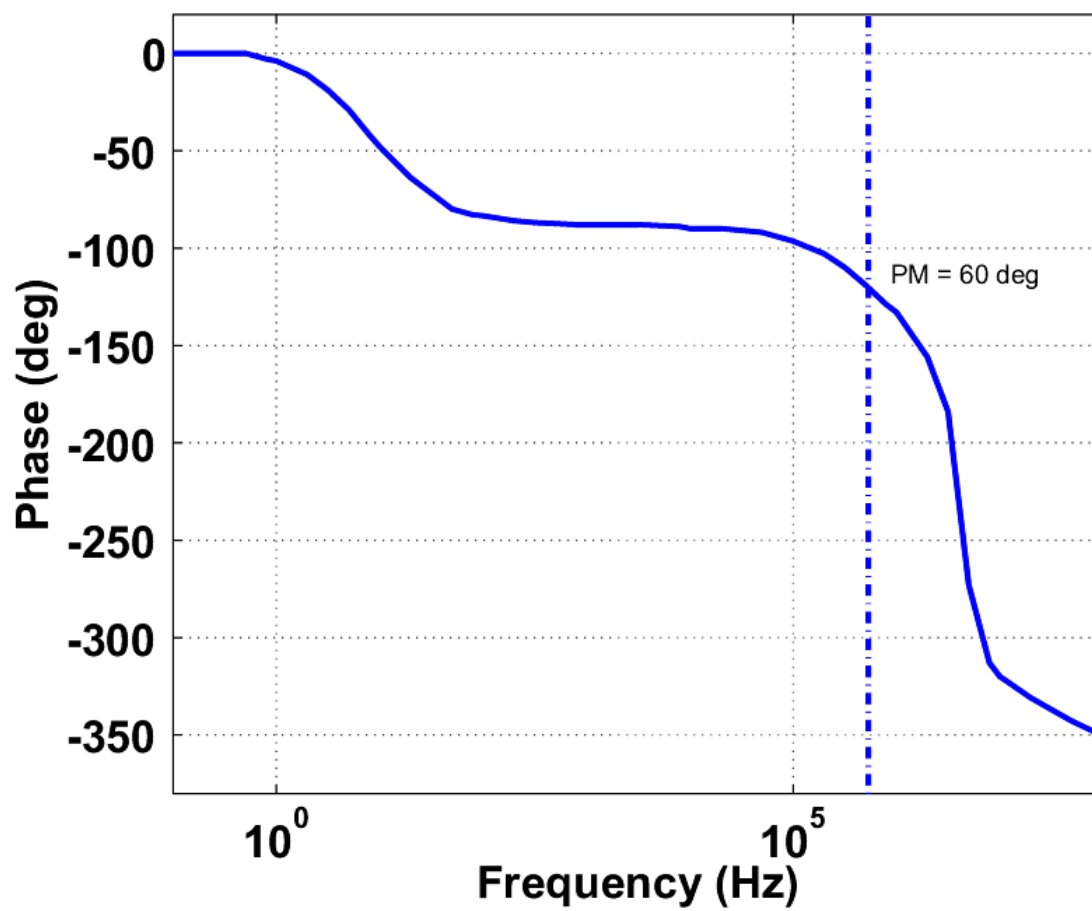FIGURE A-12. Plot of opamp gain operating at 10 V.

FIGURE A-13. Plot of opamp phase operating at 10 V.

voltage (V_{GS} - V_{TH}). Also, at higher voltages the current available to charge the capacitor is higher in a relative sense. At lower supply voltages, the sourcing capacitor charges more slowly because the pass transistor voltage overdrive is low so the pass transistor switches are driven very weakly, thus less current can be sourced to the sourcing capacitor. It takes up to 60 ms to fully charge the sourcing capacitor with a 1.3 V power supply and less than 1 ms with a 10 V supply.
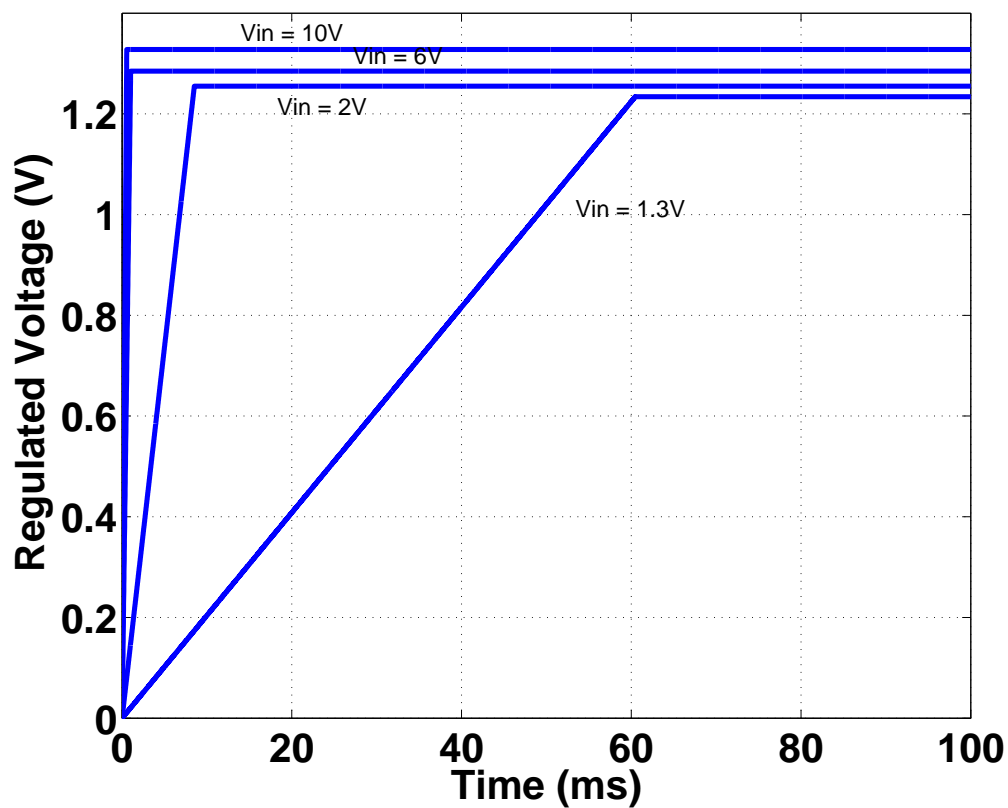

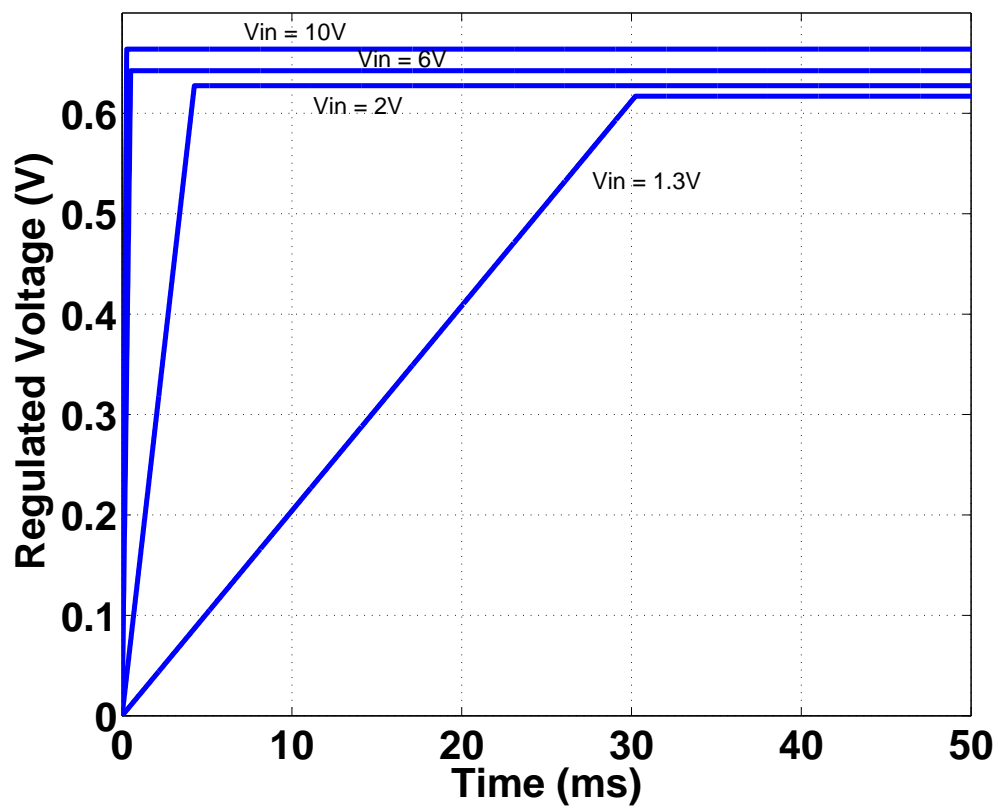FIGURE A-14. Transient response of voltage regulator.

FIGURE A-15. Transient response of the low voltage regulator.