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Min Gyu Kim for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on May 4, 2006.

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The demand for portable electronic systems and the continued down-scaling of device dimensions resulted in rapid improvement in the performance of integrated systems. Several low-voltage design techniques have been proposed to operate analog circuits with sub-1V supply. However, these techniques require higher power consumption to achieve large dynamic range while operating with low supply voltage. In this thesis, two low-power design techniques for low-voltage data converters are proposed. The first technique is low-voltage double-sampling method for delta-sigma analog-to-digital converters using a combination of switched-RC technique and floating switched-capacitor configuration. The second technique is an improved clocking scheme for algorithmic analog-to-digital converters with on-chip delay-locked-loop. A 0.9V 92dB delta-sigma audio ADC and a 10MS/s 11-b algorithmic ADC were implemented to demonstrate the proposed design techniques.

Low-Power Design Techniques for Low-Voltage Analog-to-Digital Converters

by

Min Gyu Kim

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APPROVED:

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Min Gyu Kim, Author

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*my parents-in-law MoonWoong Shin, TaeBok Park*

*my wife, SookHyun Shin*

*my daughter, JiYeon Kim and my son, Harrison Kim*

# LOW-POWER DESIGN TECHNIQUES FOR LOW-VOLTAGE ANALOG-TO-DIGITAL CONVERTERS

# CHAPTER 1. INTRODUCTION

## 1.1. Background

Analog-to-digital converters (ADCs) are indispensable blocks in applications where an interface between the analog real world and the digital modern signal processing block is necessary. They can be found in many electronic systems for multimedia, medical, communication, mobile, and portable applications. A number of architectures have been proposed to satisfy many specifications in various applications. All architectures have trade-offs between bit resolution, conversion speed, and complexity. Fig. 1.1 illustrates the ADC performance trade-off between bit-resolutions and conversion speeds. Delta-sigma ADCs generally achieve high resolution and low speed, algorithmic or successive-approximation-register ADCs achieve moderate resolution and moderate speed, and pipelined ADCs achieve moderate resolution and high speed.

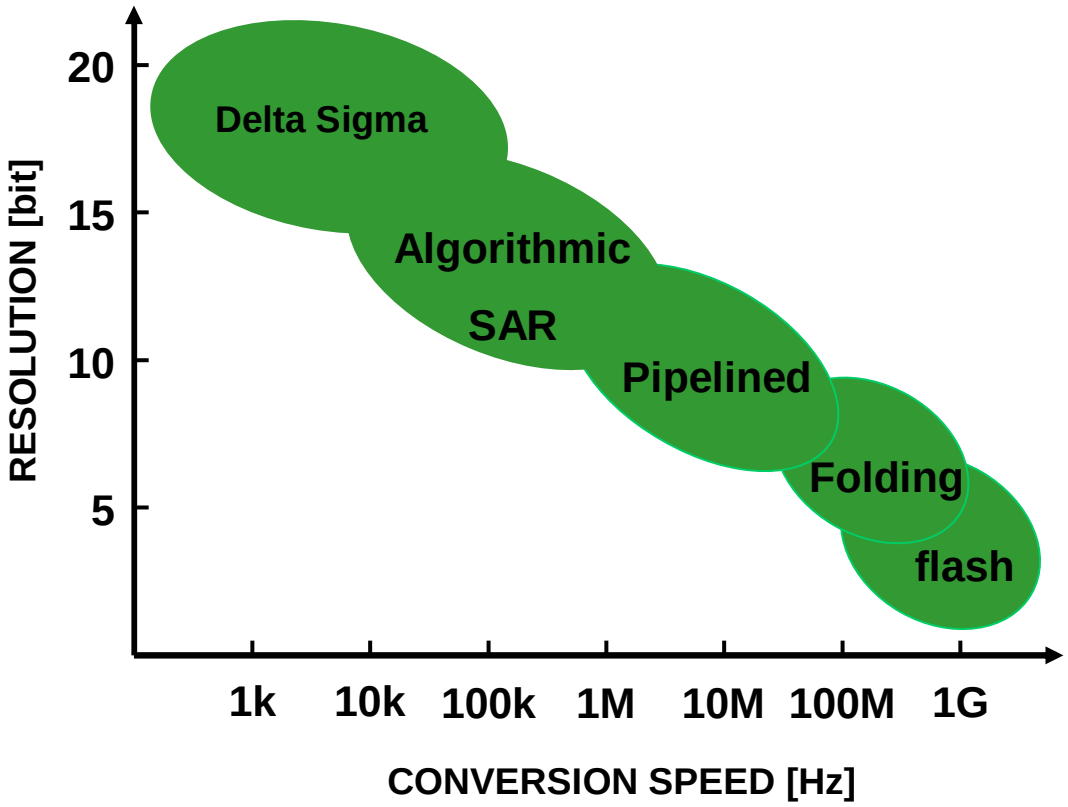



Figure 1.1: Conversion speeds and bit resolution plot for ADCs.

## 1.2. Motivation

The demand for portable multimedia electronic systems and the continued down-scaling of device dimensions resulted in rapid improvement in the performance of integrated systems. In order to reduce power consumption and the electric fields that accompany device scaling, it is necessary for circuits to operate from reduced supply voltages. Integrating both analog and digital circuits with same process and power supply voltage level provides important incentives such as low cost, high performance, reduced electromagnetic interference, and portability. However, reduced supply voltage severely limits the achievable dynamic range of

analog circuits. High dynamic range and low-power are increasingly demanded in multimedia and communication applications. Thus, the design of analog circuits naturally comes with the challenge to maintain the desired levels of performance as the supply voltage is lowered. A reduced supply voltage generally results in significant power savings in digital circuits. However, the power consumed in analog circuits is likely to increase because the reduced supply voltage limits the analog signal power thereby requiring lower noise. For this reason and the need for portability, high-performance ADCs should operate not only with a low voltage but also with low power consumption.

## 1.3. Proposed Approaches

Previously proposed techniques for low-voltage circuit design [1–7] enabled ADCs to operate with low-voltage power supplies. However, these techniques could not satisfy low power consumption which is required for portable applications and the reduced signal power caused by down scaling.

In this thesis, two novel low-power design techniques are proposed. The first is based on a double sampling technique using the switched-RC branches [7] to reduce power consumption and ensure sub-1V operation. The second is a low-power algorithmic ADC with an improved clocking scheme and an on-chip delay-locked-loop (DLL). Both techniques improve the conversion speed for a given power consumption.

## 1.4. Contributions

The contributions of this work are:

- A low-voltage double-sampling (DS) technique [8] for delta-sigma ADCs using a combination of a switched-RC technique [7] and a floating switched-capacitor DS configuration [9].
- An improved clocking scheme for algorithmic ADCs with an on-chip DLL [10, 11].
- A low-power simple dynamic-element-matching technique for 3-level quantizer delta-sigma ADCs [8].
- DC offset and memory effect suppression techniques for algorithmic ADCs [11].
- A low-voltage fully differential opamp and comparator [8].

## 1.5. Thesis Organization

This thesis is organized as follows. Chapter 2 describes the issues and existing solutions associated with low-voltage and low-power circuit design. Chapter 3 explains general functions of ADCs, delta-sigma ADC basics, and algorithmic ADC basics. Chapter 4 presents the proposed low-power design techniques for low-voltage ADCs.

Chapter 5 describes the two prototype IC designs. The first is a 0.9V 92dB DS switched-RC $\Delta\Sigma$ audio ADC and the second protoype is a 10MS/s 11-bit 0.19mm$^2$

algorithmic ADC. Experimental results for the two prototypes are included in this chapter. Finally, chapter 6 concludes this thesis and summarizes this work.

# CHAPTER 2. LOW-VOLTAGE AND LOW-POWER DESIGN TECHNIQUES

In this chapter, problems and solutions of low-voltage and low-power circuit design techniques are introduced to understand why new low-power design techniques for low-voltage analog circuits are needed. The switched-capacitor circuits are routinely used in analog building blocks for their inherent superior sample-and-hold function and good linearity. However, the switched capacitor circuits suffer from several problems as supply voltages are lowered. In following section, major issues in the design of low-voltage switched capacitor circuits are discussed.

## 2.1. Low-voltage Circuit Design Issues

### *2.1.1. Floating Switch Problem*

A generic switched-capacitor integrator (SCI) which is widely used for ADC design is chosen to explain low-voltage circuit design issues. An SCI is the main circuit block of signal processing systems such as filters, data converters, sensor interfaces. A basic SCI consists of switches, capacitors, and an opamp as shown in Fig. 2.1. During $\phi 1$ phase, capacitor C1 samples the input. During $\phi 2$ phase, the sampled charge in C1 is transferred to capacitor C2, thereby integrating the input signal.

The difference equation of an SCI is

$$C_2 V_{OUT}(n) = C_2 V_{OUT}(n-1) + C_1 V_{IN}(n-0.5)\,. \tag{2.1}$$

The z-transform of 2.1 is

$$H(z) = \frac{V_{OUT}(z)}{V_{IN}(z)} = \frac{C_1}{C_2}\frac{z^{-1/2}}{1-z^{-1}}. \tag{2.2}$$

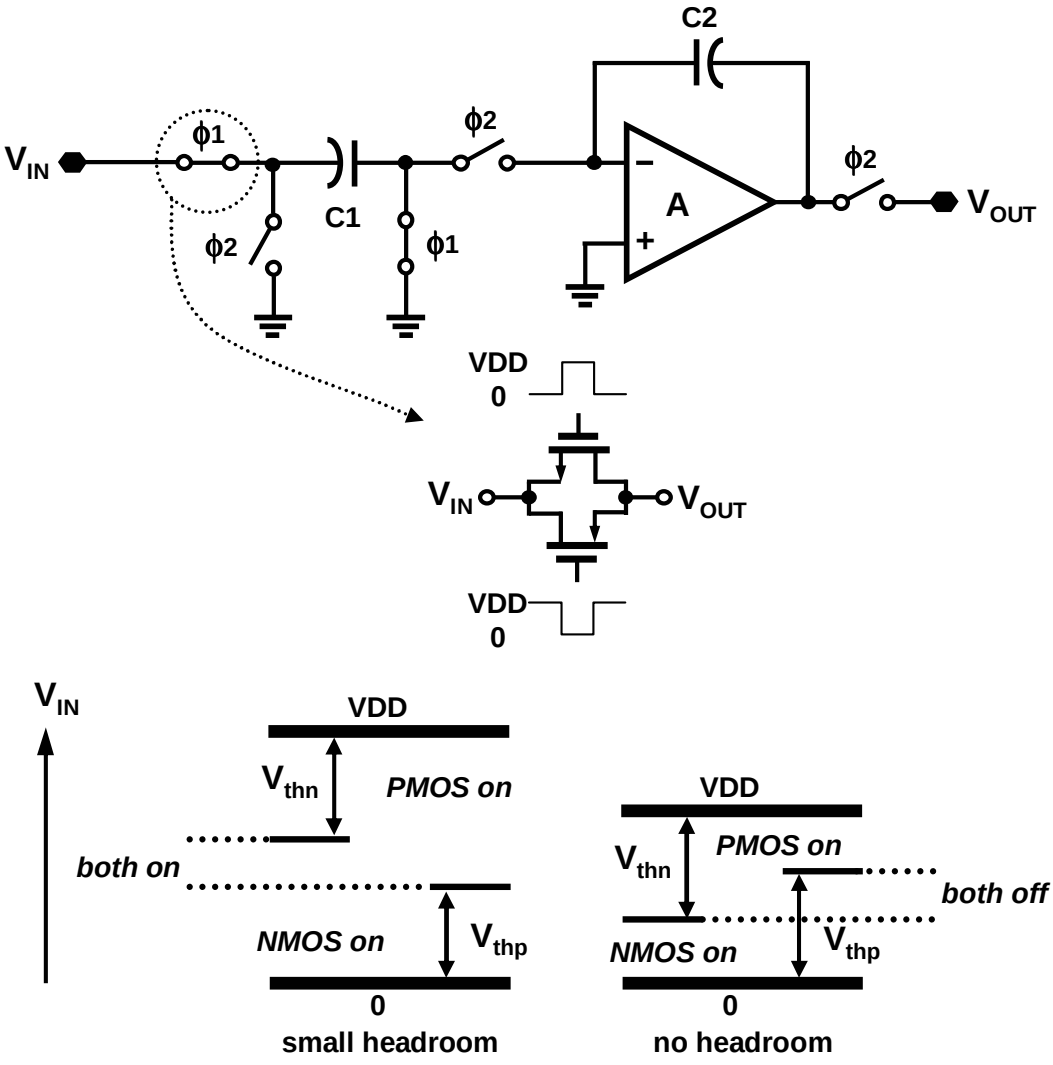



Figure 2.1: A conventional SCI and the floating switch problem.

The functionality of the capacitors in an SCI is not limited by a low supply voltage. On the other hand, switches are affected by low supply voltage. Fig. 2.1 shows the limitation on the operation of a floating switch in switched capacitor circuits. These limitations arise when the supply voltage is smaller than or equal to the sum of PMOS and NMOS threshold voltages ($V_{thn} + |V_{thp}|$). If the power supply voltage, VDD is smaller than ($V_{thn} + |V_{thp}|$), the switch will not be turned on even if the control signal voltage level of the NMOS is same as VDD or that of the PMOS is ground level. This is called the *floating switch problem* which is a serious concern in low-voltage switched-capacitor circuit design.

### *2.1.2. Noise*

Both switches and opamps contribute to the overall noise of an ADC. Minimizing this electronic noise is a massive design challenge when the supply voltage is very low. Low supply voltage results in reduction of available input and output signal power. Therefore the noise power from the circuit should be down-scaled to maintain the same signal-to-noise ratio (SNR) or dynamic range (DR). Since the noise power in an SC circuit is inversely proportional to the capacitance, larger capacitance is required to lower noise. This increased capacitance mandates larger transconductance (gm) to maintain the bandwidth. For this reason, low-voltage circuits mandate high power consumption to achieve the SNR, DR, and operational speed of high-voltage circuits.

### *2.1.3. Distortion*

Low distortion is as important as high DR in high performance applications. Low supply voltage limits the maximum input and output signal swing compared to that of similar circuit operating. Limited signal swing range translates to lower dynamic range. In order to maximize the DR, rail-to-rail signal swings are required. However, this rail-to-rail signal swing conflicts with the low distortion requirement. Large swing increases the nonlinearity of both the CMOS input sampling switches and the opamp output stage.

## 2.2. Low-voltage Circuit Design Techniques

Even though switched-capacitor circuits support robust and accurate analog design, the problems described in the previous section make low-voltage switched-capacitor circuit implementations very difficult. So, several existing low-voltage techniques have been proposed for overcoming these problems. They are introduced in this section.

### *2.2.1. Low-threshold Voltage Device*

Special process that lowers the threshold voltage can be used to increase the switch conductance [1]. This can be a solution for low-voltage supply. However, this means the cost of extra masks and process steps which are not always available in standard CMOS processes. Therefore, low-threshold voltage devices are not very attractive in cost-benefit considerations for mixed-signal integration.

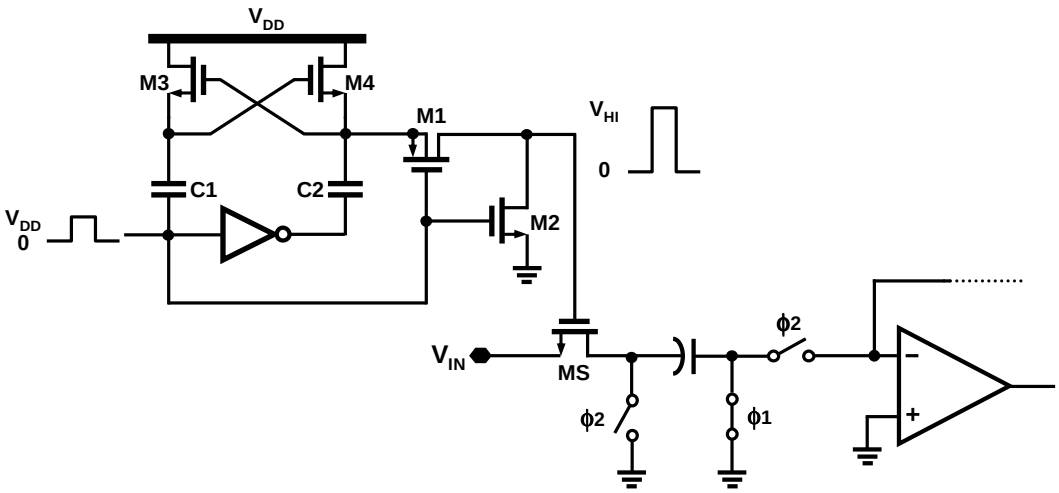



Figure 2.2: A clock boosting circuit.

## 2.2.2. *Clock Boosting*

The clock voltage boosting technique increases the gate-source overdrive typically achieved by doubling the clock voltage applied to the gate of an NMOS floating switch. A boosting circuit is shown in Fig. 2.2 [2]. When the clock input signal is low, an inverted clock will pump the voltage at the top plate of $C_2$ to be almost $2V_{DD}$ and PMOS device M1 will turn on to pass the boosted voltage to the gate of the floating switch MS. The peak voltage of the boosted clock signal is

$$V_{HI} = 2V_{DD}\frac{C_2}{C_2 + C_p + C_{gate,MS}} \tag{2.3}$$

where $C_p$ is the parasitic capacitance at the top plate of $C_2$ and $C_{gate,MS}$ is the gate capacitance of the floating switch MS.

This technique is easily implemented by simply clock voltage doubling. However, this approach introduces severe reliability issues in fine-line CMOS technolo-

gies due to the gate-oxide stress and p-n junction problems.

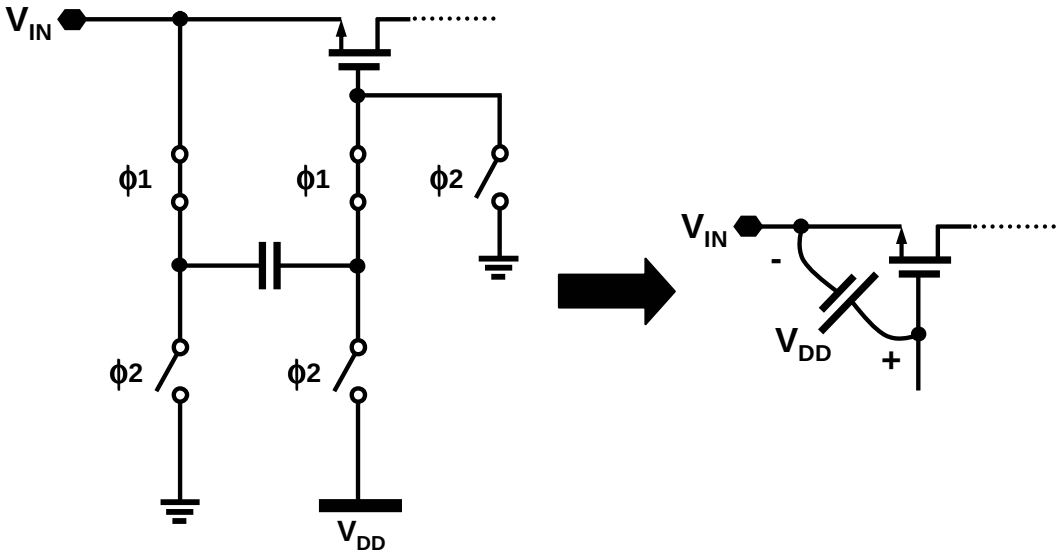



Figure 2.3: A conceptual diagram of clock bootstrapping circuit.

### *2.2.3. Clock Bootstrapping*

Another possible solution for the floating switch problem is the clock bootstrapping circuit [3, 12, 13]. Its conceptual diagram is shown in Fig. 2.3. Since the capacitor is precharged to $V_{DD}$, this circuit provides a boosted clock with constant gate-source voltage, $V_{gs}$ to the switches for all levels of $V_{IN}$.

It improves circuit reliability compared to the clock boosting scheme by limiting the gate-source voltage to less than the supply voltage. Linearity of the switch is also improved due to constant on-resistance of the transistor. However, bootstrapping circuits require many extra elements and increase circuit complexity. In addition, separate circuit blocks are required for all floating switches. That gives rise to larger die area, increased capacitive load, and higher power consumption.

## 2.2.4. Switched Opamp Technique (SO)

The third low-voltage design technique [4,14] is the switched opamp technique in which the floating switch is replaced by an output disabled opamp as shown in Fig. 2.4. This is very good for modern CMOS technology because no element in the circuit requires a high voltage level. However, since the opamps are turned off every half clock cycle, the technique suffers from limited speeds. The transients introduced during power up and power down limit the clock frequency.

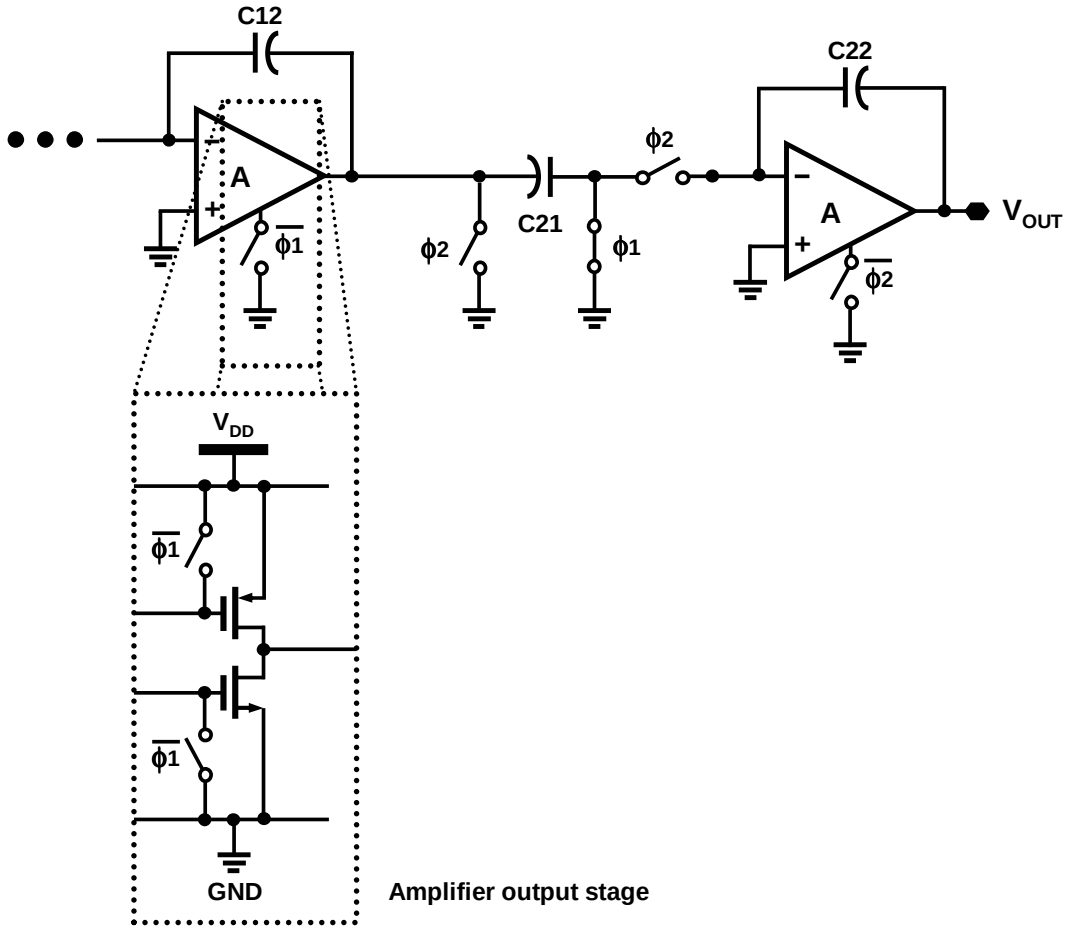



Figure 2.4: A switched opamp SCI circuit.

### *2.2.5. Opamp Reset Switching Technique (ORST)*

In the opamp reset switching technique [5, 6], the opamp is kept on while the floating switch is eliminated as shown in Fig. 2.5. After the previous stage output is sampled by the sampling capacitor C1 during phase $\phi 1$, the previous stage opamp is placed into the unity-gain feedback configuration during phase $\phi 2$ to provide the fixed reset reference. Unlike the SO technique, the opamp does not have to enter the off state. This technique can eliminate the transient time limitation of SO, hence, the circuit can operate at higher clock frequencies. As with SO, neither a floating switch is used nor does it require clock boosting or bootstrapping circuits. Both techniques are free from any reliability issues and are suitable for low-voltage CMOS technologies. However, this technique has some implementation disadvantages. It is not compatible with fully differential opamps. ORST can be implemented only with pseudo-differential opamp because the opamp should drive output as a reset voltage during the reset phase.

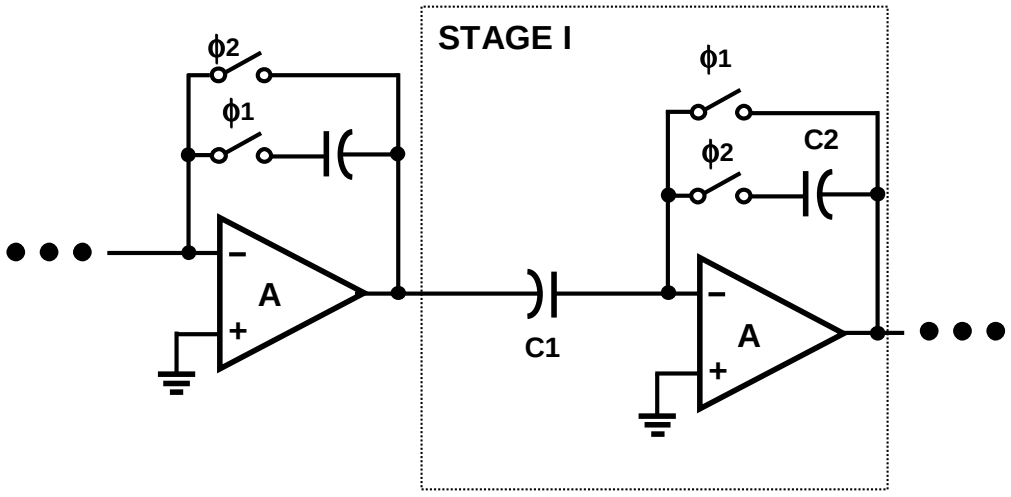



Figure 2.5: An opamp reset switching SCI circuit.

### *2.2.6. Switched-RC Technique*

In the switched-RC technique [7], as shown in Fig. 2.6, the input switched capacitor branch of a conventional SCI is replaced by a switched-RC branch, in which the floating switch of the conventional integrator in replaced by a resistor R1. During phase $\phi 1$, C1 samples the input voltage using a passive element R rather than a floating switch or active element such as an opamp. During $\phi 2$, C1 transfers the charge to C2. This technique has several benefits for low-voltage applications. First, it obviates the need for the floating switch. Second, it can achieve very high input sampling linearity irrespective of the supply voltage level. Third, the operation speed of the reset phase is never limited by the opamp bandwidth. Fourth, this technique can be implemented using fully differential opamp structures unlike in ORST.

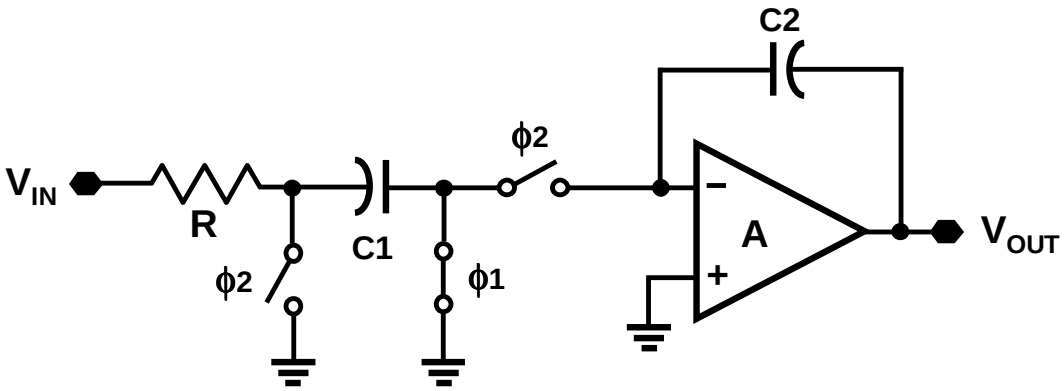



Figure 2.6: A switched-RC SCI circuit.

## 2.3. Low-Power Circuit Design Techniques

Several existing low-voltage techniques that have been proposed for solving the floating switch problem and used for low-voltage switched capacitor circuit designs, as explained in previous sections, are unsuitable for reduced power consumption. The primary purpose of low-voltage design is low-power consumption especially for portable applications. Low-voltage power supplies can greatly reduce power consumption in digital circuits. On the other hand, low supply voltage increases power consumption in analog circuits because the available maximum analog signal power is reduced by the low-voltage supply. For this reason, low-power design techniques which are compatible with low-voltage operation are required.

### *2.3.1. Double Sampling Technique (DS)*

Double sampling techniques [9, 15–18] can achieve twice the sampling frequency in switched-capacitor circuits without extra requirements for opamp settling time. Alternatively, the techniques allow a halving the clock frequency thereby minimizing power consumption. Consequently, double sampling techniques can be very useful for low power switched capacitor circuit designs. An SCI that uses double sampling is shown in Fig. 2.7. During phase $\phi 1$, CS1 samples the input and CS2 transfers the charge that was sampled previously to CF. During $\phi 2$, CS1 transfers its charge to CF, and CS2 samples the input. In other words, the output is updated during both phases. The operation speed is twice as fast as the conventional single sampling integrator.

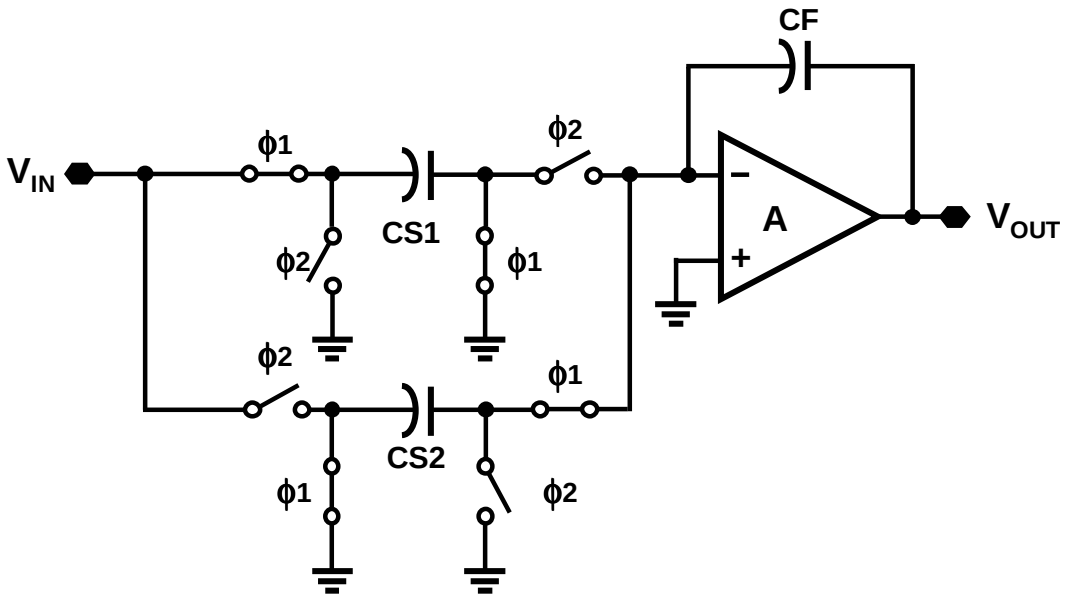



Figure 2.7: A double-sampling SCI circuit.

### *2.3.2. Amplifier Sharing Technique*

In amplifier sharing techniques [19, 20], opamps are shared between two consecutive stages in high-order delta-sigma ADCs or pipelined ADCs. Fig. 2.8 is an example of amplifier sharing in an SCI. During input sampling phase of the conventional SCI, the opamp does not have to be active. For example, the opamp in the first integrator is in the idle state during phase $\phi 1$, but that in the second integrator is active during the same clock phase. Therefore, the opamp can be shared between the two consecutive integrator stages. This technique needs only half the number of opamps, while maintaining the same bandwidth. Therefore, this technique can save up to half the power consumption.

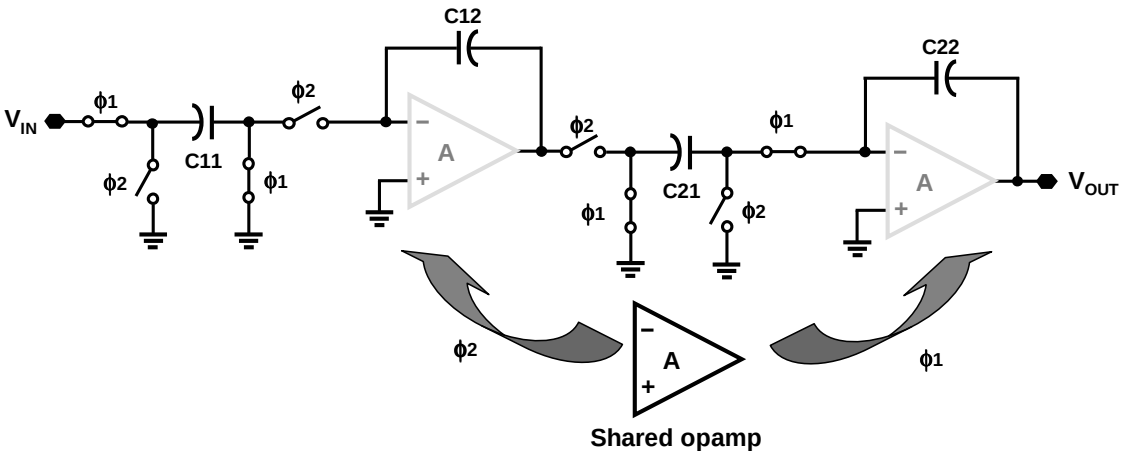



Figure 2.8: An amplifier sharing SCI circuit.

### *2.3.3. Class-AB Amplifier Output Stage*

The class-AB output stage is more power efficient than the class-A output stage in switched capacitor circuits [21]. Very high slew rates are obtained from the class-AB output stage with very small power consumption. For Class-AB opamps, the power dissipation is very small and depends on the input signal magnitude. But the class-AB output stage has poor linearity characteristic. Therefore, class-AB opamps are not preferred for high-resolution and high-linearity applications.

# CHAPTER 3. ANALOG-TO-DIGITAL CONVERTER (ADC) BASICS

This chapter presents necessary background in the field of ADCs. The general concepts of ADCs with emphasis on Nyquist-rate and oversampled ADCs are introduced. ADCs have many architectures for various applications. This chapter covers two of them, namely, delta-sigma and algorithmic ADCs, to better understand the applications proposed in this thesis.

## 3.1. ADCs

Digital signal processing, as opposed to analog signal processing, is the preferred method in implementing large electronic systems. Digital circuits offer lower sensitivity to noise, robustness to supply and process variations, easier design and testing, and better programmability. In particular, aggressive down-scaling of IC process has allowed new generations of digital circuits to achieve higher speed, integration of more functionality on chips, low power consumption, and low cost.

Even if the digital signal processing provides a strong low-cost incentive, naturally occurring signals are analog, and human beings perceive and retain information in analog form. In order to interface digital signal processors with the analog world, data acquisition circuits such as ADCs must be used. A simplified diagram of an ADC and the interface between analog world and a digital signal processor is illustrated in Fig. 3.1. Data conversion interfaces find applications in consumer

electronics, portable multimedia systems, medical systems, and aerospace systems.

ADCs often appear as the bottleneck in data processing applications, limiting the overall speed or precision due to their extensive use of mixed analog-digital operations. A number of ADC architectures such as oversampled, one-step or multi-step flash, folding and/or interpolated, pipelined, successive approximation configuration, subranging, and algorithmic structure have been employed depending on the speed and resolution requirements. This chapter covers two ADC architectures, oversampled and algorithmic ADCs which were implemented as prototype ICs to validate the applications proposed in this thesis.

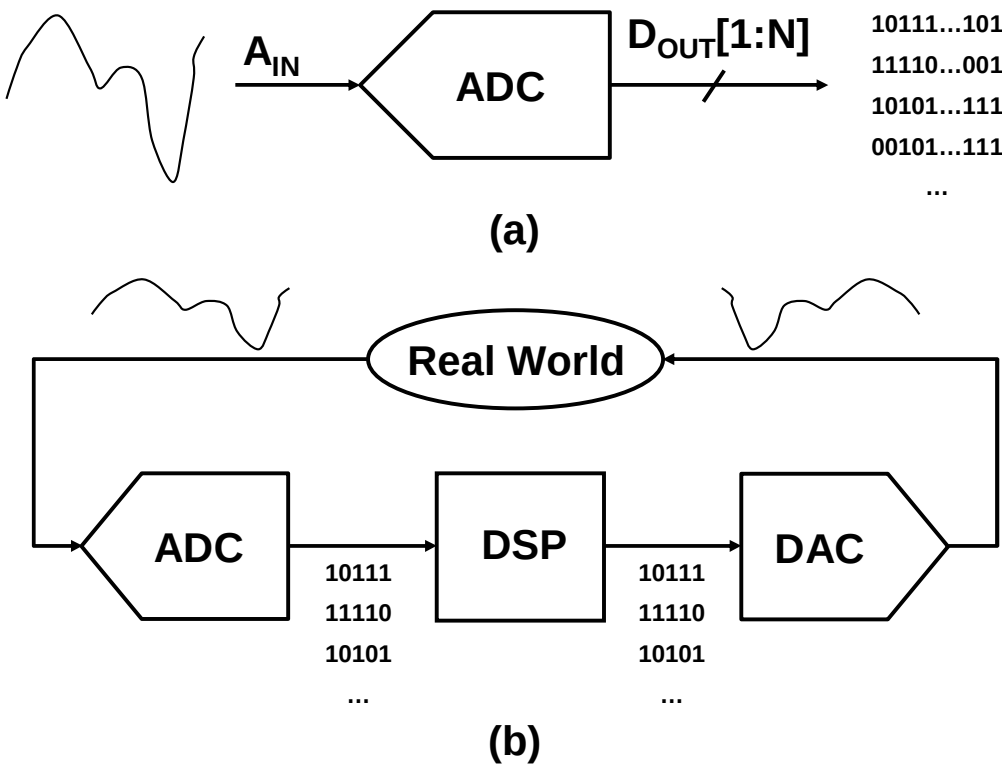



Figure 3.1: (a) A simplified block diagram of an ADC and (b) the interface between analog world and a digital processor.

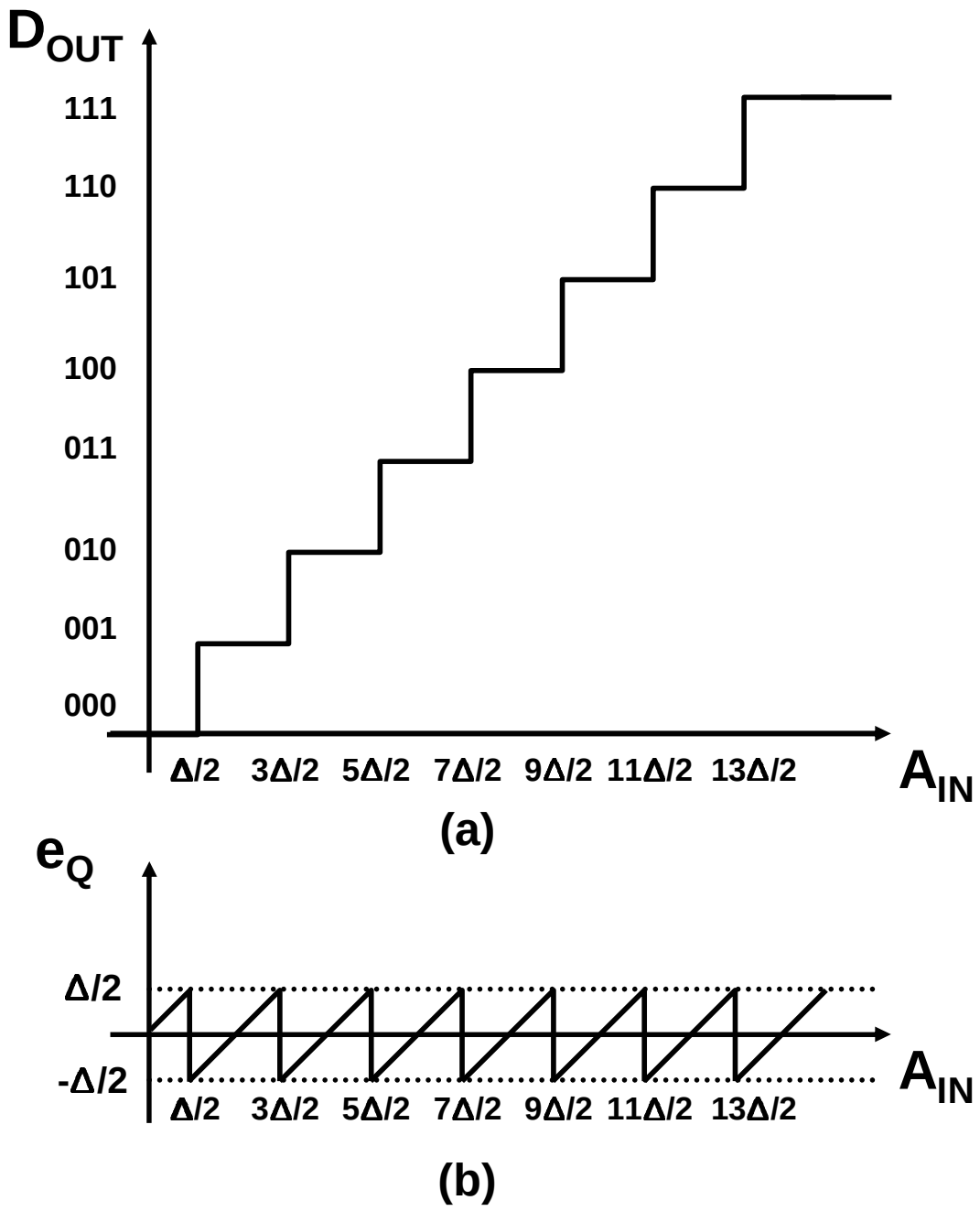



Figure 3.2: (a) Transfer function curve of a 3-bit ADC. (b) Quantization error of the ADC.

### 3.1.1. General behavior of ADCs

ADCs produce a digital output, $D_{OUT}$, as a function of the analog input, $A_{IN}$:

$$D_{OUT} = f(A_{IN})\,. \tag{3.1}$$

While the input is time-continuous signal which has an infinite number of values, the output should be selected from a finite set of digital codes given by the ADC's resolution. Fig. 3.2 (a) depicts a simple transfer function curve of a 3-bit ADC where the analog input is approximated with the nearest reference level. This approximation in ADCs is called *quantization* and the difference between the original input and the digitized output is called the *quantization error* which is denoted by $e_Q$. As shown in Fig. 3.2 (b), $e_Q$ varies with the maximum occurring before each code transition. If we assume that $e_Q$ is uniformly distributed , the quantization noise power can be expressed as the mean square of $e_Q$:

$$\overline{e_Q^2} = \frac{\Delta^2}{12}\,. \tag{3.2}$$

If the analog input is a sinusoid with the amplitude, $A = V_{REF}/2$ , its power is equal to $A^2/2 = 2^{2N}\Delta^2/8$. Thus, the signal-to-quantization noise ratio (SQNR) of an N-bit ADC is

$$SQNR = \frac{3}{2}2^{2N} = 6.02N + 1.76(dB)\,. \tag{3.3}$$

## 3.2. Delta-sigma ADC basics

Delta-sigma architecture has two important features, *oversampling* and *noise shaping*.

### *3.2.1. Oversampling*

Oversampling is a simple way to reduce quantization noise and thereby to increase SNR. Oversampling is using a higher sampling rate than the Nyquist rate. The factor OSR is referred to as the oversampling ratio (OSR), $OSR = f_s/2f_B$. Fig. 3.3 (a) and (b) are output spectra of a Nyquist ADC and an oversampled ADC. In the case of Nyquist sampling, the noise power spreads over signal band, $f_B$, which is half the sampling frequency, $f_s/2$. So, the SQNR is equal to (6N+1.73) dB in Eq. 3.3. However, if the signal is sampled by rate $f_S$, which is OSR times faster than the Nyquist frequency, $2f_B$. An octave increase in the OSR results in an increase in SNR by 3dB.

### *3.2.2. Noise Shaping*

Though oversampling is a very simple way to improve SNR, it is not very practical to obtain very high resolution such as 16 - 20 bits. In delta-sigma modulation (DSM), *noise shaping* is employed to relax OSR or, in other words, obtain higher SNR. The noise shaping property of the delta-sigma modulator can sup-

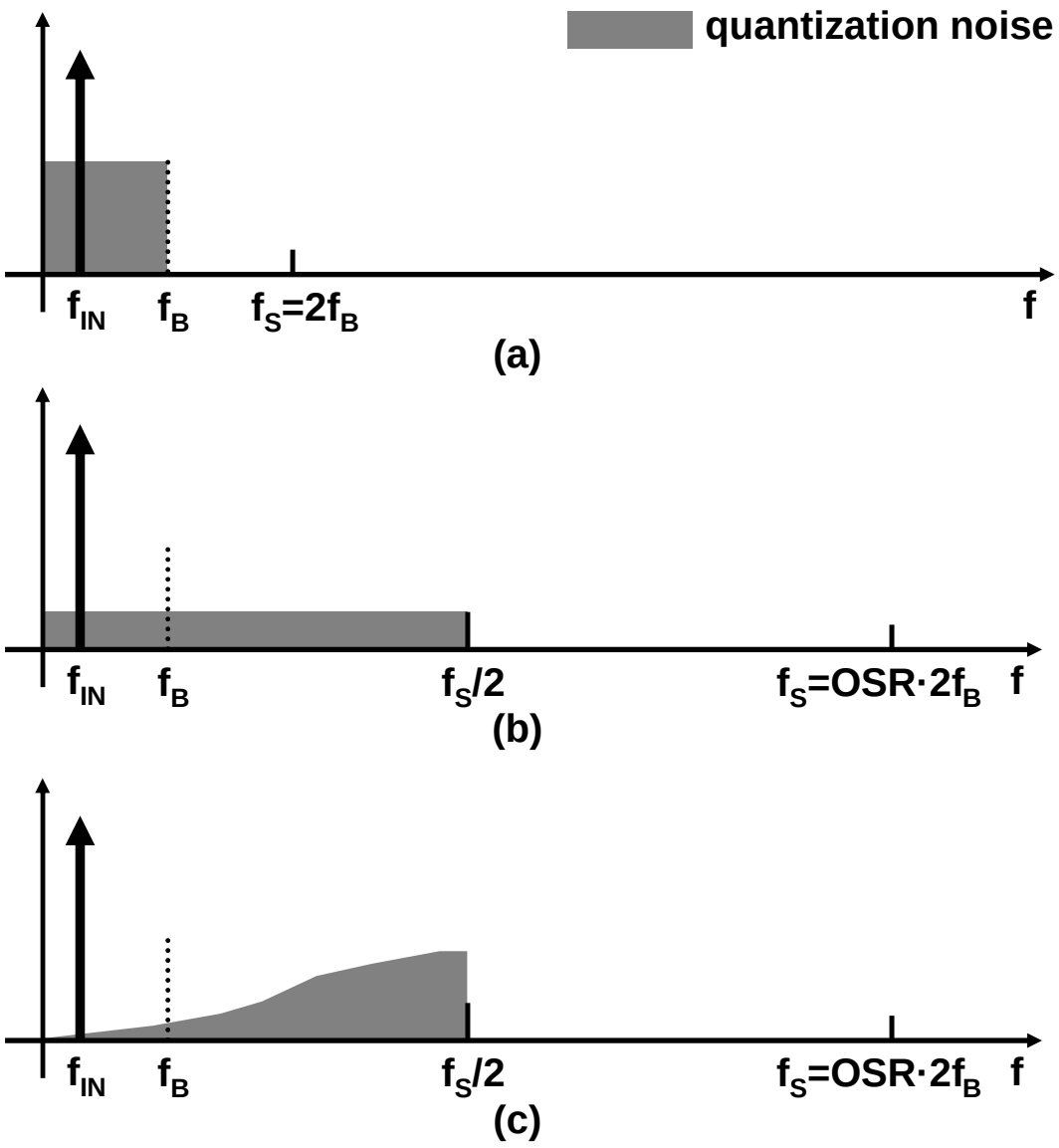



Figure 3.3: Spectra of (a) a Nyquist sampling, (b) an oversampling, and (c) an oversampling with noise shaping.

press the in-band quantization noise as depicted in Fig. 3.3 (c). Noise shaping of the quantization noise can be realized by a feedback structure including a loop filter, which is an integrator for a first-order low-pass DSM, and a coarse quantizer. Fig. 3.4 shows a linear model of a first-order DSM. The output in z-domain can

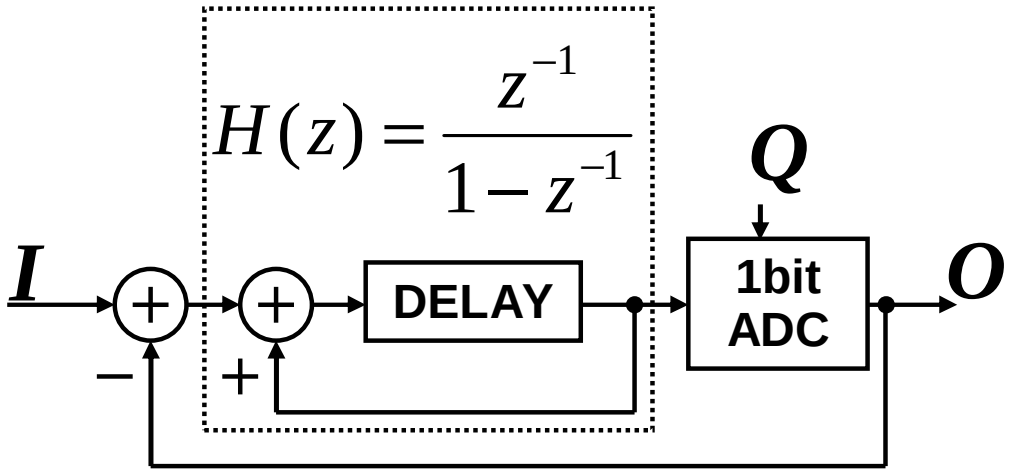



Figure 3.4: The block diagram of typical first-order DSM.

be expressed as:

$$O(z) = STF(z)I(z) + NTF(z)Q(z)\,. \tag{3.4}$$

where

$$STF(z) = H(z)/(1 + H(z)) \tag{3.5}$$

$$NTF(z) = 1/(1 + H(z))\,. \tag{3.6}$$

The STF(z) is the input signal transfer function and NTF(z) is the noise transfer function. The loop filter transfer function, H(z) of the first-order DSM in Fig. 3.4 is $z^{-1}/(1 - z^{-1})$. Therefore, The Eq. 3.4 can be rewritten as :

$$O(z) = z^{-1}I(z) + (1 - z^{-1})Q(z)\,. \tag{3.7}$$

The quantization noise is shaped by a first-order differentiator. That results in reduced noise power in the signal band, $f_B$, and increased noise power out of the

signal band. Therefore, the proper choice of noise shaping order and OSR can achieve high SNR in signal band.

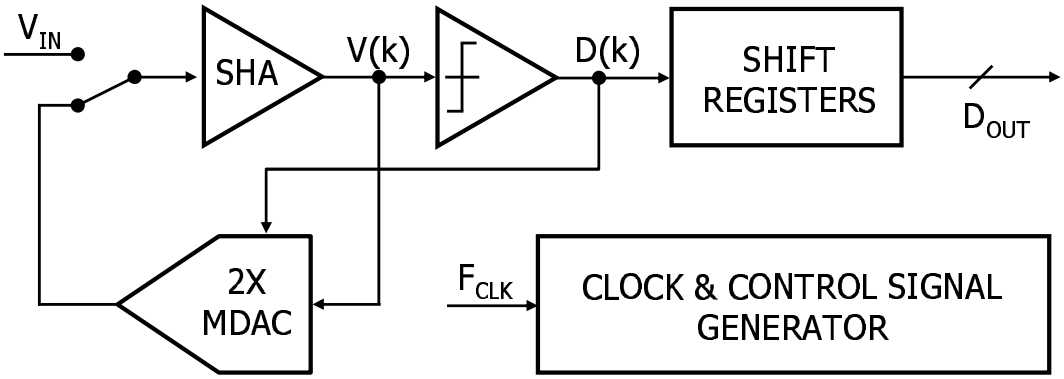



Figure 3.5: The block diagram of typical algorithmic ADC.

## 3.3. Algorithmic ADC basics

A simplified 1-bit/cycle algorithmic ADC structure is shown in Fig. 3.5. The algorithmic ADC architecture has been chosen for applications requiring low power, small chip area, and high-resolution. Algorithmic ADCs recycle the sample-and-hold amplifier (SHA) and the multiplying digital-to-analog converter (MDAC), thus reducing the hardware. For the first bit (MSB) conversion time, $V(1) = V_{IN}$, and the SHA output voltage is doubled in amplitude and added to a reference, resulting in $V(k+1) = 2V(k)+D(k)V_{REF}$. The output of the single bit comparator, $D(k)$, is either +1 or -1. The signal residue is propagated to the next cycle.

The main disadvantage of algorithmic ADCs is relatively long conversion cycles, primarily because of the closed-loop amplifier and their serial nature of operation. However, the conversion rate of the algorithmic ADC has been increasing

steadily with improvements in technology.

# CHAPTER 4. PROPOSED SOLUTIONS FOR LOW-VOLTAGE AND LOW-POWER ADCS

This chapter presents two main techniques that can be solutions for both low-voltage and low-power ADCs. The first is a low-voltage DS technique for delta-sigma ADCs [8]. The second is an improved clocking scheme for algorithmic ADCs [10, 11].

## 4.1. A Low-Voltage Double-Sampling Technique for Delta-Sigma ADCs

In this section, a low-voltage DS technique is proposed. As described in Sec. 2.3.1., DS technique in delta-sigma ADC design can halve the clock frequency for a given OSR. This means that an SNR improvement of 6N+3 dB can be achieved for an Nth order delta-sigma ADC. For this reason, DS technique can be a very useful power reduction technique. However, this technique has a serious disadvantage caused by the path gain mismatch, as explained in the next subsection. The proposed solution is explained in the following subsection.

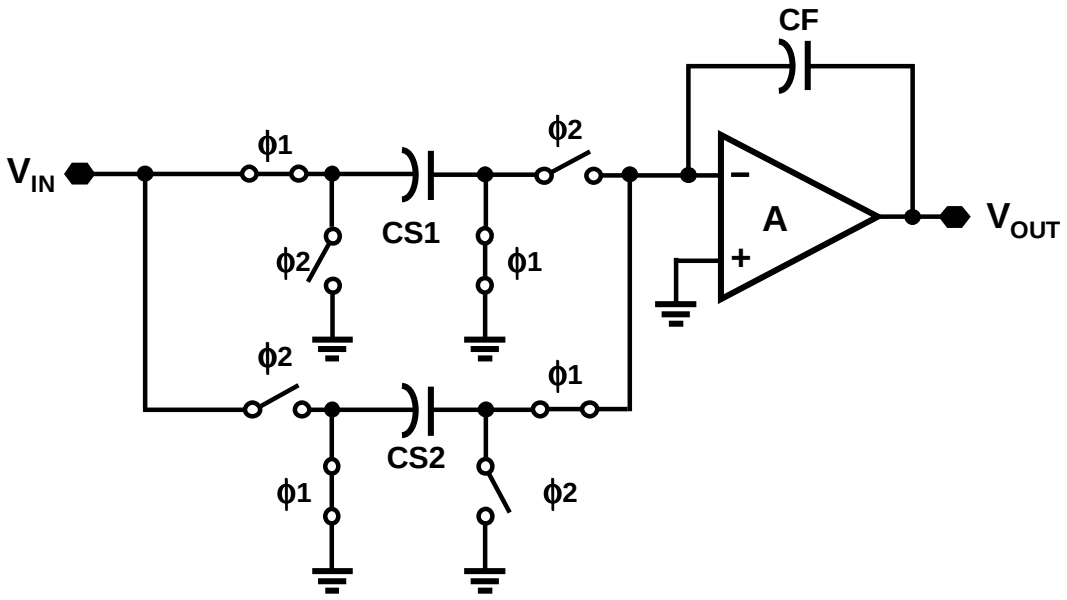



Figure 4.1: A double-sampling SCI circuit.

### *4.1.1. Path Gain Mismatch*

The schematic of the DS SCI in shown in Fig. 4.1. Each sampling capacitor samples the input during consecutive phases. Capacitor CS1 samples input $V_{IN}$ during $\phi 1$ phase, while CS2 samples $V_{IN}$ during $\phi 2$ phase. If CS1 is not equal to CS2, the change in the sampling capacitance from one phase to the next phase modulates the amplitude of the stored charge. The input-output relationship of the integrator with an ideal opamp can be written as

$$V_{OUT}(n) = V_{OUT}(n-1) + \frac{\overline{CS}}{CF} V_{IN}(n-1) + \frac{(-1)^n \Delta CS}{2CF} V_{IN}(n-1)\,. \qquad (4.1)$$

where $\overline{CS} = (CS1 + CS2)/2, \Delta CS = CS1 - CS2$, and time n=0 occurs when $\phi 2$ is high. The last term in equation 4.1 is the product of the input and $(-1)^n$, which is a modulation of the input by a sampled cosine at frequency $f_S/2$. If

$CS1 = CS2$, this term is zero and the circuit acts like an ideal discrete-time integrator. However, if $CS1 \neq CS2$, the integrator output is the sum of the input $V_{IN}(n)$ and a modulated version of the input.

The path gain mismatch effect is shown in Fig. 4.2. If the input is a low frequency signal which is band-limited by an anti-aliasing filter, the mismatch between $CS1$ and $CS2$ causes $V_{IN}$ to be modulated to a frequency band near the half clock frequency, $f_S/2$. This effect from input path gain mismatch is of little consequence, because the signal in this low frequency band is greatly attenuated by the digital low-pass filter, as shown in Fig. 4.2 (b). However, the feedback path DAC output has a large high frequency noise power as shown in 4.2 (c). The feedback signal is mixed down to the baseband, which increases the in-band noise power, hence decreasing the SNR drastically.

### *4.1.2. Floating Switched-Capacitor Configuration*

The configuration, named here the *floating switched capacitor* [9] is shown in Fig. 4.3. This SCI updates the input charge in both phases of the clock. Obviously, the effective sampling rate is twice the clock frequency. The transfer function of the fully floating SCI is given by

$$\frac{V_{OUT}(z)}{V_{IN}(z)} = \frac{1 + z^{-1}}{1 - z^{-1}} \frac{C_S}{C_F}. \tag{4.2}$$

As shown in the equation 4.2, the mismatch $\Delta C_S$ does not appear, implying that the mismatch does not affect the signal processed by the integrators. On

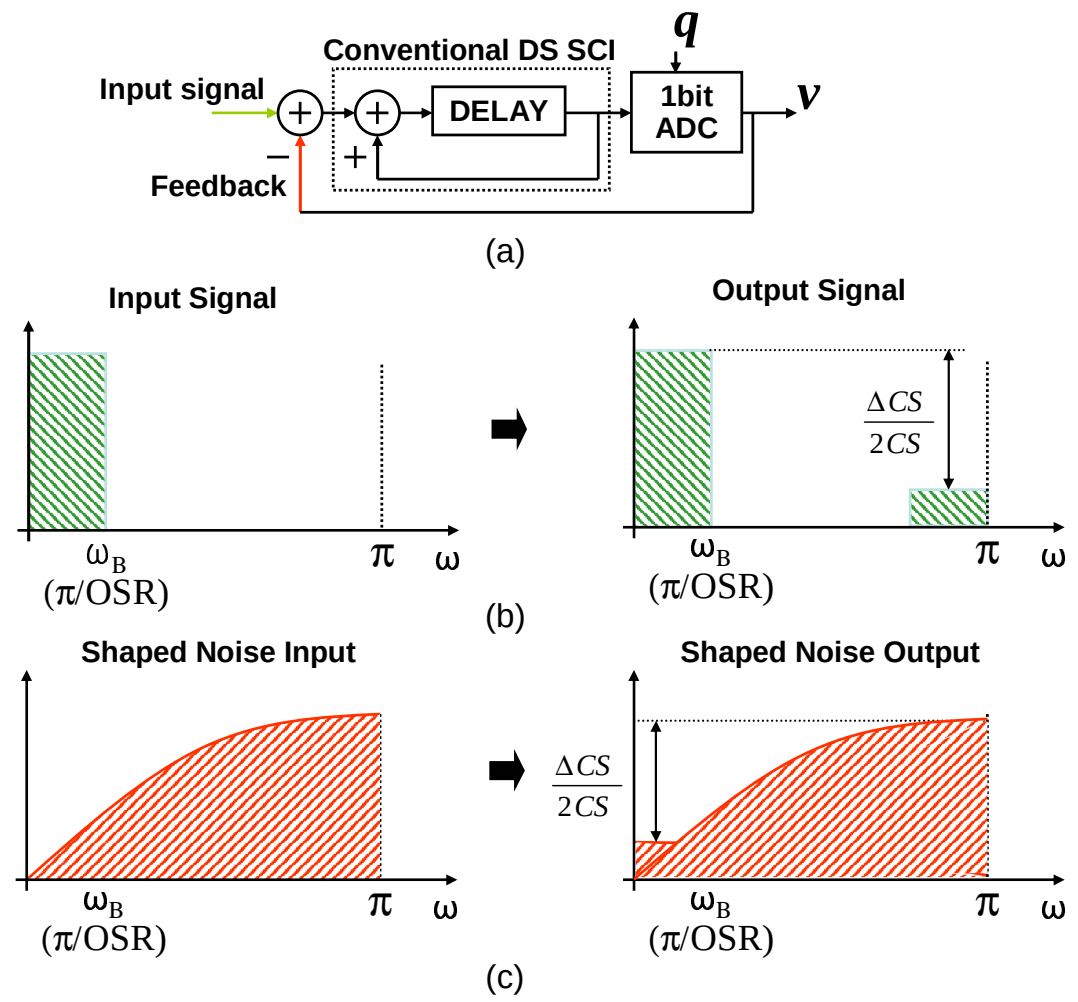



Figure 4.2: A path gain mismatch effect of a double-sampled 1st order delta-sigma ADC. (a) Block diagram of a double-sampled delta-sigma ADC. (b) The gain mismatch effect on input signal path. (c) The gain mismatch effect on the feedback path.

the other hand, the transfer function differs from that of a conventional SCI. The additional factor $1 + z^{-1}$ is included in the transfer function.

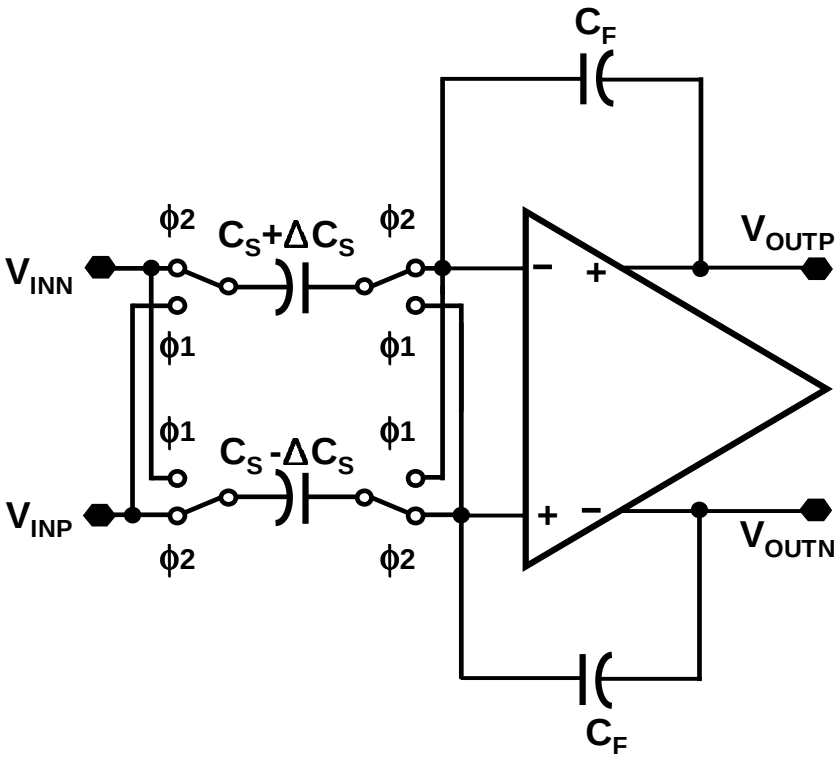



Figure 4.3: Floating differential SCI.

### *4.1.3. Proposed Low-Voltage Double-Sampling SCI*

Several existing low-voltage design techniques are introduced and discussed in Sec. 2.2. A brief comparison of them is given in the table 4.1. The DS technique can be applied to many of the low-voltage design techniques. Clock boosting or bootstrapping can make the DS technique applicable for low-voltage designs. But, as mentioned earlier, they suffer from reliability issues and require extra circuit complexity. SO and ORST techniques are not compatible with DS technique, because the active component (opamp) has to work during both phases. The switched-RC technique can provide many advantages if it is used for low-voltage

Table 4.1: Low-voltage techniques comparison

| Techniques | Characteristics | DS possible? | Floating Switches? |
|---|---|---|---|
| Clock boosting | Straightforward & simple<br>Not tolerant | Yes | Yes |
| Clock bootstrapping | Extra circuit and complexity for all floating switches | Yes | Yes |
| Low threshold voltage devices | Leakage<br>Extra mask and process step | Yes | Yes |
| Switched opamp tech. (SO) | Limited speed | No | No |
| Opamp-reset switching tech. | Faster than SO tech. | No | No |
| Switched-RC tech. | High linearity sampling<br>High Reliability | Yes | No |

DS design. First, the switched-RC provides highly linear sampling. Second, the DS technique can be applied without the need for clock boosting or bootstrapping. Finally, the DS switched-RC circuit overcomes the drawbacks inherent in the original form of the switched-RC technique. The advantages of DS switched-RC are:

- The DS switched-RC technique provides a constant input resistance, that of the SCI, because the previous stage output load condition is kept the same during both phases.
- The opamp DC gain is the same between the two phases because the opamp output load condition is the same.
- The DS switched-RC also obviates the need for half-delay elements [7], because a half-period delay translates into a full period delay for DS. Full period delay can provide more freedom for composing signal and noise transfer func-

tions.

The SCI circuit with the proposed low-voltage DS technique is shown in Fig. 4.4. A split switched-RC input branch [7] is used to keep constant the common mode level of the integrator. During the integrating phase, half of the sampling capacitor is connected to $V_{DD}$, while the other half is connected to $V_{SS}$. This results in a constant common mode level of half $V_{DD}$ for the integrator during both phases, avoiding any need for additional level shifting circuits.

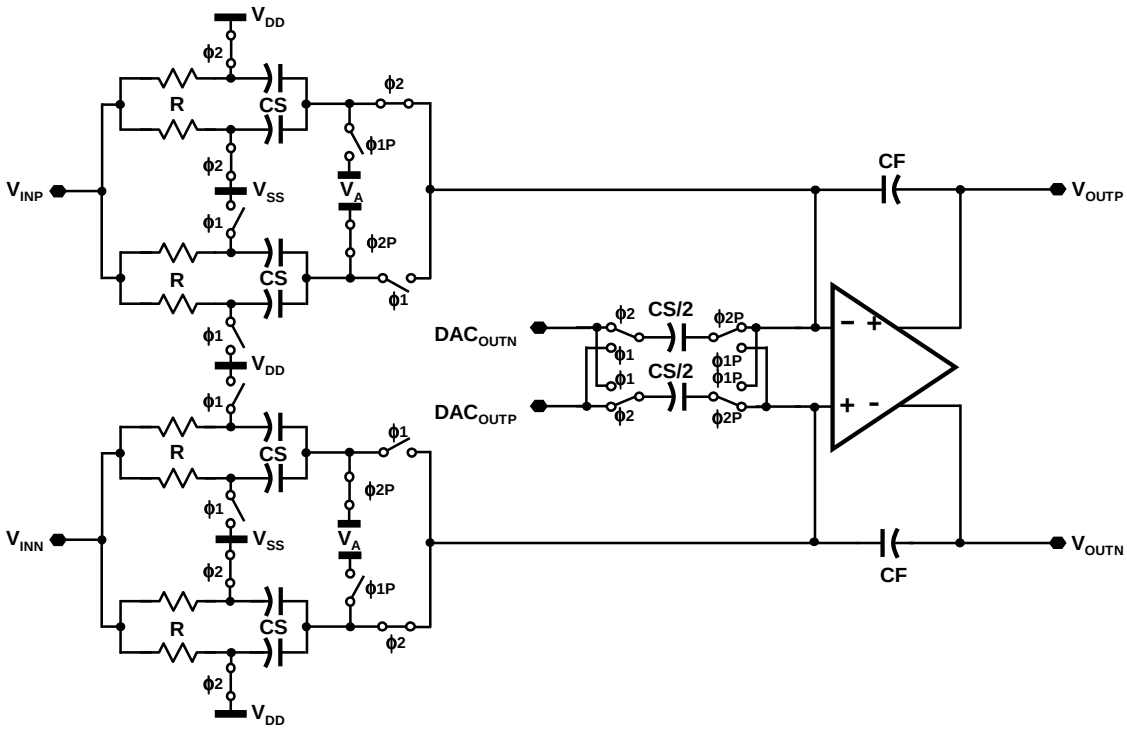



Figure 4.4: The proposed low-voltage fully differential DS integrator.

## 4.2. Improved Clocking Scheme for Algorithmic ADC

In this section, an improved clocking scheme for algorithmic ADCs is proposed.

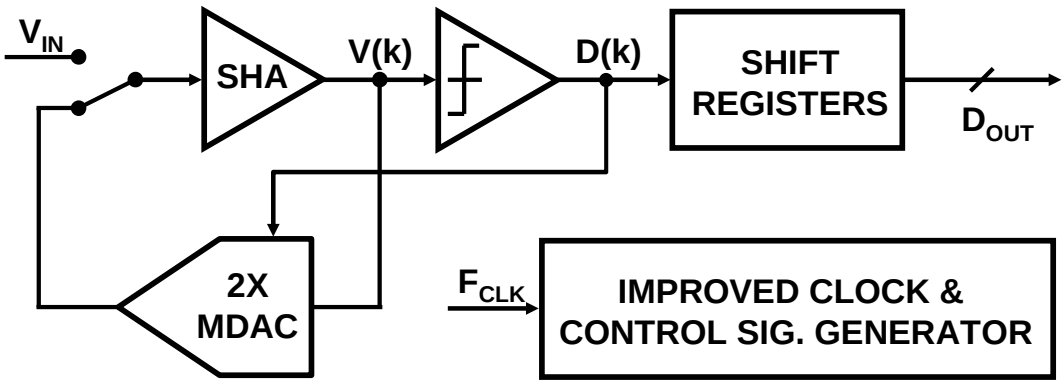



Figure 4.5: The block diagram of the proposed algorithmic ADC.

### *4.2.1. Settling Time in Algorithmic ADCs*

In the proposed algorithmic ADC shown in Fig. 4.5, the input is first sampled onto the sample and hold amplifier (SHA) capacitor and then quantized by a comparator to generate the most significant bit (MSB). The converter generates the residue by adding or subtracting reference voltage $V_{REF}$ from the amplified input signal. In the case of single-bit per conversion cycle converter, the input is amplified by an ideal interstage gain of 2. For all the following cycles, this process is repeated with fedback residue voltage instead of the converter input voltage. The resolution of the converter depends on the accuracy of the interstage gain and

the settling accuracy of the SHA. In a conventional algorithmic ADC the maximum operating speed is determined by the settling time of the SHA. Typically, for an N-bit ADC, the total conversion time is equal to N*T where is T is clock period and is sufficiently long to accommodate N-bit settling accuracy of the SHA for the first residue generation. The signal residue is propagated to the next cycle. For accurate SHA output settling, the minimum required time is

$$t_{SHA} = (n + 1 - k) \cdot ln2/\omega_{SHA}\,. \tag{4.3}$$

where $n$ is the bit number of the algorithmic ADC, $k$ is the number of conversion cycles, and $\omega_{SHA}$ is the bandwidth of the SHA. The minimum time required for accurate MDAC output settling is

$$t_{MDAC} = (n + 1 - k) \cdot ln2/\omega_{MDAC}\,. \tag{4.4}$$

where $\omega_{MDAC}$ is the bandwidth of the MDAC. Minimum output settling time decreases with the number of conversion bits. The SHA and MDAC in the algorithmic ADC have to be reused for each conversion step, and they have to satisfy the minimum settling time requirement of the first conversion step. Therefore, the conventional algorithmic ADC wastes time after the first conversion cycle.

### *4.2.2. Proposed Clocking Scheme*

In a conventional algorithmic ADC, the conversion time for each bit is equal to the clock period irrespective of the weight of the resolved bit as shown in Fig. 4.6(a). In the proposed clocking scheme [10], as shown in Fig. 4.6 (b), after the most significant bit (MSB) conversion takes place, the minimum clock period

is determined by the conversion time required to calculate the residue. The accuracy requirement of the following conversion cycles is proportionally scaled and therefore the time for conversion can also be scaled. This internal clock relaxes the MSB conversion time and progressively reduces the following bit conversion times.

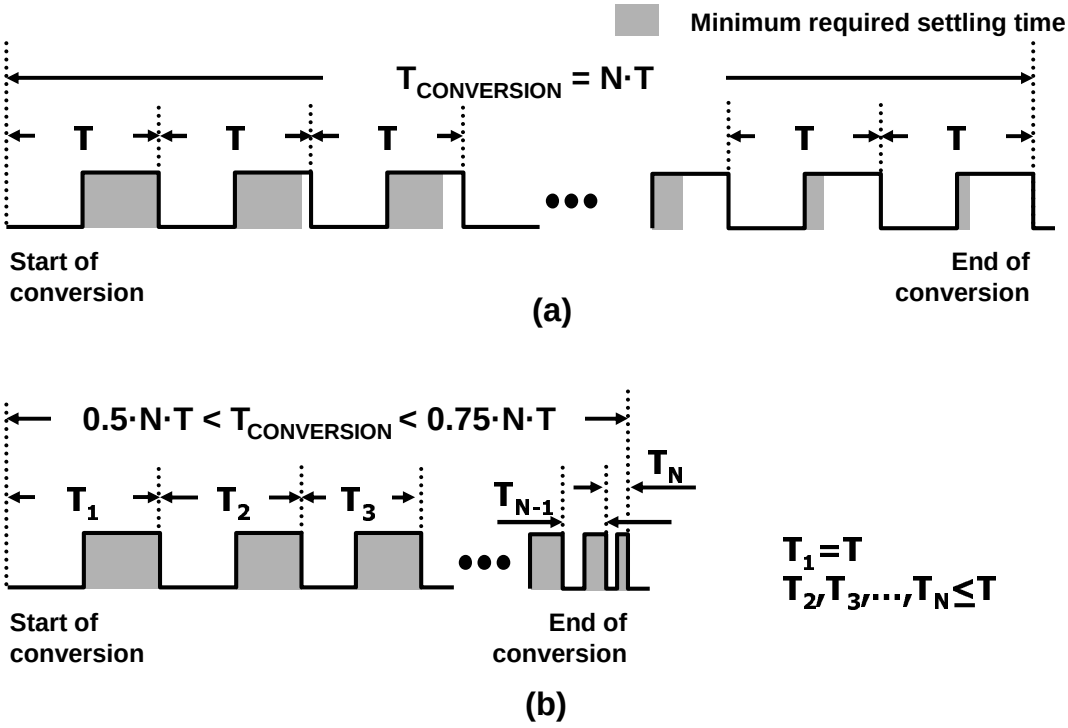



Figure 4.6: (a)The conventional and (b) proposed clock diagram of an N-bit algorithmic ADC.

The new clocking scheme can be made from pre-determined M phases. Examples of an optimized clock sequence for a 10 bit ADC made from 4 phases and 10 phases (conventional = 1 phase) are shown in Fig. 4.7 (a) and (b) respectively. In the example shown in Fig. 4.7 (a), the four different period widths T, 0.75T, 0.5T, and 0.25T are used for the ten conversion steps instead of using the same

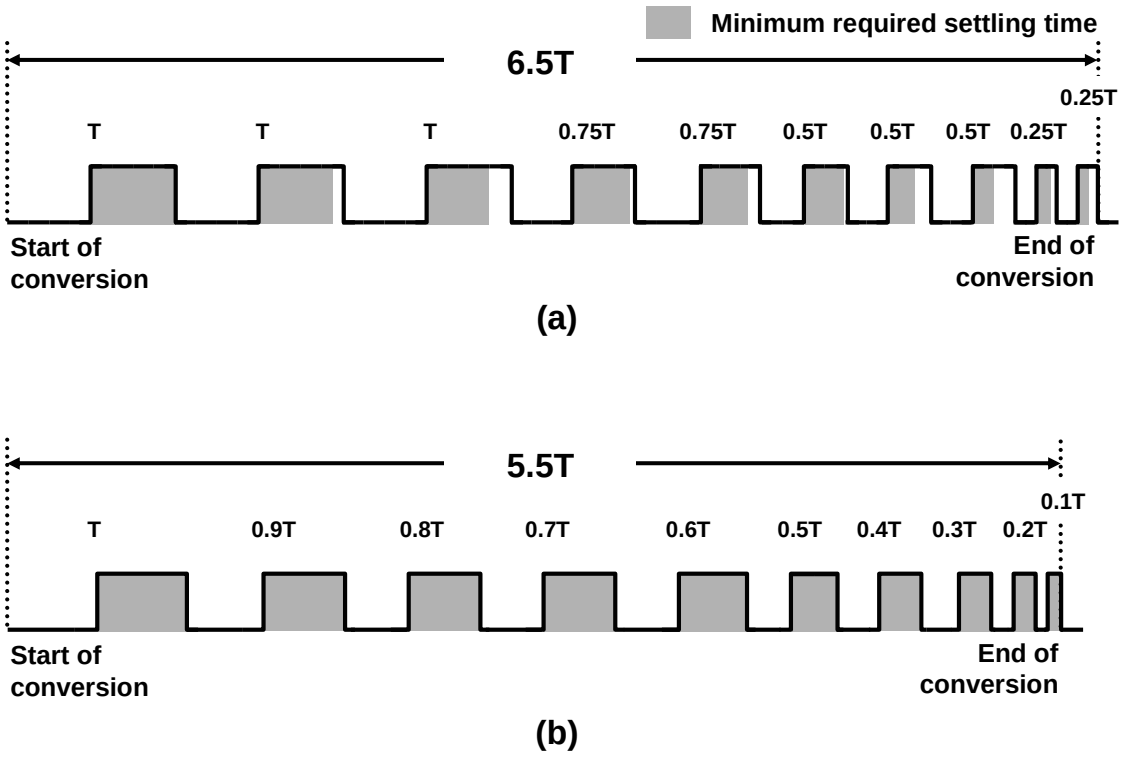



Figure 4.7: (a) an improved clock diagram which uses 4 phases for 10bit ADC, and (b) an improved clock diagram which uses 10 phases for 10bit ADC.

period T. The total conversion time is improved to 65% of that for the conventional conversion scheme. This translates to an overall conversion rate improvement of 54% where the overall conversion rate is 1/(total conversion time). In the example shown in Fig. 4.7(b), ten different timings from T to 0.1T are used for the ten conversion steps instead of using the same period T. The total conversion time is improved to 55% of that for the conventional conversion scheme. This translates to an overall conversion rate improvement of 82%.

To enable the proposed clocking scheme, the input clock must have additional phases for generating the proposed clock. Two feasible solutions are shown in Fig. 4.8 (a) and Fig. 4.8 (b). One solution is to provide an input clock with a

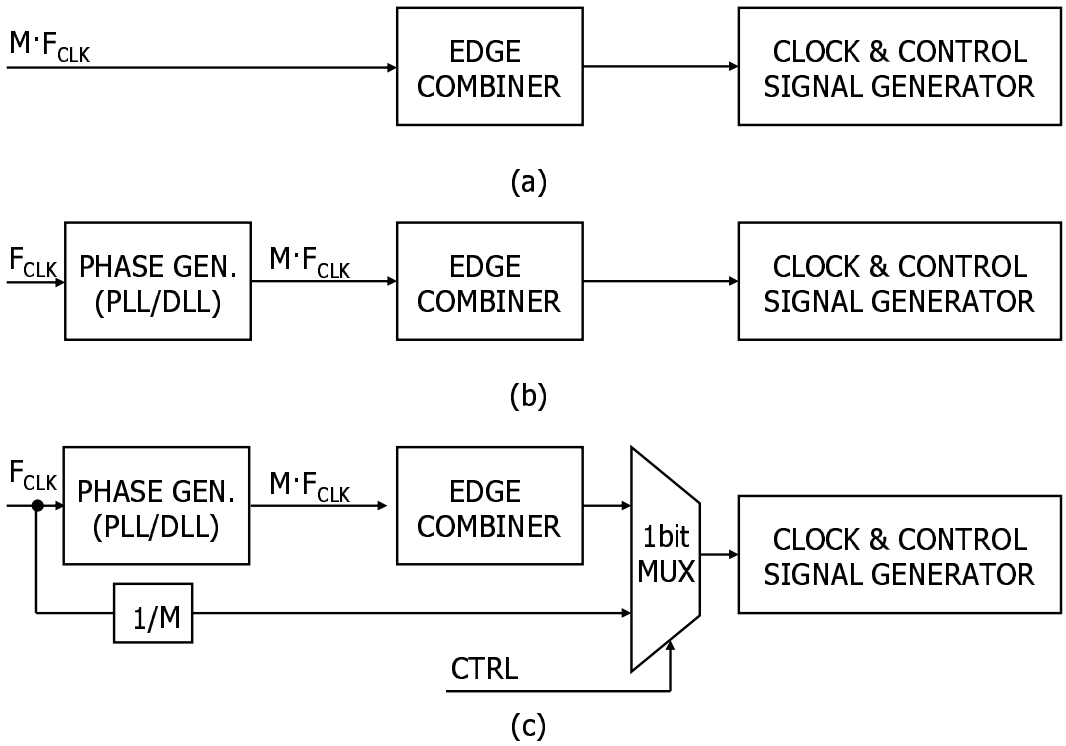



Figure 4.8: The optimized clock generator structure: (a) $Mf_{CLK}$ is received directly. (b) Phases are generated from an internal low cost PLL/DLL. (c) The phase generator output is bypassed during the timing for the first conversion step.

frequency M times higher than needed for the first stage, as shown in Fig. 4.8 (a). Another solution is to employ integrated phase locked loop (PLL) or delay locked loop (DLL) to generate the necessary phases, as shown in Fig. 4.8 (b). This PLL/DLL need not be high performance, because clock jitter is not important in later stages. Only the first conversion step where input signal sampling occurs is sensitive to clock jitter, as long as the later stages/cycles have enough time to settle. Jitter which occurs in the first conversion step is critical as in all ADCs because this can directly limit the SNDR. Therefore, as illustrated in Fig. 4.8(c), the timing for first conversion is propagated directly from the external clock input. The number of phases required to generate the optimized clock is a trade-off between circuit

complexity and improvement in conversion speed. For example, if we use 4 phases, then we can achieve 54% more speed as compared to the same ADC without any other notable disadvantages.

# CHAPTER 5. PROTOTYPE ICS DESIGN

Two prototype ICs, a 0.9V 92dB double-sampled switched-RC delta-sigma audio ADC and a 10MS/s 11-bit 0.19mm$^2$ algorithmic ADC were implemented to prove the effectiveness of the proposed solutions described in previous chapter. This chapter covers the design of the prototype IC.

## 5.1. 0.9V 92dB Double-Sampled Switched-RC Delta-Sigma Audio ADC

High-performance ADCs for portable applications should operate with a low voltage supply and also have low power consumption. DS is one possible solution for reducing power consumption. However, it requires complex bootstrapping schemes in low-voltage systems. The proposed low-voltage DS technique combined with switched-RC supports highly linear sampling without floating switch problems. A high-performance low-voltage DS audio ADC is designed with the proposed technique. The initial design target specifications summarized in Table 5.1 are focused on high-performance portable applications.

### *5.1.1. Topology Selection*

The maximum SQNR is given by the following expression:

Table 5.1: Target specifications of the audio delta-sigma ADC

| | |
|---|---|
| **Power supply voltage** | **0.9 V** |
| **Power consumption** | **2 mW** |
| **Input range** | **1.1 $V_{PP}$ (differential)** |
| **Peak SNR** | **90 dB** |
| **Peak SNDR** | **85 dB** |
| **Dynamic range** | **92 dB** |
| **Signal bandwidth** | **24 kHz** |
| **Sampling frequency** | **6.144 MHz** |
| **Clock frequency** | **3.072 MHz** |
| **Oversampling ratio** | **128** |
| **Technology** | **0.13μm CMOS** |

$$SQNR_{MAX} = 6.02N + 1.76 + (20L + 10)log_{10}OSR - 10log_{10}\frac{\pi^{2L}}{2L+1}\,. \qquad (5.1)$$

where $L$ is the order of a DSM, $N$ is the number of quantizer bit resolution. Single-loop delta-sigma topology offers several advantages for low-power, low-voltage operation, such as circuit simplicity and insensitivity to non-ideal circuits. However, this topology requires a higher order for a given OSR to achieve high SQNR. System-level simulations indicate that a third-order 1.5-bit (3-level) single-loop topology with DS offers the best tradeoff between the required clock frequency, amplifier bandwidth and SNR for the target audio ADC. The block diagram of the single-loop third-order delta-sigma ADC with a 1.5-bit quantizer is shown in

Fig. 5.1. The loop coefficients are set to [0.2, 0.3, 0.4]. These coefficients are chosen from behavioral simulations by sweeping the three coefficients. The modulator with these coefficients is very tolerant to the coefficient mismatches caused by capacitance mismatches and the inherent gain error of the switched-RC technique [7]. One major disadvantage of the conventional DS is noise folding due to path gain mismatch. The path gain mismatch in the forward signal path does not degrade performance significantly. However, in the feedback path, it degrades the SNR due to noise folding into the signal band. The integrator circuit used in this design is shown in Fig. 5.2. The DS using switched-RC branches is employed in the forward signal path, while fully-floating switched-capacitor branches that are insensitive to gain mismatch are utilized in both the first and second feedback paths [9]. A conventional DS is used in the third integrator feedback path because the use of conventional DS scheme eliminates the stability issues caused by the additional pole introduced in the fully-floating switched capacitor configuration. The DS switched-RC circuit not only doubles the OSR, but also overcomes some drawbacks of the switched-RC. The DS with the switched-RC allows a constant input resistance of the delta-sigma ADC, and the same opamp DC gain during both clock phases. Even though the required SNR is 90dB, the simulated peak SQNR is 110dB from this topology. It is necessary to minimize the quantization noise contribution in order to leave some space to other less predictable noise sources such as flicker, $kT/C$, and amplifier thermal noises.

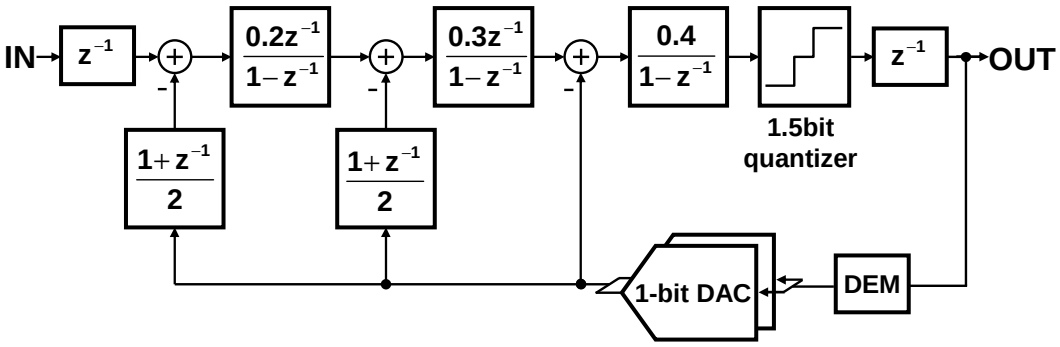



Figure 5.1: A third-order DS delta-sigma ADC topology.

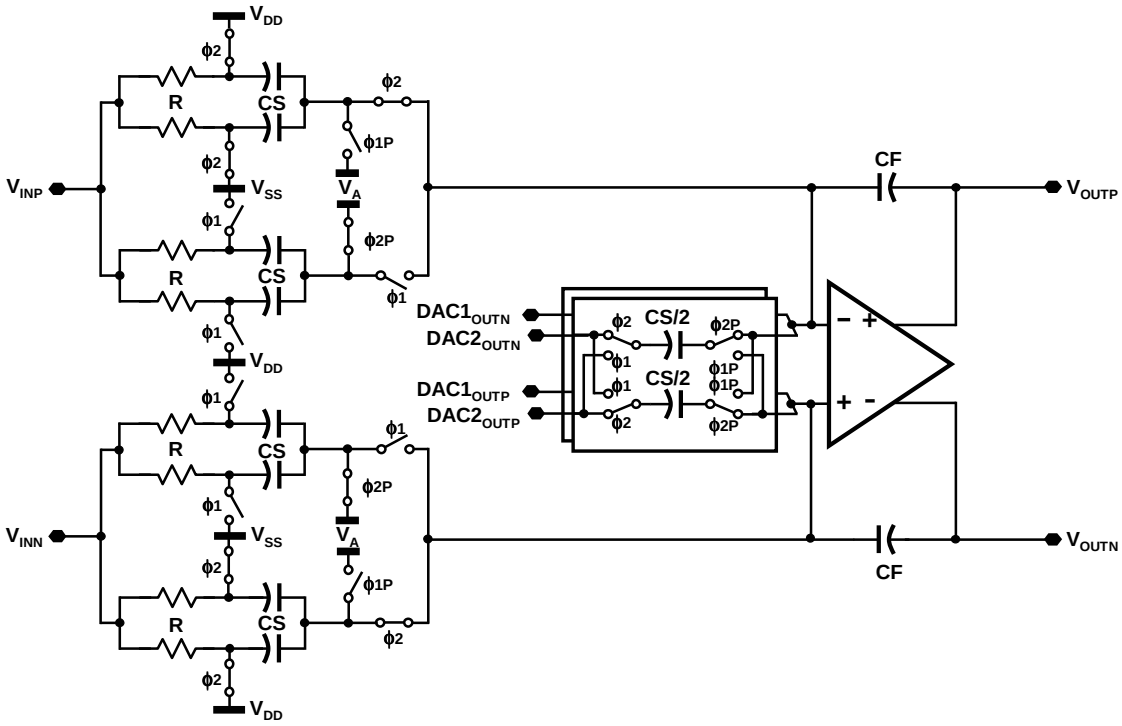



Figure 5.2: The proposed low-voltage DS integrator.

## *5.1.2. Noise Budgeting*

Many performance metrics of data converters such as SNR, SNDR, DR are related to power. Once the maximum signal power was estimated in system level

simulation by deciding the reference voltage level, the allowed total noise power can be calculated based on the desired DR. The total noise power can be expressed as:

$$P_{Ntotal} = P_{NQ} + P_{NAMP} + P_{NkT/C}\,. \tag{5.2}$$

where $P_{Ntotal}$ is the total in-band noise power, $P_{NQ}$ is the quantization in-band noise power, $P_{NAMP}$ is the amplifier in-band noise power, and $P_{NkT/C}$ is in-band kT/C noise power. As described in previous subsection, the quantization noise is already small enough to be ignored. So, the dynamic range can be written as

$$DR = \frac{P_{INMAX}}{P_{Ntotal}} \cong \frac{V_{INMAX}^2}{2}\frac{1}{(P_{NAMP} + P_{NkT/C})} \cong \frac{V_{INMAX}^2}{2(P_{NAMP} + OSR \cdot 2kT/C_S)} \tag{5.3}$$

where $V_{INMAX}$ is the maximum input amplitude of the ADC and $C_S$ is the sampling capacitance of the first integrator. The kT/C noise is easily controlled by sizing the capacitors in the integrators than the amplifier noise. So, the capacitor sizes can be decided after minimizing the amplifiers noise. The amplifier noise has two major sources, thermal noise and flicker noise. The flicker noise in a low-pass DSM is very critical because the noise is dominant at low frequencies. Several techniques to reduce or cancel this low-frequency flicker noise exist, such as correlated double sampling and chopper stabilization techniques. However, these techniques require hard-to-implement low-voltage switched capacitor circuitry. For this reason, the prototype avoided using flicker noise suppression techniques by simply increasing the geometric sizes of the transistors which are the main sources of the noise. Then, the thermal noise is the only dominant source of amplifier noise. The final noise distribution is shown in Fig. 5.3.

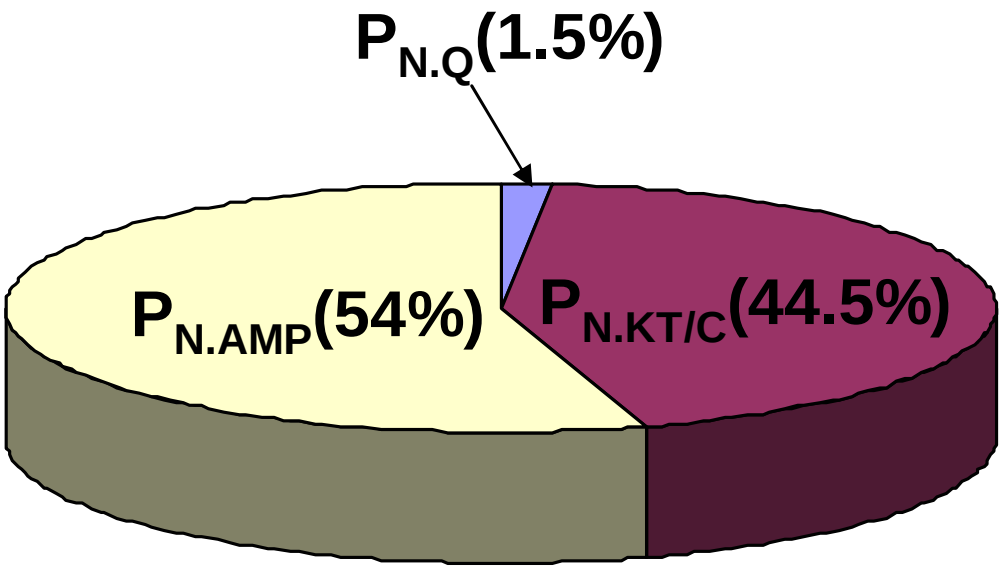
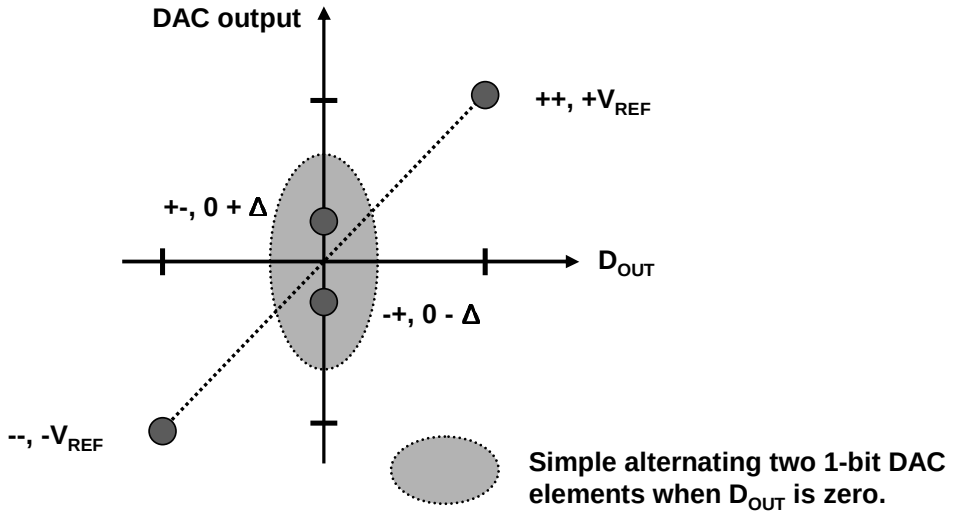



Figure 5.3: The noise distribution of the delta-sigma ADC.

### *5.1.3. A Simple Dynamic Element Matching Scheme for 3-Level Quantizer*

According to Eq. 5.1, using a 3-level (1.5-bit) quantizer and a 3-level DAC can easily improve SQNR by 3dB. However, once the number of the DAC levels is more than two, the DAC is no longer linear. The nonlinear 3-level DAC causes even harmonics of the DSM output in frequency domain without dynamic element matching (DEM) which implies extra hardware cost. However, the 3-level DAC allows the use of a simple DEM scheme suitable for low-voltage operation. In this scheme, the two 1-bit DAC elements are interchanged whenever the delta-sigma ADC output equals the middle code as depicted in Fig. 5.4. The behavioral simulation result with this proposed DEM is almost the same as that for an ideally linear DAC as shown in Fig. 5.5.




**Example)**

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $D_{OUT}$ | 1 | 1 | -1 | -1 | 0 | 0 | 0 | 1 | 0 | -1 | 0 |
| DAC output | $+V_R$ | $+V_R$ | $-V_R$ | $-V_R$ | Δ | -Δ | Δ | $+V_R$ | -Δ | $-V_R$ | Δ |

Figure 5.4: A low-power DEM for 3-level DAC.

### *5.1.4. Behavioral Simulations with Finite Opamp Gain*

A behavioral simulation was done by sweeping the opamp gain from 20dB to infinite. Fig. 5.6 shows the spectra with five opamp gains in the proposed topology. The minimum gain requirement for the opamp is 40dB to make sure the SQNR remains higher than 100dB. But this result is based only on noise shaping considerations. If more realistic factors such as the amplifier's distortion are considered, higher opamp gain is needed to achieve the required performance.

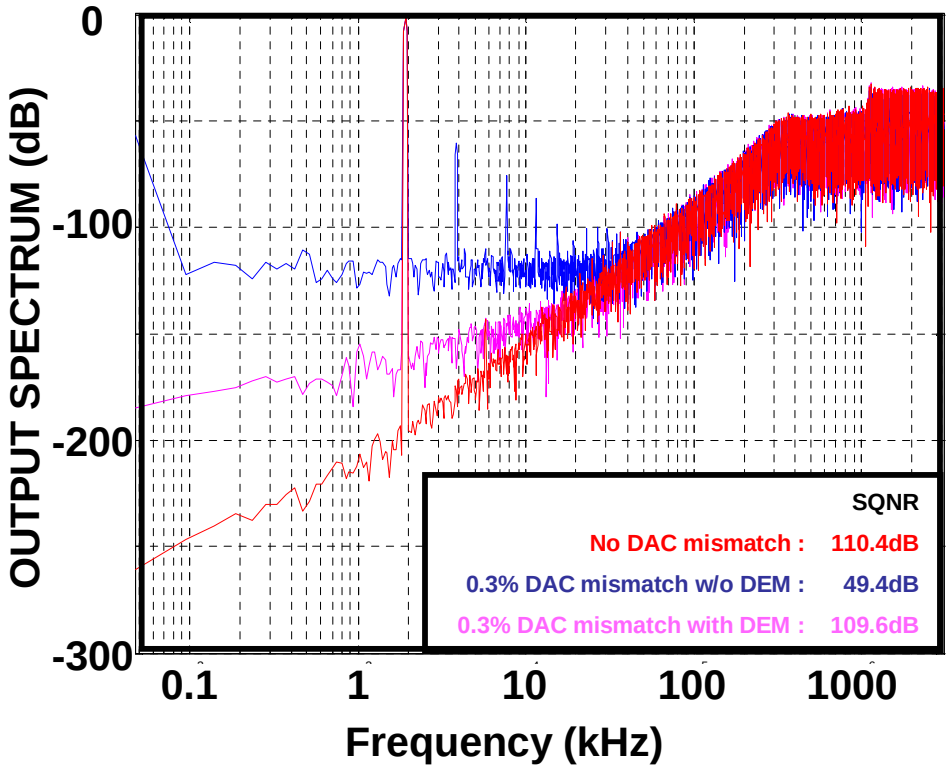



Figure 5.5: Behavioral simulation results with ideal DAC, nonideal DAC without DEM, and nonideal DAC with DEM.

### *5.1.5. Low-Voltage Fully-Differential Opamp Design*

Pseudo-differential opamps are frequently used in low-voltage applications to overcome the difficulty of realizing the low-voltage common-mode feedback (CMFB) required for a fully differential structure. However, the pseudo-differential configuration suffers from several drawbacks, including increased noise, higher power consumption, larger area, and reduced PSRR/CMRR. In order to avoid these issues, a fully-differential amplifier with a low-voltage CMFB was employed. The amplifier consists of a folded-cascode first stage for low input common-mode voltage, and a common-source second stage for wide output swing. As shown in

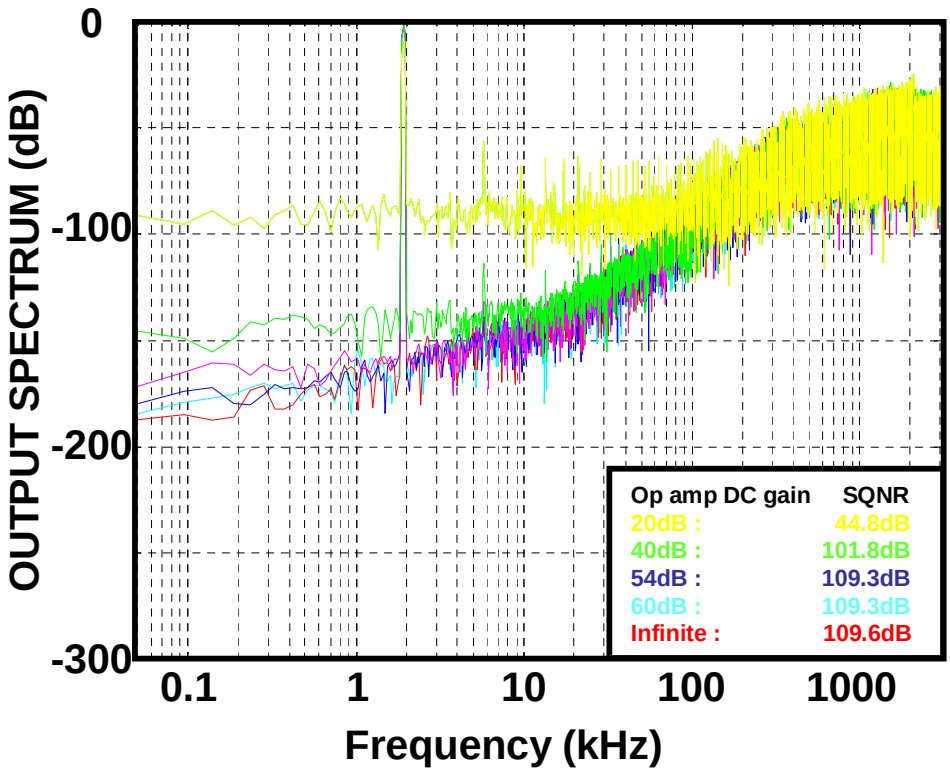



Figure 5.6: Behavioral simulation results with different opamp gains.

Fig. 5.7, an additional current source is used to shift the output common-mode level from $V_{CM} = V_{DD}/2$ to within the input common-mode range of the folded-cascode single-stage CMFB amp.

### *5.1.6. Low-Voltage Comparator Design*

Fig. 5.8 illustrates the circuit diagram of the low-voltage DS comparator used in the 1.5-bit quantizer. It consists of a split switched-RC input sampling network, a preamplifier A1 and a level-shifting amplifier A2 along with the two comparator

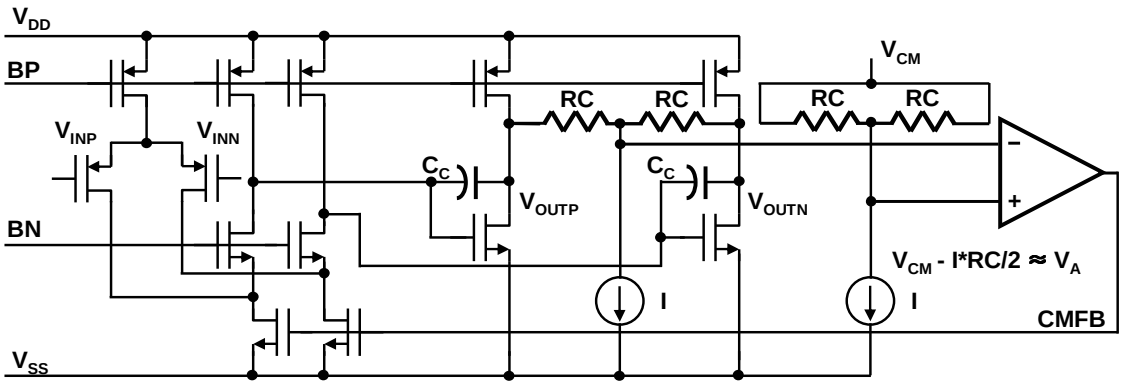



Figure 5.7: An opamp with proposed low-voltage CMFB.

latches L1 and L2. The decision levels are set by appropriately scaled capacitors C1 and C2, and the offset is canceled at the output of the preamplifier A1. The input common-mode level of A2 can be set as low as ground potential. This comparator can be used to realize a low-voltage multi-level quantizer without needing floating switches. Unlike the existing low-voltage comparator design in [7], the proposed comparator can save passive components, make the circuit simpler and less noisy by removing the summing node and an additional branch for the reference voltage level injection.

### *5.1.7. Experimental Results*

The ADC was fabricated in Samsung Electronics 0.13$\mu$m CMOS technology. The measured output spectrum with a -6dBFS 1-kHz sine input signal and 0.9V supply voltage is shown in Fig. 5.9. The measured SNR and SNDR versus input signal level characteristics are shown in Fig. 5.10. Fig. 5.11 shows that the proposed

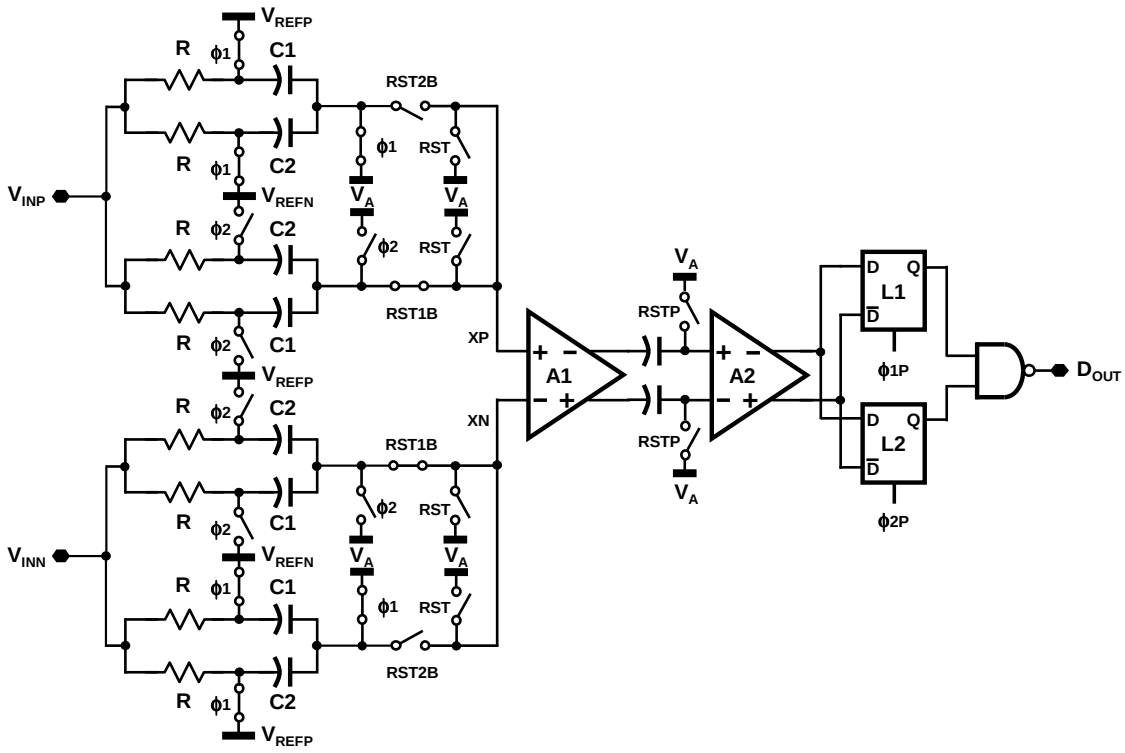



Figure 5.8: The proposed low-voltage comparator.

DEM works well and contributes to improved output linearity. The ADC can operate with supply voltages with a 0.65V to 1.5V with minimal performance degradation as depicted in Fig. 5.12. The measured performance summary is presented in Table 5.2. This prototype achieves 91dB SNR, 89dB SNDR and 92dB dynamic range with a 0.9V supply voltage. With a 0.65V supply, 83dB SNR, 79dB SNDR and 87dB dynamic range were measured. The chip micrograph is shown in Fig. 5.13. The active die area is 1.6 x 0.9 $mm^2$.

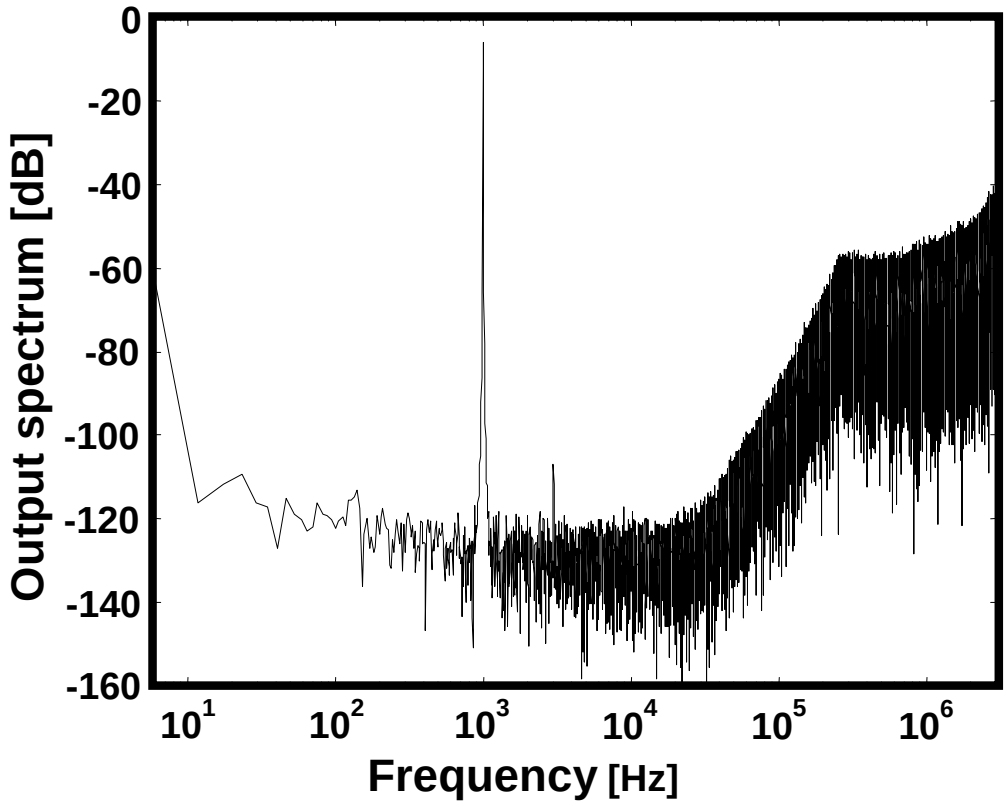



Figure 5.9: Measured output spectrum.

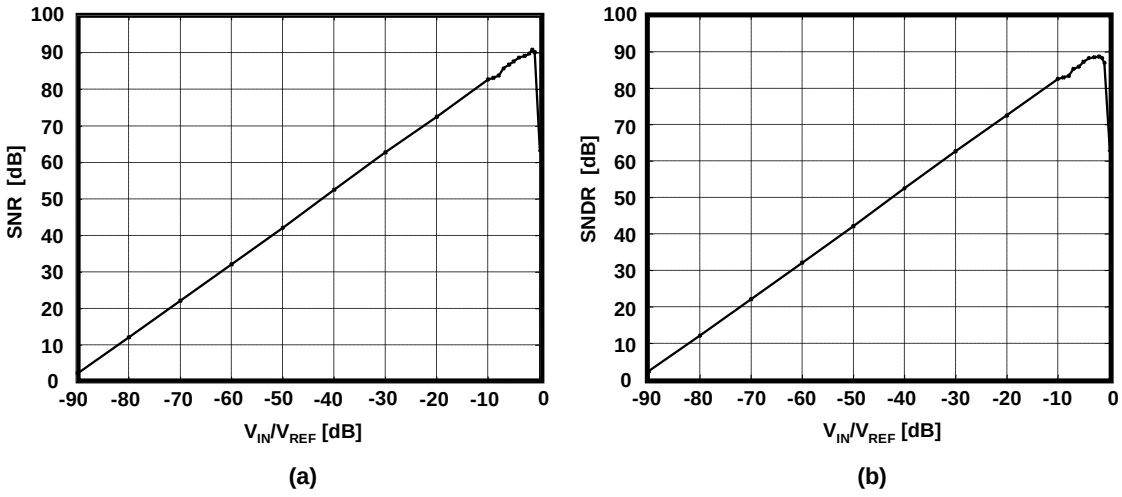



Figure 5.10: (a) SNR vs. input level; (b) SNDR vs. input level for a 0.9 V supply voltage.

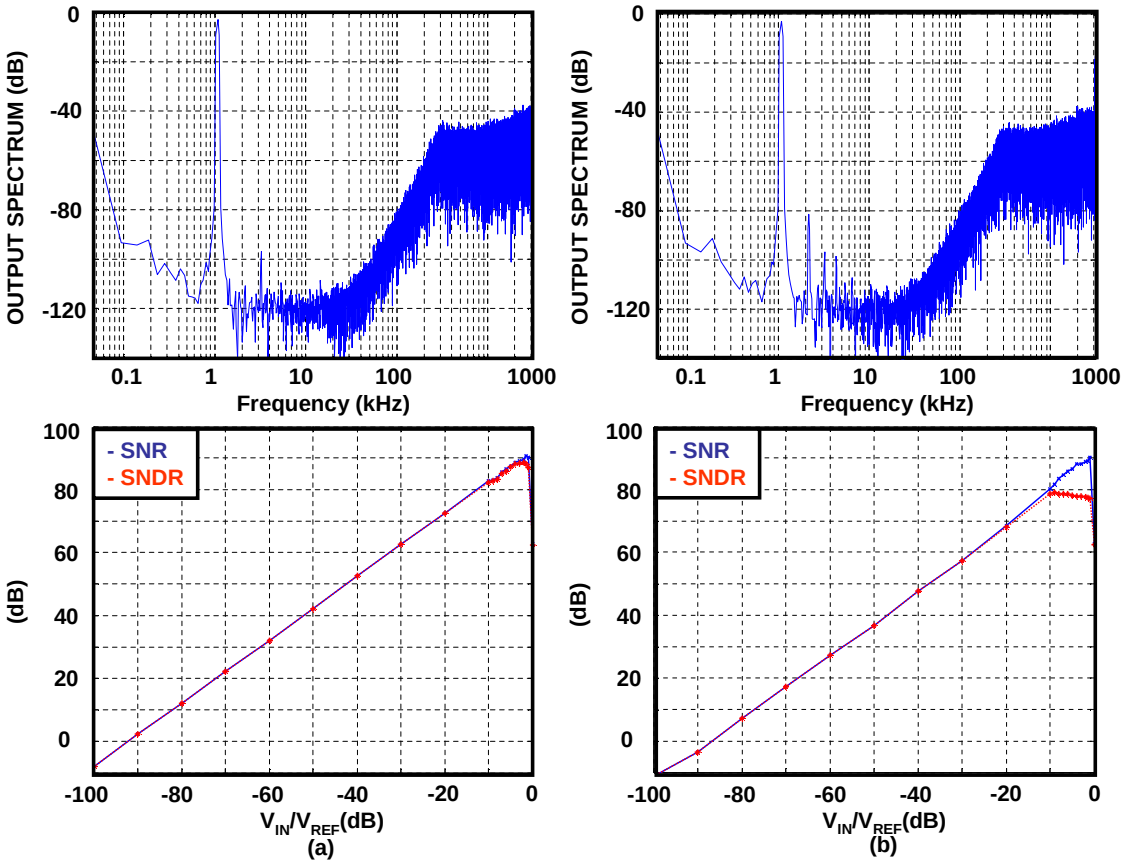



Figure 5.11: Output spectra and SNR/SNDR vs. input level plots (a) with DEM and (b) without DEM.

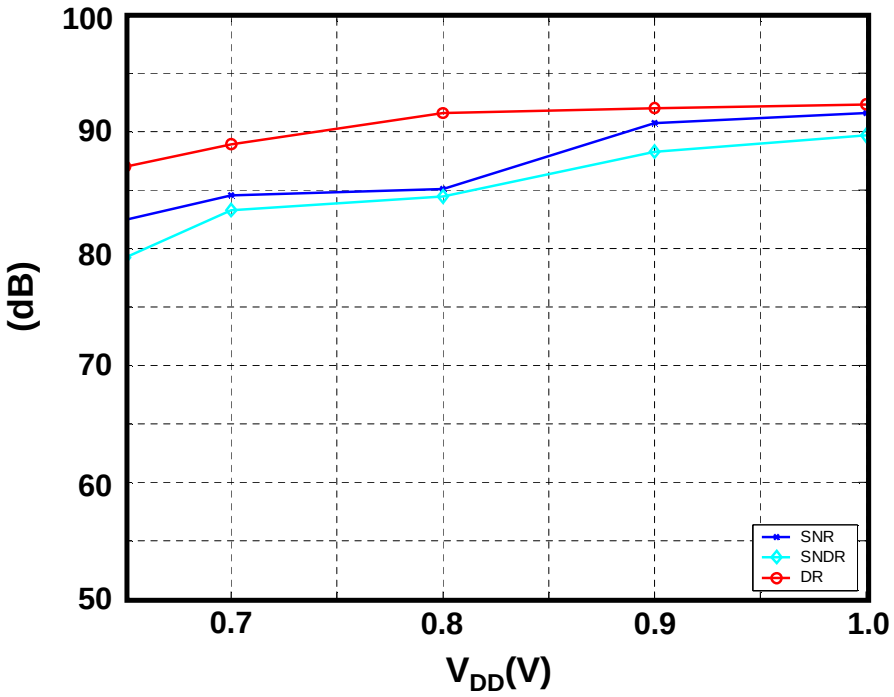



Figure 5.12: SNR, SNDR, and DR vs. $V_{DD}$ plot.

Table 5.2: Measured performance summary of the audio delta-sigma ADC

| | | |
|---|---|---|
| Power supply voltage | 0.65 V | 0.9 V |
| Power consumption | 1.1 mW | 1.5 mW |
| Input range | 0.87 $V_{PP}$ (diff.) | 1.1 $V_{PP}$ (diff.) |
| Peak SNR | 83 dB | 91 dB |
| Peak SNDR | 79 dB | 89 dB |
| Dynamic range | 87 dB | 92 dB |
| Signal bandwidth | 24 kHz | |
| Sampling frequency | 6.144 MHz | |
| Clock frequency | 3.072 MHz | |
| Oversampling ratio | 128 | |
| Active die area | 1.6 X 0.9 $mm^2$ | |
| Technology | 0.13µm CMOS | |

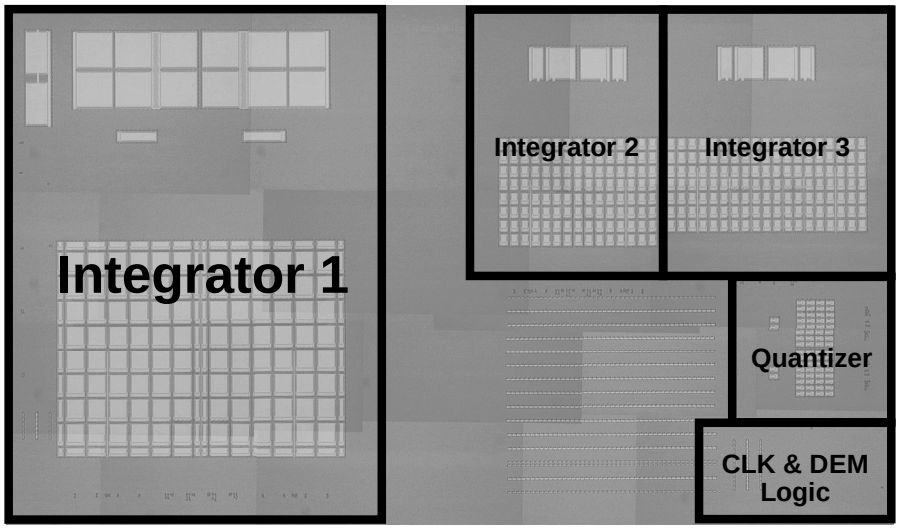



Figure 5.13: Chip photograph of the delta-sigma audio ADC.

## 5.2. A 10MS/s 11-bit 0.19mm$^2$ Algorithmic ADC with Improved Clocking

Pipelined ADCs are used in medium-speed to high-speed applications such as video and communication systems. It is beneficial to replace these pipelined ADCs with algorithmic ADCs which have advantages of low power and small chip area. However, algorithmic ADCs are inherently slower due to the cyclic nature of their conversion process. In an algorithmic ADC with two MDACs, two bits are resolved each clock cycle - one bit in each phase - and hence the total conversion time for N-bit overall resolution is N/2-clock cycles. In Sec. 4.2., an improved clocking scheme that speeds-up the conversion rate of the algorithmic ADC with minimal area and power overhead was proposed. The proposed ADC employs op-amp sharing to further reduce power. Techniques to suppress memory effect and DC offset are also presented.

### *5.2.1. Proposed Architecture with Improved Clocking Scheme and Amplifier Sharing*

The block diagram of the proposed algorithmic ADC is shown in Fig. 5.14. It consists of two 1.5-bit MDACs, 1.5-bit sub-ADCs, digital correction logic, a DLL circuit, and clock generator. The conventional algorithmic architecture consists of a SHA, an MDAC, and a sub-ADC as described in Sec. 3.3. [19]. The general SHA in an algorithmic ADC has two main functions. One is the sampling of the analog input signal and the other is the sampling of the MDAC output to transfer it to the MDAC input, recursively, for the next conversion bit stage in the same MDAC. The

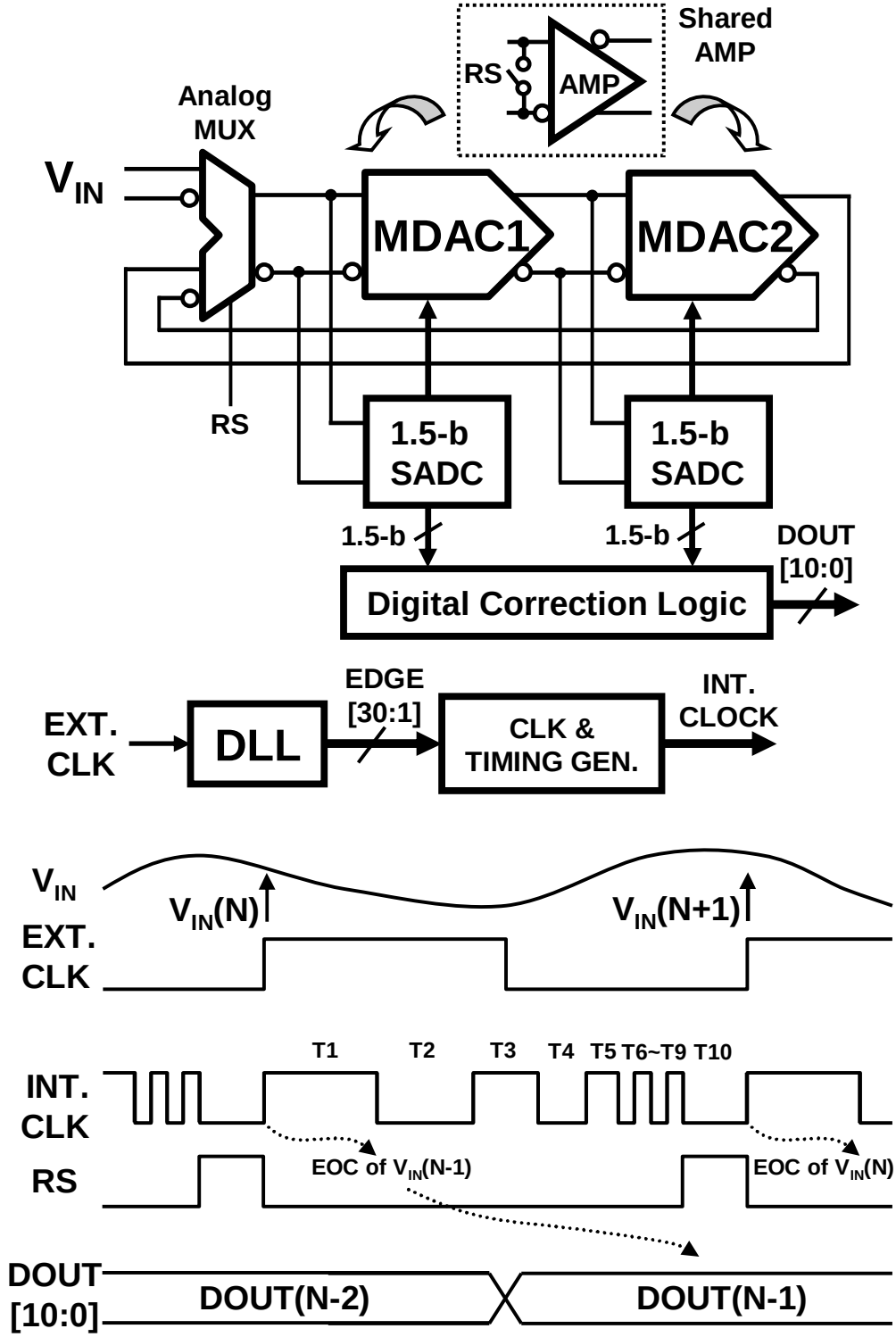



Figure 5.14: Block diagram of the proposed algorithmic ADC.

latter, required only for the recyclic attribute of the algorithmic ADC timing, does not have any effect on the conversion speed. In this prototype design the redundant block SHA was removed, and an extra set of an MDAC and a sub-ADC were added. This doubles the conversion speed compared with conventional architectures [19, 22]. In other words, the required operating speed of analog blocks is reduced by half, resulting in smaller chip area and power consumption in spite of the additional set of a MDAC and sub-ADC. In addition, only one amplifier is needed for the two MDAC operations because the amplifier sharing techniques described in Sec. 2.3.2. are employed for further power reduction. Therefore, the additional MDAC does not mean more active devices such as amplifiers. A DLL is used to synthesize an internal clock from an external clock. This internal clock relaxes the MSB conversion time, and progressively reduces the following bit conversion times. Note that unlike in a conventional algorithmic ADC, the external clock frequency is the same as the data conversion rate and that enables the algorithmic ADC operation to be same as for a full flash type ADC with minimum throughput, one external clock period.

When the external clock is at rising edge, the analog input $V_{IN}$ is sampled by MDAC1 and the conversion starts. Each set of an MDAC and a sub-ADC generate the Nth most-significant-bit (MSB) digital data in the clock period TN. Finally, the complete 11bits (2047-levels) are acquired with the next rising edge of the external clock after 5 cycles of the internal clock, which is 1 cycle of the external clock. The extra 0.5-bit in each stage is used as a redundancy for digital correction.

### 5.2.2. The Proposed Memory Effect Suppression Technique

Amplifier sharing between the two MDACs of the algorithmic ADC reduces power consumption. However, amplifier sharing has two inherent drawbacks. First, since the input node of the amplifier is never reset, the current MDAC output depends on the previous residue, thus degrading the linearity of the overall converter. This is often referred to as *memory effect*. The memory effect between the last least significant bit (LSB) conversion stage and the MSB conversion stage is particularly detrimental. This memory effect is suppressed by resetting the amplifier input before sampling the ADC input. The timing for the reset signal (RS) is easily made as shown in Fig. 5.14 because MDACs do nothing in the clock phase T10 for the LSB conversion step.

### 5.2.3. The Proposed DC Offset Cancelation Technique

Amplifier sharing techniques exacerbate the ADC offset since the amplifier is active in every clock phase and the amplifier DC offset has the same polarity and amount in every conversion step. In the proposed algorithmic ADC architecture, only one opamp is used for two MDACs in the amplifier sharing technique and every stage has 1.5-bit conversion step which has a interstage gain of 2. Therefore, the output referred DC offset, $V_{OUT,OS}$ without offset cancelation technique can be written as:

$$V_{OUT,OS} = 2^{N-1}V_{OS} + 2^{N-2}V_{OS} + \cdots + 2V_{OS} = (2^N - 2)V_{OS} \cong 2^N V_{OS}\,. \quad (5.4)$$

where $V_{OS}$ is the MDAC DC offset voltage, and N is the number of ADC resolution bit. In this prototype design, the feedback signal polarity inverting (FSPI) technique used in [20] to reduce the DC offset is extended to an algorithmic ADC as shown in Fig. 5.16 (a). The feedback signal polarity is inverted between the first and the second stage and the same polarity is kept from the second to the last stage. While the original FSPI technique reduces the offset by one third, the improved FSPI eliminates the output referred offset. The output referred DC offset, $V_{OUT,OS}$ with this improved FSPI can be written as:

$$V_{OUT,OS} = 2^{N-1}V_{OS} - 2^{N-2}V_{OS} - \cdots - 2V_{OS} = 2V_{OS}\,. \tag{5.5}$$

The behavioral simulation results are shown in Fig. 5.15. The measured output offset is within +2.5/-3.5 LSB as shown in Fig. 5.16(b).

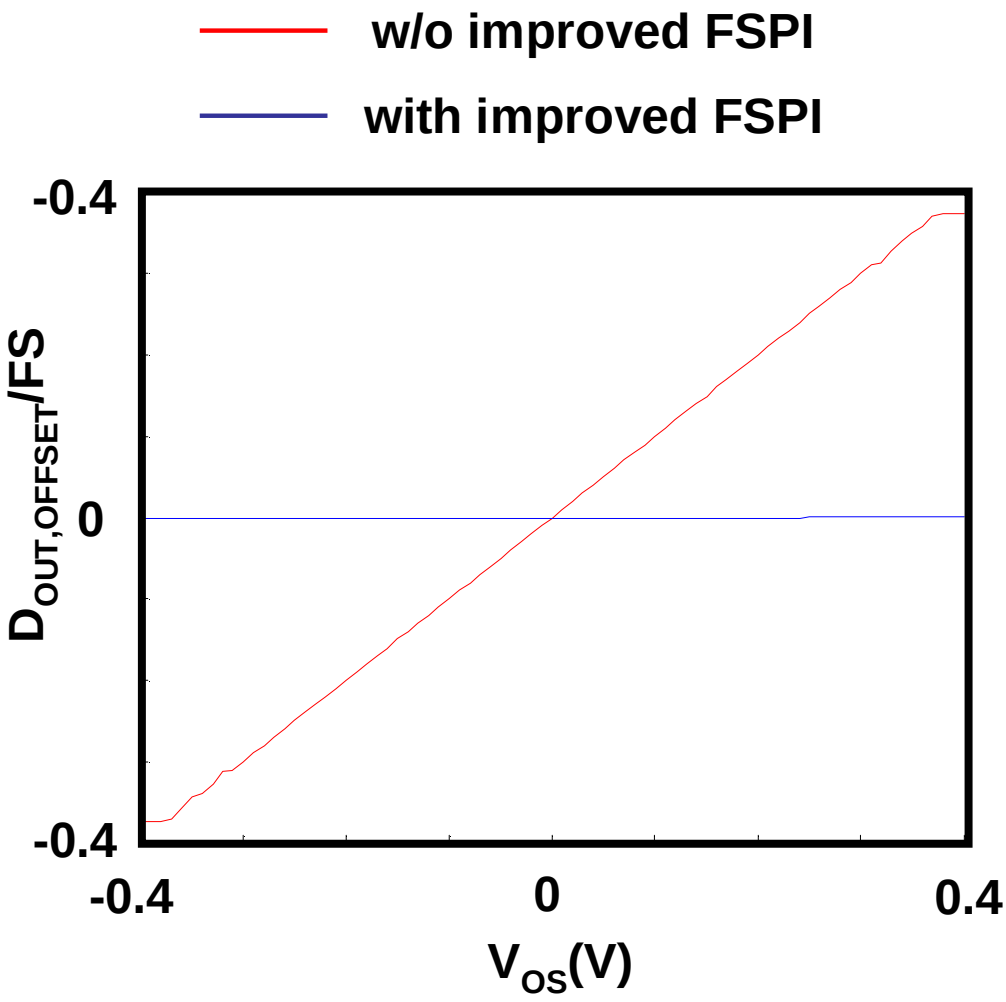



Figure 5.15: Digital output offset vs. MDAC DC offset plot from behavioral simulation.

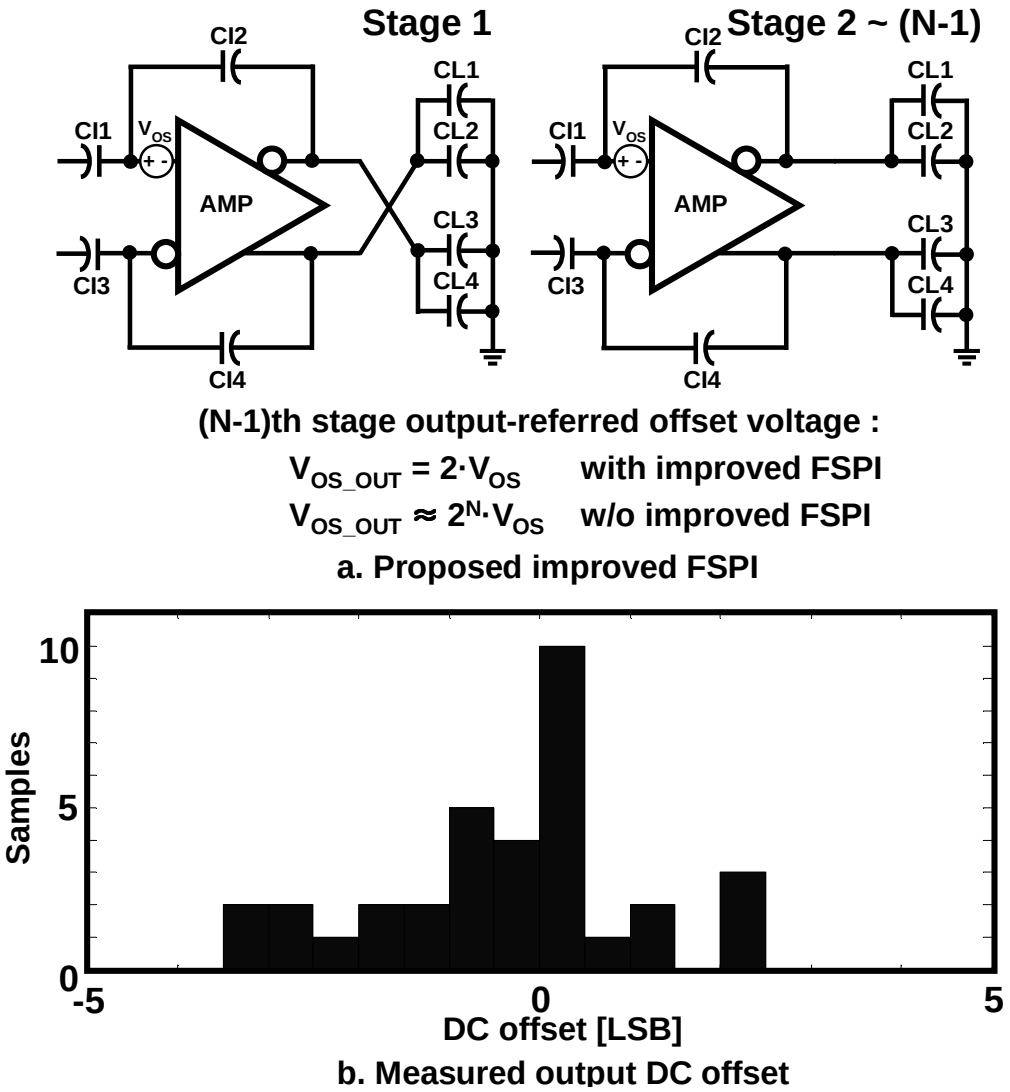



Figure 5.16: Improved FSPI technique and measured ADC output DC offset.

### *5.2.4. Opamp Design*

The opamp which is shared by two MDACs is depicted in Fig. 5.17. Two-stage opamp is employed for obtaining proper gain for 11-bit ADC. The amplifier consists of a telescopic first stage for high gain and simple CMFB, and a differential stage for proper output swing and high CMFB gain. The differential amplifier output is reset during the RS phase when the amplifier input is reset. This reset can minimize the output slewing time and memory effect.

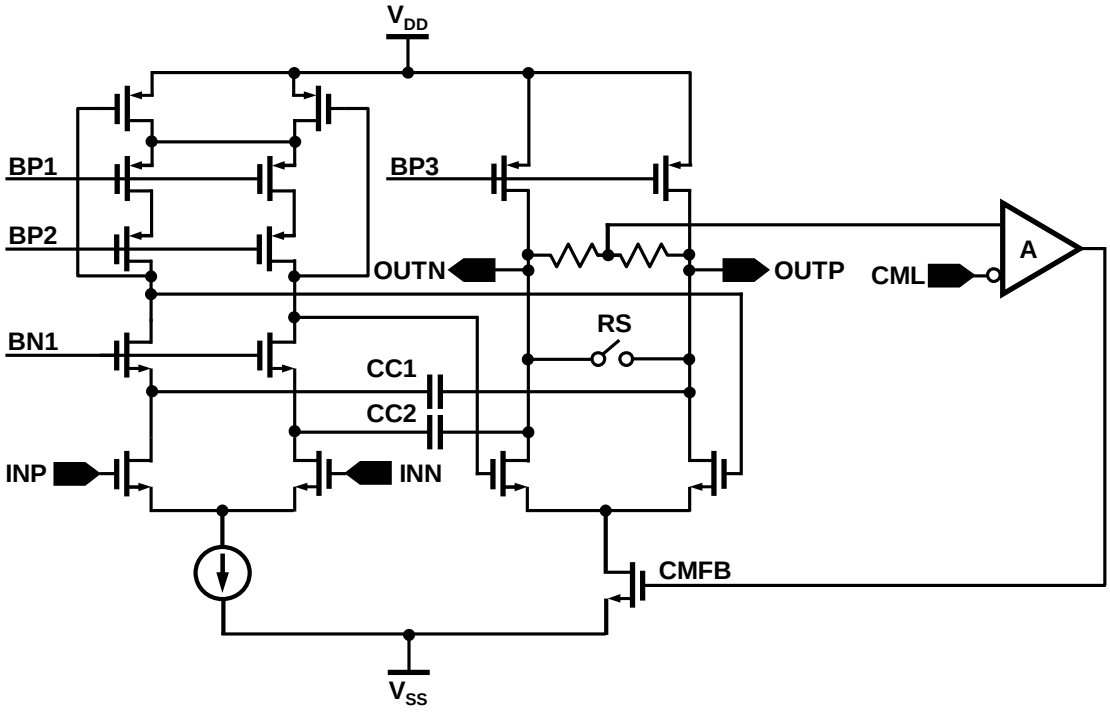



Figure 5.17: The shared opamp for two MDACs.

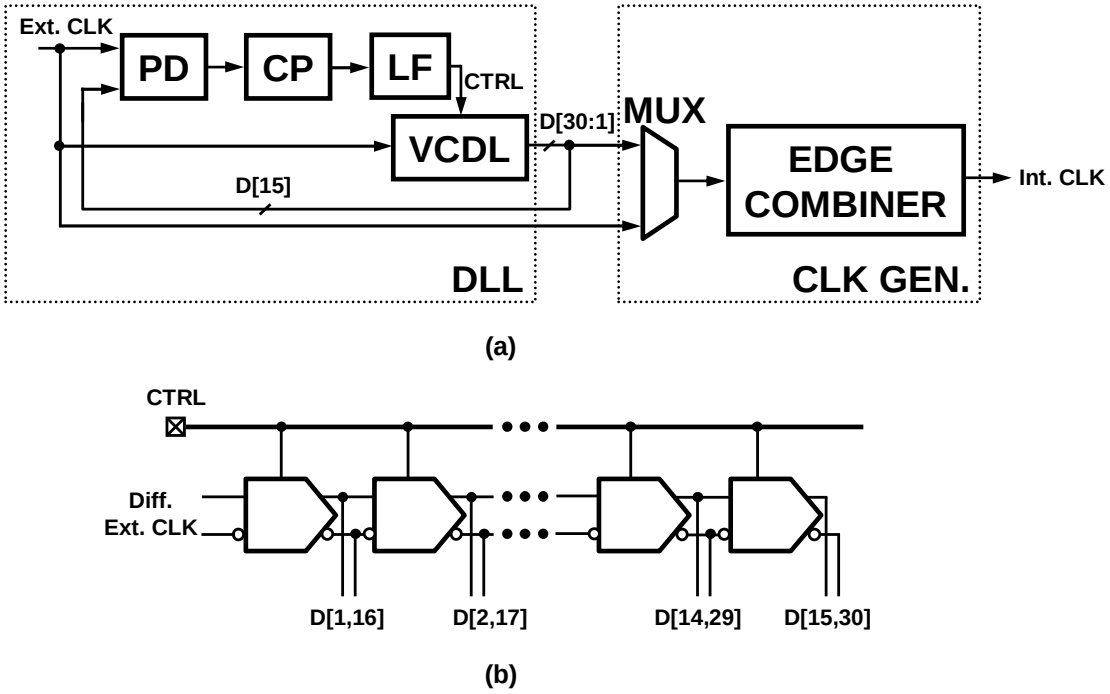



Figure 5.18: (a)A block diagram of DLL and clock generator and (b)the VCDL circuit of the DLL.

## *5.2.5. DLL Design*

As explained in Sec. 4.2.2., a low-cost DLL or PLL is needed to generate the improved clock signal internally. DLL is preferable because its circuitry is simpler, has small area, and consumes low power. A block diagram of the DLL and clock generator circuit is shown in Fig. 5.18 (a). The voltage controlled delay line (VCDL) circuit in the DLL is illustrated in Fig. 5.18. The VCDL block employed the delay cell in [23] which has a very wide delay range. The low-cost DLL generates thirty clock edges from an external clock signal, and the edge combiner synthesizes the internal clock signal for the proposed clocking scheme. To reduce hardware overhead, the DLL was designed for low-power and small area. System-on-chip

(SOC) applications usually include DLL or PLL as a sub-block and can be reused instead of building a new DLL block just for the ADC.

### *5.2.6. Experimental Results*

The measured spurious-free dynamic range (SFDR) vs. conversion rate is shown in Fig. 5.19. The SFDR with a conventional clock degrades with an increase in conversion rate, while the proposed clocking scheme maintains almost the same SFDR from 9Ms/s to 16Ms/s conversion rates. Fig. 5.20 shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL) at a 10MS/s conversion rate, where the peak DNL is +0.85/-0.9LSB, and the peak INL is +3/-3.5LSB. The measured output spectrum with 1-MHz sine input signal and 10Ms/s conversion rate is shown in Fig. 5.21. The measured performance summary is presented in Table. 5.3. The chip micrograph is shown in Fig. 5.22.

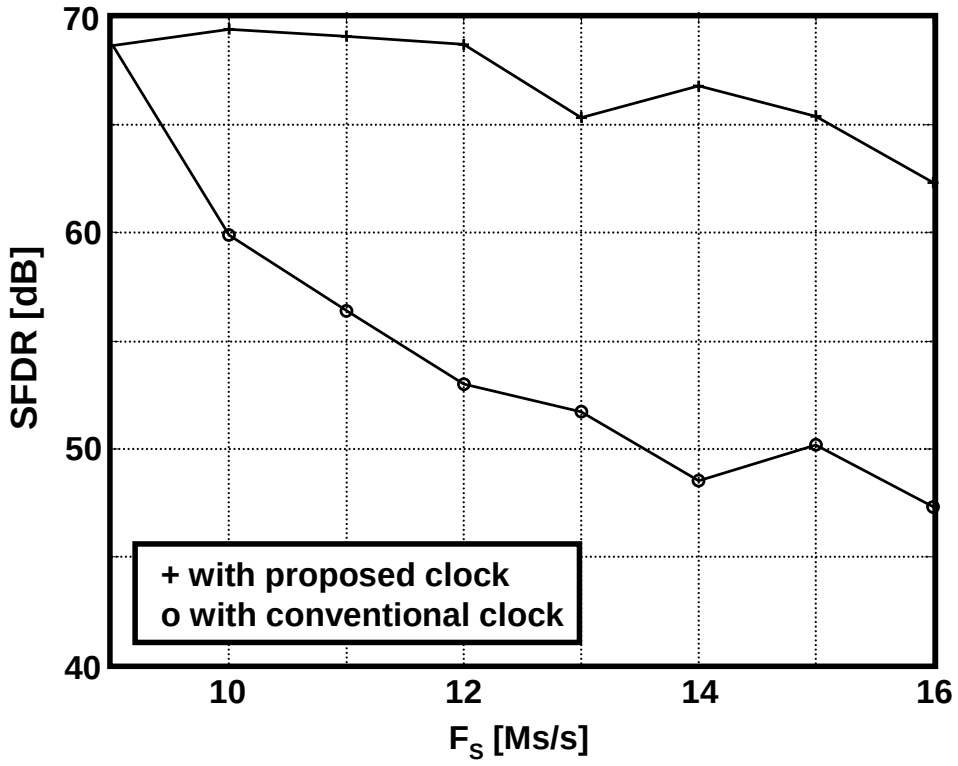



Figure 5.19: The measured SFDR vs. conversion rate plot.

Table 5.3: Measured performance summary of the algorithmic ADC

| | |
|---|---|
| **Resolution** | **11-bit** |
| **Conversion Rate** | **10 MSPS** |
| **Technology** | **0.13 um Thick Gate-Oxide CMOS** |
| **Supply Voltage** | **3V** |
| **Power Consumption** | **ADC core : 10.5mW DLL : 4.5 mW** |
| **SFDR/SNR/SNDR** | **69dB / 58dB / 56dB** |
| **DNL/INL** | **0.9 LSB / 3.5 LSB** |
| **Active Die Area** | **ADC core : 0.19 $mm^2$ ,DLL : 0.05 $mm^2$** |

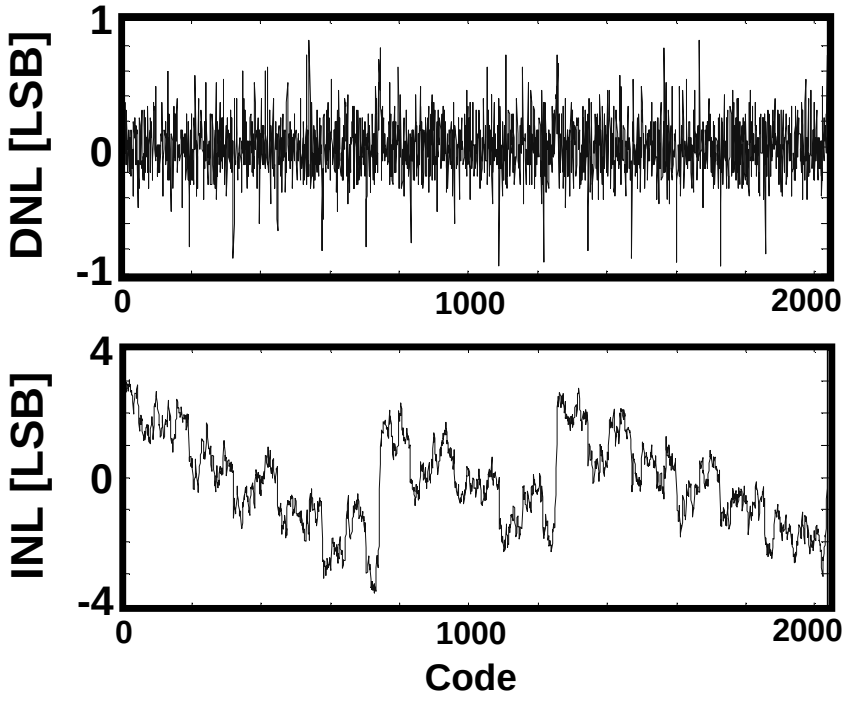



Figure 5.20: Measured nonlinearity.

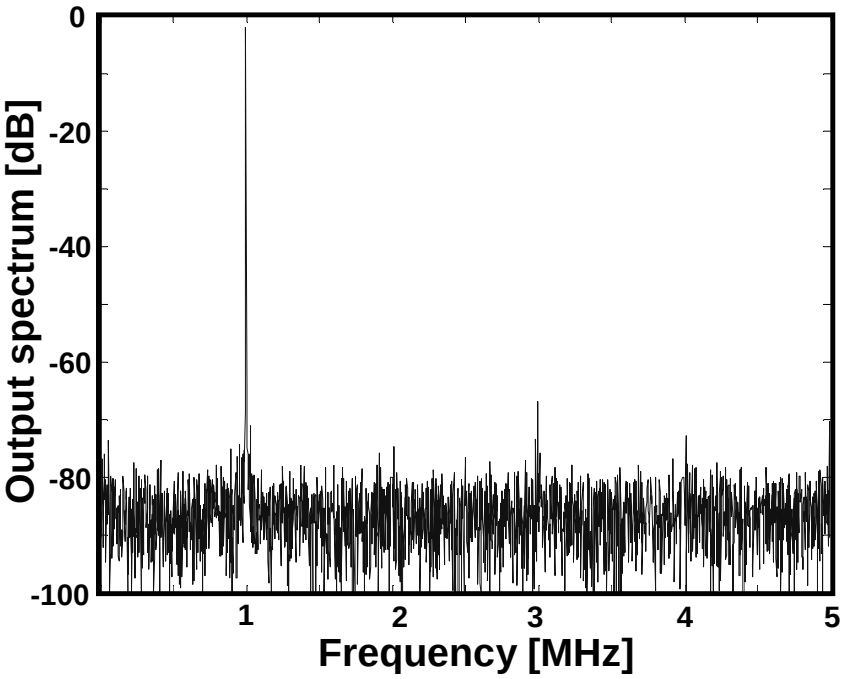



Figure 5.21: Measured output spectrum.

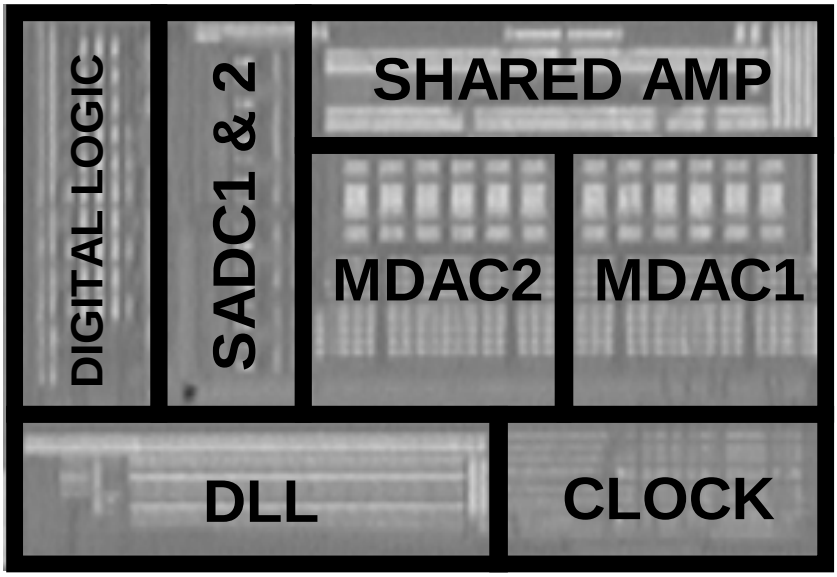



Figure 5.22: Chip photograph of the algorithmic ADC.

# CHAPTER 6. CONCLUSION

Two low-power design techniques for low-voltage ADCs are proposed. One is a low-voltage DS technique which is combined with switched-RC circuitry and the other is an improved clocking scheme with on-chip DLL for algorithmic ADCs. Both power reduction techniques are compatible with low-voltage portable applications.

The low-voltage DS technique for delta-sigma ADCs increases the OSR by two compared to conventional design, without extra power consumption and without increasing the sampling clock frequency. In other words, this technique implies power reduction for achieving a given performance. A prototype, 0.9V 92dB delta-sigma audio ADC was implemented in a 0.13$\mu$m Samsung Electronics CMOS process to prove the validity of the proposed technique. The measured results verify that the effectiveness of the proposed technique achieves low-voltage, low-power, and high performance. The prototype IC includes opamps with new CMFB circuits, a novel low-voltage quantizer circuit, and a low-power DEM for 3-level quantizer.

The improved clocking scheme overcomes the speed limitations of algorithmic ADCs without any change of the ADC core circuits. In other words, the technique implies effective power reduction of the algorithmic ADC to achieve the given conversion speed. A 10MS/s 11-b 0.19mm$^2$ algorithmic ADC is implemented in a thick-oxide gate 0.13$\mu$m Samsung Electronics CMOS process to prove the proposed technique. The improved algorithmic ADC scheme enables that the use of algorithmic ADC architecture for higher conversion speed applications (10MS/s-

15Ms/s). The prototype IC includes opamp sharing, a memory effect suppression technique, and DC offset cancelation techniques.

All of the proposed techniques are very simple, practical, effective, and easy to implement.

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